Chapter 1

Introducing Optical Lithography

Lithography creates a resist image on the wafer. The subsequent etching, lift off, or ion implantation process is masked by the resist image at the areas dictated by the lithography mask. Hence, the thin film material on the wafer is selectively removed, built up, or its characteristics are selectively altered. Replicating the mask pattern produces the resist image, except when mask making or direct writing on a wafer. Figure 1.1 depicts the mask replication process with an imaging lens. The condenser collects light from the source and illuminates the mask pattern. It passes through the imaging lens to form an aerial image to selectively expose the resist. After development, the resist image (as shown) is produced. Figure 1.2 illustrates various forms of image transfer from the resist to the underlying thin film. The film can be isotropically or anisotropically etched, lifted off, plated, or implanted, using the patterned resist as the mask. Detailed descriptions of these transfer processes are given in Chapter 3.

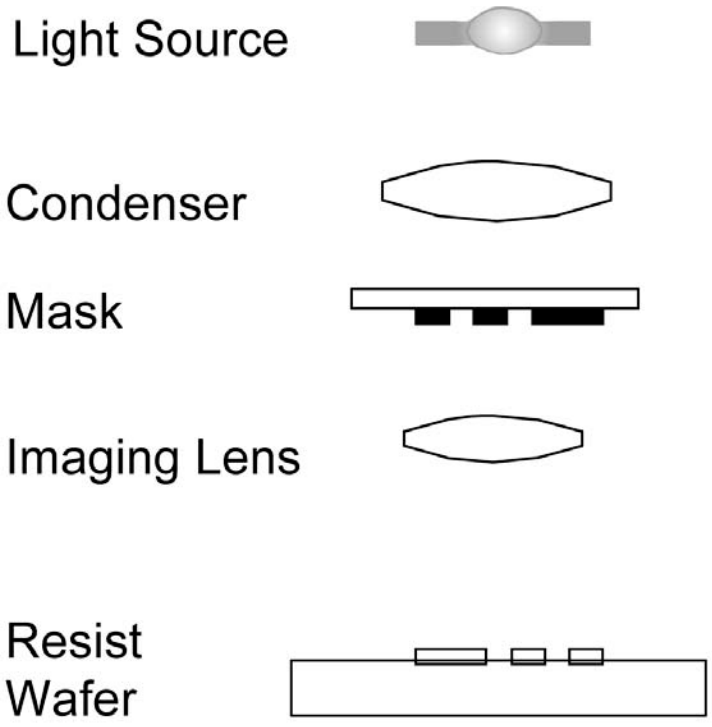

Figure 1.1 Optical lithography replicates the mask pattern through an imaging lens.

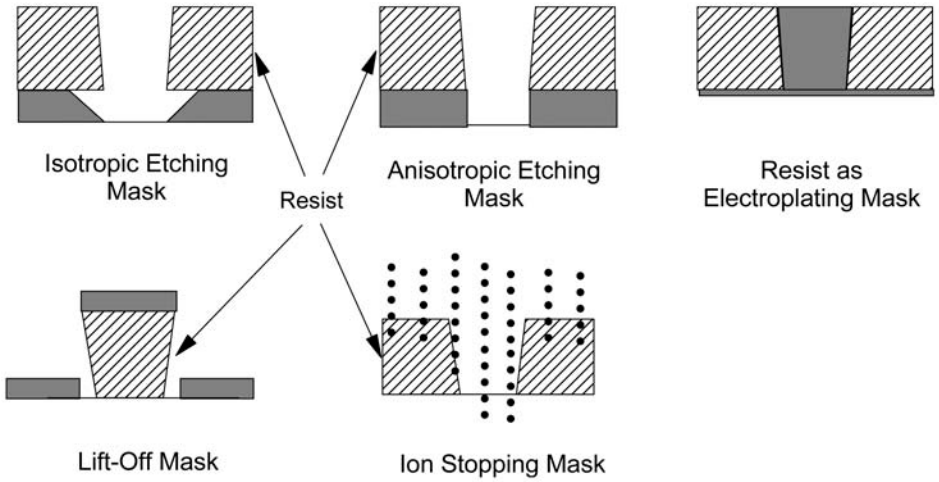

Figure 1.2 Exposed resist image transferred to the underlying thin film by isotropic etching, anisotropic etching, electroplating, lift off, and ion implant.

The image formation process is facilitated with an information-carrying beam consisting of photons, electrons, or ions. Optical lithography uses photons to carry out this process. Photons with energy ranging from visible to x-ray wavelengths can be used. However, in this book, the wavelengths range between 157 and 436 nm. A majority of these wavelengths is already fully employed in manufacturing semiconductor integrated circuits. The others have been worked on. An outlook is given in Chapter 8 on the prospect of using even shorter wavelengths to produce future circuits.

1.2 The Role of Lithography in Integrated Circuit Fabrication

Lithography is an important part of semiconductor manufacturing technology because it is needed for every masking level. In a typical 0.13-μm CMOS integrated circuit fabrication run with four metal layers, there are more than 30 masking levels using 474 processing steps, in which 212 steps are related to lithographic exposure, and 105 steps are related to pattern transfer using a resist image. Relevant steps are listed as follows.

Lithography exposure–related:

- Wafer cleaning and priming to improve adhesion
- Application of antireflection coating before and/or after resist coating
- Resist coating
- Post-application bakes
- Exposure/alignment
- Post-exposure bake

- Resist development
- Resist hardening
- Critical dimension (CD) monitoring
- Alignment monitoring
- Selective removal of antireflection coating
- Stripping of the antireflection coating and the resist

Pattern transfer–related:

- Etching
- Ion implantation
- CD monitoring
- Surface preparation
- Electroplating

Note that the actual sequence and number of processing steps may vary depending on the particular masking level. For example, the bottom antireflection coating at the wafer-resist interface is deposited on the wafer prior to priming and resist coating, if it is inorganic. Otherwise, it is applied between the priming and resist-coating steps. In the latter case, an extra baking step is required for the bottom antireflection coating. A top antireflection coating may be applied after the resist coating and baking, with or without the bottom antireflection coating. Another baking step follows the application of the top antireflection coating. A block diagram showing a possible sequence and relation of these processing steps is shown in Figure 1.3.

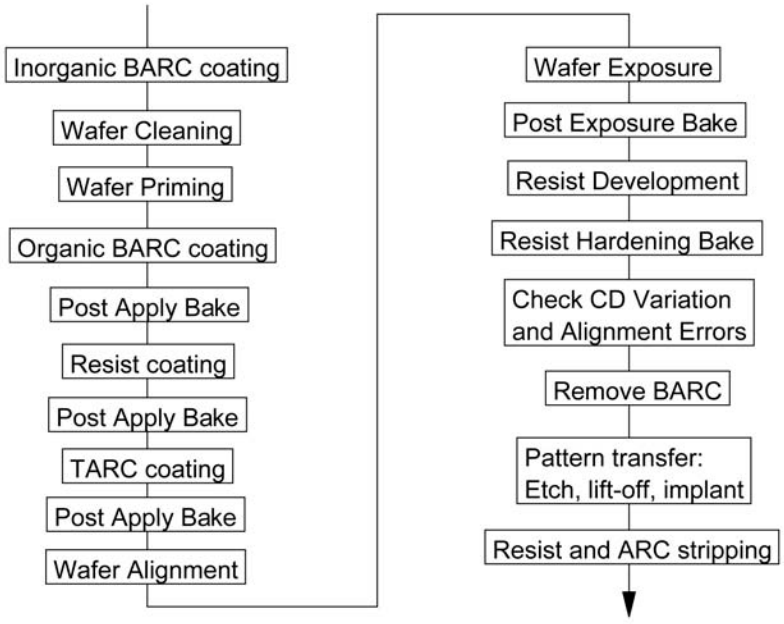

Figure 1.3 Block diagram of lithography processing steps.

Lithography is important not only because it is needed for all masking levels. It is often the limiting factor of entering the next technology node. For every node, the minimum feature sizes and their separations are reduced by a factor of √2. Therefore, the succeeding generation to 1-μm lithography is 0.7 μm, followed with 0.5 μm, 0.35 μm, 0.25 μm, 0.18 μm, 0.13 μm, 90 nm, 65 nm, 45 nm, 32 nm, 22 nm, etc., necessitating improvements in resolution and overlay accuracy that call for many of the following improvements: numerical aperture (NA) increased wavelength reduction, suppression of reflections, better resists, better masks, higher stepping accuracy, higher-precision alignment, less lens distortion, better wafer flatness, and many others. These will be discussed in detail in the following chapters.

1.3 The Goal of Lithography

In order to make the circuit usable, the features fabricated on it must meet certain criteria. The most important one is edge position control. The location of any given edge of a feature on the chip has to be within a given tolerance from a nominal position. When the edge meets this requirement, both the linewidth and the overlay controls have been maintained. This is illustrated in Figure 1.4, where each of the six edges of the L-shaped feature has to fit within the six windows surrounding the edges. The nominal position, represented by the centerline, is where the edge ideally should be. Feature size or feature placement contributes to deviation from the ideal edge positions. Despite this, it is convenient to separately deal with feature size control and feature placement; the combination of them has to meet the ultimate edge placement requirement.

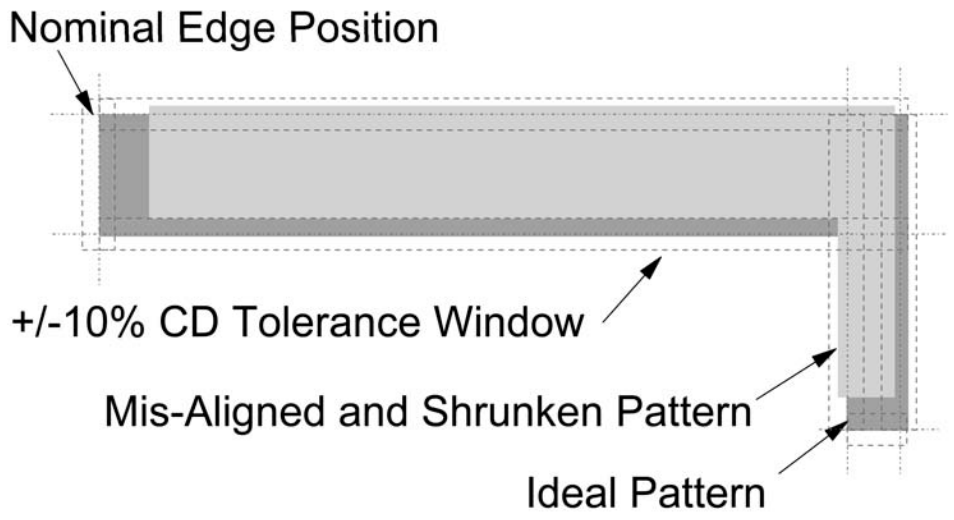

Figure 1.4 Edge placement tolerance.

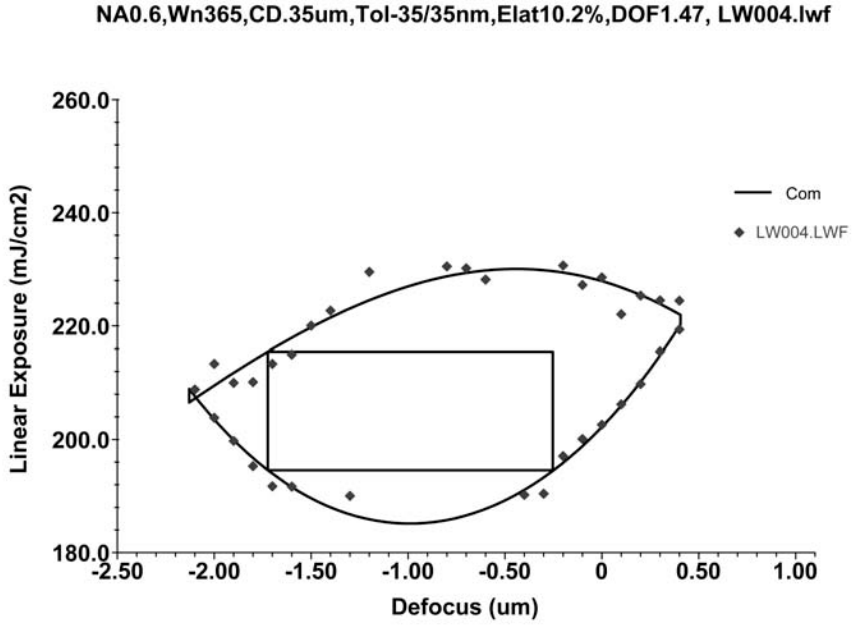

Figure 1.5 A typical E-D window in an E-D tree.

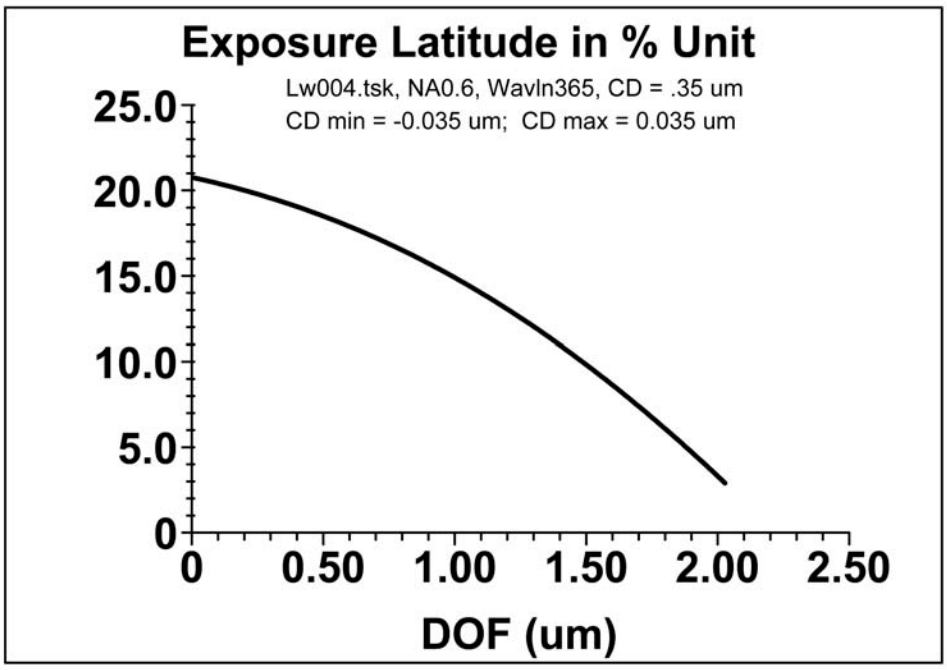

Figure 1.6 Exposure latitude versus DOF tradeoff curve.

1.4 The Meter of Lithography

Following the goal above, a measure of success lies in the size of the process window in feature size and placement controls that keep a given feature edge within its tolerance. The feature size control parameters are depth of focus (DOF) and exposure latitude (EL); whereas, the feature placement parameters are alignment accuracy, magnification, and rotations. All are mutually dependent and can be set during wafer exposure. Among these five parameters, the exposure-defocus (E-D) window (shown in Figure 1.5, with its mutual tradeoff depicted in Figure 1.6) is most frequently used. Adding alignment accuracy, magnification, and rotations generalizes the meter to include overlay-related parameters. The meters will be fully described and extensively used in this book.