CHAPTER 1

DETECTOR ARRAYS

In order to understand the performance limits and calibration requirements of an instrument it is necessary to have an understanding of the nature of the detector array, its key performance parameters, and the way these are defined and measured. These are all considered in this chapter, which serves to introduce many of the detector terms that are discussed later in the guide. At first sight there is a confusing multitude of array types, parameters and definitions, and an extensive published literature; however, it is hoped that the discussion below can act as a basic summary and a pointer to references for further reading, should these be required.

1.1 Types of Detector Arrays

This discussion is concerned exclusively with instruments that use detector arrays fabricated using semiconductor materials (sometimes termed solid-state detector arrays). Such arrays have two parts:

1. A mosaic of closely spaced detector elements that convert the incident electromagnetic radiation into electrical signals,
2. A readout circuit that relays and multiplexes the electrical signal from each detector element (or pixel) to a small number of output amplifiers (usually one or two).

Although both functions may (as in a visible CCD) be realized with the same basic structure, on a single piece of material (die) this is not necessarily the case. Hence, it is important when considering the properties of the different types of solid-state arrays that the various architectures are distinguished.

Regarding the detector elements, Fig. 1.1-1 illustrates the wide variety of semiconductor materials that can be used and their wavelength ranges and typical operating temperatures. Most are photon detectors in that they respond only to those photons that have an energy greater than the band gap of the semiconductor material. The detector response is proportional to the rate of absorption of these photons. There is another class of thermal detectors, which includes the pyroelectric and microbolometer arrays used for near–room temperature (usually termed uncooled) sensing in the infrared. In these the detector measures the total amount of heat that is absorbed, regardless of the number of photons.
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### Atmospheric Transmission

<table>
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<th>Wavelength Band</th>
<th>UV</th>
<th>V</th>
<th>NIR</th>
<th>SWIR</th>
<th>MWIR</th>
<th>LWIR</th>
<th>VLWIR</th>
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<td>0.2</td>
<td>0.3</td>
<td>0.5</td>
<td>1.0</td>
<td>2.0</td>
<td>3.0</td>
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</table>

#### Thermal Detectors

- Thermocouple
- Thermistor
- Pyroelectric
- Bolometer arrays

#### Intrinsic Photo-Detectors

- Si (300K)
- PbSe (300K)
- GaAs
- InSb (77K)
- InGaAs 300K 240K
- PtSi (77K)
- HgCdTe (160K) (120K) (77K) (40K)

#### Extrinsic Photo-Detectors

- Si:In (77K)
- Si:Ga (20K)
- Si:As (10K)
- Ge:As (77K)
- Ge:Zn (5K)

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**Figure 1.1-1** Semiconductor detector materials.

As well as different detector materials, there are also a variety of detector constructions. Photon detector materials can be used in three basic types of structures:

1. **photoconductive (PC) mode detectors**, where the absorbed photons cause a change in conductivity. When a constant bias is placed across the detector, the modulation in the current through the semiconductor is proportional to the change in irradiance.
2. **photovoltaic (PV) mode detectors**, where the absorbed photons create a change in voltage at a potential barrier either produced by
   - a p-n junction or
   - induced by electric fields with a metal-insulator-silicon (MIS) structure.
3. photoemissive detectors, such as silicide Schottky barrier devices. In these, photons are absorbed in the silicide electrode and a small fraction of the excited carriers are emitted over the Schottky barrier into the semiconductor. The charge generated at the electrode is then transferred to a readout structure.

There are also a number of different designs for readout electronics. Among these are

- CCD (charge-coupled device) readouts
- MOSFET switch readouts (including CMOS circuits)
- CID (charge injection device) readouts
- CIM (charge imaging matrix) readouts.

Many of the above detector types and readout circuits have been developed for imaging in the infrared. For wavelengths less than 1100 nm (1.1 \( \mu \text{m} \)) the choice is largely restricted to silicon detectors operating in a photovoltaic mode (either as photodiodes or as MOS capacitors). Only these will be considered in detail in the remainder of this guide, since the chief interest is in imaging and spectrometry applications in the ultraviolet (UV), visible, and near-infrared (NIR). Occasional reference will, however, be made to calibration issues for IR detectors, many of which will be similar to those for silicon detectors (see, in particular, Sec. 4.1.2). For more information on the basic principles of IR arrays the reader is referred to the following general reviews:

- Harnly et al., “Solid-state array detectors for analytical spectrometry,”\textsuperscript{1}
- Scribner et al., “Infrared focal plane array technology,”\textsuperscript{2}
- Norton, “Infrared image sensors,”\textsuperscript{3}
- Rogalski, “New trends in semiconductor infrared detectors,”\textsuperscript{4}
- Rogalski, “Infrared photon detectors,”\textsuperscript{5}
- Crowe et al., Chap. 4 in \textit{The Infrared & Electro-Optical Systems Handbook (Vol. 3)}\textsuperscript{6}

Since CMOS and MOS circuits are commonly used for readout of IR arrays, these are briefly reviewed in Sec. 1.1.6.

\subsection*{1.1.1 Types of Silicon Detector Arrays}

As mentioned above, this guide is primarily concerned with silicon detectors. Photons are absorbed via the photoelectric effect and create electron-hole pairs. Since a photon has an energy \( \frac{hc}{\lambda} \) where \( h \) is Planck’s constant, there is a limit on the longest wavelength that can be detected. This is given by

\[
\lambda_{\text{cutoff}} (\mu \text{m}) = \frac{1.24}{\text{bandgap(eV)}}.
\]  

(1.1.1-1)
Silicon has a bandgap of 1.1 eV and is sensitive up to roughly 1.1 µm. There is roll-off in response from about 0.8 µm upwards because the detector is thin (about 20 µm) and the absorption length becomes large. At short wavelengths (blue and UV) there is also a limit because the absorption length becomes small and photons are absorbed in surface layers and do not get through to the silicon. In the visible region, one electron-hole pair is created for each photon absorbed. The holes diffuse to the substrate and recombine, the electrons are collected within a pixel and give rise to the signal charge. The basic response of silicon detectors is shown in Fig. 1.1.1-1. At x-ray and far-UV wavelengths, each photon has enough energy to create several electron-hole pairs (in fact, one for every 3.6 eV of photon energy). So, a 20-keV x-ray (e.g., from a medical x-ray tube) will produce about 6000 electron-hole pairs by direct interaction with the silicon.

![Wavelength response of silicon](image)

**Figure 1.1.1-1** Wavelength response of silicon.

Silicon detectors operate in the photovoltaic mode and there are two basic detector types; the photodiode and the metal oxide silicon (MOS) capacitor. These are illustrated in Fig. 1.1.1-2. Photodiodes have only a small part of the surface covered by the contact electrode. The MOS capacitor has a semi-absorbing gate electrode and tends to have a reduced blue response when front-illuminated (c.f. Fig. 1.1.1-3). An alternative is to thin the detector and illuminate from the back. With front illumination the blue response can be improved if polysilicon, the standard electrode material, is replaced with indium tin oxide (ITO) or if “windows” are created in the electrode structure (as with *open-phase* and *virtual-phase* devices). Blue/UV response can also be boosted by using a phosphor coating (e.g., lumogen). For x-ray sensitivity, a phosphor such as...
CsI or gadolinium oxysulphide (Gadox) can be used as an alternative to the direct interaction discussed above.

In some applications (for example, imaging), the red response of the detector (out to 1.1 µm) is unwanted (because images are blurred due to chromatic aberrations in the lens). Hence, some commercial CCD cameras use detectors with a thin (~2 µm) active region (implemented via a special drain structure) to “kill” the red response. Other applications (for example, Raman spectroscopy) need good IR response and sometimes use a thick (e.g. 50 µm) active region with low doping, so that the depletion region is also thick and spatial resolution is not degraded (these are often called deep-depletion devices).

![Photodiode and MOS capacitor structures.](image)

**Figure 1.1.1-2** Photodiode and MOS capacitor structures.

![Quantum efficiency for typical CCDs and photodiodes.](image)

**Figure 1.1.1-3** Quantum efficiency for typical CCDs and photodiodes.
As discussed in Sec. 1.1, there are also two basic types of readout for silicon sensors: the charge-coupled device (CCD) and the MOS X-Y addressed switch array. In a CCD the photo-generated charge is moved across the chip towards an output amplifier by applying a clocking sequence to the CCD electrodes. A typical sequence for a three-phase device is illustrated in Fig. 1.1.1-4. CCDs can be manufactured with two, three, or four phases. Two-phase devices are the easiest to clock but need additional implants during manufacture to define the direction of charge transfer. The following simple sequence illustrates the basic principle of operation, but it should be noted that CCD manufacturers will define particular waveforms that are optimized for their own devices.

When an electrode is pulsed high, a potential well is created underneath it. At point A in the clock waveform (left of Fig. 1.1.1-4) charge collects under phases 1 and 2. When phase 1 goes low (point B) the charge is squeezed under phase 2, and when phase 3 goes high it is shared between phases 2 and 3. The sequence carries on, and at the transition F to A we arrive back at the starting point of the clock sequence, at which point it can be seen that charge has moved sideways by one pixel.

There are four basic types of readout architectures for a CCD: frame transfer (FT), full frame (FF), interline transfer (ILT or IL), and frame interline transfer (FIT). These are shown in Fig. 1.1.1-5.

![Figure 1.1.1-4 Typical CCD clocking sequence for a three-phase device.](image)

![Figure 1.1.1-5 CCD architectures. The directions of charge transfer are shown arrowed. The shaded areas are shielded from light by a metallized layer on the chip.](image)
FF CCDs have the simplest architecture and are the easiest to make and operate. They consist of a parallel CCD shift register, a serial CCD shift register, and a signal-sensing output amplifier. Images are optically projected onto the parallel array, which acts as the image plane. The resulting rows of scene information are then shifted in a parallel fashion to the serial register, which shifts each row of information to the output as a serial stream of data. The process repeats until all rows are transferred off the chip. Because the parallel register is used for both scene detection and readout, a mechanical shutter or synchronized strobe illumination must be used to preserve scene integrity. The simplicity of the FF design yields CCD imagers with the highest resolution (for a given chip size).

The FT CCD architecture is similar to that of the FF CCD, except that FT CCDs have a separate, identical parallel register, called a storage region, which is not light sensitive. The idea is to quickly shift a captured scene from the image array to the storage array. Readout off chip from the storage register is then performed as described in the FF device, while the storage array is integrating the next frame. The advantage of this architecture is that a continuous or shutterless/strobeless operation is achieved, resulting in faster frame rates. Performance is compromised, however, because integration is still occurring during the image dump to the storage array, which results in image smear (see Sec. 3.1.16). Because twice the silicon area is required to implement this architecture, FT CCDs have lower resolutions and higher costs than FF CCDs.

ILT CCDs address the shortcomings of FT devices by separating the photo-detecting and readout functions with isolated photosensitive regions between lines of nonsensitive or light-shielded parallel readout CCDs. After integrating a scene, the signals collected in the pixels are simultaneously transferred to the light-shielded parallel CCD. Transfer to the output is then carried out in much the same way as in FF and FT CCDs. During readout, the next frame is being integrated, thus achieving a continuous operation and a higher frame rate. Because of the architecture, the image smear that occurs in FT CCDs during readout is significantly reduced. It is not entirely eliminated, however, because photons can migrate sideways from the photodiode sensor to the vertical CCD shift register either by scattering or by multiple reflections in the dielectric layer under the gate electrode structure, a process known as light-piping. The FIT CCD was invented to reduce the smear that is still present in ILT CCDs.

The FIT CCD has a storage region (as in the FT) CCD so that charge does not need to stay in the vertical CCD registers during serial readout of a line. Hence, it will pick up less smear from the scene being imaged.

The major disadvantages of ILT and FIT CCD architectures arise from the complexity of the devices, which leads to higher unit costs and lower sensitivity. Lower sensitivity occurs because less photosensitive area (i.e., a reduced aperture) is present at each pixel because of the associated light-shielded readout CCD. Furthermore, quantization, or sampling errors, are greater because of the reduced aperture (hence, aliasing effects are more pronounced). Lastly, some ILT and FIT architectures using photodiodes suffer image lag as a consequence of charge transfer from the photodiode to the CCD.

With the frame transfer and full frame devices it is quite common to have output amplifiers at each end of the serial readout register so as to reduce the readout time. There is often the choice to use just one amplifier (and have just one video channel) or to use both. There is a penalty in
the additional circuitry (and pin-out) and so in cost—low-cost cameras will usually have a single video output. A variant of the frame transfer array is to have two storage regions, one at the top and one at the bottom of the image area. Half of the image is transferred up into the top storage region and half to the bottom. This results in a faster readout (two serial registers are used) and half the smear (since the time taken to transfer into the storage region is halved). Again, there is a penalty in system complexity and cost.

X-Y addressed MOS and CMOS arrays are shown in Fig. 1.1.1-6. The vertical (row) register is used to connect a whole row of detectors and the horizontal (column) register is used to connect each pixel in that row, in turn, to the output amplifier. This type of readout has the advantage of random access (not all the pixels need to be read out) but the disadvantage of high readout noise (because of the high capacitance of the readout lines) unless an amplifier is incorporated into each pixel as in Fig. 1.1.1-6(b)). Also, part of the detector area is taken up by the switching transistors, so the fill factor is low.

In summary, we have two detector types (photodiodes and MOS capacitors) and two basic types of readouts (CCD and X-Y addressed). The combinations of these are shown in Fig. 1.1.1-7. The abbreviations are defined as follows:

- **CCD** charge-coupled device
- **CID** charge injection device
- **CCPD** charge-coupled photodiode array—a linear photodiode array with a linear CCD alongside (sometimes on both sides) for readout
- **ILT CCD** interline transfer CCD
- **FIT CCD** frame interline transfer CCD
- **FT CCD** frame transfer (including full frame) CCDs

![Figure 1.1.1-6](image.png)

**Figure 1.1.1-6** Readout structure for (a) MOS and (b) CMOS-APS X-Y addressed arrays.
The performance of these detectors is briefly summarized below. The performance parameters are considered in more detail in Sec. 2.2.

**CCD detector: MOS capacitor and CCD readout.** This has good noise performance (can be as low as a few electrons), high fill factor, modest full well capacity (a few $\times 10^5$ electrons) but poor blue response (unless using a special electrode structure, phosphor coating, or back illumination).

**Charge injection device (CID): MOS capacitor and X-Y readout.** This has the possibility for random access but high readout noise due to the clock line capacitance (and low output voltage). However, there is the possibility for nondestructive readout (in which case noise can be reduced by averaging readouts).

**Photodiode array (PDA): photodiode and X-Y readout.** This has good blue response and high full well capacity ($>10^6$ electrons) but high readout noise. Hence, photodiode arrays are usually used for high-light-level applications.

**Charge-coupled photodiode array (CCPD): photodiode and CCD readout.** In linear arrays (as used in linescan cameras), it is possible to have the best of both worlds and have a photodiode detector (for good blue response and high full well capacity) and CCD readout register alongside (for low noise). Many 2D interline transfer and frame-interline transfer CCDs in fact use photodiodes as the detector elements. Also, many so-called photodiode arrays (PDAs) will have a CCPD structure and in common use the term PDA usually applies to a linear array with either a MOS (true PDA) or a CCPD structure. The term LPDA or linear PDA is also common.

**The active pixel sensor (APS): photodiode or MOS capacitor with CMOS X-Y readout and gain.** The active pixel sensor (APS) can have either photodiodes or MOS capacitors (photogates) as the detector elements and uses a CMOS switch array for readout with a gain transistor (MOSFET) within each pixel. This improves the noise performance since the
The CMOS readout technology reduces cost, simplifies drive requirements (only a few TTL clocks are needed) and allows for additional circuitry on-chip, for example, digitization (on-chip ADC), edge detection, thresholding, motion detection and spatial filtering. Random addressing is also possible in some devices. APS devices are ideally suited to many low-cost imaging and machine vision applications and the performance can in some circumstances rival that of scientific CCDs (i.e., CCDs used for scientific rather than imaging applications).

Until recently most active pixel sensors were monolithic. That is, both the detector elements (e.g., photodiodes) and the CMOS switching circuits were manufactured on the same silicon die. These devices are sometimes called MAPS (monolithic active pixel sensors). Over the past year or so, hybrid silicon APS devices have become commercially available and these provide an alternative for visible imaging. In hybrid devices the detector and readout circuits are formed on separate dies that are indium- or solder-bump-bonded together. This is a common situation for infrared arrays where the detectors are necessarily made of semiconductors other than silicon. However, though expensive, the advantages in using hybrid technology in the visible include 100% fill factor and compatibility with back illumination. Also, the readout circuit can be more complex, giving advantages in readout noise.

1.1.2 Color Imaging

The most common method of achieving 2D color imaging in high-resolution (e.g., broadcast-quality) systems is to use three CCDs (one for each primary color) and to split the light between them by means of a prism. For more commercial applications, it is common to use either stripe or mosaic color filter arrays (CFAs) placed directly on to the detector array (Fig. 1.1.2-1). Further information is given in Refs. 8 and 11. Reference 12 gives an interesting discussion on the trade-offs between the different CFA patterns.

Stripe filters are usually used in conjunction with frame transfer CCDs. For example, each pixel in a column being covered by a red, green, or blue filter (in fact, there are twice as many green pixels as either red or blue, because the eye is more sensitive to green light and because the coding for TV color signals has a luminance signal, which is sum of all the colors but weighted towards the green). There is an advantage in using the complementary colors cyan and yellow since then only two (overlapping) filters are needed (the overlapped combination of the two gives green). There is another advantage in that a green signal is present in each pixel and can be used to derive a high-spatial-frequency component in the image (“high-frequency green”).

For interline transfer CCDs the number of horizontal pixels is at a premium (since the vertical shift registers also need to be accommodated). Hence, it is usual to use a matrix (or mosaic) of filters arranged in, for example, 2×2 pixel blocks. In this way, the horizontal resolution is half that of a monochrome imager (as opposed to a third for a stripe filter), but the vertical resolution is also degraded by a factor of 2. Again, complementary color filters can be employed. Video processing ICs (ASICs) are used with mosaic CCDs to perform the arithmetic
for deriving the RGB data necessary for display. There are several possibilities for color imaging with a linear array, depending on the trade-off between spatial resolution and data rate, as shown in Fig. 1.1.2-2 (after Ref. 8).

**Figure 1.1.2-1** Examples of stripe and mosaic filters. For the mosaic filter shown, two vertically adjacent colors are always mixed together; which two depends on the interlace field (n or n+1).

**Figure 1.1.2-2** Example configurations for color imaging with linear arrays.