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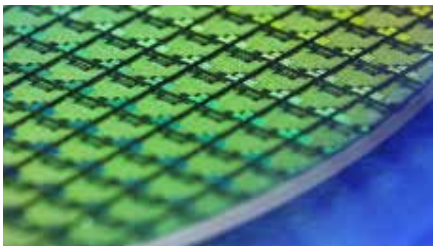

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Conference 9048: Extreme Ultraviolet (EUV) Lithography V

Monday - Thursday 24–27 February 2014

Part of Proceedings of SPIE Vol. 9048 Extreme Ultraviolet (EUV) Lithography V

9048-1, Session 1

Progress and challenges of EUV lithography for high-volume manufacturing *(Invited Paper)*

Anthony Yen, Jack Jenghorng Chen, TSMC Taiwan (Taiwan)

No Abstract Available

9048-2, Session 1

Challenges of EUV/193i complementary lithography *(Invited Paper)*

Mark C. Phillips, Intel Corp. (United States)

No Abstract Available

9048-3, Session 2

EUV resists toward 11nm half-pitch

Yasin Ekinci, Michaela Vockenhuber, Nassireddin M. Mojarad, Daniel Fan, Paul Scherrer Institut (Switzerland)

Extreme ultraviolet lithography (EUVL) is expected to be introduced for sub-20 nm technology node in semiconductor device manufacturing. As EUVL prepares for its insertion into the high-volume manufacturing phase, several challenges still remain to be addressed in the short term. In long term, for the extendibility of the EUV technology to the next technological nodes, many critical questions are open and significant challenges remain. Among several issues, development of EUV resists with tight specifications of sensitivity (dose), resolution (HP) and line-edge roughness (LER) is required. For the future of EUVL, it is crucial to illustrate the extendibility of the EUV resists to further technology nodes.

The EUV interference lithography (EUV-IL) tool at Paul Scherrer Institute is a powerful technique providing well-defined aerial image for patterning of one-dimensional and two-dimensional periodic nanostructures with a resolution beyond the capabilities of other tools. Well-resolved patterns of 7 nm HP are obtained with this tool at XIL-II beamline of Swiss Light Source (SLS), marking the record in photon-based lithography.

In this paper, we will present performance of different resists using the PSI EUV-IL tool. We present a comparative study of the performance of the chemically-amplified resists (CAR) and inorganic resists. We discuss the current status of EUV resist availability for 16 nm, 11 nm and 7 nm technology nodes. We show that the global trend of increasing resolution with decreasing sensitivity is valid across the different resist platforms. This trade-off between resolution and sensitivity is mainly dominated by the acid diffusion blur. We propose a concept how to break this trade-off. We also show that with decreasing HP, pattern collapse becomes a significant challenge, and therefore resist stability, collapse mitigation, and etch pattern transfer are significant challenges in the sub-16 nm range. Moving a step further, we also discuss the extendibility of resists to beyond EUV (BEUV) lithography and point out the potential challenges based on the obtained results with BEUVL.

9048-4, Session 2

Investigation of novel inorganic resist materials for EUV lithography

Marie E. Krysak, James M. Blackwell, Intel Corp. (United States); Todd R. Younkin, Intel Corp. (Belgium); Steve E. Putna, Michael J. Leeson, Intel Corp. (United States)

Recently, both PSI1 and ASML2 illustrated champion EUVL resolution using slow, non-chemically amplified inorganic resists. However, the requirements for EUVL manufacturing require simultaneous delivery of high resolution, good sensitivity, and low line edge/width roughness (LER/LWR) on commercial grade hardware. As a result, we believe that new classes of materials should be explored and understood. This paper focuses on our efforts to assess metal oxide-based nanoparticles as novel EUV resists.3 Spectroscopic techniques such as Nuclear Magnetic Resonance (NMR), Dynamic Light Scattering (DLS) and Transmission Electron Microscopy (TEM) were used to probe the patterning mechanism of these materials. EUV exposure data of these resists is presented to investigate the feasibility of employing inorganic materials as viable EUV resists.

[1] Yasin Ekinci, Y. et. al, Proc. SPIE 8679, Extreme Ultraviolet (EUV) Lithography IV, 867910, 2013.

[2] Peeters, et. al, Proc. SPIE 8679, Extreme Ultraviolet (EUV) Lithography IV, 86791F, 2013.

[3] Krysak, et. al., Proc SPIE 7972, Advances in Resist Materials and Processing Technology XXVIII, 79721C, 2011.

9048-5, Session 3

Stochastic effects in fabrication of 11nm line-and-space patterns using extreme-ultraviolet lithography

Takahiro Kozawa, Osaka Univ. (Japan); Julius Joseph S. Santillan, Toshiro Itani, EUVL Infrastructure Development Ctr., Inc. (Japan)

The development of resist materials used for extreme ultraviolet (EUV) lithography has significantly progressed with the advance of the exposure tool technologies. 18 nm line-and-space patterns with 2.6 nm line width roughness (LWR) have been fabricated at the exposure dose of 20 mJ cm-2, using a microexposure tool (MET) at SEMATECH Berkeley. 16 nm line-and-space patterns have been also fabricated at the exposure dose of 33 mJ cm-2, using NXE:3100 with off-axis illumination. 15 nm line-and-space pattern fabrication with a pseudo phase-shift mask has been also reported. However, there is still a gap between current status and requirements for resist materials. The resist requirements at the 16 nm node are the sensitivity of 10 mJ cm-2 and the LWR of 1.3 nm. Also, the investigation on the feasibility of 11 nm fabrication with a chemically amplified resist has already started. Results with non-chemically amplified resists [hydrogen silsesquioxane (HSQ) and hafnium oxide resists] have demonstrated that EUV lithography is capable of resolving line-and-space patterns with 11 nm half-pitch. The enhancement of sensitivity and the reduction of LWR are currently urgent tasks required for resist makers in the development of resist materials for 16 nm node. Highly sensitive resists are required in the high-volume production lines for the enhancement of productivity. Thus the stochastic effect in resists increasingly becomes a concern with the reduction of feature sizes.

We have investigated the stochastic effects induced during the exposure and post exposure bake (PEB) process using a small field exposure tool (SFET) by analyzing LWR and resist defects. The physical properties of state-of-the-art resists and the relationship between latent image and stochastic effect have been made clear. In this study, we theoretically evaluated the stochastic effects in the fabrication of 11 nm line-and-space patterns on the basis of the previously reported physical properties and relationship. The material design for 11 nm technology node will be discussed from the viewpoint of stochastic effects.

A part of this work was supported by the New Energy and Industrial Technology Development Organization (NEDO).

9048-6, Session 3

Understanding EUV resist mottling leading to better resolution and linewidth roughness

James W. Thackeray, James F. Cameron, Vipul Jain, Paul LaBeaume, Owendi Ongayi, Suzanne M. Coley, Michael Wagner, Dow Electronic Materials (United States)

500 Word Abstract: It appears that EUV technology insertion will not occur until 10nm node. The current best resists for this node are low diffusion chemically amplified resists. These resists offer the best compromise between resolution, linewidth roughness and sensitivity. However, there are legitimate concerns regarding pattern integrity and overall process window at sub- 20nm patterning. At resist exposure doses less than 20 mj, one expects stochastic variation due to exposure shot noise.1 Also, there is expected to be a significant amount of out-of-band radiation flare contributing to poor aerial image contrast.2 It is imperative that the EUV chemically amplified resists maintain high performance characteristics under these conditions. This paper will focus on Dow's learning regarding the optimal dissolution characteristics of EUV chemically amplified resists. The familiar dissolution properties such as maximum dissolution rate, Rmax, and minimum dissolution rate, Rmin, and development contrast, Tan(?), will be reported with the goal of deriving a correlation between these parameters and lithographic performance. In Figure 1 (Resist A), we show a top down pattern of 18nm line space with significant top roughness, line bending, line breakage. We characterize this behavior as resist mottling. We believe that this behavior is a consequence of isolated areas of deprotection in the nominally unexposed areas leading to irregular development on top of lines. It is well known that chemically amplified resists have a threshold percolation development which can lead to swiss cheese development.3 It is not observed in the exposed areas because the exposed resist dissolves quickly and heals upon drying. In Figure 1 (Resist B), we show a top down pattern of 18nm lines with no mottling effect. We attribute this improvement due to a lower Rmax value as well as less resist swelling during development. By modifying these parameters, we can make the development step less chaotic and reduce LWR and eliminate resist mottling. This paper will also report on our performance for line/space resists as well as contact hole resists. Also, further out-of-band radiation studies will be conducted and reported. Lastly, the tradeoff between LWR and CDU vs sensitivity will be discussed.

References: 1.) Moshe Preil, Proc. SPIE. 8325, Advances in Resist Materials and Processing Technology XXIX 832503 (2012); 2.) Gian F. Lorusso, Tasaku Matsumiya, Jun Iwashita, Taku Hirayama, Eric Hendrickx, Proc. SPIE. 8679, Extreme Ultraviolet (EUV) Lithography IV 86792V (2013); 3.) Chris A. Mack, Proc. SPIE. 7273, Advances in Resist Materials and Processing Technology XXVI 72732I (2009).

9048-7, Session 3

Comparison of EUV patterning between PTD and NTD for 1Xnm DRAM

Chang-Il Oh, SK Hynix, Inc. (Korea, Republic of)

Recently patterning technology for contact hole has become one of the major issues on 1Xnm node DRAM device. DPT (Double Patterning Technology) and SPT (Spacer Patterning Technology) can be applied for 1Xnm DRAM but too many DPT and SPT can make device shrink meaningless due to the increasing of process step and higher CoO (Cost of Ownership). EUV can be considered as a countermeasure but need to overcome critical issues such as source power, mask defectivity and resist RLS (Resolution, LWR, Sensitivity) trade-off. And from the EUV resist point of view EUV shot noise has become fundamental issue to deteriorate CDU (CD Uniformity) and delay of source power upgrade is pushing EUV resist to have high sensitivity.

Meanwhile patterning performance between PTD (Positive Tone Development) and NTD (Negative Tone Development) were compared on ArF immersion, and eventually resolution and CDU for contact hole were improved dramatically based on the benefit of image contrast and swelling by using ArFi NTD. That very fact can be the motivation we need to evaluate EUV NTD to overcome current EUV resist circumstances. In this paper, we will compare patterning performance of EUV PTD and EUV NTD, and describe current status and issues of EUV NTD for 1Xnm node DRAM device.

9048-8, Session 3

Impact of stochastic effects on EUV printability limits

Peter De Bisschop, Jeroen Van de Kerkhove, Julien Mailfert, IMEC (Belgium); Alessandro Vaglio Pret, KLA-Tencor/ ICOS Belgium (Belgium); John J. Biafore, KLA-Tencor Texas (United States)

The impact of aerial image quality and stochastic effects on EUV variability are well known and many studies have been devoted to this topic. Photo-shot noise is one of the main contributors to these effects, although some resist parameters also play a role. Usually this variability is studied in terms of LER/LWR or local CDU, and quantitative analyses and predictions – both using simple equations or stochastic rigorous simulations – are available. From this theoretical understanding as well as from numerous wafer experiments, a number of strategies to mitigate these effects have been identified (such as smoothing techniques, impact of dose-to-size etc.)

One aspect of these stochastic effects has however been less studied, namely how these stochastic effects impact the printability limit: if the CD variability becomes too large, structures can fail to be printed altogether. A well-known example is randomly missing contacts at conditions where surrounding contacts of equal size still seem to print well. But stochastic effects can also be observed in trench printing. While long dense trenches are printing well, for example, more isolated or short trenches OPC-ed to the same size are barely open, which shows that the printability limit is a structure-dependent quantity (i.e. depends on the image quality). Figure 1 shows a related example. A pattern of shorter and longer trench patterns was OPC-ed using a calibrated resist model but only prints well at high-enough doses (i.e. if we choose a resist with a large-enough dose-to-size), where we also see that exposing at a higher NA allows to use a lower dose again. All these examples and dependencies are consistent with shot-noise dominated stochastic effects.

In all these scenarios, lithographic printing failures would cause loss of yield, considering that closed contacts or locally closed trenches cannot be 'repaired' by smoothing techniques or etching. It is therefore important to understand how we can avoid such printing failures, especially in practical applications where a multitude of different structures needs to be correctly printed simultaneously (as is the case in the example of Figure 1).

We have done a study on the relationship between stochastic effects and printability limits, measuring the printability limit for a variety of structures for several dose- and NA-settings. Figure 2 illustrates our approach for the example of a contact-array of a certain pitch. When counting missing contacts in contact arrays of decreasing CD, the printability limit can be defined as the smallest contact size for which no failing contacts are observed. It is then important to not only know where this printability limit is, but also how it can be influenced, e.g. by going for a different (i.e. larger) exposure dose. From this we then need to determine the lowest exposure dose to print the requested features (with a sufficient process window), such that also the wafer throughput is not unnecessarily compromised.

In this paper we will present our data and will try to translate our findings to design rules, or to minimum exposure dose required to meet a certain design rule. We believe that such results are important in better understanding how EUV can be introduced in manufacturing, especially for Logic applications. An accompanying paper will look in more detail at the contact-hole case, investigating also the dependency of the printability limit on resist parameters.

9048-9, Session 3

EUV stochastic noise analysis and LCDU mitigation by etching on dense contact-hole array patterns

Seo Min Kim, SK Hynix, Inc. (Korea, Republic of); Chang-Nam Ahn, ASML US, Inc. (United States); Sunyoung Koo, Hynix Semiconductor Inc. (Korea, Republic of); Jun-Taek Park, Chang-Moon Lim, Myoung Soo Kim, SK Hynix, Inc. (Korea, Republic of); Anita Fumar-Pici, ASML US, Inc. (United States); Alek C. Chen, ASML Taiwan Ltd. (Taiwan)

Stochastic noise is known as the major contributors of LWR in line/space pattern and local CD uniformity (LCDU) of the contact hole patterns. Its portion increases as the number of photon decrease, the number of PAG in resist decrease, or optical contrast decrease. So, it is very natural that stochastic noise dominates as pattern size decrease. Eventually it may not allow single exposure contact hole formation within CDU requirement. In this experiment, stochastic noise component has been extracted from the contact hole LCDU before and after etching quantitatively.

Contact hole LCDU is affected by stochastic noise as well as mask local CD uniformity. Mask contribution is repeating from field to field, but stochastic noise is not. From this difference, random component mainly caused by stochastic noise and repeating component mainly came from mask imperfection can be extracted statistically from the LCDU. And also metrology error can be extracted, too.

NXE:3100 with quasar illumination (45deg, 0.51/0.81) has been used to print dense contact hole arrays of half pitch range of 25~32nm. Different mask CD in a given half pitch is also evaluated in order to get minimum LCDU condition and MEEF comparison. In order to compare the identical contact holes in repeating fields, wafer images have been captured including array corner as shown in Fig.1.

Metrology error is ~1nm level in 3 sigma value for resist pattern and looks almost constant over all half pitch ranges. Mask CD is also measured and mask contribution is confirmed through MEEF analysis. Stochastic noise is the most dominant factor of the LCDU contributors. It is more than ~60% of LCDU in linear scale.

There are several post processes considered to mitigate LWR of lines or LCDU of contact holes. Etching also can reduce LCDU. In order to check how much improvement etching can make in LCDU and what happen on stochastic noise, etching test was done on oxide stack. Fig. 1 shows typical result of LCDU improvement after etching. LCDU improved ~30% by etching in this case. Its amount depends mainly on etching process, but there is some room for further improvement through process optimization not only etching process but also lithography process targeting.

9048-10, Session 4

Accelerator-based EUV lithography source: FEL-oscillator, SASE-FEL, or a very different beast? *(Invited Paper)*

Atoosa Meseck, Andreas Jankowiak, Jens Knobloch, Johannes Bahrdt, Andreas Gaupp, Helmholtz-Zentrum Berlin für Materialien und Energie GmbH (Germany); Diana Spengler, Erik M. Sohmen, Carl Zeiss SMT GmbH (Germany); Udo Dinger, Carl Zeiss AG (Germany); Michael Patra, Carl Zeiss SMT GmbH (Germany)

In this presentation, I will discuss the prospects of different accelerator-based radiation-sources to serve EUV-lithography. Following an introduction of the basic beam requirements, which the driver accelerator needs to provide, I will present in detail several potential candidates for a radiation generation process suited to the needs of EUV-lithography. Presenting feasible or already existing facilities layouts, I will not only focus on the beam and radiation physics but also provide a good insight in what is state of the art, what is feasible today and what is possible tomorrow.

9048-11, Session 4

LPP EUV source readiness for NXE 3300

David C. Brandt, Igor V. Fomenkov, Nigel R. Farrar, Bruno La Fontaine, David W. Myers, Daniel J. Brown, Alex I. Ershov, Norbert R. Bowering, Cymer, Inc. (United States); Rudy Peeters, Hans Meiling, Noreen Harned, Daniel A. Smith, ASML Netherlands B.V. (Netherlands)

Laser produced plasma (LPP) light sources have been developed as the primary approach for EUV scanner optical imaging of circuit features in sub-20nm devices in high volume production (HVM). This paper provides a review of development progress and readiness status for the LPP extreme-ultra-violet (EUV) source. We present the latest results from testing of second generation sources, including Prepulse operation for high power, collector protection for long lifetime and low cost of ownership, and dose stability for high yield. Prepulse operation has been developed with automated control for use in the production fab, we will discuss the control parameters and show the stability of operation. We will discuss lifetesting of the collector in Prepulse mode and show the ability of the debris mitigaiton systems to keep the collector multi-layer coating free from damage with high reflectivity. Drive laser power has been inclreased for second generation sources, we will show the results of testing the drive laser needed to meet the EUV power requirements. Finally we will show how the conversion efficiency (CE) of Prepulse operaiton has increased to allow the target EUV power to be achieved.

9048-12, Session 4

Sub-hundred Watt operation demonstration of HVM LPP-EUV source

Hakaru Mizoguchi, Takashi Saitou, Taku Yamazaki, Shinji Okazaki, Hiroaki Nakarai, Tamotsu Abe, Takeshi Kodama, Tatsuya Yanagida, Tsukasa Hori, Takeshi Ohta, Krzysztof M. Nowak, Yasufumi Kawasuji, Hiroshi Tanaka, Yutaka Shiraishi, Yukio Watanabe, Tsuyoshi Yamada, Georg Soumagne, Gigaphoton Inc. (Japan)

We have been developing CO2-Sn-LPP EUV light source which is the most promising solution as the 13.5nm high power light source for HVM EUVL. Unique and original technologies such as; combination of pulsed CO2 laser and Sn droplets, dual wavelength laser pulses shooting and mitigation with magnetic field have been developed in Gigaphoton Inc..

The theoretical and experimental data have clearly showed the advantage of our proposed strategy. Based on these data we are developing first practical source for HVM; “GL200E”. This data means 250W EUV power will be able to realize around 20kW level pulsed CO2 laser. We are preparing high average power CO2 laser cooperate with a laser supplier.

We will reported engineering data from our resent test such around 20W average clean power, CE=2.0%, 100kHz operation and other data. Further improvements are underway, we will report the latest challenge to maximum sub-hundred Watt, around 4% CE with 20 micron droplet, >99% Sn ionization rate by double laser shooting scheme and >99% Sn debris mitigation by magnetic field on 100kHz proto device.

9048-13, Session 4

Highly-efficient high-power pulsed CO_2 laser characterized by transverse-flow laser amplifiers

Yoichi Tanino, Jun-ichi Nishimae, Tatsuya Yamamoto, Taichiro Tamida, Koji Funaoka, Shuichi Fujikawa, Mitsubishi Electric Corp. (Japan)

In recent years, extreme ultraviolet (EUV) lithography technology has become increasingly focused on preparations for high-volume manufacturing. The power of EUV light sources required for exposure tool throughput remains as one of critical technical challenges. Technologies for the higher-efficiency EUV light source are also demanded. CO2 laser produced tin plasma (LPP) EUV light source is the promising candidate as the 13.5 nm high power light source for EUV lithography. Availability of high-power pulsed CO2 laser is one of important key factors for applying LPP EUV light source to high-volume manufacturing.

We are developing a CO2 laser for LPP EUV light source characterized by transverse-flow CO2 laser amplifiers. In the transverse-flow laser, the laser gas flows between the electrodes. The direction of the gas flow is perpendicular to the optical path. In principle, transverse-flow CO2 lasers offer a higher gain and a shorter optical path in the amplification system compared with axial-flow CO2 lasers. At the same time, arranging multi-fold path is possible in the case of transverse-flow lasers. Therefore, the transverse-flow CO2 laser is a promising candidate for EUV light source driver.

A master-oscillator power-amplifier (MOPA) CO2 laser system was constructed for amplification test. The master oscillator emitted single-line, 10.6 um (P20) laser pulses with the repetition frequency of 100 kHz. The pulse duration of the oscillator was 15 ns. As amplifiers, transverse-flow CO2 lasers were designed and constructed. The amplification experiment was done with two transverse-flow amplifiers in cascade. The first amplifier had a five-fold optical path and the second amplifier had a single path. The electrical input for the discharge of each amplifier was up to 100 kW. The amplification test was carried out at a 100% duty cycle of discharge.

As a result, the output average power of 8.3 kW was demonstrated with the small input power of 20 W using two transverse-flow amplifiers in cascade. Thus the electrical-to-optical efficiency was 4.1% which was higher than that of reported data using axial-flow amplifiers. In this experiment, the optical power of 5 kW was drawn from the second amplifier excited by the discharge power of 100 kW.

Transverse-flow CO2 lasers demonstrated highly-efficient high-power laser amplification at a 100% duty cycle of discharge. Inherent advantage of transverse-flow laser amplifier was shown in this test. Further experiments are underway targeting the average output power exceeding 20 kW with four amplifiers in cascade. The purpose of these experiments is suggesting a possibility of highly-efficient LPP EUV light source for high-volume semiconductor manufacturing. We will report the latest results in the presentation.

9048-14, Session 4

In situ plasma cleaning method for collector optics

Daniel Elg, David N. Ruzic, Univ. of Illinois at Urbana-Champaign (United States)

Extreme Ultraviolet (EUV) lithography sources produce EUV light by transferring a large amount of energy to an Sn droplet. As a consequence, Sn ions and neutrals are expelled. These deposit on the collector optic, degrading its reflectivity and hindering the collection of EUV photons. An in-situ plasma cleaning method is being developed to etch deposited Sn by means of hydrogen radicals, which react with Sn to form gaseous SnH4. Such a method could potentially cause a great reduction in system downtime, reducing the cost of ownership. Unlike an external plasma source, the in-situ method can create the etchant radicals in the chamber near the collector, where they are needed. Though Sn decomposition and re-deposition has previously hindered efforts at cleaning large surfaces, the ability to clean a large metal disk has been demonstrated using 300W of RF power with 500sccm of H2 flow at a pressure of 130mTorr. Sn removal rates on the order of 1 nm/min have been measured. Under these same conditions, cleaning has also been demonstrated on multilayer mirror (MLM) samples. Finally, end-detection methods have also been explored. The ability to detect etch completion can both save time and prevent possible substrate damage caused by over-etching.

9048-15, Session 4

Spectral purity enhancement for the EUV source by suppressing UV reflection from multilayer mirrors

Qiushi Huang, Toine van den Boogaard, Robbert W. van de Kruijs, Erwin Zoethout, FOM Institute DIFFER (Netherlands); Eric Louis, Fred Bijkerk, FOM Institute DIFFER (Netherlands) and Univ. Twente (Netherlands)

Multilayer based spectral filtering methods are developed to eliminate the UV out-of-band radiation (?=100-400 nm) for the EUV plasma source. They are highly needed due to the imaging contrast loss caused by a possible UV straylight exposure. Our phase-shift grating (PsG) method uses the diffraction property of a quarter-wavelength height multilayer grating to filter out the UV light. An ultra-thin anti-reflection layer was also developed by creating a proper material to suppress the reflection. Both methods have achieved a suppression factor of at least 10~30 around the target wavelength while preserving the high efficiency of EUV. To achieve a broadband suppression effect, a novel surface structure was further developed. The suppression property and EUV responses will be discussed.

9048-16, Session 5

Production of EUV mask blanks with low killer defects

Alin O. Antohe, Patrick A. Kearney, Milton C. Godwin, SEMATECH Inc. (United States); Long He, SEMATECH Inc. (United States) and Intel Corp. (United States); Arun John Kadaksham, Frank Goodwin, SEMATECH Inc. (United States); Alfred Weaver, Steve Trigg, Alan Hayes, Veeco Instruments Inc. (United States)

For full commercialization, EUVL technology requires the availability of EUV mask blanks that are free of defects. This remains one of the main impediments to the implementation of EUV. Consensus is building that smaller defects can be mitigated, but defects over 100 nm in size can not, and are considered likely “killer” defects. The current defect performance of the ion beam sputter-deposition (IBD) tool will be discussed, and the progress achieved to date in the reduction of “killer” defects will be summarized, including a description of the main sources of defects and their composition.

This paper discusses the main source of “killer” defects in the IBD tool – shield defects. Figure 1 shows how ~70% of the killer defects found during multilayer deposition can be traced back to the deposition shields installed inside the IBD tool (i.e. stainless steel and aluminum oxide particles).

In previous communications we have focused on how ion beam overspray of critical shields may liberate these particles. To investigate this, SEMATECH carried out deposition experiments under four different process conditions, with the intent to modulate the added

defect signature. Figure 2 shows the results of such experiments and how “killer” defect adders can be influenced by the chosen deposition process conditions.

9048-17, Session 5

Mitigation of EUV mask blank substrate pit and scratch defects by Accelerated Neutral Atom Beam (ANAB) processing

Michael Walsh, Kiet Chau, Sean Kirkpatrick, Richard Svrluga, Bernhard P. Piwczyk, Exogenesis Corp. (United States); Frank Goodwin, Dave K. Balachandran, SEMATECH Inc. (United States)

Ability to manufacture defect-free mask blanks must be established before EUV lithography can be implemented into production. Challenging problems exist in achieving mask blank substrates able to satisfy defined requirements including surface flatness and roughness while also being entirely free of residual scratches, bumps and embedded particles. No combination of available surface preparation techniques has been found capable of accomplishing all of the flatness, roughness and residual defect demands. Extensive development efforts employing combinations of surface preparation techniques have been conducted under the direction of SEMATECH and have resulted in mask blank substrates approaching the defined goals, but a fully complete and practical solution has to date not been demonstrated. Substrates which meet flatness and roughness requirements can be produced but they still invariably exhibit non-zero counts of shallow pits and scratches having dimensions sufficient to produce printable defects on completed masks.

Exogenesis Corporation has introduced a new surface modification technique known as Accelerated Neutral Atom Beam (ANAB) processing which shows promise for being able to remove from mask blank substrates the residual defects that other techniques have not been able to eliminate. ANAB is conducted under vacuum by a beam of electrically neutral argon gas atoms which have average energies of a few tens of electron volts. ANAB can remove material by sputtering under conditions which inherently cause nanoscale bumps, scratches and pits to be diminshed as the removal action proceeds. When used to sputter material from an extremely smooth surface, ANAB can remove a precisely controllable and uniform thickness of material without resulting in any increase of roughness. In the case of a mask blank substrate already planarized and polished by CMP, without creating any additional surface roughness, ANAB is capable of removing a sufficient depth of material so as to eliminate all residual pits and scratches.

Exogenesis and SEMATECH have collaborated to conduct an initial demonstration of feasibility of using ANAB for defect correction on EUV mask blank substrates. A representative mask blank substrate was characterized by SEMATECH to identify the location and nature of residual pit defects to be re-examined following processing by ANAB. Punch marks were added to mark the pit locations. The substrate was processed at Exogenesis on an nAccel 100 ANAB system using different ANAB doses on quadrant areas of the surface so as to remove 20, 40, 80 and 160 nm thick layers from respective quadrants and then using conditions to remove 40 nm uniformly from the entire surface. Post processing examination of the substrate at SEMATECH showed that all marked pit defects initially present had been eliminated. Surface roughness after processing was measured to be 0.160 nm RMS, essentially unchanged from the initial value of 0.151 nm RMS. These results indicate the potential of ANAB as the solution for the residual defect mitigation required in order to produce defect-free mask blank substrates. Additional development is in process.

9048-18, Session 5

Durability of Ru-based EUV masks and the improvement

Suyoung Lee, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

In EUV Lithography, an absence of promising candidate of EUV pellicle demands new requirements of EUV mask cleaning which satisfy the cleaning durability and removal efficiency of the various contaminations from accumulated EUV exposure. It is known that the cleaning with UV radiation is effective method of variety of contaminants from surface, while it reduces durability of Ru capping layer. To meet the expectation of EUV mask lifetime, it is essential to understand the mechanism of Ru damage. In this paper, we investigate dominant source of Ru damage using cleaning method with UV radiation. Based on the mechanism, we investigate several candidates of capping to increase the tolerance from the cycled UV cleaning. In addition, we study durability difference depending on the deposition method of Ru capping. From these studies, it enables to suggest proper capping material, stack and cleaning process.

9048-19, Session 5

B4C as an alternate capping layer for EUV masks

Arun J. Kadaksham, Mason Jang, Alin O. Antohe, Patrick A. Kearney, Frank Goodwin, SEMATECH Inc. (United States); Carl Ventrice Jr., Tyler Mowll, Univ. at Albany (United States)

Ruthenium has been selected as the capping layer for EUV masks due to its excellent etch stop properties and chemical durability. However experiments at SEMATECH has revealed that Ruthenium capping layer may not be as durable as expected for the lifetime of EUV masks. Previous studies at SEMATECH has shown that ruthenium is oxidized and etched by cleaning chemicals, degraded by megasonics and gather contamination by storage and transport, thus drastically reducing the life of EUV mask. One of the ways to stabilize the mask is to either replace the ruthenium with an alternate material that is more durable or form an alloy of ruthenium or barrier layer for ruthenium with a more durable material.

B4C is one such material with better chemical, mechanical and electrical resistance and optical properties than Ruthenium. B4C has also been used in the semiconductor industry in the past as an etch stop material. Using the Ion Beam Deposition tool at SEMATECH, several mask blanks with B4C capping layer and combinations of Ruthenium and B4C were manufactured to understand the durability of such blanks. In this paper, we report the results of the experiments and compare the durability of such blanks with standard Ruthenium capped blanks.

9048-20, Session 6

Study of alternative capping and absorber layers for EUV masks for sub-16nm HP nodes

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One of the challenges of the reflective optics used in Extreme Ultraviolet Lithography is that EUV light cannot be incident normally to the EUV mask surface. In the current EUV exposure tool the chief ray angle with mask normal is 6 degrees. This can be increased to 8 degrees or more if higher NA mirrors are used for the advanced nodes. Therefore, the oblique incidence of EUV light on a mask will cause a shadow

of the absorber on the image. This shadowing effect is undesired in EUV lithography and its impact on imaging increases as the pattern dimensions on the mask surface arerereduced. Reducing the absorber thickness is one method of reducing the shadowing effect. However, current TaN-based EUV absorbers do not have sufficient absorption below 55 nm thickness. Hence, materials such as Pt and Ni with high absorption in EUV region are potential candidates for an EUV absorber. In this paper we present an experimental study of the EUV reflectivity of Ni at 13.5 nm and its dependence on Ni thickness. Furthermore we present data on the chemical stability of Ni to the common cleaning chemistries.

TiO2 as an alternative capping layer to Ru is investigated and its chemical stability to the common cleaning chemistry is discussed.

Our results indicate that a Ni layer with thickness of 25 nm and larger can be used for the absorber. However, Ni is etched by cleaning chemistries and should be protected by another layer. TiO2 is one of the capping layers which can be used for EUV mirrors, however it absorbs EUV light more than the Ru layer and is removed by the standard cleaning process.

9048-21, Session 6

Evaluation of mask repair strategies via focused electron, helium, and neon beam-induced processing for EUV applications

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One critical area for EUV lithography is the development of appropriate mask repair strategies. To this end, we have explored etching repair strategies for nickel absorber layers and focused electron beam induced deposition of ruthenium capping layers. Nickel has demonstrated higher EUV absorption than the standard TaN absorber layer and thus thinner films and improved optical quality can be realized. A thin (~3nm) Ruthenium is commonly used as a protective capping layer on the Mo-Si EUV multi-layer mirror which mechanically and chemically protects the multi-layers during standard mask-making procedures. The gas field ion microscope was used to investigate helium (HIM) and neon (NIM) ion beam induced etching (IBIE) of nickel as a candidate technique for extreme ultraviolet (EUV) lithography mask editing. No discernable nickel etching was observed for helium exposures at 16 and 30 keV in the range of 1x1015-1x1018 ions/cm2, however transmission electron microscopy (TEM) revealed subsurface damage to the underlying Mo-Si multilayer EUV mirror. Subsequently, neon beam induced etching at 30 keV was investigated over a similar range and successfully removed the 50 nm thick nickel absorber film at a dose of ~3x1017 Ne+/cm2. TEM imaging, however, also revealed subsurface damage in the underlying Mo-Si multilayer. Two damage regimes were apparent in the EUV multi-layer reflector films, namely: 1) beam induced mixing of the Mo-Si layers and 2) nano-bubble formation. Utilizing our new EnvizION ion-solid Monte Carlo simulation we have correlated the observed damage regimes to: 1) the nuclear energy loss and 2) critical implant concentrations.

Electron beam induced deposition (EBID) also been used to deposit ruthenium capping/protective layers. Several ruthenium precursors were screened and so far liquid bis(ethylcyclopentyldienyl)ruthenium(II) (C7H9RuC7H9) has been successful in depositing ruthenium containing deposits. The purity of the nanodeposits produced at 5 keV and 1.4 nA has been characterized energy dispersive x-ray spectroscopy and the as-deposited composition only contains approximately 10% Ru and 90% C. We will describe various chemically assisted and a new synchronized pulsed laser-assisted EBID approaches that we are exploring to purify the ruthenium EBID deposits and will show how each process affects the underlying Mo-Si multi-layer mirror.

9048-22, Session 6

Effect of cleaning chemistries on surface energy and adhesion on EUV masks, substrates, and multilayers

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Nanoparticle contaminants on mask blanks can be added during handling, processing, and cleaning steps. As a mask blank passes through various processes or environments, the force of adhesion between the contaminant particles and the mask blank surface can be modified. These changes to the adhesion properties of the particle-mask blank system will affect how easily the contaminants can be removed during cleaning. Quantification of these changes in adhesion can provide a rational basis for process development or even the selection of materials and chemicals.

When a nanoparticle contacts a surface, the van der Waals, electrostatic, and capillary/surface tension forces can dominate the interaction. The van der Waals force, which is always present, can dominate when electrostatic charges and relative humidity are minimized. Factors like particle size and shape, surface roughness, and surface deformation have a large effect on adhesion, and small changes in these particle and substrate properties can alter the van der Waals force by several orders of magnitude.

The force of adhesion between a nanoparticle and a surface can be characterized directly or indirectly. An atomic force microscope (AFM) can provide direct adhesion force measurements. Measurements of contact angles or surface energies are an indirect method of estimating changes in adhesion behavior. The time-stability of surface condition state generated by exposure to various cleaning chemistries can be quantified by measuring adhesion forces, contact angles, and surface energies versus time.

9048-23, Session 6

Direct measurement of carbon contamination topography on patterned EUV masks

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Radiation-induced carbon contamination is one of the remaining issues for extreme ultraviolet (EUV) lithography. Current carbon contamination research is primarily focused on the lifetime of the multilayer surfaces, determined by reflectivity loss and reduced throughput in EUV exposure tools. However, contamination on patterned EUV masks can cause additional effects on absorbing features and affect the printed images. In our previous work, various techniques were used to confirm the carbon contamination on the sidewall of mask absorbers. In order to further understand the effects of carbon contamination topography on mask absorbing features, direct measurements of transmission electron microscope (TEM) cross-section images were used to characterize the contaminated features.

In this work, we investigate the contamination topography using cross-section TEM image analysis on four different masks. TEM specimens of contaminated features from silicon and ruthenium capped EUV masks were prepared using a dual beam FIB. Two of these masks were sponsored by the INVENT association with 6-inch glass substrate and a silicon capping layer, and the other two were ruthenium-capped masks including a 6-inch glass mask from SEMATECH and a custom EUV mask by LBNL built on a 4-inch silicon wafer for easy cleaving for TEM sample preparation process. We conducted the contamination experiment with three different sources including EUV, out-of-band, and electron induced processes. Non-uniform and asymmetric shapes were observed

at various feature sizes and pitches on different masks. Thickness measurements from each experiment are provided. Shadowing effect and geometric analysis on the contamination topography is also discussed.

Using the real contamination topography, film properties were determined based on multiple irradiation conditions and film thickness measurements. A lithographic simulation was then developed and compared to the actual printing results from multiple masks to ensure accuracy. Various feature sizes, duty cycles, and mask absorber heights were modeled to predict the effects of carbon contamination on the printing performance of patterned EUV masks.

9048-24, Session 6

Particle control challenges in process chemicals and ultrapure water for sub-10nm technology nodes

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As the critical device size reduces towards the sub 16 nm HP node, the critical size of particulate defects extends to sub 10 nm dimensions. A particle with height of 1 nm and a lateral dimension of 40 nm on an EUV mask substrate will be printed on the wafer. Similarly a sub 10 nm particle on the surface of wafer during FinFET gate patterning may result in a reliability issue. Particles embedded in resist or added on the wafer surface during resist development and rinse processes will result in device failure.

During different processing steps from lithography to packaging, wafers are frequently in contact with UPW, chemicals, solvents, etc. Therefore, particles in solutions will eventually end up on the wafer surface. Furthermore, if there are nonvolatile residues in the UPW and chemicals, these residues will dry on surface and result in so-called watermarks. As the density of critical particles in solutions drastically increases by decreasing the size of the particle that must be removed, particle control in solutions becomes one of the biggest challenges of semiconductor manufacturing for sub 10 nm HP regardless of choice of lithography technology or transistor architecture.

As the critical dimension of particles approaches the limits of surface interactions, most physical and chemical properties of particles are affected by surface interactions and should be revisited. Particle-surface interaction will drastically affect particle transport, adhesion and removal. A team of researchers at the NanoDefect Center in SEMATECH has started extensive study of science of sub 10 nm particles in solutions. These activities include sub 10 nm particle detection, counting, deposition, characterization, filtration, and removal.

In this paper, we will discuss challenges of particle control in solutions and report our latest advancements in detection, characterization, and control of sub 10 nm particles in solutions. Our data will be complemented by TEM, AFM, and SEM characterizations of sub 10 nm particles. Also, other sources of contamination in UPW and chemicals will be discussed.

9048-25, Session 7

EUV source-mask optimization for 7nm-node and beyond

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Tachyon SMO (source-mask optimization) has been a key enabler for 20nm node and beyond with 193nm immersion lithography [1]. ASML NXE: 3300 EUV scanners [2, 3] with a set of standard off-axis illumination pupils are being introduced for the 10-nm node since 2013. For the 7nm node, freeform illumination pupils are required for low k1 EUV lithography (NA=0.33). As a result, a Tachyon M3D+ [4] and NXE-SMO solution have been developed to support FlexPupil, an illumination option extending the capabilities of the flexible illuminator designed by Zeiss and ASML built in NXE:33x0 scanners.

There are new challenges in EUV SMO primarily due to the scanner's reflective optical system. The oblique chief ray angle and mask topography introduce mask-induced telecentricity, mask defocus detuning, and mask shadowing effects that lead to pattern- and slit-dependent shift and bias. The smaller wavelength increases the effective aberration fingerprint across the slit. Furthermore, the discrete design of NXE:33x0 illuminator presents additional challenges compared to the more continuous DUV FlexRay illuminator.

In this paper we introduce new SMO capabilities for NXE:33x0 FlexPupil optimization. New algorithms have been developed that fully exploit the design of switchable mirrors and light distribution of the NXE:33x0 flexible illuminator. The fast EUV M3D+ model enables novel pupil symmetries and mask defocus optimization. This mitigates the bias and pattern shift due to shadowing and telecentricity and reduces the sensitivity to aberrations. New optimization flows include initial mirror state rendering followed by discrete mirror state and mask co-optimization. The optimized pupils are fully compliant with NXE:33x0 scanner specifications.

We will show enhanced imaging performance of NXE SMO on 7nm DRAM and logic standard cells, via and metal layers, as well as cut-masks.

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9048-26, Session 7

EUV overlay strategy for improving MMO

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EUV lithography (EUVL) is the most promising technology to extend the resolution limit, and is expected to be used if the enough source power is delivered and mask defect mitigation method is developed. However, even in that case, the number of EUV steps will be restricted by its high cost, and ArF immersion will still take a major role in the chip manufacturing. Therefore, it is important to check and improve the mix-match overlay (MMO) between EUV and ArF immersion steps.

EUV system is totally different comparing with the previous optical system. EUV uses mirror optics and electrostatic clamp instead of lens optics and vacuum chuck, which can make overlay with previous mask step worse. In this paper, we evaluate MMO with ArF immersion system by comparing with dedicated chuck overlay (DCO) of ArF immersion. The factors of overlay error are analyzed by breaking down into field, wafer and random components. The analysis shows that more improvement in field components is necessary, and several methods are suggested like in-chip-overlay, RegC, and high order correction per field. And dynamic

overlay correction on reticle and mirror heating is also suggested even though current EUV system doesn't show the effects because of its low throughput.

9048-27, Session 7

Prospects of DUV OoB suppression techniques in EUV lithography

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Though scaling of source power is still the biggest challenge in EUV lithography (EUVL) technology era, CD and overlay controls for transistor's requirement are also precondition of adopting EUVL in mass production. Two kinds of contributors are identified as risks for CDU and Overlay: Infrared (IR) and deep ultraviolet (DUV) out of band (OOB) radiations from laser produced plasma (LPP) EUV source. Infrared from plasma generating CO2 laser that causes optics heating and wafer overlay error is well suppressed by introducing grating on collector to diffract IR off the optical axis and it is confirmed by operation of pre-production tool (NXE3100). EUV and DUV OOB which are reflected from mask black boarder (BB) are root causes of EUV-specific CD error at the boundaries of exposed shots which would accompany a lot of productivity loss unless sufficiently suppressed. Therefore, reflectivity control from mask BB is one of the key technologies that must be developed prior to EUV mass production.

In this paper, quantitative assessment on the advantage and disadvantage of potential OOB solutions will be discussed. EUV and DUV OOB impacts on wafer CDs are measured from NXE3100 & NXE3300 experiments and significant increase of DUV OOB impact from NXE3300 are observed compared to NXE3100. There are three ways of technology being developed to suppress DUV OOB: spectral purity filter (SPF) as a scanner solution, multi-layer etching as solution on mask, and resist top-coating as a process solution. PROs and CONs of on-scanner, on-mask, and on-resist solution for the mass production of EUV lithography will be discussed.

9048-28, Session 7

Feasibility of compensating for EUV field edge effects through OPC

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As EUV Lithography (EUVL) continues to evolve, it offers a possible solution to the problems of additional masks and lithography steps that drive up the cost and complexity of 193i multiple patterning. EUVL requires a non-telecentric reflective optical system for operation. This requirement causes EUV specific effects such as shadowing. The absorber physically shadows the reflective multilayer (ML) on an EUV reticle resulting in pattern fidelity degradation. To reduce this degradation, a thinner absorber may help. Yet, as the absorber thickness decreases, reflectivity increases in the 'dark' region around the image field, resulting in a loss of contrast. The region around the edge of the die on the mask of un-patterned absorber material deposited on top of ML, known as the image border, is also susceptible to undesirable reflections in an ideally dark region. For EUVL to be enabled for high-volume manufacturing (HVM), reticle masking (REMA) blades are used to shield light from the image border to allow for the printing of densely spaced die. When die are printed densely, the image border of each neighboring die will overlap with the edge of a given die resulting in an increase of dose that overexposes features at the edge of the field. This effect is convolved with a fingerprint from the edge of the REMA blades. This phenomenon will be referred to as a field edge effect.

One such mitigation strategy that has been investigated to reduce the field edge effect is to fully remove the ML along the image border to ensure that no actinic-EUV radiation can be reflected onto neighboring die. This has proven to suppress the effect, but residual out-of-band radiation still provides additional dose to features near the image border, especially in the corners where three neighboring fields overlap. Measurements of dense contact holes (CHs) have been made along the image border with and without a ML-etched border at IMEC in collaboration with Micron using the ASML NXE:3100. The implementation of these measurements allow for further mitigation, i.e., compensation by OPC. Mentor Graphics' Calibre software uses the scanner's point spread function and convolves it with the mask layout to generate a flare map. It also has the capability to add additional dose to the image border which can be optimized to fit the experimental data. This includes the transition region between the image field and border that results in a linear roll-off of dose due to partial shadowing of the REMA blades. By applying this flaremap that accounts for neighboring die to the already calibrated optical and resist models, OPC can now be enabled to compensate for field edge effects.

This study has two goals. First, we will show that OPC can be used to compensate both for field edge effects with and without a etched ML border. The second is to investigate the limitations that exist for OPC in the areas altered by neighboring die. This will predict when a process to mitigate the field edge effect is needed to enable EUV HVM.

9048-29, Session 7

Comprehensive defect avoidance solution for mitigating EUV mask defects

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EUV mask blank defectivity remains a key challenge that could delay the adoption of EUV lithography. Defect avoidance based techniques have been proposed as an effective means to tolerate mask defects. These techniques rely on inspection of mask blanks to first determine defect locations. The position of the design pattern, which needs to be written on the mask, can be shifted relative to the mask to avoid the defects. Several approaches and results have been shown for such pattern shift based defect avoidance. A similar, but more general mask floorplanning based defect avoidance has been proposed as well, that allows each die copy on the mask to be placed independently. In addition to floorplanning, rotation of the mask pattern has also been explored, either small-angle or 180 degrees and flips. Recent techniques have also looked at methods that can tolerate defect position inaccuracy.

In this work, we propose a global optimization based multi-layer mask floorplanner to avoid EUV mask defects that allows both floorplanning of the various die copies on the mask, and small-angle rotation of the entire mask pattern. Our approach enables exploring all the possible degrees of freedom that defect avoidance permits, allowing mask makers to choose the best option. Our solution methodology uses a combination of random search of the entire solution space, along with gradient descent. Some key features of our methodology are as follows:

• Multi-layer: Our formulation enables global optimization of multiple layers of a design with both pattern shift and floorplanning. Our method allows the entire mask pattern corresponding to each layer to be shifted independently, while keeping the relative location of the various die copies same to ensure alignment.

• Continuous: Our method explores the continuous solution space, instead of making discrete moves as done in the previous work on defect avoidance floorplanning.

• Generic: Our optimization method can easily be adjusted to different

EUV mask defect models.

• Robust: Since mask blank inspection tools are unable to report defect locations accurately, our method can find a floorplan that is robust to a given defect position inaccuracy.

Preliminary results on the polysilicon 8nm ARM CORTEX M0 layout shows that by using the additional flexibility of floorplanning and rotation, our method can improve the mask yield significantly compared to optimal pattern shift. For masks with 30 Gaussian defects of full width half maximum 50nm and height 2nm, pattern shift can improve the mask yield from 0% to 24%. Our floorplanner can improve it further to 99%. Although our method can significantly improve the efficacy of defect avoidance over current approaches, it suffers from a slower running time. We plan to look into techniques for improving the speed of our method.

9048-30, Session 7

Pattern fidelity verification for logic design in EUV lithography

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We verify pattern fidelity in EUV lithography quantitatively by experiment and rigorous simulation.

It is well known that the shadow cast by oblique illumination on the mask topography causes CD differences between horizontal and vertical lines in 1D line-and-space patterns. Additionally, for 2D logic patterns, interaction occurs between the horizontal and vertical edges. The interaction degrades the 2D pattern fidelity on wafer. This means that a simple biasing approach, as could be applied for OPC to the 1D patterns, is no longer sufficient for compensation of pattern fidelity for actual 2D logic patterns.

A more accurate compensation is enabled by Mentor Graphics' mask topography aware OPC software1-2) that adopts Domain Decomposition Method (DDM) model to consider the edge interaction. The DDM can capture the 2D pattern fidelity induced by mask topography.

We applied DDM OPC to 2D logic patterns representative for the 10 nm generation. This node is at the resolution limit of the current EUV scanners with NA 0.33. We make recommendations for further improvement of OPC modeling by comparing OPCed and non-OPCed logic patterns.

In addition, other sources of wavefront error (WFE)3), such as illumination shape, z-position shift of a mask, aberrations and defocus on a wafer, can be present in the optical system, leading to pattern deformation. By simulation we show the mechanism by which WFEs degrade pattern fidelity.

Our study has two goals. First, we will validate the effectiveness of the DDM OPC in 2D logic patterns. Second, we will investigate the impact of all the WFEs on pattern fidelity to improve OPC modeling and to propose new metrics that can detect slight changes in pattern fidelity.

Toward the goals we have put together a variety of 2D logic layouts as shown in Fig.1. It contains eight variations with the combinations to account for the effective compensation of pattern fidelity under the different interactions between edges. This clip is placed through slit on the reticle design. The clip received DDM OPC, which is orientation- and mask topography-sensitive. We show how the DDM OPC treatment changes through pattern orientation and slit position. This reticle will be exposed on an EUV NXE scanner of ASML.

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9048-31, Session 7

EUV OPC modeling and correction requirements

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As the adoption of EUV lithography has shifted to smaller nodes, understanding the impact of effects like focus, mask process, and through-slit variation in OPC modeling is getting more and more important. The addition of model components in OPC also brings new challenges and complexities in the OPC anchoring and correction flow. For example, as shown in Figure 1, the V-H print difference across the exposure slit is usually assumed to be constant in the OPC model; however, there is a subststantial variation feature-to-feature on the wafer. This difference already introduces a residual error that needs to be addressed in the OPC modeling and OPC integration. In this paper we discuss the EUV OPC modeling challenges and potential solutions, as well as OPC integration requirements to support the forthcoming application of EUV lithography. 10-nm-node OPC modeling is considered as an example. Wafer and mask process data were collected for calibration and verification patterns, to understand the mask making error/OPC model interactions. Several factors, including compact mask topography modeling impact, were analyzed by means of rigorous simulations and model fitting. This was performed on a large-scale data set, to ensure accurate characterization of the OPC modeling strategies, using a large number of patterns. Model accuracy and calibration cost-minimization paradigm were re-evaluated to understand the consequences of empirical resist models. Based on this 10-nm-node study, we also make a projection to smaller technology nodes, and discuss implications of EUV modeling and OPC flow requirements for these nodes.

9048-63, Session PTue

EUV source modeling

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Despite significant improvements using high energy tin plasma, EUV source power and efficiency continue to be significant issues for the semiconductor industry to enable successful EUV platform commercialization. A laser-produced plasma (LPP) radiation source is one of the most promising options for the light source. A suitable LPP source will require an efficient conversion of the incident laser pulse energy to EUV radiation in a narrow spectral range, as well as nearly complete control of debris transport.

Developing a good understanding of the physical processes in EUVL plasmas is challenging, as it requires accurate modeling for the atomic physics of complex atomic systems, frequency-dependent radiation transport, hydrodynamics, and the ability to simulate emergent spectra and images that can be directly compared with experimental measurements. We have developed a suite of plasma and atomic physics codes to simulate in detail the radiative properties of hot plasmas and guide the development of higher efficiency plasma radiation sources. HELIOS-CR is a 1-D radiation-magnetohydrodynamics code used to simulate the dynamic evolution of laser-produced and z-pinch plasmas. The results of HELIOS-CR simulations can be post-processed using multidimensional spectral analysis code SPECT3D to generate images and spectra that include instrumental effects, and therefore can be directly compared with experimental measurements. The SPECT3D

package computes filtered and monochromatic images, and streaked, time-integrated, and time-gated spectra based on 1-D, 2-D, or 3-D radiation-hydrodynamics results. Simulated images and spectra can be computed with instrumental effects included (e.g., spectrometer resolution, time gating, filtering) in order to facilitate comparisons with experimental data. PrismSPECT, which shares many essential physics models with SPECT3D, computes the ionization dynamics and spectral properties of single-cell plasmas (i.e., a single volume element of uniform temperature and density), and is designed to conveniently calculate plasma properties over a grid of input parameters.

Atomic data required for accurate treatment of EUV emitting plasmas were computed using the ATBASE suite of codes. Energy levels, photoionization cross sections, oscillator strengths, and autoionization rates are calculated using a configuration interaction model with Hartree-Fock wavefunctions. Collisional coupling between states is complete – i.e., all thermal (non-autoionizing) and autoionizing states are collisionally coupled – with electron-impact collisional excitation and ionization cross sections computed using a distorted wave model. For high-Z plasmas like tin, at plasma conditions typical of EUVL radiation sources, both relativistic and configuration interaction (CI) effects are important and must be taken into account in determining the line positions and intensities for the transition arrays of interest. Also, there is a very large number of configurations with open subshells that can contribute to the opacity.

The tools developed at Prism Computational Sciences are being routinely used by many universities, national labs and corporations to understand the fundamentals of high energy density plasma.

We will present results which demonstrate impact of various parameters (laser power - pre-pulse and main pulse, spot size, pre-pulse and main pulse delay, etc.) on efficiency, and shows possible improvement areas to achieve higher efficiency.

9048-64, Session PTue

A study of the effect of pellicle-support structures on aerial-image quality in EUV lithography by rigorous electromagnetic simulation

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One of the problems facing extreme-ultraviolet (EUV) lithography in mass production is defect control of the EUV mask. To protect the mask from contamination during handling, several studies recommended the use of a pellicle. However, the pellicle membrane must be very thin due to EUV absorption. This suggests that a suitable pellicle support structure, such as a rectangular or hexagonal mesh, should be used to avoid deflection of the membrane by gravity.

Experimental results by others have previously shown that a pellicle support structure can produce an interference image on the wafer. This suggested that a pellicle support structure cannot be used. In this paper, we re-examine this issue by computer simulation.

An approximate model of pellicle support structure based on geometrical-optics propagation of the shadowed incident and diffracted light through the projection optical system has been reported by us. Simulation results based on this model have shown that a pellicle support structure can produce very distinct shadows on the wafer under coherent illumination condition, as shown in Fig. 1. However, the geometrical-optics approximation neglects the diffraction of the EUV light through the pellicle support structure.

Rigorous electromagnetic simulation of the diffraction of EUV light through a pellicle support structure is challenging due to the large size of the structure, which is typically several microns in X, Y and Z, compared to the wavelength of the EUV light, 13.5nm. Fortunately, the recently introduced pseudo-spectral time-domain (PSTD) method allows this problem to be tackled very efficiently on an ordinary workstation. Fig. 2 shows the rigorously computed shadow of the light incident on an EUV mask produced by a rectangular, 5mm-thick, 0.1mm-wide pellicle support structure with period of 3.2mm in X and Y. The result of electromagnetic diffraction through the pellicle support structure is seen to be a blurring of the shadow. Notice that the shadow is elongated in the X direction due to the oblique direction of incidence (6o from left to right). Further blurring of the shadow will occur due to the finite partial coherence of the incident light. There is also blurring of the shadows of the diffraction orders as the light propagate through the pellicle support structure a second time on its way to the EUV optics.

In this paper, we will present the rigorous model of pellicle support structure in detail. Its results will be compared to those of the geometrical-optics model to identify the limit of validity of the latter. Then we will use the rigorous model to show how the size and shape of the pellicle support structure, together with partial coherence s, can be optimized to produce a sufficiently blurred interference image of the pellicle support structure on the wafer, so as to preserve the original aerial-image contrast as much as possible and to result in an acceptable aerial image.

9048-66, Session PTue

Emission properties of Tin droplets laser-produced-plasma light sources

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Extreme ultraviolet lithography (EUVL) which uses extreme ultraviolet radiation in the 2% band at a wavelength of 13.5nm is the leading candidate for next-generation lithography technology. With the use of shorter characteristic wavelength, EUVL can print a smaller feature size. And the high reflective (of about 70%) of Mo/Si multilayer mirrors [1] at these wavelengths makes it possible to collect most of the EUV radiation for the light source. International Technology Roadmap for Semiconductors (ITRS) has listed EUVL as the main solution to resolve 16nm nodes and below.

Three kinds of systems for generating EUV light are known in general, in which laser produced plasma light source have been extensively studied as an efficient EUV light source. It generates 13.5nm radiation through irradiating a target material with a laser beam creating plasma. And the key challenges of laser produced plasma light source to achieve high volume manufacturing is the requirements of high output EUV power and long system life time. By using mass limited targets like small liquid tin droplets, the problems can be greatly relieved. There are many advantages using droplet targets including reachable high repetition rate system, larger photons collection angle, and lower ions debris and energetic particles.

In previous work, experiments based on CO2 laser produced Tin plasma using slab targets showed the different debris mitigation power using hydrogen, argon, helium as buffer gas. The maximum stopping power of argon is three times larger than hydrogen, and one and a half times larger than helium all at a pressure of 2000 Pa.

Now, a droplet dispenser has been designed to provide tin droplets for a laser plasma light source. The dispenser was able to generate 150um tin droplets with the droplets velocities ranging from 8m/s to 12m/s. A high-power pulsed TEA-CO2 laser system and an Nd:YAG laser system irradiated the droplets to produce plasma. The CO2 laser pulse duration was measured to be 70 ns (full-width at half-maximum, FWHM) with 900 mJ output energy by adjusting the pressure ratio of the working gas to CO2 : N2 : He = 100 : 100 : 400 mbar. The Nd:YAG laser works with a repetition rate of 10Hz at a wavelength of 1064nm. The pulse duration is 7ns with 200mJ energy per pulse. A X-ray Spectrometer was placed to detector the EUV spectral composition. Several Faraday Cups and EUV

detectors ware used to measure the angular distribution of the EUV and ions emission of the LPP light source. The influences of laser wave length and pulse energy on the emission properties of plasma light source were all investigated.

9048-67, Session PTue

Design and synthesis of novel resist materials for EUVL

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Currently, the implementation of EUV lithography faces several issues, including the critical challenge of ensuring photoresists that can concurrently achieve narrow line width around 16 nm, low line edge roughness at 3? (1.5nm), and high photosensitivity at 2-10mJ/cm2. To address many of the inherent problems of currently used chemically amplified resist technology, e.g. acid diffusion, sensitivity, post exposure instability, the present project encompasses the design and synthesis of resists that are directly sensitive to radiation without utilizing the concept of chemical amplification (CARs). These new resist materials, while highly sensitive to photons of various wavelengths, function as non-chemically amplified resists. This resist design is accomplished by polymeric and molecular resists that are prepared from monomers containing sulfonium groups. In order for a polymer to be directly sensitive to wavelengths, a highly sensitive group must be introduced into the polymer units. Sulfonium groups have long been found to be sensitive to UV photons. For this reason, sulfonium groups were chosen as radiation sensitive groups in non-CA resists. Herein the design and synthesis of non-chemically amplified negative tone electron-beam and EUV resists based on the sulfonium and methylmethacrylate functionalities with high sensitivity is presented. We have synthesized homopolymers of MAPDST (4-(methacryloyloxy)phenyl dimethylsulfonium triflate) and MANTMS (1-(4-(methacryloyloxy)naphthalen-1-yl)tetrahydro-1H-thiophenium trifluoromethanesulfonate) monomers using free radical polymerization with 2,2'-azobisisobutyronitrile (AIBN) initiator at 60 °C temperature in tetrahydrofuran (THF) solvent for 2 days under nitrogen atmosphere. Also, we have synthesized copolymers of MAPDST with MMA (methyl methacrylate), VCBZ (9-vinyl carbazole), STYCOOH (4-carboxy styrene) and hydroxyl styrene monomers using the same free radical polymerization method initiated by AIBN at 60 °C in a combined organic solvent, acetonitrile (CH3CN) and THF for 2 days under N2 atmosphere. A sulfonium functionality containing dendrimer has also been prepared. The synthesized homopolymers, copolymers of MANTMS and MAPDST monomers and dendrimer have been characterized using FT-IR, NMR analysis and the molecular weights of the polymers were calculated using GPC analysis. The copolymer compositions and glass transaction temperature (Tg) values are calculated using 1H NMR and DSC analysis. Initially, the homopolymer of MAPDST and MAPDST-MMA copolymer were evaluated by EB lithography. Resist solutions (3% w/v) were prepared in methanol solvent and coated on a 2? silicon wafers with a softbake at 90 ºC. The resist coated films were exposed to e-beam using 20 keV electron beam under low electron dose values (10 to 55 µC/cm2) to achieve 20 and 16 nm line patterns with L/S or L/2S line space. The exposed resist coated films were subjected to post exposure bake at 100 ºC and developed in 0.022 N TMAH aqueous solution. Thickness of films was measured around 50-120 nm using optical profilometer. Our investigation showed that these new materials can be useful for the development of highly sensitive non-chemically amplified photoresists for sub 20 nm EUVL.

9048-68, Session PTue

Imaging performance of attenuated phase-shift mask using coherent scattering microscope

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Phase shift mask (PSM) for extreme ultraviolet lithography (EUVL) provides higher image contrast and lower shadowing effect than those of the conventional EUVL binary intensity mask (BIM) in 16-nm half-pitch node technology and beyond. Thus, we have proposed a PSM consisting of a 16.5 nm-thick TaN absorber layer and a 24 nm-thick Mo phase shifter on 2 nm-thick Ru-capped Mo/Si multilayers.

In this study, we fabricated the PSM and investigated its imaging properties using coherent scattering microscope (CSM). The PSM stack was fabricated and its reflectivity was measured by EUV reflectometer. As a result, the PSM stack shows reflectivity of 13.7%, which is close to the simulation result (12.7%) at 13.5nm centroid wavelength. This PSM stack was patterned to have 88nm, 100nm and 128nm line–and-space patterns by e-beam writing. Absorber stack consisting of TaN and Mo was etched with SF6 gas in coupled plasma type etching system. A cross-sectional TEM image shows high etching selectivity and aspect ratio.

The diffraction image of mask captured by CSM is used to reconstruct the pattern image of the mask. The mask image reconstruction is accomplished by an iterative process of Fourier transform and inverse Fourier transform. Intensity profile of reconstructed PSM image clearly shows valley points of intensity between lines and spaces caused by destructive interference of phase shift. Also intensity ratio of 1st to 0th order diffraction patterns in PSM was higher than that of BIM, improving patterning properties due to increased informative photons. Furthermore, improved lithographic properties of PSM, such as image contrast and H-V CD bias, were evaluated with illumination condition (0.33 NA, ? = 0.9) by CSM.

9048-69, Session PTue

Optimization of processing parameters and metrology for novel NCA negative resists for NGL

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Development of photoresist materials for extreme ultraviolet lithography (EUVL) technology is one of the major challenges. In addition to answering the well known challenges presented by EUV radiation like the high absorption coefficients, sensitivity, resolution, etch resistance and line edge roughness (LER) the demands of high-volume production have to meet. The main focus of this paper is on the development of EUV non chemical amplified resists and ancillary materials because this technology is the most likely option for sub-20-nm half-pitch patterning. Extensive initial e-beam exposure is provided as a prelude to EUV exposures. (4-(Methacryloyloxy)phenyl) dimethylsulfonium triflate (MAPDST) homopolymer (II) was synthesized by reacting monomer (4-(methacryloyloxy)phenyl)dimethyl sulfonium triflate) (MAPDST) (I) with AIBN (azobisisobutryonitrile) initiator, 1 wt% relative to the monomer in acetonitrile at 60 °C under nitrogen atmosphere for 2 days. High resolution patterning of designed hompolymer (II) resist was carried out using 20 KeV e-beam lithography. The unexposed polymer was polar due to its ionic character and therefore soluble in polar solvents such as water. Unexposed regions of the resist film readily dissolved in an

aqueous 0.02 N TMAH developer, while the exposed regions (patterns) were maintained after dipping the exposed resist film in developer. These are characteristics of a non chemically amplified negative polymeric resist. The homopolymer (II) exhibited 20 nm as well as 16 nm L/2S patterns at a dose of 20 μC/cm2.

During resist preparation, spin coating and exposure steps, the temperature treatments (Pre Bake, post bake and during development) could seriously influence resist exposure characteristics (contrast and sensitivity), resolution and uniformity (regularity, shape, LER, surface roughness) of the final structures. The temperature can substantially alter the speed of solvent removal during drying and affect surface topographies of thin resist films.. Therefore the effect of the temperatures (Pre-Bake and post-bake) on the key performance parameters (sensitivity, contrast, resolution) of the MAPDST-homopolymer resist were investigated. We have also focused on the impact of resist pretreatments before the plasma etching step based on resist chemistries. We investigated the impact of pretreatment on the resist etch resistance and surface roughness of blank photo resist films exposed to plasma etching processes. In a second part, we reproduced those experiments on photo resist patterns to evaluate their impact on critical dimension (CD) control and LWR transfer. The chemical modifications of the photo resist films exposed to plasma and temperature treatments are investigated by Fourier transformed infrared (FTIR). The root mean square (RMS) surface roughness of the MAPDST-homopolymer resist thin film is measured by atomic force microscopy (AFM) in tapping mode. The evolution of surface roughness of reference and cured resists has also been investigated as a function of plasma etching time and these various conditions. Our results provide a clearer understanding of how these critical steps in the lithographic imaging process will affect extendibility of the non-CA resist concept to sub 16 nm features. Non-Chemically amplified (non-CAR) resists are anticipated to be strong candidates for nano-fabrication as per the ITRS road map. EUV photodynamic and exposure data will be covered in addition to the e-beam data.

9048-70, Session PTue

SEMATECH's cycles of learning test for EUV photoresist and its applications for process improvement

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With current improvements in exposure source power, novel resist materials, and post processing techniques, EUV is getting closer to the production environment. Improvements in LWR, sensitivity, and resolution are still required to meet manufacturing requirements. As reported continuously over the years, we established cycles of learning tests that are utilized to measure capability for production use. Thanks to SEMATECH core and associate members' kind attention to the project, numerous samples were tested and they were based on the best performing resists from our associate members. This year we completed the first round of evaluation for under-layers, for lines and spaces, and for contact holes. We also applied track based techniques to drive both low line edge roughness control and enlarge the process window with techniques such as FIRMTM and track based smoothing.. In this paper we will discuss about the results from cycles of learning test in terms of photospeed, Exposure latitude, LWR, LPC (Line pattern collapse), and process window for all the cycles of learning materials and show postprocessing results of the three best line and space resists when combined with different FIRMTM materials.

9048-71, Session PTue

Success rate improvement of defect mitigation with EUV actinic blank inspection prototype for 16nm hp

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For Extreme Ultra-Violet Lithography (EUVL), fabrication of defect free multi-layered (ML) mask blanks is one of the difficult challenges. ML defects come from substrate defects and adders during ML coating, cannot be removed, and are called as phase defect (PD).

Ideally, we would like to have an ML blank with no printable PD, but this is one of the difficult challenges. And even to reduce PDs, high investments will be needed for good blank yield by improving substrate material, polishing, blank handling, ML coating and so on. However, if we can accept ML blanks with certain counts of PDs, the blank yield will be drastically up and high investments won't be needed. Some researchers have been proposing use of such blanks with certain numbers of PDs by defect mitigation schemes. Those proposals are coverage of PDs by absorber pattern [1], proximity repair of mask absorber pattern to compensate the influence from PD [2]. In each scheme, the PDs need to be identified and located during ML blank defect inspection before absorber patterning for pattern shift and compensation. To locate PDs on the blanks accurately and precisely, Fiducial Marks (FM) on ML blanks are needed for mask alignment and defect location information. The proposed requirement of defect location accuracy is better than 10 nm [3].

In previous study [4], we fabricated FMs by resist exposures by E-Beam writer and etching process. And we inspected FMs with EUV Actinic full-field mask Blank Inspection tool developed by MIRAI Selete (MIRAI ABI). Then we recommended optimum FM shape for better location accuracy. And in the latest study, we inspected FMs and defects with EUV ABI developed by EIDEC-LaserTec (LT ABI) for 16 nm hp. Then we estimated defect location accuracy based on the location detection of FM and defect images by LT ABI high-Magnification Optics as shown in Figure 1 and 2. And we found that the LT ABI tool performance on defect location accuracy is necessary to be improved to meet the requirement.

In this paper, we will report the improvement result of defect location accuracy and defect mitigation success rate by LT ABI.

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9048-72, Session PTue

Time dependency of progressive defect growth on EUV masks

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Mask defect control is one of the critical issues for the high volume manufacturing (HVM) of extreme ultraviolet (EUV) lithography [1]. It is known that progressive defects on masks cause wafer print failures in

deep ultraviolet (DUV) [2]. In EUV, the same problem might occur. To figure out the time dependency of progressive defects growing on EUV masks, a series of experiments are being performed.

One issue that could cause progressive defects on EUV masks is residue from cleaning chemicals that remain on masks after the cleaning process. During EUV exposure cleaning residues may cause a chemical reaction and grow as progressive defects.

In order to mimic HVM EUV exposures without the availability of a high power EUV source, the exposures will be completed with an electron gun. Since the surface chemistry due to EUV exposure is believed to be caused by secondary electrons generated by the primary EUV photon, substituting an electron gun to provide secondary electrons at the surface should be a suitable replacement. During exposure with the electron gun, the number of secondary electrons per area generated at the surface will be significantly higher than the number of secondary electrons per area during EUV HVM exposure, so these tests may represent an accelerated EUV exposure process.

The cleaning chemistries tested include SPM and SC-1 [3, 4]. The metrology will be based on x-ray photoelectron spectroscopy (XPS) and time of flight secondary ion mass spectroscopy (TOF-SIMS) to see aggregation of the ions on the surface. Prior work indicated aggregation of the ions due to a 24 hour electron exposure [5]. This current work is focused on understanding the time dependency of that ion aggregation.

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9048-73, Session PTue

Verification of effect of phase defect shape on ABI signal intensity with experiment

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Extreme Ultraviolet lithography is one of the most promising candidates among the next generation lithography options for printing critical layers of 16 nm half-pitch ULSI devices; and this challenge is possibly extendable to devices with 11 nm half-pitch. On the other hand, one of the key challenges of EUVL is to make defect-free mask blanks. Therefore we have developed an actinic dark-field inspection tool to detect multilayer phase defect.

It is widely known that actinic blank inspection(ABI) signal intensity is influenced by phase defects size. For example, large size defect generates large intensity and small size defect generates small intensity. On the other hand, structure of phase defect is complex and there are various shapes of phase defect. For example, some defects have flat-like shapes and other defects have sharp-like shapes. These characteristics may affect not only ABI signal intensity but also defect image intensity on wafer. In previous report, relation between various phase defect shapes and ABI signal intensity was examined with simulation. ABI signal intensity and defect image intensity on wafer are affected by phase defect shape characteristics. When the impact for ABI signal intensity and defect image intensity on wafer by phase defect is considered, phase defect shape should be taken into account for an accurate estimation.

In this study, relation between phase defect shape and its effect is examined with experimental result and simulated result. We prepare programmed phase defect sample which has various types of pit phase defects and every phase defects are measured with AFM precisely. After the sample is inspected with ABI-tool, ABI signal intensity is compared with each phase defect shape. In this study, because all phase defect shapes are measured, relation between ABI signal intensity and phase defect shapes is verified accurately. According to experimental result, ABI signal intensity is affected not only by phase defect volume, but also by phase defect shape.

Also, phase defect model for simulation is created with AFM data and effect of defect model shape on ABI signal intensity is examined. In this simulation, two types of phase defect models are created and their gap is examined. One is Gaussian shape model which is created with defect size(depth, width). Another model is created with AFM measurement data. According to comparison between inspected result and simulated result, defect model which is created with AFM measurement data shows more similar tendency to experimental result compared to Gaussian shape model.

In this presentation, importance of phase defect shape will be mentioned.

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9048-74, Session PTue

Modeling of the spatial and temporal evolution of plasmas for the EUV source produced from a Sn droplet irradiated by multiple laser pulses

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EUV source at λ=13.5nm has been studied toward the realization of next generation microlithography, especially to obtain high output (>200W) with high efficiency (>5%). New pumping scheme has been proposed by irradiating a small Sn droplet by weak prepulse laser to produce preformed plasma with an optimized density for EUV emission, when the plasma were heated by the main laser pulse. The pumping scheme is used to produce the extended plasma region from initial droplet size of ≈10μm to >100μm, giving rise to the averaged ion density of the plasma of 1019/cm3. It has been shown that the conversion efficiency (CE) to the EUV emission to 2%BW will increase by decreasing density because the emission spectrum becomes narrow [1]. It will also improve the coupling efficiency of laser energy into target because matching between the size of the laser beam and target is improved. The intensity of the prepulse laser is weak, which causes fragmentation of the target during the melting and evaporation, resulting in the formation of mist [2]. Condensation of vapor also may produce particles. Density distribution of the plasma after irradiation by the main laser pulse as well as the interaction between mist and the main laser pulse may have significant effect to the efficiency. However, in most of existing hydrodynamics codes of the laser produce plasmas, target material is assumed to be in the state of plasma, from the beginning of the irradiation of the laser pulse. Furthermore, in the conventional approaches, it is difficult to reproduce the property of the target material in the two phase region. We investigate the method of modeling hydrodynamics of Sn plasmas taking phase transition from solid to liquid or gas into account. The method is based on Lagrangian hydrodynamics using triangular mesh for the 2 dimensional geometry. The phase transition is taken into account by allowing arbitrary division of the cell to produce separate liquid and gas region. Material state is determined for each cell, so that this method may have advantages for the surface tracking is not necessary, and in the calculation the pressure always decreases monotonously with respect to the volume so that numerical instabilities may be avoided. We will present firstly development of the model including numerical algorithm, secondly validation of the code for simple test problems, and thirdly we will investigate the interaction between prepulse laser to the target and properties of energy deposition and formation and propagation of the

shock wave, and finally we will investigate the fragmentation of the target during expansion. In the each stage of the calculation, the results will be compared with available observations such as the shadowgraph image, which may give size distribution of the particles, as well as measurement of density of the plasmas, to understand complex physics during the formation of the plasmas.

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9048-75, Session PTue

Repetitive operation of counter-facing plasma focus device: toward a practical light source for EUV lithography

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As the latest development status in our counter-facing plasma focus device for extreme ultra violet (EUV) light source, we report its EUV emission properties, plasma conversion efficiency (PCE), electrical properties and lithium materials supply system in 2 pulse examinations and highly repetitive mode.

We have developed the counter-facing plasma focus source which has new concept to reach the target of practical EUV emission level. IHI has developed it with Tokyo Institute of Technology on the base of the main concept which is reduction of total amount of supply material and energy. This light source has two coaxial plasma guns which are aligned face to face. Its peculiarity is that it is enable to accelerate the initial plasma, which is generated at the bottom of plasma guns with laser assist, to the center of light source with the electromagnetic force, and converge and sustain the plasma in a high temperature and high density. This light source has multiple charge and discharge circuits which are separated inductively. A short pulse laser generates initial plasma, and two plasma rings approach, and converge in a stable state at the center area of two counter-facing plasma guns. It is possible that the plasma converges with high temperature and high density, and emits EUV light which longs for 1 micro second or more in a shot. We use lithium supply system for the plasma source material. That enables us to get the light emission of 200mJ/shot in the wave length 13.5nm with energy conversion efficiency about 11%. These characteristics mean the high power EUV emission is consistent with continuous operation in this plasma source. Moreover the debris which is the problem as usual is very few, so it is advantageous to practical use.

Now, we research the behavior at 2 pulse experiment based on single pulse experimental result. We try to observe the high temperature and high density plasma, high energy efficiency and high power output of EUV light, and the difference from the first pulse to the second pulse. Furthermore the performance of each characteristic will be investigated under the condition of repetition such as 1 kHz. We research to understand the influence of continuous operation, and confirm the stability of EUV light emission for practical use. Moreover we will give a presentation of various utility characteristics such as electric charging system which supply energy indeed efficiently and repeatedly, laser irradiation system for plasma excitation, thermal characteristic around electrodes, recovery and stability of vacuum, and the possibility of continuous lithium supply system.

We show the latest experimental results for the EUV emission characteristics, PCE, charging properties and lithium supply system in this EUV emission system. In the near future we will try to demonstrate higher repetition capability and promote a working device for the practical use of advanced lithography system.

9048-76, Session PTue

At wavelength observation of phase defect embedded in EUV mask using microscope technique

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Phase defect embedded in multilayer-coated EUV mask blank is one of the great concerns because the phase defects as small as 1 nm in height (or depth) are printable on wafers. Besides the development of blank inspection technique to detect such printable defects, an understanding of the impacts of the phase defects printed on wafer is necessary to define the critical defects. Exposure test using EUVL mask with programmed phase defects is an effective method to evaluate the influence of phase defects on printed patterns. However, because of the limited capability of current exposure tools, it is difficult to evaluate the impact of phase defect on printed patterns on wafer at the small feature sizes such as half pitch (hp) 16 nm and beyond. On the other hand, several investigations on high magnification imaging technique have been reported as at-wavelength observations of EUV mask such as Fresnel zone plate optics1) and multilayer-coated mirror optics (EUV microscope)2-3) that has a potential to resolve a hp 20 nm lines-and-spaces (L/S).

In this study, a test mask containing hp 64 nm L/S corresponding to hp 16 nm generation and programmed pit phase defects was prepared. Then the test mask was observed by EUV microscope to evaluate the microscope imaging properties for observation of the phase defect impacts. The EUV microscope consists of illumination optics, multilayer-coated Schwarzschild optics, concave mirror, deflecting mirror, and CCD camera3). The Schwarzschild optics also serves as a part of illumination optics where the incident angle of EUV beam for mask illumination is larger than 10 degrees and an angle between the plane of incidence and line pattern direction can be selected in the range from 0 degree to 90 degrees.

When a phase defect existed between two adjacent absorber patterns, observation image intensity of the absorber L/S varied and an impact of a phase defect was predicted as an intensity variation of bright space image. The intensity variation was almost consistent with a simulation result. However, because of the comparatively large tilted illumination and annular pupil condition of the EUV microscope, an intensity variation was not symmetric with respect the phase defect location in X direction or Y direction.

In this presentation, EUV microscope observation images of absorber patterns affected by the phase defects will be shown and the prediction performance of phase defect impact on wafer will be discussed.
This work is supported by New Energy and Industrial Technology Development Organization (NEDO).

9048-77, Session PTue

Potential of solid state laser-driven EUV sources for HVM lithography

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Laser plasma-based sources are now the primary candidates for HVM EUV lithography tools. Solid-state lasers long ago demonstrated high conversion efficiencies (CE) with EUV targets (ref 1). The first EUV laser plasma sources with Tin-based micro-droplet targets used solid-state lasers (ref 2). High power EUV source, powers up to ~60 W (@13.6 nm/2pi/2% bandwidth) with ~3 kW, 15 kHz with CE's of 2.0-2.5% were

reported in 2005 operating at 100% duty cycles for several hours (ref 3). With planar solid tin targets CE values of > 5% have been measured with solid-state lasers (ref 4) and with CO2 lasers (ref 5). At that time only CO2 lasers could provide a clear technology path with commercially available components to the required powers for ASML's HMX 3100 and HMX 3300 EUV HVM stepper tools. In the intervening years more than $1B has been spent on the development of high-power diode pumped solid-state lasers driven principally by new manufacturing technologies and by defense needs. High brightness commercial multi-10 kW systems will soon be available as compact, efficient, rugged platforms with wall plug efficiencies ~ 30%.

We review the impact solid-state lasers will have on EUVL as it rises to meet high volume throughput, usable wafer sensitivities, long lifetime expectations and the demands of smaller feature sizes. Taking advantage of the significant developments occurring in solid-state laser architecture, materials and pulsed laser systems, we examine how technology development pathways specifically designed for EUVL might intercept with current CO2 laser source parameters.

This study is supported by one of the most comprehensive source modeling and simulation program efforts. We have always maintained a theoretical component parallel to detailed plasma diagnostics to be necessary for understanding the complex plasma and radiation dynamics in these laser plasmas (ref 6).

In summary solid-state lasers now offer an alternative path for the next generation of EUV sources for HVM lithography. Advantages will include higher efficiencies, lifetimes, simplicity, and ruggedness with reduced footprint, infrastructure, complexity and costs. Supported by comprehensive simulations including a detailed multilevel non-LTE atomic model coupled to 1D/2D hydrodynamic codes, we describe pathways for this technology to intercept current approaches.

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9048-78, Session PTue

Observation of phase defect on extreme ultraviolet mask using an extreme ultraviolet microscope

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To investigate the impact of phase defects embedded in extreme ultraviolet (EUV) mask blanks on wafer printing, we have developed at-wavelength observation technique that has a potential to resolve a half-pitch (hp) 20 nm lines-and-spaces (L/S) with the image contrast of 0.5. Previous work revealed that a prototype EUV microscope has excellent contrasts of 0.52 for hp 88 nm L/S patterns.[1, 2] In terms of the defect inspection capability, the EUV microscope could detect a 3.7-nm-high residual-type defect in hp 88 nm L/S with more than 40% of EUV light reflectivity decrease compared with reference space patterns.[3]

In this study, to predict an impact of the phase defect on wafer printed image, a programmed phase defect EUV mask was fabricated and observed using EUV microscope that employs EUV light from beam line BL3 of the New SUBARU at the University of Hyogo. The test mask contains the hp 88 and 64 nm L/S and several shapes of the phase defects. To evaluate the effect of the phase defect structure on the EUV microscope images, 2 types of phase defect were prepared. One is vertical propagation in the multilayer from the quartz surface. The other is inclined propagation. [4] The phase defects were located at several positions relative to the absorber lines. To analyze the wafer printability and inspection capability of the phase defect in detail, a lithography simulator was employed to calculate wafer printed image and EUV microscope images. As a result, the EUV microscope can predict the existence and effective position of the printable phase defect with both vertical-growth and inclined-growth, although the EUV microscope does not emulate the image of the EUV scanner completely.?This work was supported by NEDO.

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9048-79, Session PTue

Conversion efficiency of laser-produced Sn plasma EUV light source

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There is increasing interest in high-power extreme-ultraviolet (EUV) laser-based lamps operating in the region of 13.5 nm based on the Mo/Si multilayer mirrors for manufacturing the next generation of microelectronics (ref 1). We have investigated radiative properties and conversion efficiency (CE) of Sn plasma at 13.5 nm by a detailed multilevel non-local thermodynamic (LTE) atomic model including all tin charge states from neutral to fully- stripped. The atomic data calculated by the Hebrew University-Lawrence Livermore Atomic Code (HULLAC) and the relativistic Flexible Atomic Code (FAC). The line positions have been corrected (ref 2) by comparison to experimental spectra and charge-exchange spectroscopy. The net emission of Sn plasma at 13.5 nm is controlled by plasma opacity, hence for obtaining the highest CE, a mass-limited Sn droplet irradiated with either a solid-state laser or double laser pulse irradiation scheme are considered to be promising methods.

We will present the optimum regions for CE of mass-limited targets against density and laser parameters including wavelength, pulse width, and shape by means of hydrodynamic simulation coupled to developed population kinetics codes. The in-band power from mass-limited Sn target predicted based on the available solid state/CO2 lasers.

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9048-80, Session PTue

EUV resist dissolution optimization for CD uniformity and defect control in coat develop track process

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EUV lithography (EUVL) is well known to be a strong candidate for next generation, single exposure sub-30nm half-pitch lithography. Much progress relevant to EUVL has been reported for a decade, however, many issues continue to challenge implementation for volume production. On the other hand, it seems that the coat develop track process remains very similar and in many aspects returns to KrF or ArF dry process fundamentals, but in practice 26-32nm pitch patterning coat develop track process also has challenges with EUV resist.

As access to EUV lithography exposures became more readily available over the last five (5) years, several challenges and accomplishments in the track process had been reported, such as the improvement of ultra-thin film coating, CD uniformity, defectivity, line width roughness (LWR) and so on. The coat-develop track process has evolved along with novel materials and metrology capability improvements.

Coating ultra-thin under layer and resist films and approaches to control resist dissolution to improve CD uniformity, line width roughness (LWR), and defect control are demonstrated utilizing SOKUDO DUO coat develop track system with ASML NXE:3100 exposures in IMEC (Leuven, Belgium) clean room environment. Additionally, we will show the latest lithographic results obtained by novel processing approaches in EUV coat develop track system.

9048-81, Session PTue

Effect of Defects on Extreme-Ultraviolet Pellicle

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Over the past several years, a lot of studies have been reported on the ability of extreme ultraviolet lithography (EUVL) and people have been accomplished a great deal of developing the EUVL technologies. However, several problems which disturb the mass production of EUVL still remain. One of the problems is the defect control. The defects in mask bring not only patterning error, but also the reduction of mask lifetime. In order to protect the mask from the debris added during lithography process, the usage of the pellicle is essential. The pellicle is a membrane covered on the reticle. It prevents the adhesion of debris on the mask.

To realize the usage of the pellicle, we should resolve some problems such as mechanical weakness, thermal damage and image error. For a few years, several studies reported on EUVL pellicle. The pellicle structure which is first suggested is thin film with mesh support. However it causes the serious image disturbance due to thick mesh structure. Last year, the new structure of multi-stack pellicle was suggested to solve the image error caused by mesh structure. The multi-stacked type pellicle has a structure which is stacked with many extra-thin layers. However we still worried about the thermal problem due to high absorptive characteristic of EUV light. Furthermore it is necessary to find the acceptable defect size that would cause the image error. The effect of the defect on the pellicle can differ with defect size, feature conditions of the pellicle and so on. In order to realize the EUV pellicle, we should know the boundary of the acceptable defect size in terms of image error.

In this study we will report the thermal behaviors with various feature conditions of the pellicle such as material and structure. We tried to find the suitable conditions of the pellicle to obtain the small temperature rise, fast cooling speed and low image error. One of the results for EUVL patterning of 22 nm half pitch is that the intensity variation is small for smaller defects less than approximately 20 ?m (Fig. 1). However, the intensity and contrast are greatly decreased with the increasing the defect size.

9048-82, Session PTue

Conversion efficiencies from laser-produced Kr, Mo, Gd, and Tb plasmas at 6.xnm

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Progress in the field of extreme-ultraviolet (EUV) lithography based on 13.5 nm wavelength normal-incidence Mo/Si multilayer mirror technology is advancing with the development of laser-based and discharge-based tin plasma sources. It is expected to be introduced into high-volume semiconductor chip production in the next few years. Shorter wavelengths permit higher imaging resolution at lower numerical apertures (ref 1). So in seeking pathways towards still finer feature sizes, interest is rising in the possibility of fabricating high reflective EUV mirrors based in LaN and B or BC. Theoretical reflection efficiencies ~ 80% have been postulated for these mirrors in the 6.6 nm region. The Yulin group (ref 1) estimates the highest efficiencies occurring in bands at 6.635±0.018 nm or 6.675±0.015 nm, depending on whether LaN/B4C or LaN/B multilayer mirrors are used.

In this presentation, we examine the emission spectra of laser plasma sources that would be efficient in this region. In particular, the elements near molybdenum (Mo) and gadolinium (Gd) emit as intense unresolved transition arrays around 6.x nm. A detailed multilevel non-local thermodynamic (LTE) atomic model is developed (ref 2) and verified by available experimental data to investigate emissivity and absorption properties of highly ionized Kr, Mo, Gd, and Tb plasmas. Experimental spectra detected by solid state laser are presented together with analysis based on calculations using the relativistic Flexible Atomic Code. We will present the optimum regions for conversion efficiency of mass-limited targets against laser parameters including wavelength, pulse width, and shape by means of hydrodynamic simulation coupled to a developed population kinetics codes. The in-band powers from mass-limited Kr, Mo, Gd, and Tb targets predicted based on the current mirrors and available solid state/CO2 lasers.

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9048-83, Session PTue

Evaluations of negative-tone development resist and process for EUV lithography

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EUV lithography has significantly progressed through effective research and development. This emphasizes the potential of EUV as the leading next technology to realize the semiconductor device manufacturing promised by Moore's Law. To expand the capability of EUV lithography application, new process techniques were proposed such as the combinations of EUV lithography and directed self-assembly [1] and negative tone development (NTD) process [2], etc. NTD process was proposed for its advantage in trench and contact hole (CH) patterning applications. This was because, with bright field NTD process, a higher optical contrast can be achieved compared to dark field positive tone development (PTD) process. In addition, NTD process has the possibility to achieve smooth line width roughness (LWR) [3]. To enhance the NTD process applications for EUV lithography, further experimental investigations are necessary.

NTD resist and process have been and continues to be evaluated at EIDEC using the EUV small field exposure tool (SFET) with a numerical aperture of 0.3 [4]. The utilized organic developer solution is normal butyl acetate. In the previous work, 25 nm line and space (L/S) resolution, 6.0 nm LWR and 27.0 mJ/cm2 of sensitivity was obtained at annular illumination condition [3]. In this paper, several improved resists for NTD process were investigated focused on the reactivity of photo acid generator and protecting-group of polymer. As a result, 23 nm L/S resolution, 6.4 nm LWR and 15.4 mJ/cm2 of sensitivity was achieved. Additionally, ultimate resolution study is ongoing using x-dipole illumination condition. At present, 17nm L/S ultimate resolution has been achieved (fig. 1).

Under-layer materials are also evaluated. For the under-layers, adhesion enhancing is basically required to prevent pattern collapse. In the previous work, NTD-compatible under-layers of organic type were reported that contain hydrophilic polar units or exhibit high film density [3]. Based on these perceptions, inorganic type under-layers (silicon hard mask) are being studied for NTD process.

CH patterning evaluations with NTD process are currently being done using pillar mask. As a result, 10 mJ/cm2 sensitivity was obtained at 38 nm CH with no-bias mask. The resulting sensitivity of NTD process is significantly fast compared to typical PTD process performance (20mJ/cm2 or over), as expected.

Additionally, process investigations are also important for NTD process using EUV lithography. The effects of high optical flare should be considered more carefully at EUV lithography in comparison to previous lithographic techniques. Therefore, development process and rinse process well-matched for EUV lithography are believed different from those of the previous optical lithography. The effects of process assist will also be discussed at the conference.

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9048-84, Session PTue

Aerial image of mesh supported extreme ultraviolet pellicle

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The extreme-ultraviolet (EUV) lithography is about to be realized in mass production. It is regarded as the next generation lithography technology for achieving 16 nm node and beyond. However, there are still many obstacles need to be overcome. One of the most important issues is defect control of the EUV mask. Maintaining a defect-free mask is very important because defect can lead to pattern distortion.

The EUV pellicle should be very thin because it has high absorption ratio with 13.5 nm wavelength. The thin film consists of an inorganic material such as silicon and has a very small thickness of 50 nm and below to pass through enough EUV light. However, this very thin film would be deflected by gravity. This is the reason why the thin EUV membrane needs mesh support.

The hexagonal mesh shape was commonly used since it has a larger open area and higher stability compared to other structures. However there are some problems of using the mesh type support for the EUV pellicle. One of the main problems is the illumination non-uniformity at the patterned mask caused by shadow of hexagonal mesh support structure. The EUV light is diffracted by the support structure and make an interference image at the mask. And, the mask pattern image will be distorted by the image of mesh support structure.

Fiqure1 shows the aerial image of 22 nm 1:1 line and space pattern in 4X EUV system. It seems to be a serious problem, but it is not pessimistic because the problem is only related to the support structure. The image can be sufficiently blurred if we find an optimized structure that does not make a noticeable image distortion. The support structure image at the mask is varied with line width, size of open area and support height of the mesh support.

The height of support structure is about ~ 10 μm, therefore the EUV light reached to support are absorbed mostly. Thus, to reduce the transmittance loss, support structure must have small line width and large open area. Even though the shadow of mesh support structure is blurred at the wafer, the aerial image can be changed because absorbed EUV light reduces the intensity at the wafer. The decreased intensity at the wafer can have an influence on a pattern shape. It is more important to study aerial image because the target pattern size is very small in EUV lithography.

We tried to find the optimized shape of mesh support by studying the aerial image at the wafer for various pitch size, line width, support height and stand-off distance. We also studied the normalized image log slope (NILS) and Bossung-curve to estimate the effect of mesh support structure to patterning.

9048-85, Session PTue

Super-flat wafer chucks: from simulation and testing to a complete 300mm wafer chuck with low wafer deformation between pins

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Berliner Glas is a family owned, mid-sized company, located in Berlin, Germany. Our company supports the Semiconductor industry with innovative chucks for sophisticated manufacturing processes. Berliner Glas is specialized in high-performance vacuum and electrostatic wafer chucks. These chucks provide solutions to enable and optimize costumer needs with extremely flat micro – structured and wear resistant chucking surfaces, single or both sided chucking, integrated cooling and heating capability nearly zero or matched thermal expansion materials as glasses, ceramics and glass – ceramics, respectively.

Due to manufactures' needs for smaller overlay values, we pursue the production of an ideally flat wafer chuck. Such a wafer chuck will have a global flatness down to 100 nm across a surface of 300 mm in diameter and a local angle of 2 μrad. The local flatness across a die is within a few nanometers.

Key parameters in influencing the wafer table's flatness are thermal performance and thermal management, roughness of the surface, choice of materials and last but not least the design of the contact area between the wafer and the wafer chuck. In this presentation we would like to focus on the last parameter. Usually the contact area is decreased

as much as possible to avoid sticking effects and deformation of the wafer. This is realized by means of a pin structure. These pin or ring structures can reduce the contact area by a factor of 100. Besides the already mentioned reduction of sticking forces this causes also less particle sensitivity. The pin size can be manufactured down to 50 µm and a height down to 1 µm. But moving pins further apart and making them smaller as well adds new challenges to adjust the chuck's flatness. In this presentation we would like to address several methods of designing and evaluating such a pin structure.

This involves not only the capability to simulate the ideal pattern of pins on the chuck's surface, for which we will present 2D and 3D simulation results. We also would like to share first results of our functional models. Finally, our measurement capability has to be ensured, which implies the improvement and the further development of the existing interferometric flatness qualification system (Fizeau equipment).

9048-86, Session PTue

Designing extreme-ultraviolet lithographic objective for 11nm node

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Projection objective is a key component of an EUV lithography tool. To achieve 11nm resolution, a higher NA of objective around 0.45 is required. The increasing of NA makes a six-mirror design without obscuration inadequate to correct aberration. Under such a high NA, an eight-mirror design without obscuration could achieve required imaging performance. Nevertheless, the transmission would reduce to 40% of a six-mirror system and the integration and maintenance would be more difficulty. The design with central obscuration reduces the difference of angles on the last folding mirror, which enables a six-mirror system sufficient for the design correction[1,2]. However, fewer design method for EUV lithographic objective system with central obscuration has been proposed in the past.

We have developed a grouping design method with paraxial analysis, and the multi-mirror system without obscuration could be acquired with this method[3,4]. In this paper, we extended grouping design method to the design of objective system with central obscuration. Moreover, real ray analysis is used instead of paraxial analysis, which avoids the discrepancy of ray path induced by paraxial approximation. The whole system is divided into three mirror groups and each group is designed with different design constraints. First of all, initial parameters of object-side group are determined according to non-obscuration constraint. To control the size of pupil obscuration, the radio of obscuration on the last folding mirror (M5) and exit mirror (M6) are taken as design constraint of image-side group. Then, the initial parameters of image-side group are determined by obscuration-radio constraint. Once the parameters of object-side and image-side groups are determined, all the parameters of middle group can be calculated with the conjugation constraint based on real ray tracing equations and Petzval equation. Using real ray tracing analysis, the pupils of three mirror groups could match exactly. Thus, the three mirror groups can be directly connected into a feasible objective system at last.

A six-mirror objective system with a higher NA of 0.5 and a central obscuration was designed with this method. The x8 reduction design has a composite RMS wavefront error 0.029λ (λ=13.5 nm) across a 13mmx1mm ring field at wafer. Such a reduction enables the chief ray angle at mask keep on 6 degree. The size of obscuration is smaller than 30% radius of the pupil and distortion is corrected to better than 0.6 nm. The result shows that grouping design method provides an effective approach to obtain objective system with a central obscuration. Design of this six-mirror objective provides a potential solution for 11 nm node of EUV lithography.

9048-87, Session PTue

EUV resist simulation based on process parameters of pattern formation reaction

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Extreme ultraviolet (EUV) lithography which extends photolithography to extreme shorter wave length (13.5nm) is capable of achieving sub-20 nm half pitch resolution by single exposure. Therefore, EUV lithography is the leading candidate to succeed 193 nm immersion lithography. However, the RLS (Resolution, Line Width Roughness (LWR) and Sensitivity) trade-off is still a significant issue for EUV resists. On the subject of sensitivity in particular, there is a large gap between the current status and requirement. The sensitivity requirement at the 16 nm node is less than 10 mJ cm-2. However, at present, sensitivity of 20 to 30 mJ cm-2 or more is necessary to resolve 16 nm line-and-space patterns.

Even with these issues, the development of resist materials has progressed steadily. EUV resist materials are developed based on the properties such as glass-transition temperature, acid diffusion, thermal activation energy of de-protection and etc. However, these parameters are obtained by model examinations which are not the actual parameters on pattern formation processes. In the development of EUV resist, it is important to accurately understand the properties of resist materials. Thus, it is useful to simulate pattern formation reaction for obtaining these actual parameters.

We have simulated the process parameter of pattern formation reaction to include during-the-exposure and post exposure bake (PEB) process using an originally developed simulator. The resist used were EIDEC standard resist 1 (ESR1) and model resists based on the ESR1 at various quencher concentration. From these simulation results, the relationship between process parameters of pattern formation reaction and quencher concentration have been made clear.

In this work, we will simulate the ideal process parameters of EUV resist for breaking the RLS trade-off. In this simulation, process parameters are calculated from lithographic results (sensitivity, LWR and CD) based on actual SEM images. Through this methodology, ideal process parameters in obtaining the required lithographic target of EUV resist can then be obtained. However, these obtained ideal process parameters include various factors such as acid diffusion length, thermal activation energy of de-protection and etc. Thus, further analyses of these process parameters with Monte Carlo method and etc are still necessary for designing realistic resist materials. From these analysis results, we will clarify the relationship between these ideal process parameters and the above mentioned factors. Moreover, design of new EUV resist materials will be discussed from the viewpoint of process parameters of pattern formation reaction.

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9048-88, Session PTue

OBPL for the best solution to resist outgassing and out-of-band issues in EUVL toward 1Xnm hp

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EUV lithography (EUVL) is the most promising candidate of next generation technology for hp20nm node device manufacturing and beyond, however there are many critical issues to solve in the light source, tools, mask and photo resist. Regarding the development of a photo resist, it is necessary for high volume manufacturing (HVM) to improve LWR, resolution limit and sensitivity.

Additionally, concerning about deterioration of a patterning performance

by Out-of-Band (OoB) light existing in the EUV light, and contamination problem of exposure tool due to the resist outgassing are the key issues which have to be resolved toward HVM by EUVL. Especially, the outgassing problem can become a significant issue for fine patterning under high dose exposure condition.

This paper proposes the novel solution for these critical issues with the application of a top coat material which is named OBPL (Outgassing & out-of-Band Protection Layer) on resist. The key characteristics of OBPL material are to have a role in protection against the OoB adverse effect to keep up the resist performance, to suppress the outgassing from photo resist as a barrier layer and to enhance the lithographic performance such as photo resist profile and process window.

In designing the OBPL material, the optical property needs having not only the high absorbance of DUV light in OoB range but also high transmittance for 13.5nm wavelength to prevent the sensitivity loss. Furthermore, it is found that the polymer backbone affects the outgassing barrier capability in previous evaluation. Based on these investigations, a state-of-the-art OBPL achieves quite a positive lithographic result with sufficient OoB absorption and outgassing suppression. Moreover, this material has applicability to all types of photo resist including NTI process.

This paper describes the result of the feasibility study for OBPL and the lithography performance with EUV full field scanner.

9048-89, Session PTue

Temporal and spatial dynamic of a laser produced plasma through a multiple Langmuir probe detector

Nadia Gambino, Markus Brandstätter, Bob Rollinger, Reza S. Abhari, ETH Zürich (Switzerland)

In this work, a tin droplet LPP has been characterized in terms of electron and ion dynamic. The experiments have been carried out with an in-house developed motorized and multiple Langmuir Probe array detector. Up to seven Langmuir Probes were simultaneously placed at different angles with respect to the plasma expansion direction and at different distances from the plasma ignition point. These types of measurements are very limited on droplet targets. The plasma was generated by focusing a Nd-YAG laser operating at 1.6 kW of power with a wavelength of 1064 nm and a pulse duration of 24 ns on tin droplet target. The collected data were then analyzed in order to determine the temporal and the angular dynamic of the plasma particles. Using the Langmuir theory, the so called I-V curves were reconstructed. The measurements and the analysis of the I-V curves permitted to obtain spatially 3D mappings of the plasma electron density and electron temperature and the plasma potential at different expansion times. The experimental results were also compared to numerical simulations carried out with the LEC multi-scale computational tool. The code, based on a combination of a Particle-In-Cell (PIC) and Direct Simulation Monte Carlo (DSMC) method, is able to model the physical processes governing the formation and expansion of a laser plasma.

9048-90, Session PTue

EUV optical elements with enhanced spectral selectivity for IR radiation

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We report on the development of multilayer based solutions to enhance the spectral purity of EUV light generated by plasma-based sources. These multilayer systems reflect EUV radiation and simultaneously suppress infrared (IR) light, e.g. scattered CO2 laser radiation of the laser-produced plasma. Two possible solutions are discussed: 1) the planar mirrors combining EUV-reflective properties of multilayer Bragg reflectors together with IR antireflection based on the effect of destructive interference; 2) hybrid multilayer gratings combining EUV reflection with spectral-selective suppression of the specular IR reflectance due to the grating phase-shift resonance. Review of experimental results is given for 13.5 nm optics and 6.x nm optics relevant for EUV lithography and beyond.

9048-91, Session PTue

Clean and stable LPP light source for HVM inspection applications

Bob Rollinger, Nadia Gambino, Andrea Z. Giovannini, Luna S Bozinova, Flori Alickaj, Konrad Hertig, Reza S. Abhari, ETH Zürich (Switzerland)

The manufacturing technology of the next generation semiconductor devices is extreme ultraviolet lithography (EUVL). The 13.5nm radiation (2% bandwidth) can be generated from a Laser-Produced Plasma (LPP). The irradiation of tin droplets by a high power (kW) laser yields a plasma, which is highly emissive in this wavelength window. LPP EUV sources are used for high-volume manufacturing in EUV steppers, as well as for actinic mask, wafer and pattern inspection and metrology.

At the Applied Laser Plasma Science (ALPS) laboratory at the LEC, ETH Zurich we have been developing tin droplet-based laser-produced plasma sources with application in EUV lithography since beginning of 2007. The laboratory comprises three dedicated facilities, which include two LPP sources and one droplet dispenser development facility. The latest LPP source (ALPS II), which is operational since February 2013, is shown in Fig. 1. This new source is built from the significant experience from the initial (ALPS I) source while improving usability, uptime and the overall system performance. The extensive experimental and computational research, which has been conducted with the support of ALPS I, has been employed to improve the system performance of our latest source. ALPS II is equipped with a large capacity droplet dispenser and a high power (kW), high repetition rate Nd:YAG laser. This main source is used as an engineering test stand, where long-term effects (> 8 hours) of source operation are studied. The system can accommodate (high and low power) EUV collectors, which are typically protected by an inertial, gas-based debris mitigation system. The system integrates an extensive measurement system, which includes EUV monitors, soft X-ray plasma imaging and Faraday cups. As a result, the emission and debris characteristics of individual EUV pulses are monitored and logged during operation. In addition, Langmuir probes are used to characterize the plasma. Individual droplet tracking in time and space, which is coupled to a droplet positioning and triggering system increases the pulse-to-pulse EUV emission stability of the source. Recent performance results of long-term operation and future directions will be presented. The new source should address the requirements of high volume manufacturing for different inspection and metrology applications found in EUV lithography. Adlyte is in the process of commercializing the new light source.

9048-92, Session PTue

Optimized tin droplets for LPP EUV sources

Luna S. Bozinova, Bob Rollinger, Reza S. Abhari, ETH Zürich (Switzerland)

The next generation photolithography requires radiation in the Extreme Ultraviolet (EUV) wavelength region. EUV sources generate radiation at 13.5nm (2% bandwidth). The droplet-based Laser-Produced Plasma (LPP) EUV source is the most promising candidate to become the source for high-volume manufacturing in EUV steppers, as well as for actinic mask inspection and metrology. At the Laboratory for Energy Conversion (LEC), ETH Zurich a tin droplet-based EUV light source has been developed. The tin fuel is delivered to the plasma site in the form of micrometer-sized droplets. The tin droplets are irradiated with a high power Nd:YAG laser operating at frequencies up to 20 kHz with 1.6 kW of power.

During source operation, the droplet target train can be affected by the EUV emitting plasma. The stability of the subsequent tin droplet in a droplet train can be influenced by the plasma generated from the previous droplet. A maximum drop-to-drop spacing is necessary in order to avoid plasma-induced instabilities (along droplet train). The momentum exchange between the expanding plasma and the subsequent droplet can lead to droplet fragmentation or deviations from the trajectory. As a consequence, the initial conditions of the droplet irradiation are not constant. These potential instabilities at the plasma site directly translate into the pulse-to-pulse stability of the EUV source.

On the other hand the frequency of droplet generation should also match the repetition rate of the high power Nd:YAG laser, such that the pulse energy leads to an optimum conversion efficiency, i.e. the ratio between EUV and laser energy. The temporal stability of the droplet passage at the irradiation site is of paramount importance for the laser-droplet pulse synchronization, hence the source emission stability.

A next generation droplet generator has been developed in order to yield the required frequency operating range and droplet spacing. The performance of the LEC droplet generation system is experimentally and numerically assessed. A parametric study of the impact of the droplet spacing and the temporal droplet stability on source performance is presented in this work. The dispenser is then employed in the prototype source at the previously determined optimum conditions. The resulting benefits for source operation, with a focus on source cleanliness and emission stability, are detailed.

9048-93, Session PTue

Optimization of image-based aberration metrology for EUV lithography

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In EUV lithography, each optical reflection reduces the full system throughput and presents an additional source of aberration. Other influences to aberration also exist from the source to the mask and to the wafer plane. These aberrations can affect CD, depth of focus, and pattern overlay, therefore, characterization and mitigation are critical. Interferometric methods are the de facto standard aberration metrology technique of the optics industry. These methods have the potential of sub-nanometer accuracy but prove difficult to implement in-situ in a lithography process due to their sensitivity to environmental conditions. This becomes increasingly important as EUV lithography is likely more sensitive to drift from thermal and degradation effects than optical counterparts. We have developed an automated approach to photoresist image-based aberration metrology. The approach uses binary or phase mask targets and iterative simulation based solutions for the aberrated pupil. In general, smaller features are more sensitive to aberrations than larger features. A partially coherent source both introduces pupil averaging, and allows for the diffraction information of smaller features to be collected by the condenser system. There is a trade-off between target sensitivity and partial coherence. Therefore, metrology targets using this technique must be optimized for maximum sensitivity with each illumination system. This study examines aberration metrology target optimization and both low and high order aberration interrogation. The implementation of a previously developed algorithm for image-based aberration metrology is used to support this work [1]. In addition to target optimization, experimental data described by third order aberrations is presented. The effects of neglecting high order aberration, as well as several methodologies for high-order aberration interrogation, were examined as well.

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9048-94, Session PTue

Study of effects of CRAO for optical systems into the EUV

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As EUV (Extreme Ultra-Violet) attempts to outperform other lithographical methods to the sub-22nm node, the demand for a larger NA dominates the drive for scaling. Due to the reflective optics in EUV systems, an increase in NA strains the capabilities of the system; the incoming illumination light collides with the mask-reflected light. This necessitates an increase in the chief ray angle at the objective (CRAO). As this angle increases, the imbalance in diffraction orders worsens, leading to telecentricity errors at the mask. The telecentricity errors manifest as non-linear shifts in magnification and image translation through focus. Additionally, the reflectivity of the multilayer is a function of CRAO, and decreases rapidly at these increased angles. This study investigates mitigation of the telecentricity error through novel mask feature and multilayer designs. A sidewall angles are introduced in the mask features to compensate for the CRAO shadowing.

9048-95, Session PTue

Simulation and experimental study of EUV lithography and low-energy electron diffusion through photoresists

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Understanding the mechanisms behind secondary electron generation in extreme ultraviolet (EUV) lithography plays a vital role in advancing current imaging technologies. Through utilizing LESiS, a Monte Carlo-based modeling program designed and written to simulate photon and electron interactions based on fundamental atomic interactions, a theoretical secondary electron yield can be obtained. Further comparison of this secondary electron yield to experimental photoacid generation (PAG) has been done to showcase discrepancies in accepted PAG mechanisms. One of the discrepancies is the lower kinetic energy limit with which secondary electrons can expose a resist.

To study this problem, a series of current vs. resist type and thickness simulations were compared against a tri-layer study of resist on gold on silicon substrate. Preliminary experimental results show that a higher number of electrons reach ground than expected from simulation, implying extensive sub-ionization energy electron diffusion may occur. Details of the simulation and experimental results will be discussed.

9048-96, Session PTue

Modeling of multilayer mirror optics degradation for advanced nanolithography

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Photon sources for extreme ultraviolet lithography (EUVL) are based on laser produced plasma (LPP) devices with various tin targets configurations. Several criteria have being considered for the optimization of LPP systems including efficient EUV output and collection, minimized debris production and mitigation, and optical components lifetime. The multi-layer mirror (MLM) optical system for collecting EUV photons is one of critical importance in optimization and design of future EUVL systems. Ionic and atomic debris produced during laser interaction with target and developed plasma source can significantly decrease reflectivity of mirrors and further damage mirror surfaces. Heating of mirror surfaces by EUV

and out-of-band radiation from plasma can enhance diffusion processes resulting in layers intermixing that will further affect and degrade reflectivity properties.

We upgraded and enhanced our three-dimensional ITMC-DYN Monte Carlo package for the simulation of ions/target interactions with dynamic changing of target composition to analyze effect of energetic ions on mirror collection system. We implemented models for thermal diffusion and studied the dependence of MLM materials mixing on temperature and integrated effect of debris and thermal processes on mirror surface degradation. Analysis was done for MLM systems designed for 13.5 nm wavelength as well as for mirrors are being developed for beyond extreme ultraviolet (BEUV), i.e., at 6.7 nm wavelength using various materials composition including LaN/B and LaN?B4C with optimized layers thicknesses.

9048-97, Session PTue

Analysis of phase defect effect on contact hole pattern using a programmed phase defect in EUVL mask

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Phase defect embedded in EUV mask blank is one of the great concerns to achieve practical defect-free EUVL mask. As well as a development of multilayered mask blank inspection technique, understanding the impact of phase defects on the size variation of printed pattern on the wafer is also important to clarify the critical phase defect and to define the specification of phase defect inspection tool. In case of line pattern, phase defect effect was analyzed previously by using programmed phase defect mask.1)

In this study, we investigated the phase defect printability in contact hole pattern by printing the patterns on a wafer and compared the experimental results to those by computer simulation. A test mask prepared for this experiment contains programmed phase defects with width of 50 ~ 92 nm. The defects are so arrayed that the pitch differs from that of the absorber contact hole. Mask pattern was printed using an exposure tool NXE:3100. Exposure optics comprised a numerical aperture (NA) of 0.25 and 4X reduction. To evaluate the contact hole pattern affected by the phase defects, conventional illumination was employed. Incident angle of mask illumination chief ray was 6 degrees.

Printed contact hole patterns on wafer with their half-pitches of 32 nm were evaluated and the phase defect impact was examined as the hole CD variation measured by SEM. Since the phase defects were located at several positions with respect to the absorber contact hole patterns, the location of the phase defect was defined as the distance from the center of hole (Fig. 1) and the phase defect impact was evaluated as a function of the location. Example of the result is shown in Fig. 2. Although there is a quantitative distinction between simulation results and experimental results, clear relative location dependence could be verified and the effectiveness of the phase defect mitigation by covering the defect with absorber patterns was experimentally confirmed.

In this presentation, experimental results of phase defect effect on contact hole pattern depending on defect size and defect location will be shown. This work is supported by New Energy and Industrial Technology Development Organization (NEDO).

9048-98, Session PTue

The study of EUV resist material to prevent out of band (OOB) effects

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We developed blend type photo acid generator for EUV resist,, which is containing the variation of cation and anion to control the absorption of DUV. Based on this concept, our EUV resist is insensitive or need more energy on DUV radiation while the sensitivity on EUV radiation is keeping similarity to that of using general PAG.

Consequently, we tried to develop EUV resist, which is insensitive for OOB by decreasing DUV absorption. And we considered the variation of PAG functionality on PAG blend type resist. So, in this study we are going to suggest the method to solve above problems and discuss the data related to development.

9048-99, Session PTue

193nm Inspection of Extreme-Ultraviolet Mask Absorber Defect

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The defect free extreme-ultraviolet (EUV) mask manufacturing is one of the most important role in EUV lithography. To make clear pattern on the wafer, we need to control the defect on the EUV mask. Proper inspection of EUV mask defect is necessary to control the defects. The lack of the defect information such as the size and the height will cause the unexpected pattern errors on the wafer. However, the EUV actinic inspection tool is currently not ready for inspecting the EUV mask defect and it might not be available for the beginning of EUV mass production. Thus, there is a need to use a 193 nm wavelength inspection tool which is currently available.

ITRS roadmap indicates that the mask absorber defect size is 18 nm for 22 nm half pitch. But it is assumed that the defect height is the same as that of the absorber. The height as well as the size of the absorber defect would not be the same and would make different reflectance, and as a result, the effect to the patterning would be different.

Figure 1 (Ru defect) and Fig. 2 (TaN defect) show the effects of absorber defects. Blue triangle dots indicate that 25 nm size defects would make patterning error and the other sky-blue dots show that 193 nm inspection would give about the same result for Ru defect. As for TaN absorber defect, the same 25 nm size defects would make patterning error, while 193 nm inspection could only detect 30 nm defects. There is a difference between the 193 nm wavelength inspection results and the influenced EUV patterning results. We tried to minimize this kind of discrepancy between the 193 nm inspection and the patterning or actinic inspection result.

9048-100, Session PTue

Preparation and evaluation of the EUV photoresists based on molecular glasses

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Several kinds of molecular glass compounds were synthesized. These compounds can be applied as positive or negative photoresists by mixing with other components such as photoacid generators, photo-crosslinkers and other additives. The photoresists have suitable thermal properties and the amorphous films on silicon substrate can be obtained by spin-

coating of the photoresists. The extreme ultraviolet (EUV) lithography patterns were evaluated by using soft X-ray interference lithography beamline (BL08U1B) on Shanghai Synchrotron Radiation Facility (SSRF).

9048-101, Session PTue

The synthesis and evaluation of molecular glasses as EUV photoresists

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Several molecular glass compounds were synthesized. These compounds can be used as positive and negative photoresists combined with photoacid generators, coupling agents, photoresist solvents and some other additives. All the compounds showed suitable thermal properties and smooth film on silicon substrate were obtained be spin-coating. The compounds could be used for 248nm, 193nm, electron beam and extreme ultraviolet (EUV) photolithography. The EUV lithography patterns and out-gassing of the materials were evaluated using soft X-ray interference photolithography beamline on Shanghai Synchrotron Radiation Facility (SSRF).

9048-102, Session PTue

Aerial image deformation caused by various defects of EUV pellicle

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The Extreme-Ultraviolet Lithography (EUVL) is the one of next generation lithography due to technological limitations in optical lithography. To protect the mask from defects, the EUV pellicle was suggested in several years ago and it has been studied. In the EUVL process, defects on the pellicle would not give any influence on image formation at the wafer owing to out-of-focus. However, some defects can lead to intensity change at the wafer if the size is very large.

The pellicle protects mask from the defect. However, it causes some issues if the defect size grow. Many defects can change the intensity at the wafer because it interrupt an optical path in exposure process. Further the pellicle deflection will occur due to many defects, it will be the main cause of pellicle damage as well. To reduce these issues, we investigated the change of aerial image caused by various defects on and in the pellicle.

We used a computer simulation tool, “Fastlitho”, and obtained the changes of aerial images by varying the defect sizes. Figure 1 shows the aerial image variation with 50 nm silicon membrane, the stand-off distance of 2.5 mm. We used a circular illumination (0.5 ?) and applied to 22 nm haf-pitch pattern. The defect size is varied from 0 to 200 ?m. As expected, the intensity decreases gradually as the defect size goes larger.

We also changed the parameters of EUV pellicle such as the pellicle thickness, pellicle composition material, stand-off distance and illumination conditions in order to find the optimum EUV pellicle for better defect control.

9048-103, Session PTue

Correlation study on resist outgassing between EUV and e-beam irradiation

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In extreme ultraviolet (EUV) lithography, the resist screening for the outgassing risk is indispensable to save the exposure tool from the serious damage by contamination. It is resulted by the interaction between the evaporated or decomposed species from the irradiated resists and the surface of the irradiated mirror optics.

Though the detail of the contaminating mechanism is still unclear, the witness-sample (WS) method is recently accepted as the standard way to clarify pass/fail for resist outgassing [1]. The WS is the small plate which mimics the EUV mirror and it is placed in the vacuum chamber with a certain spatial arrangement from the resist coated wafer. Some of the tools for this purpose use EUV light to irradiate resists and WSs, on the other hand some use electron-beam (E-beam). The resist must pass the test by the qualified outgassing test tool, though EUV or E-beam does not a matter, before it is used in the EUV scanner. So it is necessary to check if the results by EUV exposed test and E-beam exposed test are comparable.

We have made it using EUV irradiation type test tool HERC [2, 3] and E-beam irradiation type test tool EUVOM-9000 [4]. As the contamination characteristic is thought to be material dependent, the variety of resist samples with different components was compared. For the PAG unit, which is thought to be the primal element of contamination when the chemical amplification resists are used, not only the combinations of the cation and anion in PAG blend types but also the PAG-bound types were investigated.

The comparison was made for the carbon thickness on the WSs measured by spectroscopic ellipsometer, Quadropole mass spectrum (QMS) analysis of the outgassing during the exposure, and atomic components analysis of contaminants layer on the WSs by XPS.

Through the set of QMS analysis for the resists with the different combinations of the components, we could separate the outgassing amount from PAG, protecting group and matrix polymer. It was confirmed that most of the QMS peaks are the same in EUV and E-beam. But in the sample without PAG, evidence showing that the protecting group decomposes by EUV exposure directly but not by E-beam exposure was found. On the other hand, in comparison with the contaminated film thickness with and without protecting group, it was indicated that the contribution of protecting group is negligible in both of EUV and E-beam. It means the root cause of the contamination is PAG in both cases. We will discuss these findings including the consideration of measurement conditions such as geometrical arrangement.

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9048-104, Session PTue

Predicting LER power spectral density caused by EUV mask roughness

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Replicated multilayer roughness in EUV masks causes focus dependent speckle which contributes to LER[1]. Previous work has shown how speckle contrast causes LER[2]. The model presented here extends that work to calculate the PSD of the LER from the PSD of the effective mask roughness for any illumination and defocus. It takes advantage of the roughness being small to quickly calculate these characteristics without the need to generate a set of random masks making it faster and providing more direct insights than alternative methods.

We previously presented a mathematical model that predicts the PSD of speckle directly from the PSD characteristic of the mask roughness for any illumination and defocus[3]. We have extended that model to

incorporate the effect of coherent interaction of diffracted orders from patterned lines over the rough mask blank. Using this model we are able to predict the PSD of the LER contributed by the mask roughness under different illumination conditions and roughness statistics. Figure 1 shows this PSD for coherent illumination and Figure 2 shows this PSD for quadrupole illumination. In both figures the dashed line is the average PSD extracted from conventional 2D simulations of 4 random masks. The solid line is the PSD predicted by the model for masks with the characteristics used to generate those masks.

This work performed in part at Lawrence Berkeley National Laboratory which is operated under the auspices of the Director, Office of Science, of the U.S. Department of Energy under Contract No. DE-AC02-05CH11231. This research was supported by collaboration with industry under the IMPACT+ program.

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9048-105, Session PTue

Bright EUV light source for metrology using pulsed power technology

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Actinic mask defect inspection and metrology require high-brightness EUV sources at moderate output power with enhanced stability. We report on compact EUV light source development, including an extensive computational modelling which provides the basic parameters required for high irradiance operating regime. The source is based on a fast pulsed plasma discharge created in a gas-filled capillary wall confined structure, ignited through a transient hollow cathode discharge mechanism. Nanosecond scale of the resistive discharge is provided by high voltage pulsed power technology with transmission line imbedded in the source structure. The fast discharge and the dielectric capillary wall confinement provide small size stably positioned emitting plasma source. Accelerated electrons in gas-filled capillary discharge with hollow cathode produce a narrow ionized channel and initiate the discharge. High discharge current density produces hot compact plasma intensively emitting EUV or soft X-ray light in required wavelength-band varying by gas admixtures. Computational and experimental study benchmarking with EUV source with xenon admixture is reported. The transmission line in the source is charged for few Joules of electric energy at 20-30kV voltage that provides up to 20kA current through the discharge lasting for 15ns. Pulsed plasma of 150nm diameter emits up to 5W/kHz of in-band EUV power in 2n srad. averaged at high frequency operation mode.

9048-107, Session PTue

Evaluation of EUV resist performance below 20nm CD using helium-ion lithography

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For the introduction of EUV lithography, development of high performance EUV resists is of key importance. This development involves studies into sensitivity, resolving power and pattern uniformity. We have used a sub-nanometer-sized 30 keV helium ion beam to expose chemically amplified (CAR) EUV resists.

There are remarkable similarities in the response of resists to He+ ions and EUV photons. Both primary particle beams traverse the resist and meanwhile interact with the target atoms. The low backscattering of the He+ ions results in ultra-low proximity effects, which is similar to EUV exposures. Absorption of an EUV photon creates a high-energy electron that relaxes by the excitation of Secondary Electrons (SEs). A collision of a 20-30 keV helium ion with a target atom directly releases low-energy SEs. Each ion scatters several times in the resist layer, thus enabling resist exposures at very low doses per CH. The energy spectra of SEs generated by EUV and He+ are remarkably alike. These SEs, in turn, activate the resist.

In this paper we show 30 keV He+ ions exposures of contact holes and lines with a CD of 8 – 30 nm at 20 nm half-pitch in a chemically amplified EUV resist. Two examples are given below in Figure 1. We will demonstrate the potential of using He+ ion lithography [1] in the study of EUV resists.

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9048-108, Session PTue

Non-catalytic amplification for improved LER in EUV resists

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As we approach the 10nm half-pitch, the problems with line edge roughness (LER) have become problematic. A main contributor to LER is acid diffusion in chemically amplified resists (CARs), which is exacerbated by the low photon count of EUV light. Improvement requires either a larger photo acid generator (PAG) loading or doses far outside the capabilities of the tools themselves. Our new approach to EUV resists finds amplification through self-immolating polymers. By using a dissolution-inhibiting polymer in Novolac that requires only one non-catalytic photolysis event to undergo a full depolymerization, we aim to achieve high sensitivity, high resolution and decreased LER. To achieve this amplification we have created two new polymers that act as dissolution inhibitors in Novolac and posses a low ceiling temperature (Tc). These polymers are either terminated with photosensitive end groups to generate a reactive species that cause the polymer to depropogate above its Tc or contain EUV sensitive monomers along the polymer backbone, which allows for a depolymerization event to occur anywhere in the polymer. Current research is directed towards monomer and polymer modification to give the greatest contrast in dissolution inhibition and to efficiently attach photo-labile end groups to the polymer chain. The ideal polymer must posses five key properties to be successful: 1) Be miscible with Novolac for our first generation strategy, 2) Contain Lewis acidic sites to block the phenolic groups of the Novolac resin, 3) Depropagate into neutral or Lewis basic monomers to allow dissolution, 4) Have a Tc above 0º and below 150º for tool and manufacturing compatibility, 5) Be sensitive to EUV exposure via an end-cap or intrinsically via the polymer backbone. We are currently concentrating on two polymers developed in our lab specifically for this purpose. The first is a polybenzilic ether with a Tc around 20 ºC and acceptable miscibility in Novolac. Current research is exploring monomer improvement for increased EUV sensitivity and increased dissolution contrast in Novlac. The second polymer is an aliphatic polyester, which decomposes into CO2 and toluene spontaneously upon exposure to UV light. Current work is aimed at increasing the polymers intrinsic sensitivity to EUV and preliminary imaging studies.

9048-109, Session PTue

TNO Reticle Handling Test Patform

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Particle free handling of EUV reticles is still an important issue in industry. For reaching economically acceptable yield levels, it is reported that PRP (Particles per Reticle Pass) levels should be better than 0.001 [PRP]. Until now this cleanliness level has never been reached. Simultaneously, the accepted defect sizes shrink to 13 nm in 2018. Since the number of particles increases with decreasing particle size, increasing the performance of handling equipment needs more and more effort to meet the required cleanliness.

In order to bring handling technology to a higher level, TNO initiated the Shared Research and Development Program “ACTON”. To boost the program TNO started building a reticle handler. This handler will serve as a demonstrator and development platform for the reticle handling technology for the EUV era.

The current TNO reticle handler focuses on the ambient side of reticle handling. As a design base line a modular concept with three uniform linked base frames was chosen. Each base frame can interface with two functional units at the sides. Depending on the required functionality the handling system can be expanded or reduced in size. In the first phase a dual pod load port, two exchange stations for opening inner pods and a flipping unit are integrated to demonstrate clean handling of reticles. A two sided gripper is designed for the robot to interface with inner pods on one side and bare reticles on the other side. The robot is placed on a linear track that connects the three different modules.

The reticle handler will be used for technology developments to reach higher cleanliness levels and support suppliers with the development of clean handling equipment. Cleanliness bottlenecks in the process flow can be pinpointed and each subunit can be optimized for particle cleanliness. New materials, shapes and handling strategies can be tested.

In the current design interface slots for up to four other subunits are available. Next year one slot will be provided by equipment for particle detection on flat substrates, the TNO RapidNano4. With the integration of the RN4, particles of 20 nm and larger can be detected. The integrated particle detection tool enables full automatic handling and measurement cycles for testing new insights on qualification protocols on particle cleanliness.

One of the slots will be prepared for interfacing with handling equipment in a vacuum environment.

Depending on the needs of Shared Research and Development Program the other slots will be extended with library functionality to test impact of storage conditions on reticle lifetime or interfacing with other measurement tools.

Finally, the TNO reticle handler will be available as a test platform that interfaces with other EUV reticle related tools built by customers. These tools can either be directly linked to the reticle handler or only used as a measurement platform on particle cleanliness.

9048-110, Session PTue

EUV blank mask inspection using 193nm inspector

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Blank mask defectivity is a major concern in EUV mask manufacturing. Soft defects, bumps and pits existing on the blank can introduce reflectivity and phase changes to the EUV light, resulting in printed defects on the wafer. Incoming EUV blank inspection in the mask shop is aimed to find all these defects on the blank and to characterize their type. Based on inspection result the proper mitigation technique can be performed, such as pattern-shift, ion deposition, etch/smoothing etc.

In this paper we present the Aera4TM blank mask inspection results, detecting phase defects and particles. The advantage of different illumination shaping usage for boosting detection sensitivity is demonstrated as well as the Aera4TM defect reporting accuracy with and without fiducial marks. Finally, the correlation between blank mask inspection results to the pattern mask inspection results and repeaters on wafer is made.

9048-111, Session PTue

Optimization of megasonic particle removal processes for EUV masks

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Megasonic processes are essential for removing nanoparticles from surfaces, especially in the case of EUV substrates, blanks and masks where sub 100 nm particles can form killer defects destroying masks and reducing yield. Although very efficient in particle removal, uncontrolled use of megasonic energy can result in pit formation and feature destruction which is equally detrimental for mask and blank yield. Megasonic processes are governed by the Rayleigh-Plesset equation given by

$$\ddot{R} \quad \frac{3}{2}\dot{R}^2 \quad \frac{2\sigma}{\rho R} \quad \frac{4\mu\dot{R}}{\rho R} \quad \frac{1}{\rho}\left[P_0 - \left(P_0 \quad \frac{2\sigma}{R_0}\right)\left(\frac{R_0}{R}\right)^{3\gamma} - P_A \sin\omega t\right] = 0.$$

[$P_A \sin \omega t$] is the term defining the acoustic pressure and frequency of the acoustic wave, σ, ρ and μ represents the surface tension, density and viscosity of the medium used and γ represents the polytropic index of the dissolved gas.

In the past SEMATECH has demonstrated how megasonic processes can be optimized for EUV substrate and blank cleaning by adjusting the megasonic power and frequency. In this paper we further optimize the process by carefully selecting the medium and dissolved gas, thus altering the other parameters in the Rayleigh-Plesset equation. We demonstrate pit free cleaning at ~ 35 nm and above and identify the most suitable chemical and gaseous combination for cleaning of EUV surfaces.

9048-112, Session PTue

Stochastic and systematic patterning failure mechanisms for contact-hole in EUV lithography

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Patterning uncertainty in EUV lithography arises from each lithographic component: the source, the photomask, the optical system, and the photoresist. All contribute to line roughness and contact disuniformity. In extreme cases, features variability can result in patterning failure as line-bridging or random missing contact holes.

Historically, redundant contact holes (or vias) were placed through the device layers to overcome the effects of a missing contact . Due to the aggressive CD shrink of feature size, the use of redundant contacts has been progressively decreased. For some types of devices, every contact of the billions found on the chip must be electrically active in order for the device to function . In such a scenario, lithographic printing failures may cause catastrophic loss of yield, considering that closed contacts can

hardly be corrected by smoothing techniques or etching.

In this paper, the minimum contact CD which prints without failure – the contact hole printability limit – is studied for 54 and 44nm pitch dense arrays. This approach is defined in an accompanying paper3, used to demonstrate the printability limits on a wider variety of layouts, including SRAM and Logic application. Exposures were performed using multiple JSR resists of similar contrast with the ASML NXE:3100 and NXE:3300 EUV tools . Contact hole printing failures are more often observed at small CD when each contact is defined by few absorbed photons. Increasing the sizing dose by adding quencher can mitigate shot noise effects (figure 1, left), but is an expensive technique to extend the printability limit. A faster acid diffusion rate can help reducing exposure dose but increases the minimum printable CD (figure 1, right). Alternatively, it is possible to increase the aerial image quality using tools with higher NA (figure 1, left, black edges dots), which can reduce both the minimum printable feature size and the sizing dose.

In this work we find that the same resist may show dramatically different printability limits depending upon sizing dose and illumination conditions. The printability limit cannot be considered as a resist property only, rather a combination of resist, shot noise effects and the aerial image quality. This analysis will be implemented to determine, through simulation-assisted experiments (figure 2) , the required exposure dose upon resist properties and aerial image to safely print sub-30nm contact holes.

9048-113, Session PTue

Laser-produced plasma light-source development for HVM

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This paper describes the development of a laser-produced-plasma (LPP) extreme-ultraviolet (EUV) source for advanced lithography applications in high volume manufacturing. EUV lithography is expected to succeed 193nm immersion double patterning technology for sub-20nm critical layer patterning. In this paper we discuss the most recent results from high power testing on our development systems, and describe the requirements and technical challenges related to successful implementation of these technologies. Subsystem performance will be shown including the CO2 drive laser, droplet generation, laser-to-droplet targeting control, intermediate-focus (IF) metrology, out-of-band (OOB) radiation measurements and system use and experience. In addition, a multitude of smaller lab-scale experimental systems have also been constructed and tested. This presentation reviews the experimental results obtained on systems with a focus on the topics most critical for an HVM source.

9048-114, Session PTue

Out-of-plane scatterometry for potential directional effects in EUV phase roughness

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In-plane (IP) scatterometry of EUV mask blank has recently shown a PSD behavior that is lower than that from AFM measurement on multilayer, implying that scatrometry is a more reliable means of characterizing the lithographic performance. As EUV mask blanks are made with polishing processes that potentially leave directional effects, we used out-of-plane (OOP) scatterometry measurements of multilayer coated mask blanks to look for orientation dependence in their electromagnetic performance. The goals here are to examine the strength of scattering out-of-plane, to look for asymmetrical effects, and to determine if in-plane measurements with a rotated mask are sufficient for characterizing the expected lithography performance.

Out-of-plane scatterometry data will be presented for several masks coated with ion beam deposition that resulted in several levels of final RMS roughness. The measurements were taken from the reflectometer at Advanced Light Source, Lawrence Berkeley National Laboratory. The geometrical measurement angles are defined and included. A typical comparison of Scatterometry with AFM is shown in Figure 1 where Scatterometry measured roughness appears to match the substrate roughness at low spatial frequencies and approach the multilayer roughness before it is limited by the angular bandwidth. Figure 2 shows the comparison of out-of-plane PSD (blue curve) with in-plane PSD (red curve) with offset in out-of-plane direction. Blue curve values are higher than red curve values by 83% in average from this initial data. Data for the set of masks with various programmed roughness levels will be presented and examined for small residual peaks at length scales for various blank polishing step treatments.

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9048-115, Session PTue

Limitations of resist-based characterization of mask-induced line-edge roughness

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It is well established that extreme ultraviolet (EUV) mask multilayer roughness can lead to wafer-plane line-edge roughness (LER) in lithography tools [1-5]. Assessing the severity of the problem with resist imaging, however, is extremely challenging due to elevated levels of resist LER obscuring the mask effects. Here we perform a model-based study to understand the resist LER performance needs required for such a measurement. A stochastic resist model is applied to line-space aerial images corrupted by mask induced LER. Using this technique we determine the resist LER requirements as a function of the mask roughness levels being determined. The results show that with current resist performance of on the order of 3-nm it would be difficult to observe less than 300-pm of mask multilayer roughness. On the other hand, the impact of sub-100-pm roughness is readily observed using an EUV microscope.

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9048-116, Session PTue

Clear sub-resolution assist features for EUV

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With the anticipated late insertion of EUV into mass manufacturing of integrated circuits, the k1 value for the critical level is expected to be between 0.44 and 0.54, much smaller than anticipated at the outset of the EUV programs. This means that the depth of focus for non-assisted isolated features may be of the order or smaller than what can be achieved for wafer flatness and scanner focus control. The depth of focus may have to be enhanced by sub-resolution assist features (SRAFs), as was done in KrF and ArF lithography before. The absorber thickness relative to wavelength, in addition to the reflective nature of the photo mask gives rise to strong EMF effects, while the large size of assist features relative to the wavelength can give rise undesirable SRAF printing. The non-telecentricity of the projection system on the reticle side causes different behavior for horizontal and vertical assist features, as well as potential through-slit variations. For ArF wavelength the SRAF is small compared to the wavelength in both lateral extent and also absorber thickness, and we expect a strongly attenuated transmitted intensity. For the case of non-normal incident radiation for EUV lithography, the wavelength is smaller than the lateral extent of the SRAF, but even smaller compared to the absorber thickness, which is of much concern because the absorber has to be traversed twice for reflective masks. In this paper, we discuss the issues affecting the insertion of SRAFs into the OPC correction flow. We will attempt to correlate our results to printed wafer results in an EUV projection system at 0.33 NA.

This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

9048-117, Session PTue

Ptychographic wavefront sensor for the optical testing of inspection and exposure tools

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As inspection tools and exposure tools continue to push toward higher resolutions, we continue to search for new methods of wavefront metrology to characterize and eliminate aberrations in the optical systems. High numerical apertures associated with next generation EUV optical systems create numerous complications with established interferometric techniques like Lateral Shearing Interferometry (LSI) or the Hartman sensor. Chief among these issues are systematic aberrations, alignment and calibration, and low photon flux.

Ptychography is an up-and-coming technique used by the coherent diffraction imaging (CDI) community, that has been successfully demonstrated at both visible and x-ray wavelengths. In ptychography, an unknown sample is illuminated by an unknown probe at multiples scanned locations, and the resulting diffraction patterns are captured on a CCD. The scan locations are chosen such that the footprint of the probe on the sample overlaps with adjacent footprints so that there is significant redundancy in the dataset. An iterative reconstruction simultaneously recovers the complex field amplitude of both the sample object and the probe.

For the most part, ptychography has been used as a technique for lens-less imaging, whereby the goal is to reconstruct the amplitude and phase of an unknown sample. However, solving for the probe effectively reconstructs the wavefront of the incident beam, and thus ptychography be used as a method for optical testing.

Figure 1 shows an experimental realization of ptychography in an EUV optical system. As shown in the figure, one of the key advantages of ptychography over other coherent techniques is that it can be coherently multiplexed. Light from each pinhole in the mask plane collects aberrations from the test optic and interferes in the observation plane. Thus, the “probe” is the interference between multiple sheared copies of the test wavefront. After this probe is reconstructed, it is back-propagated to the image plane, where each wave manifests as the point-spread function of the optic. In this plane, the waves are spatially separated and may be averaged to recover the test wavefront with a significantly increased signal to noise ratio.

Other attractive qualities about ptychography include its ability to operate with significant defocus – relaxing vibration and stage resolution requirements – and its simultaneous reconstruction of the object, which eases requirements on nanofabrication accuracy.

9048-118, Session PTue

AIS wavefront sensor: robust optical test of exposure tools using localized wavefront curvature

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As exposure tools continue to push the boundaries of resolution, it becomes increasingly difficult to characterize the aberrations in the system. Interferometric techniques based on reference waves such as phase-shifting point diffraction interferometry (PS/PDI) become difficult to realize due to the strict requirements on coherence and reference wave quality. Self-referencing tests such as lateral shearing interferometry (LSI) suffer from tight tolerances on grating and detector tilt.

As exposure tools like the SEMATECH Albany and Berkeley METs upgrade to 0.5 NA optics, the AIS wavefront sensor will provide robust alternative to interferomtric aberration metrology. Unlike LSI, AIS does not suffer from certain systematic errors that scale with NA, and since AIS uses a photodiode instead of a CCD, its integration can be simpler and more cost-efficient than other interferometer-based solutions.

A schematic of the AIS setup is shown in Figure 1. Light from an extended incoherent source is incident on a pupil wheel containing several swappable illumination masks that control the range of spatial frequencies entering the system. This light picks up some phase curvature caused by aberrations in the optic, which manifests as a small focus shift in the image plane.

The reticle contains three fields of 1:1 line-space grating patterns in three orientations: 0o, 60o, and 120o. The pitch of these gratings determines the diffracted order separation and controls the spatial extent of the pupil probe. In the image plane, a focus sensor measures the plane of best focus for each grating orientation at each pupil probe location. Localized wavefront curvature is computed from the measured focus shifts and fed into an algorithm that reconstructs the aberrations in the system

An EUV demonstration of AIS is currently being performed on the SEMATECH SHARP microscope at LBL in Berkeley. In lieu of a pupil wheel, the illumination is controlled via a 2-axis scanning mirror, and aberrations are intentionally added by tilting the zone plates from their nominal positions.

An optical prototype has also been constructed to simulate the AIS experiment and to study and design alignment strategies. In this prototype, the test optic is substituted with zone plate lenses with programmed aberrations spanning across the first 15 Zernike polynomials. Preliminary through-focus contrast curves show good agreement with the theory and are an important resource for setting stage specifications and design parameters.

9048-119, Session PTue

High-speed EUV using post processing and self-aligned double patterning as a speed enhancement technique

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EUV is an ongoing industry challenge to adopt due to its current throughput limitations. The approach to improve throughput has primarily been through a significant focus on source power which has been a continuing challenge for the industry. The subject of this paper is to review and investigate the application of SADP (Self aligned double patterning) as a speed enhancing technique for EUV processing. A process with the potential of running a 16 nm self-aligned final etched pattern in less than 10mj Exposure range is proposed. Many of the current challenges with shot noise and resolution change significantly when SADP is used in conjunction with EUV. In particular, the resolution challenge for a 16nm HP final pattern type image changes to 32nm as an initial pattern requirement for the patterned CD.

With this larger CD starting point, the burden of shot noise changes significantly and the ability for higher speed resist formulations to be used is enabled. Further resist candidates that may have not met the resolution requirements for EUV can also be evaluated. This implies a completely different operational set-point for EUV resist chemistry where the relaxation of both LER and CD together combined, give the resist formulation space a new target when EUV is used as a SADP tool. Post processing mitigation of LWR is needed to attain the performance of the final 16nm half pitch target pattern to align with the industry needs.

If the original process flow at an 85W projected source power would run in the 50WPH range, then the flow proposed here would run in the <120WPH range. Although it is a double patterning technology, the proposed process still only requires a single pass through the EUV tool, This speed benefit can be used to offset the added costs associated with the double patterning process. This flow can then be shown to be an enabling approach for many EUV applications.

9048-120, Session PTue

Development of a EUVL collector with infrared radiation suppression

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LPP sources for EUVL systems utilize CO2 lasers operating with a lambda of 10.6μm wavelength. As multilayer-coated reflective optics have a high reflectivity of this infrared radiation, a significant and detrimental amount is passed through an EUVL system. One method to remove the infrared radiation (IR) from the system is to utilize a binary diffraction grating. When this grating is applied directly to the surface of the primary collector optic of the source, the majority of the IR radiation is diverted outside the radius of the exit aperture of the intermediate focus (IF). This paper will report details on the performance of a full size (400mm diameter) demonstration collector utilizing IR rejection technology to produce over 125X suppression of IR radiation, equaling the performance of an IR filter. Additional details on supporting technology development of the IR rejection surface to enable a high-performance collector solution will also be reported, including the use of a glassy smoothing layer to enable a weighted average multilayer reflectance of 50.9% for unpolarized EUV radiation. These measurements were supported by the upgrade of the NIST reflectometer, which will also be discussed.

9048-121, Session PTue

Deconstructing contact hole CD printing variability in EUV lithography

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Lithographic CD printing variability can be easily captured with a CDU measurement, however delineating the most significant sources causing the variability is challenging. In EUV lithography, the resist, reticle, metrology methodology, and stochastics are examples of factors that influence printing variability. Determining the most significant sources of variability in contact hole and via patterning is particularly interesting because the variability can be measured as a function of two tethered dimensions. Contact hole variability has a direct impact on device performance while via variability affects metal area scaling and design. By studying sources of variability opportunities for improving device performance and scaling can be identified. In this paper, we will examine sources of contact patterning variability in EUV lithography comprehensively using various EUV exposure tools as well as simulation methods. We will present a benchmark of current state of the art materials and patterning methods with the goal of assessing contact hole printability at the limit of 0.33 NA EUV lithography.

9048-123, Session PTue

Fast rigorous model for mask spectrum simulation and analysis of mask shadowing effects in EUV lithography

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EUV lithography is the main candidate for the next generation lithography, especially for half pitch of 22nm and below. Because of off-axis illumination and mask topography, there is an orientation dependent pattern shift and bias, so an accurate analysis of mask topography effects is needed. Rigorous mask simulation methods like FDTD or Waveguide are usually limited by the runtime or memory requirements. For a better understanding and analysis of mask topography effects, accurate and fast methods have to be developed, which provide an analytical description of the important imaging effects.

A fast rigorous model is built for mask spectrum simulation in EUV lithography. The absorber and multilayer constituting the EUV mask are simulated separately in this model. The absorber model is a modified Kirchhoff thin mask model, where a pulse function is added to the mask pattern edge. The multilayer model is built by using an equivalent layer method to compute the multilayer reflectivity. The equivalent layer method provides a rigorous method to compute multilayer reflectivity using Fresnel Formulas. This fast rigorous model provides an analytical expression of diffraction spectrum of mask.

Base on this model, we propose a theoretical analysis of the mask shadowing effects. The expressions of phase and amplitude of mask spectrum are obtained. For oblique incident light, the resulting image

pattern center will have some shift compared with that at normal incidence. According to the Fourier transform theory, the shift in spatial domain corresponds to a linear variation in frequency domain, so an analytic expression for the best mask (object space) focus position is derived from the phase expression. With different directions of incident light, the image CDs are also different from the target CD. This is mainly result of the energy loss that mask diffraction amplitude varies with the changes of direction of incident light. We should correct the mask pattern size to compensate the energy loss for target image CD. So another analytic expression for the correct value of mask pattern size is derived from the amplitude expression.

Taking 22nm space patterns at 6° incidence angle as an example, with pattern pitches ranging from 50nm to 500nm, the simulation of this model is about 20 times faster than the waveguide method, and CD errors are below 0.15nm (0.7% CD) with little fluctuation. For 16nm space patterns, the CD errors are below 0.45nm (2.8% CD). When the mask focus is positioned on the equivalent plane of the multilayer, the pattern shift amount is reduced, and when the mask pattern size is corrected using the derived equation, the imaging CD bias is below 0.5nm.

9048-124, Session PTue

At wavelength observation of phase defects using focused lensless microscope

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For the phase defect observation, we have developed micro coherent EUV scatterometry microscope (micro-CSM) at NewSUBARU of a synchrotron radiation facility. The micro-CSM is lensless microscope with a focusing optics of Fresnel zoneplate. The illumination size was about 200 nm. The micro-CSM observed programmed phase defects with 30-nm width and 1-nm depth, which caused varied scattering distributions. It was shown that such small defect had varied phase distribution that would change the printability. As the result, characterization tool such as the micro-CSM system is essential for production of defect-free EUV mask. This work was supported by NEDO.

9048-125, Session PTue

Relation between the first 15 Zernike's of aberration on the aerial image to the printing performance

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Optical aberration correction of optical projection lithography tool has increasingly become more important with shrinking line width to meet the desired printing performance specifications. This presentation will focus on 0.3 and 0.5 numerical aperture (NA) extreme ultra-violet lithography (EUVL) exposure optics.

This is part of a larger program underway to develop an in-situ aberration measurement system to reduce aberrations within the EUV MET in Albany. This part of the program is aimed at understanding the relationship between the required accuracy of the aberration measurements and the desired resist printing performance.

Specifically, we will present the relationship between varying the amount and linear combination of the first 15 Zernike's of aberration on printing performance of lines and spaces as predicted by the aerial image distortions using rigorous finite difference time domain Maxwell solvers for mask plane and scalar propagation for rest of the domain.

9048-126, Session PTue

Characterization of high-resolution HafSOx inorganic resists

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Inorganic resists are of considerable interest for advanced lithography at the nanoscale due to the potential for both high resolution and low line width roughness (LWR). Historically inorganic resists generally suffered from low sensitivity, however approaches have been identified to improve sensitivity while maintaining high contrast. Recently, an aqueous precursor of inorganic nano-clusters, such as Hf(OH)4-2x-2y(O2)x(SO4) y?qH2O (HafSOx), has demonstrated significantly improved sensitivity to EUV and electrons, while still displaying high resolution and low LWR. In this presentation, we characterize the HafSOx precursor solutions with dynamic light scattering (DLS), and HafSOx films and patterned features on the order of 10 nm with high-resolution transmission electron microscopy (HR-TEM). DLS indicated the formation of nanoscale clusters in the precursor solution and that the stability of the precursors was enhanced by the addition of hydrogen peroxide and low temperature storage. HR-TEM of precursor solutions drop cast onto TEM grids confirmed the presence of nanoscale particles, which were consistent in size with the DLS measurements. HR-TEM cross sectional images were obtained from spin-coated films after various steps of the lithography process to investigate the evolution of structure and composition profiles of HafSOx films and patterns. It was found that spin-coated HafSOx films are initially uniform in appearance and composition, however extended exposure to the high energy TEM electron beam induces significant chemical migration. In particular, oxygen species are seen to migrate to the Si interface forming a SiOx layer with increasing TEM electron beam dose. HR-TEM of a HafSOx film exposed and developed in aqueous tetramethylammonium hydroxide (TMAH) shows an increased oxide layer thickness, suggesting oxygen migration to the Si interface may play a role in assisting radiation based condensation and thus the solubility transition observed in the films. Furthermore, sulfate is seen to be completely removed from the films during development in TMAH, initiating a second condensation process resulting in very smooth hafnium oxide films and patterns. The significant condensation exhibited in completely processed films allows for patterning of features at very low LWR (< 2 nm). HR-TEM cross-sections of patterned lines provide further information regarding line profiles and inter-line residual material. In particular, a near monolayer of clusters is seen to bond to the substrate surface at some step in the patterning process and remains following development. A thorough understanding of the HafSOx system is expected to help develop these classes of materials as promising next generation inorganic resists.

9048-127, Session PTue

The Energetiq EQ-10 EUV source for metrology: trends and developments

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Mask infrastructure is second only to scanner source power as a gating factor for high-throughput EUV lithography[1]. Actinic inspection of mask blanks, and aerial image analysis of patterned masks, are key near-term metrology challenges.

The Energetiq EQ-10 EUV source is in use today in several metrology and resist evaluation tools[2]. Evolution in the design of the metrology tools, and early experience with prototypes, is driving a re-evaluation of

metrology source requirements. Key parameters are brightness, stability (spatial and temporal), and etendue, and all of these are evolving from the initial specifications. In general, brightness requirements are being relaxed, while stability requirements are becoming more demanding. We will comment on the impact of these developments, and describe the specific algorithms used to calculate spatial stability and brightness for the Energetiq source.

The EQ-10 has applications at shorter wavelength as well. We will present data on operation at 6.7 nm (for advanced EUV R&D) and at 2.88 nm, where the source is in current use as a synchrotron replacement for water window microscopy[3].

[1] Enabling EUVL for HVM Insertion. Mark Phillips. Intel Corporation. International Symposium on EUV and Soft X-Ray Sources, 5 November 2013, Dublin, Ireland

[2] Metrology Sources for EUV Lithography, Stephen Horne, Energetiq, USA. CLEO 2013 9 June 2013, San Jose, CA USA

[3] Nanoscale Soft X-ray Microscopy in the Laboratory for Biological Applications, Arno Merkle, Xradia. CLEO 2013 9 June 2013, San Jose, CA USA

9048-128, Session PTue

Multicolumn ebeam reticle inspection using permanent magnet lens

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193 nm laser based process inspection systems will not be able to capture all defects on a 14 nm EUV reticle due to their resolution limitations. Actinic EUV inspection has high cost in terms of development and ownership. SEMs, although promising in their ability to detect small defects, have a low throughput. Multi-column ebeam inspection system increases the overall data rate of scanning electron beam microscopes, but its hardware designs and applications are not yet optimized.

This paper presents a multi-column system using permanent magnetic lens and a custom print for inspection methods. Each magnetic lens system is axially symmetric, formed from ring permanent magnetic excitation and rotationally symmetric magnetic pole-pieces. This enhances the symmetry and uniformity for high spatial resolution as well as uniformity of performance. Each column is 30mm in diameter, which allows about 69 beams for 300mm wafer simultaneously data collection. Simulation predicts 3 nm resolution with beam current of 4 nA. Custom printing method divides a full repeated reticle print into 69 sub regions on wafer, which has same dimension and orientation. Lithography tools print 69 reticle prints on the wafer in such a way that each column inspects a different reticle print sub region, allowing a collective data acquisition on wafer plane for the after development layers, allowing an inspection throughput of <5 hours per wafer.

9048-129, Session PTue

Optimization of LPP-EUV conversion efficiency by prepulses

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EUV lithography (EUVL) is one of the most promising candidates for the next generation lithography technologies for semiconductor industry, and Laser Produced Plasmas (LPP¡¯s) EUV source is one of the leading sources of EUV radiation for the application in EUVL. In the Shanghai Institute of Optics and Fine Mechanics, we have made a plan to develop LPP-EUV sources for these two years. The project and recent progresses will be introduced in this presentation. An experimental setup has been constructed, consisting of a target chamber and three kinds of laser sytem, which include a 50ns 80mJ TEA CO2 laser, a 10ns pulse Nd-YAG laser and a short pulse (picco-second or sub-ps) laser. One of the major challenges of the LPP-EUV source is to improving EUV conversion efficiency. Previous work shows that the conversion efficiency greatly benefits from a prepulse irradiating on the target before the main pulse works. The initial experiments are focused on optimization of the EUV conversion efficiency by prepulses. The influences of prepulses (pulse energy, pulse duration and the delay of prepulse) are investigated in our experiments and will be reported at the conference.

9048-130, Session PTue

Investigating printability of native defects on EUV mask blanks through simulations and experiments and developing a fundamental understanding of defect printability

Mihir Upadhyaya, SUNY College of Nanoscale Science & Engineering (United States); Vibhu Jindal, SEMATECH Inc. (United States); Henry Herbol, SEMATECH, Inc. (United States); Jenah Harris-Jones, SEMATECH Inc. (United States); Il-Yong Jang, SEMATECH, Inc. (United States); Hyuk Joo Kwon, SEMATECH Inc. (United States); Gregory Denbeaux, Univ. at Albany (United States)

Availability of defect-free masks is considered to be a critical issue for enabling extreme ultraviolet lithography (EUVL) as the next generation technology. Since completely defect-free masks will be hard to achieve, it is essential to have a good understanding of the defect printability as well as the fundamental aspects of a defect that result in the defect being printed. In this work, the native mask blank defects were characterized using atomic force microscopy (AFM) and cross-section transmission electron microscopy (TEM), and the defect printability of the characterized defects was evaluated using finite-difference time-domain (FDTD) simulations. The simulation results were compared with the through-focus aerial images obtained at the SEMATECH Actinic Inspection Tool (AIT) at Lawrence Berkeley National Lab (LBNL) for the characterized defects. There was good agreement between the through-focus FDTD simulation results and the AIT results, proving the robustness and accuracy of FDTD algorithm to simulate arbitrarily-shaped native mask defects. To model the Mo/Si multilayer growth over the native defects, which served as the input for the FDTD simulations, level-set technique was used to predict the evolution of the multilayer disruption over the defect. Unlike other models that assume a constant flux of atoms (of materials to be deposited) coming from a single direction, which is not the case, our model took into account the direction and incident fluxes of the materials to be deposited, as well as the rotation of the mask substrate, to accurately simulate the actual deposition conditions. The modeled multilayer growth was compared with the cross-section TEM images, and good agreement was observed between them. Further, FDTD simulations were used to investigate the various aspects associated with a defect like its volume, aspect ratio and slope, and the impact that each of these aspects has on the printability of the defect. Simulations were performed on 32 nm line and space (L/S) absorber patterns with different defect positions relative to the absorber stack. The aforementioned defect parameters were systematically varied to observe their effect on the printability of the defect. The defect printability was observed to be the most sensitive to the slope of the defect, and less dependent on its aspect ratio.

9048-131, Session PTue

Evaluating vacuum components for particle performance for EUV lithography

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Mask blank defectivity remains a challenge in EUV lithography. One of the mitigation strategies has been to identify the source of defect causing particles in the mask blank deposition tools. Vacuum components like valves, valve seals, stages, filters, etc. could be a possible source of particles in the tools. Therefore, it is necessary to quantify the amount of particles generated by the vacuum components. This feedback to the supplier can be used to help make vacuum components which shed fewer particles. We show results from a valve and nanoparticle particle test system at the College of Nanoscale Science and Engineering (CNSE) in collaboration with SEMATECH. The setup consists of a condensation particle counter (CPC), which can detect particles between 10 nm – 3 um, and a scanning mobility particle sizer (SMPS), which can provide the size distribution of the particles between 10 nm – 280 nm. We show results from testing two different types of 300 mm valves and compare the particle counts per cycle detected by the CPC for both. We also compare size distributions of both the valves. Moreover, choosing the best operating parameters of the valve can reduce the number of defects generated. We will present the optimized operating parameters.

9048-132, Session PTue

Purification solution for EUV

Ming-Chien Chiu, Gudeng Precision Industrial Co., Ltd. (Taiwan)

Extreme ultraviolet(EUV) pod is one of the most promising technologies for transport and shipping reticles, while maintaining reticle quality. Since the feature size miniaturization of semiconductor process, the purification requirement is becoming more strictly. However, the contamination protection issue has been received much attention. Therefore, many suppliers of semiconductor equipments devote to the purification issue of manufacturing processes of EUV pod. In this work, the Taguchi method was used to obtain the optimal condition to improve the purification quality of EUV by relative humidity(RH). The result showed that most important factor is flow rate which could reduce the time for low RH levels. The higher the flow rate was the lower the RH levels. The Taguchi method has an efficient reduction of time and cost of experiment and could determine the optimum condition to enhance the ability to decrease the RH.

9048-32, Session 8

Actinic review of EUV masks: First results from the AIMS EUV system integration *(Invited Paper)*

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The EUV mask infrastructure is of key importance for a successful introduction of EUV lithography into volume production. In particular, for the production of defect free masks, actinic review of potential defect sites is required. With such a review it can be decided if a defect printsand therefore requires repair. It also provides verification for the repair success and thus , along with the MeRiT®, completes the closed loop solution. To realize such an actinic review tool, Carl Zeiss and the SEMATECH EUVL Mask Infrastructure consortium started a development programme for an EUV aerial image metrology system (AIMS™) with realization of a prototype tool and delivery of the first customer tool anticipated for the second half of 2014. The concept and its feasibility assessment has been discussed in previous years at SPIE advanced lithography conferences. In this paper, we discuss the status of the on-going system integration and show first results from the integration of the prototype tool.

9048-33, Session 8

Actinic mask imaging: Recent results and future directions from the SHARP EUV Microscope

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The SEMATECH High Numerical Aperture Actinic Reticle Review Project (SHARP) is a synchrotron-based extreme ultraviolet (EUV) microscope dedicated to photomask research and described in several previous papers. [1, 2, 3] SHARP was commissioned in Spring 2013, and serves users from SEMATECH's member companies in the EUV lithography community. With its array of objective lenses, and fine-grained coherence control settings, SHARP is now used to conduct a wide variety of mask research including native and pattern defects, repair strategies, optical proximity correction, mask architecture, mask substrate roughness, cross-slit dependence, and more. Here, we present various performance studies and examples where SHARP's capabilities are used in EUV mask research.

One of SHARP's most compelling features is coherence control: SHARP can emulate the illumination properties of current and future lithography tools. In photolithography, as feature sizes are driven toward imaging-resolution limits, it is well known that aerial image properties depend strongly on the illumination partial coherence (essentially, the angular spectrum of the illumination). For example, at small feature sizes, at or below the coherent-imaging cutoff, increasing the partial-coherence ? value leads to increased modulation and depth of focus. Less well understood, but no less important, is the effect of partial coherence on real-world defects, repairs, and pattern roughness. Investigations performed on SHARP provide feedback for comparison with printing and mask inspection tools, and for simulation and modeling.

SHARP's current availability and imaging capabilities enable it to contribute to the active debate within the EUVL community about the future direction of high-resolution imaging—whether to achieve improvements via higher mask-side NA or higher magnification (with larger masks). SHARP's imaging lenses span a range of resolutions, emulating EUV scanners with 4x demagnification and numerical aperture (NA) values from 0.25 to 0.625, which, on the mask side, is equivalent to 0.0625 to 0.15625. The higher mask-side NA values require the central ray angle to extend beyond 6°, to 8° and up to 10°. This fact may prove problematic for mask makers, as conventional high-reflectivity multilayer coatings currently do not support reflection at angles beyond about 11° off-axis. Furthermore, mask absorber pattern shadowing becomes more severe the farther off-axis the illumination extends, and defects become more difficult to detect as critical dimensions shrink. Evidence to feed the debate can be generated by research conducted with SHARP.

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9048-34, Session 8

EUV patterned mask inspection with an advanced projection electron microscope (PEM) system

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Extreme Ultraviolet Lithography (EUVL) stands as the foremost next-generation lithographic technology after the ArF immersion lithography has reached its limit to deliver smaller features. EUV mask pattern defect detection is one of the major issues to realize device fabrication with EUV lithography. According to an ITRS2012-Update and defect printability simulation the sensitivity requirement for EUV patterned mask inspection system is to be 16 nm for half-pitch (hp) 16 nm node devices. We have designed a novel Projection Electron Microscopy (PEM) system, which appear to be quite promising for hp 1Xnm node mask inspection. To observe the PEM optics system, its potential for making to the 1X nm node have been addressed by evaluating its transmittance and its capability of resolving the pattern. From the new design concept, by employing higher electron energy as compared to that of the current PEM system, a higher degree of transmittance and better resolution could be achieved than called for by their designed values. And the basic performance of the Novel PEM technique was confirmed by obtaining hp 16 nm (64 nm on the mask) image that was consistent with the designed value.

Electron beam is generated from an electron gun, and is then deflected by a beam separator. Mask surface is illuminated through a cathode lens. Mask image projection optics consists of a cathode lens and a projection lens, where a TDI (Time Delay Integration) sensor captures the mask image. The illuminated area is wide enough to cover the entire sensor area. To execute full area mask inspection, the mask is scanned in Y direction and swath image of TDI sensor is captured with TDI mode. By repeating the step and scan movement, full mask area is inspected. Currently, the PEM optics is integrated with the pattern inspection system for the defect detection sensitivity evaluation. Model EBEYE-V30 inspection system has a high-resolution and high-throughput electron optics that enables a 19-hours long inspection time with a throughput determined by a data processing rate of 600MPPS (Mega Pixel Per Second), and a pixel size of 16 nm.

In this paper, we describe the experimental results of EUV patterned mask inspection using the system. A programmed defect mask was used for demonstrating the performance of the system. Defect images were obtained as difference images by comparing PEM images with- defects to the PEM images without-defects. The results showed that the defect with 16 nm in size could be detected. These results suggest that this advanced technique has performed well in the case of EUV patterned mask inspection for hp 16 nm node devices. Moreover, we discuss the systems extendibility to 11 nm node defect detection with higher electron illumination and improvement of defect detection signal processing.

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9048-35, Session 8

Novel zone plate design for EUV mask inspection

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In this paper, the design of a Zernike phase microscope for EUV mask inspection is presented and its performance on inspection of buried multi-layer defects is characterized through simulation. EUV defect inspection of bumps and pits on multilayer coated masks is challenging and a phase shift from plus and minus defocus positions can be used to enhance the contrast in the defect image [1]. The contrast improvement of the Zernike phase shift microscope is well known for inspecting phase objects and a concept for defining x-ray zone phase microscopes has been described [2]. In this paper we consider both the practicality of e-beam writing and the performance assessment of a Zernike zone plate microscope. The study is motivated by the fact that the Zernike phase microscope approach has several important advantages over use of defocus in defect inspection. First, the defect ray spectrum at intermediate radii in the imaging pupil can be fully phase shifted which is not possible with the slowly changing defocus aberration. Second, the radius where the abrupt phase transition occurs can be tuned to just include the near on-axis illumination. Third, the bumps and pits could be detected at the same time by Zernike phase microscope without shifting to defocus position.

These Zernike phase shift zone plates for EUV mask inspection could be defined in our existing multi-function zone plate generation code and then imported to the e-beam writer to build them. The schematic diagram of our zone plate generation code is shown in figure 1, with the abilities to input customized phase shift by putting them into optical path difference calculation and also the function that can go off-axis and tilt the zone plate all at the same time. Figure 2 shows an example for a zone plate with x-z tilt $\pi/4$ in radius, y-z tilt $\pi/6$ in radius, and astigmatism into calculation. Based on our optimized algorithm, the number of arcs to fit in each zone has reduced. Thus the computation and e-beam writing time could be significantly reduced. To generate the coordinates for a zone plate to be built by e-beam writer could be less than half hour.

The performance of a Zernike zone plate microscope compared to defocus inspection will be presented based on simulation of imaging. The buried layer scattering from typical buried defects is characterized first using RADICAL [3]. This scattering spectrum is then linked with image simulation in HyperLith from Panoramic Technologies [4]. Different height and lateral dimension of the buried defect are simulated to get the inspection signal which will be used to characterize the dependence of signal on illumination and filter radius. The effect of the Zernike phase microscope on the EUV substrate phase noise is also characterized to determine optimum definition of the phase shift and transition radius.

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9048-36, Session 8

A novel concept for actinic mask inspection method using ptychography at the Swiss Light Source

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Extreme ultraviolet lithography (EUVL) is the leading candidate for sub 20nm technology node in semiconductor device manufacturing. EUV pilot lines are being setup and high volume manufacturing tools, such as ASML's NXE 3300, are being installed this year. Despite these developments and progress, the maturity of EUV technology still faces several challenges to be addressed and needs substantial. For instance, mask defect inspection and review infrastructure occupies the second place in the list of main challenges of EUVL and mask metrology requirements continue to evolve. It is well recognized that one of the key infrastructure for EUV lithography manufacturing is the development of EUV mask inspection systems that can emulate the properties of an EUV scanner for high volumn manufacturing. In addition to the traditional mask inspection such as repair identification and repair, this tool is needed in EUV lithography to estimate the printability of the phase defects, which is possible only with actinic wavelength (EUV wavelength). The demands for the inspection technology are extremely high, i.e. extreme resolution, excellent detection ability of phase defect, and high throughput. In order to address these issues, several metrology tools are under development.

In this paper, we will introduce a novel concept for EUV actinic mask inspection technology using ptychography. Ptychography is an imaging method and is a hybrid of scanning transmission microscopy and lensless coherent diffraction imaging (CDI) method, combining many of the benefits offered by both these techniques. Ptychography provides both amplitude and phase information of the specimen with high resolution, large depth-of-focus, and high throughput. It has been demonstrated in the range of visible light to hard X-rays as well as electron microscopy and it is rapidly developing as a versatile microscopy tool for various applications. Paul Scherrer Institute (PSI) has played a leading role in the development of this technique, which is now routinely used for biology and materials science using hard X-rays.

Recognizing its great potential, we extended the application area of this technique to EUV wavelength and to the reflection mode for actinic mask inspection and developed a Ptychographic Actinic EUV Mask Inspection Tool (PAMIT) prototype. This prototype has been recently installed at the XIL-II beamline of the Swiss Light Source (SLS), which also hosts our EUV interference lithography tool. The XIL-II undulator beamline with undulator source is extendable from EUV to BEUV wavelength due to the tunability of the light source and optics. PAMIT consists of a simple condenser of Fresnel zone plate, sample stage and CCD detector. It is constructed as a flexible tool where the incident angle, wavelength, bandwidth, and numerical aperture, can be varied in a simple manner.

We present the first imaging performance of this tool through images of resolution test patterns and of phase defects in blank as well as patterned multilayer masks. In particular, we have imaged test patterns such as line and space (L/S) dense patterns, isolated patterns, and defects on blank multilayer masks using 0.25 NA and 6° of angle of incidence off-axis illumination.

We discuss the advantages of PAMIT tool based on the results of extensive numerical simulations where we show the potential and extended capabilities of ptychographic EUV as an inspection tool. We believe that the PAMIT can contribute to the studies on mask defect identification and repair. With the development of stand-alone coherent EUV sources and further development of this method, ptychography can be a powerful method for the realization of actinic mask inspection tools with high resolution and throughput.

9048-37, Session 8

E-beam inspection of EUV mask defects: To etch or not to etch?

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Numerous studies on printability of defects on EUV masks have been performed and e-beam inspection offers the highest detection sensitivity. Detailed analysis of e-beam inspection on EUV exposed programmed defect resist wafers was performed in a previous study and it required long inspection times. In this work, we show a method for a significant reduction of inspection time using patterned substrates etched into silicon. As most lithographically defined resist patterns are transferred into the substrate, inspection of after etch wafers can provide accurate printability results for a given defect type. The programmed defect test reticle is designed with both additive and subtractive features of varying size and shape, which are superimposed on a variety of features (ex: line/space, holes, and brick patterns).

The printability of defects on the EUV reticle can be assessed by comparing e-beam images from a wafer inspection tool to the print simulation in die-to-database mode using a standalone virtualization system. An Auto Defect Classification system was used to classify different types of defects. Inspection on resist wafers was done at 10nm pixel size and 16 frame average, etched wafers were inspected with a 10nm pixel size with 2 frame average. Inspection of a clear and absorber defects is shown in Figures 1 and 2 where 10nm_8F_ADI represents resist wafer and 10nm_1F_AEI represents etch wafer. We show comparable defect detection sensitivity to sub-10nm (1X) from inspection of both resist and etch patterns. Frame averaging is necessary to generate adequate signal from the patterns for efficient defect detection. Reduced averaging on etched substrates produced equivalent detection signal resulting in an 8X improvement in throughput compared to resist patterns. It should be noted from the results that resist patterns were transferred accurately into the substrate indicating no loss in transfer of programmed defects through the etch process.

9048-38, Session 9

High-radiance LDP source for mask-inspection application

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High-radiance EUV source is needed for actinic mask inspection applications. LDP source for a lithography application has been found to be also able to provide sufficient radiance with clean EUV photons for a mask inspection purpose. Introduction of new techniques with minor modification to LDP source has brought radiance level of 200 W/mm2/sr at plasma or 100 W/mm2/sr at a tool entrance. The LDP source is operated at moderate power level in order to ensure sufficient component lifetime and reliability. Operating condition such as discharge pulse energy, discharge frequency and laser parameter have been tuned to maximize radiance. It was found, throughout the preliminary experimental studies, that peak radiance of 180 W/mm2/sr was obtained with 10-kHz continuous long-term operation. Dose control was also successfully tested at this frequency showing sufficient dose stability. Since the plasma size of LDP is properly larger than LPP, not only radiance but also power is suitable for mask inspection applications. High reliability of LDP system is well proven from the field usage. Ushio is now pursuing lifetime test of key components, introduction of customized foil trap for debris mitigation and designing a prototype machine. Detailed and up-to-date information will be presented to be discussed at the conference..

9048-39, Session 9

Table-top EUV/soft x-ray source and wavefront measurements at short wavelengths

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An extremely compact and long-term stable laser-driven plasma source for metrological applications in the extreme UV and soft x-ray range was developed. Based on a pulsed gas jet target, it produces clean radiation

in the spectral region from 1 to 20nm, almost without any debris. In dependence of the chosen target gas, both quasi-monochromatic as well as broad-band spectra can be obtained. Comprehensive investigations on the emission characteristics and an improvement of the source brillance are presented in this contribution, along with performance tests of different types of optical focusing elements (EUV Schwarzschild objective, Kirkpatrick-Baez and ellipsoidal mirrors). Various applications of the table-top source are described, including EUV optics testing (reflectometry and degradation studies), characterization of resist materials and scintillators, and absorption spectroscopy (XANES).

Moreover, the propagation behaviour of short wavelength radiation is characterized with the help of a Hartmann-type wavefront sensor developed for the EUV/soft x-ray range. In cooperation with DESY / Hamburg this device has been applied for actinic fine-tuning of beam line focusing optics of the free electron laser FLASH / Hamburg at 13,5nm. The wavefront sensor is employed also for beam and optics characterization of High Harmonic (HHG) and plasma-based sources emitting in the EUV range.

9048-40, Session 9

Three-dimensional plasma shape effects on the EUV emission distribution in laser-droplet interactions

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The manufacturing technology for the next generation semi-conductor devices will be based on extreme ultraviolet lithography (EUVL) using a laser produced plasma (LPP) as a candidate 13.5nm light source. EUV sources must be stable, energy efficient and meet the power requirements at intermediate focus. In LPP sources normal incidence multi-layer (ML) collector mirrors are used, in order to focus the EUV radiation at the intermediate focus. The ML mirror has to be protected with a mitigation system, which is in charge of minimizing the plasma debris load without compromising the radiation intensity. In the design of the EUV source (for lithography and for inspection and metrology applications), the position and the dimension of the ML collector mirror, directly impact on the collector lifetime and on the EUV source power. For this reason it is important to define the EUV emission distribution in the space inside the EUV source, so that the tradeoff between large EUV flux, and low debris flux can be made. It is important for the EUV emission distribution to directly use droplet-based targets, because a different behavior is observed between the droplet-based LPP and the slab target-based LPP. The difference comes from the three-dimensional plume expansion for the droplet-based case, versus an expansion for the slab target-based case, which is confined in one direction by the target itself.

The EUV distribution is affected by the plasma plume expansion, because the surrounding plasma absorbs the EUV. In this work, the plasma plume shape is varied and its effects on the EUV spatial distribution are quantified. The variations of the plume shape are such that they can be reproduced in a EUV source by varying for example the pulse length or by adding an external magnetic field. Finally, the dependence of the laser pulse wavelength on the EUV spatial distribution is also presented. The study of the latter parameter permits to apply the conclusions of this work for metrology and inspection applications, where a Nd:YAG lasers are the optimum choice, and for lithography applications where CO2 lasers are used.

The study is performed by measuring the EUV distribution in time and space from a 30um tin droplets irradiated by a high-powered Nd:YAG laser operating at 1064nm, and at an irradiance of 2 1011 GW/cm2. The measurements are then used to calibrate a model for the opacity of the three dimensional plume surrounding the emission dominant region (EDR). The model is then used to quantify the absorption of the EUV emission in time and space, depending on the shape of the plasma (for example the result by varying the aspect ratio of the plasma plume b/a is shown in Fig. 1, where b is the plume dimension perpendicular to the laser axis and a is the parallel one) and on the position of the EDR with respect to the plasma plume.

9048-41, Session 9

Enhancing the performance of LPP sources for EUV and BEUV lithography

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Photon sources for extreme ultraviolet Lithography (EUVL) are still facing challenges in required performance for high volume manufacture. Currently EUVL community has focused the research and developments to the dual-pulse laser produced plasma (LPP) with mass-limited targets. Such complex systems require extensive optimization to enhance the conversion efficiency (CE) and components lifetime and such optimization requires significant experimental and costly efforts.

We continued to enhance our state-of-the art HEIGHTS package to analyze and optimize LPP sources and to make projections and realistic predictions of near future powerful devices. HEIGHTS package includes 3-D detail description of all integrated physical processes involved in LPP devices. The models continued to be upgraded and well benchmarked in each interaction physics phase of plasma evolution for EUV and BEUV production.

We simulated LPP sources in full 3-D geometry using fragmented and mass limited tin droplet targets composed of microdroplets as a result of prepulse or due to mist tiny droplets distribution. We studied mass dependence, laser parameters efficiency, atomic and ionic debris generation, and optimization of EUV (13.5 nm) and BEUV (6.7 nm) radiation output with prediction of potential damage to the optical collection system from energetic debris and the requirements for mitigating systems to reduce debris fluence. Our modeling and simulation included all phases of laser target evolution: from laser/droplet interaction, energy deposition, target vaporization and fragmentation, ionization, plasma hydrodynamic expansion, thermal and radiation energy redistribution, and EUV/BEUV photons collection as well as detail mapping of photons source location and size. Modeling results were benchmarked against recent experimental studies for the in-band photons production and for debris and ions generation for EUV and BEUV system.

9048-42, Session 10

Prediction of EUV resist outgassing

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EUV resists are known to outgas carbon-containing molecules. This is a concern because the carbon-containing molecules may contaminate the optical components and diminish their reflectivity. Witness sample (WS) testing system using electron beam (EB) has been proposed as a candidate for measuring EUV resist outgassing. However, the resist outgassing test is time consuming. It slows down the resist development cycle. In this paper, we derive an outgassing model to predict EUV resist outgassing and propose a novel method to test EUV resist outgassing.

In order to predict resist outgassing, specially designed EUV resists were prepared. Several parameters of EUV photoresists such as PAG acidity, Ea of the acid labile group, and base of the quencher are investigated. A semi-empirical model was derived based on all these chemical parameters. Using this model we found that the amount of the reacted acid labile group is the most critical factor in EUV resist outgassing. To validate the feasibility of the outgassing model, one novel approach, mass reduction method, was used to evaluate resist outgassing by measuring the resist mass change after exposure. The mass reduction method analyzes the wafers that were exposed by the EUV scanner and the outgassing tool to find the correlation between the outgassing test and resist outgassing in the EUV scanner. The mass reduction method can test outgassing faster. It also has good correlation with the trusted but slower WS testing system. In this paper, we combine the resist

outgassing model with the faster outgassing testing system to support EUV resist development.

9048-43, Session 10

The influence of witness sample intensity on resist outgas testing

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Before a resist can be used in an extreme ultraviolet (EUV) stepper, its contamination potential must be assessed by the resist outgas test established by the tool maker, ASML. This protocol requires irradiation of a witness sample with EUV photons (or electrons) in the same vacuum environment as a simultaneously irradiated wafer coated with the resist under test. The thickness of the resulting carbon growth on the witness sample is then measured using spectroscopic ellipsometry. If it is below a threshold value of 3 nm, the carbon contamination potential of the resist is considered acceptable. The degree of contamination by elements other than carbon is then measured by XPS after first removing the carbon deposit with atomic-hydrogen cleaning. The EUV power (or electron flux) on the resist-coated wafer is specifically determined by the need to deliver a dose of E0 (dose to clear) to the entire wafer in one hour. However, only a qualitative lower bound is specified for the intensity on the witness sample which much be sufficient to ensure "mass-limited growth." Here we investigate how variations of the witness sample intensity above this threshold may affect all three elements of the resist outgas testing procedure: the carbon thickness as measured by spectroscopic ellipsometry, the atomic-H cleaning rate and the amount of non-C contamination.

Previous studies at NIST demonstrated that the thickness determined by spectroscopic ellipsometry (using a fixed dielectric function) can significantly underestimate the amount of EUV-deposited carbon and that this discrepancy increases with EUV dose. One explanation of this is that EUV (or electron) irradiation continues to dehydrogenate the contamination molecules after deposition thereby increasing the density and sp2/sp3 ratio. This would result in lower ellipsometric thicknesses and slower atomic-H cleaning rates at higher EUV doses. Both of these effects have been observed during the course of resist outgas testing at NIST and elsewhere. Given that the witness sample intensity may differ among testing facilities, this could explain some reported discrepancies. There is also concern that the deposits formed under the high-intensity, slow-contamination conditions required in the HVM tool may be much more resistant to atomic-H cleaning than the deposits formed under outgas test conditions. To address these issues, we will present data on ellipsometric thicknesses and atomic-H cleaning rates of witness samples exposed to varying EUV doses and resist outgassing rates.

Finally, our previous work with EUV- and electron-irradiated polymer films suggested that the amount of F deposited during an outgas test could depend strongly on the intensity and method (electrons vs. photons) of witness sample irradiation. Recent preliminary measurements show that the F content of outgas contamination (before AH cleaning) increases with decreasing witness sample intensity. This suggests that EUV-induced desorption could play an important role in resist outgas testing, which could explain why significant amounts of F have never been detected in outgas tests. We will present ongoing measurements of non-C concentrations from several resists and discuss the degree to which this aspect of the resist outgas test depends on WS intensity.

9048-44, Session 10

Contribution of EUV resist components to the non-cleanable contaminations

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The suppression of outgassing from the EUV resist is one of the most significant challenges to be addressed for realizing EUVL since the outgassing might be the main contributor to the contamination of the mirror optics in scanners which result in the reflectivity loss. The pragmatic outgas qualification utilizing the witness sample (WS) is becoming the general method to clarify pass/fail for commercially available resists. In this method, two kinds of the contaminations are evaluated. One is the cleanable contamination which can be removed by the hydrogen radical cleaning treatment. Another is the remaining contamination which consists from the non-carbon components after the cleaning. Also, there are two irradiation sources; the EUV light and electron beam (EB), for both the resist exposure and contamination deposition. The EB source system is preferable due to its high throughput. However, between EUV source and EB source system, the correlation of the contamination, especially non-cleanable, is not so clear yet.

EUVL Infrastructure Development Center (EIDEC) was focused on the resist outgassing to realize high volume manufacturing by EUVL and has two outgassing evaluation systems [1-7]. One is the outgas evaluation system by EUV light from the synchrotron radiation of NEWSUBARU in Japan and another is the EB-based evaluation system. In our previous study, the comparison of cleanable contamination for several model resists showed the linear correlation between the EUV-based and EB-based evaluation system. Also we studied the non-cleanable contamination on the un-exposed area and clarified its dependency on the geometry of WS in the vacuum chamber. Moreover the comparison of both the cleanable and non-cleanable contaminations for resist family, which are consisted with the same components with various protecting ratio and PAG loading, showed good correlation. The comparison of non-cleanable contamination for resists with various components is however not so sufficient. Because those contaminations depend on not only resist components but also the geometrical settlement of the WS, cleaning and measurement conditions. The contamination adhesion will be studied in the conditions of the film structure of WS, pre-cleaning for WS, cleaning tool and so on. We will present the non-cleanable contamination-result comparison between EUV-based and EB-based for several resists with the different components and the details of its origin will be discussed.

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9048-45, Session 10

Resist outgassing contamination on EUV multilayer mirror analogues

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EUV lithography is a technology enabling next generation electronic devices, but issues with photoresist sensitivity, resolution and line edge roughness as well as tool downtime and throughput remain. As part of the industry's efforts to address these problems we have worked with resist suppliers to quantify the relative contamination rate of a variety of resists on EUV multilayer mirror analogues following ASML approved protocols. Here we present results of our ongoing program to better understand the effect of dose, resist thickness, exposure time, outgassed species, and EUV photons versus electron exposures on the contamination rate of ruthenium coated witness plates.

9048-46, Session 10

Relationship between resist outgassing and witness sample contamination in NXE outgas qualification using electrons and EUV photons

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EUV photoresists are considered as a potential source of optics contamination, since they introduce irradiation induced outgassing in the EUV vacuum environment. Therefore, before resist material can be used on e.g. ASML NXE:3100 or NXE:3300, it needs to be tested in dedicated equipment according to a well-defined procedure, which is based on exposing a witness sample (WS) in the vicinity of a simultaneously exposed resist as it outgasses. During this test, a resist related contamination is then generated on the WS, which can be qualified by ellipsometry and XPS. Such an outgassing test infrastructure is available at many sites, but exposure modes on the witness sample and wafer can be significantly different, which potentially could lead to different test results.

Since the outgas tester at imec allows different exposure modes on the resist wafer, we have investigated possible differences in test results for various resists. The exposure mode is either by EUV photons from an Energetiq source or by electrons (~2-5keV) from Kimball Physics Electron gun. During this testing the outgassing can be measured quasi-continuously for the different atomic masses involved by Residual Gas Analysis (RGA). Using this infrastructure where both RGA outgassing and WS contamination can be measured, we have found that the contamination thickness resulting from the NXE WS outgas test correlates well with the time integral of the mass-weighted sum of RGA peaks above some threshold mass [1]. The parameters in the correlation (the mass-weighting exponent and threshold mass) could be determined by linear regression of outgas test results from a limited number of resists with different formulations.

In this work we show an extensive overview of test results from (commercial and model) resist materials that have been tested towards this relationship. It is found that the correlation holds for all resist material tested so far independently from suppliers, which suggests that the approach of this outgassing quantification is in 1st order very adequate for the EUV resist chemistries that are currently used. Note also that the test results are including both EUV exposed and electron exposed resist test results. It is now investigated how meaningful the (small) variations are in the RGA-CG correlation plot, and to which parameters these are related (test conditions or resist chemistry). Moreover, it will be investigated in what way the time dependent outgas parameter could be used as a model to predict contamination results in different test conditions.

[1] I. Pollentier et al, Proc. of SPIE Vol. 8679, 86790K

9048-47, Session 11

Oxide nanoparticle photoresists: EUV patterning and mechanistic evidence

Souvik Chakrabarty, Li Li, Cornell Univ. (United States); Chandrasekhar Sarma, SEMATECH Inc. (United States); Emmanuel P. Giannelis, Christopher K. Ober, Cornell Univ. (United States)

Previous investigations on the patterning mechanism of nanoparticle photoresists provided insight into ligand displacement exerting a controlling influence on dissolution behavior of nanoparticles in organic developers. To extend this study and to confirm our earlier observation, hybrid nanoparticles were synthesized comprised of a hafnium oxide core and surface functionalized by aliphatic or aromatic acid groups. Acid ligands with a range of pKa values were chosen as the organic component in order to study the effect of binding affinity on the patterning process. The present study describes EUV patterning results on the hafnium oxide nanoparticle resists in the presence of both a non-ionic photoacid generator which liberates a sulphonic acid derivative and a photoradical initiator which liberates benzoic acid on UV exposure. Resolution up to 22 nm (line-space) was achieved for the HfO2-benzoate resists with sensitivities as high as 15 mJ/cm2 at EUV wavelengths for compositions having between 5 wt% and 7 wt% nonionic PAG. LER performance can be improved with some sacrifice in sensitivity. The present study on nanoparticle resists functionalized by strongly bound ligands provides useful insights on ligand strength and sensitivity, wherein, optimizing the difference in binding affinity between the photoacid generated ligand and the nanoparticle surface ligand becomes essential. Investigation of patterning on the nanoparticle resists offers immense scope for ligand modification by altering their binding strength, thus optimizing resist behavior.

9048-48, Session 11

Novel EUV resist materials for 16nm half pitch and EUV resist defects

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Extreme ultraviolet (EUV) lithography is a candidate for the manufacturing of semiconductor devices at the 22 nm half pitch node and below. EUV lithography requires high performance resist with limited outgassing property. The key challenge for EUV resist is the simultaneous requirement of ultrahigh resolution (R), low line edge roughness (L) and high sensitivity (S) for lines and spaces (LS) features. To achieve high sensitivity, containing fluorine atom is one of the popular methods because the fluorine atom absorbs EUV light strongly. However, when the resist polymer has fluorine atom, the contact angle (CA) of the resist becomes high. It is difficult to rinse high CA resist so the containing fluorine atom have a problem of defects. In this paper, we will report the relationship of line edge roughness and acid diffusion length and the method to diminish defects caused by high CA. We achieved good resolution and LER improvement by controlling acid diffusion length. Moreover, we found the relationship of the number of defects and the structure of the monomers containing fluorine units.

9048-49, Session 11

Novel EUV resist materials design for 14nm half-pitch and below

Hideaki Tsubaki, Shinji Tarutani, Toru Fujimori, Hiroo Takizawa, Takahiro Goto, FUJIFILM Corp. (Japan)

We report herein novel chemically amplified resist (CAR) materials design to overcome resolution, LWR, and sensitivity (RLS) requirements. Point beam E-beam at FUJIFILM and EUV micro-field exposure tool (MET) at SEMATECH Berkeley were utilized to systematically investigate how to satisfy such a challenging RLS requirements. Key design is to achieve a significantly short chemical blur for 14 nm half pitch using novel CAR materials. Another key is to design novel sensitizers to afford high sensitivity against EUV light. New sensitizer will be described in this paper. Advantage of negative-tone imaging will be also reported in this paper in viewpoint of LWR.

9048-50, Session 11

Electron and hole transfer in anion-bound chemically amplified resists used in extreme-ultraviolet lithography

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Extreme ultraviolet (EUV) lithography is the most promising candidate for the mass production of semiconductor devices with half-pitches of 16nm and below. The feature size is shrinking so markedly that the uniformity of acid generator distribution in resist matrices is becoming a serious problem. The phase separation between resist components has also been concerned. The best way to solve the problems is the incorporation of acid generators into polymers typically via covalent bonds. Particularly, the incorporation of the anion part of acid generators into polymers is expected to improve LER and achieve a high resolution by reducing acid diffusion length.

First we measured the acid generation efficiency of our designed anion-bound polymer (ABP). As the result, the efficiency of the ABP was lower than the mixture of PHS and TPS-TF. For the enhancement of EUV resist performance, the result is disadvantage. In this report, the reaction mechanism of anion-bound chemically amplified EUV resists will be discussed using pulse radiolysis, and the transfer of electron and hole generated through ionization will be discussed

9048-51, Session 11

Secondary electrons in EUV: Experimental studies

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The interaction of EUV photons with photoresists generates primary and secondary electrons, which subsequently induce the chemical decomposition of photoacid generator (PAG) molecules within the resist. Since the initial spatial distribution of acid molecules is a key determinant of the fidelity of pattern transfer from photomask to resist, understanding in detail how electrons – particularly low-energy electrons – propagate and interact with the resist during exposure is critical. More specifically, we are investigating: 1) how far secondary electrons travel, 2) how many secondary electrons are made at each energy level, and 3) how reactive secondary electrons are with PAG molecules as a function of energy.

A custom electron exposure chamber was built to experimentally probe these three questions. By using a combination of ellipsometry after exposing and processing the resist and in-situ quadrupole mass spectrometry, we can determine the number of productive reactions as a function of thickness loss and quantitate the number of PAG reactions. In addition, direct measurement of the penetration depth of the electrons can be performed with a picoammeter connected to a conductive layer directly below the photoresist. Finally, using photoresist coated on a conductive substrate and a custom apparatus that uses a probe to apply a potential to the surface of the resist, we can characterize the resist's dielectric properties directly.

9048-52, Session 11

Comparative analysis of shot noise characteristics of EUV and e-beam lithography

Suchit Bhattarai, Univ. of California, Berkeley (United States); Weilun Chao, Lawrence Berkeley National Lab. (United States); Andrew R. Neureuther, Univ. of California, Berkeley (United States); Patrick P. Naulleau, Lawrence Berkeley National Lab. (United States)

This paper presents a systematic analysis of shot noise by conducting an experimental side-by-side comparison of EUV and e-beam printing performance of a leading chemically amplified (CA) EUV resist. LER and sensitivity are two of the most important resist metrics that are closely affected by shot noise. Limitations imposed by shot noise on LER/sensitivity become increasingly important with shrinking feature sizes. We quantify the noise limits for EUV and e-beam printing through both an experimental and a modeling approach, and compute the total shot noise accounting for all the discrete events involved in the imaging process. Differences in the exposure events in the CA resist between EUV and e-beam are likely within a factor of two, so the main challenges are in replicating the experiments and refining the model carefully for a meaningful comparison.

50 nm lines/spaces were patterned using annular EUV illumination and 100 keV Gaussian e-beam at the Center for X-Ray Optics. Doses to print the lines were 13.5 mJ/cm2 (EUV) and 83 ?C/cm2 (e-beam), which correspond to energy density of 567 J/cm3 and 506 J/cm3 respectively. The measured LERs averaged over 41 lines were 4.42 nm and 5.31 nm for EUV and e-beam respectively, and the standard deviations were 0.47 nm and 1.03 nm respectively. Measured exposure latitude over ±10% CD change was larger for EUV (0.33) compared to e-beam (0.22), despite a larger expected e-beam deprotection gradient. Results will be reported on more extensive experiments aimed at distinguishing LER and exposure latitude between EUV and e-beam with significant statistical confidence. Results for printing performance of contact arrays will also be reported.

We use many of the physical models reported in literature for shot noise calculations. Shot noise originates from random fluctuations in the number of discrete events involved in the imaging process, e.g. incident electron/photon absorption, secondary electron generation, and PAG activation. Han et. al. generalized the method of virtual quanta for computing the number of absorbed electrons [1]. Models for secondary electron generation with e-beam and acid generation probability as a function of secondary electron range were developed by Wu et. al. [2] and Kozawa et. al., [3] respectively. This paper will demonstrate a shot noise model that encapsulates the contribution of all these discrete events. Results will be reported on the comparison between computed noise and the noise determined through measured LERs.

[1] G. Han and F. Cerrina, "Energy transfer between electrons and photoresist: Its relation to resolution," J. Vac. Sci & Technol. B, 18(6), 3297 (2000)

[2] B. Wu, A. R. Neureuther, "Energy deposition and transfer in electron-beam lithography," J. Vac. Sci & Technol. B, 19(6), 2508 (2001)

[3] T. Kozawa, S. Tagawa, T. Kai, T. Shimokawa, "Sensitization distance and acid generation efficiency in a model system of chemically amplified electron beam resist with methacrylate backbone polymer," Journal of Photopolymer Science and Technology, 577-583 (2007)

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9048-53, Session 11

Improved measurement capabilities at the NIST EUV Reflectometry Facility

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The extreme ultraviolet reflectometry facility at the National Institute of Standards and Technology was originally designed to accommodate optics up to 35 cm in diameter and 40 kg in mass with sags up to 5 cm and surface slopes up to 30°. Recently, laser-produced-plasma collection optics have exceeded these values. In response, NIST has instituted improvements to allow measurement of optics up to 45 cm in diameter with sag up to 15 cm and surface slopes up to 50°. These improvements have been to both hardware and data acquisition methods.

The reflectometer has a sample goniometer with three rotation and three translation axes and detector mount with one rotation and two translation axes. Due to fundamental mechanical constraints in the original design, increasing the range of motion in the linear displacement axes of the sample goniometer would be prohibitive. Therefore, in order to access the entire surface of a 45-cm-diameter optic, we have moved the center of platen rotation 5 cm along the horizontal axis (x-axis) from the previous center, converting the range of x-motion from ±17.5 cm to +22.5 cm/-12.5 cm. To accommodate slopes up to 500, the transverse motion of the detector was increased from 100 mm to 300 mm.

Since laser-produced-plasma sources are unpolarized, the desired reflectivity is that for unpolarized light. The high degree of horizontal polarization of the synchrotron radiation complicates the determination of unpolarized reflectivity unless special provisions are made. We have chosen a mechanical method to achieve this goal; by positioning the mirror for any spot on the surface so that the polarization vector is 45° from the plane of reflection, we obtain the unpolarized reflectivity by direct measurement.

In order to accommodate sag in excess of 5 cm, the sample surface must deviate from the center of rotation of the sample goniometer. To accommodate the 45° requirement on the plane of incidence and simultaneously determine the position of the beam on the sample and detector, we developed a complex algorithm for the goniometer settings as a function of position on the mirror, with a piece of the program providing the appropriate location for the detector along the reflected ray. We will describe full capabilities of the new instrument along with the model used to develop the algorithm for the placement of the sample and detector. We will finally present reflectivity data from one such large collection optic.

9048-54, Session 12

EUV lithography: NXE platform performance overview *(Invited Paper)*

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The first NXE3300B systems have been qualified. The NXE:3300B is ASML's third generation EUV system and has an increased NA of 0.33. It succeeds the NXE:3100 system (NA of 0.25), which has allowed customers to gain valuable EUV experience. Good overlay and imaging performance has been shown on the NXE:3300B system in line with 22nm device requirements. Dedicated chuck overlay and full wafer CDU performance of <2nm for 22nm dense and iso lines at a dose of ~19 mJ/cm2 has been achieved. Matched machine overlay (NXE to immersion) down to 3.5nm has been demonstrated. Dense lines have been exposed down to 13nm half pitch, and contact holes down to 17nm half pitch. Metal-1 10nm node layers have been exposed with a DOF of 120nm, and using single spacer assisted double patterning flow a resolution of 9nm has been achieved.

Source power is the major challenge to overcome in order to achieve cost-effectiveness in EUV and enable introduction into High Volume Manufacturing. With the development of prepulse operation of the source significant steps in power have been made, and with automated control the sources have been prepared to be used in a production fab environment.

Further flexible pupil formation is under development for the NXE:3300B which will extend the usage of the system in HVM, and the resolutions for the full system performance can be extended to 16nm. Further improvements in defectivity performance have been made, while in parallel full-scale pellicles are being investigated.

In this paper we will discuss the current NXE:3300B performance, its future enhancements and the recent progress in EUV source performance.

9048-55, Session 12

Projection optics for EUVL microfield exposure tools with 0.5 NA

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In support of the Extreme Ultraviolet Lithography (EUVL) roadmap, a SEMATECH /CNSE joint program is under way to develop photolithography tools at 13.5 nm wavelength with small fields (Micro-field Exposure Tools [METs]) and Numerical Apertures (NAs) of 0.5 that will enable advanced R&D projects addressing issues related to EUV extendibility, including ultra-high resolution resist studies and next generation mask architectures.

The transmitted wavefront error of the two-mirror optical projection module (Projection Optics Box [POB]) is specified to as small as 0.5-nm root mean square (rms) at the center of the field and less than 1 nm rms over its entire 30 µm ? 200 µm image field. Lithography models of the specified aberrations have been shown to support less than 12 nm resolution under conventional illumination and down to an ultimate resolution of 8 nm with extreme dipole illumination. As with the current MET systems, the new MET has a magnification of 5X resulting in a mask side NA equivalent to a 0.4-NA production scale 4X system. Moreover, the mask angle of incidence is kept at 6 degrees mitigating the detrimental mask effects present in high NA 4X systems.

In our presentation at last year's conference (8672-42) we discussed the POB's design, requirements and the resulting challenges. Furthermore, the techniques and equipment that have been applied to manufacture and test the mirrors and the POB were described.

This year, the focus will be on presenting achievements and results.

Mirror metrology data will be presented and mirror polishing results will be discussed supporting less than 5% system flare and specified transmitted wavefront performance. Preliminary POB alignment wavefront results will also be presented highlighting the mechanical stability of the module.

Also discussed will be the designs of multilayer coatings and results on their uniformity and stability.

We note that an update on the development of the entire lithography tool including the illumination sub-system will be given in a companion presentation.

SEMATECH = SEmiconductor MAnufacturing TECHnology Association

CNSE = College of Nanoscale Science and Engineering

9048-56, Session 12

Across scanner platform optimization to enable EUV lithography at the 10nm logic node

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With the move to the 10-nm logic node it is expected EUV lithography will be used to print the very most critical layers. This will enable the maximum possible area shrink factor, and avoids further design limitations imposed by double patterning. For the other critical layers ArF immersion lithography will remain the working horse, and as a consequence, the process integration will require across scanner platform optimization of the lithography processing steps.

In this paper we will discuss the working flow used to optimize imaging and overlay simultaneously on the EUV scanner platform and the ArF scanner platform. This is done using computational lithography and angle resolved scatterometry to characterize imaging and overlay performance of the scanners.

In the mixed used of EUV and ArF for critical patterns, image placement, line width CD and overlay determine the resulting performance of the device. These parameters not only must be optimized on each individual scanner, but also need to be matched across platform. Using computational lithography, process windows are optimized and sensitivities for optics aberrations and process variations are minimized. Using wafer metrology the exact overlay and CD fingerprints of the scanners can be characterized and by adjusting the scanner actuators the wafer fingerprints can be optimized and matched. Best performance is obtained using field-to-field adjustments of the high order intra-field parameters for imaging and overlay.

The results presented in the paper will demonstrate scanner baseline control for matched EUV to ArF lithography performance.

9048-57, Session 12

Update on the SEMATECH 0.5 NA extreme-ultraviolet lithography (EUVL) microfield exposure tool (MET)

Kevin D. Cummings, Dominic Ashworth, SEMATECH Inc. (United States); Mark Bremer, Rodney Chin, Zygo Corporation (United States); Yu-Jen Fan, SEMATECH Inc. (United States); Luc Girard, Holger K. Glatzel, Zygo Corporation (United States); Michael Goldstein, SEMATECH Inc. (United States); Eric M. Gullikson, Lawrence Berkeley National Lab. (United States); Jame Kennon, Robert Kestner, Louis A. Marchetti, Zygo Corporation (United States); Patrick P. Naulleau, Lawrence Berkeley National Lab. (United States); Regina Soufli, Lawrence Livermore National Lab. (United States); Johannes M. Bauer, Markus Mengel, Joachim Welker, Michael Grupp, Erik M. Sohmen, Carl Zeiss SMT GmbH (Germany); Stefan Wurm, SEMATECH Inc. (United States)

In support of the Extreme Ultraviolet Lithography (EUVL) roadmap, a SEMATECH/CNSE joint program is underway to produce multiple EUVL (wavelength of 13.5 nm) R&D photolithography tools. The 0.5 NA projection optic magnification (5X), track length and mechanical interfaces match the currently installed 0.3 NA micro-field exposure tools (MET) projection optic. Therefore significant changes to the current tool platforms and other adjacent modules are not necessary. However many of the existing systems do need upgrades to achieve the anticipated smaller exposure feature sizes. To date we have made considerable progress in the production of the first of the two-mirror 0.5 NA projection optics for EUVL. With a measured transmitted wavefront error of less than 1 nm root mean square (RMS) over its 30 ?m ? 200 ?m image field, lithography modeling shows that a predicted resolution of $\leq$ 12 nm and an ultimate resolution of 8 nm (with extreme dipole illumination) will be possible.

This presentation will present an update from the 0.5 NA EUVL program. We will detail the more significant activities that are being undertaken to upgrade the MET, report program achievements, compare the resulting data to our specifications, and discuss expected performance. A companion presentation will discuss the details of the development of the projection optics module lead by ZYGO Corporation.

9048-58, Session 12

Progress on EUV-pellicle development

Carmen Zoldesi, Kursat Bal, ASML Netherlands B.V. (Netherlands); Brian D. Blum, ASML (United States); Guus Bock, Derk Brouns, ASML Netherlands B.V. (Netherlands); Florian Dhalluin, ASML Netherlands B.V (Netherlands); Nina V. Dziomkina, ASML Netherlands B.V. (Netherlands); Juan Diego Espinoza, ASML Netherlands B.V (Netherlands); Joost de Hoogh, Silvester Houweling, Maarten J. Jansen, Mohammad Kamali, Alain Kempa, Robert C. de Kruif, Jorge Lima, Yang Liu, Henk Meijer, Hans Meiling, Ijen van Mil, Marco Reijnen, Luigi Scaccabarozzi, Daniel A. Smith, Beatrijs Verbrugge, Laurens de Winters, ASML Netherlands B.V. (Netherlands); Xugang Xiong, John D. Zimmerman, ASML (United States)

As EUV approaches high volume manufacturing, reticle defectivity becomes an even more relevant topic for further investigation. Current baseline strategy for EUV defectivity management is to design, build and maintain a clean system without pellicle. In order to secure reticle front side particle adders to an acceptable level for high volume manufacturing, EUV pellicle is being actively investigated. Last year ASML reported on our initial EUV pellicle feasibility. In this paper, we will update on our progress since then. We will also provide an update to pellicle requirements published last year. Further, we present experimental results showing the viability and challenges of potential EUV pellicle materials, including, material properties, imaging capability, scalability and manufacturability.

9048-59, Session 12

Driving the industry to a consensus on high-NA EUV

Patrick A. Kearney, SEMATECH Inc. (United States); Eric Hendrickx, IMEC (Belgium); Obert R. Wood II, GLOBALFOUNDRIES Inc. (United States); Gregory R. McIntyre, IBM Corp. (United States); Soichi Inoue, EUVL Infrastructure Development Ctr., Inc. (Japan); Stefan Wurm, SEMATECH Inc. (United States)

High-NA EUV has been proposed for insertion at <10nm HP nodes. In order to meet this schedule, the industry needs to start working on the transition from EUV to high-NA EUV in 2014. SEMATECH, IMEC, and EIDEC are collaborating to drive the industry toward consensus on what high-NA EUV will look like, and define where more data or lack of industry consensus exist. Imaging requirements will require higher magnification which implies either a smaller wafer field or a larger mask. An industry survey was conducted, and two previous industry meetings, at SEMICON and the EUV symposium, have provided important feedback into what the remaining issues are. This talk summarizes the current consensus and identifies where the remaining gaps exist.

Figure 1 shows the 8 high-NA EUV cases considered. The ovals indicate the preferred cases for the different industry groups, chipmakers, mask makers, and mask equipment and material suppliers as reported in the surveys. The chipmakers want full-field solutions, which implies a larger mask as the industry moves to high-NA. In contrast, the mask makers and mask equipment and material suppliers want to stay with 6" masks. In the discussions at the SEMICON West meeting, it was clear that the mask equipment and material suppliers will not invest in a larger mask size without clear indication from the chipmakers that a specific larger mask size is required. They would also prefer some sort of help in financing the transition. The chipmakers seem to be waiting for the successful implementation of EUV before committing to high-NA EUV. If this impasse continues, it may delay the implementation of high-NA EUVand limit the choice of the early high-NA implementation to the cases with 6" masks.

9048-60, Session 13

Whatever will be the EUVL extension technology which realizes a next-generation semiconductor device? *(Invited Paper)*

Tatsuhiko Higashiki, Toshiba Corp. (Japan)

No Abstract Available

9048-61, Session 13

Integration of a EUV metal layer: 20/14nm test-chip demonstration *(Invited Paper)*

Craig D. Higgins, GLOBALFOUNDRIES Inc. (United States); Erik A. Verduijn, GLOBALFOUNDRIES Inc. (Belgium); Xiang Hu, Jean Raymond Fakhoury, Mark Zaleski, Yi Zhou, Pawitter J. Mangat, GLOBALFOUNDRIES Inc. (United States)

EUV technology has steadily progressed over the years including the introduction of a pre-production scanner- NXE3100 that has enabled EUV process development to advance one step closer to production. We have carried out the integration of a test vehicle with 20/14nm metal layer design rules converting double patterning with ArF immersion process to EUV with a single patterning solution utilizing NXE3100 exposure tool. The exercise through the integration of a mature test chip with a EUV level has allowed us to have early assessment on the process challenges and new workflow required to enable EUV to the mass production stage. Utilizing the NXE3100 in IMEC, we have developed an OPC model and litho process to support 20/14nm node EUV wafer integration of a metal layer in conjunction with multiple immersion ArF layers. This allows early assessment of mix-and-match overlay for EUV to immersion system that is critical for EUV insertion strategy. It also enables further understanding of thin film EUV resist litho-etch process, OPC, and mask defect control specific to EUV single patterning.

Through this work we have demonstrated high wafer yields on a 20/14nm backend test vehicle utilizing single EUV Metal layer along with additional ArF immersion levels. We were able to successfully demonstrate low mask defectivity and good via chain, open and short electrical yields. This presentation will summarize the learning cycles from mask defect mitigation and mix machine overlay through post metal CMP wafer integration highlighting the key accomplishments and future challenges.

9048-62, Session 13

The economic impact of EUV lithography on critical process modules

Arindam Mallik, Naoto Horiguchi, Jürgen Bömmels, Aaron Thean, Kathy Barla, Geert Vandenberghe, Kurt G. Ronse, Julien Ryckaert, Abdelkarim Mercha, Laith Altimime, Diederik Verkest, An Steegen, IMEC (Belgium)

Traditionally, semiconductor density scaling has been supported by optical lithography. The ability of the exposure tools to provide shorter exposure wavelengths or higher numerical apertures have allowed optical lithography be on the forefront of dimensional scaling for the semiconductor industry. Unfortunately, the roadmap for lithography is currently at a juncture of major paradigm shift. EUV Lithography is steadily maturing but not fully ready to be inserted into HVM. Unfortunately, no alternative litho candidate is on the horizon that can take over from 193nm. As a result, it is important to look into the insertion point of EUV that would be ideal for the industry from an economical perspective. This paper details the benefit observed by such a transition.

We have analyzed the module-based cost over different technology node. We see an increase in wafer cost from 28nm till 10nm. The primary reasons for such an exponential increase is the introduction to epi-stressors and local interconnects (N20), introduction to finFET (N14). In the N10 node, complexities in the FEOL, MOL and BEOL results an increase in wafer cost significantly, due to dimensional scaling and resultant multiple patterning. We looked into each of the FEOL, MOL and BEOL modules to analyze the cost contributors at every technology node. We have proposed EUV transition of every critical layer at an industry relevant N10 technology node. The primary contribution of this paper is to quantify the benefit observed in each of this layer to shortlist the most promising candidate. After a conclusive analysis with the cost model developed in [1], we evaluate that EUVL adoption in gate pattern (FEOL) will result will not a cost benefit in the FEOL module. For the MOL module, the baseline N10 assumptions have two critical layers that use total 7 lithography masks. We looked into gradually introducing EUV into the local interconnect layers as shown in Figure 1(b). Among the local interconnect layers, IM2 layers seems to be most beneficial for EUV transition as it reduces the MOL cost by 17%. A transition to a single-IM deep and shallow interconnect scheme can reduce the MOL cost by 33%. However, the contribution of the local interconnect layers on the overall wafer cost is below 10%. As a result, around 3.5% of the overall wafer cost gets reduced due to EUVL transition of the MOL. The V1_M5 BEOL stack seems to be the most expensive layers in an N10 equivalent technology that is responsible for almost 60% of the total wafer cost. We evaluated the benefit of introducing 193i triple-patterning and EUV in this stack. An introduction to EUV in the Vx layer would reduce the cost of the stack by 6%. A full transition to EUV (EUVMxVx) would cut down the cost of the V1_M5 stack by 17% as compared to a LELELE_MxVx solution. EUVL will enable a number of critical layers to be printed in single pattern and thus reducing both number of process steps and critical masks. The BEOL MxVx stack has been identified as the most viable stack to introduce EUVL to benefit in terms of cost. A throughput sensitivity analysis of EUVL shows 75 wafers/hour to be the enabling factor in terms of balancing cost of EUVL innovation. Additionally, the cost of mask would play a significant role in selection of EUV lithography for a critical layer based on the wafer production volume. An EUV mask is assumed to be 75% more expensive than corresponding 193i mask in this particular study. Primary results from this study shows for low volume mask usage (5000 wafers/mask), the cross-over point for EUV vs 193i lithography occurs earlier than that of High volume production (50000 wafers/mask).

[1] Arindam Mallik, Wim Vansumere, Julien Ryckaert, et al., "The need for EUV lithography at advanced technology for sustainable wafer cost", SPIE Advanced Lithography, February 2013

9048-106, Session 13

High-resist sensitization by pattern and flood combination lithography

Seiichi Tagawa, Akihiro Oshima, Satoshi Enomoto, Osaka Univ. (Japan)

In EUV lithography, a promising next generation high volume manufacturing (HVM) candidate, the most critical issue over the past decade, has been low intensity of the EUV light source. The sensitization of EUV and EB resists to compensate for this low intensity is one of the most critical challenges for EUV and EB lithography implementation for HVM. However, the intensity remains much lower than the required EUV power. The sensitization of the EUV resist without loss in space resolution is inadequate to compensate for the low intensity of the EUV source by EUV single exposure. Therefore, we propose high resist sensitization by the combination lithography of EUV or EB pattern exposure with UV flood exposure (PF combination lithography). This method achieved one order higher sensitivity than that by EB single pattern exposure without loss in space resolution.

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9049-1, Session 1

Forced evolution: the increasingly symbiotic relationship of future device, circuit, and patterning technology *(Keynote Presentation)*

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Innovation in CMOS device architecture, circuit design and patterning technology has consistently resulted in the elimination of obstacles that were predicted to be insurmountable barriers to further scaling. In many ways, this method of development is similar to the “forced evolution” effect observed in biological systems. Organisms can undergo rapid transformation as a response to unexpected threats in their environment as a means to ensure their survival. The resulting evolutionary metamorphosis often produces surprising results.

In the past decade, an increased use of physics-based predictive models has aided technology development and reduced some of the uncertainty associated with defining future research directions. When combined with experimental data from prototype device and interconnect structures these models can be used to construct scenarios for continued CMOS scaling well beyond the 10 nm node that will deliver reduced power, increased density and higher frequency performance. While some aspects of these envisioned technology generations remain unclear, the need for accurate, high-density patterning coupled to suitable circuit design topologies that leverage the features of future devices is unquestionable.

In order to discern which patterning options have the best chance of delivering useful solutions, it becomes important to understand the way that devices, interconnects and circuits are likely to co-evolve. In this talk, we will focus on this symbiotic development as it pertains to the manufacturing of high performance logic and embedded memory circuits. Based on the density and feature complexity requirements of future process generations, motivations for pursuing directed self-assembly (DSA), sidewall image transfer (SIT), multiple expose 193i and EUV will be discussed. We will also present results from circuit pattern and device prototyping work at densities commensurate with the 7 nm node and beyond fabricated using some of these patterning techniques.

9049-2, Session 1

Nanomanufacturing: Is there life beyond silicon? *(Keynote Presentation)*

James A. Liddle, National Institute of Standards and Technology (United States)

Photolithography applied to the fabrication of integrated circuits in silicon is the preeminent nanomanufacturing technology and has transformed our world. The functionality and value provided per unit area by silicon are extraordinary by any measure. As a consequence, it is economically viable to use very capital-intensive fabrication processes to generate the required nanostructures. The success of silicon has inspired many to contemplate using the IC fabrication toolbox to produce nanoscale products, but the vast majority of other nanotechnology products cannot support the cost of such sophisticated manufacturing methods. Further, the diversity of nanoscale items is so great, that it is only in rare instances that process and design modularity is sufficient to result in the development of a platform manufacturing technology. In this talk I will give examples of how the complexity of the final product, its value and the overall market size dictate what type of nanomanufacturing approach, if any, is viable, using examples from the flat panel display, high-density storage, photonics and biomedical fields.

9049-3, Session 1

E-beam lithography: The real case for manufacturing *(Keynote Presentation)*

Timothy R. Groves, Univ. at Albany (United States)

Electron beam lithography(EBL) is firmly established as the method of choice for writing patterns with features down to a few nanometers in size. Because the pattern is written directly from computer, EBL does not require a pre-existing mask. This enables several important options, including quick turn-around time for trying out new nanoscale patterns, and fabrication of masks for photolithography. The historical Achilles Heel of EBL has been its low throughput. For high-volume manufacturing of VLSI chips, the relevant figure of merit remains the cost per wafer of patterning. Separately, investment in electron beam lithography development remains low. The present study addresses how this equation is evolving, and how this just might alter the prospects of manufacturing going forward.

9049-4, Session 2

Defect reduction and defect stability in IMEC’s 14nm half-pitch chemo-epitaxy DSA flow *(Invited Paper)*

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Directed Self-Assembly (DSA) of Block Co-Polymers (BCP) has become an intense field of study as a potential patterning solution for future generation devices. The most critical challenges that need to be understood and controlled include pattern placement accuracy, achieving low defectivity in DSA patterns and how to make chip designs DSA-friendly. The DSA program at imec includes efforts on these three major topics. Specifically, in this paper the progress in DSA defectivity within the imec program will be discussed.

In previous work defectivity levels of ~560 defects/cm2 were reported and the root causes for these defects were identified. Various causes including particle sources, material interactions and pre-pattern imperfections were revealed. The specific efforts that have been undertaken to reduce defectivity in the line/space chemo-epitaxy DSA flow that is used for the imec defectivity studies will be discussed. In parallel, efforts have been ongoing to enhance the defect inspection capabilities and allow a high capture rate of the small defects. Further requirements for achieving manufacturable defect levels will be determined from this study.

9049-5, Session 2

Pattern replication and pattern transfer using sequential infiltration synthesis in block copolymer patterns for sub-15nm lithography

Yves-Andre Chapuis, HGST (United States); Shisheng Xiong, The Univ. of Chicago (United States); Lei Wan, Jeffery Lille, Kanaiyalal

C. Patel, HGST (United States); Paul F. Nealey, The Univ. of Chicago (United States); Thomas R. Albrecht, Ricardo Ruiz, HGST (United States)

While Directed self-assembly (DSA) of block copolymers (BCPs) continues to make great strides in forming higher quality patterns for data storage or semiconductor applications, high quality pattern transfer below 15nm critical dimension remains one of the main challenges in BCP lithography. Similarly to other lithographic techniques, pattern transfer from BCPs is commonly achieved by subtractive processes (e.g., reactive ion etching using the BCP as a mask) or by additive processes (e.g. plating or lift-off). As dimensions continue to scale towards 10nm features and below, film thickness of the BCP also scales down compromising etch contrast and making it difficult to achieve high quality pattern transfer with the above mentioned conventional techniques.

Recent developments in selective synthesis by infiltrated organometallic precursors into polymers present an attractive alternative to conventional pattern transfer techniques. Lately, Elam and co-workers1 have shown that by using an atomic layer deposition (ALD) system, specific organometallic precursors can be selectively infiltrated into self-assembled BCPs to pattern nanoscopic metal oxides that replicate the patterns formed by the BCPs. This process has been referred to as sequential infiltration synthesis (SIS).

Since the initial work, several groups have made progress using this technique, focusing on different polymers, as well as materials/precursor involved in the infiltration. The understanding of the diffusion and the chemical reaction mechanism between precursors and reactive groups of the polymers have also been investigated as well as the details of the resulting structure. However, few of these studies have focused on the quality of pattern replication and pattern transfer at lithographically relevant dimensions (below 15nm CD) on full wafer scale.

In this presentation, we will discuss the opportunities and challenges for SIS in BCPs for lithographic applications in the context of template fabrication for bit patterned media. We chose the model reaction sequence of trimethylaluminum (TMA) and water as reactant and co-reactant respectively to perform SIS on two distinct BCP systems.

We performed block-selective synthesis in poly(styrene-block-mehtylmethacrylate) (PS-b-PMMA) BCPs to evaluate the selectivity of the AlOx growth in the PMMA domain vs. that on the PS domain. We also used the PS-b-PMMA system to compare the CD uniformity and quality of pattern transfer when using SIS vs conventional etching or lift-off without SIS. We find that the SIS method has the potential to deliver an improved line roughness after pattern transfer albeit with a reduction of CD width. We also find that achieving a high synthesis contrast at smaller dimensions in PS-b-PMMA may require further improvements in the selectivity of the reaction.

Perhaps one of the most appealing advantages of SIS in BCPs is the opportunity to create etch contrast BCPs that lack etch selectivity, which may enable sub-10nm lithography thanks to their higher interaction parameters. To this purpose, we demonstrate block selective synthesis in poly(2-vinylpyridine-block-styrene-block-2-vinylpyridine) (P2VP-b-PS-b-P2VP) triblock copolymers with a full pitch of 22nm and 16nm validating the potential of SIS to enable pattern transfer in BCPs where conventional etching or lift-off techniques are not accessible and at dimensions that are amenable to ~2Tdot/in2 bit patterned media.

9049-6, Session 2

Pattern transfer challenges in >2 Tbpsi bit patterned media template fabrication using PS-b-PDMS

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As a major provider of data storage, the hard disk drive (HDD) industry is adopting magnetic recording technologies crossing 1 terabit/in2 (1 T) quickly now. Bit patterned media (BPM) is deemed as one of the upcoming solutions to ultrahigh density magnetic recording. Lithography-defined physical dimensions of as small as a 19 nm pitch (in a hexagon lattice) is projected to be a potential starting point of BPM in production by 2020 or earlier.

Directed self-assembly (DSA) of block copolymers (BCPs) is currently under intensive development as an effective way, if not the only way, to enable sub-20 nm pitch dense patterning over large area for BPM template fabrication, at several HDD industrial research labs. Recently our group demonstrated up to 2 T BPM templates fabricated by using spherical PS-b-PDMS DSA dot patterns1. A big challenge is how to minimize pattern quality deterioration during pattern transfer from BCP to template materials such as quartz. Due to ever-shrinking functional volume of BCP nanostructures at higher pattern density, pattern transfer is definitely in need of process innovation. As shown in Figure 1 and Table 1, compared to a typical 2 T PS-b-PDMS dot pattern (Figure 1a), a 'modified' BCP dot pattern (Figure 1c) enables better pattern transfer results with improved dot size/spacing uniformity. Besides, pattern transfer challenge of cylindrical PS-b-PDMS DSA line patterns with a pitch of 15 nm, as shown in Figure 2, targeted for rectangular BPM application2, will also be discussed.

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9049-7, Session 2

Computational simulations and parametric studies for DSA process development

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Directed Self-Assembly (DSA) of block copolymers (BCP) and homopolymers (HP) is driven by the competition between intermolecular ("enthalpy") and intramolecular ("entropy") forces and results in a formation of features with pitches in low tens of nanometers. Such patterning capabilities make DSA of BCP and HP a promising candidate for high-volume nano-fabrication, especially in fabrication of integrated circuits at advanced nodes, patterned media for data storage, and emerging applications of metamaterials.

Development of the DSA process for IC fabrication presents many challenges [1], stemming from the fact that the result of DSA is influenced by many process parameters, some of which are difficult to measure and to control. Computational simulations provide an important tool allowing not only to predict accurately the result of the DSA process, but also to study the parameters of DSA result, which otherwise will be difficult or impossible to measure in the experiment.

We start by presenting the further enhancement of the DSA computational simulation tools being developed in GLOBALFOUNDRIES and described originally in [2]. We proceed by showing the results from recently adapted Monte Carlo simulations approach developed by Peters and de Pablo [7] to examine DSA in graphoepitaxial confinement wells. These simulations are employed in parametric studies to understand how chemical and geometric factors influence the phase morphology.

We also present an upgrade to our Self-Consistent Field Theory (SCFT) DSA Solver [2], originally based on SCFT models [4-6]. This upgrade allows DSA simulations of BCP and HP blends.

The results of the simulation studies are presented next. One important aspect of the DSA process design is to ensure that the polymer phase morphology resulting from DSA provides a robust etch mask for subsequent processing. We present the simulation studies of the DSA in graphoepitaxy confinement wells, where the DSA process parameters are varied in order to determine the optimal set of parameters resulting in a robust and etch transferrable phase morphology.

The results of the 3D SCFT simulation studies on the influence of interfacial interactions on CH DSA at the sidewall and bottom of the guiding confinement, are presented next. Simulation results show that independent control of interactions at these interfaces are vital to control and obtain desired DSA morphology, which will significantly impact

processing details on pattern transfer.

While cylinder-forming BCPs are well suited for forming vias or contact holes with nearly circular crossections, modern semiconductor layouts often prefer elliptical structures; HP blend materials have been shown to be compatible with such non-circular structures. The results of the DSA simulations and studies for the DSA process using of a binary blend of homopolymers are also presented here, and compared with the results obtained using simulated BCP systems.

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9049-8, Session 2

Toward electrical testable SOI devices using DSA for fin formation *(Invited Paper)*

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Directed self-assembly (DSA) of block copolymers (BCPs) is an alternative approach to extend optical lithography, which utilizes a topographical or chemical guiding pattern to direct the BCPs into a desired morphology at a pre-determined location while the material properties of the BCPs control the feature size and uniformity of the resulting structures. Such a technique has drawn great attention due to its capability for pattern density multiplication and defect rectification. Recent studies on 193i/High Volume Manufacturing (HVM) compatibility and defectivity of DSA further reinforce its role as a potential candidate for lithography extension rather than merely a lab-scale nanofabrication method. Current applications of interest of DSA in the semiconductor industry range from periodic lines (for fin, gate, or metal layers), periodic holes/posts, to aperiodic holes with various densities (for via or contact layers).[1-3]

Although great progress has been made for several different DSA processes in the past few years, including defectivity analysis and short-loop electrical tests of via-chain,[4-6], a fully integrated device with modern 300mm tool set using DSA in at least one critical layer has not yet been seriously pursued. Mainly because the current DSA processes and materials are mostly designed and tuned for technology nodes with pattern pitch below 30nm. In this work, a first attempt of SOI device fabrication using DSA for fin formation at 42nm-pitch will be presented. The major challenges and learnings, including line-edge/width roughness (LER/LWR) optimization, pattern transfer, and integration scheme, will be discussed. Compared to what was previously reported, [7] the pattern quality, especially the LWR, are greatly improved and is now comparable to the standard Sidewall Image Transfer (SIT, aka self-aligned double patterning) technique. The structural results and preliminary learnings from device fabrication will be illustrated. The extendibility of using DSA for devices with smaller pitches will be discussed as well.

9049-9, Session 3

Closed-loop high-speed 3D thermal probe nanolithography *(Invited Paper)*

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Thermal Scanning Probe Lithography (tSPL) is an AFM based patterning technique, which uses heated tips to locally evaporate organic resists such as molecular glasses [1] or thermally sensitive polymers [2]. Organic resists offer the versatility of the lithography process known from the CMOS environment and simultaneously ensure a highly stable and low wear tip-sample contact due to the soft nature of the resists. Patterning quality is excellent up to a resolution of sub 15 nm [1], at linear speeds of up to 20 mm/s and pixel rates of up to 500 kHz.[3] The patterning depth is proportional to the applied force which allows for the creation of 3-D profiles in a single patterning run.[2]

For reliable patterning at high speed and high resolution an efficient control system is essential. Here I will discuss how we implemented a closed-loop lithography control scheme. We obtain the control signals by reading the topography in the retrace motion of the scan, while writing is performed during the trace motion. We use the acquired data to optimize the position stability in vertical direction, the amplitude and offset of the applied writing force and the applied force during reading. Excellent control of all parameters is important for an accurate reproduction of complex 3D patterns. Here we demonstrate that depth levels are reproduced with an error of less than 1 nm.

These novel patterning capabilities are equally important for a high quality transfer of two-dimensional patterns into the underlying substrate. We utilize an only 3-4 nm thick SiOx hardmask to amplify the 8±0.5 nm deep patterns created by tSPL into a 50 nm thick transfer polymer. The structures in the transfer polymer can be used to create metallic lines by a lift-off process or to further process the pattern into the substrate. Here we demonstrate the fabrication of 27 nm wide lines and trenches 60 nm deep into the Silicon substrate [4]. The line-edge roughness is 2.7 nm (3sigma) at a write-pixel-pitch of 9 nm, which enables high throughput fabrication of high resolution structures. The high quality of the transferred patterns is a direct consequence of the 0.5 nm RMS depth control during writing and the high etch selectivity of the SiOx mask. The demonstrated feature density and line-edge roughness fulfill today's requirements for mask-less lithography for example for the fabrication of EUV-masks.

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9049-10, Session 3

Sub-wavelength printing with displacement Talbot lithography in the deep-UV region

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Displacement Talbot Lithography (DTL) is a new photolithography technique for forming high-resolution periodic patterns using a relatively simple and low-cost system [1]. The resolution available with DTL depends on the wavelength of the light used, similar to conventional projection lithography. The first demonstration of the DTL technique was performed using light in the near-UV which limited the resolution of the printed patterns [1]. Here, we report the first results from the implementation of the technique in the deep-UV region to print higher-resolution structures, including dense line/space patterns with a half-pitch of 100nm.

DTL is a non-contact photolithographic technique in which a periodic pattern is transferred from a mask to a substrate in a manner similar to proximity printing except that the separation between the mask and substrate is varied during the exposure by a distance corresponding to the Talbot distance of the periodic pattern. The technique results in a time-integrated image that has an effectively unlimited depth of focus, thereby enabling periodic patterns to be printed uniformly over large areas. In DTL all of the diffracted orders from the mask contribute to the image; therefore the numerical aperture (NA) of the imaging system using this technique is equal to one (1) and is obtained without any high-cost projection optics. Since in the case of 1-D line–space patterns, the period of the printed pattern using the DTL technique is half of that in the mask, the ultimate resolution available of the technique without immersion is equal to ?/4.

In the experiments we present here, a frequency-quadrupled diode-pumped solid-state laser emitting light at a wavelength of 266nm was used to provide uniform and well- collimated illumination of masks for exposing 4" wafers. Two different masks were used in the demonstration experiments. Firstly, an amplitude mask consisting of etched holes in a Cr film on a fused silica substrate for printing two dimensional patterns; and, secondly, a phase-mask consisting of a patterned silicon nitride film on a fused silica substrate mask for printing linear gratings. Silicon nitride was chosen as the phase-shifter because its high refractive index enables the formation of relatively strong diffraction orders from phase gratings with periods approaching the wavelength. The DTL images were printed onto Si and quartz wafers coated with photoresist and bottom anti-reflection layers. The resulting patterns printed into the photoresist include a 2D array of holes on a hexagonal lattice with a nearest-neighbor-distance of 350nm and a linear grating with a half-pitch of 100nm. From the angles of the diffraction orders produced by the mask, the NA of the imaging light forming the two printed patterns is calculated to be 0.88 and 0.66 respectively, demonstrating the very high NA possible with the DTL technique.

The implementation of the DTL technique at deep-UV wavelengths enables the low-cost manufacture of sub-100nm patterns for applications such as moth-eye type anti-reflective nanostructures, distributed feedback lasers, zeroth-order gratings, wire-grid polarizers and engineered substrates for LEDs, among others.

9049-11, Session 3

Positive and negative-tone mode closed-loop scanning probe lithography on calixarene molecular glass resist

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To continue Moore's law in the future, keeping alive the technological evolution on which our modern society is based, novel nanofabrication technologies act as a "catalyzer" for opening new horizons in nanotechnology and nanoelectronics. Herein, single nanometer manufacturing (SNM) technology, in particular, single nanometer lithography (SNL) [1], including nanometer precise pattern generation, pattern overlay alignment, and measurement, constitutes an essential requirement for beyond CMOS (single-electron and quantum-dot based) device fabrication. Besides high-resolution capability, economic factors like throughput, cost, and reliability of the lithographic method are also important and have to be considered.

In this paper we show the advancement of the previously demonstrated electric current-controlled scanning probe lithography [1-7] towards the dynamic mode mask-less writing of positive (fig. 2-A & 2-C) as well as negative tone features (fig. 2-B & 2-D). In negative tone mode the field emitted electrons are penetrating the molecular glass resist underneath the nanoprobe and leading to breaking bonds within molecules and cross-linking. In consequence, reduced solubility of exposed calixarenes makes them persist after wet development process. In positive tone mode the combination of high, non-uniform electric field, emission current, and controlled atmosphere causes a direct removal of the resist from below the tip apex. In this mode, no development step is required. By choosing appropriate patterning conditions, dynamic switching between positive and negative tone SPL modes is possible (Fig. 2).

Owing to highly promising merits of the SPL, like: (1) Capability of closed-loop lithography, including pre-imaging, overlay alignment, and post-imaging for feature inspection [4]; (2) Capability of sub-5-nm lithographic resolution with sub-nm line edge roughness (LER) [5, 7]; (3) High overlay alignment accuracy close to atomic level [5]; (4) Ease-of-use and relatively low costs of ownership, SPL consists a promising nano-tool for rapid nanoscale prototyping and high resolution nanoimprint lithography (NIL) template fabrication.

However, the main limiting factor for scanning probe technology turns out to be low throughput capability in consequence of serial imaging and patterning processes. The challenge for the lithographic technologies comprises the marriage of down-scaling device-relevant feature size towards single-nanometers with simultaneous increase of throughput capability. Mix-and-match lithographic strategy is a promising path to beat this trade-off paradigm. A proof-of-concept combining high throughput electron beam lithography (EBL) with outstanding capabilities of closed-loop electric current-controlled scanning probe nanolithography (SPL) is demonstrated. For this, a home-developed SPL set-up (Fig. 1) was used, utilizing self-actuating, piezoresistive cantilevers with conductive tips. For mix & match lithography experiments a standard Gaussian beam EBL system operating at 10 keV was applied.

9049-12, Session 3

A frequency multiplication technique based on EUV near-field imaging

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Near-field imaging is a potential solution to break the diffraction limit of conventional lithography. However, applying this imaging technique to 193-nm lithographic process is impossible due to its long wavelength. The 193-nm exposure wavelength with a manageable propagation depth Z (e.g., 10 nm or larger) will result in a Fresnel number small than one.

This corresponds to a far-field diffraction mode that does not provide any resolution benefit. The possibility of 13.5-nm EUV near-field imaging is more promising due to its much shorter wavelength which can bring Fresnel number into the near-field range (larger than one). When the imaging system operates in the Fresnel-approximation regime, there exist several wave peaks/valleys in the near-field region immediately underneath the aperture where the light propagates through. This will enable spatial frequency multiplication by exposing the imaging material with patterned absorbers sitting on top (to absorb EUV light).

In Fig. 1, we show the frequency multiplication process and a typical film stack that is composed of a patterned absorber layer, imaging layer, and hard-mask substrate. The absorber layer (e.g., 50 nm thick TaN) is patterned by standard EUV lithography and followed up with an etch step to shrink line CD (pitch: 60nm, overexposed/trimmed line CD: 10 nm). Subsequently, the wafer is exposed with open-field EUV light. According to the near-field optics, a series of line/space patterns (with a density higher than that of TaN absorber) can be generated and captured by the underlying photosensitive imaging film. Recent research progress made in CVD and inorganic EUV resist can bring this technique to be production worthy.

In this paper, we present a simulation study with results presented as TE/TM waves. Rigorous electromagnetic simulations are performed to investigate the near-field EUV imaging performance and its process capability. Methodologies of the lithographic process design, simulation setup and optical analysis of this disruptive lithography concept are discussed for the potential applications in VLSI manufacturing. We keep the thickness of absorber layer constant, while modifying the imaging layer thickness as well as the material choice of the underlying hard-mask (substrate) layer. An optical index, depth of thickness fluctuation (DOT), is defined to characterize the tolerable variation of the imaging layer thickness. DOT index plays a key role in evaluating the feasibility of this near-field technique. The aerial image is observed through various depths in the photosensitive imaging film.

For this study, we chose hafnium-oxide's (n, k) parameters to approximate the complex refractive index of a polymer based on a HfO2 core. HfO2 based polymer has been used to build stable metal inorganic resists for EUV and DUV lithography. The choice of hard-mask substrate is TaN, amorphous carbon (a typical hard mask material for pattern transfer), or silicon dioxide. Two cases of TE/TM intensities are shown in Fig. 2 for amorphous carbon and TaN substrate. Even though the second layer is self-aligned to the TaN pattern, our simulation shows that varying HfO2 thicknesses can shift the near-field line/space patterns. High sensitivity of the near-field image (profile and amplitude) to the absorber line width, imaging layer thickness and propagation depth is found in both TE and TM illumination modes. Impact of focus and process variations is discussed as well. The near-field patterns are not just limited to 1-D structure. We shall also study the imaging performance of 2D contacts through this process. Despite the attractive prospect of applying this near-field imaging technique to deep-nanoscale semiconductor fabrication, the challenges from its lithography process control are non-trivial.

9049-13, Session 4

Large-area, continuous roll-to-roll (R2R) nanoimprinting with PFPE hybrid molds: A route to high-throughput manufacturing of sensors

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Successful implementation of a high-speed roll-to-roll nanoimprinting technique for continuous manufacturing of electronic devices has been hindered due to lack of simple substrate preparation steps, as well as lack of durable and long lasting molds that can faithfully replicate nanofeatures with high fidelity over hundreds or thousands of imprinting cycles. In this work, we demonstrate large-area high-speed continuous roll-to-roll nanoimprinting of 1D and 2D micron to sub-100 nm features on flexible substrate using perfluoropolyether (PFPE) hybrid molds on a custom designed roll-to-roll nanoimprinter. The efficiency and reliability of the PFPE based mold for the dynamic roll-to-roll patterning process was investigated. The PFPE hybrid mold replicated nanofeatures with high fidelity and maintained superb mold performance in terms of dimensional integrity of the nanofeatures, nearly defect free pattern transfer and exceptional mold recovering capability throughout hundreds of imprinting cycles. The roll-to-roll nanoimprinted substrate was used to suspend multiwall carbon nanotubes applied via a simple roll-to-roll nanocoating process for the fabrication of highly sensitive infrared (IR) and terahertz (THz) sensors. The successful roll-to-roll sensor fabrication process developed in the present work has opened up a new low cost, high volume manufacturing technique for the production of sensors based on 1D nanomaterials.

9049-14, Session 4

High-resolution patterning for flexible electronics via roll-to-roll nanoimprint lithography

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Flexible electronics is a growing technology and currently reaching the market in applications such as displays, smart packaging, organic light-emitting diode (OLED) and organic photovoltaic (OPV). In order to process flexible substrates at high throughput and large area, new patterning techniques are needed. Conventional optical lithography is limited in throughput and requires several alignment steps in order to define multi-layered patterns; hence it remains an expensive industrial process. Imprint lithography is an excellent alternative to optical lithography that can achieve patterning at a wide range of resolutions, from several microns down to a few nanometres. In display devices, imprint lithography can be used to define several layers: micron sized patterns for thin-film transistors (TFT) backplane as well as optical nano-structures frontplane. Moreover a self-aligned approach can be used in order to decrease the number of alignment steps. Imprint lithography is a fully roll-to-roll (R2R) compatible process and enables large area and high throughput fabrication for flexible electronics.

R2R imprint lithography is under development within Holst Centre as a low cost, large area and high throughput patterning method. In order to process flexible substrates and reach high production speed, a R2R UV imprint tool has been built (Fig. 1). Templates up to 300mm wide, consisting of PDMS or flexible Ni shims, can be attached onto the main drum. The two rollers pushes on the drum in order to provide the necessary pressure onto an UV curable resist that has been preliminary wire bar coated on the substrate. While the template is in pressure contact with the coated film, UV flood exposure at 365 nm cures the resist. The R2R imprint equipment can be run at speeds of up to 3m/min depending on the resist used.

The imprint activities within Holst Centre focuses on the development of processes for self-aligned TFTs fabrication on flexible substrates using R2R imprint lithography. Multi-level templates allow patterning of a TFT stack in one imprint step and subsequent etching of the different layers. The first layer, 100nm of molybdenum (Mo) has been successfully patterned with the source and drain (S&D) structures via R2R imprint lithography (Fig. 2 & Fig. 3). Post processing such as residual layer etching and Mo wet etching are done on a sheet-to-sheet basis, but remain fully compatible with R2R processes; and in the future can be implemented on a complete production line. In parallel, sub-micron R2R imprint is also investigated to pattern light management structures, such as anti-reflective layers and light coupling structures over large area. This process aims for patterning of optical layers in flexible OLED display and flexible OLED lighting devices in order to enhance their performances by reducing internal reflection and allowing better top emission coupling. The nano structures such as moth-eyes shown in Fig. 4 can reduce the reflection of the device and are currently being fabricated with our R2R imprint lithography tool.

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9049-15, Session 4

Scalable roll-based nanopatterning using jet and flash imprint lithography

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The ability to pattern materials at the nanoscale can enable a variety of applications ranging from high-density data storage, displays, photonic devices and complementary metal oxide- semiconductor integrated circuits to emerging applications in the biomedical and energy sectors. These applications require varying levels of pattern control, short- and long-range order, and have varying cost tolerances.

Roll-to-roll (R2R) printing or web printing involves the patterning of flexible materials such as plastics or metal foils. The flexible material, or web, is unwound from a core, processed, and then returned to a second core at the end of the sequence. R2R processing is in use today by industry and many R2R processes already exist for etch and deposition. Lithographic processes are also established for micron-scale manufacturing and for applications that only require polymer embossing without any subsequent processing. Recent work has investigated devices requiring metal etching in conjunction with imprint lithography, but again at a micron scale. However, R2R patterning of arbitrary patterns with thin residual layer control (needed for subsequent pattern transfer) at the nanoscale is far more challenging, particularly at a cost structure suited for commodity applications. The challenge is to create a process that is scalable and meets defectivity, throughput, and cost of ownership requirements.

There are additional requirements keeping for the adoption of R2R nanoimprint lithography. One requirement is achieving the lithographic performance required for pattern transfer of nanoscale structures (as opposed to strictly a functional pattern such as an embossed film). Typical lithography metrics such as aspect ratio, minimum critical dimension, pattern complexity dependence, residual layer thickness (RLT), and consumables costs are especially demanding at the scale required for realizing patterned nanostructures over large areas and at high throughput. In additional, a manufacturing infrastructure must be established to support production processes. Large-area nanostructured devices will require master patterns written using high-end lithography (e-beam, 193 immersion) and replication to create large-area daughter imprint templates. Also, processing steps such as descum etching must be implemented over a large area and at a throughput similar to the lithographic process.

The Jet and FlashTM Imprint Lithography (J-FIL™) process uses drop dispensing of UV curable resists to assist high resolution patterning for subsequent dry etch pattern transfer. A drop-on-demand ink-jetting approach is used to reduce material waste and achieve very thin and uniform RLTs by matching the amount of low viscosity resist dispensed to the actual relief images in the imprint template. Following deposition, a controlled pattern fill step is used to fill the relief images. The process takes advantage of the capillary force created between the mask and substrate, and requires no additional pressure during filling, thereby minimizing any distortion or damage to either the mask or substrate.

Wire grid polarizers (WGPs) are already used in digital projectors. The combination of performance and temperature durability makes their use an attractive choice for this market.

Their application to larger displays, including mobile phones, tablets, monitors and TVs has been limited by an inability to scale the WGP to the required areas for these markets. A roll based printing process enables printing over substantially larger areas and therefore addresses the requirements of both performance and cost of ownership. In this paper, we have applied a roll-based nanopatterning tool, the LithoFlexTM 100 (see Figure 1), to fabricate high performance wire grid polarizers. Figure 2 shows the transmission and extinction ratio of both a 65nm and a 50nm half pitch WGP across the visible spectrum. Maximum transmission in TM mode is close to 90% and extinction ratios approach 40,000 at the higher wavelengths.

The next step is to scale the technology and process to address industry requirements for both area and throughput. To do this will require both a new template infrastructure and an imprinting scheme that accommodates substantially greater web widths. We are currently developing a next-generation tool that will enable imprinting across a 350mm web. A photograph of a scaled prototype module is shown in Figure 3a. In addition, we have established a supply of 300mm master templates (see Figure 3b). Finally, initial performance and patterning results of the new tool will also be discussed.

9049-16, Session 4

Enabling large area and high throughput roll-to-roll NIL by novel inkjetable and photo-curable NIL resists

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Nanoimprint lithography (NIL) was established in the mid 90's by S. Chou [1]. The very first approach of NIL, based on the plasticizing effect of macromolecules at elevated temperatures, was extended by a NIL process in which photocurable resists are cross-linked by exposure to light [2]. Both processes are characterized mainly by the use of rigid substrates and mold materials and are defined by a plate-to-plate NIL (P2P-NIL) approach. Recently, industrial interests have shifted alongside to alternative processing technologies which guarantee high throughput as well as patterning of large areas to lower fabrication costs such as the roll-to-roll (R2R) or roll-to-plate (R2P) NIL process. In this way, more versatile applications can be realized with nanopatterns using different substrates like flexible plastics or metal foils.

In the case of thermal NIL a thermoplastic polymer is used. Its imprint behavior is almost defined by the (co)polymer composition. Further material performance can only be controlled to a minor extent by adding additives, e.g. fluorinated additives to lower the release force during mold detachment [3]. Since a photocurable resist formulation is based on liquid and reactive monomer components, the performance of the finally cured and structured layer can be defined more precisely by the selection of the monomers and in addition by the diligent integration of additives. Hence, the NIL approach by light irradiation is more flexible for the high-throughput realization of nano-patterned large areas.

In this contribution we will introduce two novel photocurable NIL resists having the unique feature to be imprintable by very different NIL techniques. The novel photocurable NIL resists can be deposited by e.g. ink-jet dispensing or gravure printing. They can be cured by use of mercury lamps or HB-LED arrays, and can be imprinted batch-wise or by roller type imprint processes onto different substrates, e.g. Si or different plastics like PC or PET. Various mold materials can be applied, e.g. SiO2, Ni or OrmoStamp® [4].

This contribution will highlight the material development of photocurable NIL resists considering the different NIL techniques (P2P and R2R) and the final applications of the imprinted substrates. A special focus will be on the properties of the base formulations with respect to the photocuring behavior reflecting the high-throughput processing potential,

the viscosity adjustment addressing different deposition methods (ink-jet dispensing and gravure printing), the viscosity-temperature dependence, and the final imprint behavior of the photocurable NIL resist. Furthermore, the finally cured materials will be discussed with respect to optical transparency, refracting index, cross hatch tests on different substrates, and surface polarity. Imprinted nanostructures realized by various techniques as batch-wise or R2R-NIL on several substrates will be shown conclusively proofing the broad range of application flexibility of the new photocurable NIL resists. The high speed processing potential of the novel resist materials will be demonstrated by the high structural replication fidelity even at web speeds of 30 m min-1 in a continuous roller process.

9049-17, Session 4

Challenges for pattern formation with sub-100nm residual-layer thickness by roll-to-roll nanoimprint lithography

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Technologies for pattern fabrication on a flexible substrate are being developed for various flexible devices. A patterning technique for a smaller pattern of the order of sub-100 nm will be needed in the near future. Roll-to-roll Nano-Imprint Lithography (RtR-NIL) is a promising candidate for extremely low-cost fabrication of large-area devices in large volumes. A residual layer thickness (RLT) of a pattern transferred by RtR-NIL distributes around several micrometer or above thickness. We tried to thin the RLT below 100 nm and confirmed the controllability of the RLT and its deviation in the patterned sample.

An RtR-NIL apparatus, CMT-400U, developed by Toshiba Machine Co., was used in experiments for verification of thinning the residual layer. It can handle a wider film substrate with a width of 300 mm and control a distance and a pressure between a gravure-roll and a backup-roll. We conducted many experiments with combinations of various parameters, and each thickness of the residual layer was measured. The parameters the pressure and the distance between rolls, the thickness of the resin put on the film substrate, i.e. the first thickness, the concentration of the resin, the viscosity of the resin, and the feeding speed of the PET substrate film. The film mold was used for pattern transfer by RtR-NIL. The diameter of the film mold was 300 mm, and many spots for measuring the RLT were distributed in the mold. Two kinds of the UV-curable resins were used for experiments which have about 30 and 60 mPa.s. of the viscosity, respectively, and they were diluted by 10% or 50% with acetone. Thickness of the RLT was measured with a reflective film thickness monitor.

We checked the controllability of the RLT by above parameters for the conditions of thicker RLT with 4 or 5 micrometers of the first thickness on the PET substrate because the resins can be put stably. The RLTs and their deviation in each sample were analyzed and models explaining them with the above parameters were developed. The RLTs distributed between about 3 and 4 micrometers even the first thickness and the viscosity of the resins when the resin didn't diluted by acetone, and distributed between about 1.5 and 2.5 micrometer at the concentration of 50%. The RLT predicted by the developed model was 1.49 micrometer with the range of about 300 nm. The deviations of the RLT in the samples were distributed about 4% of the RLT in the conditions without dilution. But the deviations were increased up to about 12% when the resin was diluted by 50%, especially the deviation was remarkable when the viscosity of the resin was smaller. RLTs of sub-100 nm were attained when the concentration of the resin was 10%. The smallest RLT was predicted about 90 nm by the model, but the range of the RLT was about 90 nm. In order to decrease the deviation of the RLT, the characteristic of the resin will be improved.

9049-18, Session 5

Directed self-assembly: Where does the line roughness come from? *(Invited Paper)*

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Line roughness is one of the most critical figures when it comes to evaluating the quality of block copolymer patterns for lithographic applications. With block copolymer directed self assembly (DSA) being now a serious lithographic option for storage or semiconductor applications, the issue of line roughness control will become even more relevant. Line roughness in block copolymer DSA has a very different origin than that of conventional e-beam or photo resists due to the self assembled nature of block copolymer patterns and hence should be treated differently.

We explore line roughness of DSA patterns and their corresponding pattern transfer in the context of lamellae-forming poly(styrene-b-methyl methacrylate) block copolymers which is perhaps the most widely studied model system for block copolymers. We estimate line roughness in real and reciprocal space from scanning electron micrographs and track the evolution of line roughness from self assembly to dry developing to pattern transfer.

The smectic layering of block copolymer lamellae in which each molecule shares each half of its volume on each side of the domain interface, together with the mechanical properties of each block, make for interesting correlations between width and edge roughness and across consecutive lines. It is also important to note that block copolymers, on their own, exhibit very short-range translational order. It is through the use of an external chemical or topographic pattern that directed self assembly achieves long range translational order. Because of the deterministic role that the guiding patterns play in the placement of the self assembled lines, we have proposed previously to analyze line roughness in DSA in terms of line placement, line width and line edge roughness as opposed to only width and edge roughness as it is conventionally done. We find that placement, width and edge roughness are not independent and are related through the linear correlation coefficient. Measurements of the evolution of line roughness during removal of the PMMA block by oxygen plasma suggest that placement roughness is mostly determined by the external guiding patterns while the width roughness is strongly determined by the mechanical properties of the polymer and the etching process. We finish by discussing the current status of line roughness in the context of bit patterned media specifications and speculate on areas of opportunity to further reduce line roughness as lithographic dimensions continue to scale down for future technologies.

9049-19, Session 5

Kinetics of defect annihilation in directed self-assembly of block copolymers using chemically nanopatterned surfaces

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Recently, directed self-assembly (DSA) of block copolymers (BCP) has been identified as a potential lithographic technique for future generation

semi-conductor devices. Research in this field performed in a fab environment, with automated processing and electronic-grade materials, was required to evaluate the impact of the boundary conditions on the assembly process. At imec, the implementation of a chemo-epitaxy flow on 300mm wafers to obtain 28nm pitch line/space patterns has focused on defect minimization. Initial work consisted in the fabrication and inspection of fully patterned samples and allowed us to identify the properties of the chemical patterns, such as the chemistry and geometry that resulted in a high degree of order of the BCP domains. However, the determination of the process windows was limited to the analysis of top-down SEM image on small areas. More recently, progress made on the transfer of the poly(styrene) nano-patterns into the silicon substrate, allowed significant improvements during optical inspection the DSA samples. The high capture rate of dislocation defects has led to the thorough identification of the optimal properties of the pre-patterns based on defect density data. Even more, in addition to the study of the role of boundary conditions, the kinetics of the assembly process was also investigated. By varying the BCP annealing time and temperature, it was possible to establish the impact of both parameters in defect annihilation. The progression of DSA-specific defects obtained at different annealing conditions was monitored in terms of defect densities. With this work, the best processing conditions for chemical pre-pattern fabrication and BCP anneal are identified in terms of defectivity. This will allow future optimization of materials and processes for defect annihilation.

9049-20, Session 5

Measurement of the buried structure of sub-30nm block copolymer lithography patterns using resonant x-ray scattering

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The semiconductor industry is pushing the limits of conventional optical lithography. According to the ITRS roadmap, new lithographic methods will be required to economically produce the smaller patterned features of future processing generations. Technologies being evaluated to produce these finer feature sizes include extreme ultraviolet (EUV) lithography, multiple-beam electron beam lithography, multiple exposures, and directed self-assembly (DSA) of block copolymers (BCPs). BCP lithography uses a template to direct the self-assembly of the block copolymer. If the template is an integer multiple of the BCP natural repeat distance, the pattern frequency can be multiplied and result in a much smaller pitch than the original lithography method could obtain.

One of the critical questions remaining for BCP lithography is the buried structure and potential 3D defects not visible with surface characterization methods such as CD-SEM and AFM. We will combine resonant soft x-ray scattering with critical-dimension small-angle x-ray scattering (CD-SAXS) to determine the buried structure of the two blocks, the interfacial roughness, and the pitch uniformity in native BCP films with sub-12 nm features with programmed changes in the template. We found samples that had similar top surface structure often had substantial variations in their buried structure. We also found that lamella on a neutral surface were almost always different from the neighboring lamella on a preferential surface. We will show how these insights into the 3D structure of the block copolymer interface validates computational simulations of the directed self-assembly process of line-space pattern gratings.

9049-21, Session 6

Size and shape control of sub-20nm patterns fabricated using focused electron-beam induced processing

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To make patterns of lateral size smaller than 20 nanometer is quite challenging using resist-based Electron Beam Lithography (EBL), as a result of the straggling of the electron beam in the resist layer during the exposure step and the subsequent development process. This is avoided in Focused Electron Beam Induced Processing (FEBIP) where a monolayer of precursor molecules, adsorbed to the substrate surface, is employed. Electron beam exposure of such a monolayer results in the dissociation of the precursor molecules and the direct deposition of molecule fragments. No development process is required, it is a one-step process. The spatial resolution is determined largely by the electron beam probe size and the secondary electron emission area around the primary beam [1]. Simulations, as well as experiments, have demonstrated that deposits even as small as 1 nm can be made on thin membrane substrates [2] and as small as 3 nm on bulk Si substrates [3] (see figures 1 and 2). The challenges are i) to control the composition of the deposits, ii) to control the shape of the deposits, and iii) to enhance the deposition speed. The first challenge is about preventing unwanted precursor molecule fragments (mostly carbon) to be co-deposited (e.g. by using better precursor molecules), or to remove those fragments afterwards (e.g. by exposure to hydrogen or oxygen radicals). The third challenge is about increasing the inherently low speed of a serial writing process. Solutions can be found in the design of precursor molecules with much larger dissociation cross sections, or in massively parallelizing the writing process [4]. This work focuses on the second challenge, to accurately control the dimensions of FEBIP patterns in the 1-20 nm range. A number of parameters is involved in the deposition process: the electron flux, electron energy, electron exit area of scattered electrons, energy distribution of surface electrons, substrate material, substrate temperature, substrate surface properties, the precursor gas flux, precursor surface diffusion, adsorption/desorption of precursor molecules, electron stimulated desorption, electron induced dissociation cross section, electron beam induced heating, and background pressure (residual gases). Usually many of these parameters are not very well known, or vary between experiments and between labs. The purpose of this work is to characterize the FEBIP process, as it usually done in electron microscopes, in terms of these parameters. And then learn how to control the parameters such that deposits of prescribed size and shape can be fabricated. Results of this work will be presented.

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9049-22, Session 6

The next-generation proton beam writing

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Proton beam writing (PBW) is a direct-writing technique that uses a focused beam of MeV protons to pattern resist material at nano dimensions. In PBW vertical, smooth sidewalls and low edge roughness in thick resists of up to 50 μm can be fabricated with minimal proximity effects.This is significantly better than that can be achieved with electron beam lithography because of the smaller lateral spread of secondary electrons produced by collision between protons and electrons. PBW has been used in many areas like photonics, micro or nano-fluidics, nano imprinting, silicon machining and mask for x-ray lithography.

At the Centre for Ion Beam Applications (CIBA), in the Physics Department of the National University of Singapore, there exist two proton beam writing lines. In the first generation PBW facility, the

proton beam can be focused down to 35?75 nm2. Direct proton beam written sub-100 nm details have been obtained in negative resist like SU-8 and HSQ, featuring 60 nm and 22 nm wide lines respectively. The newly developed second generation PBW beam line has a higher demagnification, which results in a proton beam with a spatial resolution of 12.6 ?29.9 nm2 [1].In the experiments presented here, 10 µm thick PMMA positive resist and 100 nm thick HSQ negative resist (XR-1541, Dow corning) are evaluated. A focused 2 MeV proton beam (with a beam spot size of 50?100 nm2) are used to write parallel lines by exposing the PMMA. After nickel electroplating 72 nm wide lines with 5 µm high featuring an aspect ratio of 69, are obtained (see Fig.1).Next the beam is focused down to 19 nm in X direction and lines are written in HSQ. A line width of 19 nm and a spacing of 60 nm structure is achieved (see Fig. 2). To date this is the smallest structure written by PBW.

As a mask-less technique, PBW has low throughput and is not suitable for mass production. In order to overcome this obstacle, a high aspect rationano-aperture Nimaskis fabricated by PBW and used in masked resist exposures. In this waya 4" area can be exposed in about 1 min, which greatly increases the efficiency.

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9049-23, Session 6

Increased throughput, determined by a suite of benchmark patterns, in a Gaussian electron-beam lithography tool with a 100 MHz writing rate

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In order to meet the requirements for future nodes on the ITRS roadmap, the development and qualification for wafer processing and inspection equipment requires test structures with critical dimensions below 20 nm. This requirement is met with high repeatability and flexibility by Gaussian e-beam lithography.

At the College of Nanoscale Science and Engineering (CNSE) in Albany, the Vistec VB300 e-beam lithography system is routinely used to expose 300mm wafers to meet these nano-patterning requirements. The ever-increasing demand for these test structures highlights the importance of continuous improvement in the throughput performance of e-beam systems. CNSE and Vistec are partners in a continuous throughput improvement program.

In e-beam lithography with a single Gaussian beam, write times are very pattern-dependent. In order to quantify our throughput improvements we defined a suite of benchmark patterns to compare throughput "before and after" the various stages of the throughput improvement program. In the first phase of development, which concentrated on the reduction of overheads, the suite of benchmark patterns showed an average throughput improvement factor of 2.1.

The second stage of this program has been recently implemented on CNSE's VB300. This phase concentrated on hardware, firmware and software changes to enable faster digital data transfer, faster beam deflection and a higher duty cycle of beam switching. The maximum clock speed in the new configuration is 100 MHz, meaning the beam dwell time at each exposure coordinate can be as short as 10 ns. This stepping rate required upgrades to the analogue electronics and cabling, modifications to firmware and software, and careful attention to timing of signal propagation.

The patterns chosen for the benchmark suite represent a range of real-world lithographic challenges. These include the ISMI 13 nm gate intentional defect array (IDA) pattern used for testing metrology tools. Other patterns demonstrate 3D lithography, zone plates, gratings and a range of arrayed small shapes used in applications such as patterned media and DRAM. Real exposure times are recorded for the individual patterns written in order to show the results for each pattern in time per square millimeter. Micrographs of the lithography before and after the upgrade are presented. The challenges of writing at a high clock rate, including selection of appropriate beam current and step size, are discussed.

Patterns are not affected equally by the various throughput improvements. The result of this second phase of the program has shown a net average improvement factor of 4 times over the timings at the start of the continuous improvement program.

9049-24, Session 6

Impact of model inaccuracy on patterning in electron-beam lithography

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Electron beam lithography is a promising technology for next generation lithography. Compared to optical lithography, it has better pattern fidelity and larger process window. However, the proximity effect caused by the electron forward scattering and backscattering in the resist and in the underlying substrate materials has a severe impact on the pattern fidelity when the required critical dimensions (CD) are comparable to the electron beam blur size. Therefore, accurate electron scattering model and proper proximity correction play a vital role in electron beam lithography. In this paper, we describe a 50-kV electron scattering model in terms of multiple Gaussian kernels with an in-house proximity correction scheme to achieve better accuracy and more self-consistency than the double Gaussian kernel. The impact of various Gaussian kernels used in the proximity correction on the lineation of typical patterns is also addressed.

9049-61, Session PS1

Novel Fluorinated Compounds that Improve Durability of Antistick Layer for Quartz Mold

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In recent years, the size of patterns used in nanoimprint lithography (NIL) continues to shrink rapidly. Since nanoimprinting is a form of contact printing, increasing the separation force might damage the master and imprinting tool, as well as degrading the pattern quality. The mold-release characteristics of the master and resin remain a key concern. Although Optool DSX (DAIKIN Ind. Ltd.) is the de facto standard for mold release agents, its durability with regard to UV-NIL is suspect. Our previous solution was a class of material that offers enhanced mold-release characteristics. The new fluorinated copolymers based on ?-chloroacrylate and low molecular weight perfluorocompounds, were intended to be resist additives. We reported the synthesis method, specific properties such as static contact angle, release force and the use of other fluorinated compounds for resin surface treatment in last year. These results showed the possibility that the fluorinated additives was useful as anti-sticking agents. This paper reports the quantitative measure of releasing force about the fluorinated additive, and aimed at the durable improvement of novel anti-sticking agents for quartz mold.

9049-99, Session PS1

A single-nanometer nanoimprint-mask fabrication by EBL followed by NIL and self-aligned double patterning

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A nanoimprint-mask (master-mold) is generally made by EB lithography (EBL) for the ultimate pattern resolution. A polymer EB resist ZEP520A, with a poorer solvent developer such as a fluoro-carbon and alcohol mixture, provides the best resolution with acceptable quality of line width roughness (LWR). However, this resist system requires a significantly high EB exposure dose, typically 875?C/cm2 (@100kV), for hp24nm, while 90?C/cm2 for hp48nm LS patterns. 1/3 shrinkage induces 1/10 productivity very much roughly, as far as we studied.

In the semiconductor industry, by the way, self-aligned spacer double patterning (SADP) technique has been practically employed in high volume manufacturing lines of NAND flash memory devices. And, SADP performance was already demonstrated on 193-i lithography resist and also on EUV lithography resist [2], but not yet in details on EBL resist nor nanoimprint lithography (NIL) resist as a mandrel material.

We then introduced SADP technique on to ZEP520A EB resist line patterns as mandrels to make a nanoimprint-mask (master-mold). SADP technique is used to double (x1/2) a pattern pitch for shrinkage commonly. But, our approach is differently to double (x2) a target pattern pitch instead in the first EBL, and to employ SADP technique to double (x1/2) the pattern pitch back to the target one. And, we tried to prove merits of this method, which could be a significant reduction in exposure dose as well as an improvement in LWR quality.

We also tried nanoimprinting with the EB master-mold made (x2 pattern pitch of the target) to produce NIL resist mandrels to see particularly if further quality improvement of LWR could be obtained in that case. Nanoimprinting provided us LWR improvement between the master-mold to the replica, as far as we experienced. Then, we did nanoimprinting over several times to make replicas to see if further LWR improvement could be seen by the multiple nanoimprinting in order to make NIL resist mandrels with superior LWR quality.

Finally, we tried to make hp20nm patterns on an EB master, followed by NIL to make NIL resist mandrels to improve LWR quality, and lastly followed by SADP to make hp10nm spacer patterns to make a nanoimprint-mask (master-mold).

This paper describes a new patterning scheme and its advantages to make a nanoimprint-mask (master-mold) for a single-nanometer lithography; 1) in which firstly EBL employed as usual but x2 pitch of the target one to make EB resist mandrels, and finally followed by SADP technique (x1/2) back to obtain the target pitch and a single nanometer such as less that hp10nm features, 2) in which firstly EBL employed as usual but x2 pitch of the target one to make a master-mold, and followed by NIL to make NIL resist mandrels with superior LWR quality, and finally followed by SADP technique (x1/2) back to obtain the target pitch and a single nanometer such as less than 10nm features.

9049-101, Session PS1

Fluorine coatings for nanoimprint lithography masks

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A structure and method for an improved Nano Imprint Lithography mask has been designed. The process involves a variety of conformal ALD layering methods as well as sequential monomolecular depositions. The schema describes chemically bonded, high density, smooth coatings having fractional fluorine terminations. Various reactive site surface chemical functionalization schemes are described which allow the attainment of various percentages of controlled F terminations. The percentage of area covered with fluorine terminations is adjustable and controllable from 0% to 100%. Chemistries are described that result in coating layers less than 0.25nm. These coatings may be useful for the reduction and minimization of defects in the advanced imprint lithography processes.

9049-63, Session PS3

Quantum optical lithography from 1nm resolution to pattern transfer on silicon wafer

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Many attempts have been made to break the diffraction limit, a major problem in optical lithography. Here, we report and demonstrate a lithography method, Quantum Optical Lithography [1-3], able to attain 1 nm resolution by optical means using new materials (fluorescent photosensitive glass-ceramics and QMC-5 resist). The performance is several times better than that described for any optical or Electron Beam Lithography (EBL) methods. The written patterns on resist were transferred to Si wafer. In Fig. 1 we present TEM images of 1 nm lines recorded at 9.6 m/s. Multiple 5-10 nm etching lines are shown in Fig.2.

Fig. 1 TEM images of: a) multiple 1 nm lines written in a fluorescent photosensitive glass-ceramics sample;

b) single 1 nm line written in QMC-5 resist .

Fig. 2 SEM images of a written pattern on (100) Si covered by resist: (a) multiple etching lines with minimum width between 5 -10 nm; the resist is partially removed; (b) four parallel etching lines with 5 -10 nm minimum width, between two 20 nm line markers; the resist is completed removed by plasma cleaning; (c) etching lines on a (100) Si sample covered by Au particles; 5.3 nm, 8.5 nm, 11.8 nm and 14.4 nm etching lines were marked; (d) etching lines on a (100) Si sample covered by Au particles and treated by plasma cleaning for 5 minutes ; 3.39 nm and 5.74 nm etching lines were marked.

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9049-64, Session PS3

Circumventing the diffraction barrier in nanopatterning via optical saturable transformations

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The ability to directly write sub-micron features on various substrates with high throughput, accuracy, and uniformity using optical approaches suffers from a fundamental resolution limitation, which arises from the diffractive nature of light [1]. While current approaches to overcome this barrier involve near-field techniques [2], which are typically difficult to parallelize, and far-field techniques [3,4,5] that require high light intensities that also limit parallelizability, we hereby propose and demonstrate patterning via optical saturable transformations (POST).

POST is a new high-throughput, low-cost, novel nanopatterning method that is capable of circumventing the far-field diffraction limit by exploiting the chemistry of novel organic photochromic molecules [6]. This novel nanofabrication technique uniquely combines the ideas of saturating optical transitions such as those used in stimulated emission-depletion (STED) microscopy [7], with interference lithography, which makes it a powerful tool for large-area parallel nanopatterning of deep subwavelength resolution features onto a variety of surfaces with potential extension to 2-dimensions and 3-dimensions.

To demonstrate POST, a diarylethene molecule derivative, namely, 1,2-bis(5,5?-dimethyl-2,2'-bithiophen-yl) perfluorocyclopent-1-ene, (BTE), is used as the recording medium. A thin film of BTE is thermally evaporated onto a substrate, upon irradiation with short-wavelength UV, the open-ring isomer converts to the closed-ring isomer, Fig.1. The basic method of POST uses a standing wave with a focused node at visible wavelength, which converts the molecules back to the open-ring isomer, except in the near-vicinity of the node. By optically saturating this transition, the molecules in the closed-ring isomer remain in a region that is far smaller than the far-field diffraction limit. Then, by a subsequent highly selective "locking" step a pattern is left behind with nanoscale topography. This sequence of steps can be repeated, Fig. 2, with intervening displacements of the sample relative to the optics in a "dot-matrix" fashion to create arbitrary geometries with features spaced much smaller than the far-field diffraction limit [8,9].

The key aspect of our approach is the use of this "locking" step and its distinctive selectivity. In nanopattering, a "locking" step is necessary to fix the sub-wavelength region, and isolate it from further optical processing. One of the "locking" mechanisms developed by our group exploits the selective electrochemical-oxidation of the closed-ring isomer into a stable cation [6,8,9]. Due to the extended ?-conjugation of the closed-ring isomer, this results in the decrease of the oxidation potential of the closed-ring isomer as compared to the open-ring isomer. The oxidized closed-ring isomer is subsequently developed away in a polar solvent leaving behind nanoscale features, Fig. 3. Another "locking" step that is being explored by our group is based on the selective dissolution of the closed-ring isomer. Note that this is advantageous as compared to the electrochemical oxidation "locking" step, as a conducting Pt working electrode is not required.

In this presentation, we will describe our recent experiments to improve the robustness of the POST process and the implications for high-throughput nanopatterning of complex geometries. We will also present simulations that demonstrate the potential of this approach.

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9049-65, Session PS3

Molecular glass resists for scanning probe lithography

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As the semiconductor industry moves to smaller structures and devices, scanning probe lithography (SPL) is emerging as one of the lithographic techniques for the generation of sub-5nm feature sizes. But this challenging technique requires tailored resist materials, which must be sensitive in order to get a high throughput and capable of producing ultimate resolution features. In this context a new promising material class, so-called "molecular glasses", is more and more investigated. In addition, molecular glass materials offer the advantage of solvent-free film preparation by physical vapor deposition (PVD). The PVD prepared films are very uniform and can be produced with a precise thickness in the nanometer range. PVD provides enhanced film forming properties and the prepared films are clean of residual solvent domains, which can affect locally the film properties. Because of the non-chemically amplified resist nature and the absence of corresponding material diffusion, novel SPL resists have the potential to reduce line edge roughness (LER). The patterns are generated directly by the applied SPL patterning technique. Thus the resulting LER should be only influenced by the film quality and the writing tool. To gain sub-5nm pattern SPL must be capable to achieve below 1nm values of line edge roughness.

In this work, we present novel non-chemically amplified molecular glass resist materials of (i) calix[4]resorcinarene resist system, (ii) twisted fully aromatic dicarbazole-biphenyl materials, and (iii) fully aromatic spiro based SPL resists. Their lithographic performance was investigated with respect to stable amorphous film forming of solvent coated and solvent-free PVD prepared films, sensitivity, etch resistance, etch transfer, and LER. Their high resolution patternability was investigated based on producing positive and negative tone images (see Figure) generated by the closed-loop scanning proximal probe lithography (SPL) or the thermal scanning probe lithography (tSPL).

9049-66, Session PS4

REBL DPG lenslet structure: design for charging prevention

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KLA-Tencor is currently developing Reflective Electron Beam Lithography (REBL), targeted as a production worthy multiple electron beam tool for next generation high volume lithography. The Digital Pattern Generator (DPG) integrated with CMOS and MEMS lenslets is a critical part of REBL. Previously, KLA-Tencor reported on progress towards a REBL tool for maskless lithography below the 10 nm technology node. However, the MEMS lenslet structure suffered from charging up during writing, requiring the use of a charge drain coating. Since then, the TSMC multiple e-beam team and the KLA-Tencor REBL team have worked

together to further develop the DPG for direct write lithography. In this paper, we will introduce a hollow-structure MEMS lenslet array that inherently prevents charging during writing.

9049-67, Session PS4

Analysis of mix-and-match litho approach for manufacturing 20nm logic-node products

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Lithographic equipment and process costs increase consistently with the progress of technology nodes. In order to support 86nm CPP (contacted poly pitch) and 32nm half-pitch metals, techniques, such as double-patterning (DP), negative-tone-develop (NTD), and source-mask optimization (SMO), are used in 20nm node. The adoption of these techniques has effectively boosted the litho process windows, however, at the expense of additional litho process and higher wafer-loads to make 20nm product affordable. This situation has prevented many small designers' products going into manufacturing fabs, because their product volumes are too small and cannot afford the huge manufacturing cost. We propose a new litho solution: E-beam lithography (multi e-beam, mask-less lithography) will be used to replace the 193nm immersion processes for critical layers in the process flow. Two distinguish advantages of the e-beam lithography are (1) high resolution, which can resolve 32nm half-pitch without using DP process, and (2) masklesss, which saves the mask costs. In this paper, we analyze the performance capability of multi e-beam lithography and how it matches with optical lithography, such as resolution, CD uniformity, alignment and overlay. Our results suggest that current multi e-beam tool is capable to process 20nm critical layers although mix-and-match overlay still needs to be improved. Proximity correction software that is able to handle full chip design is yet to be developed. Within certain volume, the mix of e-beam and optical lithography (for non-critical layers) is more cost efficient than the regular approach with 193nm immersion.

9049-68, Session PS4

A shape-modification strategy of electron-beam direct writing considering circuit performance in LSI interconnects

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As the feature size of LSI shrinks, the cost of mask manufacturing and the turn-around time continue to increase. Maskless lithography using electron beam direct writing (EBDW) technology attracts attention in recent workshops and conferences on semiconductor lithography. However, compared with conventional photolithography, EBDW throughput is lower because it requires many electron beam (EB) shots for exposure of whole patterns on a wafer. Furthermore, the proximity effect correction (PEC) used for highly accurate EB drawing converts an original layout into complex drawing patterns. It causes even lower drawing throughput. In order to enhance the throughput, we have already proposed a dose-modification strategy considering reliability for TDDB degradation [1]. PEC is performed by shape- and dose-modifications.

In this paper, we try to enhance the EBDW throughput more by considering a shape-modification. Our proposed method simplifies an original layout into EB drawing patterns with rounded corner that have lower interconnect resistance. Figure 1 (a) shows an original metal line (upper) and electrical equivalent mesh network (lower). Figure 1 (b) shows a metal line with rounded corner (upper) and electrical equivalent mesh network (lower). Figure 2 shows simulated current distributions for Figs. 1 (a) and (b). We calculated relative resistance change of the metal line from A to B as a function of the degree of roundness x when the layout is changed from Fig. 1 (a) to Fig. 1 (b). As shown in Figure 3, it was seen that metal lines with rounded corner indicated lower interconnect resistance. Figure 4 shows EB drawing patterns for Fig. 1 (a) and metal line with rounded corners (x=72nm), respectively. The pattern with rounded corner was drawn by less EB shots and achieved EB drawing time reduction of 6.6%. At the conference, we will report evaluation results for microprocessor layouts synthesized with the Nangate 45 nm Open Cell Library.

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9049-71, Session PS5

DSA template optimization for contact layer in 1D standard cell design

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At the 10 nm technology node, the contact layers of integrated circuits (IC) are too dense to be printed by single exposure lithography. Block copolymer directed self-assembly (DSA) has shown its advantage in contact/via patterning with high throughput and low cost. To pattern contacts with DSA process, guiding templates are usually printed first with conventional lithography, e.g., 193 nm immersion lithography (193i) that has a coarser pitch resolution. The guiding templates play the role of controlling the DSA patterns inside, which have a finer resolution than the templates. The DSA contact pitch depends on the chemical property of block copolymer and it can be adjusted within a certain range under strong lateral confinement to deviate from the natural pitch. As a result, different patterns can be obtained through different parameters.

However, DSA patterning must satisfy the overlay accuracy requirements while the guiding templates also need to be printable by conventional lithography. This presents a unique opportunity of DSA patterning and layout design co-optimization for improving the manufacturability of DSA. A previous work [5] focused on standard cell level designs. The authors proposed a MaxSAT formulation to minimize the patterning cost. However, their problem formulation and approach suffer from the following disadvantages:

1. Intra-cell contact redistribution is far from enough to optimize the entire contact layer, since inter-cell connections are not considered.

2. The MaxSAT approach is expensive cannot be well scaled to a full chip layout.

In this work, we consider the following problem formulation. Given a contact layer in 1D design, optimize the layout such that it can be patterned by a given set of DSA guiding templates, and the total cost of the templates are minimized. In particular, the following practical constraints are considered:

1. Vertical constraint. This is the same as the vertical constraint in the classical channel routing problem. If there are two contacts in the same column, there will be a vertical constraint between them. This implies that one metal wire must be above the other.

2. Track constraint. Intra-cell connections are used for PMOS/NMOS connections. Thus, a wire that is connecting PMOS (NMOS) can only utilize the tracks that lie in the N-active (P-active) and the free tracks between N-well and P-well. A wire that is used for inter-cell connections can utilize any routing tracks.

3. Contact constraint. The contacts that are used to connect the polysilicon cannot be placed on the gate regions. This implies the underlying metal wires can only utilize the routing tracks between N-active and P-active.

We propose a simulated annealing (SA) based approach to solve the problem efficiently. The objective is to minimize the total patterning cost. The above constraints are incorporated in the annealing process to generate a valid solution. The proposed solution can optimize the full layout and output a satisfactory solution in a reasonable time.

9049-72, Session PS5

Simulation analysis of directed self-assembly for hole multiplication in guide patterns

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In this report, morphology block copolymer in the guide patterns is analyzed by simulation and compared with experimental results. In the case of the hole multiplication, selection the guide pattern size and the surface affinity of the substrate and the wall is necessary for stable micro structure. To confirm the good comditions, density functional theory simulation is used for 2D analysis because of the high calculation speed. Based on the 2D simulation results, 3D morphology is then confirmed by using dissipative particle dynamics simulation. Finally, these simulation results are compared with the actual experimental results by CD-SEM and STEM.

These simulation approaches will be important to decide the lithography mask design, film stack and pre-treatment conditions for more complex multiplication process, for example, the cut mask application.

9049-73, Session PS5

Self-consistent field theory of directed self-assembly on chemically-prepatterned surfaces

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Directed self-assembly (DSA) has recently attracted attention as a next-generation patterning technique to complement conventional photo-lithography. DSA is a technique in which chemical or physical guidance can be used to direct the self-assembly of materials such as block copolymers (BCPs) and induce defect-free patterns.?Several techniques have been developed for DSA applications. The most promising techniques for industrial implementation are grapho-epitaxy and chemo-epitaxy. The first one utilizes topographic features to control the orientation and the position of the BCPs. The second utilizes the chemical contrast between two different materials at the substrate to control the self-assembly.

In this study, we use self-consistent field theory to investigate the self-assembly of AB diblock copolymers on substrates with varying chemical affinities to each block. Using our simulations, we compute the formation energies of various structures arising in a polymer film. We focus in particular on substrates in which attractive stripes are alternating with neutral ones at different width ratios. An example of our calculations and the resulting morphologies on patterned substrates with different stripe attractive to neutral width ratios, SA, is shown in Fig.1. In this example, we consider a lamella-forming block copolymer with an A-block fraction, f = 0.5, a segregation strength, ?N = 25, a bulk lamellar width, l0 = 4.2 Rg and a radius of gyration of the unperturbed chain, Rg ? 7.2 nm. The height of the film is fixed at 6 Rg while both the length and the width are set to 24 Rg. In the presence of fully neutral substrates (SA = 0), the block copolymer forms defective (perpendicular) lamellar patterns without directional guidance. On the other hand, BCPs on predominantly A-attractive substrates (SA = 0.75 and 1.0) produced lying-down (parallel) lamellae. For SA=0.25, our target of directionally guided, near-perfect perpendicular lamellae are obtained. In the present circumstances, when SA = 0.25, the width of each A-favorable stripe is 2 Rg, very close to l0/2, which explains why perpendicular lamellae form when SA = 0.25. With increasing stripe width ratios of SA=0.40 and 0.50, defect-free, perpendicular lamellae could not be observed using simulations run from random seeds.

Our findings suggest that the formation of perfectly guided perpendicular lamellae requires attractive stripes of width close to half the natural period of the diblock copolymer.

9049-75, Session PS5

Toward fast DSA models: improvement of computational performance of DSA simulations

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Use of directed self-assembly (DSA) of annealing block copolymers (BCP) or homopolymers (HP) in the fabrication of integrated circuits (IC) requires computational DSA models [1-3] capable of predicting the DSA result for large areas on the wafer, ideally for the full chip.

In the case of DSA processes used to fabricate the IC patterns substantially deviating from the limited set of natural DSA morphologies, chemoepitaxy pre-patterns or graphoepitaxy confinement wells are used to provide a coarser scale “direction” modifying these natural morphologies. The intermolecular and intramolecular forces acting between and within the BCP molecules also provide a mechanism ensuring self-assembly of features at a smaller scale and at a smaller pitch, compared to the scale and the pitch of the directing patterns. To determine an optimal geometry of the directing patterns, a solution of the inverse DSA problem, or DSA PC problem [4-5] is needed. The algorithms solving such inverse problems for the whole chip will need to use the fast models for the lithographical processes used to fabricate the directing patterns (e.g. models used for OPC in optical lithography), along with the fast models for the DSA process. Similarly to the OPC algorithms, such algorithms combining OPC and DSA PC [4,5] will need to be run iteratively. Currently used rigorous DSA simulation algorithms are expected to be a performance bottleneck in such iterative algorithms combining OPC and DSA PC.

In this paper, we concentrate on the ways to improve the performance of the DSA computational models. We start by reviewing the computational complexity of a rigorous self-consistent field theory (SCFT) DSA model [1] and also the currently utilized ways to reduce this computational complexity and improve its performance [1,2], as implemented in GLOBALFOUNDRIES DSA Solver [3,4]. We proceed with presenting new approximations in the SCFT model making it possible to improve the computational performance of the DSA model further. We present the results of benchmarks demonstrating both the accuracy and performance improvements in the new fast DSA models.

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9049-76, Session PS5

New neutral layer material for directed self-assembly (DSA) patterning

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Directed self-assembly (DSA) of block co-polymers (BCP) is one of the promising advanced technologies for sub-20nm half pitch node device manufacturing, and still its commercial application has been issued by some significant remaining hurdles such as environmental controllability around each BCP molecules. We studied the self-assembly process of the block copolymer film spin-coated on different random brushes obtained by varying several parameters such as the random brush ratio, and the annealing time and temperature. There are two types of under layer material related to BCP patterning, brush type and cross-linking type under layer. We will discuss about our new approaches to develop new neutral layer materials by new synthetic and formulating methods.

9049-77, Session PS5

Self-assembly of Si-containing block copolymers with high-segregation strength: toward sub-10nm features in directed self-assembly

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Perfectly ordered microstructures with nanometrically defined periodicity offer promising opportunities in microelectronic applications and nanotechnologies for the production of advanced CMOS digital logic circuits wherein the pitch reduction and the component density increase are two of the main challenges. To produce long-range ordered two-dimensional arrays inherent to such technologies, the combination of the “bottom-up” self-assembly with “top-down” guiding patterned templates has been successfully introduced (1) leading to new technological breakthroughs wherein self-assembling materials (and particularly block copolymers) are the cornerstone of the “bottom-up” nanofabrication processes through their self-assembly in periodic mesostructures. Among the materials used in the direct self-assembly methodology, poly(styrene-b-methylmethacrylate) systems have reached an unprecedented level of maturity which will lead to their introduction into current technological nodes.(2,3) However, this system suffers from deficiencies such as a low Flory Huggins parameter (?=0.04 at 25°C) and a low chemical contrast as regards to the etching processes which are problematic for targeting sub-22 nm features.

Consequently we have developed a new system based on polylactide-b-polydimethylsiloxane-b-polylactide ABA block copolymers (PLA-b-PDMS-b-PLA) which are characterized by a high segregation strength (?=1.4 at 25°C) as well as a strong chemical etching contrast. In this contribution, we focus on a PLA-b-PDMS-b-PLA triblock copolymer with a low molecular weight which shows a hexagonally packed cylinder morphology in the bulk with a periodicity L0 = 15 nm. We demonstrate the control of the mesostructure and its orientation in the thin film configuration through the use of polymeric brushes consisting of polystyrene-stat-polymethylmethacrylate (PS-stat-PMMA). Indeed, by using an appropriated composition of the PS-stat-PMMA brush, it is possible to control the surface interactions between the substrate and the PLA and PDMS domains in order to obtain cylinders oriented perpendicularly to the substrate upon a simple thermal annealing (see Figure 1). This process flow is highly similar to the one used for the PS/PMMA system which renders it very attractive from an integration point of view. Characterization of the self-assembly both by AFM and GISAXS measurements have confirmed the perpendicular orientation of the cylinders through the whole film thickness which allow us to envision the use of this system as lithographic mask. Besides a preliminary study of the integration of this block copolymer with directed self-assembly methodologies such as graphoepitaxy was performed and we show that such materials could be efficiently used to reduce the size of the features beyond the capabilities offered by the PS-b-PMMA system.

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9049-78, Session PS5

Process optimization for directed self-assembly lithography using dissipative particle dynamics and self-consistent field theory

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Directed self-assembly (DSA) lithography, which combines self-assembling materials and lithographically defined pre-patterns, is a potential candidate to extend optical/EUV lithography beyond sub-10nm. Taking full advantage of DSA lithography requires maximizing DSA lithography process windows (PWs) by carefully designing lithographically defined pre-patterns and precisely adjusting process conditions. A number of process conditions should be taken into consideration for optimization through simulations capable of successfully replicating DSA lithography experiments. Recently many simulation studies to evaluate DSA lithography PW have been reported, such as self-consistent field theory (SCFT) [1, 2], dissipative particle dynamics (DPD) [3-5], Monte-Carlo theory (MC) [6], approximated mean field theory [7]. These simulation methods are reported to achieve good agreement with the DSA lithography experiments.

In this work, we have investigated optimal process conditions for Line/Space patterning using two simulation methods, DPD and SCFT. By properly utilizing two different simulators which cover different length/time-scale, we can understand DSA mechanism in more detail and improve the simulation accuracy. The optimization was carried out by comprehensively evaluating CD uniformity (CDU), line edge roughness (LER), placement error, and the DSA specific defects. Optimization knobs are (1) chemo-epitaxy/grapho-epitaxy, (2) material design (cylinder/lamella, polydispersity, additive), (3) film thickness, (4) pre-pattern geography , (5) annealing conditions, (6) pre-pattern’s chemical properties. We will also compare simulations with wafer experimental results and discuss optimal process conditions systematically.

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9049-79, Session PS5

Computational studies of shape rectification in directed self-assembly

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The development of new patterning tools is increasingly essential to progress in nanofabrication due to rapidly-approaching scaling limits of conventional optical lithography. The directed self-assembly (DSA) of block copolymers stands out as one candidate for next-generation lithography techniques. The benefit of graphoepitaxial DSA for Vertical Interconnect Access (VIA) type features is not only in shrinking the guiding hole but also in improving both critical dimension (CD) uniformity and shape rectification. In this talk, we reveal our recent studies on shape rectification in hole-shrink problems. We use self-consistent field theory (SCFT) to investigate the various morphologies inside the prepattern, as well as to compute their formation energy and their dimensions. Furthermore, we use the string method to compute the transition pathways and the barrier heights for the melting of defects into perfect structures.

To relate our findings to experiments, we consider poly(styrene-b-methylmethacrylate) (PS-b-PMMA) diblock copolymers confined in staggered and overlapped non-cylindrical guiding patterns [Fig.1]. Our goal is to show how DSA can rectify non-uniformities in confinement conditions and reduce variations in the center-to-center distance of VIAs. In Fig. 1, the prepattern major CD, minor CD and height for the rounded confinements are ~90nm, ~60nm and ~85nm, respectively, whereas the center-to-center distance along the x- and y-axes is ~30nm and ~60nm, respectively.

An example of the morphologies resulting from 3D SCFT simulations is shown in Fig. 2. We find that DSA not only leads to features with a reduced CD relative to the prepattern, but also rectifies the non-regular shape of the prepattern. As can be seen in Fig. 2, two stand-alone PMMA domains with oval-like shapes form inside the guiding prepattern. In addition, all other observed defective morphologies have a formation energy cost of a few tens of kT, translating to defect densities below the ITRS requirements. The barrier height for the melting of the defects and the corresponding annealing conditions will also be discussed.

9049-80, Session PS5

Dry development of high-chi block copolymers for directed self-assembly

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Directed self-assembly (DSA) is one of the promising candidates for next generation lithography. It is an alternative bottom-up patterning approach utilized both for hole patterns [1], [2] and line/space patterns [3]-[5]. By controlling micro-phase separation of block copolymers (BCPs) by using lithographically defined pre-patterns, viability of 193 nm or EUV lithography approaches to sub-20 nm patterning. The nanofabrication is further extended to sub-10 nm features using high chi block copolymers, where chi is the Flory-Huggins interaction parameter. In order to use micro-phase separated BCP as a mask for pattern transfer to under-layer, one segment of BCP needs to be removed prior to the pattern transfer. Dry development is a unique technique of removing one segment of BCP using reactive ion etching (RIE), although higher RIE selectivity is required for smaller features. Si containing BCPs with high chi parameter were used in this work because they have an advantage in etching selectivity. In order to achieve RIE selectivity enough for pattern transfer of sub-10 nm features, high chi BCPs need to be used along with appropriate process conditions.

In this work, we investigated process conditions of dry development, in particular, how the RIE selectivity changes by gas chemistry, RF power, pressure and etc. Latest status of sub-10 nm patterning is also presented.

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9049-81, Session PS5

300mm pilot line DSA contact hole process stability

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Directed Self-Assembly (DSA) is today a credible alternative lithographic technology for semiconductor industry [1]. In the coming years, DSA integration could be a standard complementary step with other lithographic techniques (193nm immersion, e-beam, extreme ultraviolet). Its main advantages are a high pattern resolution (down to 5nm), a capability to decrease an initial pattern edge roughness [2], an absorption of pattern guide size variation, no requirement of a high-resolution mask and can use standard fab-equipment (tracks and etch tools). The potential of DSA must next be confirmed viable for volume manufacturing. Developments are necessary to transfer this technology on 300mm wafers in order to demonstrate semiconductor fab-compatibility [3-7]. The challenges concern especially the stability, both uniformity and defectivity, of the entire process, including tools and Blok Co-Polymer (BCP) materials.

To investigate the DSA process stability, a 300mm pilot line with DSA dedicated track (SOKUDO DUO) is used at CEA-Leti. The SOKUDO DUO track allows copolymer coatings, bakes and specific wet treatments. Copolymer coatings are achieved by automatic dispense from plumbed gallon bottle. Bakes can be completed up to 350°C under nitrogen to avoid copolymer oxidation. Acetic acid wet treatment is used for selective removal of one phase of BCP. Copolymer materials are synthetized and formulated in large scale by Arkema in semicontinuous industrial process. Both block copolymers and random copolymers used are based on a PS-PMMA chemistry. Morphologies with PMMA cylinders in a PS matrix are investigated (about 36nm natural period). Different methods to remove PMMA domains will be benchmarked: dry etch only, wet develop only and pre-exposure step before wet develop.

BCP self-assembly in free surface or graphoepitaxy (Figure 1) configurations are considered in this study. Free surface configuration

will initially be used for process optimization (thermal budgets, copolymer consumption and recipe steps time reduction) and fix a process of record. Secondly, this process of record will be monitored with a Statistical Process Control (SPC) in order to validate its stability. Various parameters such as copolymer thicknesses, BCP period and PMMA cylinder diameter will be checked at different steps of the process over time (Figure 2 and 3). The results and measurement methodology of these parameters will be discussed. Steps optimization will be applied to graphoepitaxy process for contact hole patterning application. A process window for absorption of guide size variation will be defined. Process stability (CD uniformity and defectivity related to BCP lithography) will be investigated through SPC. Correlation between BCP lithography and BCP pattern etching (size and circularity control) will be addressed in another paper (reference paper P. Pimenta Barros).

9049-83, Session PS5

Streamlined etch integration with a unique hardmask neutral layer (HM NL) for self-assembled block copolymers (BCPs)

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A multifunctional hardmask neutral layer (HM NL) was developed to improve etch resistance capabilities, enhance reflectance control, and match the surface energy properties required for polystyrene (PS) block co-polymers (BCPs, such as PS-b-PMMA). This neutral layer minimizes the number of substrate deposition steps required in graphoepitaxy directed self-assembly (DSA) process flows. A separate brush layer is replaced by incorporating neutral layer properties into our hardmask to achieve microphase separation of the BCP during thermal annealing. The reflection control and etch resistance capabilities are inherent in the chemical composition, thus eliminating the need for separate thin film layers to address absorbance and etch criteria. We initially demonstrated successful implementation of the HM NL using conventional PS-b-PMMA. A series of BCP formulations were synthesized with Lo values ranging from 28 nm to 18 nm to test the versatility of the HM NL. Quality “fingerprint” patterns or microphase separation using a 230°-250°C anneal for 3-5 minutes was achieved for an array of modified BCP materials. The HM NL exhibits water contact angles of 78°-80° and polarities in the 5-6 dyne/cm ranges. The scope of BCP platform compositions evaluated contains a 20° water contact angle variance and 10 dyne/cm fluctuations in polarities. All BCP formulations were coated directly onto the HM NL followed by thermal anneal processing and SEM analysis for effective “fingerprint” patterns. We offer a simplified alternative path for high etch resistance in a graphoepitaxy DSA flow employing a single-layer hardmask for etch resistance demonstrated to be compatible with diverse BCP-modified chemical formulations.

9049-84, Session PS5

Control of PS-b-PMMA directed self-assembly registration by laser-induced millisecond thermal annealing

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Directed self-assembly (DSA) of block copolymers has emerged as a likely candidate for bottom up lithography to enable patterning at dimensions below 20 nm. The PS-b-PMMA system has been extensively explored and has demonstrated the ability to register patterns to both chemical and physical features during thermal annealing at temperatures near 250oC in the minutes time frame. Challenges remain however with regard to defects, registered domain sizes, and line width roughness (LWR). While annealing for much longer periods improves patterning characteristics, throughput concerns mount and polymer degradation limits use of higher temperatures.

We have previously demonstrated the ability to extend polymer processing to substantially higher temperatures by limiting anneals to sub-millisecond and millisecond time frames. In this work, we utilize a scanned laser spike annealing system (LSA) to develop and register PS-b-PMMA DSA patterns at peak temperatures of 300-600°C for 10 ms. The high mobility of the polymer chains at these temperatures enhances registration over large lateral length scales resulting in larger domains of aligned structures compared to conventional thermal anneals.

PS-b-PMMA films 75 nm thick were cast on patterned substrates with a copolymer neutral layer. Molecular weights correspond to 15 nm line/space with a 3X multiplication. Samples were annealed using a 980 nm diode laser focused to a line beam (1.6 mm x 400 ?m) at temperatures up to 600oC and for dwells between 1 and 20 ms. Decomposition of the PS-b-PMMA film was observed to begin at 650oC (10 ms) but did not fully decompose until temperatures exceeded 1000oC. For comparison, samples were also annealed on a hot-plate in air at 250oC for 2-10 minutes.

SEM images of the DSA pattern were compared between 10 minute thermal anneal and multi-pass laser annealing at ~450oC. Both conditions result in features well-aligned to the underlying template over micron length scales. However, the domain size after laser annealing is significantly improved compared to hot plate conditions. In addition, defects are more often localized resulting in decreased area fraction of faulted material. Alignment increases with both annealing temperature and the number of laser scans.

Thermal quench from high temperatures enables the small structure directing forces of the template to align blocks over large dimensions. Further control of the temperature and time characteristics may allow low-temperature refinement of structures following the initial alignment at high temperature. In addition, systems beyond PS-b-PMMA can be considered given the extended temperatures possible with laser processing.

9049-85, Session PS5

Improvement in electron-beam lithography throughput by exploiting relaxed patterning fidelity requirements with directed self-assembly

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Line edge roughness (LER) influencing the electrical performance of circuit components is a key challenge for electron-beam lithography (EBL) due to the continuous scaling of technology feature sizes. Controlling LER within an acceptable tolerance that satisfies International Technology Roadmap for Semiconductors requirements while achieving high throughput becomes a challenging issue. Although lower dosage and more-sensitive resist can be used to improve throughput, they would result in serious LER-related problems due to increase relative fluctuation in the incident positions of electrons. Directed self-assembly (DSA) is a promising technique to relax LER-related pattern fidelity (PF) requirements due to its self-healing ability, which may benefit throughput. To quantify the potential of throughput improvement in EBL by introducing DSA for post healing, rigorous numerical methods are proposed to simultaneously maximize throughput by adjusting writing parameters of EBL systems subject to relaxed LER-related PF requirements. The patterning simulation employs a fast, continuous model for parameter sweeping and a hybrid model for more accurate patterning prediction. The tradeoff between throughput and DSA self-healing ability is investigated by this method. Preliminary results indicate that significant throughput improvements are achievable at certain process conditions.

9049-86, Session PS5

Inspection of directed self-assembly defects

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Directed Self-Assembly (DSA) is considered as a potential patterning solution for future generation devices. One of the most critical challenges for translating DSA into high volume manufacturing is to achieve low defect density in DSA patterning process. The defect inspection capability is obviously fundamental to defect reduction in any process, more so with DSA process. While the challenges of other candidates of new generation lithography are relatively known, such as smaller size, increasing noise level due to LER etc, the DSA process causes certain unique defects that are planar, defect size same as post pitch multiplication resolution. These defects, termed as dislocation and disclination have very little material contrast. While large clusters of these unique defects are easy to detect, single dislocation and disclination defects offer considerable challenge.

In this investigation, defects unique to directed self assembly, such as single dislocations and disclinations are studied using a Rigorous Coupled Wave Analysis (RCWA) method for solving Maxwell's equations to determine the capability for optical inspection systems to capture these defects of interest over the system and wafer noise. Controllable sensitivity factors include various illumination and collection apertures, noise filtering, focus, pixel size, and signal processing. From the simulation, the optimum optical conditions are determined for the best inspection signal pre and post etch for multiple film thicknesses. The study is also extended to investigate wafer-level data at pre and post etch inspection.

9049-87, Session PS5

Understanding defects in DSA: Calculation of free energies of block copolymer DSA systems via thermodynamic integration of a mesoscale block-copolymer model

Andrew J. Peters, Richard A. Lawson, Peter J. Ludovice, Clifford L. Henderson, Georgia Institute of Technology (United States)

Directed self-assembly (DSA) of block copolymers (BCPs) is a promising technique for producing sub-30 nm pitch regular patterns, and the development of these DSA techniques could benefit greatly from computer simulation of such methods. Unlike other models, molecular dynamics (MD) combined with realistic potentials for polymer behavior can potentially provide more accurate simulations of the inherent polymer behavior, dynamics, and equilibrium states without a need to guess modes of molecular movement and without oversimplifying interatomic interactions.

Through the use of thermodynamic integration, this model allows calculation of free energy differences between various states, provided a reversible path can be envisioned between them. Using this technique, various equilibrium and metastable states can be compared. Defect free energies and subsequently defect densities can be calculated as functions of polymer and underlayer properties. Defectivity is one of the primary hurdles for implementation of BCP-DSA into semiconductor fabrication and defect free energies are critical to guide defectivity reduction techniques and patterning techniques. Free energy maps as a function of system properties like pitch, and polymer parameters can also be calculated. These calculations can provide insight into ideal and practical best case scenarios for both polymer properties and system guiding properties, whereas vast number of experiments would have to be run to achieve the same conclusions.

9049-88, Session PS5

Using chemoepitaxial directed self-assembly for repair and frequency multiplication of EUVL contact-hole patterns

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The patterning potential of block copolymer materials via various directed self-assembly (DSA) schemes has been demonstrated for over a decade. At cost-effective low printing doses, EUVL suffers from shot noise effects while patterning sub 30 nm contact hole dimensions. As the CD of DSA systems is largely determined by polymer dimensions, it is theoretically expected that the local CD uniformity of EUVL pre-patterns can be improved by the DSA of pitch matched block co-polymers. In this work we demonstrate continued improvements, including pattern transfer results, on our previously reported chemo-epitaxy DSA integration flow. Also, we achieve dense arrays of contact holes via 1:3 and 1:4 frequency multiplication of EUVL patterned contact hole arrays.

9049-89, Session PS5

Effects of surface characteristics of geometrically confined prepatterns on contact-hole patterning using directed self-assembly lithography

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Due to the resolution limit for conventional optical lithography, several types of next generation lithography have been investigated for the 2xnm node and beyond. Among them, directed self-assembly lithograph (DSAL) has recently attracted much attention for use as sub-20nm contact hole patterning. Even though these patterning performance surpass that of optical lithography, lithographically defined prepatterns are required to control the placement and to improve uniformity of the self-assembly patterns at desired area. Therefore, the challenge is how to optimize design layout and surface affinity of prepatterns while retaining its resolution advantage. This paper presents our investigated correlation between surface characteristics of prepatterns and critical dimension uniformity of contact hole patterning applicable to memory devices.

9049-90, Session PS5

Creation of chemical guiding patterns for directed self-assembly of block co-polymers by AFM lithography

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Directed self assembly (DSA) of block co-polymer (BCP) allows to complement the fabrication methods of nanometer-scale patterns at high resolution and with a throughput and defectivity level compatible with the future requirements of the nano-electronics industry [1]. It is based on directing the alignment of the co-polymer blocks by creating guiding patterns on the surface. The guiding patterns can be either of topographic (grapho-epitaxy) or chemical (chemo-epitaxy) nature. In this work, we present our advances in fabricating chemical guiding patterns by atomic force microscopy (AFM) nanolithography. The main advantages of AFM nanolithography are (i) the higher resolution and control in the definition of the guiding patterns and (ii) the simplification of the overall process.

The interaction of the BCP with the substrate surface dictates the capability for a correct segregation of the two phases of the BCP and the performance of the guiding patterns for alignment. A surface that presents an equal interaction energy with the two blocks of the BCP is necessary for an optimal segregation. When an area of the surface is chemically modified to present larger affinity with one block of the BCP, the blocks can be forced to be aligned in a convenient way. An approach to create guiding patterns consists on covering the surface with a neutral brush polymer layer, that it is selectively chemically modified by performing a lithography step using EBL [2] or DUV lithography [3], followed by a plasma process to change the chemistry on the patterned areas. By using AFM lithography, the chemical patterns are directly created on the brush layer, reducing the number of processing steps [4,5].

We have performed a detailed study on the optimal conditions for the formation of the brush layer, including its characterization by XPS. We show that AFM lithography can create functional guiding patterns at very high resolution. The AFM tip is scanned in non-contact mode over the brush surface while applying a voltage between tip and substrate. This action produces the chemical modification of the surface. The line width resolution is limited by the size of the water meniscus. In order to improve it, relative humidity is kept low during the experiments. We show an example of a pattern formed by an array of lines of 16 nm linewidth. The line separation is equal to integer multiples of the di-block co-polymer period, what allows to achieve density multiplication by a factor of 6. We will discuss possibilities for the applicability of AFM lithography in DSA of BCP in view of instrumental developments in the framework of the European Initiative SNM.

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9049-91, Session PS5

Scanner effects on directed self-assembly patterning

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Continuing demand for printing of ever-smaller feature sizes coupled with delays of EUV lithography have highlighted the possible use of directed self-assembly (DSA) of various polymers as a next-generation lithography component. The combination of DSA materials with extended ArF immersion lithography seems at first glance to be a natural partnership. Lithographers can use an ArF scanner to print guide structures with pitches accessible with current technology. The DSA materials, in a non-exposure step, fill in the gaps between guide structures and self-organize into regular structures smaller than the guide. For line/space patterns, pitch multiplication of 3? or 4? is feasible, and guided formation of small contact holes and 2-D structures has been demonstrated.

Because functioning chip patterns will have very stringent defectivity requirements, considerable research is being done to understand the defect level in DSA feature formation. Some investigators have deliberately introduced patterning errors into the guide patterns and observed the reaction of the DSA patterns. Several groups have built DSA patterns using a full focus-exposure matrix of the guide patterns. Some have made initial conclusions about the effects of, for example, sidewall angle of guide patterns in graphoepitaxial DSA schemes.

So far, the requirements for the guide patterns appear to be within capability of modern 193nm immersion scanners. The scanner effects have not, though, been investigated in detail. While modern scanners print with amazing fidelity, they do exhibit printing errors like CD non-uniformity and overlay errors. We need to know whether DSA pattern formation will place any special requirements on the scanner. For instance, guide lines formed in a double-patterning process will exhibit a CD uniformity effect linked to overlay between the two prints. Will an overlay error of, say, 2 nm be enough, or is the DSA pattern too sensitive?

We are able to evaluate expected CD, overlay, and other errors in the scanner from known modeling techniques, and therefore predict printing of DSA guide patterns. Then we send that guide pattern prediction to a DSA model to evaluate predicted DSA performance. This work uses DSA models available within the industry, coupled with modeling of scanner performance, to predict and analyze the size and severity of DSA errors caused by scanner errors. We use this to assess the current state of ArF immersion scanners for DSA complementary lithography.

9049-92, Session PS5

DSA-Aware Detailed Routing for Via Layer Optimization

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In detailed routing for integrated circuit (IC) designs, vias are usually randomly inserted in order to connect between different routing layers. In the 10 nm technology node and beyond, the wire pitch is below 48 nm, and consequently, the vias become very dense, bringing via layer printing a challenging problem. Recently block copolymer directed self-assembly (DSA) technology has demonstrated great advantages in via layer patterning using guiding templates. To pattern vias with DSA process, guiding templates are usually printed first with conventional lithography, e.g. 193 nm immersion lithography (193i) that has a coarser pitch resolution. Then the guiding templates will determine the DSA patterns (i.e. vias) inside and these patterns have a finer resolution than the templates. Usually regular shaped guiding templates are preferred in order for better overlay control. However, randomly distributed vias may result in very irregular shaped templates where overlay accuracy is a big problem. If a group of closely positioned vias guided by a single template has overlay variation larger than the threshold value, we call them a DSA hot spot. A full chip via layer may have billions of vias, which may result in thousands of hot spots. Therefore, an automatic hot spot fixing strategy that has low impact on circuit performance is greatly in need.

Targeting this problem, we propose a via layer hot spot cleaning algorithm based on multilayer local rerouting. For each isolated hot spot, we first clip a window centered at the hot spot location. If a group of hot spots are very close to each other, a larger window will be clipped to cover all of them together. Next, for every wire passing through this window, we fix their locations on the window boundaries and reroute them inside the window to redistribute the vias. Due to the limited window size, in each clipping window, we formulate the local rerouting problem as an ILP problem and solve it optimally. Note that the wire locations at window boundaries are kept unchanged. Consequently, as long as the wires are successfully rerouted inside the window, the logic connections of the entire design remain valid after hot spot cleaning. If local rerouting fails to remove all hot spots, we gradually expand the window by a certain step size and repeat local rerouting in the expanded window. The step size and maximum window size can both be tuned up as trade-off between the success rate of hot spot cleaning and the running time.

9049-93, Session PS5

Pattern density multiplication using block copolymer directed self-assembly via chemoepitaxy without traditional pinning stripes

Benjamin Nation, Andrew J. Peters, Richard A. Lawson, Peter J. Ludovice, Clifford L. Henderson, Georgia Institute of Technology (United States)

Chemoepitaxy is often used to induce pattern density multiplication in the directed self-assembly (DSA) of block copolymers (BCPs) by using a chemically patterned guiding underlayer. This underlayer is often viewed as being composed of a pinning stripe or region (i.e. the term “stripe” is appropriate for lamellae forming block copolymers while “region” is more appropriate for cylinder forming materials) and a neutral stripe or region. In such cases, the pinning region is made of a material that is energetically favorable and thus highly preferential in its interaction with one phase of the BCP while the neutral region is a material that is neutral to both phases of the BCP. Nominally, the pinning region is used to fix the location of one phase of the block copolymer, thus allowing for registration of a pattern to the underlying substrate and promoting long rage order in the block copolymer thin film patterns, while the neutral region allows for formation of the ordered block copolymer pattern that propagates away from the pinning regions without introducing defects and causing other problems such as polymer mis-orientation, etc. The current work presented in this paper suggests that instead of thinking of the pinning regions or stripes as guiding a single phase domain of the BCP, it may be better to think of the contrast between the pinning and the neutral stripe as the active feature that aligns BCP domains. Based on this idea, a new underlayer patterning strategy is proposed where instead of the underlayer patterns previously described in literature, a new underlayer composed of two large slightly preferential sections is used in order to induce pattern alignment and density multiplication. A key requirement is that each section of the guiding pattern is some odd number of lamellae wide. This form of an underlayer would be beneficial since the pattern would be more easily produced with current lithographic such as 193i lithography since the guiding pattern not only utilizes a more relaxed pitch but also a more relaxed minimum feature size than the ultimately desired density multiplied patterns formed in the BCP. The effectiveness of this new chemoepitaxial guiding pattern strategy has been evaluated using detailed mesoscale molecular dynamics simulations. Comparisons of this new strategy against more common single lamellae-wide pinning stripes with neutral intervening stripes will be made.

9049-94, Session PS5

Multiscale DSA simulations for efficient hotspot analysis

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In this study, we propose new, multi-scale simulations of directed-self assembly (DSA) for detecting hotspots (i.e., defects) efficiently over a large area. This multi-scale approach links “large-scale simulations with a simplified model” to “meso-scale simulations with the detailed models,” i.e., self-consistent field theory (SCFT) [Fredrickson G. H. (2006)]. For the simplified model, we utilize the so-called Ohta-Kawasaki (OK) model, which is an approximation of SCFT. Our previous study shows that the OK model is computationally very inexpensive while providing reasonably accurate results [Yoshimoto K. and Taniguchi T. (2013)]. We also add some new features (e.g., extension to the strong-segregation regime, inclusion of homopolymers and solvents) in the OK model that were not supported in our previous work.

Our multi-scale simulations are implemented as follows: 1) decomposition of a large, three-dimensional system (e.g., hundreds of micrometer) into relatively small sizes (e.g., a few micrometer), 2) parallel computations of block-copolymer annealing with the OK model, 3) detection of defected region, and 4) detailed analysis of the defects with SCFT simulations. From Step 3) to 4), the local volumetric densities of block copolymers calculated by the OK model are used as an input to SCFT simulations. Note that step 4) is necessary to understand the local conformations of polymer chains at the defects, and that most of the physical parameters (e.g., fraction of the blocks, degree of polymerization, Flory-Huggins parameter) are set to be the same as those in the OK model.

As a test case, we perform the multi-scale simulations for the formation of lamella structures on a relatively large area, consisting of some chemically guided regions. Our preliminary results (please see Fig.1 in the supplementary file) show that the lamella structures are formed perfectly on the chemically guide patterns, while that they become random at the edges of the guide patterns and in between the guided regions. By the same approach, we also attempt to find the locations of DSA hotspots in some other practical layouts and analyze the detailed chain conformations of block copolymers by performing SCFT simulations. In addition to the hotspot analysis, it is expected that this multi-scale modeling simulations may also be applied to design/process optimizations, new materials development (e.g., triblock, high ?), and so on.

9049-95, Session PS5

Achieving sub-10nm half-pitch structures by directed assembly of PS-b-PLA diblock copolymer thin films

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Directed assembly of block copolymers on chemically nanopatterned substrates (or chemical patterns) combines advantages of conventional photolithography and polymeric materials and allows the fabrication of dense arrays of regular and non-regular structures with a high degree of perfection and placement accuracy over arbitrarily large areas. Tremendous progress on directed assembly of block copolymers has been made in the past decade, however, previous work mainly focused on directed assembly of poly(styrene-b-methyl methacrylate) (PS-b-PMMA) diblock copolymers.1,2 The relative small x value of PS-b-PMMA limits its smallest achievable feature dimension. A high x block copolymer is required in order to fabricate sub-10 nm feature dimension.

Here we report our study on directed assembly of poly(styrene-b-lactide) (PS-b-PLA) on chemical patterns to fabricate sub-10 nm half-pitch structures for lithographic applications. PS-b-PLA has a higher x value relative to PS-b-PMMA and can microphase separate into structures with sub-10 nm feature dimension. Directed assembly of thin films of symmetric PS-b-PLA diblock copolymers was demonstrated with a high degree of perfection, registration, and accuracy on striped patterns having periods, Ls, commensurate with the bulk period of the copolymer, Lo (Figure 1). When Ls was incommensurate with Lo, defect-free assembly was only achieved on PS-b-PLA with racemic PLA blocks and the copolymer domains could be stretched up to ~60% on chemical patterns compared to Lo to match the Ls of the underlying substrate, analogous to the assembly behavior of PMMA-b-PS-b-PMMA triblock copolymers.3 The expansion ratio was significantly larger than that (~10%) of PS-b-PMMA diblock copolymer,4 which may be attributed to the formation of PLA stereocomplex.5 In comparison, PS-b-PLA with PLLA or PDLA blocks was only be able to assemble on chemical patterns with Ls close to Lo. When Ls was equal to nLo (n=2, 3), the block copolymer domains could interpolate on chemical patterns to multiply the feature density by a factor of n to achieve sub-10 nm half-pitch.6 We also demonstrated that the assembled domain structures could be transferred to the underlying silicon substrate by reactive ion etching.

9049-96, Session PS5

The formation of novel conformal self-assembly (DSA) for via pattern forming

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Directed Self-Assembly (DSA) is gaining momentum as a means to extend optical lithography past its current limits. There are many forms of DSA to bring solutions to both line/space and hole patterns. Similar to other pioneering techniques, the DSA process faces several challenges such as defect and process complexity. In order to optimize the DSA process and reduce the defect resource, a solution is to accomplish all the processes in the lithography track.

There are two steps to form the neutral layer (NL) pattern. First, a negative tone image (NTI) guiding pattern was formed and developed by negative tone developing (NTD) solvent. The NTI guiding pattern, with hydrophilic polymer remains, can resist the NL organic solvent during the NL coating. Second, a novel NL material is coated on the guiding pattern surface. After reaction and solvent strip, a conformal neutral layer is formed on the guiding pattern surface. In order to increase the neutral layer affinity to the guiding pattern, a cross-linking agent is added into the guiding resist. It is reported in this paper.

A typical polystyrene-block-methyl methacrylate (PS-PMMA) is used as our testing copolymer. The guiding resist with the new cross-linking agent improves thermal stability and linking reactivity with the NL material from baseline. After PS-PMMA coating and thermal annealing, the PMMA block was removed by O2 plasma for DSA patterning. This work shows a workable new method to form a 28-nm-pitch DSA pattern.

9049-97, Session PS5

Development of fast DSA simulation method using OCTA system

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It is considered that directed self assembly (DSA) method is one of the next generation lithography techniques to obtain the shrunk patterns. In the DSA method, the control of the block copolymer is much important to obtain the defect-free pattern and its control has been done in the several processes, such as coating or annealing processes. And more, there are several problems for DSA lithography as the pattern near the guide or pattern in the corner, etc. To study these DSA patterning, it is needed the DSA simulation to design the block copolymer and the DSA processes.

In the DSA patterning simulation, self consistent field (SCF) method is applied by several groups, and showed many kinds of results of patterned structures. The disadvantage of SCF method is the cost of SCF simulation. In the SCF method, the calculation of path integral takes much more cost and convergence of self-consistent field is also the critical problem for the cost. Another problem of SCF method is the simulation for the strong segregation system. In the strong segregation system, smaller mesh width is needed to represent the thin interface. However if we used the smaller mesh width, much more number of meshes are needed and its simulation becomes the heavy and the time-consuming simulation. These problems makes the SCF simulation limited tits system size and its time for these simulations.

To overcome these problems, we proposed the DSA simulation technique which is the combined method between two dimensional (2D) SCF and three dimensional (3D) dissipative particle dynamics (DPD) methods. This combined method has advantages of both an accuracy of SCF and fast and stably-working simulation of 3D DPD methods regardless of the strong repulsive interaction.

One example shows the DSA film on the chemical guide of the bottom layer. First we perform the SCF simulation of the 2D section. Using the density profile of 2D section by SCF method, 3D structure by DPD model is constructed by density biased Monte Carlo (DBMC) method which is one of the functions of COGNAC simulation in OCTA system. Each polymer chain by DPD particle is put along the density obtained by SCF method. From these simulations, we can obtain the phase separated structures. We can also discuss the line edge structure of the pattern from the phase separated structure. In the session we will discuss the DSA structure obtained by our techniques, and also discuss the availability of our simulation technique using our OCTA system.

9049-98, Session PS5

Design rules for directed-assembly of block copolymer films using topcoats

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Directed self-assembly (DSA) processes, based on block copolymer (BCP) films and lithographically pre-defined chemical pattern, have been extensively researched as an alternative lithographic technology to enhance the resolution of current lithography tools. [1-3] In the past two years, this approach has been implemented on 300 mm wafer scale fab processes in which the pre-patterns are defined using 193i lithography and trim etch.[4] DSA generation one processes are PS-PMMA with a resolution limit of ~12 nm. Here, we address challenges associated with generation two materials targeting further enhancement of resolution to achieve feature size below 10 nm. Fabricating sub 10 nm features using block copolymer requires the use of materials with Flory-Huggins interaction parameters larger than PS-PMMA. Often such block copolymers (BCPs) show the significant differences in surface energy between the blocks, one block tends to segregate to the free surface of films and precludes the assembly of the desired through-film perpendicularly oriented structures. We describe a generalizable toacoat strategy to solve this limitation based on both experimental and molecular simulation results. [5] The allowable properties of the topcoats depend on the interfacial energies of the layer with the blocks of the copolymer, and the block-block interfacial energy. The strategy is demonstrated experimentally by directing the assembly of polystyrene-block-poly-2-vinylpyridine (PS-b-P2VP) films on chemically nanopatterned substrates with different topcoat materials. The method introduced here allows us to realize 8 nm half-pitch line and space pattern by thermal annealing and pattern transfer.

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9049-100, Session PS5

Investigation of the resist outgassing and hydrocarbonaceous contamination induced for multi-electron-beam lithography tools

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Currently, inside single direct write lithography tool, contamination of the projection lens induced by resist outgassing is considered as not critical. Indeed, single electron beam induces too few sub-compounds outgassed from resist that deposition rate on projection lens remains negligible. However, in the incoming massively parallel e-beam exposure tools, designed to achieve a throughput of 10 wafers per hour per exposure module, the projection lens contamination issue no longer remains negligible. Consequently, it becomes mandatory to carefully analyze the mechanisms governing the contamination layer growth and to clearly evaluate its impact on the tool performances and stability.

In realistic operating conditions, the outgassed hydrocarbonaceous (CxHy) molecules are cracked by the high energy of incident electrons nearby the projection lens aperture and, consequently, a contamination layer is expected to grow on the various electron-optic elements. The purpose of our current experimental investigations is to determine under which conditions, the growth of contamination layer may obstruct projection lens aperture and modify, thereby, the e-beams path characteristics and the exposure performances. The work presented in this paper will describe a practical resist outgassing characterization system built in CEA-LETI laboratory. It has been designed in order to perform electron bombardment at 5keV of the e-beam resists coated on 100mm silicon wafer size. The wafer stage can be moved at constant speed to properly expose the resist surface with respect to the incident e-beam and to ensure a proper exposure dose control. A Quadrupole Mass Spectrometer (QMS) has been plugged to our experimental set-up and is used to monitor the sub-compounds outgassed from resist during wafer exposure. An additional ex-situ experimental method based on Thermo Desorption - Gas Chromatography - Mass Spectroscopy (TD-GC-MS) allowed also in parallel the identification of the sub-compounds outgassed from the resist coated wafer sample during the thermal desorption. The combination of those techniques was adopted to perform a comparative study of different resist formulations. Additionally, the wafers are exposed through micro-patterned silicon membranes (called mimics) that simulate the projection lens of the real multi e-beam exposure tool. This complementary test setting allows evaluating the contamination impact on these mimic projection optic lenses. This information is essential to evaluate the need of cleaning operation and to determine the need of maintenance to maintain a full and optimal operability of the massively parallel E-Beam machine.

This paper will report on the evaluation of the outgassing amount of various e-beam resists, with and without Photo Acid Generator (PAG) formulations. It will characterize the contamination layer induced by this outgassing phenomenon on the mimic projection lenses. Outgassing results on various resist formulations obtained on this test bench will be detailed. Furthermore, the effect and efficiency of top coat layer preventing resist outgassing and induced mimic contamination has been also investigated and this paper will discuss about the overall TC efficiency. Finally, insights on e-beam resist

performances assessment relatively to the outgassing and contamination requirements for multi e-beam lithography tools will be provided. The research leading to these results has been performed in the frame of the industrial collaborative consortium IMAGINE.

9049-25, Session 7

Improvements of self-assembly properties thanks to homopolymer addition or block-copolymer blends

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This contribution will be divided into two main parts. In the first one, we will present our own studies about the effect of homopolymer addition in a poly(styrene-block-methylmethacrylate) (PS-b-PMMA). The second part is devoted to the properties arising from the effect of blending different PS-b-PMMA based materials having different molecular weights (i.e. self-assembly of BCPs with large dispersity indices). For both studies, the BCP's self-assembly is performed on substrates presenting various surface-energies, with different BCP's film-thicknesses, and keeping in mind evident lithographic requirements such as short (few minutes) thermal bake, metallic residues-free starting materials, ambient atmosphere, etc… The BCPs materials used are synthesized in Arkema's factory at an industrial scale with a semi-continuous reaction process. Being aware about the critical importance of the reproducibility aspect in BCP's physico-chemical characteristics for lithographic applications, this unique semi-continuous process enable us to easily ramp up the synthesized quantities to tons level, and is well-known for its stability when compared to the recognized batch to batch variability of ultra-low temperatures ones. Moreover this reaction process allows in controlling precisely the amount of homopolymer, generated during the synthesis, present in the final material. Following this idea, some BCP materials containing various homopolymer amounts have been especially prepared for this study.

In both parts of this study, we will 1/ highlight the rules governing the BCP's period evolution within the final structure, 2/ describe the general properties (achievable film-thicknesses, CD uniformity…) of the final material through a comparison with pure BCPs systems having the same period (figure1), 3/ perform a statistical defectivity analysis5 in order to compare blended materials (BCP-homopolymer blends as well as BCP-BCP blends) and the pure BCPs. To further deeply understand the behaviors and abilities of blended systems, their respective self-assembly properties are also studied through graphoepitaxy templated approaches (i.e. lines-spaces as well as contact-hole shrink dedicated templates) and compared with their pure counterpart to highlight the advantages and drawbacks of both kind of materials toward physical constrains. These studies allowed us to extract precise material's physico-chemical characteristics requirements in order to be used for advanced lithographic applications.

9049-26, Session 7

300mm wafer performance characterization of the SMART™ directed self-assembly

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Polystyrene-b-poly(methyl methacrylate) (PS-b-PMMA) block copolymer (BCP) is a leading material candidate in directed self-assembly (DSA) technology development towards industrial applications for integrate circuit (IC) chip fabrication. At this moment, PS-b-PMMA is the only BCP system demonstrated on a whole 300mm wafer for its DSA performance

through either chemoepitaxy or graphoepitaxy DSA process. Great research efforts from both IC industry and academia have been devoted to understand a wide range of performance parameters which are critical for practical IC applications such as 300mm wafer DSA performance stability, DSA defectivity, pattern development via wet or dry process, DSA pattern LER/LWR, pattern etching transferability into hardmasks and so on. In this publication, we will start with a brief summary of current status of PS-b-PMMA DSA development toward IC applications and major issues. A new DSA chemoepitaxy flow, the SMART™ (Surface Modification for Advanced Resolution Technology), is reported. Its working mechanism is discussed. Good 300mm wafer DSA performance through SMART™ was achieved. Results of SMART™ DSA pattern CDU, LER/LWR and its pattern etching transfer into hardmasks are published. Simulation results of SMART pattern placement accuracy are discussed.

9049-27, Session 7

Extending the scope of polystyrene-block-polymethyl methacrylate in directed self-assembly

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Directed self-assembly (DSA) is a promising technique for extending conventional lithographic techniques by being able to print features with critical dimensions under 10 nm. The most widely studied block copolymer system is polystyrene-block-polymethyl methacrylate (PS-b-PMMA). The system is well understood in terms of its synthesis, properties and performance in DSA. However, PS-b-PMMA also has a number of limitations that impact on its performance and hence scope of application. The primary limitation is that it has a low Flory Huggins polymer-polymer interaction parameter (kai), which ultimately limits the size of features that can be printed by DSA. Another issue with block copolymers in general is that specific molecular weights need to be synthesized to achieve desired morphologies and feature sizes. We are exploring the use of additives to PS-b-PMMA which increase the kai parameter. This allows smaller feature sizes to be accessed by PS-b-PMMA. Depending on the amount of additive it is also possible to tune the domain size and the morphology of the systems. These findings may expand the scope of PS-b-PMMA for DSA.

9049-28, Session 7

Simulation study of the effect of differences in block energy and density on the self-assembly of block copolymers

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Implementation of directed self-assembly (DSA) of block copolymers (BCPs) introduces a series of engineering challenges that have not been completely addressed in previous BCP and lithography studies. One of the required innovations for DSA implementation is the accurate simulation of specific block copolymer chemistries and their interactions with interfaces. Many of the BCP simulation tools developed so far are based on mean-field type approaches which provide rapid simulation of equilibrium structures for ideal polymers, but have limitations or difficulty in terms of matching many of the common issues in experimental BCPs such as polydispersity and different statistical segment lengths. One of the potentially most important issues is the fact that real BCPs often have block energy and/or density asymmetry, meaning that each block has a different homopolymer density or cohesive energy density. For example, in polystyrene-block-poly(methyl-methacrylate) (PS-PMMA), PS has a density of around 1.05 g/cm3, while PMMA has a density of 1.18-1.19 g/cm3. As much higher x BCPs are investigated, the differences in block energetics will only increase which can lead to a number of problems that have only just begun to be investigated such as “skinning” of the top-surface of a BCP film by one of the blocks. As discussed last year, we have developed a simulation of BCP behavior and DSA processes based on molecular dynamics (MD) of coarse-grained polymer chains simulated using graphics processing units (GPUs) to perform the calculations. The polymers consist of a bead-spring type system where a single bead corresponds to multiple monomers. Each bead undergoes several interactions and these potential types allow us to fine-tune each individual block’s properties to accurately match experimental properties and easily capture asymmetry and differences between each block such as flexibility, statistical segment length, density, and cohesive energy density. In our work last year, we examined symmetric BCPs where the A block’s interactions and density is the same as the B block. This provides results similar to mean-field simulations, but we extended it to study blends of BCPs and polydispersity. , An example of the similarity in our results is illustrated in Figure 1 which shows the coexistence curve from the phase diagram of a mean-field simulation compared to our model for a symmetric BCP. This year, we have extended the simulations to study the effect of the block asymmetry on self-assembly. Figure 2 shows the experimental phase diagram for polyisoprene-b-polystyrene and our simulation results for the coexistence curve for a BCP model with similar asymmetry in density and energy. The real phase diagram in Figure 2 is much more asymmetric and tilted than the mean field result, and our model can clearly capture the changes in physics that gives rise to this asymmetry. If the simple differences between block energy and density can give rise to such large changes in the phase diagram, then how big is the effect on properties such as domain scaling with N and ?, self-assembly dynamics, and propensity to “skin” the top-surface? These issues must be investigated if we wish to accurately model true BCP behavior. Simulations of these issues will be described, we will discuss our simulation results, and suggestions for future design rules will be considered.

9049-29, Session 7

Directed self-assembly of block copolymers under graphoepitaxial confinement

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Directing the self assembly of block copolymers with graphoepitaxy is gaining attention as an option for advanced patterning. These physical confinement techniques provide strong driving forces for alignment, and techniques for aligning spherical, cylindrical, and lamellar morphologies have been developed. The mismatched surface energies typical of high chi materials can also be overcome by graphoepitaxy, thus enabling use of high-chi block copolymers. In this paper, we will present some of our efforts to develop new materials for graphoepitaxy DSA for line/space and contact hole patterning. We will discuss the impact of confinement on block copolymer morphology and reveal some unique morphologies not observed in bulk. We will also describe the impact of block copolymer composition and formulation on DSA patterning, including the effects on kinetics of self assembly and pattern fidelity.

9049-30, Session 8

Directed self-assembly of ABA triblock copolymer on chemical contrast pattern for sub-10nm nanofabrication by solvent annealing

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We report a fast, room temperature solvent annealing method for directed self-assembly of symmetric ABA triblock copolymer to form perpendicularly oriented lamellae on chemical patterns. The phase separation of ABA triblock copolymer is analogous to the counterpart AB diblock copolymer with half molecular weight. However, a much broader neutral window for surface wetting was found for the triblock. During the annealing process, the thickness change was monitored by in-situ reflectometry. After exposing to the solvent vapor for a certain time, thin films of a symmetric poly (2-vinylpyridine-styrene-b-2-vinylpyridine) (P2VP-b-PS-b-P2VP) triblock copolymer self assemble, while the nanostructure is retained after rapid solvent evaporation. The perpendicular lamellae with sub-10nm feature size can be assembled with density multiplication on lithographically defined chemical pre-patterns to form registered periodic arrays of striped patterns with exacting precision in continuously varying period and spacing. Using block-selective infiltration (Atomic layer deposition with sequential long soaking/purge cycles), the alumina composite with high etch resistance was specifically incorporated into the polar and hydrophilic P2VP domains; thereby the sub-10nm scale surface pattern was successfully transferred into underlying Si substrates by fluorine plasma etching.

9049-31, Session 8

Sub-10nm patterning process using directed self-assembly with high-x block copolymers

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The application of directed self-assembly (DSA) technology to the semiconductor production has been activated. DSA lithography has a potential to fabricate sub-10 nm patterns combined with ArF immersion or extreme ultraviolet (EUV)?lithography. In the several reports, hole-shrink and lines/spaces patterning processes were demonstrated using PS-b-PMMA materials. However, the phase separation limit of PS-b-PMMA materials is considered to be close to half pitch 10 nm lines/spaces patterns. In order to realize sub-10 nm lines/spaces patterning processes, a combination of materials with high-chi parameter equipped with the phase separation limit down to sub-10 nm regions and the suitable surface modification processes on chemical/physical guide patterns is required. [1, 2]

In this work, we report a fabrication process of sub-10 nm lines/spaces patterns using the DSA materials with high-chi parameters. As one of the most promising DSA materials we applied Si containing DSA materials to realize sub-10 nm lines/spaces patterning processes. Vertical lamella structures are considered to be suitable for lines and spaces patterning provided suitably modified surfaces on chemical/physical-guide patterns are prepared. Horizontal cylinder structures are considered to be convenient for lines and spaces patterning without any surface modification processes, in spite of difficulty on hard etch processes. Our target in this work is to clarify the process suitability of phase separation structures for lines and spaces patterning processes.

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9049-32, Session 8

Guided self-assembly of Si-containing block copolymer with a topcoat surface treatment

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Directed self-assembly (DSA) of block copolymers (BCPs) is one of candidate for next generation patterning technique. Many good demonstrations of DSA have been reported using polystyrene-block-poly(methyl methacrylate) (PS-b-PMMA) these days. On the other hands, BCPs which show high chi parameter are being developed because the BCPs can be formed smaller features than PS-b-PMMA. Si-containing BCPs are one of them. Moreover Si-containing BCPs show higher etch selectivity than PS-b-PMMA because of higher etch resistance of Si-containing block. Unfortunately, while Si-containing BCPs can be aligned by solvent annealing, they but cannot be aligned perpendicular to the substrate by thermal annealing. Because Si-containing block which has low surface energy achieves maximum interaction with air interface by forming a top parallel wetting layer to the substrate.

One solution to control of surface energy on top surface is the use of Top-Coat (TC). It has been already demonstrated that TC with Si-containing BCP could form perpendicular pattern. The challenges are TC coating onto BCP film and TC stripping after annealing. In order to solve these problems, polarity-changeable type TC has been developed. The effect of TC materials to generate finger print of BCP has been reported. However, this TC process should combine with DSA process to form aligned patterns.

Graphoepitaxy is one of the DSA technique to align BCP pattern using guide pattern. In this technique, the characteristic of guide pattern side wall is very important to control BCP pattern alignment for the Graphoepitaxy process. Also, in order to establish the process, there are two key parameters for the materials. One is BCP and guide pattern should have enough resistance to TC solvent through TC coating process. The other is TC can be removed easily with basic aqueous solution before BCP patterning. In this report, a detail of examination for TC Graphoepitaxy process will be discussed.

9049-33, Session 8

Self-assembly of high-resolutions PS-b-PMMA block-copolymers: processes capabilities and integration on 300mm track

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In this contribution, we aim to fulfill this lack of knowledge concerning PS-b-PMMA systems exhibiting both cylindrical and lamellar morphologies with high-resolution features in order to compare their

behavior toward the self-assembly with the ones of more classical BCPs with higher molecular weight. The BCPs materials are synthesized in Arkema's factory at large scale and present low metallic contents to be processed on TEL's 300mm track coater/developer. We first show that due to the specific synthesis approach used in Arkema's factory, the period of conventional BCPs is well controlled along different synthesis campaigns, illustrating the high level of polymer's characteristics reproducibility from one campaign to another. The improved lithographic process window (in terms of surface energy and accessible films thicknesses with defect-free perpendicular orientation) of these classical polymers allowed us to efficiently push down the PS-b-PMMA system toward its lowest limits, leading to high-resolution BCPs (periods close to ~20nm and domains dimension close or below 10nm). A first study is performed with different techniques to evaluate the order-disorder temperature (TODT) of the bulk polymers. Afterwards, using CEA-LETI clean room facilities, the self-assembly processes are optimized in order to determine both the best self-assembly temperatures and the best random copolymers sub-layers to achieve perpendicular features without defects, and a comparison between the TODT in bulk and the thin-film configuration will be scrutinized to correlate the influence of the surface's proximity on the self-assembly process. A special highlight will be also made on the influence of the reversibility on the self-assembly of these BCPs (i.e. over-passing the TODT and afterward going back to a cooler temperature for the self-assembly to take place), since only this kind of PS-b-PMMA polymers with low molecular weights could benefit from such process without degradation.

The integration of these BCPs is also studied by using various graphoepitaxy approaches (i.e. line-space (figure 2) or contact-hole shrink configurations), allowing therefore the determination of the best template size which can be used for lithographic applications. A study about small variations on the BCP's period templated in given patterns with fixed sizes allow to correlate their impact in terms of lithographic constrains.

It is well known that transfer's capabilities into substrates become increasingly more difficult along as the initial feature's size is reduced. Thus we address in this study this specific problematic to further illustrate the usefulness of these high-resolutions PS-b-PMMA BCPs for lithography: their transfer into substrates of interest (typical industrial 300mm stacked layers) are then studied using dry-etching techniques to find the best conditions leading to aggressive features.

9049-34, Session 9

Hard disk drive thin-film head manufactured using nanoimprint lithography *(Invited Paper)*

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The lithographic requirements for the thin film head industry are comparable to the semiconductor industry for certain parameters such as resolution and pattern repeatability. In other aspects such as throughput and defectivity, the requirements tend to be more relaxed. These requirements match well with the strengths and weaknesses reported concerning nanoimprint lithography (NIL) and suggest an alternative approach to optical lithography.

We have demonstrated the proof of concept of using NIL patterning, in particular Jet and FlashTM Imprint Lithography (J-FILTM) , to build functional thin film head devices with performance comparable to standard wafer processing. An ImprioTM 300 tool from Molecular Imprints, Inc. (MII) was modified to process the AlTiC ceramic wafers commonly used in the thin film head industry. Templates were produced using commercially viable photomask manufacturing processes and the AlTiC wafer process flow was successfully modified to support NIL processing.

Future work is identified to further improve lithographic performance including residual layer thickness uniformity, wafer topography, NIL to NIL overlay, and development of a large imprint field that exceeds what is available in optical lithography.

Keywords: nanoimprint lithography, hard disc drive, thin film head, AlTiC, NIL, template, RLT, Jet and Flash Imprint Lithography (J-FIL)

9049-35, Session 9

High-throughput jet and flash imprint lithography for advanced semiconductor memory

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Imprint lithography has been shown to be an effective technique for replication of nano-scale features.1 Jet and Flash Imprint Lithography (J-FILTM) involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate.2-4 The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed leaving a patterned resist on the substrate.

Previous studies have demonstrated J-FIL resolution better than 10nm (Figure 1), making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there is no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single level processing and zero waste, leads to a cost model that is very compelling for semiconductor memory applications.

The acceptance of J-FIL technology for the manufacturing of non-volatile memory will require a demonstration that it can attain defect levels commensurate with the defect specifications of high end memory devices. Typical defectivity targets are on the order of 0.10/cm2.

Non-fill defectivity must always be considered within the context of process throughput. Processing steps such as resist exposure time and mask/wafer separation are well understood, and typical times for the steps are on the order of 0.10 – 0.20 seconds. To achieve a total process throughput of 20 wafers per hour (wph), it is necessary to complete the fluid fill step in 1.0 seconds, making it the key limiting step in an imprint process. In our previous work, a non-fill defect density of 1.2 def/cm2 was demonstrated at fill times of 1.5 seconds (See Figure 2).5 For longer fill times, the defectivity dropped to zero. The controlling parameters for fast filling include small drop volume, GDS based volume targeting, fluid front control, low viscosity imprint resists and materials optimized for wetting and filling performance.

In this study, we have applied drop volumes as small as 1 picoliter to achieve filling times of less than one second (See Figure 3). Details surrounding the improvement in fill time, in addition to other aspects of the technology will be discussed.

9049-36, Session 9

The prospects of design for nanoimprint lithography: Layout refinement utilizing process simulation

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1. INTRODUCTION

Continuous shrinkage of design rule (DR) in ultra-large-scale integrated circuit (ULSI) devices brings about greater difficulty in the manufacturing process. Among several alternative lithography processes, NIL (Nano-Imprint Lithography) is one of the most promising candidates for its clear pattern transfer characteristics of mold contact patterning. Comparing SADP (Self-Aligned Double Patterning) or SAQP (Self-aligned quadruple patterning), finer pattern is formed with fewer process steps, and so the effect of greatly shortened TAT process is expected.

On the other hand, as pattern transfer process is completely different from optical lithography, new LCC (Lithography Compliance Check) and iPC (imprint Proximity Correction) flow preparation considering NIL process characteristic is indispensable for rapid yield ramp-up1-3).

In this paper, NIL LCC flow utilizing NIL simulation is examined applying to device test patterns under 30 nm.

2. NANOIMPRINT LITHOGRAPHY COMPLIANCE CHECKING SYSTEM

Figure 1 shows an example of schematic flow of NIL processes. The processes consist of template making, resist application, mold imprinting, and mold removal. In these processes, patterns are transferred through imprint process contacting mold to wafer, not through light propagation. And so lithography hotspot occurs at a context different from the hotspot occurs under optical lithography process. Layout dependent hotspot occurs through every step in NIL process. For example, variation through mold making, resist application, resist spreading, resist filling to mold trench, and resist corruption at mold releasing. To avoid hot spot occurrence, predict hotspots and fix them through litho-compliance check. An example of NIL compliance check flow is proposed in figure 2. Layout is analyzed with design rule checker (DRC), and hotspot candidate is extracted. And then, each hotspot is examined with NIL process simulation. Critical hotspots are modified in design or process, so NIL friendly design data is provided. At detailed NIL simulation, nano-scale three-dimensional process simulation, such as mechanical, structural, and resist fluid type simulation is indispensable, so computational cost as well as data volume are considerable issues. Modification rule is added to NIL design rules, so design rules are updated through compliance checking flow.

3. RESULT AND DISCUSSION

The proposed NIL-compliance checking flow is examined using NIL simulation applying to test device layout with line and spaces of 30 nm and below. Figure 3 shows examples of the simulation results based on known NIL hotspot in test pattern. Using mechanical simulation (a), resist corruption spot, caused by stress concentration on the border of different pitch of line and space area, is anticipated. Using resist flow simulation (c), layout dependency of resist flow is predicted. To fix resist spreading/filling hotspot, layout adjustment, as well as optimizing resist drop placement is indispensable. In this way, NIL process friendly design is coodinated. The detailed result will be shown in the presentation.

Development status of nanoimprint template quality

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Nanoimprint lithography is one of the potential candidates for the next generation lithography for semiconductor. This technology needs almost no additional mask data preparation from design, simpler exposure system, and just single patterning process without any coat/develop truck, and has potential of cost effective patterning rather than very complex optical lithography and/or continuous delaying EUV lithography.

The quality of the templates replicated from electron beam written “master templates” by nanoimprint lithography is one of the important aspects of the nanoimprint lithography technology.

As for the nanoimprint templates, defect quality is one of the most concerns. The master templates were fabricated by electron beam writing and photomask manufacturing technique and were almost defect free owing to the advanced repair technology. On the other hand, there were several nanoimprint specific defects on the replicated templates. By classifying these defects and analyzing the mechanism of the defect generation, we have succeeded to reduce the defect density drastically.

Master template characteristics should be transferred to the replicas without any degradation during the replication. Regarding the critical dimension, nanoimprint lithography step can increase the CD uniformity range. Nanoimprint step and following etching step have been optimized for CD uniformity improvement.

Image placement is also need to be cared during the nanoimprint step. Any induced distortion will increase image placement error.

Regarding the resolution, 1xnm HP LS pattern was already demonstrated and this is promising result for the coming semiconductor lithography.

In this presentation, the recent progress of the replicated template quality will be reported from the nanoimprint point of view.

9049-38, Session 9

Step-and-repeat nanoimprinting on pre-spin coated film: from sub-15nm metal patterning to the fabrication of a spectrometer-on-chip

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UV Nanoimprint Lithography (UV-NIL) is a very attractive technology to reproduce micro/nano-patterns over large area at low cost [1]. The Step&Repeat approach for UV-NIL allows reaching high throughput and is currently in industrial pre-production phase for various applications. Over the last few years, we have reported an attractive method combining the advantages of Step&Repeat technology and the imprinting of spin-coated films. Our process SR-NIL allows imprinting and the pattern transfer of the smallest features (sub-10 nm) reported in the literature [2-4]. It is also suitable to fabricate nanophotonic devices [5]. Here we present a novel process to fabricate sub-15 nm metallic nanostructures and show the full fabrication of a spectrometer-on-chip by SR-NIL.

To fabricate metallic structures by our SR-NIL, we developed a novel multi-layer PMMA/SiO2/APS/mrUVCur resist system in order to overcome adhesion issues of the NIL resist. Sub-15 nm metallic nanostructures were successfully replicated by imprint (Fig. 1a) and metal lift-off (Fig. 1b) opening a route to fabricate plasmonic devices by SR-NIL [6].

To prove capabilities of our process to fabricate real and complex devices, a nanospectrometer based on Digital Planar Holography (DPH) coupled with a full optical circuitry was fabricated. Devices are sequentially imprinted with the experimental mrNIL200 resist from MicroResist [7] and transferred into Si3N4 waveguide core film by two plasma etching steps. Finally a SiO2 upper cladding layer is deposited by plasma enhanced chemical vapor deposition. The spectrometer device lays on a 1.5?1 cm chip (Fig. 2). Dozens of devices were characterized to test the repeatability and the reliability of the NIL process. Optical measurements of the device properties show performances comparable with electron beam lithography fabricated devices.

Results prove the flexibility and robustness of the pre-spin coated SR-NIL process and establish the new state-of-the-art for SR-NIL confirming its actual potentials towards high throughput manufacturing of nanodevices with sub-15 nm features.

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9049-39, Session 10

MAPPER pre-production platform: Outlook on the 1st lithographic performances *(Invited Paper)*

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After several years of patterning capability demonstration on prototype platforms, massively parallel direct write lithography enters in a new phase with the introduction of a pre-production platform into LETI pilot line. This step represents a major achievement since it will allow to assess this technology capability versus the needs of the semiconductor industry(1). MAPPER lithography is currently the first company to have shipped such pre-production platform which will be validate in a production-like infrastructure at LETI. The challenges are quite simple: in the frame of the collaborative industrial consortium IMAGINE, the work will evaluate the ability of this new platform to answer industry requirements for the 14nm CMOS logic node as an introduction point.

In its 1st part, this paper will present the level of demonstration achieved so far on the current operated pre-alpha platform, confirming the capability of this technology to address a large range of domains for high to low end applications (fig. 1). Then this work will highlight the coming challenges till to be overcome for definitively confirm the potential of this technology in terms of alignment, overlay, throughput and reliability.

Since the arrival of the 1st parts of the future MAPPER pre-production tool mid 2013 at LETI site (figure 2), named FLX1200, the IMAGINE team started the hook-up phase of this new generation massively parallel that integrates optical alignment capability and is able to drive individually 1300 beams in parallel to reach a final throughput of 1 wafer per hour (2). This paper will detail all the results obtained from the hook-up phase to the 1st exposure results. Based on these results, a discussion will be engaged to draw the perspective of this technology with respect to semiconductor industry needs.

9049-40, Session 10

Demonstration of EDA flow for massively parallel e-beam lithography

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Today's soaring complexity in pushing the limits of 193nm immersion lithography drives the development of other technologies. One of these alternatives is mask-less massively parallel electron beam lithography, (MP-)EBL, a promising candidate in which future resolution needs can be fulfilled at competitive cost.

MAPPER Lithography's MATRIX MP-EBL platform has currently entered an advanced stage of development. This tool will operate using more than 13,000 beams, each one writing a stripe 2.2?m wide. 0.2?m overlap from stripe to stripe is allocated for stitching. Each beam is composed of 49 individual sub-beams that can be blanked independently in order to write in a raster scan pixels onto the wafer.

Simultaneous with the development of the tool itself, steady progress is being made in e-beam process and EDA infrastructure.

This paper focuses on the data preparation for the MATRIX tool, in particular model calibration, a performance comparison of different Proximity Effect Correction (PEC) methods and stitching methods. Besides 32nm HP designs – the initial target for this tool – this paper shows data preparation flow performance on 22nm HP designs.

In single e-beam tools (Gaussian or Shaped-beam), throughput depends heavily on the number of shots. In MATRIX this is not the case as in the raster scan strategy the entire area of the written field is scanned regardless of the design itself. Instead of pattern density, the maximum local dose on the wafer is limiting throughput.

For proximity effect correction in MATRIX three elementary building blocks exist: dose modulation, geometry (size) modulation and background dose addition. In this paper, (combinations of) these three methods are compared quantitatively in terms of throughput impact and process window. On top of that, over-exposure in combination with negative bias results in process window enhancement at the cost of throughput, a trade-off that is explored in detail.

Typical test cases include dense and isolated regions, contacts and line ends.

Before the performance of PEC methods is compared, a method of Model Calibration (Point Spread Function of the e-beams) is described and applied.

As a last topic, the interplay between PEC method and tool characteristics of on-tool data path and beam to beam stitching is studied.

The combined results are concluded into recommendations on and qualification of the optimal data preparation strategy for 32nm HP and 22nm HP designs in the MATRIX tool.

The research leading to these results has been performed in the frame of the industrial collaborative consortium IMAGINE.

9049-41, Session 10

Reflective electron-beam lithography: alignment and stitching of patterns printed via CMOS DPG chip *(Invited Paper)*

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Maskless electron beam lithography can potentially extend semiconductor manufacturing to the 10 nm logic (16 nm half pitch) technology node and beyond. KLA-Tencor is developing Reflective Electron Beam Lithography (REBL) technology targeting high-volume 10 nm logic performance. REBL uses a novel multi-column wafer writing system combined with an advanced stage architecture to enable the throughput and resolution required for a NGL system. Using a CMOS Digital Pattern Generator (DPG) chip with over one million microlenses, the system is capable of maskless printing of arbitrary patterns with pixel redundancy and pixel-by-pixel grayscaling at the wafer. Electrons are generated in a flood beam via a thermionic cathode at 50-100 keV and

decelerated to illuminate the DPG chip. The DPG-modulated electron beam is then reaccelerated and demagnified 80-100x onto the wafer to be printed.

Previously, KLA-Tencor reported on the successful use of a fully-functional CMOS controlled DPG chip to achieve grayscale printing in photoresist on a moving stage. The present work expands upon these results to demonstrate alignment and stitching between print swaths using REBL's third generation column operating at 75keV and mounted on a maglev lithography stage. Using both positional detection of the electron beam and the optical-based REBL Wafer Metrology System (WMS), print swaths have been aligned to features on the wafer and each other to stitch them into larger printed areas. Print results for line/space and device test patterns at the 45nm node will be presented.

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9049-42, Session 10

The REBL digital pattern generator: recent innovations and remaining challenges

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Reflective electron-beam lithography (REBL) employs a unique device to impress pattern information on an electron beam. This device, the Digital Pattern Generator (DPG) is an array of small electron reflectors, in which the reflectance of each mirror is controlled by underlying CMOS circuitry. The array is illuminated by a beam with a rectangular cross-section, which is decelerated as it approaches the array so that the small voltage swings available from the CMOS circuits is sufficient to make the individual reflective elements reflecting or non-reflecting. Each reflective element contains a tiny electron-optical system consisting of several focusing elements in addition to the switched electrode.

Those electrons that are reflected are re-accelerated as they depart the DPG. Thus the DPG is effectively a programmable electron-luminous image source. By switching the mirror drive circuits appropriately, the DPG can scroll the image of an integrated circuit pattern across its surface; and the moving electron image, suitably demagnified, can then be used to expose the resist-coated surface of a wafer or mask.

This concept has been realized in a device suitable for 40nm lithography demonstrations. A next-generation device has been designed and is presently nearing completion. The new version includes several advances intended to make it more suitable for application in commercial lithography systems. The improvements include high-speed data inputs, on-chip data decompression, bi-directional data movement, mirror calibration capability, a new reflector array with a smaller pitch, and error detection and diagnostic features. A new lenslet fabrication process was also adopted.

We will describe the analysis which led to the design of the current DPG, and discuss the innovations and compromises made in designing this next-generation device. For application in commercially-practical high volume ML2 at upcoming device nodes, still more innovations are needed. We will describe some of the directions in which our present technology can be extended, and also discuss some more speculative potential innovations.

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9049-43, Session 10

Massively parallel EB direct writing (MPEBDW) system based on microelectromechanical system (MEMS)/nc-Si emitter array

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On a basis of our previous report on Massively Parallel Electron Beam Direct Writing (MPEBDW) with the active-matrix drive nanocrystalline Si (nc-Si) electron emitter, some important aspects are discussed including the resolution limiting factor. We have constructed the MPEBDW system by development of the nc-Si electron emitter array compatible with an active-matrix large-scaled-integrated circuit (LSI). We demonstrated the 200x200 prototype emitter array operated the 1:1 EB exposure test that the selected subset square patterns were reproduced on the target wafer with little distortion and fluctuation1. More than ten thousand electron sources are arrayed in the 10mm square, and the electron image emitted from the sources is reduced and projected on the target wafer. Electron optics of the system consists of the emitter array, a MEMS condenser lens array, a stigmator, three-stage deflectors, and a reduction lens as shown in Fig. 1. The reduction lens focuses all beams on the surface of the target wafer, and reduces the electron image to 1%-10% in size. The diameter of the column including this electron optics is suppressed to 100 mm. In the conventional way for fabrication of the electron optics under a paraxial ray condition, the size of the column should become larger because our electron source occupies 10 mm square.

In the present system, the beams incident on the outside of the paraxial region of the reduction lens can be also employed using the emitter array including functions of correcting optical aberrations. One of major determining factors of the resolution and the throughput of the electron beam writing is the coulomb blur. To avoid the effect of coulomb repulsion, the electron optics is designed such that the electron beams have no crossover points in the region from the output of the condenser lens array to the focusing target. Figure 2 indicates the effect of coulomb repulsion in the reduction lens. When each beam current is lower than 10 nA, the spot size of 10 nm can be obtained with the acceleration voltage of 5 kV in this electron optics. The usefulness of the mask-less multi-column/multi-beam EB lithography will be made clear by the demonstration of high resolution writing using the MPEBDW system.

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9049-44, Session 11

Block copolymer lithography in the fabrication of templates with high-bit aspect ratio rectangular bits

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Since the first demonstration of rectangular patterns by block copolymer directed self assembly, the main strategy for pattern formation of rectangular arrays with arbitrary aspect ratio has revolved around a dual process in which two separate and perpendicularly oriented arrays of

stripes are intersected to form a rectangular lattice.1, 2 In the context of doing lithography at densities in excess of 1Tdot/in2 for magnetic recording bit patterned media, the application needs to overcome two important challenges. First, the critical dimension of each feature needs to be pushed at or below 10nm which is out of the range of what can be currently transferred with PS-b-PMMA block copolymer lithography. Second, the process leading to the intersection of the two arrays of lines needs to be designed to optimize yield while efficiently managing the risk inherent in a long sequence of fabrication steps.

Here, we present an overview of DSA strategies addressing the above mentioned challenges. To address the feature density and critical dimension issue, dense arrays at or below 20nm full pitch are achieved through a series of density multiplication and double patterning techniques. For the second issue, the intersection of the two perpendicular arrays of lines can be done through a parallel process involving two separate sub-master templates that are then intersected in double imprint process or a serial process involving a single master on which two consecutive DSA steps are performed on top of each other. In all cases, block copolymer lithography is at the core of all nanofabrication strategies.

Here, BCP lithography is implemented by directed self-assembly of PS-b¬-PMMA on e-beam lithography defined chemical patterns. A state-of-the-art rotary e-beam tool is used to expose resist prepatterns with periodicities commensurate to the natural periods of different lamellae-forming PS-b-PMMA block copolymers. Directed self-assembly with 2 or 3 times density multiplication is carried out on chemical contrast patterns produced by a combination of cross-linkable mats and polymer brushes.3 Sub-master templates with circumferential lines are obtained by transferring the BCP patterns into silicon substrate. The templates with radial lines are pre-deposited with a layer of mandrel material. The BCP patterns are transferred to the underlying mandrel layer preferably by a block-selective sequential infiltration synthesis (SIS) technique4, 5. A SADP process was carried out on the mandrel lines to double the line frequency in comparison to the BCP patterns. The cross line patterning can be obtained by imprinting from a sub-master template with circumferential lines and using the imprint resist as a mask to chop the radial lines. Another method for cross line patterning is to perform a second directed self-assembly step. We first apply a layer of crosslinked polystyrene mat to planarize the radial line patterns, coat an e-beam resist film, and send the template back to the rotary e-beam lithography tool to generate circumferential line chemical patterns. Directed self-assembly is then performed to obtain long-range ordered BCP patterns. A block-selective SIS technique is used to metalize the PMMA bocks. After removing polymer by oxygen plasma, the remaining metal lines serve as mask for chopping the radial lines. We have successfully demonstrated fabrication of imprint templates with rectangular bits for areal densities 1.6 Td/in2 and above.

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9049-45, Session 11

Customization of directed self-assembly patterns from chemoepitaxial etch trim using a self-aligned hardmask (CHEETAH)

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The directed self-assembly (DSA) of block copolymers (BCPs) is a promising resolution enhancement technology to extend lithographic patterning capability. Chemoepitaxy has been demonstrated to reliably generate dense gratings and hexagonal arrays from sparse chemical prepatterns. However, many patterning applications demand complex customization of BCP patterns with constraints on edge placement accuracy that may exceed the capabilities of current lithographic tools. To address this challenge, we introduced a simple and versatile self-aligned customization process, CHEETAH (CHemoEpitaxial Etch Trim using a self-Aligned Hard Mask). The CHEETAH chemical prepatterns consist of inorganic directing lines and “masking features” on organic neutral substrates. Figure 1 shows the schematics and SEM images of CHEETAH process and the results of bi-directional customization of 25nm pitch PS-PMMA lamellae patterns. The directing lines guide the alignment of lamellae and the masking features serve as block out masks (figure 1.1). Incorporating non-directing masking features into chemical patterns enables bidirectional customization using CHEETAH based on the capability of the BCP to form globally aligned periodic features over these masking features self-aligned with the pattern of like periodic features in the surrounding areas (figure 1.2). A composite mask combining self-assembly domains and the inorganic prepattern is formed after selectively removal of PMMA (figure 1.3). Subsequent pattern transfer steps render the composite mask features into the bi-directional customized patterns in the organic hardmask layer (figure 1.4).

In addition to demonstrating bi-directional customization of dense line-space patterns at very high resolution, we have further investigated several parameters with respect to the performance of the CHEETAH process. The impact of these key parameters and fundamental DSA mechanism will be discussed for CHEETAH customization.

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9049-46, Session 11

Tuning the strength of chemical patterns for directed self-assembly of block copolymers

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Directed self-assembly (DSA) of block copolymers (BCP) via chemo-epitaxy is a potential lithographic solution to patterns of dense features. The LiNe (Liu-Nealey) flow for fabricating the chemical pattern is illustrated in Figure 1. The chemical pattern guides the BCP due to the different wetting behavior of the materials. Fine control of both the chemical pattern chemistry and geometry are important for DSA of BCP. For example, non-bulk morphologies that can complicate pattern transfer have been observed to form due to non-optimal chemical patterns. Furthermore, wetting behavior considerations for DSA extend beyond pattern design and include the surrounding region. BCP DSA would be easier to integrate into device design if the patterned region were isolated with a featureless region (horizontal lamellar BCP assembly) rather than undirected BCP fingerprint structures. Selecting the background behavior requires control of the wetting behavior of the materials.

This study explores the relationship between the chemical contrast of the pattern and the BCP DSA. Chemical contrast refers to the difference in the wetting behavior of BCP on the guiding stripe and the background. The wetting behavior depends on the selection of crosslinking and brush materials as well as the annealing conditions, since the guiding stripe

is modified by the brush deposition process. Using this tunability of the wetting behavior of the preferential guiding stripe as well as the bordering unpatterned preferentially wetting surface, the strength of the chemical pattern can be controlled to optimize the process window and orientation control.

9049-47, Session 11

Predicting process windows for pattern density multiplication using block copolymer directed self-assembly in conjunction with chemoepitaxial guiding layers

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Pattern density multiplication using directed self-assembly (DSA) of block copolymers (BCPs) is a technique capable of producing patterns with small pitches utilizing guiding template patterns printed as larger feature sizes and pitches. One method for achieving this density multiplication is to utilize chemoepitaxy based on a guiding underlayer that is nominally topographically flat but which is composed of a pinning region, or stripe if referring to lamellae, which will chemically prefer one microphase of the BCP, as well as a second region that is often referred to as “neutral” to both phases of the BCP. In most conceptions of such a chemoepitaxial approach for alignment of lamellae patterns, the pinning stripe is typically the width of a single lamellae of the phase separated BCP, while the neutral stripe is some odd number of lamellae widths. It is currently unclear how such underlayers and their ability to successfully guide DSA patterns are affected by variations in the width of the guiding stripe, which may occur due to difficulties in patterning, as well as variations in the overall composition of the pinning and neutral stripes. In this work, detailed simulation studies have been performed to elucidate the effects of such variables (e.g. guiding stripe size, chemical composition pinning and neutral stripes, etc.) on the process window, overlay accuracy, and CD uniformity in DSA pitch sub-division patterning processes. A simple but novel technique has been developed and utilized to quantify the level of alignment of a simulated BCP film to an underlying guiding pattern. Such process windows and lithographic parameters have been studied for several different pitch sub-division conditions including 1:1, 1:3, 1:5, and 1:7 pinning stripe:neutral strip width ratios. It is found that the center of the processing window occurs at a composition of the “neutral stripe” such that it is slightly to somewhat strongly preferential to the type of polymer of opposite type to that attracted by the pinning stripe, and that this ideal “neutral stripe” composition becomes more neutral as the density multiplication increases.

9049-48, Session 11

Directed self-assembly of diblock copolymers in laterally confining channels: Effect of rough surfaces on line-edge roughness (LER) and defectivity

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The directed self-assembly (DSA) of diblock copolymers in laterally confining channels is a promising avenue to produce line and space patterns with a sub-25 nm pitch. In this study, we use self-consistent field theory (SCFT) to investigate the DSA of both cylinder- and lamellaforming diblock copolymers in narrow trenches with corrugated sidewalls. Specifically, we focus on systems that form lying-down cylinder monolayers or standing-up lamellae parallel to the sidewalls of the channel. While previous experimental and computational studies highlighted well-ordered cylinders and lamellae in smooth channels, undesirable defective structures are also observed. In the present study, the wetting sidewalls of the channels are no longer flat and smooth surfaces. Rather, we consider undulating sidewalls and investigate the effect of the rough surfaces on defectivity and line edge roughness (LER) in the self-assembled morphologies.

We use SCFT to investigate the formation free energy of isolated, metastable defects of both cylindrical and lamellar block copolymers inside channels with sinusoidal corrugations along the sidewalls. Parametric studies include the effects of the amplitude and the frequency of the sinusoidal wall shape function, the placement of the defect core, as well as the number of cylinders and lamellae in channels with varying widths.

Our simulations indicate that the relative drops in defect formation energy in rough channels compared to smooth channels are strikingly similar in both cylinder - and lamella-forming melts.

Furthermore, using a suitable order parameter and the center -to-center displacement of the self-assembled lines, our investigations show that the propagation of the LER is sensitive to the amplitude and the wavelength of the sidewall shape function, with an even stronger dependence in the lamellar case compared to the cylindrical case.

More broadly, our study reveals the dependence of line edge roughness propagation on a wide range of parameters that must be carefully controlled in order to successfully implement a directed self-assembly process with block copolymers.

9049-49, Session 12

Nanoimprint lithography process chains for the fabrication of micro- and nanodevices *(Invited Paper)*

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Device manufacturing for research and industrial applications relies on process chains involving both standard and innovative process steps. Standards can only be defined if tools, materials and protocols exist which allow to setup new processes, innovation implies the use of specific properties inherent to the new process. Particularly interesting are cases where new process steps such as nanoimprint are used to replace other lithographies, to add new functionalities to existing devices or to enable the fabrication of new devices not or difficult to achieve with other processes. In my talk I will present a tool box approach for micro- and nanodevices based on nanoimprint lithography, and illustrate this with examples ranging from surface patterning of polymer microcantilevers for biosensing to surface patterning of lightguides for backlight applications.

9049-50, Session 12

Detection of the early stage of recombinational DNA repair by nanowire transistors fabricated by oxidation scanning probe lithography

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A silicon nanowire-based biosensor has been designed and applied for label-free and ultrasensitive detection of the early stage of recombinational DNA repair by RecA protein.[1] Silicon nanowire transistors were fabricated in a top-down approach on a silicon-on-insulator substrate, first by defining a mask by oxidation atomic force microscopy nanolithography, followed by reactive ion etching in a O2-SF6 plasma. Contacts to the nanowire were finally defined by photolithography and the device was integrated into a microfluidic environment.[2] The sensor operates by measuring the changes in the resistance of the nanowire as the biomolecular reactions proceed. We show that the nanoelectronic sensor can detect and differentiate several steps in the binding of RecA to a single stranded DNA filament taking place on the nanowire-aqueous interface.[3] We report relative changes in the resistance of 3.5% which are related to the interaction of 250 RecA•single stranded DNA complexes. Spectroscopy data confirm the presence of the protein-DNA complexes on the functionalized silicon surfaces.

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9049-51, Session 12

Lithography challenges and opportunities in fabrication of bit patterned media with areal density beyond 1.5 Tdpsi

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Bit patterned media (BPM) recording is currently being considered for the next generation high capacity magnetic recording. However, BPM presents extreme challenges to lithography because of the small feature size and the tight spacing tolerance requirements. Directed self-assembly (DSA) of block copolymers has been proposed as a viable lithography strategy for BPM patterning. In this paper, we will present a DSA process with sphere-forming PS-b-PDMS pattern (hcp) for coherent dot patterning over large area at density of up to 3.2 Tdpsi (Figure 1). Using this process, a 1.5Tdpsi BPM template with integrated servo has been successfully fabricated in quartz wafers for nano-imprint lithography (NIL). A two-step DSA integration scheme has been developed for patterning hexagonal arrays of dots in data sectors, and non-periodic servo dot patterns in servo sectors (Figure 2). 1.5Tdpsi BPM media with integrated servo on 2.5” disks have been successfully fabricated by NIL and pattern transfer into a magnetic thin film layer by ion beam etching (Figure 3). The integrated servo in the 1.5Tdpsi BPM media has enabled closed loop servo tracking on a spin-stand test, similar to our previously reported test recording at 1.0 Tdpsi where BER of -2.43 (Figure 4) was achieved. Although a significant progress in 1.5 Tdpsi BPM patterning has been achieved, many lithography challenges still remain, principally in skew limitation, and in density extensibility, and size variation control. Possible solutions such as patterned rectangular media with lamellae-forming BCP and double patterning process will be discussed.

9049-52, Session 12

UV nanoimprint lithography for the fabrication of MEMS tunable Fabry-Perot infrared filters

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One of the largest application fields for Nanoimprint Lithography (NIL) is the fabrication of optics and photonics. Driven by the demand of miniaturized and highly integrated functionalities in the area of photonics and photonic circuits, Plasmon optics has become a promising method for manipulating light. Especially the application of periodic sub wavelength holes/pillars structures within an opaque metal film on a dielectric substrate holds many advantages for the realization of optical filters, since the variation of the hole/pillar diameter and the periodicity allows a selective filter response.

This paper introduces a typically used process flow for pattern transfer via UV-NIL for the fabrication of MEMS tunable Fabry-Perot infrared filters. This process flow includes the fabrication of the working stamps, the NIL process itself and the dry etching for pattern transfer. For the filter element an optical nano structure was fabricated into 80 nm thick aluminum layer deposited on a 200 nm silicon nitride membrane onto 4 inch 300 µm thick silicon substrates.

For the fabrication of this filter with a wavelength range from 3.1 µm up to 3.7 µm and full width at half maximum of min. 80 nm it is necessary to realize a pillar array with a pillar diameter of 1 µm and a periodicity of 150 nm. The simulation results of this geometry/construction using Finite-Difference Time-Domain (FDTD) method is described elsewhere.

First, a 6 inch Ormocer® working stamp was fabricated by molding technology to build up a negative replica of the master (Figure 1). Therefore the silicon master wafer was coated with an anti-sticking layer. In parallel the 500 µm glass backplane was coated with an adhesion promoter using spin coating. After that, the photo sensitive forming polymer was coated onto the master and a glass backplane was inserted. Then, the stack was cured with UV light and manually demolded. This technology allows the fabrication of working stamps with dimensions ranging from µm to nm with a dimensional accuracy of ±7 %. For the UV-NIL process the substrates to be patterned (4 inch silicon wafer with 80 nm aluminum on top of a 200 nm silicon nitride membrane) were coated by primer and UV resist. The substrates and the working stamps were pressed together and exposed using an EVG 6200 Aligner. After manual demolding the substrates were dry etched to remove residual resist layers and to transfer the pattern into the substrate (Figure 2). In order to ensure the dimensional stability of the molded structures, characterization was consequently done by means of a self made non-contact mode atomic force microscope. The functionality of the optical filter was proved by comparison of the measured and the simulated transmission (Figure 3), respectively. After the whole production run the tunable filter (Figure 4) were characterized using an FTIR-spectrometer. Herein, it is shown, that in the 4th order it is possible to filter light from 3.1 µm and 3.7 µm with an actuator voltage of 0 V to 75 V.

9049-53, Session 12

New lithography technology for sub-10nm patterning with shrinking organic material

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1. INTRODUCTION

In next generation lithography to make sub-10nm pattern, some technologies (Extreme-UV (EUV), Directed self-assembly [1], [2] (DSA) and Nano-imprint lithography (NIL) etc.) are proposed.

In the case of EUV, it is easily possible to reduce the pattern size by enlarging numerical aperture (NA) of optical system. However, complicated equipment increase a cost of lithography. In the case of DSA, it is feasible to make nanometer size patterning by optimizing a block co-polymer and a guide pattern. However, development of various polymers is necessary to make various pattern pitches. In the case of NIL, it is also possible to get nanometer structure by preparing a master

template recorded with electron beam (EB). However, production time of the template becomes elongated to get extra-fine nanometer structures.

This paper describes cost-effective new lithography process for making sub-10nm pattern using special organic material which is able to reduce a pattern size by shrinking. Shrinking ratio of various methods, decreasing line edge roughness (LER) and patterning of less than 10nm will be reported.

2. NEW LITHOGRAPHY WITH PATTERN SHRINKING

Figure 1 shows process flow chart of new lithography using pattern shrinking. First, master template is produced with conventional lithography. The resin of pattern shrinking material is prepared and coated on the master template. After UV irradiation, organic soft template is separated from the master template. The pattern is replicated on the surface of the organic soft template. Through shrinking process, the soft template is shrinking and its replicated pattern is also shrinking. When the above process is repeated, pattern size will be extremely reduced. The shrinking soft template can be used to make a copy quartz template with reduced patterns (Fig. 2).

3. RESULTS AND DISCUSSION

There are some concepts to achieve shrinking of lithography patterns. The first one is to use UV curable resin with multi-functional monomers. As cured photo-polymer has large shrinkage, the pattern size is reduced. The second one is to apply fluorocarbon. UV resin with fluorocarbon liquid is used. After peeling, fluorocarbon becomes gas so that pattern shrinking of cured photo-polymer occurs. The third one is changing chemical structures of a polymer. The special organic material is coated on the template. Then, the soft template is replicated. After baking process, the pattern size is markedly decreased.

Shrinking ratio of each concept is shown in Fig.3. The largest shrinkage was observed using the special organic material. SEM pictures of the shrinking organic soft template are shown in Fig.4. Shrinking ratio and a pattern size dependence of shrinking ratio were evaluated. The shrinking ratio of 23% was obtained on both half pitch (hp) of 100nm and 38nm. Also LER was evaluated and the results are shown in Fig.5. LER reduction by the shrinking soft template was observed.

4. CONCLUSION

New lithography technology using the pattern shrinking material has been proposed. It was confirmed a half pitch size was markedly reduced. The shrinking ratio of 23% and LER reduction of 70% were obtained.

9049-54, Session 13

A full-chip DSA correction framework

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The graphoepitaxy directed self-assembly (DSA) process uses confinement wells to direct the thin film self-assembly of block copolymer into the desired features which are etch transferrable into the substrate. To fabricate these confinement wells, the conventional DUV immersion lithography adopted in 28nm, 20nm technology node or EUV lithography for smaller nodes is still required. The shape of the confinement wells needs to be designed properly, to ensure that the DSA process in them results in the DSA features of desired shapes and placements. Therefore DSA proximity correction (PC), in addition to OPC, is essential to obtain confinement well shapes that resolve the final DSA patterns precisely [1].

In this paper, we applied DSA PC to obtain arrays of contact-like holes which can form cylindrical structures with appropriate process parameters of DSA diblock copolymer for volume fraction and Flory Huggins parameter. Smart methodology of decomposition on the designed contacts into several groups, each sharing a single confinement well is developed to deliver best confinement well shapes that are DSA PC convergence friendly. In proximity correction, two different kinds of model are involved, one is regular OPC model and the other is the DSA model where they correspond to optical/resist and DSA processes, respectively. Since the DSA simulation can consume a large portion of the simulation time, the correction algorithm is optimized to minimize the number of DSA simulation function calls. We also intensively leverage the fast OPC simulation in correction iterations.

The goal of this paper is to look into the technical prospects of DSA correction technology. We have developed an in-house correction tool and fast DSA simulation model [2] that provides the ability to optimize process and integration [3] and define design rules [3]. We discuss the DSA full-chip computational correction framework using the contact holes as an example. Appropriate cost functions, various optimization approaches and multiple correction flows are proposed and investigated. Finally, we will summarize the challenges associated with computational DSA technology.

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9049-55, Session 13

DFM for defect-free DSA hole shrink process

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The application of directed self-assembly (DSA) to the hole shrink process has gained large attention because of the low cost and the potential for sub-lithographic patterning of contact, via and cut masks ([1] and references therein). The DSA hole shrink process is proceeded as follows: 1) lithographic step to generate holes on the substrate, 2) deposition and annealing of poly(styrene-block-methyl methacrylate) (PS-b-PMMA) block copolymers on the pre-patterned substrate, 3) selective removal of cylindrical PMMA domain formed at the center of the pre-patterned hole, 4) pattern transfer to the underlying layer via plasma etching. After the annealing, PS residual layer is formed at the bottom surface of the pre-patterned hole (Fig. 1) and it prevents the etch process from passing through the substrate. This defect issue still remains unresolved, mainly due to numerous parameters affecting on the formation of the PS residual layer, e.g. hole radius, depth and taper angle.

In this study, we utilize the so-called Ohta-Kawasaki (OK) model in order to find the most sensitive parameters to the defects and to optimize the designs and processes of the DSA hole shrink process. The OK model is an approximation of self-consistent field theory (SCFT), whose advantages are reasonable accuracy and computational time [2]. We also add some new features that were not supported in the original OK model: 1) extension to the strong-segregation regime, 2) inclusion of homopolymers and solvents, 3) formation of meniscus at the air-copolymer interface. Note that various other simulation methods, such as SCFT [3] and dissipative particle dynamics [4], have been applied to predict the formation of the PS residual layer. However, those simulations are generally computationally expensive and not suitable for the elaborate process optimization with multiple parameters.

In addition to the simulations, we also examine the optimized designs and process conditions on 300 mm wafers. In our design-for-manufacturing (DFM) flow, first we calibrate the simulation parameters (e.g., interfacial parameters between the block copolymer and the wall) with some top-down and cross-section SEM images (e.g., Fig. 1). Next, we perform simulations with the calibrated parameters, using the OK model. In the optimization, we focus on the design and process parameters which are easily modulated in experiments, e.g., hole size, depth, taper angle, and film thickness. Finally, we run the DSA hole shrink

process on 300 mm wafers under the optimized conditions. The results show that the number of the defects is decreased effectively by the optimization. It is expected that our DFM approach may also be applied to the other DSA processes, such as density multiplication of line/hole structures.

9049-56, Session 14

Evaluation of integration schemes for contact-hole graphoepitaxy DSA: A study of substrate and template affinity control

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In recent years, block copolymer (BCP) directed self-assembly (DSA) has been widely investigated as a potential technique that can extend lithography to meet the challenging requirements of future nodes. In particular, the grapho-epitaxy DSA shrink of contact-holes in a resist pre-pattern has become a promising and versatile method to obtain sub 20nm holes.

The critical points for a grapho-epitaxy contact-hole shrink DSA process in a guide resist template include: (1) obtaining a good quality guide resist pre-pattern and (2) realizing proper phase separation of the BCP. Herein, we study the impact of the resist and substrate on the pre-pattern generation and BCP assembly. In addition, the effect of template affinity control for BCP assembly is investigated and is shown to result in a substantial improvement in the BCP phase-separation.

The quality of the contact-hole shrink is ultimately evaluated through the use of an integrated electrical test vehicle.

9049-57, Session 14

Field-theoretic simulations of directed self-assembly in cylindrical confinement: Placement and rectification aspects

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The directed self-assembly (DSA) of block copolymers has recently attracted a great deal of attention as a simple and cost-effective patterning tool for Vertical Interconnect Access (VIA) lithography. A major goal of VIA lithography is to produce high-resolution cylindrical holes with reduced critical dimensions (CD) relative to a cylindrical prepattern created with top-down lithography. In addition to hole shrinking, rectification and placement aspects are key features required for the success of DSA applications in VIA lithography, as it is of paramount importance that the shrunk hole have the right CD and be well located for connecting the various conducting layers joined by the VIAs.

In this study, we use field-theoretic simulations to investigate the fluctuations-induced variations in the CD and position of the PMMA cylindrical microdomain that forms in the middle of the guiding hole.

Our study goes beyond the usual mean-field approximation and self-consistent field theory simulations (SCFT) and incorporates the effects of thermal fluctuations in the description of the self-assembly process using complex Langevin (CL) dynamics. Using CL simulations, we therefore explore the properties of the formed PMMA cylinders, including fluctuations in the center and the size of the domain, for various prepattern conditions. A few snapshots of a fluctuating PMMA-density profile is shown in Fig.1.

In a parallel effort to study the placement of the PMMA domains, we also used a modified SCFT-based method that does not require complex Langevin dynamics. In this new scheme, an external chemical-potential-like field is applied to displace the PMMA cylinder away from its centered, lowest energy configuration. To retain the shape uniformity of the PMMA cylindrical domains, we chose a line potential that selectively attracts PMMA monomers uniformly along the height of the guiding hole. The location of the line sets a target for the shift or deviation of the PMMA domain away from its center position in the guiding hole. By tailoring the selectivity and the magnitude of the interactions between the monomers and the external potential, as well as the center line position of the potential, the PMMA domains are ‘’pushed” away from the center of the guiding hole. By comparing the free energy of the resulting shifted morphologies to that of well-centered structures, we can compute the energy cost associated with the displacement and the resulting equilibrium density of cylinders at a given location. Using our modified SCFT-based simulations, we report the variance of measured displacements for various prepattern CDs and compare to CL results.

The results of our simulations should inform about placement errors and rectification in the formed VIAs and ultimately assist in the design of guiding patterns and polymer formulations for the integration of DSA-based processes into VIA lithography.

9049-58, Session 14

Contact holes patterning by directed self-assembly of block copolymers: What would be the Bossung plot?

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Directed Self-Assembly (DSA) of block copolymers (BCPs) continues to attract significant interest as a promising patterning alternative to be used for the future CMOS technology nodes [1-3]. While in the conventional optical lithography, the process window (PW) of a printed feature (linewidth or contact hole) is well determined by the so-called Bossung plot, in the DSA this PW needs to be also identified in order to control such a lithographic process and know its capabilities.

In this work, we extensively investigate the PW of contact holes (CHs) generated by the DSA of PS-b-PMMA BCPs based on the graphoepitaxy approach. For the ‘’hole-in-a-hole” structure (also known as CH shrink), we plot the BCP critical dimension (CD) variation as a function of the guiding template CD (CDguiding) for various BCPs of different morphologies (lamellar and cylindrical) and different molecular weights. According to this plotting method, one can define the PW as the best CDguiding range and BCP characteristics (chemical composition and molecular weight) couple to produce the required CD within a specific tolerance. This PW is also discussed in terms of quantitative defectivity analysis and studied according to different process parameters such as the BCP film thickness and the self-assembly annealing.

In addition, our study highlights two interesting properties related to the use of BCPs for CH shrink. The first one deals with the BCP capability to absorb the CDguiding variation (i.e to have a wide range

of CDguiding latitude) as shown in Figure 1. So, it could be useful if one would like to correct poor CD uniformity induced by standard lithography tools. The second property points out that CH shrink is controlled by the commensurability between the BCP's natural period (L0) and the CDguiding. This allows us to predict in advance the required CDguiding for CH shrink just by knowing the L0 of the used BCP. In the same way, for relatively higher CDguiding, this commensurability seems to be also respected. Indeed, according to Figure 2, the sequence of morphological transition (one straight cylinder to multiple straight cylinders to concentric cylinders) depends on the ratio between the CDguiding and L0. These experimental morphologies are consistent with previous simulation studies carried on the confinement effect of BCPs inside cylindrical pores [4,5].

Finally, we also report a preliminary study on CH multiplication in elliptical guiding template. For a constant minor axis of the guiding template, we clearly show the transition from one contact to multiple contacts as the major axis increases. This transition is not really abrupt but rather marked by a change of the BCP contacts shape from circular to elliptical form (Figure 3).

BCPs used in this study are synthetized by ARKEMA under the tradename Nanostrength® EO [6]. The research leading to these results has been performed in the frame of the industrial collaborative consortium IDeAL.

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9049-59, Session 14

Influence of litho patterning on DSA placement errors

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Directed self-assembly (DSA) of block copolymers (BCPs) is currently being investigated as a complementary technique to lithography. The merits of DSA include shrinking of critical dimensions, pitch multiplication, contact hole repair and CDU reduction. However DSA is also facing critical issues like overlay and defectivity that need to be resolved. DSA is an additional process after the lithography step and previous work [1] has shown that BCPs are flexible materials adding a local overlay or placement error to the total overlay budget. Our paper focuses on the placement errors associated with DSA and how the mandrel shape generated by lithography influences that.

DSA was used to shrink the diameter of contact holes created by lithography from 50-80nm down to 15-30nm. We will report the experimentally determined placement error that the DSA process adds. The shrinking of these contact holes with DSA was also simulated by computer simulations based on Dynamic Density Functional Theory (DDFT), a self-consistent field theory method. For these simulations 3? placement error is determined. Good agreement between simulated and experimental placement errors was found.

Extensive DDFT simulations have been done for other several sizes of contact holes while systematically varying the ratio between the block copolymers (Figure 1a). These simulations show that the placement error is originating from the block copolymer itself and depends on the length of the block copolymer (Figure 1b). A simple mechanical model is used to explain the simulation results.

Finally, the DDFT results reveal the relation between confinement and placement error for double contacts (so-called 'peanut' shapes). Brion's computational platform TachyonTM was used to simulate and optimize through process window contours using 193i and EUV optical models. DSA simulations were then performed based on these through process window contours. It was found that the high-fidelity mandrel shape created by EUV resulted in a lower placement error and pitch variation than observed with the shapes created with 193i. We conclude that only EUV has the pattern fidelity to direct the self-assembly process.

9049-60, Session 14

Directed self-assembly patterning for sub-20nm half-pitch using conventional lithography system

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Directed Self-Assembly (DSA) process of block copolymers (BCPs) has been considered as a candidate for sub-20nm patterning. In recent years the semiconductor manufacturers have been interested in DSA usage in HVM. Many semiconductor manufacturers studied about CD rectification for contact hole and pitch multiplication for L/S. Last year, we published the paper about the CD uniformity improvement in CD rectification process, too. However there were no papers about contact hole pitch multiplication. Because the conventional lithography system cannot make contact hole pattern under 50nm pitch, this technology is very important.

DSA process is based on the intrinsic property of the BCPs which is phase-separation in the molecular scale. Therefore we can get the pattern of under 50nm pitch if we control the molecular which consist of BCPs. By using the conventional lithography system, we were going to make the hole pattern which have under 50nm pitch. If we succeed by using the conventional lithography system, there are some advantages that reduce the cost and become simple process.

So far, few companies have announced that it is possible to make contact hole patterns under 50nm pitch using DSA process. But their process was required the e-beam facility. Because their process need the small pre-pattern (equals to PMMA size), e-beam facility is essential part of their process. If we use e-beam facility for preparing pre-pattern, we will face some problems such as increasing cost, decreasing throughput, and etc. Therefore we decided to use conventional lithography system to make pre-pattern and PS-b-PMMA BCPs to make hole pattern under 50nm pitch.

In figure 1 shows that we can make the hole pattern under 50nm pitch using conventional lithography system and PS-b-PMMA BCPs. From the results, it is proven that conventional lithography system is possible to DSA process.

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9050-1, Session 1

CDSEM: Past, present, and future: from metrology to patterning diagnosis *(Keynote Presentation)*

Hiroshi Fukuda, Hitachi High-Technologies Corp. (Japan)

No Abstract Available

9050-2, Session 1

Addressing emerging challenges in advanced patterning, interconnect, and 3D device integration *(Keynote Presentation)*

Ofer Adan, Applied Materials, Inc. (Israel)

No Abstract Available

9050-3, Session 2

Optimizing hybrid metrology through a consistent multi-tool parameter set and uncertainty model

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There has been significant interest in hybrid metrology, a novel method for reducing overall measurement uncertainty and optimizing measurement throughput (speed) through rigorous combinations of two or more different measurement techniques into a single result. This approach is essential for advanced 3-D metrology when performing model-based critical dimension measurements. However, a number of fundamental challenges present themselves with regard to consistent noise and measurement uncertainty models across hardware platforms, and the need for a standardized set of model parameters. This is of paramount concern when the various techniques have substantially different models and underlying physics. In this presentation we will work through realistic examples using SEM, CDSAX, CDAFM and Optical CD methods applied to sub-20 nm dense feature sets. We will show reduced measurement uncertainties using hybrid metrology on 10 nm CD features fabricated using pitch quartering methods.

Hybrid metrology has recently been shown to directly improve measurement uncertainty introduced through parametric correlation and has further utility in selecting the correct minima among multiple nearby local minima in the fitting space. Here we show the ability to create a 3-D monolithic representation of a structure where the data reconstruction comes from independent measurements while other attributes are from combined data. The use of parallel regression and a priori information through Bayesian statistics entangles the measurement information even from those parameters or dimensions that appear orthogonal. We will explore different parametric combinations to arrive at the most comprehensive 3-D description while minimizing uncertainty through judicious choice of overlapping parameters. Those parameters that overlap provide integrated measurements for those overlapping variables while still influencing the quasi-independent parameters resulting in reduced uncertainties in all parameters. This approach allows the most flexible use of the different measurements to characterize a 3-D target yet also enables flexible strategies to enhance throughput.

When modeling measurements a library of curves is assembled through the simulation of a multi-dimensional parameter space. Although parametric correlation, measurement noise, and model inaccuracy lead to measurement uncertainty in the fitting process, fundamental limitations exist due to parametric correlations. Hybrid metrology provides a strategy to decouple parametric correlation and reduce measurement uncertainties. However, in the practical application of hybrid metrology amongst multiple tool platforms or models, it becomes essential to ensure a consistent overlap in the characterization parameters and the uncertainties. We will describe a new approach for using multiple tools or platforms that have intrinsically different modeling parameters to characterize the structures of interest. We will then develop a rigorous framework using a generalized parameter set that enables each independent measurement method to excel in that unique aspect of a measurement that it only can reveal yet provide a priori information that influences attributes in common.

One of the key challenges in quantitative hybrid metrology is utilizing consistent noise and uncertainty models across the different platforms. To address this underlying requirement we will develop a rigorous approach to systematic uncertainty evaluation applied across multiple tool platforms. The uncertainty analysis across the various measurement platforms must comprehensively address the systematic uncertainty components as well as accommodate uncorrected bias or systematic error in the regression-based fits.

9050-4, Session 2

Leveraging data analytics, patterning simulations, and metrology models to enable accurate CD metrology and patterning

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Integrated circuit technology is changing in many ways: 193i to EUV exposure, planar to non-planar device architecture, patterning through self-assembly, etc. Through all this, the critical dimension and process window are shrinking, and the CD control requirement is becoming more stringent. Three sigma CD control < 2 nm is required in complex geometries, and the associated metrology uncertainty required to achieve the target CD control for advanced IC nodes (e.g. 10 nm and 7 nm nodes) is < 0.2 nm. Reference or physical CD metrology is provided by CD-AFM, and TEM, but these techniques have inherent limitations; the accuracy of CD-AFM is ~ 1 nm, and the precision in TEM is poor due to limited statistics. Workhorse metrology is provided by CD-SEM, scatterometry, and model based infra-red reflectrometry (MBIR). These measurements need to be calibrated by reference measurements to ensure the accuracy of patterned CDs and patterning models. Precision alone is not sufficient moving forward. There are fundamental capability and accuracy limits in all the metrology techniques that hinder the success of advanced IC nodes. No single technique is sufficient to ensure the required accuracy of patterning.

There is a dire need to measure with < 0.2 nm accuracy and the capability does not exist. Being aware of the capability gaps for various metrology techniques, we have applied various predictive data analytics and data integration techniques to a few applications employing statistical, patterning, and metrology models to demonstrate the potential solution and practicality of such an approach for advanced nodes. Data from multiple metrology techniques have been analyzed in multiple ways to extract information with associated uncertainties, and integrated to extract the useful and more accurate CD and profile information of the patterns. One example is the need to accurately measure the CD of litho

trenches less than 40 nm wide relevant for EUV and FinFET patterning. AFM is not capable to measure sub-40 nm trenches with needed accuracy, and the CD SEM does not provide physical CD measurement. A feasible solution is to extrapolate the AFM data that can be measured with acceptable accuracy. However the uncertainty associated with extrapolation can be large and is a concern. In such case we have made use of measurements from CD-SEM, CD-AFM along with the patterning and scatterometry simulation models to estimate the uncertainty associated with extrapolation and methods to reduce it. The study lays out various basic concepts, approaches and protocols of multiple source data integration for hybrid metrology approach. Impacts of this study include more accurate metrology, patterning models and better process controls for advanced IC nodes.

9050-5, Session 2

New techniques in large-scale metrology toolset data mining to accelerate integrated chip technology development and increase manufacturing efficiencies

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Today, metrology toolsets report out more information than ever. This information applies not only to process performance but also metrology toolset and recipe performance through various diagnostic metrics. This is most evident on the Critical Dimension Scanning Electron Microscope (CD-SEM). Today's state of the art CDSEM reports out over 250 attributes and several images per measurement. It is not unusual for a state of the art fab with numerous part numbers to generate at least 20TB of information over the course of a year on the CD-SEM fleet alone. Most of this comes from improvements in throughput, increased sampling and capabilities like image analysis relative to previous generations of tools. Oftentimes, much of this additional information is useful for helping to determine if the process, metrology recipe or tool is deviating from an ideal state. Many issues could be missed by singularly looking at the key process control metric like the bottom critical dimension (CD) or a small subset of this available information. Looking at distributions rather than narrow specific data, a strong signal can be discerned out of the noise. Unfortunately making sense of all this information is very time consuming. Given the ever increasing and large amount of metrology steps in the product routes requiring recipes and the additional information mentioned, there is a large opportunity for developing techniques to manage all this information more effectively. This can result in driving down the mean time to detect and debug manufacturing issues, improving cycle-time, process capability and speed up development cycles of learning. We explore these opportunities through a joint project between Applied Materials and IBM. This paper highlights the new capabilities realized through this joint project. Numerous case studies will be shown describing how these capabilities helped improve manufacturing and development at IBM. We will conclude with industry recommendations.

9050-6, Session 2

Data fusion paradigms for next-generation CD metrology

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Next generation semiconductor devices manufacturing imposes to metrology tool providers an exceptional effort in order to meet the required targets of precision, accuracy and throughput stated in the ITRS. The challenge generates additional risks and cost for IDMs and foundries aiming ever better devices to ensure their economic viability.

Data Fusion is the Art of gathering, combining and processing heterogeneous data containing different level of information to produce the best measurements or decisions. For several years, Data Fusion for metrology, also named Holistic Metrology, Hybrid Metrology or Combined Metrology is considered has a must for next generation metrology methodologies. However, several paradigms are possible with various advantages and drawbacks, and no clear comparison has been reported.

In this contribution, we review different approaches and unify terms related to Data Fusion architectures, at different level of abstraction. These levels range from High Level Data consisting in CD individually measured on different tools to Deep Level Data consisting in internal parameters extracted during data processing. Depending on the challenge of the metrology, HVM fabs shall be able to switch effortlessly from one level to another.

We demonstrate the potential advantages to use Data Fusion at High and Deep Level on concrete examples dealing with sub-28 nm nodes metrology using scatterometry, CD-SEM, TEM and AFM technologies.

9050-7, Session 2

CD-SEM AFM hybrid metrology for the characterization of gate-all-around silicon nanowires

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In our ongoing study of physical characterization of Gate-All-Around Silicon Nano Wires (GAASiNW), we found that thin suspended wires are prone to buckling as a function of their physical dimensions, length and diameter. Buckling, which takes place between the fixed source and drain regions of the suspended wire can affect the device performance and therefore needs to be studied and controlled.

CDSEM measurements suggest that the onset of buckling in wires can be described by Euler's theory. This finding offers a mathematical representation of this phenomenon, proposing a way to predict at what SiNW dimensions, buckling may occur.

For cylindrical SiNW the theory predicts that buckling has no directional preference. However, 3D CDSEM measurement results indicated that cylindrical wires prefer to buckle towards the wafer. To validate these results and determine if the electron beam or charging is affecting our observations we used 3D-AFM measurements to to evaluate buckling.

To assure that the CDSEM and 3D-AFM measure the exact same locations, we developed a design based recipe generation approach to match the 3D - AFM and CDSEM coordinate systems. Measuring the exact same sites enables us to compare results and use 3D-AFM data to optimize CDSEM models.

In this paper we will present hybrid metrology characterization of GAASiNW for sub-nanometer variations, validating experimental results, and proposing methods to improve metrology capabilities.

9050-8, Session 2

Hybrid metrology universal engine: co-optimization

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Technology node shrink and increased device complexity continue to push the limits of existing metrology performance. In recent years Hybrid Metrology emerged as an option for enhancing the performance of

existing toolsets, and is sparking increased interest.

Hybrid Metrology is the combination of measurements using different toolsets, each toolset bringing its own strengths into the mix in order to enhance the overall performance of the result. Top-down linewidth measurements of CD-SEM provide good synergy to scatterometry (OCD) full profile measurements, as both measure line width, but in case of OCD the linewidth measurement can correlate with other profile details (not measured by CD-SEM). “Fixing” the linewidth to the correct value improves measurement performance of the remaining model parameters. This combination is currently implemented in production where the CD-SEM data is used to actively improve the spectral modeling of OCD.

One challenge of combining data from different technologies is matching of the common parameters. Inherent uncertainties in the “secondary toolset” (CD-SEM in this case) can transfer into the model of the “primary toolset” (OCD). Figure 2 illustrates one source of errors: percentage threshold analysis of gray-level contrast does not provide unambiguous indication of the height at which the linewidth is measured. CD-SEM is helping OCD, but who is helping CD-SEM?

The “Holy Grail” of Hybrid Metrology is the universal hybrid engine, an engine that can combine both processed data (results) and raw data (at modeling level) from any toolset. Co-optimization is another stepping stone in the path to the universal engine. Within the co-optimization framework different toolsets are actively helping each other, with common parameters optimized together in order to eliminate remaining ambiguities. It is worth noting that the optimal solution for both toolsets is different from the solution from each toolset by itself, or from the solution with standard hybridization from one tool to the other – owing it to higher measurement artifact rejection of the co-optimization solution. While “standard” hybrid adds processed data from secondary tool into the model of the primary tool (Figure 1a), co-optimization operates directly with the models of two or more toolsets. Co-optimization can benefit from a physical model-based analysis of images, but works even with currently available threshold-based models. This report introduces the co-optimization concept using a silicon fin height measurement (Figure 3) and High-k/Interfacial layer on Silicon fin as test vehicles (figure 4). Using 3-wafer design of experiments we compare the performance of individual toolsets with standard hybridization (CD-SEM helping OCD through line width measurements), and with the results of the co-optimization. The concept illustrated here is directly extendible to combination with other technologies.

9050-9, Session 3

10nm three-dimensional CD-SEM metrology

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The semiconductor industry is relentlessly moving toward the production of integrated circuits built with 10 nm or even smaller structures. Accurate and reliable imaging and measurements of these very small three-dimensional (3D) features have not been worked out well enough to fulfill the technology requirements. We are reporting here the results of successful 3D SEM measurements on close-to-10 nm 32 nm nominal pitch Si oxide lines that closely match the results of CD-SAXS and TEM measurements.

Nanometer-scale dimensional metrology at and under 10 nm scale is especially difficult because the key features of the samples might be comprised of only a few (dozens of) atoms, and the signals they generate are inherently very small. Insufficient spatial resolution, sample damage, and too large sample stage drift or vibration can prove to be prohibitive problems. These problems are significantly bigger for 3D measurements, so optimization of the measurements is indispensable. Especially for process control, it is important to know the quality and relevance of the measurement results, i.e., the confidence in the information gained by them. Measuring too little means loss of control, measuring too much means loss of efficiency, and both could cause significant loss of money and time. Using good measurement practices and physics-based modeled library method were equally important to be able to arrive at results presented here.

For image acquisition the SEM operating parameters were carefully optimized and a drift-compensatory method (qACCORD) [1] developed at NIST was used. At all measured locations of the wafer a large number of fast image frames were acquired with 100 ns pixel dwell time. These images were very noisy, but with qACCORD their centers were found to line up and add them together so that sample-drift-related blurring and distortions were eliminated to a large extent.

For the identification of the best matching 3D structure libraries generated by the NIST 3D Monte Carlo modeling method (JMONSEL) [2] were employed. At first a library of trapezoidal approximations was used and lead to useful results. Later a refined “shark fin” model was used that accounted for more 3D details of the sample. The SEM-determined mean profile matched the results of CD-SAXS and TEM measurements. The SEM results present nanometer-scale, site-specific size and 3D shape information, allow for the calculation of line edge roughness, and permit identification of locations where the integrated circuit structures were formed out of the boundaries of the intended size and 3D shape ranges.

The results of this study in our view prove that SEMs can deliver useful 3D information on 10 nm and probably even smaller structures. Further efforts are needed and some are already underway to explore the possibilities and to find production-worthy solutions.

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9050-10, Session 3

Metrology for FinFET sidewall roughness: A study of H2 anneal smoothening for mobility enhancement

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FinFETs are the best solution to scale the MOSFETs beyond 22nm [1] due to better gate electrostatics at aggressive channel lengths (Lch). However, aggressive fin pitch processing impacts the fin surface and makes it rough, thus affecting the device performance. This work focuses on regaining the lost performance by surface smoothening using H2 annealing, and measuring the effect with CDSEM and AFM.

H2 annealing of SOI finfets [2] under high temperature and pressure is done which smoothens the fin surface (Fig 1). Optimization of the H2 annealing condition is important as it can drastically change the fin shape due to fin etching and Si atom migration [3]. In this work careful process calibration is done to obtain the desired fin shape for reduced surface roughness and better gate control.

AFM and CDSEM were used to quantify the fin sidewall roughness. For AFM the CD measurement mode was used allowing dynamic change from tapping vertically on flat surfaces to dithering horizontally on the sidewalls (Fig. 2a). For CDSEM, the line edge roughness (LER) of both the top and bottom of the fins were measured. A comparison (Fig. 3) of ten different conditions shows good correlation between the two measurements. While the CDSEM is faster and is a non-contact measurement, the AFM is the more direct measurement of the sidewall. Here we focus on the AFM measurements [4] and four of the ten samples on which electrical testing was done.

The roughness information is fitted to an exponential power spectral density using the method of [5, 6]. The roughness is characterized by the root-mean-square (Δrms) and correlation length (?rms) [6]. The Δrms reduces by ~25% with H2 annealing suggesting smoother fin surface compared to the control Si finFET (Fig. 3). Theoretical calculations of surface roughness scattering (SRS) limited hole mobility (μh) in finFETs [7] (Eq.1 in top panel in Fig. 4) show that ?rms has a much larger impact on mobility compared to λrms (Fig. 4). Theoretical calculations suggest that ?rms reduction from 0.24nm (experimental Δrms for control Si finFET) to 0.18nm (experimental Δrms for H2 annealed Si finFET) improves μh by

~7% at an inversion charge density (Qinv) of 1e13/cm2 (Fig. 4b).

In summary, an effective process for improving the fin surface quality is reported using a high temperature and pressure H2 annealing process. The improvement is quantified with both CDSEM LER and sidewall AFM, which strongly correlate, and the effect is observed in electrical measurements.

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9050-11, Session 3

Addressing FinFET challenges in 1Xnode by image-based 3D metrology using CD-SEM tilt beam

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As Moore's Law continuously drives IC performance forward, key challenges for fabrication are shrinking device dimension and increasing complexity of device geometry in all three dimensions. Along with such fabrication needs, traditional metrology is facing challenges to enable more accurate, intricate three-dimensional measurement such as sidewall angle, profile, spacer widths, spacer pull-down, footing/undercut, etc.

Traditionally Scatterometry/Optical critical dimension (OCD) technique, and occasionally Atomic Force Microscope (AFM), has been used to characterize such three dimensional applications in-line. OCD, possessing a wide range of metrology capability and tight precision, suffers from prolonged model development time in the initial state, and the developed model can be very sensitive to process variation, which is inevitable when a new fabrication technology is in the stage of development or ramping up to production. AFM, although is not modeling based, yet is intrinsically limited by the dimension of the physical scanning tip, which becomes a more prominent limitation as device dimension shrinks. At 1X technology node, the design of the FinFET structure takes advantage of the 3D metal gate, which poses a tremendous challenge to metrology for advanced process control. In order to fill this metrology gap in the R&D stage of 1X node, a tilt beam perspective has been added to a conventional top-down CD-SEM to enable three-dimensional measurement. Benefiting from the tilt beam feature and in-situ image-based analysis, the measurement setup time and process time can be theoretically dramatically shortened compared to other modeling-based metrology.

The deployment of the 3D CD-SEM tilt beam metrology to ramp-up stage and further to high-volume production (HVM) stage has two phases: phase 1, proving of viability in terms of accuracy, precision, and sensitivity challenged by 1X technology node; phase2, proving production worthiness on tool qualification and inline wafer monitoring. Currently we are implementing phase 2.

In this paper, 3D tilt beam metrology methodology will be presented with a specific showcase in measuring sidewall angle and spacer height on a FinFET device to help monitor and control 14nm gate height in-line. Two angels of tilt beam (low tilt 5?, high tilt 14?) have been calibrated on a CD-SEM to obtain two sets of images where measurement was performed to calculate sidewall angle and height. Strong correlation with TEM ranging from 0.89 to 0.998 has been demonstrated in measuring height of different FinFET structures. A best height measurement precision of 1.42 nm has been achieved. Sensitivity to DOE wafers and within wafer variation will be demonstrated. SPC charts of inline wafers will be shown to demonstrate production worthiness. Further, we will present the daily qualification data (precision & matching) of CDSEM fleet for this specific application.

We will also discuss current limitations of the 3D Tilt Beam metrology in terms of height precision and applications. Future work includes improving calculation model based on specific applications, developing new applications such as FIN Height, coupling with OCD to provide a more comprehensive measurement for 3D fabrication.

9050-12, Session 3

Novel three-dimensional (3D) CD-SEM profile measurements

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The 22 nm node [1] marked the beginning of a major transition from conventional scaling-driven planar devices to complex 3D transistor architectures, redefining future needs for lithographic metrology solutions for high-volume manufacturing (HVM). Evaluation of CD, roughness and other parameters in fin field-effect transistors (FinFET) [2][3][4] raises new metrology challenges, as the entire 3D structure becomes critical for process control, including fin and gate dimensions, profiles, roughness, and undercuts. Similarly, future 3D memory devices will include multiple gate-level structures defined by high-aspect ratio (HAR) trenches and holes in multilayer stacks—all of which are major gaps in current metrology technology [2][3][5]. At 1D or 2D level control, CD-SEM and OCD (Scatterometry) techniques are standard measurement tools in IC wafer production, and this is still true for CD of lithographic, hard mask and other planar features. However, for process control of 3D devices, both conventional topdown CD-SEM and OCD are not sufficient and have intrinsic limitations. Conventional topdown CD-SEM, an image-based technology which is sensitive to discrete features, CD variation and roughness, is insensitive to profile. Vice-versa, OCD, a scattering-based technology, is sensitive to profile, but must use a specialized grating target, and is incapable of measuring discrete features, CD variation or roughness. CD-AFM is generally employed for such 3D profile information, but this technique has its own limitations for 1X node production due to tip size constraints in the tightest spaces, and due to finite tip lifetime which can influence measurement stability [3].

However, to address these gaps, Advantest, long a supplier of reticle SEMs, has developed a wafer-capable MVM (Multi Vision Metrology)-SEM that can address these issues by supplying a novel image-based 3D measurement method. Using patented multi-channel detector technology [6], this system can acquire information of surface concave and convex features and relative SWA and height quickly and non-destructively for nanoscale structures such as finFETs, using electron beam technology with its well-known long probe lifetime and stability and small probe size.

In this work, we will explore the capabilities of this new technology with the SEMATECH CD-SEM specification [7]. Quantitative 3D metrology capabilities will be demonstrated on FinFET features, top corner rounding, LER and SWR will be shown on photoresist and hardmask features, and 3D evaluation of hardmask strip residues will be shown. These values will be correlated to CD-AFM reference metrology [8]. Furthermore, we will show how applicable MVM SEM is to EUV resist profile metrology.

9050-13, Session 3

Metrology and 3D shape process monitoring of HAR features using TSOM method

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In-line metrologies currently used in the semiconductor industry are being challenged by the aggressive pace of device scaling and the adoption of novel device architectures. Critical dimension (CD) metrology of high aspect ratio (HAR) features such as trenches or contact holes will become more challenging as technology progresses, particularly in memory applications where designs are evolving from planar to vertical architectures with multi-level gates assembled in 3D structures. From the process control perspective, CD metrology entails control of top CD, bottom CD, profile and detection of residues, which introduce a new set of gaps in metrology capability, since current non-destructive metrology techniques lack the sensitivity and resolution to characterize such features. Moreover, the physics of these measurements are hindered by the extremely deep and geometrically confined volumes involved. Charged particle-based imaging techniques such as CD scanning electron microscopy (CD-SEM), and helium ion microscopy (HeIM) have sensitivity limitations arising from sidewall charging, as only a small fraction of scattered particles ultimately reach the detector.

The limitations outlined above prompt the need for alternative non-destructive metrology methods that can achieve sensitivity at the nanoscale while maintaining throughput compatible with high volume manufacturing. In light of this, optical techniques are desirable. In this paper we extend the application of the through-focus scanning optical microscopy (TSOM) method for 3-D shape analysis of HAR targets, especially for inspection and process monitoring applications. Both simulations and experimental results are presented. Simulation results of trenches and holes down to the 11 nm node indicate that the sensitivity of TSOM may match or exceed the ITRS measurement requirements for the next several years. Experimental TSOM measurements were compared with 3-D shape measurements done using focused ion beam.

Measurements were done using a 300 mm wafer with HAR targets of about 1.1 μm deep in a Si oxide layer. It is expected that variations in feature structural parameters will exhibit a signature induced by processing conditions: a radial signature imparted by etch rate variations across the wafer, and a horizontal signature imposed by variation of lithography exposure conditions as shown in the background circle of Fig. 1. In summary, the differential TSOM image patterns and the OIR values were found to vary radially both in the vertical and horizontal directions, approximately matching the fabrication conditions and expected signature as shown in Fig. 1. These results demonstrate that TSOM can identify process variations across the wafer.

The ability of the TSOM method to analyze an array of HAR features or a single isolated HAR feature is also presented. This allows for the use of targets with area 300 times smaller than that of conventional gratings, saving valuable real estate on the wafers. The simplicity, low-cost, small target size, high throughput, and nanometer scale 3-D shape sensitivity of the TSOM method make it an attractive inspection and process monitoring solution for nanomanufacturing.

9050-14, Session 3

Metrology of white-light interferometer for TSV processing

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According to Moore's law, the number of transistors in an IC chip has been doubled every 2 years, and it has been the most powerful driver for development within the semiconductor industry. This law focuses on lithography scaling and the integration of all functions on a single chip, but it is expected that this scaling technology would reach a fundamental limit. To break through the limit, 3D integration technology has been a good alternative to achieve the integration of all functions. 3D integration technology allows for a single integrated circuit, built by stacking wafers and/or dies and interconnecting them vertically so that they behave as a single device.

TSV (Through Silicon Via) is one of the most important technologies in 3D IC integration. TSV is a rapidly developing technology that utilizes short, vertical, electrical interconnections or vias that pass through a silicon wafer, in order to establish an electrical connection from the device side to the backside of a die. This provides the shortest possible interconnect path, and creates an avenue for highly efficient 3D integration. TSV technology can give greater space efficiencies and higher interconnect densities than wire bonding and flip chip stacking. TSV technology also enables a higher level of functional integration and performance in a smaller form factor. Throughout TSV processing, measurements for all TSV processing steps are important in post-etch, and all follow-up processing to check status of TSV.

White light interferometry (WLI) has been used for the measurement of topography, step height, and via depth, using its short coherence length. The nanometer level resolution of this technique is ideal for TSV measurements in the high aspect ratio vias.

In this paper, we will discuss the important measurement steps of 20nm TSV processing using a white light interferometer system and the relation of these measurements to TSV processing.The TSV depth and width dimensions used for this research are 55um and 6um, respectively. Fig. 1 shows the steps we have measured using WLI system. We have measured 6 critical TSV processing steps. 1) Post TSV etch: depth, top CD (TCD) and bottom CD (BCD), 2) Post TSV liner and 3) Post TSV barrier seed: BCD, 4) TSV Electro-Chemically Plated (ECP) copper and 5) Post annealing: step height of bumps 6) TSV CMP: dishing measurement.

These measurement steps have been implemented inline for advanced technology node TSV process flows at GLOBALFOUNDRIES. Figure 2 illustrates current inline data trends for TSV depth and bottom CD.

In this measurement: we have evaluated a wafer map for processing that includes the wafer center and edge area. We have measured 10 times at 13 sites to check repeatability. We have >90% correlation with reference measurement tools, such as cross section SEM for TSV and bump measurement, and AFM for dishing measurement. We had < 0.5% repeatability data for each step's measurement. All details will be provided in full throughout this paper.

9050-15, Session 4

Influence of metrology error in measurement of line-edge roughness power spectral density

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Control of roughness in photoresist and post-etch features has become more important as features continue to shrink. However, the need for control is accelerating; with planar CMOS, the roughness of the bottom edge defines a transistor's effective width, whereas with our contemporary FinFETs and TriGates, the roughness of the entire sidewall acts as the active surface for these non-planar transistors. Metrology studies have gradually improved our ability to measure roughness, but as we approach the 10 nm node, sub-nanometer roughness control will be required, with metrology error decreased to a mere 20% of that, i.e. approaching size ranges that can be described as atomic scale. Achieving such uncertainty levels will be quite challenging.[1][2][3]

The current SEMI standard for line-edge roughness (LER) and linewidth roughness (LWR) measurement [4] specifies the sampling intervals and

length, as well as the roughness amplitude metric in terms of a standard deviation. While this standard was, at the time, a very important step in the right direction for guiding the industry towards compatible and consistent measurements that reflected industry requirements, more information is needed for fully characterizing roughness, particularly the various spatial frequency characteristics. LER and LWR in lithography are best characterized by the power spectral density (PSD) of the roughness, or similar measures of roughness frequency and correlation. The PSD, in turn, is generally thought to be described well by three parameters: the standard deviation (RMS roughness), correlation length, and roughness exponent. A thorough theoretical study of these metrics was recently published by one of the coauthors [5][6]. The next step towards enabling these for pertinent industrial use is to understand how real metrology errors interact with each of those metrics, and what should be optimized on the CD-SEM to improve the error budgets. Another previous work introduced the idea of the uncertainty of a single edge location as being a fundamental building block for how metrology error influences various CD and LER metrics [7][8], and this edge uncertainty, sigma-e, is also directly related to the LER bias [8] and to the integral of the high frequency noise floor through the entire frequency range of a given measurement.

In this work, JMONSEL simulation [9] is used to better understand how various SEM parameters, beam size/shape, and sample profile influence sigma-e and also some of the systematic shifts in edge location assignment. These results can then be input into previously-presented random edge roughness generators and solvers [6][10] and iterated to generate the expected error responses in the various proposed roughness metrics. From this, we can better understand what SEM optimizations are important for actual use of these proposed roughness metrics.

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9050-16, Session 4

Monte Carlo simulator of resist shrinkage in SEM metrology

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Resist lines change their shape and size under the electron beam, causing resist shrinkage in CD-SEM, which creates systematic errors in semiconductor metrology.1 In fact, the results of the CD measurements correspond to the resist pattern that is left after e-beam irradiation, while it is of interest to know the CDs before the SEM image was taken. Understanding the dynamics of the shrinkage, optimizing CD-SEM conditions to minimize the shrinkage, and predicting shrinkage for specific resists and SEM setups is necessary.

In this paper, we describe a 3D simulator of resist shrinkage. A commercially available Monte Carlo simulator, CHARIOT, was upgraded to handle shrinkage modeling. The software is a comprehensive simulator of SEM images using the Monte Carlo method; it involves advanced models to simulate slow and fast secondary electrons in 3D samples, charge and discharge, electrical fields inside and outside the sample, trajectories of primary and secondary electrons in these fields, as well as the geometries and properties of the detectors.

In shrinkage modeling, the 3D target is dynamically reconstructed while the electron beam continues scanning over the target. The changes in the resist shape depend on the resist properties, e-beam voltage and current, and dose and scanning parameters of the beam. The distribution of the absorbed dose is accurately simulated in the resist volume and is dynamically updated as the irradiation proceeds and the shape changes according to the dose distribution. The dose simulation takes into account the geometry of the target, including the influence of the neighboring features on electron scattering. The surface tension is also taken into account as a significant factor. The simulation results for a 3D shrinkage model of a resist line, a post, and a contact hole are presented. The results are compared to known experimental data; the simulations reproduce the experimental data well.

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9050-17, Session 4

A new integrated Monte-Carlo code for the simulation of high-resolution scanning electron microscopy images for metrology in microlithography

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Monte Carlo (MC) simulation codes for the reconstruction of secondary electron (SE) images in scanning electron microscopy for metrology applications require a very accurate description of the geometry of arbitrary resist structures. In spite of the fact that real samples are complex three-dimensional volumes with heavily textured surfaces, the main available simulation codes are often limited to the use of basic body geometries, since they have to keep within practical limits the computation time required by the MC engine. In the paper, an original MC code (Integrated Electron beam Simulator, IES) is presented, which uses unstructured tetrahedric meshes to define 3D sample geometries in the sub-nanometer scale to account among other for irregular shapes and their roughness. In the proposed approach, the geometries used within the MC code can be either generated manually by the structure editor of a TCAD tool, or imported from a process simulator. The overhead in computing time resulting from models including 200,000-500,000 tetrahedra does not exceed a factor of three compared with that needed by similar structures defined by basic shapes. This is achieved thanks to the use of the hierarchical structures and efficient parallelization schemes

for high-performance computing.

Besides the proper definition of the geometry, IES includes an accurate description of the physical interactions leading to the formation of a SE image, which is based on a multiple collision scheme combined with a powerful particle tracking algorithm, and original models for the different materials especially optimized for low electron beam energies (< 500 eV). Charge trapping in isolators during irradiation is calculated at the same time as the SE. Post-processing by a device simulator provides the final spatial distribution of the trapped charge (resulting from drift-diffusion), as well as the local electric field obtained by solution of the Poisson equation in the vacuum chamber and in the sample materials with particular emphasis on space-charge induction in semiconductors. Therefore primary and secondary electrons can be tracked with a high spatial accuracy in the electro-magnetic field up to the detectors, in particular in the close vicinity of sharp resist edges. An additional parameter, which is calculated, is the local dose arising in the sample due to the energy deposited during every single electron scattering event. This feature in combination with the accurate description of the sample geometry through a tetrahedric mesh in the nanometer-scale yields a first estimate of the local 3D local dose distribution to be used as an example for the simulation of the proximity effects in intricate resist structures deposited on the top 3D substrates, as well as the local heat generation during e-beam irradiation.

In the first part of present paper, the IES tool is first applied to simulate SE linescans and SE images of photoresist models generated by mesoscale models. In the second part, IES is used to calculate the point spreading function of an electron beam impinging on different photoresist layers and substrates, as well as to expose phoresist structures, which are successively imaged by SEM simulation.

9050-18, Session 4

Correction of EB-induced shrinkage in contour measurements

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Immersion-ArF lithography will remain a major technology for mass production of semiconductor devices for several years owing to the postponement of the launch of EUV lithography. Thus, extremely fine patterns whose pitch is less than the half wavelength should be resolved. The multiple-pattering technique drives the scaling of simple patterns in memory devices. Meanwhile, the strong OPC is inevitable to resolve the complicated small patterns in logic devices. The OPC modeling process requires accurate contour measurements of two dimensional resist patterns. The only available instrument for contour measurements is a CD-SEM. However, it is well known that the electron beam (EB) irradiation during image-acquisition induces shrinkage of the resist patterns. In other words, the measured contours are “shrunk contours”. Although the conventional OPC with shrunk contours showed no serious contradiction thus far, we expect that the shrinkage correction would improve the accuracy of the contours and thus shorten the modeling time. For this reason, we developed a model-based shrinkage correction method.

The shrinkage correction procedure is made of 4 steps. First, the shrinkage of calibration patterns is measured to calibrate the shrinkage model, which takes into consideration the elastic nature of the resist shrinkage. Second, the SEM image of two dimensional patterns is acquired and the shrunk contour is extracted. Third, the shrinkage vectors (amount and direction of shrinkage of each edge point on the shrunk contour) are calculated by the model. Finally, the original contour is reconstructed by subtracting the shrinkage vectors from the measured shrunk contour.

We applied this method to ArF resist patterns. Line patterns were used for model calibration and elbow patterns were used for validation of the method. For both patterns, SEM image acquisition was repeated 16 times on the same field of view. Then, we extracted the slightly shrunk contour from the first image (the first contour) and the well-shrunk contour from the last image (the last contour). The shrinkage of the line patterns, which was measured by the difference between these two contours, increased as the CD increases and saturated for lines wider than about 90 nm. The shrinkage model was calibrated on the basis of the results to reproduce this CD-dependence of the shrinkage. With the calibrated model, we reconstructed the first contour of the elbow patterns from the measured last contour. The reconstructed contour was found to be consistent with the measured first contour. For example, the small shrinkage at the inner corners (1.5 nm) and large shrinkage at the outer corners (3.5 nm) were correctly reproduced. Quantitatively, the root-mean-square error of the reconstructed contour was 0.5 nm. Therefore, this method is a good approximation of shape change of the two-dimensional patterns due to shrinkage.

In summary, we proposed a model-based correction method of shrinkage in contour measurements. This method reconstructs the original contour from the measured “shrunk contour”. The application of this method on the elbow patterns showed that the calculated shrinkage was consistent with the experimental result. The shrinkage correction in contour measurements will contribute to the fast and accurate OPC modeling.

9050-19, Session 4

Dependence of secondary-electron yield on aspect ratio of several trench patterns

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Recently, semiconductor logic and memory devices are switching from a 2D planar structure to a 3D structure. Forming these complex structures requires sophisticated process control and metrology for high-aspect-ratio (AR) structures. In regard to CD-SEM metrology, many of the secondary electrons (SEs) generated at the bottom of a high-AR structure hit sidewalls. Thus, contrast of the SEM image at the bottom is degraded. To improve contrast of the SEM image, it is important to systematically understand SE emission in the case of a high-AR structure. However, predicting SE emission in the case of a high-AR structure such as the bottom of a trench or hole presents several challenges because SE emission from the bottom is a very complicated phenomenon; in particular, SE generation and reflection at sidewalls should be considered. In light of these issues, SE emission from the bottom of a trench was investigated by measuring contrast in SEM images of samples with different ARs.

To investigate SE emission in the case of a high-AR structure systematically, trench patterns with AR between 0.5 and 8 were fabricated. Top-view SEM images were acquired by CD-SEM at landing energies of primary electrons (PEs) of 300, 800, and 1600 eV. SE yield and contrast-to-noise ratio (CNR) between the signal intensities for Si and SiO2 at the bottom of a trench were calculated from signal intensity for a selected area in the top-view SEM image. CNR is defined as the differential signal intensity for Si and SiO2 divided by the standard deviation of the signal intensity in the selected area. Dependence of CNR on AR was measured. CNR increases with decreasing landing energy of PEs. This increase comes from the difference between the landing-energy dependences in the cases of silicon and SiO2; that is, yield of silicon increases with decreasing landing energy, whereas yield of SiO2 stays constant below 800 eV owing to a positive charging effect.

To elucidate the behavior of SEs inside a trench, a Monte Carlo (MC) simulation on the signal intensity for silicon was performed by using MC simulation software, namely, CHARIOT. The experimentally measured signal intensity for Si, which is related to SE yield, was compared with the MC-simulated signal intensity. The measurement and MC simulation results are clearly different for AR over 5. The reason for this difference is assumed to be the effect of reflection of SEs at the sidewall, which is not included in CHARIOT. To verify this assumption, the reflectivity of SEs at the sidewall was calculated by applying a simple quantum-mechanical model. In this model, reflectivity is written as a function of SE energy, incident angle, and electron affinity. The model-based calculation confirms that the simulation taking into account sidewall reflection gives a better agreement with the experimental measurements than the

simulation not taking it into account.

In summary, dependence of SE yield on AR for several trench patterns was investigated. The investigation results show that reflection of SEs at the sidewalls is essential for understanding the behavior of SEs inside a high-AR structure.

9050-20, Session 5

Determination of line edge roughness in low dose top-down scanning electron microscopy images

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The determination of Line Edge Roughness (LER) becomes increasingly important as the semiconductor devices decrease in dimensions. Recent models have improved the LER analysis by taking into account the noise level of the equipment [1]. In this paper we analyse (1) the effect of Gaussian filtering on the high-frequency content of the edges and (2) the problem that experimental images of line edges can have intrinsic rotation.

In general, the peak detection of line edges in raw experimental images follows after applying a filter in order to reduce the noise content of the image. The strength (or spatial width) of this filter balances the signal-to-noise ratio with the high-frequency content of the edges. Choosing a very weak filter hardly improves the signal-to-noise level, but leaves the high frequency information on the line edge roughness intact. On the other hand, if we choose a very strong filter then the signal-to-noise level improves at the cost of destroying the high frequencies of the edges. The optimized filter, which balances the noise level for peak detection while maintaining the high-frequency content, is somewhere in between. We therefore developed a method for optimizing the strength of the filter, such that it has the lowest influence on the high-frequency content while ensuring that the peak detection is consistent and unambiguous for all edges in an experimental image. The method increases the strength of the filter step by step and checks the topography of the detected edges.

The inclusion of intrinsic rotation in experimental images of line edges affects the 3-sigma value, no matter how sophisticated the line edge roughness analysis. We show, by eliminating the rotation using orthogonal regression, that the 3-sigma value of 2.7 micrometer line edges increases already by 2 nanometer for rotations of order 0.1 degree. The power spectral density of the line edge roughness reveals that the significant contributions from the rotation are found in the lower frequencies of the spectrum.

Adaptive Gaussian filtering and the elimination of rotation using orthogonal regression yields a more accurate measurement of the power spectral density and corresponding 3-sigma value of line edges.

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9050-21, Session 5

Cross-sectional profile prediction from top-view SEM images based on root-cause decomposition of line-edge roughness

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This paper introduces a method for predicting cross-sectional profiles of topographic features from high resolution top-view SEM images. We show the effectiveness of the method in sub-20-nm node, where both structural topography and geometry variations are critical challenges for metrology.

Basic concept of our approach is to predict the local slope angle of topography from how surface roughness (morphology) looks in top-view SEM images. To quantify the surface roughness of topographic features, careful analysis has been made on line edge roughness (LER) obtained from top-view SEM images, and it revealed that LER (standard deviation: s) is decomposed into four components as,

$$s^2 = s_{shift}^2 + s_{figure}^2 + s_{morphology}^2 + s_{noise}^2 \quad (1)$$

where s_shift, s_figure, s_morphology, and s_noise are variations caused by parallel shift along the x-axis (direction normal to the edge) of the nominal profile, by cross-sectional shape deformation (figure error), by surface roughness (morphology), and by SEM image noise, respectively. We'll show that the each component in (1) has its own specific spatial distribution and power spectrum density (PSD) in real and spatial frequency domains, respectively, enabling us to decompose the measured LER into the four components and to extract each of them.

As practical procedures, plural pattern edges are extracted with varying threshold levels T in top-view SEM image and PSD is obtained for each of them. Here, we clearly see that each spectrum is decomposed into three components, a 1/f component over wide spatial frequency range, a peak in middle spatial frequency range (fpeak ~ 0.02 nm-1), and a peak in high spatial frequency range (fpeak>0.1 nm-1). We assume that these three components correspond to s_shift, s_figure, s_morphology, respectively. Because detected edge position along the x-axis is scanned with varying T, these components are obtained as functions of x. Here, the surface roughness component s_morphology corresponds to the projection of surface roughness onto the substrate plain, and thus contain information on local slope angle of pattern surface. As a crude approximation, we used following model for predicting local slope angle Q from s_morphology,

$$s_{morphology}^2(x) = L^2 \cos^2 Q(x) + H^2 \sin^2 Q(x) ,$$

where L and H are the statistical representatives for the periods and amplitudes of surface roughness.

The cross-sectional profiles Z(x) are predicted as,

$$Z(x) = [\text{integral}] \tan Q(x)\, dx.$$

The method was applied to several samples such as 50-nm width resist patterns and sub-20-nm width etched features. Reconstructed cross-sectional profiles showed good agreements with the results obtained by other metrology methods such as an atomic force microscope.

Top-view images captured in CD-SEMs have widely been used in the semiconductor industry because of their high accuracy and resolution capability. CD-SEMs use secondary electron intensity profiles for measuring CD and then use spatial variations in CD for measuring LER. Now, we use spatial variations in LER for predicting topographic profiles, fully utilizing the advantages of high-resolution CD-SEMs.

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9050-22, Session 6

Metrology for directed self-assembly block lithography using optical scatterometry

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Many research efforts are investigating the manufacturability of block copolymer directed self-assembly (DSA) for advanced lithographic patterning. It is well recognized that DSA performance and defectivity levels are closely related to parameters such as the pitch multiplication, underlying pre-pattern pitch, guide stripe critical dimension (CD), variation in chemistry of guide stripe/background materials and block copolymer film thickness(1). Accordingly, DSA lithography will require advances in CD metrology but most importantly will also require additional high speed techniques for evaluating defectivity. In this work,

we report on a study of Mueller Matrix Spectroscopic Ellipsometry (MMSE) measurements of 28nm pitch DSA line/space patterns consisting of polystyrene-block-polymethylmethacrylate (PS-b-PMMA). Block copolymer sample was fabricated using a chemical epitaxy process(2). Generalized ellipsometric data (all 16 Mueller elements) was collected over a spectral range from 245 to 1700 nm for various different pre-pattern pitch/guide strip CD combinations created by modulating the pre-pattern photoresist CD (i.e. focus-exposure-matrixes). Scatterometry models were used to evaluate and calculate the CD, line shapes, and thicknesses of the plasma developed PS patterns (PMMA removed.) Likewise, spectral comparisons based on anisotropy and depolarization were used to determine the sensitivity of ellipsometry to DSA pattern defectivity. SEM metrology comparisons were also carried out. The impact of pre-pattern pitch and pitch multiplication on block copolymer CD and defectivity and the effectiveness of MMSE as a technique for defect and CD measurement at DSA dimensions will be discussed.

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9050-23, Session 6

Novel metrology methods for fast 3D characterization of DSA patterns for high-volume manufacturing

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One of the major challenges associated with insertion of a DSA (Directed Self-Assembly) patterning process in high volume manufacturing(HVM) is finding a non-destructive, yield-compatible, consistent critical dimension (CD) metrology process. Current CD SEM top-down approaches do not give the profile information for DSA patterns, and profile is paramount in determining the subsequent pattern transfer process (etch). The low contrast difference between the alternate lamellar patterns makes the situation even more complex for cross-sectional characterization. DSA profiles can vary markedly along the thickness. Bridging, for example at the bottom, could not easily be detected from the top. There is, therefore, an urgent need for a method that is sensitive to the two phases along the entire profile. There are efforts ongoing to capture cross-sectional images of DSA patterns using techniques such a soft X-ray. But the correlation of top-down image with cross section still remains a major challenge.

SEMATECH, in cooperation with some of the major players of the metrology and DSA materials supply chain, has led an effort to solve the above discussed metrology issues in DSA. We will discuss several techniques developed in this endeavor and how they could potentially be used in an HVM environment to evaluate the robustness of DSA patterns prior to any etch.

One of the techniques we discuss is a scatterometry-based method that attempts to track DSA yield on a full wafer scale. DSA patterned wafers were made by a chemo-expitaxy method using guide patterns exposed in a focus exposure matrix (FEM). Based on optical inspection and knowledge of the guide pattern separation due to FEM, the 'non-yielding" dies are marked in red and the good dies are marked in green as shown in Figure 1. Figure 2 shows a scatterometry model calibrated with 'good' DSA patterns and applied to the entire wafer and it shows that scatterometry prediction aligns well with the yielding dies. Figure 3 shows prediction of bridging based on a calibrated scatterometry model, and it indicates a potentially much thicker bridging on the right side of the wafer, which also tracks well with the initial yield map of the wafer.

We also evaluate the possibility of using top-down SEM to be able to a detect bridging signature. Initial modeling was done to optimize SEM parameters to enable such a technique. Fig 4 shows, for example, the optimum voltage needed in a system of PS-PMMA for best contrast for different length bridging of PMMA under PS. We discuss the verification of such simulation on wafer data.

In summary, we have developed and evaluated several techniques that are potentially very attractive in determining DSA pattern profiles and embedded bridging in such patterns without resorting to destructive cross-section imaging. We show how such processes could be fine-tuned to enable their insertion for DSA pattern characterization in a high volume manufacturing environment.

9050-24, Session 7

Estimating pattern sensitivity to the printing process for varying dose/focus conditions for RET development in the sub-22nm era

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Optical lithography has been for decades the principal method for printing nanoscale semiconductors. However, as the industry keeps on shrinking the feature size while not modifying the 193nm lithographic wavelength, variability of the printing process has become more and more critical. To address these issues, Resolution Enhancement Techniques (RET) have been developed such as Optical Proximity Correction (OPC). However, analysis of mask patterns sensitivity to process parameters variability has been very limited until now, while being very important in order to give feedback to these RET. The main relevant approaches have taken two different directions: the first is to work directly on the Critical Dimension (CD) to improve the simulation model ([1], [2]); while the second uses contour extraction from microscope imagery (SEM) of printed wafers to compare it to simulated data ([3]-[7]). Both these approaches suffer from drawbacks however. They heavily rely on the simulating model to compare their results to, and the resulting metric is very pattern-dependent, making difficult the effective comparison between patterns across dose/focus conditions, or within same dose/focus conditions.

In this work, we demonstrate how we can use microscopy images of printed wafer patterns with different dose/focus conditions to evaluate the variability of the printing process in such a way that it does not rely on simulation models, and allow comparison between patterns or printing conditions. We first show how image analysis can be used to recover the printed shape of a pattern by mixing Watershed ([8]) and Random Markov Field techniques. Using the target mask shape as a prior, we attain efficiently an accurate representation of the above printed shapes from the microscopy images. Then, by comparing the obtained printed shapes with the target mask shape, we can measure shape differences through a normalized error metric (EM). This error metric is based on morphological analysis of the target shape, extracting the topology and characteristics of the target to compare it to the extracted contour. We reduce corner effects by manipulating L-∞, L-2 norms. The resulting shape difference is measured on a normalized scale from 0 (perfect "match" between target and extracted contour) to 1 (printing failed). Finally, we use the obtained values to fit a statistical model with varying mean and variance according to the dose/focus conditions. This gives us access to two kinds of possible printing variabilities: across printing conditions or for a given dose/focus situation (across measurements). Furthermore, the normalization of the error-metric allows comparison between target mask patterns, to evaluate which are the most sensitive to variations. The method can be used in the RET determination phase and in both sample plan generation and SEM images filtering phases of the OPC calibration process.

Experiments have been performed on a set of 15'000 images divided in ~140 (23 FEM conditions x 7 measurements) images for each of a set of 93 different patterns. Figure 1 compares our results with the traditional CD measurements and shows better accuracy, stability and ability to spot unexpected behavior from the printing process.

9050-25, Session 7

Lithography run-to-run control in high-mix manufacturing environment with a dynamic state estimation approach

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The quest to create robust control solutions for Photolithography processes is an ongoing matter. Over the past few decades several threaded and non-threaded Run-to-Run (RtR) control solutions have been introduced addressing various specific Lithography process control requirements. With continually shrinking semiconductor technology nodes greater interdependencies are being observed between processes requiring more complex control solutions that rely on increasing process context. With the high product mix, associated metrology costs add to this growing complexity, in using existing control solutions effectively.

Investments have continuously been pouring in control solutions' research and development to gain required momentum in an effort to create solutions meeting the future challenges. Most commonly used Lithography control solutions include both Threaded and Non-Threaded control approaches. The Threaded approach allows control to be performed using a set of context values, or "threads", e.g., Tool, Chamber, Product, Layer, etc. It allows good control state management allowing great granularity with features such as excellent noise isolation using simple mathematics. Drawbacks in this approach include thread starvation, data poverty, etc. especially in high mix environments with metrology sampling. The initiation of expired control threads using pilot lots or running full production lots with less accurate recipe settings are both costly results of thread starvation. While Non-Threaded control approaches can address many of the threaded solution limitations, it requires very complex solutions that are difficult to manage. Non-threaded controls on the other hand demand complex procedures allowing noise propagation making these solutions difficult to realize, and implement in complex semiconductor manufacturing environments.

This paper discusses the architecture of a dynamic RtR control solution approach that is successfully implemented in GLOBALFOUNDRIES high mix manufacturing environment offering coverage to all Lithography process steps in Fab8. This approach not only addresses the above discussed issues providing much of the flexibility offered by non-threaded approaches but also overcomes the limitations of threaded approaches. This solution is built on a carefully designed database using a control calculation methodology that allows a dynamic thread definition implementation.

Traditional threaded control solutions calculate the state values and recommended settings using the lot metrology and recipe settings used by the tool following post metrology feedback. Our method calculates ideal states at the metrology step and waits for lot arrival to calculate the recommended setting using these ideal states. The greatest advantage of this approach is to not require updating dynamically changing state values at every metrology feedback, reset, or other events that can trigger a change of estimated state value. The greater advantage of this methodology is to be able to calculate multiple parameter values dynamically with individually defined thread definitions per need. This simple approach offers great flexibility in managing the threads. Similar to threaded control approaches we calculate estimated state using individual ideal states defined by thread components.

Thread starvation can occur in High mix SM environments where data cannot be found within a defined time window to calculate the recipe parameter values. In static control environment, a pilot lot is often used to keep the threads alive requiring complex analytical techniques and/or seed values. Our dynamic control solution uses a thread reduction approach where in event of no relevant thread data, the number of thread components is reduced following a clearly defined precedence rule until sufficient amount of data is available to calculate the recipe parameter values to process the lot, as depicted in Figure 1. Precedence rules are defined using control data history with the help of different statistical analyses. This solution allows using different precedence rules for individual sets of hardware and/or for other relevant factors. This approach helps reducing the number of pilot lots for thread revival offering great flexibility and reduced overall cycle time.

One of the greatest advantages achieved by using this methodology is the ability to provide individual treatment of the special needs lots without compromising the control structure/hierarchy. The background database structure used for this methodology allows Engineers to select and define the precedence of thread components to be used for such lots. Control solution at lot arrival, then, retrieves this information to use in calculating the recipe settings to process the individual lots. A pictorial depiction of such is presented in Figure 2.

In order to assign precedence to the thread components, a rigorous statistical analysis is performed periodically assuring the validity of the thread definitions. This analysis also allows the inclusion of new thread components that are often required for introduction of new technology nodes, process methodologies, and innovations in the field of Lithography.

9050-26, Session 7

Improvement of interfield CDU by using on-product focus control

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On-product dose and focus control is crucial as process window of lithography process is getting tighter. For example, 1x nm node of ArFi scanner with 1.35 NA requires critical dimension uniformity (CDU) to 1 nm and available depth of focus (DOF) to 40 nm.

This paper mainly introduces to improve inter-field CDU with on-product focus control by diffraction based focus (DBF) method. DBF makes use of asymmetric targets, which have different side wall angles in between right and left edge sides. It is called as asymmetry, results in the difference of ± first order of diffracted light on the both edge sides, and changes monotonically through focus by a scatterometer.

For evaluation, the focus optimization flow from target design to on-product focus control is summarized as follows; 1) DBF design, 2) Integration of the selected DBF on a product reticle, 3) Focus metrology setup, 4) On-product focus monitoring, 5) On-product focus control.

The design rule for targets is to maximize both the sensitivity of the asymmetry towards focus and the monotonic range for focus. In contrast, other effects such as scanner dose variation, layer variation, reticle writing errors should be minimized to the sensitivity of the asymmetry.

For DBF target selection, the above design rules were considered. As a result, a robust focus metrology for focus control on product wafers was obtained with the specifications at an optimized wavelength shown in figure 1. The selected DBF target was integrated on each seven spot of a product reticle.

For on-product focus control, in advance, on-product focus monitoring during one week was performed to generate focus fingerprints on wafers. Daily-based five lots showed a stable focus fingerprint. Based on the monitoring results, focus height offset, and focus tilts of Rx and Ry corrections per field on wafers were applied. The result shows in figure 2. Focus uniformity of a controlled wafer was improved about 32% (3?) in comparison with a non-corrected one. It is outstanding result because focus related process latitude of the applied layer is very narrow.

To demonstrate the improvement of inter-field CDU, Full CDs on wafers were measured by Scanning Electron Microscope (SEM). As a result, inter-field CDU for controlled wafers was improved about 16% (3?) and 28.5 % (range) compared with non-controlled wafers, shown in figure 3.

In conclusion, we successfully improved inter-field CDU by using on-product focus control with DBF method. This achievement will be a great help to process window control.

9050-27, Session 7

Improving on-product performance via litho-cluster control using integrated, process-robust, diffraction-based metrology fueled by computationally designed device-like targets fit for advanced technologies (including FinFet)

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In order to meet current and future node overlay and focus requirements, metrology and process control performance need to be continuously improved. In addition, more complex lithography techniques, such as double patterning, advanced device designs, such as FinFet, as well as advanced materials like hardmasks, pose challenges for metrology and process control. In this publication several systematic steps are taken to face these challenges.

Designing metrology targets that will mimic device-like behavior is one of those important steps. Targets are designed using a computational solution which not only ensures printability but also predicts metrology signal-to-noise for the ASML YieldStar metrology system. Furthermore, the target design generation process simulates the target behavior for its robustness through process variations and also optimizes the design with the goal to match the target readings to the critical product features that need to be controlled.

For on-product overlay control, the above computationally designed targets are now used with the recently introduced µDBO technology for measurement of overlay using YieldStar systems in advanced FinFet process. Much attention is paid towards accuracy and process robustness (in addition to precision and speed) of overlay measurements in FEOL and MEOL layers of a FinFet process and results are reported in the publication.

For on-product focus control, asymmetric focus targets are being tested on product layers for measurement resolution, accuracy and robustness to process. Results from these product layers will be shared in the publication. Integrated metrology (IM) in combination with the technologies above shows the most optimum result. In previous publications the authors discussed the benefits of IM; in this current work much focus is paid towards the implementation of IM in high-volume manufacturing. A dynamic litho-cluster (scanner + track + IM) throughput model is developed and employed to successfully address several scenarios where IM needs to support “excessive” measurement load while keeping up with a production litho-cluster. Some of the scenarios of such “excessive” measurement loads are: (1) double patterning / triple patterning steps – to accommodate more than one overlay layer pair from a single measurement step; (2) via “last” process – to measure overlay at via layer with both metal layers (so called ‘double layer’ overlay); (3) Small lots – short exposure time, allowing less time for measurement; (4) combined overlay and focus measurements.

9050-28, Session 8

CD-SEM metrology for sub-10nm width features

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Although a variety of critical dimension (CD) metrology techniques is available, no single technology satisfies all CD metrology needs. Various workhorse metrologies such as CD-scanning electron microscopy (SEM) and optical critical dimension (OCD) scatterometry are in widespread use and provide complementary information. For example, OCD is useful for profile and average CD over a statistically valid number of similar features. CD-SEM is useful for measuring CD variation and roughness, with the invaluable abilities inherent to image-based systems for spot-checking design weak points of discrete features, measuring contour information, and, of course, the qualitative excursion information gained only from an image. These technologies are also beginning to directly support each other through combined or so-called hybrid metrology [1]. However in their present forms, they are beginning to reach physical limitations in usefulness for some important applications. The 22 nm node also marked the beginning of a major transition from conventional scaling-driven planar devices to complex three –dimensional (3D) transistor architectures, redefining future needs for lithographic metrology solutions for high-volume manufacturing [2]. Evaluation of CD, roughness, and other parameters in FinFETs raised new metrology complexities, as the entire 3D structure became critical for process control, including fin and gate dimensions, profiles and roughness, and undercuts. Similarly, future 3D memory devices will include multiple gate-level structures defined by high-aspect-ratio (HAR) trenches and holes in multilayer stacks. To address these challenges, a robust metrology strategy should encompass the extendibility of conventional techniques that are approaching their fundamental limits, as well as the development of new technologies [3].

Over the past many years, some have stated that CD-SEM is near the end of its usefulness. However, aside from possible high-voltage SEM or helium ion microscope, there are promising improvements for extending the well-proven conventional LV-SEM technology [4][5]. A couple of past works [3][6] showed that the spatial resolution of CD-SEMs has stagnated in recent years, and it is falling behind the requirements of Moore’s law, which demands improvement. A recent paper has claimed a possible leap forward through aberration correction [4]. As for the needed 3D requirements, model-based measurement methods have shown capabilities to infer 3D information if the waveform fidelity is good enough. Also, there are still other possibilities, such as tilt SEM [7] or advanced multi-channel detector schemes [8]. However, the key parameter that must be improved for most of these to be extended into the sub-10 nm regime is spatial resolution. Today, there is no image resolution standard, such that it is not very meaningful as a quantitative term. One can consider it to represent the smallest distance one can measure, but in reality image resolution is a convolution of beam spot size, interaction volume at the sample surface and also detector optics and other aberrations such as charging or vibrations. Spot size is a more descriptive term. But regardless, when such beams are applied not to the large features of yesterday, where the interaction volume was far smaller than the targets, but to the sub-10 nm features of tomorrow, where linewidths are smaller than the interaction volume, other complications arise for quantitative CD metrology.

This paper will explore the possibilities of CD-SEM metrology at sub-10 nm feature sizes using modeling. JMONSEL simulations will be used to illustrate SEM waveforms for very small features, as a function of beam energy, feature size, profile height and sidewall angle. It will also be shown that the dimensions of the electron beam and interaction volume have very strong influence on the results. Using modeled results, an assessment concerning required image quality for future tools will be presented. Additionally, from the generated waveforms, various measurement algorithm prospects will be evaluated for such future nanometer-scale applications.

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9050-29, Session 8

Improving SEM image quality using pixel superresolution technique

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As the semiconductor industry moves toward increasing the number of transistors within integrated circuits, the size of structures such as lines, trenches and contact holes will continue to shrink. For advanced technology nodes, the critical dimension (CD) of several structures will be below 10nm resulting in LER and CER less than 3nm. For this reason, the ability to detect and measure nanoscale structures becomes of critical importance in metrology and inspection. The most up-to-date scanning electron microscope (SEM) can provide image magnification up to 500kX, translating to an effective minimum pixel size of 0.53nm at the detector plane. In spite of high magnification, precise measurement of fins, for example, with 5nm CD is still challenging. CD-SEMs currently on the market will only utilize 9 pixels across the fin of this size and thus only ~ 3 pixels will be utilized to measure LER and CER. The most direct solution to increase spatial resolution is to reduce the physical pixel size. As the pixel size decreases, however, the amount of light available for each pixel also decreases and generated shot noise at each pixel degrades the image quality. In addition to the pixel size limitation, spatial aliasing together with existing noise and blurring can lead to an unreliable measurement for such small features.

An alternate solution is to use signal processing techniques to obtain a high resolution (HR) image by using information from a sequence of low resolution images. This technique is called Pixel Super resolution (PSR) technique and it has proven to be useful in many practical applications. Figure 1 shows the schematic of the PSR image reconstruction process. The physical pixel grid of imaging systems represented in Figure 1(a) is a low resolution (LR) grid. If the LR images have different sub-pixel shifts from each other, as shown in Figure 1(b), the new information contained in each LR images can be exploited to generate a high resolution image with a denser grid, shown in Figure 1(c). It is important to note that the super resolution image reconstruction process consist of three computational steps: registration, interpolation, and restoration.

This work will show how to apply the PSR technique for CD-SEM image analysis and will demonstrate how to improve image quality by utilizing more digital pixels, while at the same time suppressing measurement noise.

9050-30, Session 8

Contour-based metrology for complex 2D shaped patterns printed by multiple-patterning process

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We developed a new measurement method enabling to quantitatively and accurately evaluate 2D pattern shapes, which becomes critical in patterning control of Metal layer patterns printed by Litho-Etch-Litho-Etch (LELE) process.

In LELE, a split patterning of Metal-A (MA) layer and Metal-B (MB) layer makes patterning control more challenging. Hence, it is essential to evaluate the shape of printed patterns after final etching in order to verify that the patterning control of MA and MB layer patterns is performed within an allowable budget. For this, our Pattern Shape Quantification (PSQ) method [1], which enables to measure dimensional difference of printed pattern shape from their target design, is an effective metrology.

Patterns printed through a LELE process contain the effects of two types of causes. First is the fidelity of the printed pattern shape (e.g. pattern-end pull-back or push-out) whose determinative factors are adopted design (e.g. OPC and SRAF), process condition (of e.g. lithography and etching), etc. The second is the shift in position between MA and MB patterns induced by overlay (OVL) errors. That means, the edge-placement errors (EPE) in the final pattern are not only due to the fidelity of the printed pattern shape, but are also impacted by the overlay error between MA and MB patterns . On the other hand, a space between MA and MB patterns will also be affected by the OVL errors. A failure to maintain a required minimum space between patterns would cause leak-current between patterns (and hence directly affect device performance), so it is important that the positional shift between MA and MB can be measured accurately.

Therefore, we developed a method to measure local overlay errors between MA and MB in actual device patterns, from CD-SEM images, while also to outputting a pattern-contour of MA and MB in which this overlay error has been removed. Utilizing such a pattern-contour into the PSQ method enables to quantitatively determine the fidelity of printed pattern shape solely induced by the 1st cause, while providing overlay-error data from the device patterns themselves. We believe that high-leveled patterning control (by e.g. optimization of process condition) of MA layer and MB layer patterns can be performable only by using such a measurement result.

This paper demonstrates and discusses the capability and effectiveness of our newly developed method.

9050-31, Session 8

Parallel SPM cantilever arrays for large-area surface metrology and lithography

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Scanning Probe Microscopy (SPM) belongs to the technologies, which enable high resolution investigations and modifications of surface properties. Despite its high sensitivity, which enables imaging of atomic structures, the standard SPM applications are restricted to small area specimens. In addition, the relatively long time of the imaging or modification process makes the usage of the SPM-based technology in industrial applications limited. By fabricating sensor arrays, in which the cantilevers are placed parallel to each other, both the throughput and sensing possibility can be increased. In the described process, the deflection of each cantilever must be controlled and sensed individually. In this paper we will introduce the operation of thermally actuated piezoresistive cantilever arrays. The piezoresistive microcantilevers are widely applied in measurements of low forces, masses and viscosity due to their high sensitivity [1], [2]. Because the deflection signal is sensed electronically, the design and fabrication of elaborate SPM systems is simplified. In addition, integration of thermal actuator with the piezoresistive cantilevers opens the possibility to control the cantilever tip deflection and increase surface metrology and lithography throughput [3], [4]. It should be underlined, that the piezoresistive cantilevers belong to the only few micro electro mechanical systems

(MEMS), which enable metrological (in other words quantitave) force and deflection investigations [5], [6]. The unique features presented here make thermally actuated piezoresistive cantilever arrays the best technology for parallel surface imaging and modification (Fig.1). However, a reliable application of the solution described requires profound analysis of the system properties. In this article it will be presented, how to calibrate the detection and actuation sensitivity of the one dimensional (1D) array cantilever deflection. In these procedures advanced SPM and interferometrical methods are used to determine the indicated parameters (Fig.2). It will be also presented how to determine the cantilever spring constant. This procedure is based on spectral analysis of spring beam thermomechanical fluctuation, which is the limit of minimal detectable force. The spring constant obtained on the basis of the noise analysis was compared with spring constant values calculated on the basis of spring beam resonance frequency and its geometry. The architecture of the SPM based system for the surface metrological investigations and lithography, which utilizes the thermally actuated piezoresistive probes will be introduced [7], [8]. The results of the surface measurements using 16 cantilever array will also be presented.

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9050-32, Session 8

In-situ defect classification by AFM-based nanomechanical measurement

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Fast in-line material classification of sub-40 nm defects is a major challenge in current HVM manufacturing. With defects of interest entering the single digits in nanometers, conventional in-line material identification technology (primarily SEM-EDX) is unable to meet future characterization needs. massive growth in demand for expensive, destructive, and time consuming off-line analysis technology (such as TEM) in order to compensate.

With extreme surface sensitivity and high resolution compared to an SEM, AFM has many obvious advantages as a defect imaging system. With the recent introduction of fast-scan systems able to measure images in seconds, much of the previous gap in terms of throughput has narrowed. No analogous equivalent exists for SEM-EDX to allow material classification; however, many alternative data streams are available to the AFM that have the potential to fill a similar function. For instance, Bruker's Icon AFM system can obtain quantitative mechanical data from objects while obtaining topographic and/or imaging data. The major gap is in linking such alternative data streams to compositional data in a way that allows actual decision making. Bridging this gap is the aim of the current work.

In order to obtain a wide range of realistically sized defects of varying materials, we obtain real defect masks from SEMATECH's EUV Mask Blank Defect Reduction Program. Defects are located via inspection in a Lasertec M7360 confocal inspection tool, which allows recapture in a Bruker Icon FastScan AFM in a very reasonably sized search scan. The Icon is used to provide size and shape data, as well as quantitative nano-mechanical data using Bruker's Peak Force – QNM measurement mode. PF-QNM provides information on the adhesion force, repulsion force, and modulus of the defect. Composition of defects is then evaluated in an FEI Titan 80-300 S/TEM equipped with a SuperX windowless silicon drift detector, allowing us to fully map the elemental composition of very small defects.

A defect library is being amassed to determine primary defect classifications by linking the nano-mechanical and compositional information of a large. We are able to parse out defect material classifications into categories using the AFM data that in turn can be used to identify the probable yield priority of different defect groups, while retaining extremely high resolution, sensitivity, and throughput.

9050-121, Session 8

The pattern wiggling metrology using CD-SEM

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No Abstract Available

9050-33, Session 9

CD-SAXS comparison study of lab sources versus synchrotrons

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The semiconductor industry is rapidly moving toward non-planar device architectures and nanoscale dimensions to increase device power efficiency and performance. These 3D, multicomponent nanostructures present new challenges to conventional processing metrology. We will discuss how critical-dimension small angle x-ray scattering (CD-SAXS) provides a non-destructive route for dimensional characterization of 3D nanostructures for determination of line-edge roughness, pattern shape and pitch. The presentation will focus on moving CD-SAXS from the synchrotron to the fab. We have completed a transmission CD-SAXS study on a series of 32 nm pitch line gratings fabricated using a spacer-based pitch quartering process (1) and 65 nm pitch dual-lithography SOI finFETs.(2) We measured the same targets on both the

synchrotron and our laboratory source to obtain direct comparisons. On the laboratory source, we conducted an exposure series to determine the minimum measurement time required to get an adequate data fit. We found the resolution of current laboratory source to be sufficient with the only limitation being number of photons. We will discuss guidance for new, higher brightness x-ray sources and routes for decreasing the measurement time.

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9050-34, Session 9

Characterization of directed self-assembly process using grazing incidence small-angle x-ray scattering

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The LiNe (Liu-Nealey) flow implemented at imec, which uses chemical patterns to direct the self-assembly (DSA) of block copolymer (BCP) films, enables the fabrication of 28nm pitch line/space patterns on 300mm wafers. [1, 2] Critical next phase of development of DSA in general is reducing feature size below 10 nm and developing metrology to inspect the process and defects. Here, we apply state-of-the-art X-ray scattering technique toward the metrology of the entire DSA process. We inspect each step of LiNe flow using grazing incidence small angle X-ray scattering (GISAXS) beam line at Advanced Photon Source of Argonne National Laboratory. Based on the GISAXS results, we characterize the geometries (pitch, width, and edge profile) of PS guiding stripes and chemical pre-patterns, which are the key parameters of DSA process. For inspection of BCP films, we control the incident angle of X-ray and also azimuthally rotate the samples. The directional ordering of BCP films is evaluated by the scattering pattern in perpendicular orientation of incident beam and chemical pre-pattern. GISAXS patterns of BCP films are almost identical regardless of geometry of chemical pattern when the top-down SEM shows well aligned BCP domains and the incident angle of X-ray is below the critical angle of BCP. However, the GISAXS patterns with incident angle above the critical angle of BCP are significantly different, indicating that inner structures of BCP films are different. The details of the three-dimensional structure of individual block copolymer domains will be captured by the analysis of form factor from GISAXS data of BCP films in conjunction with molecular simulation that uses the quantitative geometrical information of chemical pattern obtained by GISAXS of chemical pattern as the boundary conditions.

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9050-35, Session 9

Correlation of CD-SAXS and CD-AFM measurements for FinFET fabrication process monitoring

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As critical dimensions of FinFET channels shrink, sidewall roughness may contribute significantly to the variation in critical dimension. In a Si-FinFET device, the current flows predominantly along the Si/high-k interface at high gate bias and, therefore, carrier mobility degrades due to surface scattering from large interface roughness [1]. To mitigate these effects, hydrogen annealing is often used to round off the corners and to smooth the sidewalls of the Si fins prior to high-k gate stack deposition, greatly improving gate leakage; it is also used to reduce the width of the fins,lowering the threshold voltage, and decreasing drain-induced barrier lowering (DIBL) characteristics [2].

In this study, we locally measure the CD, height, sidewall angle and sidewall RMS roughness of Si fin channel arrays using CD-AFM for a variety of different H2 anneal conditions. In addition, we used synchrotron CD-SAXS to measure the same structures to obtain average values for pitch, pitchwalk, CD, height, sidewall angle in order to create a representative trapezoidal cross-section [3].After careful correction of the contributions of scattered intensity due to angular divergence of the X-ray probe, slit scattering, and absorption correction through Si substrate, we analyzed the diffuse scattering intensity due to Si fin roughness about the fundamental Bragg diffraction orders. We have also included simulations that estimate the sensitivity of synchrotron CD-SAXS to Si fin roughness to access if the roughness measurements are within the expected uncertainty budget.

9050-36, Session 9

Nanometrology on gratings with GISAXS: FEM Reconstruction and Fourier Analysis

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The pursuit of the semiconductor industry to decrease the feature sizes of integrated circuits poses a huge technological endeavor. Consequently, new difficulties arise for metrology on structures in the nanometer regime. Scatterometry is a fast method which provides non-contact non-destructive characterization of photomasks or exposed wafers. However, the determination of important absorber grating parameters like critical dimension (CD), pitch and the sidewall angles (SWA) are still a big challenge in nanometrology.

Grazing incidence small-angle X-ray scattering (GISAXS) is another versatile technique to measure both vertical and lateral structural features in the nanometer range with high sensitivity. Our measurements were conducted at the four-crystal monochromator (FCM) beamline operated by the PTB at the electron storage ring BESSY II in Berlin with a tunable photon energy range from 1.75 keV to 10 keV. In conjunction with a unique in-vacuum PILATUS 1M hybrid pixel detector, the entire energy

range is accessible for SAXS and GISAXS measurements on a wide range of sample systems.

We apply GISAXS to investigate structural parameters such as period length, side wall angle, line width and height on silicon gratings. Our test structures were fabricated with electron beam lithography (EBL) with nominal values of 25 nm and 50 nm in the critical dimension and a 100 nm pitch. The scattering patterns have been analyzed with a simulation-free forward calculation which yields a traceable characterization of the grating lines with respect to critical dimension and pitch.

Access to other parameters such as sidewall angle and height is more demanding and requires rigorous modeling to solve the inverse problem. We show the first applications of a Maxwell solver based finite element method (FEM) to the reconstruction of the scattering pattern in gracing incidence small angle X-ray scattering.

9050-37, Session 10

Monitoring process-induced overlay errors through high-resolution wafer geometry measurements

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The unrelenting reduction of critical dimension size in semiconductor devices continues to place significant demands on advanced lithography processes. Overlay is recognized as a significant challenge at current and future nodes in ITRS as overlay budgets for many devices are approaching the range of a few nanometers. Process-induced overlay errors, such as those due to the deposition/etching of films with residual stress and RTP steps, are of particular concern and are identified by the ITRS as a key challenge. In the present work, we demonstrate a fundamental relationship between changes in local wafer shape, residual stresses, and overlay errors. The relationship between these quantities allows wafer geometry measurements to be used to rapidly assess the effect that a multitude of wafer processing steps can have on overlay errors. Furthermore, the ability to predict overlay errors based on wafer geometry measurements may eventually enable feed-forward correction schemes in which local wafer geometry information can be fed to scanners to choose correction strategies that will minimize overlay errors for specific wafers.

It is well established that the deposition of residually stressed films can induce both out-of-plane and in-plane wafer distortion. The out-of-plane distortion can be measured using wafer geometry metrology tools. In modern scanners, the wafer is chucked flat during exposure, thus only the in-plane distortion contributes to overlay errors. If the residual stress in the film is uniform, the stresses induce a simple deformation field on the patterned surface of the wafer that can be corrected through standard linear corrections in the lithography process. However, if the stress or thickness of the film varies with spatial position on the wafer, local distortions that cannot be corrected with linear corrections will be induced and cause overlay errors. Through an analytical mechanics model, we have shown that the non-correctable component of the in-plane distortion (i.e., overlay) induced by changes in film stress is linearly proportional to a shape metric related to the local wafer slope.

This relationship between local wafer slope and overlay error has been validated through both computational mechanics simulations and experiments. We have demonstrated this relationship using finite element simulations consisting of two steps: (1) simulated wafer shapes were generated by assuming a non-uniform residual stress in a film and predicting the change in wafer shape and in-plane distortion, (2) overlay resulting from the stress-induced deformation was predicted by simulating the chucking of the deformed wafer and applying linear corrections. Local slope, calculated based on the simulated wafer shapes, was shown to be linearly proportional to the predicted overlay. Furthermore, experiments performed at IBM in which stressed nitride films were deposited and patterned on wafers between lithography steps demonstrated a strong correlation between local slope and overlay*.

This talk will summarize: (1) The mechanics analysis that shows the fundamental relationships between residual stress, local slope, and overlay, (2) Results of finite element simulations of wafers with non-uniform stresses demonstrating the relationship between slope and overlay, (3) Comparisons between experimental results and predictions from the analytical and finite element models.

References:

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9050-38, Session 10

Investigation on reticle heating effect induced overlay error

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As design rule of semiconductor shrinks continuously, overlay error control gets more and more important and challenging. It is also true that on product overlay (OPO) of leading edge memory device shows unprecedented level of accuracy, owing to the development of precision optics, mechanic stage and alignment system with active compensation of various overlay error terms. However, the heating of reticle and lens acts as a dominant detriment against further improvement of overlay. Reticle heating is more critical than lens heating in current advanced scanners because lens heating can be mostly compensated by feed-forward control algorithm. In recent years, the tools and technical ideas for reticle heating control are proposed and thought to reduce the reticle heating effect. Nevertheless, it is still not simple to predict the heating amount and overlay. And it is required to investigate the parameters affecting reticle heating quantitatively.

In this paper, the reticle pattern density and exposure dose are considered as the main contributors, and the effects are investigated through experiments. Mask set of various transmittance levels are prepared by changing pattern density. After exposure with various doses, overlay are measured and analyzed by comparing with reference marks exposed in heating free condition. As a result, it is discovered that even in the case of low dose and high transmittance, reticle heating is hardly avoidable. It is also shown that there are simple relationship among reticle heating, transmittance and exposure dose. Based on this relationship, the reticle heating is thought to be predicted if the transmittance and dose are fixed. In addition, the effects of pattern localization, i.e., non-uniform pattern density are studied.

9050-39, Session 10

Compensating process nonuniformity to improve wafer overlay by RegC

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The introduction of double and triple patterning tightened the Overlay current nodes’ specifications across the industry to levels of 5nm and 3nm respectively.

Overlay error is a combination of Intra-field and field-to-field errors.

The Intra-field error includes several systematic signatures, such as overlay magnitude differences between X and Y axes, field center vs edge and more.

The recent developments in scanner technology improved the intra-field Overlay to high orders.

In this work we have quantified the state-of-the-art residual overlay errors and applied the RegC product, a new solution of deep sub-nanometer pattern shift, to further improve the overlay process control, in addition to the current lithography's state-of-the-art capabilities.

As a result we managed to reduce the baseline overlay error by more than one nanometer and reduced systematic intra-field non-uniformities, by removing the 3 sigma difference between X and Y to zero.

The combination of intra-field control by RegC with high order correction per exposure (CPE) by the scanner provides a new era of overlay control required for the 2x and 1x multiple patterning processes.

9050-40, Session 11

Optical three-dimensional volumetric detection of sub-20nm dense patterned defects with noise

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As critical dimensions decrease, the optical detection of "killer" pattered defects from two-dimensional images becomes problematic. Recently, we have demonstrated a new approach using focus-resolved optical microscopy that enables a volumetric analysis of three-dimensional volumes of measured optical data with up to fourfold improvement in sensitivity as compared to two-dimensional images. Images for such volumes are collected at several focal planes, with all data assembled and processed as a single matrix of (x,y,z,I) values where I is the intensity. Simulations and experiments using this approach on the 9 nm node SEMATECH intentional defect array (IDA) have shown that the extent of the defect optical signal persists through large (>350 nm) axial extent along the z axis, especially compared to the spatial extent of the defect signal in the xy plane. In this presentation, the extensibility of these methods as the critical dimensions decrease and pitches are reduced is evaluated using the 9 nm node and 7 nm node IDAs.

Given their relative importance at smaller dimensions, additional emphasis will be placed on the effects of wafer noise and line-edge roughness (LER) upon optical two-dimensional and three-dimensional optical techniques. Simulation studies using rigorous three-dimensional electromagnetic models of the IDA layouts with differing amounts of LER and wafer noise are presented with the optical difference signals compared quantitatively. Polarization, incident angle, and focus effects are included in this analysis.

Experimental evaluation of the optical scattering from patterned defects with noise will be performed using an IDA wafer with varying e-beam patterning quality. Variation of the patterning across several copies of the IDA ensures that one copy will be optimally printed, but this yields opportunities probing the effects of increased noise due imperfections in the underlying structure. Detectability metrics are used to compare measurements among these die, each of which has been characterized using scanning electron microscopy (SEM). The implications of noise upon two- and three-dimensional imaging using focus-resolved optical microscopy with polarized deep-ultraviolet illumination are examined, with options for multi-focus collection for increased throughput explored.

9050-41, Session 11

9nm-node wafer defect inspection using visible light

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Presently, the 22nm node process is widely used in semiconductor chips, which has significant performance improvement over the previous node. With continuing efforts on nanofabrication, node sizes shrinking to 10 nm will be possible around 2017, according to the International Technology Roadmap for Semiconductors (ITRS). During semiconductor manufacturing, critical dimension (CD) metrology plays an indispensable role to maximize the throughout and increase the performance of devices. The current widely used CD metrology tools are based on scanning electron microscopy (SEM), atomic force microscopy (AFM), and optical microscopy. Optical CD metrology tools are usually non-destructive and have high throughput, making it suitable for in-line defect inspection, whereas its sensitivity is modest.

Over the past two years, we have developed a highly sensitive optical metrology tool based on a 532 nm laser epi-illumination diffraction phase microscopy (epi-DPM). Epi-DPM is a common optical-path digital holography microscope. Using it, we have successfully demonstrated detection of different types of defects down to 20 nm wide by 100 nm long or similar in a 22nm node intentional defect array (IDA) wafer. We retrieve both the phase and amplitude of the reflected light from the wafer surface and use a comprehensive image post-processing method to extract the wafer defect signal. The processing method is called 2DISC, which is a combination of producing 2nd order difference of transverse scan image frames, image stitching, and defect pattern convolution. Recently, we adapted the system to inspect 9nm node IDA wafer defects. This wafer has defect sizes that are only 10 nm wide (40% compared with 22nm node IDA wafer). Thus, the system's sensitivity needs to be tremendously enhanced to successfully detect defects. We replaced our 532 nm solid state laser with a 405 nm diode laser that has a 10x better power stability and inserted a 405 nm narrow-band filter in front of the camera. With the 2DISC method, we have detected parallel bridge defects in both phase and amplitude images.

To further improve the sensitivity, several approaches were explored. One approach is dark field imaging, which is suitable for detecting edge defects. We use an inverse pinhole filter to high pass the image at the Fourier plane to remove laser speckle noise. In this way, the CCD camera's full dynamic range can be used for the wafer signal. Our results from measuring a parallel bridge defect showed about 50% sensitivity improvement compared to bright field. Another approach uses a z-scan to produce a 3-dimentional wafer image. Our z-scan measurements used a white light illumination system (400-1100nm). From the 2nd order differential z-stack images, the defect signal can be clearly identified from many cross-section planes.

9050-42, Session 11

Highly-effective and accurate weak point monitoring method for advanced design rule (1xnm) devices

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Historically when we used to manufacture semiconductor devices for 45 nm or above design rules, IC manufacturing yield was mainly determined by global random variations and therefore the chip manufacturers / manufacturing team were mainly responsible for yield improvement. With the introduction of sub-45 nm semiconductor technologies, yield started to be dominated by systematic variations, primarily centered on resolution problems, copper/low-k interconnects and CMP. These local systematic variations, which have become decisively greater than global random variations, are design-dependent [1, 2] and therefore designers now share the responsibility of increasing yield with manufacturers / manufacturing team's. A widening manufacturing gap has led to a dramatic increase in design rules that are either too restrictive or do not guarantee a litho/etch hotspot-free design. The semiconductor industry is currently limited to 193 nm scanners and it's honest to say no relief is expected from the equipment side to prevent / eliminate these systematic hotspots. Hence we have seen a lot of design houses coming up with innovative design products to hotspots based on model based lithography checks to validate design manufacturability, which will also

account for complex two-dimensional effects that stem from aggressive scaling of 193nm lithography.

Most of these hot spots (AKA weak points) are especially seen on Back End of the Line (BEOL) process levels like Mx ADI, Mx Etch and Mx CMP. Inspecting some of these backend levels can be extremely challenging as there are lots of wafer noises or nuisances that can hinder an inspector's ability to detect and monitor the defects or weak points of interest. In this work we have attempted to accurately inspect the weak points using a novel broadband optical inspection approach that enhances defect signal from patterns of interest (POI) and precisely suppresses surrounding wafer noises. This new approach is a paradigm shift in wafer inspection by leveraging systematic defect locations for high sensitivity inspection, thereby enhancing the discovery and monitor of yield limiting defects at traditional optical inspection throughput.

9050-43, Session 11

Real-time inspection system utilizing scatterometry pupil data

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Scatterometry-based CD, also known as Optical CD (OCD) significantly matches CD-SEM in accuracy and precision, in addition to offering superior full-profile reconstruction. OCD, however, is computationally intensive. For solver-based OCD, a Maxwell's equation solver, typically employing a Rigorous Coupled Wave Analysis (RCWA), is used to compute pupil maps with diffracted zero or first orders for gratings with different parameters. This computation has to be repeated many times per measurement, within an optimization algorithm in order to find the grating parameters that minimize the cost function between the sample pupil map and the simulated pupil map. An example of this is ASML's YieldStar S-200C in-line metrology tool, which can take from 1.2 to 8 seconds / measurement depending on the type and complexity of the profile. Library-based OCD is faster when measuring, but requires a massive pre-computed library of different profiles, needing hours or days of computation time to construct.

In this paper, our objective is to construct an extremely fast screening tool that determines whether a sample should or should not proceed to subsequent manufacturing steps. To this end we examine the diffracted pupil map in order to determine whether a sample is in or out of its specification limits. This allows us to allocate traditional metrology resources only on samples that show unusual behavior. Our screening tool is computationally efficient since it uses supervised classification techniques on the patterns observed in the pupil map. While training is required, it can be accomplished by a number of RCWA computations that is orders of magnitude smaller than what is needed in typical library-based OCD. No RCWA computation is needed during actual inspection, and classification is very quickly accomplished using closed-form expressions.

The proposed system is constructed by using each pixel of the pupil map as a feature, resulting in a high-dimensional binary classification problem. Support Vector Machines (SVM) are trained and applied to classify each incoming sample as in-spec or out-of-spec. Out-of-spec samples are further classified using two polyhedral SVM classifiers, one that allows us to detect and classify known faults, and another that allows us to create new fault labels as new samples are observed. We have analyzed both simulated and real data for 2 different types of periodic grating profiles. For simulated data, we generate pupil maps for in-spec, CD out-of-spec, and Sidewall Angle (SWA) out-of-spec samples; for real data, we have exposed and inspected a focus-exposure matrix for a rectangular silicon-BARC-photoresist stack. The grating dimensions were 45(90) and 150 (600), where CD (pitch) in nm. For both cases we use the 10% process window and analyze misclassification rates as well as false and missed alarm rates.

Results show that our prototype screening system is approximately 100 times faster than solver-based OCD while its misclassification errors are in the order of 5% or less for simulated cases with 700 training and 300 test samples. For our example, the training time was 1000 RCWA simulations (approximately 4 hours on an i5 processor) but if focused on samples along the in-spec/out-of-spec boundary, computation time can be further reduced.

9050-44, Session 11

New inspection technology for observing nanometer size defects using expansion soft template

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1. INTRODUCTION

In next generation lithography for semiconductor devices, some technologies (Extreme-UV (EUV), Directed self-assembly (DSA) and Nano-imprint lithography (NIL) etc.) are proposed and the patterning size by those technologies is markedly reduced into a nanometer size. In this case, inspection technologies for detecting nanometer size defects on wafers are quite important.

In the case of EB inspection, it is easily possible to detect nanometer size defects. However, EB inspection systems increase a cost of inspection process and inspection time of the wafer becomes elongated to observe the smallest defect. In the case of optical inspection, it is difficult to detect a defect whose size is less than 23nm because of optical resolution limit though it is easy to reduce inspection time.

This paper describes cost-effective new inspection technology for detecting a nanometer size defect with the optical inspection technology using replicated soft template which is able to enlarge a defect size by expanding. Expansion ratio of various expanding methods and feasibility of detecting a nanometer size defect will be reported.

2. NEW INSPECTON TECHNOLOGY WITH EXPANSION TEMPLATE

Figure 1 shows basic concept and process flow chart of new inspection technology using expansion soft template. First, the resin of pattern expanding material is prepared and coated on the master template (or the wafer). After UV irradiation, organic soft template is separated from the master template. The pattern and the defects are replicated on the surface of the soft template. Through expanding process, the organic soft template is expanding and its replicated pattern and its replicated defects are also expanding. Extremely small size defects are perfectly detecting and remaking by analyzing the large size defects with expanding on expansion soft template by current optical inspection equipment.

3. RESULTS AND DISCUSSION

There are some concepts to expand a soft template. The first one is to use solvent and shown in Fig.2 (a). After peeling from the master template, the replicated soft template is located in the solvent liquid and swelling. Then, removing the solvent liquid and cleaning, the expansion soft template is made. The second one is to use a mechanical enlarging tool and shown in Fig.2 (b). The soft template is elongated using the mechanical enlarging tool, so that the template is expanding.

The largest expansion was observed using the special organic material. Optical microscope pictures of the master template and the expansion soft template are shown in Fig.3 (a) and (b), respectively. The expansion ratio of 240% was obtained. The result shows feasibility of defect inspection of 9.6nm size by optical inspection system.

4. CONCLUSION

New inspection technology for detecting nanometer size defects using the expansion soft template has been proposed and expanding ratio was 240%. Feasibility of inspection of a nanometer size defect is confirmed.

9050-45, Session 11

Parallel, miniaturized scanning probe microscope for defect inspection and review

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With the device dimensions moving towards the 1X node, the semiconductor industry is rapidly approaching the point where 10 nm defects become critical. Moreover, the contrast between defects of interests from nuisance defects becomes so low that it makes the recognition very challenging. Therefore, new methods for improving the yield are emerging, including inspection and review methods with sufficient resolution and throughput. Existing industrial tools cannot anymore fulfill these requirements for upcoming smaller and 3D features, since they are performing at the edge of their performance.

Scanning probe microscope (SPM) has the distinct advantage of being able to discern the atomic structure of the substrate. It can also be used for true 3D scanning of the nano-features [1]. However, the current state-of-the-art SPMs have several limitations, among them the low throughput is one of the main bottlenecks.

In order to meet the increasing demand for resolution and throughput of defect inspection and review, we have introduced the parallel SPM concept [2], consisting of parallel operation of many miniaturized SPMs (MSPMs) on a 450 mm wafer. Figure 1 illustrates the model of part of the system. In this paper we present the performance of critical sub-systems, and the progress towards a demonstrator, which includes:

1-High speed parallel positioning unit: This positioning unit consists of parallel mechatronics arms, each capable of positioning a MSPM towards a wafer. Positioning of each MSPM is done individually to enable maximizing the wafer surface coverage. The positioning is done in closed loop to achieve high positioning accuracy. Figure 2 shows the final design of one positioning arm that carries one MSPM. The experimental results revealed a positioning accuracy better than 200 nm. Figure 3 shows the experimental test setup and the results of positioning repeatability.

2-High speed MSPM: A miniature scanning probe microscope (Size ~ 70x19x45 mm3) has been designed and realized to scan area of 10 x 10 µm2 to detect and review the defects. The scanner has a bandwidth of 30 KHz and a z stroke of 2.1 µm. The read-out of the probe has a resolution of 15 fm/√Hz and a bandwidth of 3 MHz, which allows the use of ultra-high frequency cantilevers. The preliminary experimental results of z scanner frequency spectra and the noise performance of the optical beam deflection of the MSPMS are illustrated in figure 4.

9050-46, Session 11

Quantitative tabletop coherent diffraction imaging microscope for EUV lithography mask inspection

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Lithographic inspection tools routinely require nanometer scale sensitivity in metrological applications such as defect analysis. Control over critical transistor dimension begins with proper mask inspection and due to this, current mask metrologies not only include defect inspection but also probe mask induced phase shifts as part of a process known as optical proximity correction (OPC), which attempts to most accurately reproduce the mask pattern on the wafer. Even though mask features are roughly four times larger than what is eventually printed, after OPC the half-pitch feature size on the mask itself can be smaller than what is printed. For this reason, inspection technologies are driven by patterning capabilities and represent a substantial roadblock for the future of EUVL. From the SPIE Newsroom, “Extreme ultraviolet lithography (EUVL) has been identified as the most promising technique for generating semiconductor wafers with a 22nm half-pitch or less, according to surveys taken at SEMATECH’s Lithography Forum last year as well as at the 2008 International EUVL Symposium.1, 2 The same groups ranked mask defectivity as the second highest challenge – after source power – that needs to be overcome in order to ensure the success of this technology” [sic].

Coherent diffractive imaging (CDI), also known as lensless imaging, is an alternative microscopy method that has no need for image forming optics. In CDI, coherent light illuminates the sample and the far field scatter pattern is recorded with a CCD. Assuming the scattered intensity is Nyquist sampled (which conventionally means the sample is isolated), a phase retrieval algorithm can be used to reconstruct the image of the sample. CDI provides aberration-free, diffraction-limited images and is capable of evaluating the width and height of phase defects as small as 220nm on EUV mask blanks, imaging patterned EUV mask with 100nm resolution, and obtaining actinic critical dimensions.

We demonstrate, for the first time to our knowledge, keyhole CDI (KCDI) using a compact EUV source capable of providing quantitative feature depth characterization. In KCDI, a pinhole is placed in a converging beam, so the isolation requirement is imposed on the illumination rather than the sample. With consideration of astigmatism introduced by the non-normal incidence on multilayer curved mirror, we successfully reconstructed selected regions of an extended test pattern, with ~ 200nm resolution using 30nm HHG. However, much higher resolution is achievable since we can easily shift from 30nm to 13nm HHG and use higher NA.

Additionally we have demonstrated reflection CDI on a periodic sample using conical correction for non-normal incidence diffraction. In our recent work, KCDI has been performed on general extended non-periodic sample. We will describe our preliminary results on the first demonstration, to our knowledge, of reflection KCDI with tabletop EUV source.

Our goal is to implement a standalone and compact EUV microscope with particular emphasis on EUVL mask inspection. It will also have other applications such as imaging 3D interconnects, buried and layered structures, biological samples, and the dynamics of magnetic domain flipping and nanoscale heat transport.

9050-47, Session 11

Computational techniques for determining printability of real defects in EUV mask pilot line

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With EUV lithography on the ITRS roadmap for sub-2X half-pitch patterning, it has become increasingly essential to ramp up efforts in being able to manufacture defect-free reticles or at least ones with minimal defects initially. For this purpose, much of the focus in recent years has been in finding ways to adequately detect, characterize, and reduce defects on both EUV blanks and patterned masks. With the current inspection of EUV blanks and patterned masks being primarily high-resolution DUV or e-beam based, it becomes very challenging to assess the real impact of the detected defects on EUV plane. Even with the realization of the EUV beta AIMSTM aerial-image based metrology in 2014-2015, the exact nature of buried defects in EUV blanks, and hence the appropriate repair strategy, will still need to be determined. In this paper, we demonstrate computational techniques that instead use

supplementary metrology information to effectively predict printability of variety of real defects found in running EUV pilot line production in the mask shop.

The fundamental EUV simulation engine used in this approach is the EUV Defect Printability Simulator (DPS), which uses simulation and modeling methods designed specifically for the individual EUV mask components, and achieves runtimes several orders of magnitude faster than rigorous FDTD and RCWA methods while maintaining adequate accuracy. The EUV DPS simulator is then coupled with supplemental inspection and metrology measurements of real defects to effectively predict wafer printability of these defects. Several sources of such supplementary data are explored here, and, may sometimes be dependent on the actual nature of defect. These sources include 193nm high-NA inspection images and perhaps those even captured through-focus, SEM top-down images and perhaps those even captured with multiple-views or detectors giving estimations of defect depth profile, and AFM height-profile images. From each of these supplemental data sources, the mask and defect information is first extracted or recovered, and then forward-simulated in DPS to generate the EUV aerial images which are then analyzed for wafer printability.

Each of the data sources have their strengths and limitations vis-à-vis use in a production pilot line and we exploit a mix-and-match approach to effectively filter down to the defects that really matter. The 193nm inspection image data are readily available and although the pixel-sizes are somewhat coarse compared with the mask pattern widths, computationally predicting EUV printability off these images provides a quick filter of the obvious false and nuisance defects. SEM images on the other hand provide a much better two-dimensional top-down resolution of the patterns and hence work well for full-height excess or missing absorber defects but not so well for three-dimensional defects such as pits and bumps in the EUV multilayer. The AFM height profile provide the ultimate resolution of patterns and defects for further simulation to EUV, however, tip and image stability, and data acquisition time need to be comprehended.

Computationally exploiting these supplemental defect inspection and metrology data in a somewhat mix-and-match approach, effectively filters defects down to those that really matter to print, thereby providing an effective way of delivering well-characterized EUV masks to the wafer fab.

9050-61, Session PWed

Evaluation of lens heating effect in high transmission NTD processes at the 20nm technology node

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The NTD (Negative Tone Developer) process has been embraced as a viable alternative to traditionally, more conventional, positive tone develop processes. Advanced technology nodes have necessitated the adopting of NTD processes to achieve such tight design specifications in critical dimensions. Dark field contact layers are prime candidates for NTD processing due to its high imaging contrast. However, reticles used in NTD processes are highly transparent. The transmission rate of those masks can be over 85%. Consequently, lens heating effects result in a non-trivial impact that can limit NTD usability in a high volume mass production environment. At the same time, Source Mask Optimized (SMO) freeform pupils have become popular. This can also result in untoward lens heating effects which are localized in the lens. This can result in a unique drift behavior with each Zernike throughout the exposing of wafers.

In this paper, we present our experience and lessons learned from lens heating with NTD processes. The results of this study indicate that lens heating makes impact on drift behavior of each Zernike during exposure while source pupil shape make an impact on the amplitude of Zernike drift. Existing lens models should be finely tuned to establish the correct compensation for drift. Computational modeling for lens heating can be considered as one of these opportunities. Pattern shapes, such as dense and iso pattern, can have different drift behavior during lens heating.

9050-62, Session PWed

Automatically high accurate and efficient photomask defects management solution for advanced lithography manufacture

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Managing mask haze defects is a critical issue, which is more important in advanced semiconductor FABs with immersion lithography process. Mask defects detection usually occurs during mask inspection or, in the worst case, as a result of a yield loss event. Modern FABs have implemented a number of containment actions, such as time- or exposure-based mask inspection. Suspected masks are returned to the mask shop for re-cleaning. But the actions are expensive, time loss and harmful for mask lifetime. The remained question here is how to manage the defects based on our inspection information.

The mask defects located on don't care area would not hurt the yield and no need to review them such as defects on dark area. However, critical area defects can impact yield dramatically and need more attention to review them such as defects on clear area. With the rapid development and decrease of integrated circuit dimensions, mask defects are always thousands detected during inspection even more. Traditional manual or simple classification result is unable to meet efficient and accuracy requirement. This paper focuses on automatic defect management solution using image output of Lasertec X736 inspection equipment and Anchor pattern centric image process technology, SMDD system, to handle large number defects with quick and accurate defect classification result and decision make.

We request system to handle defect into12 defect types including ESD, Particle on clear, clear extension, dark extension, pinhole, pindot and so on. Zero critical defects missing and extended capability to 28nm node even more.

Our experiment includes die to die and single die modes. The classification accuracy can reach 87.4% and 93.3% with 47 and 48 cases within one month test period. No critical defects are missing in our test cases. The missing classification defects are 0.25% and 0.24% in die to die mode and Single die mode. This kind of missing rate is encouraging and acceptable in production line.

The result can be output and reload it back to inspection machine to have further review. This step help user to validate some unsure defects with clear and magnification images when captured images can't provide enough information to make judgment.

This system effectively reduces expensive inline defect review time. As a fully inline automated defect management solution, the system could be compatible with current inspection approach and integrated with optical simulation even scoring function and guide wafer level defect inspection.

9050-63, Session PWed

Design of the phase-shifting algorithm for the flatness measurement of a mask blank glass

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The mask blank glasses, which are used widely in lithography equipment, have been increasing in size to satisfy the requirements of mass production, to reduce costs, and because of the technical advantages of the larger size. As mask blank glasses continue to increase in size, the demand for precise measurement of their properties such as flatness, thickness, and refractive index is increasing. And EUV lithography technology with shorter wavelength is used recently to satisfy the requirement of miniaturization. In EUV lithography, the type of mask glass is the reflection type, so the flatness requirement of the mask glass is more severe than that of the optical mask glass of the ordinary lithography. ITRS table shows the technological requirements of mask glass flatness in detail.

The phase-shifting interferometry has been widely used for surface profile measurement of a transparent plate such as mask blank glasses. In phase-shifting interferometer, the phase difference between an object reflected beam and a reference reflected beam is varied by phase-shifting and the signal irradiance is obtained at the same interval of the phase difference. The phase distribution of interference fringe is calculated by phase-shifting algorithm.

The systematic phase-shift errors, which are caused by nonlinear sensitivity and the coupling between the phase-shift error and the harmonic component of the signal, are the most common source when evaluating the phase distribution. And the phase-shift errors of the multi-layered interference system are more prominent than that of single interference system because of the coupling problem between the phase-shift errors and harmonic component of the multi-layered interference system.

Many studies have been reported on error compensating algorithm which can eliminate the effect of the systematic phase-shift errors. In this presentation, we classify the conventional phase-shifting algorithms according to the immunity nonlinear sensitivity and the coupling between the phase-shift errors and harmonic component of the signal. And we propose new phase-shifting algorithm compensating the coupling between the phase-shift error and the harmonic component of multi-layered interference system as well as the nonlinear sensitivity.

As the analytical approach of the systematic phase-shift error, we choose the analytical error expansion method. We expand the error equation and divide into the two terms of nonlinear sensitivity and coupling. Next, we develop the expression to satisfy the condition to compensate for the coupling between the phase-shift errors and harmonic component. Finally, we develop the phase-shifting algorithm to measure the surface profile of a transparent plate such as photomask compensating the nonlinear sensitivity and coupling problem.

9050-64, Session PWed

Precise CD-SEM metrology of resist patterns at around 20nm for 0.33NA EUV lithography

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As LSI (large-scale integration) patterns are scaled, performance requirements for Critical Dimension (CD) metrology are becoming tighter. CD-SEM (critical dimension-scanning electron microscope) has been a powerful tool for measuring CDs. However, establishing a BKM (best known method) has been a longstanding challenge for the expert users because of the complex requirements to meet both high precision and small resist shrinkage. Optimization of the measurement conditions and tool improvements have been helping to solve this challenge for ArF resist pattern measurements. However, the transition from ArF to EUV lithography may require new methods to establish BKM because the challenging patterning requirements, smaller CDs, tighter pitches and thinner resist materials. The shrinkage of EUV resist materials is smaller than that of ArF resist materials in most cases, but the ratio of shrinkage to the original CD is becoming larger due to the pattern scaling. Therefore, developing a more accurate measurement of shrinkage is required.

In the light of above-described circumstances, we have established an accurate and fast measurement method of resist shrinkage which can be applied to optimization of CD-SEM measurement conditions for EUV resist patterns at around 20 nm created by 0.33 NA EUV tool. In the conventional method, shrinkage is simply defined as CD difference between the first and second measurements. Measurement accuracy of resist shrinkage is about the same as resist shrinkage during the first measurement, and it may change for different measurement conditions. Especially for large dosage conditions, the measured shrinkage by the conventional method is no longer accurate because it shows saturation or decrease of shrinkage due to a large shrinkage at the first measurement. On the other hand, our proposed method can measure shrinkage with a constant and sufficiently small dosage, and a separated electron beam irradiation is applied to induce resist shrinkage as shown in Figure 1. It enables us to measure shrinkage at various irradiation conditions such as electron beam landing energy, magnification, and probe current with fixed measurement conditions. Thus, it is expected that our proposed method gives more accurate shrinkage in a wide range of dosages for various measurement conditions. Resist shrinkage is compared between conventional and the proposed methods, and an example of measured results is shown in Figure 1. The difference in shrinkage is about 0.4 nm at a typical CD-SEM measurement condition of 220 ?C/cm2 (500 V, Mag=300Kx53K, 8pA, and 8Frame), and it becomes larger for larger dosage conditions as we expected.

Size dependence of resist shrinkage was measured down to 20 nm under various landing energy conditions using the proposed method for EUV resist pattern to explore the optimum measurement conditions. The landing energy dependence of shrinkage changed significantly as a function of pattern size, and almost constant shrinkage was observed for all the landing energy conditions at 30 nm and below. The proposed method of shrinkage measurement will help establishing BKM for small feature sizes at around 20 nm.

9050-65, Session PWed

Lithography focus/exposure control and corrections to improve CDU at post etch step

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As leading edge lithography moves to advanced nodes in high-mix, high-volume manufacturing environment, automated control of critical dimension (CD) within wafer has become a requirement. Current control methods to improve CD uniformity (CDU) generally rely upon the use of field by field exposure corrections via factory automation or through scanner sub-recipe. Such CDU control methods are limited to lithography step and cannot be extended to etch step.

In this paper, a new method to improve CDU at post etch step by optimizing exposure at lithography step is introduced. This new solution utilizes GLOBALFOUNDRIES' Run-to-Run automation solution and KLA-Tencor's K-T Analyzer as the infrastructure to calculate and feed the necessary field by field level exposure corrections back to scanner, so as to achieve the optimal CDU at post etch step. CD at post lithography and post etch steps are measured by scatterometry metrology tools respectively and are used by K-T Analyzer as the input for correction calculations.

This paper will explain in detail the philosophy as well as the methodology behind this novel CDU control solution. In addition, applications and use cases will be reviewed to demonstrate the capability and potential of this solution. The feasibility of adopting this solution in high-mix, high-volume manufacturing environment will be discussed as well.

9050-66, Session PWed

The metal ions from track filter and its impact to product yield in IC manufacturing

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The influence of metal ions within track filter on the micro-bridge defect is investigated. We focus on the chemical reaction between immersion ArF photoresist and metal ions and then try to figure out the root cause/mechanism by systematic methods and DOE splits. Micro-bridge defect is produced by immersion ArF resist and metal ions reaction. Track filter with higher level metal extract has higher probability of creating higher micro-bridge level and hence has an impact on defect density. In the experiments, different immersion ArF resists are tested. Eventually, from the outcomes we find out the trend which can well explain the hypothesis. Following the final result, we can easily make prediction before filter inline test. Moreover, optimization of our clean track performance via proper filter selection can be achieved as well. We adopt the new methodology and conclusion at current 28nm node volume production. More interestingly, in the course of investigation we find out a countermeasure which can effectively reduce filter metal extract concentration and which is applicable to next generation lithography. New filter for verification is the next stage CIP(Continue Improvement Project) and we plan to start it in the near future.

9050-67, Session PWed

Advanced broadband optical inspection on complex logic structures using NanoPoint at sub-20nm design nodes

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With shrinking design features the detection of patterning defects on wafer have become more challenging. Cell-to-cell comparison renders array mode optical inspection more sensitive than the die-to-die comparison for logic inspection. Logic structure yield is as important as the array for the chip functionality. Wafer noise limits the logic sensitivity with defect signal embedded in the surrounding noise. A novel NanoPoint technology enables better sensitivity in logic wafer optical inspection. NanoPoint is a combination of innovations in hardware and algorithms implemented on the 29XX broadband inspection platform that is specifically designed to discover and monitor systematic defects, helping yield engineers achieve faster learning cycles during early development for sub-20nm design rule devices. This paper will present fab use cases of NanoPoint for front end-of-line (FEOL), middle of line (MOL) and back end-of-line (BEOL) process modules, enhancing the optical inspection sensitivity in logic regions. This sensitivity is achieved by using very tiny inspection care areas that are derived using NanoPoint technology to define critical regions in a die. Figure (a) explains in detail how NanoPoint enables defect discovery and monitoring. NanoPoint utilizes these micro-care areas in two ways:

1. CBI (Context Based Inspection): Patented technology that utilizes design information to generate targeted care areas surrounding critical regions based on intelligent, user-defined rules.

2. TBI (Target Based Inspection): Patented technology that utilizes the optical properties of the pattern on the wafer to find similar patterns and creates tiny care areas.

Figure (a): NanoPoint enables generation of very small specific and targeted care areas which allows for removal of nuisance generating patterns and inspection of yield-critical patterns

Below are some defects detected using NanoPoint at 20nm for MOL (contact liner) and BEOL (M1 CuCMP). Using traditional optical defect inspection methodologies, these defects have been a gap in detection due to noise limitations. This paper will discuss on how DOI detection is enabled and what potential use cases can be developed using NanoPoint's unique capabilities.

Figure (b): 1. Bridge defect at Contact Liner 2. Bridge defect at M1 CuCMP

9050-68, Session PWed

In cleanroom, sub-ppb real-time monitoring of volatile organic compounds using Proton-Transfer Reaction/Time of Flight/Mass Spectrometry

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When the device feature size reached sub-half-micrometer ranges, Airborne Molecular Contaminants (AMCs) became of particular concern. A case study of photolithography defectivity on Deep-UV tools due to presence of acetic acid in ambient cleanroom and other reactions due to the presence of bases and acids as T-topic effect on resist or haze creation on photomask are reported in literature [1,2].

The adverse effects of Volatile Organic Compounds (VOCs) are also well known, especially in lithography and wet cleaning areas. Indeed, VOCs are particularly problematic because of their abundance, greater mobility, and low vapor pressures. They easily condense on the surface of wafers [3] with reported detrimental impact on the performance, yield, and reliability of semiconductor devices [4,5] or scanner optics [1] with potential irreversible dramatic impact, in case, for instance, of refractory compounds presence such as Trimethylsilanol (TMS).

Several studies were conducted in order to identify and quantify AMCs in cleanroom by witness wafer method [6] or by air sampling on sorbent tubes [7]. To better identify their potential sources and implement solutions, VOCs online real-time monitoring is crucial.

In this study, a Proton-Transfer Reaction/Time-of Flight/Mass spectrometry (PTR-TOF-MS) was used as monitoring tool [8]. This equipment allows simultaneous on-line monitoring of VOCs present down to concentrations of 10pptv in ambient air. The combination of very low detection limit, speed and high resolution provides the ability to analyze a whole mass spectrum in a fraction of a second.

We used this equipment to control the VOCs upstream and downstream of chemical filters used to remove VOCs from the ambient of photolithography zone. We will show the variation in the VOCs levels depending on the process (Figure 1; Figure 2) and demonstrate the added value of such monitoring. For example, results shown in Figure 3 demonstrate that the filters strongly retain the TMS, a compound that is well known to degrade performances in photolithography equipment.

The results obtained with PTR-MS-TOF were then compared with conventional analytical techniques (Figure 4), having low time resolution and including two main steps for trapping and analysis using gas chromatography coupled to mass spectrometry (ATD-GC-MS).

The compared results exhibit a very good agreement for Propylene Glycol Methyl Ether Acetate (PGMEA) and its hydrolysis products as well

as for Toluene. However, regarding the TMS, the amount determined by ATD-GC-MS is five times less than the one measured by PTR-MS-TOF. This could be explained by less favorable interactions between TMS and the adsorbent Tenax TA tube used in conjunction with ATD-GC-MS [9].

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9050-70, Session PWed

AFM image placement accuracy and automation for the next mask manufacturing generation

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Alternating phase shift masks use small differences in quartz thickness to print the fine pitch and features required for today's advanced integrated circuits. To ensure the fidelity of the printed features wafer print, the quartz depth differences must be tightly controlled in mask production. In addition to this tight metrology process control, mask defectivity monitoring and review is increasingly vital to mask viability and will be critical for EUV mask production.

The Atomic Force Microscope (AFM) has sub nanometer depth metrology precision over a range from angstroms to microns. A Critical Dimension AFM (CD-AFM) is not only capable of metrology in the vertical or depth/height direction, but is also capable of CD metrology for line or trench width, sidewall angle, line edge roughness (LER), line width variation (LWV) and sidewall roughness (SWR). These qualities have enabled the technique to be widely adopted as both in-line depth metrology system as well as Reference Metrology System (RMS) in the semiconductor manufacturing industry. In addition, AFM provides key three-dimensional, topographical information for defect review. This additional information permits a more accurate classification of defects and thus a faster time to solution for eliminating the defectivity.

For both metrology and defect review, image placement accuracy is a key factor in the total measurement uncertainty. A reduction in the uncertainty of the image placement insures that the measurement is performed at the desired location. Reducing image placement uncertainty on the previous generation automated AFM (AAFM) required a complex recipe set up that needed a physical representative mask, tool time and an advanced trained operator on the floor. All of these requirements reduced tool availability and degraded lot throughput and operator productivity increasing the tool cost of ownership.

In this paper, we present a new AAFM with key improvements in image placement accuracy and automation for the next mask manufacturing technology node. The tool features a metrology platform containing a high precision interferometer based X-Y stage and a XML based recipe generation system that enables full ahead of the lot recipe off-line generation with design pattern data. These advances eliminate the need to take the tool out of production for recipe generation, pull a representative sample out of the production line and reduce the engineering time for recipe. Data demonstrating the greatly improved image placement accuracy and precision to design pattern data model for alternating phase shift masks will be presented. Finally, a quantitative cost model for offline versus inline recipe generation for AAFM will also be shown to demonstrate the increased productivity and reduced cost of ownership for this next generation AAFM.

9050-71, Session PWed

Optical technologies for TSV inspection

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In the realm of 2.5D/3D packaging, a high throughput/production ready metrology tool with a single high performance sensor that addresses multiple measurement needs throughout the process flow, from FEOL to BEOL can be very valuable in terms of yield improvement, cost of ownership reduction and tools utilization. Frontier Semiconductor will introduce and present data on a new sensor platform we refer to as Virtual Interface Technology (VIT). VIT is a Fourier domain technique that utilizes temporal phase shear of the measurement beam. The unique configuration of the sensor enables measurement of wafer and bonded stack thicknesses ranging from microns to millimeters with measurement repeatability $\leq$ nm and resolution of approximately 0.1% of nominal thickness or depth. We will present data on high aspect ratio via measurement (depth, top critical dimension, bottom critical dimension, via bottom profile and side wall angle), inspect for debris at via bottom, bonded wafer stack thickness; Cu bump measurement.

Using typical VIT signature for TSV sample one can determine via depth, via bottom profile, side wall angle of tapered etch without applying model based analysis. TSV bottom profile can be extracted from VIT signal without the use of modeling. A complimentary tool developed at FSM is a high resolution μRaman method to measure stress-change in Si lattice induced by TSV processes. Applications include via post-etch; via post fill, and bottom Cu nail stress measurements, These measurements are important to determine Keep-Out-Zone in the areas where devices are built so that the engineered gate strain is not altered by TSV processing induced strain. Stress profile between two TSVs separated by 100μm has been measured. Profile measured on several pre and post annealed samples will be presented.

In our presentation, the capabilities of and measurement results from both tools will be presented and discussed in more detail.

9050-72, Session PWed

A new method for wafer quality monitoring using semiconductor process big data

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As the semiconductor industry meets shorter life cycle of new design rule nodes, advanced wafer inspection and metrology techniques are required for the fast driving of process qualification. With an ever increasing number of metrology and inspection steps it becomes more critical to focus on in-situ metrology in order to develop robust processes providing sustainable device yields. Traditionally, metrology of process-driven defectivity is focused on investigating pattern abnormality primarily in the form of particle defects, miss-alignment of each process layers or CD (Critical Dimensions) changes. Conventional semiconductor metrology methods such as optical critical dimension (OCD), CD-SEM (CD-Scanning Electromagnetic Microscopy), bright and dark field optical inspection, and spectroscopic thickness measurement have been effectively used for wafer quality assessment during the production processes. Even destructive method for example transmission electron microscopy (TEM) measurement has been used to visualize under layer profile. However those methodologies generate production loss

increasing number of process steps and destructive treatment of the real products. Thus the need of in-situ process monitoring methodology without additional measurement steps has been requested increasingly. In addition finding main cause of the failure during the process should be advanced by in-situ monitoring.

We now propose a new analysis and monitoring methodology PLAM (Process Log Analysis Metrology) using process big data for the detection of process defectivity especially applicable in semiconductor lithography processes. The research includes development of statistical main cause analysis methodology and monitoring system. Exclusively in this research the process big data includes process log, optically emitted spectrum, fault detection and classification data, measurement data, electrical die sort failure analysis data and etc. Process logs and classification data are usually generated during lithography process and spectrum data are generated by plasma reaction of target material during the etch process. Those data are generated in huge amount, ie. big data, for example more than 5Tera bytes per day in one production line. To analyze the big data it is essential to extract desired data easily and rearrange the data structure in appropriate manner for the analysis convenience. Practically this kind of data handling burden engineers taking more than a month just for data pre-processing. To solve the big data handling problem in pre-processing stage we developed automated data collecting and arranging system which is able to handle large amount of data very effectively. The system has been proved that it provides effective data pre-processing method reducing preparation time from more than 2 month to less than 5 days. Also systematic analysis approach provides fast and concrete generation of result from cumbersome big data. As one of the application we analyzed process big data generated in lithography coating process to verify the process key parameters of specific functional failure using the developed system. It is also proven that the analyzed parameters work as key factor of the defect occurrence showing good correlation with final chip failure result. This study will provide new big data analysis methodology in semiconductor process as well as in-situ quality monitoring technique in various applications.

9050-73, Session PWed

Investigation of a methodology for in-film defects detection on film coated blank wafers

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Multi-patterning is one of the commonly used processes to shrink device node dimensions. With the miniaturization of the device node and the increasing number of coated layers and lithography processes, the needs for defects reduction and control are getting stronger.

Although there are needs for detecting in-film defect during the lithography process, it is difficult to verify in-film defects detected by an optical inspection tool because in-film defect usually appears as SEM-non visual (SNV) during defect review using a scanning electron microscope (SEM). This makes the tuning of optical inspection tools difficult since these defects may be considered as noise. However, if these defects are “real defects”, they will negatively impact the manufacturing yield.

In this paper, we investigate a new methodology to detect in-film defects with high sensitivity utilizing a broadband plasma inspection tool. This methodology is expected to allow the early detection of in-film defects before the pattern formation, hence improving device manufacturing yield.

9050-74, Session PWed

Improving the accuracy of overlay measurements with calibration of wafer-induced shifts

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In the manufacturing of integrated circuits, one of most critical techniques is the measurement of overlay accuracy between patterned layers on a wafer. The overlay measurement is done with specific alignment marks that are etched in to the layers for previous and current steps. The most commonly used alignment marks are concentric squares referred to as box-in-box and x directional, y directional bar. The relative displacement is measured by imaging the alignment marks of the previous and current layers at high magnification with optical microscopy.

The accuracy of overlay measurement connects to overlay measurement system, alignment mark condition and alignment measurement algorithms. Various overlay measurement systems such as visible microscopy, IR microscopy and phase detection microscopy have been developed and successfully applied for monitoring overlay displacement. However, the error source has been generally induced by TIS(Tool Induced Shift) and WIS(Wafer Induce Shift). TIS is created by the asymmetry of measurement optics. Illumination asymmetry may also result in TIS.

WIS is generally caused by the asymmetry of overlay alignment marks due to metal deposition. Keeping the metal asymmetry low is important for measurement accuracy. After metal deposition and CMP process, alignment marks could be deformed and each side wall of the alignment marks has different metal thickness which causes the overlay measurement errors. A peak position of image intensity profile of the alignment marks may be shifted due to asymmetric deposition. Therefore, a calibration technique is required for acquiring the overlay accuracy. To calculate the asymmetry of thin film deposition thickness, we have analyzed the overlay alignment mark captured by an optical microscopy. Each bar pattern has dark areas at the edges of the left and right sides. The width of dark area is connected with the deposition thickness. To enhance the contrast of the dark area signal, edge images are extracted with vertical edge extraction method. The CD1 and CD2 determined by the deposition thickness of the side walls of alignment concave pattern can be calculated by finding out the peak position of the projection intensity profile of the edge extraction image. Each bar patterns has width around 30 pixels and 2?m. In order to measure the very small WIS value below 5nm with low resolution optic image, 7th polynomial fitting process has been applied with 10 points for each peak position. To examine the relation between overlay accuracy and mark asymmetry, we coated the sample wafers which have different thickness of the tungsten metal deposited on the side walls of the alignment mark. Overlay shifts were measured with the proposed asymmetry calibration method. Normal and asymmetric alignment mark have similar signal profile. However, there is CD difference which increases from left side to right side on the wafer. The shift results of overlay values were fluctuated ranging from 0 nm to 7.5 nm. The trend of overlay shift was similar to the deposition asymmetry induced by manufacturing process. The proposed measurement method could detect the overlay shift below 5nm induced by WIS.

9050-75, Session PWed

Across wafer CD uniformity optimization by wafer film scheme at double-patterning lithography process

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The Double Patterning lithography(DPL) process is the well known method to overcome the k1 limit below 0.25, but the pattern final performance (OVL /CD) get more sensitive with the initial core CD uniformity, one of the main factors is across wafer CD uniformity control. Previous improvements applying scanner dose or PEB temperature multi-zone control, the others by the vacuum PEB plate design. In this paper, we adopt different DPL sacrificial layers to modify wafer warpage level, it can adjust a suitable wafer warpage profile, By this method, we can achieve 30% CD uniformity improvement without the scanner dose/ PEB multi-zone heating compensation,

9050-76, Session PWed

Defect analysis methodology for contact hole graphoepitaxy DSA

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Next generation lithography technology is required to meet the needs of advanced design rule nodes. Directed Self Assembly (DSA) is gaining momentum as an alternative or complementary technology to EUV. We investigate defectivity on a 2x nm patterning of contacts and identify a defect density reduction methodology for 25 nm or less contact hole assembly by grapho epitaxy DSA technology with guide patterns printed using immersion ArF negative tone development. This paper discusses the development of an analysis methodology for DSA with optical wafer inspection, based on defect source identification, sampling and filtering methods supporting process development efficiency of DSA process and tools.

As process optimization continues, the analysis methodology for DSA critical defectivity is required to accelerate process and tool development in parallel with traditional process metrics. Currently DSA inspection has challenges in the identification of not only critical defect types but also non-critical and some nuisance defect types.

Defect coordinate based overlay analysis of inspection result from individual process steps, known as defect source analysis, has the potential to separate defects of interest from under layer film or guide structure sources. However, the optimization of this methodology is required for better sensitivity and design rule of DSA.

Each defect detected during inspection has multiple defect attributes such as signal level, size, polarity and brightness. Using a combination of these attributes, we have the potential to separate critical defects. With optimal inspection conditions, we will discuss the ability to generate a more flexible combination of defect attributes, using a hierarchical flow to separate defects of interest. Noise reduction enablers are also identified using both inspection parameters and attributes to improve signal to noise for critical defect types.

The development of a defect sampling methodology is also essential to provide a focus on the critical defect issues. Random sampling has been widely used but when specific defect types dominate does not provide a complete picture of all defect types. We will discuss the development of a weighted sampling methodology, to enable a greater percentage of the sampling budget for critical defect types whilst allowing an adequate sample of non-critical types to generate an actionable pareto. We also discuss a methodology for normalization using defect groups generated from defect attributes to provide an accurate measure for quantification of each defect type.

Defect inspection and sampling requirements change over time from a unit process development, to module integration and finally full flow processing. Advancement of inspection and sampling methods to improve signal to noise provides the opportunity for earlier defectivity improvement of both potential baseline and excursion issues in the process and even tool development. This will facilitate a fast and cost effective integration of this next generation lithography technology into mainstream process flows.

9050-77, Session PWed

Defect analysis and alignment quantification of line arrays prepared by directed self-assembly of a block copolymer

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Self-assembled one-dimensional nanostructures are a class of elements of key technological importance in many areas including electronic and lithography applications, templates, x-ray gratings, photonic crystals, etc. Directed self-assembly (DSA) of block copolymers (BCP) appears in the ITRS roadmap as a potential bottom-up lithography solution for the 11 nm node. Nevertheless, fundamental challenges remain to set standards to enable comparison and reliability studies of dimensions and ordering of these nanostructures. The key for success of a production-compatible nanometrology system is based on reliable, large-area, in-line and robust inspection tools to assure the quality of the fabricated nanostructures.

Here we present an image analysis method dedicated to the analysis of self-assembled nanowires from BCPs, thus 1D features, with feature sizes below 20 nm. The defects identified are dislocations, branching points, lone points and turning points, being depicted in histograms and analyzed statistically according to type. Furthermore, the pitch and linewidth variations are estimated and, in parallel, quantification of the wire alignment and defect density are calculated.

The morphology analysis, defect and alignment quantification of linear patterns, presented here is probably unique at this time. Moreover, the fast response and simplicity of operation positions this technique as a highly promising nanometrological tool to standardize DSA characterization.

9050-79, Session PWed

New robust edge detection methodology for qualifying DSA characteristics by using CD SEM

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Grapho-epitaxy based hole shrink process of Directed Self-assembly (DSA) is one of the candidates for less than 30 nm hole pattern fabrication. The guide patterns of grapho-epitaxy are made by using ArF immersion scanner under the condition of near resolution limit to the 193-nm exposure. Hence, guide patterns have measurable level of edge roughness and edge placement errors. Those errors cause serious size errors and placement errors of DSA hole patterns. RED (Robust Edge Detection) is a new measurement function of CD-SEM for qualifying guide pattern shapes and DSA pattern shapes simultaneously. In this paper, we applied RED for qualifying 1X nm-node hole process, and discuss DSA process control.

RED can catch the slight differences of edge roughness in small size holes less than 20 nm, by using unique algorism for noise reduction and flyer data screening. Additionally, capture image of high density pixel can be applied to multiple DSA patterns and multiple guide patterns in the same FOV (Field of View). Above-mentioned characteristics work out precise measurement of local misalignment, CER (Contact Edge Roughness) and circularity for DSA hole pattern formation.

Furthermore, robust algorism for memory array pattern is being prepared, which cancels noise of electron charging automatically. In addition, this can be applied to logic patterns with another new method using "Grid Metrology". These technologies can be applied to measurement of PS-b-PMMA BCP hole patterns in ArF resist guides. Because ArF resist shows the similar behavior of electron yield as PS-b-PMMA BCP the contour of borders between guide and DSA patterns tends to be unclear for SEM measurement with conventional algorisms. These phenomena are particularly observed for DSA processes with very shallow step height between guide pattern and DSA patterns. The new algorisms enable the SEM measurement of those difficult situation observed in DSA processes.

Measurement results of 20 nm DSA hole patterns are as follows. Automatic measurement success rate is > 95%. It is found that the measurement repeatability of registration, guide pattern's CD, guide pattern's CER, guide pattern's circularity, DSA CD, DSA pattern's CER and guide pattern's circularity are all less than 1.0 nm (3?), respectively. From our experimental results, RED is found to be very effective for qualification of DSA process condition, and then this enables better DSA process control.

9050-80, Session PWed

Laser-based vacuum-ultraviolet light source

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The vacuum-ultraviolet light sources have applications in various scientific and engineering fields, such as semiconductor industry, nanometer processing, and photochemistry. A detailed multilevel non-local thermodynamic (LTE) atomic model is developed to investigate emissivity and absorption properties of low temperature Nobel gas plasmas based on the in-band regions (~ 56±2 nm, 72±2 nm, and 82±2 nm) of the available Yb/Al multilayer mirrors (ref 1). Experimental spectra detected by 1064 nm Nd:YAG laser are presented together with analysis based on calculations using the state-of-the-art relativistic Flexible Atomic Code.

We will present the optimum regions for conversion efficiency (CE) in laser-produced and/or discharge-produced plasmas. In addition, the CE of mass-limited targets against laser parameters including wavelength and pulse width predicted by means of hydrodynamic simulation coupled to developed population kinetics codes. The in-band powers from mass-limited Ar, Kr, and Xe targets predicted based on the current mirrors and available solid state lasers.

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9050-81, Session PWed

An analytical method for the measurement of trace level acidic and basic AMC using liquid-free sample traps

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The measurement of parts-per-trillion (ppt) level acidic and basic airborne molecular contamination (AMC) is essential for process protection and yield control in semiconductor photolithography and adjacent applications.

Real-time monitoring solutions are highly desired, as they provide instantaneous and continuous measurement. However, even the most advanced monitors are only able to achieve detection limits in the low parts-per-billion (ppb) range and many restrictions apply for the detection of acidic AMC. High cost of ownership is another disadvantage.

Discontinuous sampling with sample traps is capable of achieving ppt-level measurement, but the currently accepted methods use sample traps filled with deionized water (impingers, bubblers, beakers) to capture soluble acidic and basic AMC. Inherent disadvantages of these methods are low shelf-life, bacterial contamination, variable capture efficiency as a result of analyte solubility, limitations in flow rate and sample time through evaporative losses, reactions with atmospheric gases, increased sample time to reach desired detection limits and increased probability of in-field contamination through handling the exposed liquid, plus international shipping complications. Some proprietary solid state solutions are available, but usually are very involved in preparation, still limited in detection limits or requiring 24-hour sample duration, or they are protected trade secrets and not available as an industry standard.

To eliminate these disadvantages, Entegris has developed a novel, liquid-free sample trap that allows parts-per-quadrillion (ppq) measurement of acidic and basic AMC within a short, 4-6 hour sampling period. The traps can easily be manufactured and prepared in small lab operations, are completely sealed from the outside and operator handling in the field, have months of shelf life, generally much higher capture efficiency and minimize chemical reactions and other analytical artifacts.

The results for the liquid-free base trap using ammonia (NH3) as a test gas yielded a capacity of more than 200 ppb-h at 100% capture efficiency without any moisture (simulating sampling of CDA or N2). Capacity at 40% relative humidity yielded 350 ppb-h. Given modern supply gas concentrations of less than 1 ppb and cleanroom concentrations of less than 10 ppbV of NH3, that figure translates to a quantitative capture of NH3 for 20-35 hours of sampling at 3.5 lpm, much in excess of was is required for ppq-level analysis. This allows for the sampling of AMC within one work shift and without the need for overnight (typically 12-24 h) sampling.

Several dozen in-field measurements were carried out to compare dry and wet trap performance. Both trap types showed a repeatability of about 5% between measurements. However, impingers showed capture efficiencies consistently 5-20% lower than that of the liquid-free traps (see Figure).

The final paper will show detailed comparison of several AMC types between dry traps and wet impinger traps, in-field validation data and the design of the traps, which we propose to be used as a new industry-wide standard to establish more accurate measurements of acid and base AMC.

9050-82, Session PWed

Analytical method for the measurement of moisture and trace level gas contamination in carbon dioxide

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The latest generation of 193 nm immersion lithography scanner equipment was developed to use purified carbon dioxide (CO2) gas instead of extra clean dry air, to shape immersion liquid and purge exposure lens ambient for contamination free operation. In contrast to air, CO2 dissolves faster in immersion water without forming bubbles that might create exposure defects on wafers.

Determination of gas-phase contaminants in the supply and effluent of CO2 purification systems is essential to evaluate compliance with scanner manufacturer requirements and to avoid potential process impact from moisture as well as acidic, basic or organic trace contamination. We demonstrate suitable analytical methods for accurate, quantitative determination of such trace level gases in CO2.

For economic and supply reasons, the industry appears to be settling

on beverage grade CO2 as the source gas for this application. Whereas suitable for human consumption, beverage grade CO2 is highly contaminated with respect to semiconductor processing environments, and is typically provided at 3.8N (99.98%) purity, potentially leaving 200 parts per million (ppm) of contamination in the gas. Lithography scanner equipment is sensitive to the parts per trillion (ppt) level, one million times less concentrated. For the purification of this gas to become suitable, swing bed purification systems are provided to the industry to remove contaminants. The analytical methods published here are able to validate CO2 supply gas, purification systems and scanner operation to assure contamination-free high volume production.

Specifications for contamination in purified CO2 are similar to specifications published previously for clean dry air and nitrogen supply gases, with required detection limits to determine acidic, basic and organic compounds in the low ppb and mid-to upper ppt range. However, some specifications were lowered, such as the detection of SO2 and silicon-containing organic compounds, which need to be measured at 5 and 1 ppt, respectively, a very challenging specification from both an analytical and logistical (in-field sampling) point of view.

We modified standard analytical methods (GCMS for organic and refractory compounds, ion chromatography for acids and bases, cavity ring-down spectrometry for moisture) to be used for these analyses such that statistically determined method detection limits (MDL; as per SEMI C10-0299) provided enough resolution at the low end to carry out the required detection of low ppt-level AMC. MDL for organic compounds is 600 parts per quadrillion (ppq), that for SO2 is 3 ppt. All other AMC can be measured at the 10 ppt level.

Several challenges are associated with AMC detection at such low levels. One is that sampling in the field requires specialized equipment that has low outgassing and internal contamination, a setup that avoids operator contamination and certified, on-site expertise to apply the methods. Other challenges include the potential formation of ammonium carbamate salt in an excess CO2 matrix, which can settle out in supply and sample tubing, preventing accurate and quantitative detection and potentially contaminate purification system and supply lines over time.

The publication will show findings on the formation of ammonium carbamate as well as results of first in-lab and in-field validations of CO2 purification systems to apply the described methods.

9050-83, Session PWed

A method for the combined measurement of volatile and condensable organic AMC in semiconductor applications

Charles M. Miller, Emily C. Zaloga, Jürgen M. Lobert Jr., Entegris, Inc. (United States)

Monitoring airborne molecular contamination (AMC) at the parts per trillion (ppt) level in cleanroom environments, scanner applications and compressed gas lines is essential process-, equipment- and yield-control.

Current industry standards use sample traps comprised of porous 2,6-diphenylene-oxide polymer resin, such as Tenax®, for measuring volatile (<6 C-atoms, approximately IPA/acetone to toluene) and condensable (>6 C atoms, about toluene and higher) organic AMC. Inherent problems associated with these traps are a number of artifacts and chemical reactions that reduce accuracy of reported organic AMC concentrations. Most importantly, these traps have a poor capture efficiency for volatile organic compounds (VOC) and the break-down of the polymeric material forms false positive artifacts when used in the presence of reactive gases, such as nitrous acid and ozone, which attack and degrade the polymer to form detectable AMC.

To address the disadvantages of polymer-based sample traps, Entergris developed a method based on carbonaceous, multi-layered adsorbent traps to replace the 2,6-diphenylene-oxide polymer resin sample trap type. Entegris proposes to adopt that methodology as a new industry standard to overcome widespread inaccuracy in the reporting of volatile organic AMC and false positive condensable AMC.

Along with this trap's ability to retain VOC, the trap was found to provide artifact-free results. With industry trends towards detecting more contaminants while continuously reducing required detection limits to report those compounds in the low ppt range, artifact-free and accurate detection of AMC is needed at the parts per quadrillion (ppq) level. The proposed, multi-layered trap will accurately capture AMC required by scanner OEMs, and will increase laboratory productivity substantially by eliminating the need to analyze condensable and volatile organic compounds with two separate methods, thus reducing lab overhead and deployment of equipment for two methods.

Permeation sources have been used to study the capture efficiency of volatile and condensable organic compounds. Even some organic compounds with six C-atoms, that are part of scanner OEM requirements, were not effectively retained by polymeric traps, but were fully retained on the multi-layered adsorbent trap (see Figure). This demonstrates that the standard trap used in the industry will result in significantly underreporting actual AMC concentrations for volatile organic compounds, including some siloxanes (TMS, HMDSO, D3).

Performance of the proposed trap was excellent at zero and 50% relative humidity (Table 1), an important metric, as the trap is used for AMC detection in dry supply gases and in humidified environments. We will show recovery and analysis of compounds from acetone to high molecular weight organic AMC and in-field validation data between the two investigated trap types.

9050-85, Session PWed

Handling, clamping, and alignment evaluation for multibeam technology on Matrix1.1 platform

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Multi-beam lithography has already been shown as potential solution for advanced node lithography to extend Moore's law. MAPPER Lithography is developing a maskless lithography technology based on massively-parallel electron-beam writing with high speed optical data transport for the individual driving of electron beam lines. Last June 2013, CEA-LETI received the 1st pre-production platform named MATRIX 1.1, figure 2, and started to evaluate module by module this platform that will operate 1300 beams for an initial throughput target of 1 wafer per hour. [1].

Handling and alignment capability represents two new and innovative aspects among the key points introduced in this new generation system. Concerning handling, the development of massively-parallel electron-beam lithography requires strict temperature control and clamping reliability of the wafer during alignment and exposure for the achievement of good overlay performances. The low costs and small footprint of the MATRIX platform does not allow MAPPER to use conventional handling systems. Mapper developed a new type of handling with a Vertical Transfer Robot. To ensure a reliable wafer handling and clamping process, new modules have been developed. CEA-LETI and MAPPER directly investigates the robustness of the different modules in real manufacturing conditions, including the interface of the MATRIX platform with the SOKUDO DUO track. Results on performances in terms of reliability, repeatability and stability will be reported.

Once clamped and loaded in the exposure chamber, the wafer need then to be aligned prior to the exposure start.

The MATRIX platform integrates the new type of alignment solution developed by MAPPER (figure 1) [2]. This paper will show the first results on alignment sensor repeatability on golden matching wafers and on production wafers. It will report as well on the robustness of the

alignment sensor and the process window for mark reading.

Preliminary results on the overlay performance of the MATRIX platform will be presented and discussion will be engaged to position the MAPPER alignment concept with respect to the ITRS roadmap expectations.

9050-86, Session PWed

Focus control budget analysis for critical layers of flash devices

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As design rule shrinks down, on-product focus control became more important since available depth of focus (DOF) is getting narrower and also required critical dimension uniformity (CDU) becomes tighter. It means that monitor and control the scanner focus error are crucial for reducing the focus control budget of scanner.

In this paper, our study mainly focused on the analysis of intra-field, inter-field focus control budget using both top-down and bottom-up approach as a preliminary study for focus control budget improvement. Target layers of analysis were critical layer of flash devices.

For top-down approach, we introduced product-like-test (PLT) using test stack which is similar to the production stack. 5 lots (4 wafers per lot, total 20 wafers) were exposed for PLT, exposed wafers were measured on ASML Yieldstar which uses scatterometry based metrology for focus readout. Scatterometry based metrology measures sidewall angle and CD on each measurement point and translate into focus values using calibrated model. Focus uniformity components were separated into lot-to-lot, wafer-to-wafer, inter-field, intra-field terms, then the fingerprint and variation of each terms were calculated. Those results were also verified by new diffraction based focus (DBF) method and the results by different measurement method were matched well.

For bottom-up approach, we categorized the factors that affect focus control budget into machine budget and product budget. Machine budget analysis includes inter-field/intra-field uniformity, best focus stability, chuck-to-chuck offset, air gauge leveling measurement reproducibility and product budget analysis includes wafer flatness, intra-field topography, lens heating effect, best focus accuracy for each layers. Bottom-up analysis showed focus uniformity was dominated by inter-field focus uniformity, which can be improved by applying focus height offset, tilts (Rx, Ry) correction per field. Intra-field fingerprint (mainly field curvature, quadratic wedge) which should have been corrected by reticle shape correction remained and it is the dominant factor of intra-field focus uniformity.

As a result, main contributors of focus control budget which could be improved and their potential were evaluated. For the inter-field focus uniformity, the main factor, the potential that it can be reduced by 30% was shown by simulation applying correction per field. Intra-field topography, it can be minimized down to 20% of its original value when assisted with air gauge improved leveling (AGILE). It was shown that reticle shape correction can also be improved by 2 nm (3?) by introducing 9 mark pairs instead of 5 pairs. Expected total improvements of focus control budget for layers were 17.1% and 23.7% each (in 3?) by applying all the solutions we found.

In conclusion, we successfully figured out the main contributors of focus control budget quantitatively, then evaluated the potential improvement for dominant factors. And the total focus control budget of bottom-up analysis corresponds to that of top-down analysis very well.

9050-87, Session PWed

Macroscopic exploration and visual quality inspection of thin film deposit

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The presented work focuses on the quality inspection of thin deposit of self-assembled micro-particles. The interest of the inspection system is that it allows exploring a large area of the deposit (several cm ?) quickly (a few seconds) and simply [1].

Firstly, according to the state of art, the techniques allow characterizing the surface without associating quality value. Secondly, the employed techniques are either from the microscopy with low optical field of view, or they are technically complex to implement such ellipsometry and polarimetry, etc. [2].

It does not propose to replace these techniques to know the surface details. However, it is proposed a much simpler device, composed of cameras and leds lighting on a dome. It allows seeing and exploring macroscopically rendering surface appearance without visual discomfort such as glare or bright environment problems. Its advantage is that customers and industrials agree on the desired quality with a joint view on the product, and to provide a memory of surface. Thus, the quality inspection of thin film deposit is compatible with industrial production deadlines.

Then, the device design explores all configurations to identify the minimum required configuration and to detect surface anomalies. Three parts in the actual execution of device can be distinguished. The light data acquisition and the light rendering construction of deposition make the first two parts of the device. The first part makes use of optical skills, mechanics and electronics for the device design. The second part follows from skills in optics and surface metrology, for the rendering interpolation. The third part concerns the processing necessary to detect thin anomalies. The skills from the image processing / analysis and pattern recognition are used, especially correlation, classification and mathematical morphology [3]. Anomalies have features (size, eccentricity, position on object) to weight quality of deposits.

To justify the relevance of this work, a validation with L2CE laboratory of CEA/Liten, specializing in the field of thin film deposit techniques was performed. This work is completed by a study of monolayer of self-assembled particles made by technology, called BooStream©.

BooStream© (BOtttom-up/tOp-down technique based on a smart STREAM) is a breakthrough technology developed at CEA on the basis of self-assembly at the air/liquid interface. The aim is the online manufacturing over large surfaces (possibility of deposit on miles) [4], hence the importance of knowing how to inspect the deposit quality. In its basic function, BooStream© process allows the realization and transfer of compact film of colloids as Langmuir-Blodgett technique [5], but adapted for the use of small, large, planar, non-planar, rigid or flexible substrates. From the studied deposit, it was made a scale of quality value. Especially, the thin anomalies of aspect surface can be extracted and identified to evaluate the quality of these deposits. These deposits used to in mechanics and lithography to microstructure in DLC (Diamond Like Carbon). The first result allowed reducing of 50% the friction coefficient between mechanical parts.

In addition, these deposits compound particles of monodisperse size, allow calibrating the inspection system quality to know about the information derived by sub- pixel interpolation method.

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9050-88, Session PWed

Wafer surface pre-treatment study for micro-bubble free of lithography process

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Photo resist micro bubble and void defect is reported as a typical and very puzzle defect type in photo lithography process, it becomes more and more significantly and severely with the IC technology drive towards 2x node. Introduced in this paper, we have studied the mechanism of photo resist micro bubble at different in-coming wafer surface condition and tested a series of pre treatment optimization method to resolve photo resist micro bubble defect on different wafer substrate, including in the standard flat and smooth wafer surface and also in special wafer surface with high density line/space micro-structure substrate as is in logic process FinFET tri-gate structure and Nor type flash memory cell area Floating Gate/ONO/Control Gate structure. As is discovered in our paper, in general flat and smooth wafer surface, the photo resist micro bubble is formed during resist RRC coating process (resist reduction coating) and will easy lead to Si concave defect after etch; while in the high density line/space micro-structure substrate as FinFET tri-gate, the photo resist void defect is always formed after lithography pattern formation and will final cause the gate line broken after the etching process or localized over dose effect at Ion IMP layers. The 2nd type of photo resist micro bubble is much more complicated and hard to be eliminated. We try to figure out the interfacial mechanism between different type of photo resist (ArF, KrF and I-line) and pre-wet solvent by systematic methods and DOE splits.

For the 1st situation, in general flat and smooth wafer surface, our experiment major focus on the PR coating step. We tested different type of photo resist from DUV, I-line to ArF under different wafer surface condition as acidity and alkaline surface. The experiment result show us there are several factors such as the surface acidity and alkaline concentration, the resist coating main speed, the RRC(resist reduction coating) priming time, that have strong correlation to resist micro bubble. As is discovered in our paper, the best way to solve the resist micro bubble in general flat and smooth wafer surface is to add 5~10s solvent priming pre-wet step before RRC coating. And the pre-wet solvent is just same as RRC and EBR (edge bead removal) which is easy to realize and maintain in fab process.

For the 2nd situation, in the high density line/space micro-structure substrate as FinFET tri-gate or Nor type flash memory SAS&GP layer which easy to reported of the photo resist void defect, we major focus on the pre-treatment before photo process. Two pre-treatment method reported in this paper, one is PECVD N2O pre-treatment, which reacts with Silanol and is decomposed into H2O/N2/O2 gas to volatile out ; the other is high temperature 1800C high temperature Pre-bake, both are proved to be useful to solve the photo resist void defect(micro bubble) trapped in logic process FinFET tri-gate or Nor type flash memory GP&SAS layer. And the PECVD N2O pre-treatment is the best solution with longer process queue time and better defect stability that final used in SMIC all tech node Nor-type flash memory cell structure with photo resist stand on high density line/space micro-structure substrate.

Finally, we succeeded to dig out the best solution to eliminate the micro bubble defect in different wafer surface condition and implement in the photolithography process.

9050-89, Session PWed

Characterization of e-beam patterned grating structures with Mueller matrix polarimetry

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As a non-imaging optical measurement technique, Mueller matrix polarimetry (MMP) has been introduced for critical dimension (CD) and overlay metrology with recent great success. Compared with conventional ellipsometric scatterometry, which only obtains two ellipsometric angles, MMP-based scatterometry can provide up to 16 quantities of a 4?4 Mueller matrix in each measurement. Consequently, MMP can acquire much more useful information about the sample and thereby can achieve better measurement sensitivity and accuracy. In this paper, we use MMP to characterize e-beam patterned grating structures with small CDs. The factors that affect the final measurement accuracy are fully investigated, which include the geometric models applied in the fitting process, the spectral range, and the depolarization effects. It is demonstrated that significant improvement in the final reconstructed structural parameters is achieved after taking the above factors into account.

9050-90, Session PWed

Run-time scanner data analysis for HVM lithography process monitoring and stability control

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There are various data mining and analysis tools in use by high-volume semiconductor manufacturers throughout the industry that seek to provide robust monitoring and analysis capabilities for the purpose of maintaining a stable lithography process. These tools exist in both online and offline formats and draw upon data from various sources for monitoring and analysis. This paper explores several possible use cases of run-time scanner data to provide advanced overlay and imaging analysis for scanner lithography signatures. Here we demonstrate a powerful and flexible user friendly solution for monitoring, analyzing and stabilizing lithography processes based on KLA–Tencor solutions and GLOBALFOUNDRIES infrastructure.Such a system could be useful for performing a variety of analyses and would provide a visualization of key lithography process parameters. Applications include high order wafer alignment simulations in which an optimal alignment strategy is determined, dynamic wafer selection, reporting statistics data & analysis of the lot report, and scanner fleet management (SFM)

9050-91, Session PWed

Isolation grooves scatterometry simulation with GPU and groove shapes optimization

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Scatterometry is capable of measuring the critical dimension and profile measurements of grating structure.It is possible to get down to approximately 16nm with high precision in semiconductor manufacturing process control. When the measurements are actually taken on the wafer's grating structures, we find the simulated signature to match closely with the measured signature. The quality of results depends on the measurement setting parameters, and on algorithms used by the analysis software. However, the scatterometry equipment is very expensive, and it cannot easily check the measurement's performance. In the papers on Microlithography in 2004-2008, we completed the

3D-FDTD analysis of the arbitrary shapes for isotropic and anisotropic mediums. In Microlithography 2010-2012, we developed the scatterometry simulation software that has the spectroscopy calculation and optimization algorithm systems. We calculated the spectroscopy using the Rigorous Coupled Wave Analysis that provides a method for calculating the diffraction of electromagnetic waves by periodic grating structures. The Conjugate Gradient and the Binary-Coded Genetic Algorithm methods were used to automatically search data that matches the given spectrum. In 2013, we sped up the scatterometry simulation for the 3D RCWA by using GPU and CUda LApack. The data movement between CPU and GPU memory takes time. So, when there's a low calculation amount, the results were not obtained using CULA. The 3D RCWA needs a big matrix and the calculation times were quicker by about 12-13% for the higher modal numbers over 10. Next, the 2D scatterometry simulator was improved using a Real-Coded GA. We used the RCGA to increase the population, to make a more sensitive solution and to get better fitting groove figures. The scatterometry characteristic was examined by choosing the n-th power cosine type period groove and approximating the smoothly changing groove shape with four trapezoids. As the result, the reflection characteristic for both TE mode and TM mode almost agreed with the purpose reflection characteristic.

In this paper, we continue to speed up the scatterometry simulation software and improve the performance. In 2013, we calculated most parts of 3D RCWA calculation on CPU and only matrix calculations on GPU using CULA, and the calculation times were quicker by about 12-13%. In this paper, we calculate most parts of the 3D RCWA and GA calculations on GPU using CUDA. We proceed the multi-thread parallel computing using CUDA on 4 sets of NVIDIA Tesla C2070 GPU (448 cores) because the direct memory exchange became possible without using CPU from CUDA4.0. The scatterometry characteristic is examined by choosing the n-th power cosine type period groove. Then, the calculation times are quicker by about 20 times for the higher modal numbers over 10. Next, the 2D scatterometry simulator is developed for the isolated grooves using RCWA and Perfectly Matched Layer. RCWA is usually used for the period grooves and the scatterometry is now used for measuring the period groove shapes. Here, we try to examine the sensitivity of scatterometry for the isolated groove shapes. Finally, we apply the scatterometry simulator in order to get optimum groove shapes to fit a desired scattering characteristic. The optimum design of the groove shapes which control zero order and higher modes is important in various fields. Then, the simulation results are shown.

9050-92, Session PWed

Deep-level data fusion for CD metrology: Heterogeneous hybridization of scatterometry, CDSEM, and AFM data

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Next generation semiconductor devices manufacturing imposes to metrology tool providers an exceptional effort in order to meet the required targets of precision, accuracy and throughput stated in the ITRS. Such challenges will generate additional risks and cost for IDMs and foundries aiming ever better devices to ensure their economic viability.

Data Fusion is the Art of gathering, combining and processing heterogeneous data containing different level of information to produce the best measurements or decisions. For several years, Data Fusion for metrology, also named Holistic Metrology, Hybrid Metrology or Combined Metrology is considered has a must for next generation metrology methodologies. However, several paradigms are possible with various advantages and drawbacks, and no clear comparison has been reported.

In this contribution, we provide a detailed analysis of Deep Level data fusion involving scatterometry, CDSEM and AFM metrology by universal computational techniques. Results are demonstrated for sub-28 nm CD metrology. Such approach is paving the way to cycle time reduction and yield ramp enhancement

9050-93, Session PWed

Accurate contour extraction from mask SEM image

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Photomasks for 193nm optical lithography have complicated optical proximity correction (OPC) patterns, and the metrology for these patterns is key technology as well as conventional CD measurement. The lithography simulation based on the contour extraction from the SEM images on photomasks is one of the methods to assure OPC patterns.

We investigated the function of the contour extraction of mask SEM image captured Mask CD-SEM 'Z7,' the latest product of HOLON.

In this paper, we will explain the function of the above-mentioned contour extraction, and the performance requirements for the CD-SEM for this function. Furthermore, we will outline the perspectives of the application of our contour extraction method.

The wide image size (for example, more than 16?m x 16?m square [1]) is used for simulation. The field of view of SEM images, however, is restricted and it is impossible to cover all areas required to carry out the simulation. Accordingly, we capture the most important areas into SEM images, as "hotspots," output their contour extraction data in GDSII / OASIS format, embed them onto the GDSII / OASIS design data, and conduct Lithography Simulation. When performing the embedding, the important thing is to make sure that GDSII / OASIS data of the contour data of SEM and design data match with sufficient accuracy. To realize this, it is important that nonlinear distortion of the SEM image is kept at the minimal level. Moreover, it is necessary to carry out high-precision corrections on linear distortions, such as position shifts, magnification changes, and rotational changes which occur by various hardware factors.

In order to solve this problem, we at first evaluated how much nonlinear distortion was present in Z7 SEM images. As a result, it turned out that the gap of the center positions of 49 arranged holes in 8?m SQ was less than ±1nm, after conducting linear corrections. This proved that if the linear distortion could be corrected, it could be used for Lithography Simulation. We therefore developed a function which could correct the linear distortion of extracted contour data of SEM images with high precision on the basis of the design data. First, measurable parts are detected and determined automatically from design data in horizontal and vertical directions respectively. The coordinates points of the contour data of SEM and design data in the set-up measurement parts are clipped, the center coordinates of each measurement part are computed, and the correction values of shift, magnification, and rotation are calculated based on those data. And the contour data of SEM is recalculated and outputted based on such correction value.

This correction method realizes a highly precise matching with design data, because it not only corrects the rotation and magnification changes based on focus change and the rotation error at the time of loading of a mask, but also corrects errors based on other sources such as magnification changes of SEM by the mask pattern coverage. In addition, we are considering that highly precise CD measurements will become feasible by applying this method for usual CD measurements. Moreover, since this method enables highly precise superposition of the contour data of a design and SEM, we will be able to carry out 2D measurements at much higher reproducibility.

9050-94, Session PWed

Accuracy improvement of overlay measurement

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In the current overlay measurement, the difference between overlay error measured on the overlay target and the overlay error of the real device emerging through processes appears to be a serious problem.

The mismatch between the overlay of device pattern and the overlay of the overlay target can cause the decrease in overlay control accuracy of semiconductor device, and therefore it can lead to yield loss. To resolve this issue, Critical dimension scanning electron microscope (CD-SEM) is now attracting attention as a tool that can accurately measure overlay error of device patterns [1]. The bias between target-based overlay results and device overlay can be quantified by high resolution measurement using CD-SEM. Thus, it becomes possible to correct target-based overlay results, which are widely used to determine overlay errors.

However, the measurement accuracy can get worse due to overlay mark asymmetry as in the case of image based overlay (IBO) and diffraction based overlay (DBO). The measurement uncertainty is caused also by measurement tool itself. In addition, there exists the interaction between tool-induced inaccuracy and target-induced inaccuracy as a factor of decreasing CD-SEM measurement accuracy. Thus, to evaluate measurement error caused by mark asymmetry, it is important to divide tool-induced error and target-induced error, and analyze the influence of each factor on the measurement error statistically. For IBO and DBO, a systematic way of correcting the inaccuracy arising from measurement patterns was suggested [2]. For CD-SEM measurement, on the contrary, although a way of correcting CD bias was proposed [3], it has not been argued yet how to correct the inaccuracy arising from overlay mark asymmetry using CD-SEM itself. In this study we propose how to quantify and correct the measurement inaccuracy affected by overlay mark asymmetry.

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9050-95, Session PWed

Mean offset optimization for multipattering overlay using Monte-Carlo simulation method

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The overlay (OVL) mean offset of each exposure for multi-patterning OVL is critical to yield. Mean offset specification (mean spec) for rework is needed. However, setting mean spec tighter than necessary will cause a high rework rate which is not cost effective. Currently, there is no established method available to optimize mean spec and thereby minimize the rework rate.

We have developed a Monte-Carlo simulation method to simulate multi-level OVL. By simulation results, we investigated the details of how the mean offset of each level affects final OVL performance.

Based on simulation results, we have found: (1) Contributions of mean offset of previous levels to the final VOL are dependent on mean offset value, exposure sequence, and alignment strategy. For example, for LELELE as previous level, the simulation result is shown in Figure 1. The mean offset of exposure C contributes more to the final OVL than exposure B resulting in an individual mean spec for each level. (2) The combinations of mean offset of previous level make the optimized mean offset value of following layer vary. As shown in Figure 2, if the last exposure is D. In the optimized mean offset of D smaller is not always better. Therefore, the mean spec of next level should be set based on previous levels. (3) The best OVL performance is also dependent on the reference location of alignment. Two reference strategies for alignment are shown as examples in Figure 3. The best strategy is also depends on the mean offsets of previous levels.

Based on the simulation results, we propose the Dynamic-Mean-Offset (DMO) method which can achieve an optimized OVL performance that will sustain high yield while minimizing rework rate.

9050-96, Session PWed

Lithography develop process electrostatic discharge effect mechanism study and process optimization

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Electrostatic discharge (ESD) problem resulting from charges on wafers is a serious concern in IC manufacturing. In the photolithography process, ESD charge effect is mainly considered during the mask making and reticle maintenance but seldom be noticed in the lithography process flow itself. As is discovered in our paper, 2 types of defect, AA (active area) damage and IMD (Inter Metal Dielectric) crack that are confirmed to be induced by lithography process related ESD charging effect. We carefully studied the mechanism of these ESD charging effect by DOE splits and succeeded to dig out that these electric charge major comes from the lithography develop process. In the lithography coating and developing wafer process, the wafer will be at high spin speed at many of the steps which will easy help to store the electric charge on the wafer. In our study, the rinse step in developing process is the most key factor to store the electric charge on wafer. In generally, the higher rinse speed, the higher positive electric charge. Furthermore, we also discovered that the different step in develop rinse process have different impact on charge level, in which the acceleration and deceleration step has the highest charge voltage.

In fab process real situation, there are 3 major types of ESD charge effect was discovered. The 1st type ESD charge effect is discovered in the thin oxide layer such as DG (dual gate) and LDD (light doped drain) layer , this type ESD charge is detected as pin hole or poly/gate oxide/AA(active area) burn out, and tightened KLA scan recipe help us to catch this type of ESD charge in-line; The 2nd type ESD charge effect is discovered in the IMD layer during Via photo process , this type of ESD charge is reported as IMD crack with worse wafer center defect map which can be easy detected by in-line defect scan; While, the last type of ESD damage discovered in Al BEOL metal layer process is the hardest to be detected and identified, this type of ESD charge has no any defect signal in Litho in-line process detection methodology , but it will finally neutralize the metal etch O2 plasma which may have influence on Al etch galvanic corrosion effect with early fail from wafer edge. Of these 3 different type of ESD charge effect, no matter what is the different defect type and failure mechanism in different process step, the most key process factor to dominate ESD charge in photo process is just the develop rinse step. As is in our study, with the wafer surface condition change, different process will have different optimized develops rinse speed range.

As to minimize and eliminate the ESD damage in lithography process, we finally carry out the simplified recipe optimization solution which only need optimize for the develop rinse speed with different in-coming surface charge level and process application, so that can be easy implemented in the worldwide fabs

9050-97, Session PWed

20nm middle-of-line overlay case study

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The ITRS roadmap for lithography calls for an overlay budget of about 5nm (3 sigma) for DRAM and logic going into 2014. This value gets much tighter for double patterning layers. The specification of the NXT immersion tools is about 4.5 nm for machine to machine and 2.5 nm for dedicated machine and dedicated chuck overlay. Although from the tool specification, the ITRS target seems achievable; an increasing part of the overlay budget is consumed by contribution from process. This is especially evident during the technology development phase where a

large number of experiments on wafers poses a challenge to the overlay control strategy.

In this paper we look at the various overlay challenges faced at the Middle of line (MOL) to poly layer in the 20nm node and the steps taken to mitigate the effects of these issues to improve overlay margin. The overlay is measured between the TS layer and the Poly layer, the TS layer provides a contact path to the active regions of the transistor and must be precisely aligned so as to not cause shorts with the metal gate. The problems can be broadly categorized into three categories, measurement uncertainty due to process impact on target, variation in target quality within wafer due to process variation, and process related wafer to wafer variation in overlay signature.

Due to lack of sufficient segmentation and surrounding dummy features it was found that the blossom targets used to measure were susceptible to the CMP process. The blossom targets for the previous layer are made of the metal gate and due to insufficient margin in the CMP process, we observed a correlation between the gate height and the overlay measurement. The sampling strategy called for 8 sites per field with the measurement locations being at the four corners and four intrafield locations. It was seen that due to density differences in the pattern surrounding the intrafield locations some sites exhibited a different signature compared to the other intrafield sites. The problems in overlay measurement were further exacerbated due to the use of a TiN hardmask which greatly reduced the contrast of the previous layer marks.

The measurement related problems have been greatly reduced by addressing each of these concerns. Across wafer gate height uniformity was improved by moving to a low down force CMP process shown in Fig 1. The figure shows comparison between wafers with same gate heights with and without the LDF CMP process and the resulting overlay values. Switching to the green filter on the metrology tool increased the measurement accuracy and provided an improvement of upto 30% in the residuals. The use of a softmask in lieu of the TiN hardmask further improved the contrast of the previous layer. We also looked at the asymmetry of the measurement target and changed the intrafield selection by measuring different wafers with varying gate heights and selecting target locations which exhibited low Qmerit scores across various gate heights. This trend is shown in Fig 2 below where the M+3S value of overlay and the gate height are indicated. As the gate height increases the overlay value decreases.

In order to address the wafer to wafer and lot to lot variation, the alignment on the scanner was modified to use the Higher Order Wafer Alignment which reduced wafer to wafer variation. To meet the stringent specification of this layer we had to increase the intrafield sampling to apply CPE and iHOPC on a per lot basis. Various schemes to address the wafer to wafer variation from the process integration side are ongoing.

9050-98, Session PWed

Metrology of advanced N14 process pattern split at lithography

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In advanced semiconductor N14 process, due to the requirement of shrinking the pitch, pattern split is introduced. However, either two of the pattern split methods, SADP (Self-aligned double patterning) and LELE (Litho-Etch-Litho-Etch) has the drawback which might cause the “pitch walking”. Pitch walking is a product while SADP has a CD or spacer error or LELE has overlay deviations. Pitch walking does not only result in the different line spaces but also affect the later steps, ex: etch different depth and CDs. Because of pitch walking, it is challenge to control the CD for better CD uniformity. This paper demonstrates how to use OCD (Optical Critical dimensions) tools to measure the different critical dimensions and spaces which can be advantageous to verify the CD and overlay in the metrology tool at the same step. Traditionally, wafers have to go through both CD metrology tool and overly tool in order to verify CD uniformity and grid uniformity. The methodology introduced in this paper can efficiently shorten cycle time since only CD metrology tool will be the reference for verifying both CD and overlay. SpectraShape is a proven optical CD tool based on spectroscopic ellipsometery. In optical model type metrology, pitch walking can be an item with very low sensitivity to measure. Hence this demonstration will be performed on new generation platform: Spectrashape 9010. Spectrashape 9010 has a new light source, LDLS (laser driven light source), which provides high intensity and better signal to noise ratio. With this light source and improved optics Spectrashape 9010 has a very good capability to measure pitch walking, the very insensitive measured item.

9050-99, Session PWed

Development of UV inspection system on the defect of electrode for 5um level multilayer pattern

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In General, OLED, LCD, TSP Glass Pattern consists of multi- layer of electrodes separated by a thin insulating film and layers are very close to each other. Using image at the visible light (550nm above) for the inspection of electrode pattern & defect is difficult to define among layers. So the inspection of electrode pattern & defect by using images at the visible light (550nm above) is not easy to define among layers. Cause of deep depth range in conventional visible optics. This study uses UV wavelength that has larger reflectance gap between different materials than visible light, to increase image contrast. New development of optical system and image analysis units are focused to the proper inspection wavelength at the UV range to clearly define a top electrode layer and reduce image processing time. Final image shows good selective contrast and resolution between layers even in the high depth condition followed by required NA for the target resolution.

1.Introduction

In general, display panel is made up of Gate, anode, cathode, organic and passivation layers. Light reflection and absorption rate at the layer surface depends on the material and wavelength of illumination. Almost all the metal (conducting material) surface has similar hi-reflectance at the long wavelength (IR) and even shows lower than 20% difference at the visible light. However, they show relatively big difference in reflectance at the UV wavelength (max 60%; refer to the Fig.1.). 1, 2 And especially, organic and passivation layer materials have high UV absorption rate at the UV. [40 % nominal] So, UV imaging with specific wavelength and intensity between 350nm and 450nm can be used for selective imaging among layers separated with sub-micrometer thickness.

2.Contents

A scanning image system with linear CCD of 63mm length and 5.2um size pixel is used. To detect defects on the electrode, the resolution of the optical system should be much higher than the spatial frequency of the electrode size. After considering system requirements, two types of different magnification systems (1.8 X and 3X) are developed.

Direct side illumination is available in 1.8X system which has large back focal length, however, 3X system needs on axis illumination. Line beam illumination from the multi-point LED source (custom made) is used to increase the light efficiency and decrease noise.3

Illumination beam passing through common objective lens (front part of imaging lens) and included cylinder lens is realized 1 dimensional Fourier plane on the surface of target electrode and the beam uniformity is within 3%.4 Abstract of optical specification is presented in Table1. Lay out of imaging and illumination system is also presented in Fig. 2.

Electric units for high speed data processing & transfer and image processing algorithm are also developed. For processing large capacity image data (2Gbyte) synchronized with moving sensors in real time,

embedded system with hardware optimizing design and FPGA module camera are adopted. This inspection system can be used in inspection of PCB Pattern, LCD, OLED, Mobile Glass, including many other film and glass.

3.RESULTS AND DISCUSSION

Final results and more detail information will be presented at the conference.

9050-100, Session PWed

Scatterometry performance improvement by parameter and spectrum feed-forward

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Advancements of manufacturing processes continuously bring new opportunities and challenges for critical dimension (CD) metrology to characterize a large variety of device structures at critical process steps. Optical CD metrology using scatterometry has been widely adopted for fast and non-destructive in-line process control and yield improvement. Recently there has been increased interest in metrology performance enhancement through a holistic approach. In this work we investigate the benefits of feed-forward of metrology information from prior process steps using a sample from magnetic hard disk drive manufacturing. The measurements are performed on scatterometry targets at post develop and post reactive ion etch (RIE) steps. The scatterometry targets are composed of rather isolated gratings that are designed to have better correlation with device features. The scatterometry challenges come from low sensitivity and parameter correlations. The utilization of metrology information from previous steps can be done with two methods: parameter feed-forward or spectrum feed-forward. In parameter feed-forward scheme, measurement results from previous steps are passed onto the measurements at later steps, i.e., the corresponding parameters are fixed at the results measured from previous steps. It effectively breaks parameter correlations and improves the overall measurement quality. In spectrum feed-forward scheme, spectra collected from previous steps are passed onto the measurements at later steps. For the measurements at later steps, two structures, one from previous step, one from the current step, are modeled simultaneously with corresponding parameters coupled together. Spectrum feed-forward is expected to deliver enhanced sensitivity and reduced parameter correlation. We demonstrate improved measurement accuracy and precision using parameter or spectrum feed-forward.

9050-101, Session PWed

Spectroscopic critical dimension technology (SCD) for directed self-assembly

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Directed self-assembly (DSA) is being actively investigated as a potential patterning solution for future generation devices. While SEM based CD measurement is currently used in research and development, scatterometry-based techniques like spectroscopic CD (SCD)are preferred for high volume manufacturing. SCD can offer information about sub-surface features that are not available from CD-SEM measurement. Besides, SCD is a non-destructive, high throughput technique already adopted in HVM in several advanced nodes.

The directed self assembly CD measurement can be challenging because of small dimensions and extremely thin layers in the DSA stack. In this study, the SCD technology was investigated for a 14 nm resolution PS-b-PMMA chemical epitaxy UW process optimized by imec. The DSA stack involves new materials such as cross-linkable polysterene (XPS) of thickness approximately 5 nm, ArF immersion resist (subsequently removed), -OH terminated neutral brush layer, and BCP material (Polystyrene-block-methyl methacrylate of thickness roughly 20 to 30 nm). The main portion of the mask design contains three blocks of guide patterns with multiple pitches. While these blocks are designed for optimizing the patterning performance, they can also be used for characterization of SCD metrology. The block of guide pattern with 84nm pitch results in a 3X multiplied pitch of 28 nm (14 nm Line/Space) after DSA annealing step. The experimental data collected is at 'post-PMMA removal' step which is one of the most critical steps in the DSA process. In addition, the mask also contains a large CD and pitch matrix, for studying the quality of self-assembly as a function of the guide pattern dimensions. We report on the ability of SCD to characterize the dimensional variation in these targets and hence provide a viable process control solution.

9050-102, Session PWed

SEM-contour shape analysis method based on pattern structure for advanced systematic defect inspection

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We developed a practicable measurement method which contributes to reliably perform systematic defect inspection for advanced semiconductor devices. A kind of systematic defects due to design-process and mask-process is a dominant component of integrated circuit (IC) yield loss in nano-scaled technologies. Therefore, it is required to detect systematic defects definitely at an early stage of a wafer fabrication. In the past, these circuit pattern shapes have been evaluated by the human eyes or taking manual Critical Dimension (CD) measurements. However, these operations are sometimes unstable and inaccurate. Last year, we proposed a new measurement method by using a SEM-contour. This method enables a highly precise quantification of various complex 2D shaped patterns by comparing a contour extracted from a SEM image using a CD measurement algorithm and an ideal circuit pattern.

We improved this method for realization of the inspection suitable for every pattern structure required by process margin minimization. This method measures a circuit pattern using information about structure of the ideal circuit pattern shapes and layers. As a result, it was confirmed that a critical defect of a connecting part of upper (lower) layer circuit and a high-density part were detected by this method. This improved method and the evaluation results will be presented in detail in this paper.

9050-103, Session PWed

Innovative fast technique for checking overlay accuracy with ASC (Archer self-calibration)

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Overlay metrology challenges can be attributed to Total Measurement Uncertainty (TMU), Design rule compatibility, Device correlation & Measurement Accuracy. With process impact in overlay metrology for 2x nm node and below becoming more critical due to challenges in the management of shrinking overlay budgets, a methodology is needed

to check the accuracy of target/metrology settings before baseline establishment. In this paper, we present a study of a fast technique to estimate overlay accuracy.

A propriety quality metric based on measurement asymmetry, Qmerit, is used to show process impacts across various target/metrology settings. An advanced version of the quality metric, Qmerit by layer, allows separation of current and previous layer behavior such that we can identify which layer or have an indication of which stage of the processes contribute to an impact on overlay target and its accuracy. Using this quality metric we can quickly eliminate target/metrology candidates showing the most process impacts. Furthermore, based on the quality metric, an innovative fast calibration technique, ASC (Archer Self Calibration), is used to estimate the inaccuracies with each target/metrology settings.

In this study, data is collected for each target/metrology combinations at the ADI & AEI stages to check how processes/ film stacks between these stages impact the overlay accuracy. Based on the inaccuracy estimates, best candidates were selected for ADI & AEI and verified with electrical tests.

9050-105, Session PWed

Overlay improvements using a real-time machine learning algorithm

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While semiconductor manufacturing is moving towards the 14-nm node using immersion lithography, the overlay requirements are tightened to below 5-nm. Next to improvements in the immersion scanner platform, enhancements in the overlay optimization and control are needed to enable these low overlay numbers. Whereas conventional overlay control methods address lot and wafer variation autonomously with wafer alignment and post exposure metrology, we see a need to reduce lot and wafer to wafer variation by correlating more of the TWINSCAN's sensor data directly to the YieldStar metrology in time. In this paper we will present the results of a study on applying a real time control algorithm based on Machine Learning Technology. Machine learning methods use sensor data from the TWINSCAN paired with YieldStar metrology to recognize generic behavior and train the control system to anticipate on this generic behavior. Specific for this study, the data concerns immersion scanner sensor data and on-wafer measured overlay data. By making the link between the scanner data and the wafer data we are able to establish a real time systematic relationship. The result is an inline controller that accounts for small changes in scanner hardware performance in time while picking up subtle wafer to wafer deviations coming from process.

The immersion scanner used is an ASML NXT:1950i system and the overlay measurements are done with in-line YieldStar T200 using diffraction based overlay targets.

9050-106, Session PWed

Method and system for real-time overlay measurement using fluorescent markers

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In lithography, overlay control is getting increasingly complex [1]. Advanced Process Control uses metrology data of previously exposed wafers to minimize excursions from the process window for the present exposure. Unfortunately, there is always a delay of tens of minutes before the information is available. This paper proposes the combination of a patterned expose beam and a patterned fluorescent marker on a wafer to generate a fluorescent signal that carries real-time information of the overlay of the expose pattern with the pattern on the wafer [2]. This enables monitoring overlay during exposure. The signal can also be used to improve position control of wafer and/or reticle during exposure, and thus improve the overlay (and thereby yield), especially for multiple patterning processing.

A practical realization requires some changes to the exposure process, stepper design and reticle lay-out. Firstly, a matched pair of markers on the wafer and reticle is required. The absorber pattern on the reticle patterns the expose beam. The overlap of the patterned beam with the marker on the wafer generates a fluorescence signal that represents the (error in the) overlay, see e.g. Figure 1. The exact pattern design can vary, but will typically contain an (at resolution) grating and may consist of multiple smaller markers that each addresses a direction of the overlay error. The markers for the different directions can be read out in a time-multiplexed way. With advanced spatial designs of the markers, the fluorescent signal strength can be optimized for maximal overlay measurement accuracy. Secondly, the generated fluorescent signal must be measured, for example with a (spectrally filtered) photon counter close to the expose area of the wafer. A high collection efficiency of the detector is needed for a strong and reliable overlay signal. At last, the markers from the previous lithography step shall, after development, be filled with fluorescent material. This deposition requires an additional process step.

Photon budget calculations suggest an overlay measurement accuracy of less than a nm (real-time), see e.g. Figure 1.

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9050-108, Session PWed

High-precision self tool CD matching with focus target assist pattern by computational ways

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As design rules of advance devices shrink, not only process-window budget of lithography process is getting tight, but also CD control to target on multiple tools is getting important for HVM (High Volume Manufacturing) process. CD bias or CD difference among tools can be caused by minute residual differences in imaging parameters after regular control. The CD differences can be reduced to sub-nanometer scale for critical features by using matching tools such as LithoTuner PMFCTM. During the CD matching process, the tool uses tunable imaging parameters as matching knobs and provides new settings that user can apply to exposure process. However, the perceived CD bias can be impacted by further imaging-related system parameters with CD sensitivity as in the case of focus control. By considering the focus impact on CD proximity bias via computational method, the matching between tools could be accurately performed and estimated.

In this study, best-focus indicator pattern (BFI) is selected within marginal process window range by rigorous M3D simulation considering focus sensitivity and relative amount of best-focus shift among the patterns of concern. This choice of BFI allows us to minimize the variation of CD proximity bias induced by the focus variation coming from intrinsic performance of chuck and leveling, chuck to chuck, scan-up & down, and tool-tool difference. Fig 1 and Fig 2 is showing simulation

comparison of proximity CD change to understand how much such focus variation could give impact on CD variation even at pre matching stage. We compare the results with and without BFI focus targeting for multiple critical features for a sample case (Unit of Y axis is arbitrary, same scale for both plots). We observe ~ 40% improvement of tool-to-tool CD matching performance using BFI pattern as focus target pattern in this specific case. Tool-to-tool CD matching performance with BFI will be also compared on L2x devices.

9050-109, Session PWed

In-line focus monitoring and fast determination of best focus using scatterometry

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Persistently shrinking design rules and increasing process complexity require tight control and monitoring of the exposure tool parameters. While control of exposure dose by means of resist single metric measurements is common and widely adopted, focus assessment and monitoring are usually more difficult to achieve. A diffused method to determine process specific dose and focus conditions is based on plotting Bossung curves from single CD-SEM metric and choosing the best focus setting to obtain the desired target CD with the widest useful window. With this approach there is no opportunity to build a data flow architecture that can enable continuous focus monitor on nominal production wafers. KLA-Tencor has developed a method to enable in-line monitoring of scanner focus on production wafers, by measuring resist profile shapes on grating targets using scatterometry, and analyzing the information using the AcuShape and K-T Analyzer software. This methodology is based on a fast and robust determination of best scanner focus by analyzing focus-exposure matrices (FEM). This paper will demonstrate the KT CDFE and FEM Analysis methods and their application in production environment.

9050-110, Session PWed

Comparative defect classifications and analysis of Lasertec's M1350 and M7360

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Defect classification and characterization on mask substrates and blanks can be used to the identify defect sources within the tool and process. Morphology and placement in the multilayer stack points to origin and timing of defect introduction. Manipulation of parts and processes can then be examined for the effectiveness of elimination or suppression of these well-classified defects. Defect reduction has been achieved in SEMATECH's EUV Mask Blank Development Center (MBDC) over the last three years, aided by successful classifications of defect populations.

Failure analysis of EUV substrate and blank defects in the MBDC begins with automatic classification of the defects detected by M1350 and M7360 Lasertec inspection tools. Since the M1350 is less sensitive at smaller defect diameters, it is often used to detect and classify the noisier multi-layer depositions where defects of interest are 100 nm in diameter or higher. The M7360 is usually confined to the study of mask substrates at pre- and post-cleaning steps.

The limits of defect detection are defined by the optics of the available detection tools. The detection system of the M7360 tool is more advanced than the M1350. Laser illumination and signal capture on quartz reach detection limits of 65 nm for the M1350 at a capture rate of 100% and 35 nm for the M7360 at a capture rate of 96.8%. On multilayer blanks, laser illumination reaches detection limits of 70 nm for the M1350 at a capture rate of 100% and 40 nm at a capture rate of 95.2% for the M7360.

Two sets of defect images and classification emerge from the two detection tools. The M1350 provides a more variegated set of 13 defect class types, while the M7360 provides eight. During manual review of the classifications, the defect class sets for both tools are often collapsed to only two major classes of interests with respect to production and failure analysis: particles and pits. This leaves various other classes ignored at subsequent characterization steps like SEM classification and composition analysis. The usefulness of tracking and verifying more detailed classes of defect needs to be explored.

SEM analysis can be used to validate the relative size comparison yielded from inspection data alone, beyond the calibrated comparison of inspection signals from well-understood polystyrene latex spheres. The accuracy of rule-based defect classification of inspection tool data must be quantified by strict statistical comparison to SEM analysis and classification. Additionally, the size distorting effects of defect composition and morphology on laser reflectance and detection can be tracked and quantified.

Finally, classification of false counts increases as sensitivity of detection tools are increased to ensure the capture of smallest defects. The validity of calling a defect "false" is usually a manual review of pixel images created on the detection tool. These falses require some verification by more sensitive SEM review.

9050-111, Session PWed

Tracking defectivity of EUVand SADP processing using bright-field inspection

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As the silicon industry develops extreme ultraviolet (EUV) lithography and advanced patterning techniques, monitoring defectivity becomes crucial to successfully shrinking feature size to the 1X node. In this study, dense line and space (L&S) pattern was printed with EUV lithography, and processed using self-aligned double patterning (SADP). This process uses a pre-existing pattern to double the number of features at half the size. In order to improve these innovative techniques, a greater understanding of which defects on the EUV mask transfer to the wafer, and how those printed defects affect the final product is required. This research utilized programmed defects to study EUV+SADP defectivity, and examined bright field inspection capabilities for the 1X node.

Programmed defects of known size, shape, and location were printed using EUV lithography at imec, and were then inspected throughout the wafer fabrication process. Pindot and extension type defects ranging from 8 to 40nm in size were systematically printed in 30, 32, 35, and 40nm L&S areas (Figure 1). The wafer was inspected after the lithography, etch, deposition, and SADP spacer open steps to accurately determine defect print and inspection capture rates throughout production (Figure 2). To maximize bright field inspection sensitivity, a recipe optimization study was conducted using polarized light, high intensity light, and customized light collection masks. Repeater analysis was used to filter out random defects, and focus only on programmed defects for review. To determine whether or not a programmed defect printed, a high resolution image of each defect location was taken using a defect review SEM after each process step.

After inspecting and reviewing the wafer throughout production, several

conclusions can be drawn from the data. On average, 68% of the defects programmed on the EUV mask actually printed, and of those an average of 88% were detected by the inspection tool (Figure 3). Most defects that appeared on the wafer after EUV lithography remained defective post-SADP. This shows the importance of inspecting wafers soon after they're printed to catch process issues early in the development flow. Overall, extension defects were more likely to print than pindots, yet were harder to detect. This is because small pindot defects did not print, while extension defects of the same size remained small extensions. These tiny extensions bear a striking similarity to line roughness, and were difficult to detect. Defects with a 1:1 X:Y aspect ratio were also less likely to be detected than defects with a 1:2 or 2:1 ratio because of their small size. In addition to these discoveries, other conclusions illustrating print and capture rates were drawn by comparing defect attributes to L&S pattern size.

By tracking programmed defects throughout wafer development, this research shows how defects on the EUV mask affect the final defectivity of the product post-SADP. This research provides a greater understanding of EUV defectivity, and also shows meaningful data on detecting defects at the 1X node using bright field inspection.

9050-112, Session PWed

Improving reticle requalification efficiency and reducing wafer print-checks via automated defect classification and simulation

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Advanced IC fabs must inspect critical reticles on a frequent basis to ensure high wafer yields. These necessary but expensive requalification inspections can now be analyzed automatically giving improved accuracy, mask utilization, and wafer yields.

Requalification inspections are expensive for many reasons including the costs of capital equipment, maintenance, and labor. In addition, critical reticles typically remain in the "requal" process for extended, non-productive periods of time. One major requal cycle time component is the disposition of defects found during automatic defect inspection. Not only is non-productive time extended by reviewing sometimes hundreds of potentially yield-limiting detections, but each additional manual review classification increases the risk of human error accidentally passing real, yield-limiting defects. The time reticles spend in an unproductive state combined with the potential for high yield loss due to the erroneous passing of a lithographically-significant (printable) defect presents significant risk to both productivity and financial losses.

An automatic defect analysis system has been implemented into a 20nm node wafer fab to automate reticle defect classification by simulating each defect's printability under the illumination conditions used for each reticle. Reliance on the application's disposition accuracy dramatically reduced reticle requalification cycle time and virtually eliminated the need for wafer print checks. In this paper, we have studied and present results showing the impact that an automated reticle defect classification system has on the reticle requalification process; specifically, defect classification speed and accuracy. Defects of interest were further analyzed with lithographic impact simulation software and compared to the results of both AIMS™ optical simulation and to actual wafer prints.

9050-113, Session PWed

Direct-scatterometry-enabled PEC model calibration with two-dimensional layouts

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Accurate and fast kernel-based proximity effect correction (PEC) models are indispensable to full-chip proximity effect simulation and correction. The attempt to utilize optical scatterometers for PEC model calibration instead of scanning electron microscopes is primarily motivated by the fact that scatterometry can be faster, more stable, and more informative if carefully implemented. Conventional scatterometry measures periodic patterns and retrieves their dimensional parameters by solving inverse problems of optical scattering with predefined libraries of periodic patterns. PEC model parameters can be subsequently calibrated with the retrieved dimensional parameters. However, measuring only periodic patterns limits the usage of scatterometry, and the dimensional reconstruction is prone to generate estimation errors for patterns with complex 3D geometry. Previously, we have proposed directly utilizing scattering light for PEC model calibration without the need for the intermediate step of retrieving the dimensional parameters. By iteratively comparing scattered light from predefined calibration patterns measured by a scatterometer to that predicted by the corresponding scattering and lithography models, PEC model parameters can be effectively calibrated with standard numerical optimization algorithms and 1D periodic patterns. In this work, 2D periodic test structures and 2D circuit layouts are designed and utilized to study the applicability and potential limitations of the proposed method on the lithography of practical circuit designs.

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9050-114, Session PWed

Implementation of background scattering variance reduction on the rapid nanoparticle scanner

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Over the past few years, TNO have developed the Rapid Nano particle scanner [1]. This scanner was developed for detection of nanoparticles on flat substrates, e.g. EUV reticle blanks. The main application of this system is in the particle qualification of reticle handling equipment. Particle maps from pre-scans and post-scans can be matched, identifying particles added by the reticle handling equipment.

The measurement principle of the scanner is imaging dark-field microscopy. In the standard illumination mode, a laser beam illuminates the substrate from a high elevation angle. A long working distance microscope images a small portion of the substrate on a CCD camera. In the absence of particles a nearly dark image is recorded. When a

particle is present some light is scattered into the microscope and a bright dot shows up in the image. A full reticle is inspected in a step-and-scan mode by combining about 10.000 such images. In the basic configuration, without the upgrade described below, the sensitivity of the scanner is 59 nm LSE (95 % capture efficiency according to SEMI M50).

Recently, we developed a model predicting the performance of the scanner as a function of the most important design parameters [2]. Using this model we found a new illumination mode that allows for detection of 27% smaller particles compared to the previous illumination mode [3]. Most of the sensitivity increase (20%) is due to an increase in the signal-to-noise by reducing the variance in the background signal.

Here we report on the successful implementation of this illumination mode on the Rapid Nano particle scanner. We demonstrate the increased particle detection sensitivity by comparing data recorded with and without background variance reduction. The typical background distributions due to surface scattering with each illumination mode are shown in Figure 1. With the new illumination mode, the variance in the background distribution is about five times lower. Therefore, the detection limit can be set a factor of 2.2 lower for the same false-positive rate and thus increase the sensitivity of the scanner to a 14% smaller particle size compared to no variance reduction. The lower detection limit for the system with the new illumination mode is calculated to be 47 nm.

Our model predicts a maximum reduction in background variance by a factor of nine, resulting in an increase in sensitivity by 20% LSE. We are currently optimizing the systems alignment and illumination uniformity to get closer to the theoretically achievable variance reduction and thereby further increasing the detection sensitivity of the particle scanner towards 43 nm.

These results demonstrate that the illumination technology works, enabling the next steps on the Rapid Nano sensitivity roadmap toward a sensitivity of 20 nm LSE.

9050-115, Session PWed

The measurement uncertainty of CD measurement in the optical measurement technology using pupil

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At the present CD measurement, we measured the minimum sampling plan using CD-SEM that consider the device influence and measurement cost. However, if device node becomes still smaller towards a 19nm generation, the spec control of CD measurements become severe, and the budget of processing accuracy will become severe. If we try to increase the number of samplings rather than the present condition using CD-SEM, TPT and an equipment price will become main issue. On the other hand, CD-SEM has unstable element since vacuum equipment such as maintenance, a running cost, and a failure rate. Therefore we need a more high speed, cheaper, more stable equipment for multi-sampling CD measurement. As CD measurement technology other than CD-SEM, there are application of the usual OCD technology, the optical measurement technology using pupil, the next-generation OCD technology using pupil, and a macro inspection apparatus, etc. In this way, the optical measurement technology using pupil can get much information by various optical conditions (incidence angle/ azimuth angle). As a result, various issues were found for measurement uncertainty of CD measurement in the optical measurement technology using pupil, so this report discusses it. The basic equipment configuration of CD measurement technology using pupil is shown in Fig.1. The optical CD measurement which is not a simulation- base cannot measure CD value directly. Therefore, it is necessary to acquire correlation with CD-SEM when we require the recipe setup. In this evaluation, the correlation with CD-SEM has been obtained (Fig. 2). As a reason which optical CD measurement cannot measure robustly, the noise (change of parameters other than CD value) has a significant impact on signal (CD value change), and it is occur that the fact signal change is deceived (it is robustly immeasurable). When the NAND process is formed by the number of the laminated films and the number of the patterns, CD measurement in the optical measurement technology is influenced by these parameters.

9050-116, Session PWed

Process control using set-membership vector-form affine projection adaptive filtering scheme

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A virtual multiple-input multiple-output (VMIMO) architecture is proposed recently, which allows cooperatively data exchange among each node in a sensor network. We consider to apply the adaptive filter to design a VMIMO receiver. In order to improve the convergence problem and reduce the complexity of the scalar-form Affine Projection (AP), the method of set-membership filtering (SMF) is applied to the Affine Projection adaptive algorithms.

Simulation results show that the SMF is able to reduce the computational complexity effectively and achieves a better performance.

9050-117, Session PWed

Phase-shift focus monitor for OAI and high-NA immersion scanners

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Phase Shift Focus Monitor (PSFM) has been successfully utilized as a focus monitoring tool from the g-line era to the most advanced immersion technology nodes. The functional concept of PSFM consists of a bar-in-bar target which has 8 isolated chrome lines. The quartz was etched on one side of the chrome line to a depth of a quarter of the wavelength. When focus changes, the position of the chrome image in the resist will shift. The shift can be measured by overlay tools as overlay misregistration errors. The recommended PSFM illumination conditions are conventional mode, high NA, low sigma, thin resist and small target line width for best sensitivity and linearity over a usable focus range. PSFM has shown high sensitivity, linearity and repeatability for immersion scanners under these conditions (NA 0.93), as shown in Fig 1, and has been widely used in the industry.

However, the performance of PSFM is not well studied when it is used under the conditions of Off-Axis Illumination (OAI) and high NA (>0.93). It has been noted that PSFM linearity deteriorates when 100 nm PSFM target, conventional mode and NA > 0.93 are used, limiting the use of PSFM for immersion tools to NA 0.93. As shown in Fig 2, the overlay misregistration of 100 nm bar-in-bar targets does not have a linear relation with defocus at NA1.35.

This paper aims to study the PSFM sensitivity and linearity under the conditions of OAI and High NA based on the simulation and wafer results. A microlithography model was created using Hyperlith with these settings: Alternating PSM (Rigorous) mask technology with proper parameters; iso-line chrome patterns with 90 degree phase-shift opening on one side and non-phase-shift on the other side of the line; line width, illumination and exposure parameters as variables; default Hyperlith values used for other parameters. Wafer exposure was done with ASML NXT immersion scanners and the overlay was measured with KLA-Tencor Archer 500 plus. The microlithography model predicts that a PSFM sensitivity of 260 nm/um (overlay shift per focus change) can be achieved with conventional mode, NA 0.93, sigma 0.372 and PSFM 40 nm target. While sensitivity as high as 700 ~ 1000 nm/um can be achieved when an OAI, 40 nm PSFM target and NA 1.35 were used. Wafer data verified the simulation results. There is a triple sensitivity improvement. On the other hand, the PSFM linear focus range, or depth of focus (DOF), of the NA 1.35 condition is less than 100 nm, which is much smaller than

that of NA 0.93 (800 nm). Although the DOF is smaller for higher NA, the linear range of 100 nm is perfectly enough for the immersion scanner focus monitoring. The influence of illumination conditions on PSFM, such as OAI modes (annular, Quadra and X-Quadra), NA / Sigma values and PSFM target sizes, has also been explored by the microlithography model.

9050-118, Session PWed

CD uniformity optimization at volume ramp up stage for new product introduction

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In this paper we describe the joint development and optimization of the critical dimension uniformity (CDU) at an advanced 300 mm ArFi semiconductor facility of SK Hynix in the high volume device.

As the ITRS CDU specification shrinks, semiconductor companies still need to maintain high yield of good wafers per day and high performance (hence market value) even during the introduction phase of a new product. This cannot be achieved without continuous improvement of the on-product CDU as one of the main drivers for yield improvement. ASML Imaging Optimizer is one of the most efficient tools to reach this goal.

This paper presents experimental results of post-etch CDU improvement by ASML Imaging optimizer for immature photolithography and etch processes on critical features of 20nm node.

We will show that CDU improvement potential and measured CDU strongly depend on CD fingerprint stability through wafers, lots and time. However, significant CDU optimization can still be achieved even for variable CD fingerprints.

In this paper we will review point-to-point correlation of CD fingerprints as one of the main indicators for CDU improvement potential. We will demonstrate the value of this indicator by comparing CD correlation between wafers used for Imaging Optimizer dose recipe development, predicted and measured CDU for wafers, and lots exposed with various delays ranging from a few days to a month.

This approach to CDU optimization helps achieve higher yield earlier in the new product introduction cycle, enables faster technology ramps, and thereby improves product time to market.

9050-120, Session PWed

Plasma-etched surface scanning inspection recipe creation based on bidirectional reflectance distribution function and polystyrene latex spheres

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The continual increasing demands upon Plasma Etching systems to self-clean and continue Plasma Etching with minimal downtime allows for the examination of SiCn, SiO2 and Sin defectivity based upon Surface Scanning Inspection Systems wafer scan results. Historically all Surface Scanning Inspection System wafer scanning recipes have been based upon Polystyrene Spheres wafer deposition for each film stack and the subsequent creation of light scattering sizing response curves.

This paper explores the feasibility of the elimination of Polystyrene Latex Sphere and/or process particle deposition on both filmed and bare Silicon wafers prior to Surface Scanning Inspection System recipe creation. The study will explore the theoretical maximal Surface Scanning Inspection System sensitivity based on PSL recipe creation in conjunction with the maximal sensitivity derived from Bidirectional Reflectance Distribution Function maximal sensitivity modeling recipe creation. The surface roughness (Root Mean Square) of plasma etched wafers varies dependent upon the process film stack. Decrease of the root mean square value of the wafer sample surface equates to higher surface scanning inspection system sensitivity.

Maximal sensitivity SSIS scan results from bare and filmed wafers inspected with recipes created based upon Polystyrene/Particle Deposition and recipes created based upon Bidirectional Reflectance Distribution Function modeling will be overlaid against each other to determine maximal sensitivity and capture rate for each type of recipe that was created with differing recipe creation modes.

A statistically valid sample of defects from each Surface Scanning Inspection system recipe creation mode and each bare wafer/filmed substrate will be reviewed post Surface Scanning Inspection System processing on a Defect Review Scanning Electron Microscope. Native defects, Polystyrene Latex Spheres will be collected from each statistically valid defect bin category/size.

The data collected from the Defect Review Scanning Electron Microscope will be utilized to determine the maximum sensitivity capture rate for each recipe creation mode. Emphasis will be placed upon the sizing accuracy of Polystyrene Latex Sphere versus Bidirectional Reflectance Distribution Function modeling results based upon automated Defect Review Scanning Electron Microscope defect sizing. An examination the scattering response for both Mie and Rayleigh will be explored in relationship to the reported sizing variance of the Surface Scanning Inspection System to make a determination of the absolute sizing accuracy of the recipes there were generated based upon Bidirectional Reflectance Distribution Function modeling.

This paper explores both the commercial and technical considerations of the elimination of Polystyrene Latex Sphere deposition as a precursor to Surface Scanning Inspection System recipe creation. Successful integration of Bidirectional Reflectance Distribution Function modeling into the technical aspect of Surface Scanning Inspection System recipe creation process has the potential to dramatically reduce the recipe creation timeline and vetting period. Integration of Bidirectional Reflectance Distribution Function modeling has the potential to greatly reduce the overhead operation costs for High Volume Manufacturing sites by eliminating the associated costs of third party Poly Styrene Latex Shere deposition.

9050-49, Session 12

Weak measurements applied to process monitoring using focused beam scatterometry

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The capacity to measure rapidly and accurately key parameters of subwavelength deep trench structures is of central importance for the monitoring of manufacture processes in the production of computer integrated circuits. Parameters of interest include, for example, trench depth, duty cycle, wall angle and oxide layer thickness. The measurement method proposed here is based on scatterometry, where the illumination consists of a focused field with a suitably tailored spatially-varying polarization distribution. This approach is related to measurement techniques such as off-null ellipsometry [1] and weak measurements [2].

Our approach is as follows: First, the amplitude and polarization distributions of the illuminating field are prepared by means of a spatial light modulator (SLM). This field is then focused through a microscope objective onto the sample. The scattered field is collected and collimated

by the same microscope objective, before passing through a uniform polarization analyzer followed by a charged-coupled device (CCD) detector. The sample to be measured is at a plane that is Fourier conjugate to both the SLM and the CCD, so that a pixel at the SLM corresponds roughly to a direction of incidence at the sample, and a direction of reflection from the sample corresponds roughly to a pixel at the CCD.

The key of the new approach is the design of the polarization distribution for the illuminating field. This design requires an accurate model for the scattering matrix of the structure in question in terms of the parameters to be measured. This model can result, for example, from the use of rigorous coupled wave theory. The paper will present approaches to the design of pupil polarizations that optimize the ability to discriminate between various process parameters and numerically test them using rigorous coupled wave simulations.

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9050-50, Session 12

Enhanced optical CD metrology by hybridization and azimuthal scatterometry

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Manufacturing yield improvement requires tight process control using high precision, accurate, non-invasive and high throughput metrology solutions. Scatterometry is successfully employed for characterization of a large number of device structures in different development environments and production modules. More recently the technology has been utilized in magnetic hard disk drive (HDD) manufacturing with rigorous pattern transfer performance demands with MEMS-like isolated read/write device features. Scatterometry requires a periodic grating structure and the measurements are done in a plane of incidence normal to the grating orientation. Recent algorithm and hardware advancements have made azimuthal scatterometry a logical manufacturing worthy reality, which utilizes a single non-zero azimuth angle or a combination of azimuth angles, in a parallel analyses scheme, to give at hand improved sensitivity to features that are otherwise difficult to fully characterize. In this work we present a comparison of conventional scatterometry and azimuthal scatterometry characterizing post develop and post RIE structures with line widths at two extreme dimensions approaching resolution limits of the technique. For example, it will be shown that using azimuthal scatterometry it is possible to accurately characterize resist line edge roughness which is conventionally determined by CD-SEM. A comparison between scatterometry and CD-SEM results and analysis techniques will be made. Increasing complexity of the structures, however, demands utilization of more comprehensive arsenal of techniques and solutions. In this work we also discuss pros and cons of a so-called hybridized azimuthal scatterometry (HAS) technique where measurement inputs from reference systems such as CD-SEM and CD-AFM are utilized to enhance accuracy and fleet measurement precision characteristics of the line edge roughness and side wall angle measurements. It will be shown that hybridization of line edge roughness using CD-SEM as a source tool can lower the CD and sidewall angle fleet measurement precision by more than 60%.

9050-51, Session 12

High-speed optical metrology solution for after etch process monitoring and control

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Monitoring and control of the various processes in the semiconductor require precise metrology of relevant features. Optical Critical Dimension metrology (OCD) is a non-destructive solution, offering the capability to measure profiles of 2D and 3D features. OCD has an intrinsic averaging over a larger area, resulting in good precision and suppression of local variation.

In this paper we demonstrate the feasibility of process monitoring and control in AEI (after etch inspection) applications, using the same angular resolved scatterometer as used for CD, overlay and focus metrology in ADI (after develop inspection) applications [1]. The sensor covers the full azimuthal-angle range and a large angle-of-incidence range in a single acquisition. The wavelength can be selected between 425nm and 700nm, to optimize for sensitivity for the parameters of interest and robustness against other process variation.

One important AEI application concerns the FinFET technology. The processes involved in FinFET fabrication require tight control of in plane dimensions, such as line and space control, as well as vertical dimensions, such as recess.

We have developed optimized recipes for the YieldStar angular resolved scatterometer, which provide robust measurement results with the required precision. The OCD metrology data, gathered at 3 measurements per second, reveal the details of the across wafer fingerprint with a good precision while the global fingerprint shows an excellent match with the reference metrology which is a good indication that the OCD metrology data is robust.

In this paper we will demonstrate the validity of the OCD data through the measurement and comparison with the reference metrology of multiple wafers and at different steps of the FinFET fabrication process in order to show that this high precision OCD tool can be used for process monitoring and control.

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9050-52, Session 12

Visualization of Si surface and interface quality by non-contact optical characterization techniques

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To gain useful insights into Si surface and interface quality in various dimensions or aspects, a variety of characterization techniques have been used in process development and process monitoring/control for manufacturing. Surface characterization techniques, such as atomic force microscopy (AFM), scanning electron microscopy (SEM), and optical interaction-based metrology focus on the physical properties of Si surfaces, such as roughness, flatness, thickness variation, particles, haze and pits. The surface and interface between the Si and deposited films were typically characterized by high resolution cross-sectional transmission electron microscopy (HRXTEM), Auger electron spectroscopy (AES), secondary ion mass spectroscopy (SIMS), X-ray photoelectron spectroscopy (XPS) and electrical measurement tools (such as I-V, C-V and carrier lifetime measurements).

As device dimensions continue to decrease and the complexity of device structures continue to increase, the proper understanding and control of Si surface and interface quality become very important. While conventional characterization techniques provide very useful information on the properties of the Si surface and interface, they cannot provide additional clues regarding surface passivation and Si interface problems which strongly affect electronic carrier behavior at or near the active device layer. Si lattice stress (i.e., Si bond length or elastic deformation of the Si lattice) at or near the Si interface, overall quality of the Si surface and interface, and plasma process induced damage (PPID) need to be carefully investigated as they can provide insights which lead to meaningful performance improvement and yields from current levels.

In this paper, Si lattice stress at or near the surface and overall quality of the Si surface and interface (including passivation characteristics) were characterized using multiwavelength, high resolution Raman spectroscopy and photoluminescence (PL) spectroscopy. To understand the depth distribution of Si lattice stress and electrically active defects/traps at or near the Si surface, a wide range of excitation wavelengths, from ultraviolet (UV) to infrared (IR), with different probing depths, were used as the probing light source. In this experiment, the characteristics of the surface and interface were anything but uniform. Significant variations in Si lattice stress, Si bond lengths and electrically active defects/traps were found at or near the Si surface and interface using multiwavelength Raman and PL spectroscopic to study the Si wafers under various process steps. Multiwavelength Raman and PL spectroscopy were able to detect and identify process defects and characteristics which cannot be detected from the conventional surface and interface characterization techniques. Visualization of variations in Si surface and interface quality within wafer and wafer-to-wafer was successfully demonstrated and potential applications of multiwavelength Raman and PL spectroscopy for inline process monitoring and control are suggested using practical examples.

9050-107, Session 12

Integrated ADI optical metrology solution for lithography process control of CD and OV

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Monitoring and control of the various processes in the semiconductor require precise metrology of relevant features. Optical metrology offers the advantages of a high speed, non-destructive solution for CD and Overlay control..

In this paper we demonstrate process monitoring in High Volume Manufacturing (HVM) of Critical Dimension (CD), using a scatterometer integrated in the litho cluster. The scatterometer has an angular resolving sensor, covering full azimuthal-angle range and a wide angle-of-incidence range. The tool combines OCD metrology capability with diffraction based overlay (DBO).

The target sampling plan is aimed at obtaining all OV and CD critical parameters on every production lot within required accurately and without impacting the litho cluster inline throughput. Next to inline OV and CD monitoring and control, the OCD profile measurement capability of the YieldStar allows to monitor the process through reporting the Side Wall Angle (SWA), resist and BARC heights, and heights of layers in the stack underneath the lithographic layers.

One of the challenges in optical CD and profile metrology, is the creation of recipes that are robust against process variations seen in HVM production conditions. The settings in the CD profile recipe are optimized to this extend using various simulation tools. The true validation is under HVM conditions, comparing the YieldStar CD over a series of wafers from different lots with a reference tool which is known to be robust against process variation, typically a CD-SEM. The data shows that the wafer to wafer variations have an excellent match, where the differences are dominated by the repeatability of the reference tool.

Compared to the original baseline of using CD-SEM for this ADI application the use of YieldStar Optical metrology integrated in the litho cluster provides a significant lower Cost of Ownership (CoO) due to a reduced litho cycle time, less metrology floor space and lower rework rate (faster reaction time to excursion).

The CD profile recipe set up, including HVM verification has been completed for 4 critical layers in different products. Next steps are the setup of the diffraction based overlay metrology and completion of the combined OV and CD control onto an integrated YieldStar T200C at the target sampling plan.

9050-119, Session 12

Novel in-line metrology methods for Fin pitch walking monitoring in 14nm node and beyond

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Integrated circuits from 22nm node and beyond utilize many innovative techniques to achieve features that are well beyond the resolution limit of 193i lithography. The introduction of complex 3D structures in device design presents additional challenges that require more sophisticated metrology with high accuracy and precision. Asymmetry introduced by multiple patterning has proven to be a challenge for in-line metrology techniques. As feature dimensions near the resolution and physical size limitation of direct measurement techniques (AFM, CD-SEM), inverse approaches based on rigorous model based methods rise as viable alternatives.

One such example of an asymmetric feature is pitch walk induced by multiple-patterning such as multiple lithography exposures and sidewall-image-transfer techniques. The effects of this non-ideality can propagate downstream introducing unwanted variability to device and circuit performance. Quantification of pitch walk has traditionally been a challenge. In this paper, we present two ways of capturing pitch walking using optical and X-ray techniques.

One approach is to use scatterometry. Modeling shows that in Mueller matrix spectroscopic ellipsometry setups, additional data at different azimuth angles has an enhanced sensitivity to pitch walking. This paper investigates the feasibility of non-orthogonal azimuth angle spectroscopic reflectometry setups for Fin pitch walk measurements, which is useful for in-line monitoring in 14nm node microelectronics manufacturing.

Another approach is using high-resolution X-ray diffraction (HRXRD). Reciprocal space mapping shows diffraction peaks corresponding to spacing of the periodic Fin structures. Pitch walking is seen as additional peaks in the map and the intensities can be used to quantify the pitch walking. In addition, additional information about the Fin profiles (e.g. sidewall angle, CD and height) can be obtained. Note that in HRXRD measurements, all the parameters are deconvoluted from the pitch walking. Furthermore, it is possible to measure the resulting epitaxial growth quality as a result of pitch walk with this technique.

The two techniques have different strengths which are complementary to each other. Scatterometry is flexible to be applied to non crystalline systems that can measure mandrel spacer right before final fin patterning, double patterned dummy gates in replacement metal gate technologies, and aggressively scaled metal trenches. However, the wavelength limits of the source and detector in commercial scatterometers makes it difficult to extract crystalline information. On the other hand, HRXRD provides information regarding the crystal structure, strain in the Fin and changes in Fin dimensions with processing.

In this paper, we will discuss the results from measurements using the two techniques and how the combination of the two techniques can give complete information about the Fins needed for in-line monitoring.

9050-53, Session 13

Sidewall roughness and line profile measurement of photoresist and finFET features by cross-section STEM image for reference metrology

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The novel method of sub-nanometer uncertainty for the line width measurement and line profile measurement using STEM (Scanning Transmission Electron Microscope) images is proposed to calibrate CD-SEM line width measurement and standardization of line profile and sidewall roughness measurement as reference metrology. In accordance with the proposed method, we already have established the methodology of profile of Si line and photoresist feature for reference metrology. In this article, we applied the proposed method to sidewall roughness estimation methodology of the photoresist feature and finFET feature. Using the proposed method, a specimen of photoresist feature and finFET feature is sliced as a thin specimen of 100 nm thickness by FIB (Focused Ion Beam) micro sampling system. Then the dark-field cross-sectional images of the specimen are obtained by STEM. Sidewall roughness is estimated by the maximum angle of image intensity graph at the edge of the feature. Then the sidewall roughness is also measured by CD-AFM, we compared the sidewall roughness measured by CD-AFM and the proposed methodology using STEM image. From series of analyses, we established the sidewall roughness estimation methodology of photoresist and finFET feature for reference metrology.

9050-54, Session 13

Verification metrology system by using inline reference metrology

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With the size shrinkage and the complicated structure of semiconductor devices, inline metrology systems such as CD-SEM and Scatterometry are also required higher accuracy. In early phase of device development and production, measurement uncertainty of typical patterns and layers have been evaluated one time by reference metrology system (RMS) and tool under test (TuT). The typical reference tools are TEM, cross-section SEM and AFM. These tools can measure a cross sectional shape and critical dimension with high accuracy, but are destruction metrology tools. Therefor these tools are difficult to apply inline non-destructive metrology. For higher accurate metrology and process control, inline reference metrology system with accurate inline metrology tools has been required in HVM phase. In this paper, we will discuss about inline reference metrology system “Verification Metrology System (VMS)” centering on high accurate metrology tools with non-destructive method.

Figure1 shows a conceptual diagram of VMS. Target wafers are measured by a reference tool with fixed sampling rate. This inline reference tool is required with high accuracy, non-destructive metrology and high throughput. After the reference metrology, the target wafers are measured by normal inline metrology tools such as CD-SEM and Scatterometry. The reference data xRef and the inline metrology data x are analyzed by VMS system. If x value is not consistent with xRef value, measurement uncertainty of the inline metrology has a possibility of accuracy decreasing. These difference between x and xRef are caused by process variation, process condition change and so on. VMS has a potential to correct the inline metrology data with the accurate reference data and optimize tool recipes and measurement conditions. In this paper, we will discuss about the verified system which is set up a GI-SAXS (Grazing Incidence small Angle X-ray scattering) as the reference tool and a CD-SEM or Scatterometry as the inline metrology tool.

9050-55, Session 13

Impact of shrinking measurement error budgets on qualification metrology sampling and cost

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Semiconductor metrologists often seek to assess the accuracy of their measurements by comparing a set of such measurements to another set of measurements on the same samples using a trusted reference tool. These assessments are typically planned using an area of applied statistics called design of experiments (DOE), which involves the controlled variation of one parameter and the observation of its effect on another parameter. Generally a process parameter is changed, with the intent of determining how well the measurement of this parameter is tracked by one tool as compared to another (reference) tool. Often, such an experiment is designed for a small number of wafers; for example, during the development and qualification of a metrology application. Once the wafers have been processed, they are measured on both the reference tool and the tool being evaluated. By this point the experimenter has decided upon the measurement sampling plan for the wafers. The results of these accuracy evaluations are statistically based, so the higher the sampling, the greater the confidence in the results. But by the time the data analysis is complete, it is often difficult or impossible to collect additional measurements on the wafers. There are many reasons for this, including unavailability of the wafers, or the knowledge that additional measurements will deteriorate the controlled conditions under which the original measurements were taken. Thus, the experimenter must decide what sampling to use before he has the results, and then hope it is sufficient.

TMU (Total Measurement Uncertainty) analysis1,2 is a statistically-based methodology that is used to determine the relative accuracy of a Tool under Test (TuT) when compared to a Reference Measurement System (RMS). It computes the total error in a correlation, then subtracts out those components of error that are not associated with the TuT, leaving just the error associated with the TuT. This error is called the TMU, and is an estimate of the “true” TMU that would be determined under an ideal set of measurement conditions, most notably an infinite sampling size. TMU is more useful than the commonly-used R2 metric because it has units, is not affected by the range of the measurement data, does not have RMS components of error embedded in it, and outputs statistically-based upper and lower confidence limits3 on the TMU. These limits are called the TMU UL (TMU Upper Limit) and TMU LL (TMU Lower Limit), and are calculated from several parameters, including the TMU of the TuT and the total number of samples measured, N. Traditional TMU analysis provides only rough guidelines for the user to know before the experiment is run what value of N is needed. Instead, N is chosen based largely on the experience of the user and the resources available. If N is too small, the confidence limits are too far apart to provide an accurate enough estimate of the “true” TMU. If N is too large, valuable resources are expended unnecessarily due to over-sampling.

This paper presents a solution, called inverse TMU analysis, to this problem by allowing an experimenter to optimize his sampling plan before the experiment has begun, using the constraints of desired uncertainty in TuT measurement quality (e.g., upper and lower limits) and available resources (e.g., cost or available tool time). To do this, we began with the equations that use the chi-squared distribution of possible “true” TMU values to determine the upper and lower limits. Those equations depend on the TMU, which depends on the knowledge of the individual (x, y) data pairs in the correlation. Because the information on the individual data pairs is only known after the measurements are collected, the equations were altered to remove this dependency. The new form of the equations (figure 1) thus allows the user to determine how many measurements (N) should be used based on quantities that can be reasonably estimated before an experiment has begun. These

quantities are the confidence level (which is a percentage measure of the likelihood that the "true" TMU will fall between the upper and lower limits, and is expressed here as (1-?)), the Reference Measurement System Uncertainty (RMSU), the (estimated) TMU, and either the TMU UL or the TMU LL (one equation is associated with the UL and a similar one is associated with the LL).

The paper will explore the relationships between these parameters for realistic semiconductor scenarios, and through these scenarios it will compare different ways for an experimenter to parameterize the problem and solution. Such parameterizations can help the user make important "risk vs. reward" sampling, cost, and equipment decisions. For example:

a) The user can start with a maximum allowable cost or sampling plan and calculate the resulting confidence interval (a measure of the span of "possible" TMU values) achievable with this plan.

b) Since some reference techniques can be used to measure the sample multiple times to obtain a more accurate reference estimate of the parameter being measured on the sample (e.g., measuring multiple lines on an OCD grating using a CDSEM), the solution can be used to perform a cost analysis that properly balances this type of sampling with the sampling associated with the total number of data pairs, N.

c) The relevance of equipment decisions will be shown through the demonstration that in most cases improved measurement quality from the TuT or the RMS allows the user to "get by" with less sampling; that is, better metrology equipment can be used to reduce sampling costs.

d) If the user defines a confidence interval in absolute terms, one can consider a ratio of this interval to the specification for the application. The user can then find it helpful to define a goal such that the sampling achieves a given, constant ratio. The paper will then demonstrate that as the measurement error budget, also known as the specification, shrinks the number of samples N that must be measured to achieve this constant ratio grows very quickly.

Due to the low cost-per-measurement of OCD and CDSEM tools, experimental data from real applications were collected on these tools, with OCD as the TuT and CDSEM as the RMS. The techniques demonstrated in the paper were applied to these applications in order to illustrate the properties seen in the inverse equations and to determine the optimal sampling for the applications, based on given constraints. The effect on reference metrology cost of shrinking measurement error budgets and the corresponding growth in required sampling will then be explored through examples using various reference tools. Because these costs can be quite alarming for large values of N, the paper will conclude with strategies on how to manage and mitigate these costs.

9050-57, Session 14

The effect of individually-induced processes on image-based overlay and diffraction-based overlay

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For advanced node of semiconductor manufacturing, accurate overlay measurement becomes more important. Therefore, improvements in measurement accuracy have been properly achieved with technological development.

However, when there is some process noise, one of the most difficult things is finding optimized overlay measurement method and recipe. The reason for the difficulty is that there are two categories in overlay measurement methods: image based overlay (IBO) and diffraction based overlay (DBO) and there exist vast number of controllable recipe parameters within each method. Therefore, the guideline of selecting proper method and recipe for specified layers and fundamental understanding of process related overlay error are needed.

Previous researches have mainly used process integrated wafers for investigation on readability at extreme overlay mark conditions, comparison of measurement uncertainty and dependency of overlay measurement result of each method.

Since several processes are included in the integrated wafers, the effects of processes toward overlay mark condition are overlapped accordingly. To suggest guideline for the integrated wafers, basic understanding about the correlation between measured overlay variation and unit process error is required. Consequently, to understand the effects of individual processes on overlay mark condition, each process effects on the mark should be separately considered.

In this paper, set of wafers with separated processes was prepared and overlay measurement result was compared in two methods; IBO and DBO. The separated processes which are used in this study are transparent and opaque hard mask formation, chemical mechanical polishing and metal deposition, which are highly suspected to cause overlay noise.

Based on the experimental result, theoretical approach of correlation between overlay mark deformation and overlay variation will be presented. Moreover, overlay reading simulation was used to verify and predict overlay variation when overlay mark was deformed by processes.

Through this study, understanding of individual process effects on overlay result and guideline of choosing overlay measurement method and recipe of process affected wafers can be given.

9050-58, Session 14

Real-cell overlay measurement through design-based metrology

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Until recent device nodes, lithography has been struggling to improve its resolution limit. Even though next generation lithography technology is now facing various difficulties, several innovative resolution enhancement technologies based on 193nm wavelength were introduced and implemented to keep the trend of device scaling. Scanner makers keep developing state-of-the-art exposure system which guarantee higher productivity and meet a more aggressive overlay specification. "The scaling reduction of the overlay error has been a simple matter of the capability of exposure tools. However, it is clear that the scanner contributions may no longer be the majority component in total overlay performance. The ability to control correctable overlay components is paramount to achieve the desired performance." In a manufacturing fab, the overlay error which is determined by a conventional overlay measurement: by using an overlay vernier based on IBO and DBO etc. often does not represent the physical placement error in the cell area of memory device. The mismatch may arise from the size or pitch difference between the overlay vernier and the cell pattern. Pattern distortion caused by etching or CMP also can be the source of the mismatch. Therefore, the requirement of a direct overlay measurement in the cell pattern gradually increases in the manufacturing field and also in the development level.

To overcome the mismatch between conventional overlay measurement and the real placement error of layer to layer in the cell area of a memory device, we suggest an alternative overlay measurement method utilizing by design based metrology tool. A basic concept of this method is shown in figure1. A CD-SEM measurement of the overlay error between layer 1 and 2 could be the ideal method but it takes too long time to extract a lot of data from wafer level. An E-beam based DBM tool provides high speed to cover the whole wafer with high repeatability. It is enabled by using the design as a reference for overlay measurement and a high speed scan system. In this paper, we have demonstrated that direct overlay measurement in the cell area can distinguish the mismatch exactly, instead of using overlay vernier. This experiment was carried out for several critical layer in DRAM and Flash memory using DBM(Design Based Metrology) tool, NGR2170™.

9050-59, Session 14

Integrated production overlay field-by-field control for leading edge technology nodes

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In the past few years, field-by-field correction (FxFc) or Correction Per Exposure (CPE) was introduced in high volume manufacturing (HVM) production as an additional, complimentary, control loop. The purpose of this addition is to compensate for the systematic overlay wafer process signature that cannot be corrected by the standard APC run-to-run (R2R) linear 10 terms or by the use of high order control correctables. The FxFc does improve the overlay performance and has become well accepted in the 2x nm HVM process nodes. However, due to the full wafer field sample plan requirement, the updates for the FxFc control loop have not been lot-by-lot based, but rather have been limited to a less frequent update based on wafer process stability.

As photolithography will continue with 193nm immersion multiple patterning technology for the leading edge HVM process node, the production overlay requirement for critical layers in logic devices has almost reached the scanner hardware performance limit. To meet the extreme overlay requirements in HVM production environment, the authors are proposing a new control concept which integrates the above two production control loops into a single integrated R2R FxFc (iR2F2) control path. To keep cost of ownership low and to maintain high correction effectiveness, the iR2F2 control has to satisfy production-worthy sampling plan requirements and still achieve good predicted correction for the unmeasured fields. In this paper, detailed implementation of this concept will be discussed, along with some preliminary results.

In addition to the above traditional two control loops R2R APC and FxFc, a scanner baseline control loop is recommended by the exposure tool vendor to correct mechanical and optical drifts for the scanner. The baseline control periodically measures non-product preventative maintenance (PM) wafers to trace and correct the machine drift. In general, this kind of baseline control does not require a specific metrology tool type or a specific type of target. Instead of using the commercially available scanner vendor solution, the authors will demonstrate an in-house baseline control system which provides optimal metrology fleet utilization and gives the user flexibility to choose his model. This baseline control loop together with the proposed iR2F2 control path can be provided as input to the fab host APC system as an integrated single control input to the exposure tool that traditionally is handled by 3 separate control paths.

In conclusion, the authors propose a new integrated overlay control concept for leading edge technology node that combines the R2R linear or high order control loop, periodic field-by-field wafer process signature control loop, and the scanner baseline control loop into a single integrated overlay control path through the fab host APC system. The goal is to meet the fab requirements for overlay performance, lower cost of ownership, and freedom of control methodology.

9050-60, Session 14

Mask contribution to intra-field wafer overlay

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Shrinking wafer overlay budgets raise the importance of careful characterization and control of the contributing components, a trend accelerated by multi-patterning immersion lithography [1]. Traditionally, the mask contribution to wafer overlay has been estimated from measurement of a relatively small number of standard targets. There are a number of studies on test masks and standard targets of the impact of mask registration on wafer overlay [2],[3]. In this paper, we show the value of a more comprehensive characterization of mask registration on a product mask, across a wide range of spatial frequencies and patterns. The mask measurements will be used to obtain an accurate model of mask contribution to wafer overlay. Furthermore, the model will be verified with overlay metrology on wafers.

[1] ITRS: International Technology Roadmap For Semiconductors Update 2012 Tables, http://www.itrs.net/Links/2012ITRS/Home2012.htm

[2] G.T. Huang et al: Mask registration impact on intrafield on-wafer overlay performance, Proc. SPIE 7971-5, 2011

[3] K. Bubke: Mask characterization for double patterning lithography, J.Micro/Nanolith. MEMS/MOEMS 8(1), 011004 (Jan-Mar 2009)

9050-104, Session 15

Innovative techniques for improving overlay accuracy by using DCM (device correlated metrology) targets as reference

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Overlay metrology challenges can be attributed to Total Measurement Uncertainty (TMU), Design rule compatibility, Device correlation & Measurement Accuracy. With process impact in overlay metrology for 2x nm node and below becoming more critical due to challenges in the management of shrinking overlay budgets, techniques to improve measurement accuracy becomes more important. In this paper, we present a methodology for improving overlay accuracy using innovative techniques.

A propriety quality metric, Qmerit, which can be used as a measure to show process impact, is employed to identify overlay metrology measurement settings with least process impacts and most reliable accuracies. This quality metric can be used in comparative analysis for a range of overlay target designs and metrology settings, thereby, identifying good candidate combinations of target designs & metrology settings that show least process impacts and best accuracies. This result is first verified with correlation study of various combinations with reference CDSEM data collected on DCM (Device Correlated Metrology) target. Furthermore, simulation of light spectrum behavior with metrology and film stack information also supports candidate selection based on quality metric application.

Using the quality metric results, an innovative calibration method ASC (Archer Self Calibration) is used to remove the inaccuracies. Using the measurement information from various target/ metrology settings, the calibration methodology estimate the inaccuracies and calibrate the overlay data to most accurate behavior. After calibration, overlay data improved in matching while correlating to a most accurate behavior. This in turn results in significant improvement in correlation to reference CDSEM data measured on DCM target for available target/metrology combinations.

Both the quality metric and calibration methodology are designed to be on-the-fly applications that do not affect measurement time, making it optimized for the production environment.

9050-122, Session 15

The pattern wiggling metrology using CD-SEM

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No Abstract Available

9050-123, Session 15

Advanced CD-SEM metrology for pattern roughness and local placement of lamellar DSA

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Directed self-assembly (DSA) applying chemical epitaxy is one of the promising lithographic solutions for next generation semiconductor device manufacturing. We have introduced Fingerprint edge roughness (FER) as an index to evaluate edge roughness of non-guided lamella finger print pattern, and have found its correlation with the LER of the lines assembled on the chemical guide pattern.

In this work, we evaluate both FER and LER on DSA wafers in Focus Exposure Matrix (FEM) wafers and Uniformity wafers in several formulation condition of PS-b-PMMA block copolymer (BCP), measuring widths, pitch and edge roughness in each process steps of LiNe flow, i.e. former Wisconsin flow, (after trimming of resist patterns, after stripping resist on chemical guide patterns, and after DSA).

As a result, we found the followings. (1) Line widths and space distances of DSA are slightly different each other depending on their relative position to the chemical guide patterns. Additionally, the right condition that all lines are in same size exists, and if is not always same condition of spaces. (2) LER and LWR (Line Width Roughness) of DSA do not depend on either width or LER of guide patterns. (3) LWR of DSA is proportional to width roughness of fingerprint pattern (FWR) locally even in uniform wafers. (4) FER is influenced not only by the BCP formulation, but also by its film thickness.

We introduced new methods for optimization of the BCP formulation and process conditions by using FER measurement and local CD valuation measurement.

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9051-1, Session 1

Directed self-assembly (DSA) of block polymers: past, present, and future *(Keynote Presentation)*

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DSA of block polymer films on lithographically-defined chemically nanopatterned surfaces is an emerging technology that is well-positioned for commercialization in nanolithography and nanomanufacturing. Generation 1 (G1) DSA at a resolution of 25 to 28 nm full pitch employs poly(styrene-block-methylmethacrylate) (PS-b-PMMA) films assembled on chemical pre-patterns derived from electron beam and 193i lithography. Typically the pattern of through-film, high aspect ratio domains induced to assemble in the block copolymer film enhances the resolution of the chemical pre-pattern by a factor of three or four. G1 DSA is currently a topic of intense research interest in the semiconductor manufacturing and data storage industry. Research objectives include demonstrations that DSA can meet manufacturing requirements related to degrees of perfection, processing latitude, and integration of the technology with existing infrastructure, and device design for use with DSA patterns. The fundamental physics and chemistry governing G1 DSA is now well established. In the first part of the presentation, scale–up from the laboratory to application relevant 300 mm wafer and hard drive formats will be discussed in the context of the underlying science, how that knowledge is being applied, and results and phenomena that are not yet completely understood. The value of combining experiment and theory, and academic and industrial partnerships will also be highlighted.

G1 DSA is facilitated by PS and PMMA having nearly equal surface energies at the temperature of assembly, but the resolution limit using PS-b-PMMA is approximately 12 nm. Fortunately, the rules of assembly for G1 materials may be applied to Generation 2 (G2) block polymer systems with minor adjustments. G2 block polymer systems have suitably large Flory-Huggins parameters to enable patterning in the 5 to 10 nm regime. In systems for which the surface energies of the blocks are not nearly equal, the DSA process may be modified by: 1) depositing a layer (a top coat) on the surface of the block copolymer film to control interfacial energies between the blocks of the polymer and the top coat, or 2) using solvent annealing. Recently we have developed a quasi-equilibrium process in which the block copolymer film is infused with just the right concentration of solvent such that system dynamics are rapid, the polymer remains in the microphase-separated state, and the solvated blocks have nearly equal surface energies but retain sufficient chemical contrast to recognize and be directed by underlying chemical pre-patterns. Finally, high x materials with similar block surface energies may be designed for DSA and thermal annealing based on A-block-(B-random-C) chain sequences. Demonstrations of DSA of 8 nm features (and below) by all three G2 approaches will be presented and compared.

9051-2, Session 1

Resist materials in the limits of nanopatterning: New physics, new chemistry, and new opportunities? *(Keynote Presentation)*

Clifford L. Henderson, Georgia Institute of Technology (United States)

Photoresist materials and the continued advancement of resist material capabilities have been key enablers for the remarkable scaling achieved in the semiconductor industry over more than the past 50 years. In fact, in recent lithography generations, one can easily argue that gains in resolution provided by photoresist technology have outpaced advancements in the exposure tools and techniques themselves. Continued advancement of resist materials and lithographic technologies into the sub-40 nm feature size regime (i.e. sub 80 nm pitch regime), which is roughly the limit for single layer resist processing using 193 nm immersion lithography, has arguably proven more difficult than in past scaling efforts. Such difficulties have been due in part to difficulties in developing mature exposure technologies capable of generating aerial images of appropriate feature sizes with appropriate wafer throughputs for high volume manufacturing. However, many things are in a state of flux as well in photoresist technology that may affect the industry's ability to provide successful patterning solutions for sub-40 nm pitch patterning. First, the physicochemical behavior of photoresist materials has been shown to dramatically change from expected bulk behavior once film thicknesses and feature sizes have decreased below roughly 100 nm. For example, the mechanical strength of organic resist materials is degraded significantly in sub-50 nm features. This new behavior offers both a challenge and potentially an opportunity in the design of future resist material processes. Second, chemical amplification in resists as we know it may be reaching the end of its glorious run of continuing to enable Moore's Law scaling over the last several decades. However, new methods for more precisely controlling such amplification through new resist mechanisms, chemistries, and processes offer some hope for the future. Third, radical alternative resist designs and patterning schemes have been proposed in recent years that can potentially enhance the capabilities of current and future lithographic exposure technologies. This talk will give an overview of the rise of important new physics in organic resists materials in the limits of nanopatterning, discuss some of the methods for potentially overcoming some of the challenges faced by current resist material and process designs, and finally highlight some of the radical new materials patterning approaches that may allow the industry to continue to push the limits of practical resolution even further into the future.

9051-3, Session 2

Process-stable EUV patternable metal oxide hardmask

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Inpria is developing directly patternable, metal oxide hardmasks for EUV lithography. Our resists have demonstrated 13nm half-pitch with ASML's NXE 3300 (Peters, SPIE 2013), and 10nm half-pitch with 0.7nm LWR at the Paul Scherrer Institute (Ekinci, SPIE 2013). We have recently made significant design changes leading to a second generation of metal oxide resists. This new platform eliminates hydration sensitivity leading to greatly improved process stability and shelf-stable storage at room temperature. These materials offer substantial flexibility in choice of developer and process tone, including standard organic developers (negative tone) and 0.26N TMAH (positive tone). Initial imaging results show 12nm half-pitch by e-beam and sub-20nm by EUV. High EUV absorbance combined with strategies for higher quantum efficiency indicate a path to the sensitivity required for commercial viability. Pattern collapse is also mitigated since an ultrathin (20 nm) imaging layer is possible, and the film itself serves as a high-selectivity inorganic etch mask. In this paper, we introduce the new platform, review its performance, and discuss process integration results.

9051-4, Session 2

A molecular inorganic approach to EUV photoresists

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The need to simultaneously improve the resolution, line-edge-roughness (LER) and sensitivity of EUV resists remains one of the most critical challenges in EUV lithography. Standard approaches based on organic polymers may be unable to meet the demands of 16- and 10-nm nodes. As a significant department from standard resist chemistry, Cornell and Inpria have demonstrated revolutionary resists based on HfO2 nanoparticles that have excellent sensitivity and resolution performance. One possible reason for the success of these resists is the high optical density of Hafnium metal.

We will present on a new series of inorganic resists using first-row transition metals and oxalate ligands. Specifically, we will describe the chemical and lithographic properties of complexes of the formula M(bpy)n(ox)m (bpy = 2,2'-bipyridine, ox = C2O42-) where M = Cr, Fe, Co. Figure 1 shows the lithographic performance of a resist prepared from [P(CH2Ph)(Ph)3][Co(ox)2(bpy)].

We chose to focus on metal-oxalate complexes because they are stable, easy to prepare1-5 and have known photochemistry that results in the reduction of the metal concomitant with the generation of CO2.6 We will present results of these complexes from the Berkeley Direct Contrast tool and imaging on the EUV interference-lithography tool at the Paul Scherrer Institute. Contrast curves show negative-tone behavior with Emax values ranging from 3 to 40 mJ/cm2 with Egel's of approximately 0 mJ/cm2. The following trends in sensitivity have been observed: 1) Co > Fe > Cr, 2) M(ox)3 > M(bpy)(ox)2 > M(bpy)2(ox) > (M(bpy)3.

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9051-5, Session 2

Novel nonchemically amplified (n-CARs) negative resists for EUVL

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According to ITRS-2011, one of the most prominent challenges for promoting EUVL are the requirements for improvements in resist performance like sensitivity, resolution, etch resistance and line edge roughness (LER) to fulfill the demands of high-volume production. The introduction of chemically amplified resists (CARs) has enabled the reduction in the half-pitch of patterned structures down to 22 nm in production. However, CARS can limit the ultimate minimum half pitch resolution due to acid diffusion problems and post exposure instability, especially for features at 16 nm and below. For this reason, recent attention has focused on the development of non-chemically amplified resists (n-CARs) for future lithography nodes.

One such approach being investigated by us is the development of polymeric non-CA negative resists for sub 16 nm technology. These are directly sensitive to radiation without utilizing the concept of chemical amplification (CARs). These resist designs are accomplished by homopolymers and copolymers that are prepared from monomers containing sulfonium groups. The latter have long been found to be sensitive to UV radiation and undergo polarity change-hydrophilic to hydrophobic in exposed regions only, acting as "negative tone" n-CARs. Thus non-chemically amplified negative tone resists based on the copolymers poly(4-(methacryloyloxy)phenyl dimethylsulfonium triflate-co-methylmethacrylate) (Poly(MAPDST-co-MMA)) with high sensitivity are presented. The resist, poly(MAPDST-co-MMA), was synthesized using AIBN initiated free radical copolymerization between MAPDST and MMA (1 : 1 monomer feed ratio). Similarly, MAPDST-homopolymer was synthesized by reacting monomer MAPDST and using AIBN as initiator. The synthesized resist materials were characterized using FT-IR, 1H NMR, DSC-TGA analysis. The molecular weight of the above copolymer (WM= 10.8?103) was calculated using GPC analysis.

We have also observed that these n-CARs are sensitive to e-beam irradiation and would therefore be useful for EUVL down to the 16 nm node and below. High resolution patterning of designed copolymer resist was carried out using 20 KeV e-beam lithography. The unexposed polymer was polar due to its ionic character and therefore soluble in polar solvents such as water. Unexposed regions of the resist film readily dissolved in an aqueous TMAH developer while the exposed regions (patterns) were maintained after dipping the exposed resist film in developer. LER of 20 nm lines patterns were calculated by SuMMIT® software and are within the permissible range. The MAPDST co-polymer exhibits a contrast of γ=1.96 with a threshold dose D0= 7µC/cm2. The homopolymer also exhibited 20 nm as well as 16 nm L/2S and L/S patterns at a dose of 35 µC/cm2. High resolution features at 13.5 nm exposures will be presented as well as fragmentation dynamics under EUV. Although, this has been termed as a "negative resist", yet its exposure and development are very similar to those of CA resists. These new negative tone resists provide a path forward for designing non-CARs that may obtain higher resolutions than current chemically amplified resists at competitive sensitivities. Therefore this polymer can meet the requirements of high throughput with no significant changes in EUV fab manufacturing.

9051-6, Session 2

Evaluation of vacancies in positive tone nonchemically and chemically-amplified EUV/EB resists: Relationship between free-volume and LER

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Extreme ultraviolet lithography (EUVL) at a 13.5 nm is one of the most promising next generation nanofabrication technologies for half-pitch 16 nm node device manufacturing and beyond. Moreover, soft-X-ray lithography using PMMA which delivered from synchrotron light source has already established with LIGA process. Electron beam (EB) lithography is currency employed nanofabrication process for specialty devices, such as MENS and NEMS.

EUV, X-ray, EB induce mainly ionization in resist materials and its energy deposition process is different from ArF exposure. Therefore the knowledgebase of radiation chemistry is required for understanding the resist performances for EUVL.

In order to acquire the knowledge of resist materials for a next generation EUVL from a viewpoint of free volume, the positron annihilation spectroscopy was carried out using positron probe microanalyzer (PPMA) installed at AIST. The lifetime and intensity of ortho-Positronium (o-Ps) in EB exposed positive tone non-chemically (non-CA, ZEP) and chemically (CA, UV-III) amplified EUV/EB resists were observed.

EB from low energy EB accelerator (Hamamatsu Photonics, EB-engine, 40 keV – 110 keV) and EB lithography system (Elionix, ELS-7700T, 75keV) were used for the exposure tool.

For non-CA and CA resist materials, it was found that changes of free volume due to polarity change and chain scission would be hardly influenced for LER.

9051-7, Session 3

Manufacturability improvements in EUV resist processing

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As the design rule of semiconductor process gets finer, extreme ultraviolet lithography (EUVL) technology is aggressively studied as a process for 22nm half pitch and beyond. At present, the studies for EUV focus on manufacturability. It requires fine resolution, uniform, smooth patterns and low defectivity, not only after lithography but also after the etch process.

In the first half of 2013, a CLEAN TRACKTM LITHIUS ProTMZ-EUV was installed at imec for POR development in preparation of the ASML NXE-3300. This next generation coating/developing system is equipped with state of the art defect reduction technology. This tool with advanced functions can achieve low defect levels. Apart from defectivity, we evaluated CD uniformity and line width roughness (LWR) through the etch process, including pattern smoothing optimizations.

This paper reports on the progress towards manufacturing defectivity levels and latest optimizations towards the NXE-3300 POR for both lines/spaces and contact holes at imec.

9051-8, Session 4

Investigation of interactions between metrology and lithography with a CD SEM simulator

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The predictive power of computational lithography is often demonstrated by showing predicted 2D pattern shapes compared with top-down SEM images. However, image formation in a SEM is a complex process [1-3], and for most 3D lithography and OPC simulators, line width measurements and 2D pattern shapes are based on extracted resist polygons at a fixed height above the substrate. Generating resist polygon shapes with this method is driven by computationally efficiency instead of an attempt to describe the image formation process in an actual SEM. We present PROLITH photolithography simulations combined with simulation of the CD SEM to investigate the interactions between lithography and metrology. Our CD SEM simulator is a simplification of the complicated image formation process [4], but it captures many effects seen experimentally. For example, narrow trenches and contact holes are dark at the bottom in our simulated SEM images, while for isolated lines, the sidewall of the photoresist can clearly be observed all the way to the resist foot at the substrate. This simple result has important implications when evaluating lithographic phenomena such as LWR: for polygon-based metrology, simulated LWR is approximately constant with resist thickness; by contrast, the LWR increases with decreasing thickness when the same simulated 3D resist profiles are evaluated with the CD SEM simulator. We also examine contact hole CDU [5]and shifts in focus-exposure process window shape due to interactions between metrology and lithography [4].

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9051-9, Session 5

Assessing CD-SEM contour-based OPC models quality using rigorous simulation

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For aggressive design rules, the patterning is so complex that the process margins for manufacturing tend to be very limited. In particular, state of the art lithography always requires improved OPC models, not only to achieve a better pattern fidelity but also to predict with a higher accuracy of any hotspot in the design. The traditional approach to build an OPC model with high quality relies on the accumulation of thousands of CDSEM measurements acquired for various process window conditions. However this method has reached its limits in term of cycle time for data collection. Moreover regular CD measurement are extremely challenging when considering bi-dimensional features like the majority of the hot spots flagged during OPC review.

In this paper we propose to use contours extracted from CDSEM images acquired after lithography to quickly calibrate the OPC models and stress the dramatic reduction of metrology work load. Thanks to the hundreds of CD measurement potentially contained in a single CDSEM image 1,2. The versatility of CDSEM contour give the opportunity to build simultaneously two OPC models: the first based on resist bottom contours and the second based on resist top contours. Then the quality of these two models is assessed using rigorous S-Litho simulations3 as reference.

Two OPC models using CDSEM contours were calibrated with only 12 different features across 11 process window conditions. A 28nm node metal layer was chosen because of its very limited process window and its propensity to generate a lot of critical defects. The accuracy of the models and their capability to predict the patterning failures have been evaluated with respect to rigorous 3D simulations run on specific hot spots.

The comparison with S-Litho (see Fig.1.) has clearly demonstrated that the model based on the resist bottom model is very well matched with the rigorous simulation, qualifying the use of CD-SEM contours to build OPC models. On the other hand the model based on resist top is not always following the rigorous simulation. The discrepancy is mostly driven by variation of resist thickness on specific hot spot sensitive to resist top loss which is not compatible with the assumption of a simulated contour located in a single plane in resist. Notwithstanding this limitation, the combination of both models has been investigated as an additional tool to better characterize hot spots considering their 3D nature.

9051-10, Session 5

Simulation-aided exclusion of underlayer visible pattern for sub-10nm SEM metrology and inspection

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No Abstract Available

9051-11, Session 6

Further investigations of bottom-up/top-down lithography using vertically assembled block brush polymers

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Films composed of vertically-assembled block brush polymers of highly uniform composition and chain length offer opportunities to demonstrate a novel deterministic bottom up / top down approach to sub-30 nm photolithography. The polymer architecture consists of a rigid backbone of polymerized norbornene, each linked to flexible short side brush chains. The resultant 'bottle brush' topology has a cylindrical shape with short brush chains arranged concentrically around the backbone, in which the cylinder radius is determined by the number of monomers within the brush fragment, while the cylinder length is determined by the degree of backbone polymerization. The modularity of the synthetic system allows a wide diversity of lithographically-useful monomers, sequencing, dimension, and property variation. Placement of brush chains of different compositions along different regions of the cylinder, along with variation of the relative concentric and lengthwise dimensions, provides mechanisms to align and control placement of the cylinders. These polymers are compatible with photoacid generators (PAGs) and crosslinker functionality. Vertical assembly (bottom up) of the cylinders yields a 'forest' of cylindrical block brush polymers, with the film thickness determined by the lengths of the cylinders and the number of layers, and the minimum pixel size determined by the cylinder diameter.

In this update, we will discuss the relationship between film thickness and film morphology using negative tone materials. At film thicknesses commensurate with an integer number of rod contour lengths, vertical alignment is improved and fine lithography is possible. At incommensurate film thicknesses, tilted or unaligned rods within the film diminish lithographic fidelity. Additionally, at higher thicknesses, vertical orientation requires consideration of head-tail and head-head interactions.

We will also discuss design of bottle brush materials for positive tone lithography. We have encountered several challenges in this pursuit including achieving vertical orientation, substrate adhesion, control of photoacid diffusion length, and sufficient structural integrity to survive development and rinse processes. Synthetic routes to addressing these issues will be described, along with recent encouraging results.

9051-12, Session 6

Chiral nanomaterial fabrication by means of on-edge lithography

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Already centuries ago people obtained benefit from plasmonical effects where they impressively handcrafted stunning motley church windows and brilliant luminous jewelry and cups. Nowadays the physical mechanisms of plasmonic optical effects induced by strong interactions between impinging light and tiny metallic nanoparticles seem to be well understood. Based on theoretical insight and strong knowledge about nano-patterning and nano-lithography techniques, researchers are able to tailor metallic nanoparticles shape, size and composite not only to achieve optical effects, but also to control light propagation within media.

Chiral shaped nanostructures offer great potential regarding chiroptical effects e.g. circular dichroism, polarization rotation and asymmetric transmission. These kinds of structures cannot be superimposed on their mirror image, defining chirality as a purely geometrical property. First, planar chiral structures were investigated, where theory predicts rather weak chiroptical effects, a result stemming from the substrate only [1]. Later, various three-dimensional chiral shaped designs were proposed and successfully realized, either based on lithography e.g. helices [2], twisted pattern [3] or more complex pattern [4] or based on self-assembly e.g. chiral shaped clusters [5] or by template assisted self-assembly [6]. On the one hand deterministic, highly resolved, three-dimensional chiral shapes are desired. On the other hand fast, efficient and on large scale processing is favored.

Therefore we developed an access to deterministic chiral nanostructures even on larger scale, an approach we named on-edge lithography [7]. Here variable shaped electron beam lithography (VSEBL) is processed on an e-beam resist spin-coated, pre-structured template. In connection with shadow evaporation the 2D written pattern are projected onto the uneven surface subsequently unfolding into 3D pattern. Thus the problem of defining three-dimensional shaped pattern is assigned towards a convenient designed template profile.

We demonstrate process performance of on-edge lithography by creating an array of 3D shaped pattern (Fig. 1) and present a comparison of the measured optical properties with data obtained by simulations. In addition, we figure out prerequisites to transfer the process for other nanostructure designs. We further refine the technique by switching from VSEBL to character projection [8] and thus we address curved and rounded pattern and minimized writing time at once (Fig. 2). Finally we will outline one of the big advantages which on-edge lithography holds: fullest compatibility with nano-imprint lithography. In conclusion, on-edge lithography paths the way for deterministic, three-dimensional and highly resolved nanostructures, while simultaneously lowest writing efforts and an efficient processing is attained.

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9051-13, Session 6

Positive tone cross-linked resists based on photoacid inhibition of cross linking

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Conventional chemically amplified resist (CAR) designs are unable to obtain the combination of resolution, line edge roughness, and sensitivity required for future patterning nodes. Likewise, pattern collapse is an ever increasing concern due to the high capillary forces at small feature spacing and the decreased modulus of the small features due to their high surface-to-volume ratio. There is a need for the investigation of non-conventional resist designs that can overcome many of these problems. A positive tone cross-linked resist would be favorable because it should show greatly improved pattern collapse performance due to the higher modulus of the cross-linked system compared to the linear polymers of conventional CARs which are not covalently connected to one another. This approach also provides the opportunity to compare the effect of development in a variety of different solvents beyond standard aqueous developer. The patterning scheme in this design approach has generally been based on the idea of a thermally driven cross-linking before exposure followed by an acid catalyzed depolymerization/bond-cleavage during the post-exposure bake to change the solubility by reducing the molecular weight. In comparison, we have developed a novel imaging design approach that works by photoacid inhibition of cross-linking during the post-exposure bake step. The key to this design approach is the addition of a second catalyst that catalyzes the cross-linking of epoxides and phenol groups in the absence of photoacid. When photoacid is present, the catalyst consumes epoxides, terminating before significant cross-linking can occur. Photoacid has no effect on the cross-linked network if cross-linking occurs before exposure. This design approach is also intriguing because in the absence of the second catalyst (or at low loadings), the photoacid can catalyze the epoxide-phenol cross-linking. This approach is unique because through manipulation of the second catalyst loading, the resist tone can be reversed from negative tone (low second catalyst, higher photoacid) to positive tone (high second catalyst, low photoacid), with the possibility of dual tone imaging at certain formulation conditions. Figure 1 shows coarse contrast curves illustrating the change in resist tone with the change in second catalyst loading. Figure 2 shows a more complete positive tone contrast curve for a different formulation of the first generation material. EUV patterning of initial designs is currently underway and will be discussed. The effect of functional group ratios and catalyst loading will also be discussed.

9051-14, Session 6

In-situ FTIR spectroscopy to study surface chemistry of SIS lithography

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Sequential infiltration synthesis (SIS), related to atomic layer deposition (ALD), involves gas phase molecular assembly reactions and has been recently demonstrated to increase the etch resistance of lithography resists. SIS precursors such as trimethylaluminum (TMA) and water (the same precursors used for Al2O3 ALD) react directly with the patterned resist layer within an ALD chamber operating in semi-static mode. The enhanced etch resistance eliminates the need for an additional hard mask during etching yet preserves the line-edge roughness (LER) of the lithographically defined pattern. Sub-20 nm dense lines etched into silicon with greater than 6:1 aspect ratio is reported using Al2O3 SIS-modified PMMA. It is essential to understand the behavior of the complex processes involved in SIS to achieve a high degree of perfection in large-scale lithography. In-situ Fourier transform infrared (FTIR) spectroscopic measurements during SIS treatment on PMMA thin films were performed to understand the reaction dynamics.

In this study, PMMA films of different thicknesses were used as model resist layers, and TMA and water were used as SIS precursors. FTIR spectra acquired after each precursor exposure provided a detailed description of the SIS surface reactions. FTIR spectra recorded after the TMA exposures revealed that TMA interacts with the carbonyl and ester groups causing a decrease of intensity in the carbonyl peak at 1729 cm-1 and ester peak at 1260 cm-1, and an increase in the C-H stretching from the Al-CH3 group of TMA at 2923 cm-1. Surprisingly, a majority of the TMA adsorbs reversibly to the PMMA surface as evidenced by a partial reversal in these spectroscopic changes versus time. Subsequent water exposure removes the Al-CH3 feature and produces an increase in the Al-O mode ~800 cm-1 due to Al2O3 formation. A red shifted carbonyl peak at 1672 cm-1 also appears after TMA exposure, which is removed after water exposure. FTIR spectra were recorded over several TMA/water cycles until there is no change observed in the spectra, suggesting a densification of the PMMA film such that infiltration of the gaseous TMA and H2O was blocked. It was found that the number of SIS cycles for completing the reactions increased with the PMMA thickness and the residual functional groups present in PMMA after the previous TMA exposure. In conclusion, in situ FTIR measurement provides a powerful tool for understanding the underlying surface chemistry for SIS. These results have important implications for the implementation of SIS lithography in semiconductor manufacturing.

9051-15, Session 6

Nanopatterning with tailored molecules

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We present our work of innovative materials design for nano-patterning. We are currently working on different material classes of chemical amplified resists based on polymeric and molecular glass systems, but also on molecular glasses for tip-based nano-patterning.

Here we demonstrate our progress on star block copolymers for their application as high performance resist materials. This polymer architecture offers besides their controlled spherical shape also defined monomer incorporation and positioning due to the shell-like structure. The tailored star block copolymers were synthesized utilizing the core-first ATRP route by full conversion of a first monomer and in-situ polymerization of additionally added monomer resulting in narrow polydispersity indices (PDIs < 1.2). The new star block copolymers demonstrated their excellent solubility contrast in the exposed state and their up to eight times increased sensitivity in comparison to the reference linear polymer. The most sensitive star block copolymer was investigated in a ternary combinatorial library – exposure dose and feature size, PEB temperature, and development time – for its lithographic performance. In the optimized sector, well-defined 1:1 line/space patterns down to 66 nm with LER values of about 6 nm were achieved utilizing a 20 kV electron-beam tool. As future high resolution resists for even smaller feature widths will be limited by molecular size,

further investigations concerning star block copolymers with reduced molecular weight and reduced monomer block composition will provide opportunities for further improvement of patterning performance. In summary we have successfully demonstrated that tailoring the molecular architecture towards a star block copolymer provides a significant improvement in realizing a new generation of high-sensitivity and high performance resist materials.

9051-16, Session 6

Line width roughness reduction by rational design of photoacid generator for sub-millisecond laser post-exposure bake

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Laser spike annealing was recently introduced to photolithography for the post-exposure bake step in order to address the line width roughness issue. Its premise is that by annealing at high temperature for a short time, laser heating is able to induce deprotection and control excessive diffusion. However, the deprotection and diffusion kinetics of the laser post-exposure bake process are very different from conventional minute timescale hotplate PEB. Therefore, the materials including the photoresist and the photoacid generator need to be optimised in order to take advantage of the sub-millisecond annealing process. In previous studies, we compared three different photoresists and found that one resist with a relatively high deprotection activation energy and relatively low diffusion activation energy helped to reduce line width roughness when using the laser PEB method.

In this study, we extend the research from the photoresist to the photoacid generator. A large molecule core multisite PAG (3P3A) was compared to a conventional DUV ionic PAG triphenylsulfonium nonaflate (TPS-NF), which contains the same cation as 3P3A. The quantum yields are similar for both PAGs, though 3P3A requires a much high dose for deprotection due to its low diffusivity. Despite the dose difference, the resist with 3P3A shows a 50% improvement in LWR by replacing hotplate with laser PEB. In particular, the LWR of the resist with 3P3A is only 1/3 of the same resist with TPS-NF. The investigations on activation energy of deprotection and diffusion reveal that high deprotection activation energy and low diffusion activation energy are two important conditions for materials design for a laser PEB process. The correlation of the resist and PAG performance under laser PEB and activation energy provides valuable clues for future materials design for both hotplate and laser PEB.

9051-17, Session 7

Process optimization of templated DSA flows

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Directed Self-Assembly (DSA) of Block Co-Polymers (BCP) has become an intense field of study as a potential patterning solution for future generation devices. The most critical challenges that need to be understood and controlled include pattern placement accuracy, achieving low defectivity in DSA patterns and how to make chip designs DSA-friendly. The DSA program at imec includes efforts on these three major topics. Specifically, in this paper the progress in DSA defectivity within the imec program will be discussed.

In previous work defectivity levels of ~560 defects/cm2 were reported and the root causes for these defects were identified. Various causes including particle sources, material interactions and pre-pattern imperfections were revealed. The specific efforts that have been undertaken to reduce defectivity in the line/space chemo-epitaxy DSA flow that is used for the imec defectivity studies will be discussed. In parallel, efforts have been ongoing to enhance the defect inspection capabilities and allow a high capture rate of the small defects. Further requirements for achieving manufacturable defect levels will be determined from this study.

9051-18, Session 7

An insitu hard mask block copolymer approach for the fabrication of ordered, large scale, horizontally aligned, Si nanowire arrays on Si substrate

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The computer processor industry is facing a number of challenges in defining 1D (nanowire) nanostructures at substrate surfaces. These challenges are related to lithographic and etch limitations and, in particular, the need to use double or triple patterning to create 1D features for use in logic or interconnect circuitry. Advances in extreme UV lithography have been slow and costs are spiralling. Directed self-assembly (DSA) where arrays of nanowires can be created by a combination of spontaneous arrangement of materials and 'directing' forces which force the patterns into alignment with a surface feature/direction. The most promising technique appears to be the DSA of block copolymers (BCPs) which have been shown an extremely versatile platform to form highly regular nanostructure arrangements and also can be used as templates to achieve secondary patterns of interest. But, Si nanopatterns formed by block copolymer templating suffer from edge anisotropy, roughness and dimensional variability. In contrary, hard masks offer the ability to create high aspect ratio features by subtractive processing. We report a simple technique to fabricate horizontal, uniform Si nanowire arrays with controlled orientation and density at spatially well defined locations on substrate based on insitu hard mask pattern formation approach by microphase separated polystyrene-b-poly(ethylene oxide) (PS-b-PEO) BCP thin films. The methodology may be applicable to large scale production. Ordered microphase separated patterns of the BCP were defined by solvent annealing and the orientation was controlled by film thickness and annealing time. Films of PEO cylinders with parallel orientation (to the surface plane) were applied to create 'frames' for the generation of inorganic oxide nanowire arrays. These PEO cylinders were subject to selective metal ion inclusion and subsequent processing was used to create iron oxide nanowire arrays. The oxide nanowires were isolated, of uniform diameter and their structure a mimic of the original BCP nanopatterns. The phase purity, crystallinity and thermal stability of the nanowires coupled to the ease of large scale production may make them useful in technological applications. We also demonstrate that the oxide nanowire arrays could be used as a resist mask to fabricate densely packed, identical ordered, good fidelity horizontal silicon nanowire arrays on the substrate. The techniques may have significant application in the manufacture of transistor circuitry.

9051-19, Session 7

Investigation of cross-linking poly(methyl methacrylate) as a guiding material in block copolymer directed self-assembly

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Directed self-assembly (DSA) of block copolymers (BCP) is attracting a growing amount of interest as a technique to expand traditional lithography beyond its current limits. It has recently been demonstrated that chemoepitaxy can be used to successfully direct BCP assembly to

form large arrays of high-density features; a schematic of the process is shown in Fig. 1 below. This process uses lithography and trim-etch to produce a "prepattern" of cross-linked polystyrene (PS) stripes, which in turn guide the formation of assembled BCP structures. The entire process is predicated on the preferential interaction of the respective BCP domains with particular regions of the underlying prepattern.

The use of polystyrene as the guiding material is not required, however, and in fact may not even be preferable. This study investigates an alternate chemistry – crosslinked poly(methyl methacrylate) or PMMA – as the underlying polymer mat. In contrast with PS, which is difficult to trim-etch evenly, PMMA can be easily etched to create more sharply defined regions of contrasting interfacial energy. Furthermore, PMMA itself is a more polar molecule than PS and therefore has a stronger auto-affinity, a property which enables PMMA stripes to have a stronger guiding ability. In addition to the advantages of the chemistry under investigation, this study will also explore the broader theme of extending BCP DSA to other materials by identifying new challenges and their solutions.

9051-20, Session 7

Novel surface treatment materials for aligning block-copolymer in directed self-assembly processes

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Directed Self-Assembly (DSA) process is one of the attractive processes for creating the very fine pitch pattern. Especially, the contact hole shrink processes with block-co-polymer (BCP) or polymer blend materials were attractive processes for creating very small size hole patterns with better CD uniformity compare to general photo-lithography patterning. In general contact hole shrink process, the pattern of Spin-on Carbon Hardmask (SOC) or the photo Resist pattern created by Negative-Tone Development (NTD) process were selected for guide patterns. Since the alignment property of BCP was affected by the surface of these guide materials, it is important to control the surface condition of guide in order to obtain good shrunk contact hole patterns.

In this study, we will report the surface treatment materials to control the surface condition of guide patterns such as SOC or NTD resist to achieve the better contact hole shrink performance. These materials were attached to guide pattern surface and controlled the surface energy.

9051-21, Session 7

Directed self-assembly process integration: Fin patterning approaches and challenges

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Resolution requirements for photolithography have reached beyond the wavelength of light. Consequently, it is becoming increasingly complicated and expensive to further minimize feature dimensions as required to push the limits of Moore's law. EUV lithography has been the much anticipated solution; however, its insertion timing for High Volume Manufacturing is still an uncertainty due to source power and EUV mask infrastructure limitations.

Directed Self Assembly (DSA) processes offer the promise of providing alternative ways to extend optical lithography cost-effectively for sub-10nm nodes. As a result, DSA has gained increased momentum in the recent years, as a means for extending optical lithography past its current limits. The availability of a DSA processing line can enable to further push the limits of 193nm immersion lithography and overcome some of the critical concerns for EUV lithography.

Although the progress in the field of DSA has been rapid, DSA integration to CMOS process flows is yet to be demonstrated which will confirm and reinforce its viability as a candidate for sub-10nm technology nodes.

In this contribution, we will present fin patterning approaches and challenges for sub-10 nm CMOS technology nodes.

9051-22, Session 8

High-volume manufacturing equipment and processing for directed self-assembly applications *(Invited Paper)*

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Directed Self-Assembly (DSA) is one of the most promising technologies for scaling feature sizes to 16 nm and below. Both line-space and hole patterns can be created with various block-copolymer morphologies, and these materials allow for molecular-level control of the feature shapes—exactly the characteristics that are required for creating high fidelity lithographic patterns. Over the past five years, the industry has been addressing the technical challenges of maturing this technology by addressing concerns such as pattern defectivity, materials specifications, design layout, and tool requirements 1-5. Though the learning curve has been steep, DSA has made significant progress toward implementation in high-volume manufacturing.

Tokyo Electron has been focused on the best methods of achieving high-fidelity patterns using DSA processing. Unlike other technologies where optics and photons drive the formation of patterns, DSA relies on surface interactions and polymer thermodynamics to determine the final pattern shapes. These phenomena, in turn, are controlled by the processing that occurs on clean-tracks, etchers, and cleaning systems, and so a host of new technology has been developed to facilitate DSA. In this paper we will discuss the processes and hardware that are emerging as critical enablers for DSA implementation, and we will also demonstrate the kinds of high fidelity patterns typical of mainstream DSA integrations.

9051-23, Session 10

An in-situ analysis of resist dissolution in alkali-based and organic solvent-based developers using high-speed atomic force microscopy

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With extreme ultraviolet (EUV) resist lithography targets for resolution, line width roughness (LWR), and sensitivity pushing towards fine patterning of 11 nm half-pitch (hp) lines and spaces (L/S) and beyond, a rethinking of

present resist formulations and related processes is necessary.

In the past few years, an alternative process that has been gaining interest is negative tone development (NTD) using organic solvents. With this technique, encouraging results in terms of LWR and ultimate resolution have been reported [1]. To further advance the development of this promising technology, related resist material / process enhancements will be necessary. To do this, a number of fundamental investigations on both materials and processes are being taken. Pattern formation during resist dissolution in organic solvent is one such topic being pursued.

The authors have proposed an approach using an in-liquid high-speed atomic force microscope (HS-AFM) for the in situ analysis of the resist dissolution behavior of actual resist patterns. This allows a visual appreciation of the pattern formation, as it occurs during development. Recent improvements in this technique have successfully resulted in the ability to measure hp L/S patterns [2]. Further system enhancements (tool/methodology) have also enabled the analysis of NTD resists in organic solvent.

This work focuses on the in situ characterization of pattern formation during resist dissolution with NTD method, using the HS-AFM. Resist patterns were exposed using the 0.3NA EUV small field exposure tool (SFET). NTD was done using the butyl acetate organic solvent developer. This was compared to results with a positive tone development (PTD) using the conventional aqueous alkali-based developer; 2.38wt% tetramethyl ammonium hydroxide (TMAH). For this comparative investigation, the same resist material / process conditions (post application bake / post exposure bake) was used at a film thickness of 50 nm. This is the NTD-based EIDEC standard resist 3 (ESR3), a resist which was confirmed to have the capability to resolve patterns not only in organic solvent developer, but also in alkali developer.

Figure 1 shows the (a) preliminary in situ dissolution analysis results (top view image) for the 35nm L/S pattern EUV-exposed on the ESR3 and processed at both NTD and PTD processes, in comparison to the (b) top down images obtained through scanning electron microscope (SEM). No significant swelling during dissolution was observed for both development methods. However, it is visually obvious that the ESR3 exhibits grain-like dissolution when it is developed in organic solvent.

During the conference, a detailed analysis of pattern formation characteristics of the ESR3 at both NTD and PTD methods will be discussed. The effect of these dissolution characteristics in the resist's lithographic performance will also be presented.

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9051-24, Session 10

In-situ analysis of defect formation in coat develop track process

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Typical defects to resolve during coat develop track process have been confirmed during each resist generation; i-line, KrF, ArF, ArF immersion and recently EUV. In this study, two types of defect formation could be analyzed: Organic film post coating non-uniformity spots and water-mark defects post develop. When these typical defects were generated a characteristic phenomena is always observed using high-speed video camera while rotating substrate. Post coating spot defects were linked to bubble formation while post developing defect was linked to the wafer drying condition.

Utilizing high-speed camera we can reveal mechanism of defect generation for several typical phenomena confirmed with several different resists and correlate these to defect inspection results.

9051-25, Session 10

Methods of controlling cross-linking in negative-tone resists

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Pattern collapse is an ever increasing concern as photoresist resolution is continually pushed smaller due to both the increase in the capillary forces experienced by the resist walls in the smaller features and the decrease in the modulus of the resist away from the bulk as the very small dimensions lead to high surface-to-volume ratios. Negative tone resists based on cross-linking of molecular resists is a promising method to improve this issue because the cross-linked structure has much higher bulk modulus and potentially improved small feature modulus due to reduced surface effects compared to conventional positive tone resists. We have previously shown that these types of negative tone resists based on cationic polymerization/cross-linking have the capability for high resolution patterning with good LER and sensitivity. However, their ultimate resolution can be limited due to propagation of polymerization outside the nominally exposed region. Conventional methods of controlling diffusion of active photoacids such as addition of base quenchers are generally ineffective in cationic polymerization types of negative tone resists because the photoacid is not the primary "active species". The photo-generated acid exists as a small molecule acid only long enough to protonate an epoxide which initiates polymerization via a living cationic or oxonium site. Neutralization of the photoacid with a base is also statistically unfavorable since the epoxide or other cationic polymerizable groups are generally at an order of magnitude higher concentration than a catalytic amount of base or acid. Therefore, the polymerization itself must be controlled in order to improve resolution in these systems. We have developed multiple novel approaches to control the polymerization in these negative tone systems ranging from simple additives to structural modifications of the cross-linking molecules. One successful approach is based on addition of a second photo-sensitive compound other than the primary photoacid generator. The additional photo-sensitive compound acts to significantly slow cross-linking in the unexposed regions but has a minimal effect as it becomes exposed. This not only improves resolution, but acts to improve contrast as well. Figure 1 shows DUV (248 nm) contrast curves illustrating the effect of this compound. Figure 2 shows the immediate improvement in EUV performance for a 4-functional epoxide functionalized molecular resist. The resolution obtained when no control agent was used was 32 nm with LER (3?) of 4.9 nm. When 2.5 wt% of the additive is used with no other changes, the resolution is immediately improved to 25 nm with an LER (3?) improvement to 4.0 nm. A more recent additive that has been developed that acts to strongly terminate cross-linking and should be even more general in its applications to these types of systems. EUV patterning of negative resists with this additive is currently underway. These specific agents for cationic polymerization resists will be further discussed along with additional approaches for controlling radical polymerization resists.

9051-26, Session 10

How to design a good photoresist solvent package using solubility parameters and high-throughput research

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Understanding fundamental properties of photoresists and how interactions between photoresist components affect performance targets are crucial to the continued success of photoresists. More specifically, borderline polymer solubility behavior is a cause of defects in photoresists that needs to be addressed. While several theories describe polymer solvent solubility, the most common industrially applied method

is Hansen's solubility parameters. Hansen's method, based on regular solution theory, describes a solute's ability to dissolve in a solvent or solvent blend using four physical properties determined experimentally through regression of solubility data in many known solvents. The four physical parameters are dispersion, polarity, hydrogen bonding, and radius of interaction. Using these parameters a relative cohesive energy difference (RED), which describes a polymer's likelihood to dissolve in a given solvent blend, may be calculated. Leveraging a high throughput workflow to prepare and analyze the thousands of samples necessary to calculate the Hansen's solubility parameters from many different methacrylate-based tetra/pentapolymers, we compare the physical descriptors to reveal a large range of polarities and hydrogen bonding. Further, we find that Hansen's model correctly predicts the soluble/insoluble state of 3-component solvent blends where the dispersion, polar, hydrogen-bonding, and radius of interaction values were determined through regression of experimental values. Further, in order to more accurately simulate the process conditions that these polymer/solvent blend would be exposed to during processing, i.e., spin coating, the solvent evaporation profile was modeled using UNIFAC activity coefficients to account for changes in the relative evaporation rates of individual solvents due to the presence of the mixture. These modeling capabilities have allow for optimization of the photoresist solubility from initial blending through application providing valuable insights into the nature of photoresist.

9051-27, Session 10

Ionic contrast enhancement for organic solvent negative-tone develop

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The use of organic solvents in the development of chemically amplified (CA) resists has been known since the introduction of DUV into manufacturing over 20 years ago [1]. In this approach an aqueous base developable positive tone resist is employed to produce a negative tone image by developing in an organic solvent. Recently there has been an increased interest in negative tone imaging due to superior performance for specific masking levels such as narrow trenches and contact holes [2].

Negative tone imaging of this type is based on differences in the polarity between the exposed and unexposed regions of the resist film. The dissolution contrast can be optimized by selecting a solvent with the proper match of solubility parameters (polarity, hydrogen bonding and dispersion) for good solubility of the relatively non polar unexposed resist and poor solubility of the deprotected acidic exposed film. Another approach is to tune the properties of the resist polymer for a given solvent and create a new resist. We have explored a third methodology to achieve a high contrast solvent developable system without a need to modify resist or solvent. In this report we describe a process to attempt to employ the differences in solubility between ionic and organic materials. The method involves introduction of ionic species into the resist film to change the polarity in such way that the resist contrast can be improved for an organic solvent development. We will describe processes using salt containing pre-rinses and developers. Lithographic response will be presented for a variety of resist platforms using contrast curves and imaging. We will further show the ionic incorporation into the resist film using SIMS, XPS, QCM and FTIR characterization. We will show applicability to 248nm, 193nm, e-beam and EUV exposures.

9051-28, Session 10

Introduction of an innovative solvent-free photoresist stripping process using intelligent fluids

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The usage of phase fluid based stripping agents to remove photoresists from silicon substrates was studied. Although the use of resists is very common, their successful integration often depends on the ability to remove the resist after certain processing steps. On the one hand the resist chemistry is changing during subsequent process steps that can cause a thermally activated cross-linking which increases the stripping complexity. Resist removal is also challenging after the formation of a hard polymer surface layer during plasma or implant processes which is called skin or crust. On the other hand the choice of stripping chemistry is often limited due to the presence of functional materials such as metals which can be damaged by aggressive stripping chemistries.

An alternative phase fluid based stripping chemistry known as lisoPUR© was investigated regarding its cleaning efficiency as well as contamination behavior to enable usage in semiconductor manufacturing. Phase fluids are liquid-liquid-based complex fluids based on micro emulsions and could be called enhanced micro emulsion. While classical emulsions contain dispersed spherical oil or water droplets, phase fluids are built up from dynamic and flexible plasmicells. The globular shapes of the fluid interact with each other and tend to change their forms within some milliseconds. Therefore phase fluids offer a new and innovative working principle: they are penetrating layers through smallest openings and lift off the material from the surface [fig. 1]. The fluids have a high water share, work in a neutral pH range, are biodegradable and do not consist of aggressive ingredients which offers additional benefits in total cost of ownership.

Since this is a completely new type of stripping chemistry the contamination behavior was investigated in this study by using FTIR, TXRF and ICP-MS methods. Experimental results on silicon samples as well as on 12inch wafers show adequate removability of the cleaning agent by water rinsing. A wet process flow has been developed on pilot line scale with a remaining ionic contamination of <10E10 at/cm? on 12inch wafers [fig. 2]. Finally the phase fluid based cleaning sequence has been tested on silicon samples and 12inch wafers prepared with different types of negative and positive tone resists such as positive chemically amplified E-Beam resists (pCARs), AZ125nXT, THB151N, IX420 and SU-8 varying from 80nm to 48µm in thickness. Additional process steps like plasma etching or implanting have been done to increase the level of complexity. The cleaning efficiency was characterized by optical methods as well as surface analytics. Experimental results indicate the potential to reduce stripping time to between 5min and 15min even for thick photoresists or resist layers post implantation processes.

9051-29, Session 11

Reduction of image placement error on photomask-making for multiple patterning

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ArF immersion lithography is extending by multiple patterning techniques. The technique requires high overlay accuracy in the lithography process. Therefore, the multi-split photomasks have to be high accurate in image placement. The accuracy is strongly related to the pattern density because the photomask patterns are delineated with the electron beam

writer. An exposed area with higher dosage of electrons has higher electron charges on resist surface during the electron beam writing. The accumulated charges on resist surface deflect the electron beam, and the position is drifted. To remove the resist charging, “Charge Dissipation Layer (CDL)” is the most familiar method. All of commercialized CDL materials can improve the image placement error, as shown in figure 1. However, they have some side effects on resist performance for the advanced mask-making process, such as defect quality and resist performance changes1. One of common CDLs induce the excess resist dissolving after TMAH developing process due to CDL coating on resist surface. It is related to acid diffusion from CDL components to resist surface during PEB (post-exposure baking) process. The acid induces the decomposition of the positive-tone chemically amplified resist materials. To suppress the acid diffusion from CDL components, the mask-makers have to remove CDL before PEB process by DIW rinsing. This process disturbs the continuous mask-making flow, such as EB writing, PEB and developing process. Therefore, we have studied many different components to reduce the acid diffusion even if PEB process is applied. Figure 2 showed the film loss (resist dissolving thickness after develop process) after PEB and developing process as compared among without CDL, with commercial CDL and with new CDL. New concept of CDL performed almost zero film loss increasing from without CDL coating process. It is available the develop process after PEB process. Furthermore, the CDL coated resist is no degradation in sensitivity and resolution performance over 30 days. The novel CDL showed much potential for mask-making of multi-patterning.

9051-30, Session 11

Robust complementary technique with multiple-patterning for sub-10nm node device

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EUV lithography is one of the most promising techniques for sub-20-nm half-pitch HVM devices, however it is well known that EUV exposure solutions still face significant challenges. Therefore we have focused on 193 lithography based self-aligned multiple patterning(SAMP), because this SAMP technique easily enables fine periodical pattern. As you know, these SAMP techniques have already been applied to mass productions of all semiconductor devices.

We have already introduced innovative resist core based SADP/SAQP techniques and have demonstrated results in past SPIE sessions[1][2][3][4][5]. Moreover, these 193 extension techniques strongly accelerated shift to 1D layout[6][7]. Although SAMP techniques can be easily extend to the fine grating formation for 1D layout, these line cutting performance will become a very important factor for edge placemen error(EPE).

In this paper, we will introduce the demonstration result of the sub 10-nm logic patterning, and discuss about the EPE including hole shrink performance.

9051-31, Session 11

Advanced develop processes for reducing defects related with e-beam resists

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Masks used for sub-20 nm half pitch of devices are required to be defect-free as well as to have more complicate and smaller patterns. For higher resolution for sub-20 nm device, the masks that can provide wider process windows on wafers are made using negative e-beam resists and new mask materials.

An introduction of advanced mask systems needs methodologies to overcome defect challenges that did not occur at previous mask systems. The defects should be related with chemical and physical properties from negative e-beam resists or/and new type blanks used for advanced masks such as EUV or optical masks. The negative resists which have chemical mechanisms through such as polarity switch or crosslink reactions by secondary electrons, have lower polar solvent dissolution rates. As a mask pattern size is shrunken, the masks also have complicate structures and different surface properties from low end mask systems.

Defect removal on the masks is more important even in a develop process among mask manufacturing processes. This paper reports that advanced technology applications on mask develop processes have performed to remove defects on the masks. First, a new rinse system has applied into a mask develop process for defect reduction during a develop process. Second, improved develop processes were also performed to remove defects on masks. An innovated develop system combined with the new rinse system or/and the improved develop system has reduced more than 50% of defects including e-beam resist residue and small defects.

It mainly focuses on defects related to negative resist on masks and their solutions to reduce or/and remove the defects, which used for sub-20 nm half pitch of devices, in terms of mask develop process.

9051-33, Session 11

Recent progress on multiple-patterning process

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As reported before, the typical 193 immersion lithography film stack (photo-resist/Si-ARC/SoC) was used to implement the SAQP scheme, and the low temperature spacer film deposition was used two times on 1st resist core pattern and 2nd SoC pattern. Therefore, any additional sacrificial film is not needed to form “Core-pattern” through deposition and etching process steps, because key issue in DP process must be the saving process cost. In order to implement the SAOP scheme, most important thing is material selection of the core and spacer pattern fabrication to obtain higher etching selectivity, etching durability, thickness controllability, conformability and wiggling avoidability. The successful result was obtained in SAOP scheme demonstration and final multiplied pattern CD achieved 6nm hp.

9051-34, Session 11

Novel and cost-effective multiple patterning technology by means of invisible SiOxNy hardmask

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The Cost of Ownership (CoO) for semiconductor processing has been primarily dominated by lithography. In multiple patterning processes, additional materials and the impact to throughput of multiple patterning passes appear to become additional major contributors to manufacturing cost as well. We introduce SiOxNy hardmask as a new memorization layer for multiple patterning that addresses the non-lithographic cost contributor to manufacturing. The optical constants of the SiOxNy hardmask are matched to those of the photoresist at the imaging wavelength, and that makes it invisible at the exposure wavelength, enabling lithography directly over the hardmask topography, while at the same time it will be visible to those wavelengths that are used for

alignment and overlay. The SiOxNy hardmask is inserted below the photoresist which will make the rework and integration schemes much simpler and result in a cost saving by replacing only photoresist layers during multiple patterning processes. Additionally, by eliminating the need for traditional spin-cast planarization and the associated tri-layer etch we can reduce the critical dimension uniformity (CDU) and proximity contributions from etch, and their respective etch proximity corrections. In this work, we engineered the lithographic stack to be compatible with the invisible SiOxNy hardmask. Lithographic process windows, CDU, and LER/LWR are compared with conventional trilayer stack and we demonstrate triple patterning memorized into the SiOxNy hardmask after which patterns are then transferred, at once, into the bottom integrated stack. We also investigated the impact of reworking as well as the change in n & k induced by rework and report how it will affect CDU and defectivity. Finally, major benefits of using the invisible hard mask on device scaling and patterning challenges are discussed, such as for LE^2, LE^3, and trench and cut patterning.

9051-52, Session PS1

Innovative solutions on 193 immersion-based self-aligned multiple patterning

Sakurako Natori, Shohei Yamauchi, Arisa Hara, Masatoshi Yamato, Kenichi Oyama, Tokyo Electron AT Ltd. (Japan); Hidetami Yaegashi, Tokyo Electron Ltd. (Japan)

193 lithography related self-aligned multiple patterning(SAMP) is continuously applied to the current advanced technology node. As you know, SAQP scheme has already achieved the capability of 10nm hp pattering resolution. For sub-10nm hp patterning generation, although DSA may become one of the most promising techniques, SAMP has the higher reliability for mass-production application[1][2][3][4][5]. So, we have focused on SAMP resolution limitation by using self-aligned octuple patterning(fig.1). Of course, DSA and SAMP are fundamentally based on same 193 processing technology, therefore the cutting solution which used in 1D layout can be sharable for minimization of edge placement error.

In this paper, we will introduce the demonstration results of the sub-10nm hp LS and sub-20nm hp hole pattern multiplication. Then, for the 1D layout extension, we'll discuss about the EPE tolerance including the hole shrink solutions.

9051-53, Session PS1

Wet particle source identification and reduction using a new filter cleaning process

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Defect adders on wafer after spin coating, sometimes called "wet particles," is a widely used indicator for the readiness of lithography chemical dispense modules. Wet particle reduction during filter installation and start-up aligns closely with initiatives to reduce both chemical consumption and preventive maintenance time. The incidence of wet particles after filter installation has significantly increased since resolution of the on-wafer particle detection metrology has improved to sub-30 nm.. Typically, identification of wet particle sources has been very difficult without a method to directly analyze nanoscale particles. Previous work focused on microbubbles from the filter as a possible source and identified several operational recommendations for improved start-up [1-3]. The present study focuses on the effects of filter materials cleanliness on wet particle defectivity through evaluation of filters that have been treated with a new cleaning process. Furthermore, we explored the relevance of filter extractable results with regard to the identities and origins of wet particles.

Particle cleanliness and solvent extraction tests were conducted in order to compare the impact on wet particle defectivity for a standard commercial point-of-use filter (Pall PhotoKleen EZD-2X PE-Kleen Filter Assembly) and an analogous product that was treated with a new cleaning process (Pall Xpress EZD-2X PE-Kleen Filter Assembly). Solvent extractions from sample filters using PGMEA and methylene chloride were generated and analyzed for various contaminants. ICP-MS was used to quantify metals and GC-MS was used to quantify organic compounds within PGMEA extracts. Methylene chloride extracts were evaporated to dryness and then measured for non-volatile residue (NVR). Results given in Figures 1-3 and in Table 1 show no significant differences between filter types for >40 nm particle cleanliness and metal extractables, however NVR and organic extractables were much lower within extracts of the specially cleaned filters.

Evaluations for wet particle defectivity were conducted using a SOKUDO DUO track system to dispense TOK OK73 solvent through sample filters onto bare silicon wafers. Wet particle measurements were collected using a KLA-Tencor Surfscan SP3 inspection system. Defect performance trends are resolved by measuring wet particles at 500mL dispense intervals, with flow cessation after 4L. Wet particle trends throughout filter start-up is given in Figures 4 and 5. For each filter type the two graphs illustrate a significant difference in defect detection capabilities between established metrology capabilities and a state-of-the-art tool. With established metrology, as illustrated in Figure 4, little difference in filter performance is observed between the two filter types at a size detection threshold of 60 nm. Conversely, clear differences in defect performance are observed at a size detection threshold of 26 nm (Figure 5). Additionally, the more sensitive metrology shows the initial wet particle count after 500 mL dispense with the specially cleaned filter was one-tenth (1/10) that of the standard filter. Similarly, the dispense volume required for the specially cleaned filter to establish a typical performance target (e.g. <100 counts / wafer) was one-quarter (1/4) that of the standard filter. Further, wet particle excursions due to flow cessation were clearly observed in the standard filter upon flow resumption, but not in specially cleaned filter.

Based on these results the newly developed filter cleaning process is effective to reduce organic extractables from the standard filter. It can also be suggested that organic compounds can be identified as a potential source of wet particles. However, the impact is best observed with the most advanced sub-30nm inspection capabilities that are currently available.

Results suggest that organic compounds extracted from filter materials of construction may be a source of wet particles that are detectable by state-of-the-art defect metrology tools. Pall recommends filters that have been treated with the special cleaning process (Xpress) for applications with a critical defect size of less than 60 nm. Standard filter products are capable to satisfy wet particle defect performance criteria in less critical lithography applications.

9051-54, Session PS1

Adsorption characteristics of lithography filters in various solvents using application-specific ratings

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It is known that DUV resist filtration using adsorptive Nylon 6,6 membrane significantly reduces microbridge defects within the lithography process[1-5]. Also, a need has been identified for an adsorption retention performance index that will complement the familiar filter removal ratings that are currently used for microelectronics-grade filter products, which describe sieving retention performance by removal of classical hard particles from an aqueous colloidal system[6].

Previous work has described a method to determine an adsorption performance index for lithography process filters[7]. Using this metrology, adsorption characteristics of a filter that is challenged with modified metal nanoparticles, which simulate interactions with microbridge defect precursors, is quantitatively determined in the form of kinetics

parameters. In this paper, the effects of filter grade, filter material, and solvent type on adsorptive retention are explored. Further, the relationship between adsorption kinetics parameters and solvent properties are discussed.

The adsorption performance index determination method developed in the previous study was employed. The test filters were 10, 20 and 40 nm rated asymmetric Nylon 6,6 and 30 nm rated high density polyethylene (HDPE). The test fluids were PGMEA, cyclohexanone, n-butylacetate (n-BA) and gamma butyrolactone (GBL), all of which were selected as common lithography solvents. Heptylamine-substituted palladium nanoparticles (Pd-HA), which were selected to simulate microbridge precursors, were used as challenge particles. The Pd-HA concentration in the influent was 0.5±0.025 ppb. Flow rate was controlled to vary contact time. The Pd concentration in the influents (=C0) and the effluents (=C) were analyzed using ICP-MS, to calculate removal efficiency (=1-C/C0).

Adsorption kinetics at equilibrium are described by equation (1).

$$-d(C-CE)/dt=k(C-CE)^n \quad (1)$$

Where C=adsorbent concentration, t=contact time, k=adsorption rate constant, n=adsorption reaction order, and CE=equilibrium concentration.

Pd removal efficiency values (= 1-C/C0) were fitted to Eq. (1) using Origin 7.5 data analysis software in order to determine adsorption kinetics parameters k and CE. A second-order relationship (n = 2) was modeled using the results.

Figure 1 shows the results from various filters in PGMEA. Adsorption rate constants, k, and equilibrium concentrations, CE, were determined and are compiled in Table 1. The kinetics parameters in cyclohexanone, n-BA, and GBL are also determined with the same procedure.

Equilibrium concentration (CE) is the Pd concentration in filter effluent at t=∞ and indicates removal efficiency at actual process condition, which is conventionally t = 5 to 20 s in point-of-use resist filtration. Figure 2 shows the averaged CE of the various membranes in four different solvents. As a result, adsorption performance of the all Nylon 6,6 filters at similar contact times was very efficient (0.9 ? 0.95); however, CE did not vary significantly with either membrane or solvent. Some variation with the solvent was found in HDPE 30 nm filter, but CE values were, overall, greater than those for Nylon 6,6 filters (i.e., Nylon 6,6 filters demonstrated greater retention efficiency).

Adsorption rate constant (k) indicates the speed of adsorption and is determined by the slope of the kinetics curve during short contact times. The rise of the particle removal data was observed in only Nylon 6,6 40 nm and HDPE 30 nm and not observed in other filter membranes due to high inherent differential pressure (i.e., Contact time was not sufficiently minimized). In Figure 3, averaged k for Nylon 6,6 40 nm is compared to solvent properties that possibly affect k, such as octanol-water partition coefficient (Log Pow), which indicates hydrophobicity (Greater values indicate increased hydrophobicity), and viscosity. Based on the results, k seems to depend both solvent properties in Nylon 6,6 40 nm. In particular, k is greater in both lower-LogPow and lower-viscosity solvents.

In conclusion, it is possible to predict that, in real lithography processes, adsorption removal performances of tested Nylon 6,6 membranes are similar among the various membrane grades and highly efficient within the solvent types tested. The adsorption rate in Nylon 6,6 40 nm filter was observed to be greater in both lower-LogPow (hydrophilic) and lower-viscosity solvents, possibly providing a direction for improved filtration performance based on the solvent properties. The complemental adsorption kinetics parameters give more accurate suggestion for the filter performance in lithography applications combined with the conventional sieving filter ratings.

9051-56, Session PS1

Removal of highly crosslinked resists and hybrid polymers for single-microparts fabrication and nanoimprint stamp rework

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Thick photoresists, e.g. with 1 mm layer thickness, are widely used for the manufacture of high aspect ratio microstructures, and used as mould for the fabrication of metallic micro parts. The polymer mould consists of high-grade crosslinked polymer materials since they have to withstand the micro fabrication processes. Such resists or materials exhibit high mechanical and chemical stability. The solvent based removal after the pattern transfer process is difficult or not possible in many cases. Selective mould removal – without the damage of electroplated metal structures – is required for the fabrication of single micro parts. For this purpose dry etching techniques are suitable alternatives in a variety of applications since the generated gaseous degradation products of polymers and resists can easily be removed even from small cavities and high aspect ratio dense patterns. By using conventional plasma or dry etching tools non-satisfying results. e.g. remaining of insoluble residues, can be observed. Moreover, these tools are not suitable to remove large areas of crosslinked thick resist or polymer layers with satisfactory results and in a cost efficient time required for industrial use. Hence, we demonstrate the application of a new plasma-assisted etching tool STP 2020 from MUEGGE-R3T [1] consisting of a traveling wave reactor TWR 2000 as source of a cooled high-density flow of chemical radicals for remote dry etching of strongly crosslinked polymers and hybrid materials. The developed etching processes for the isotropical etching of highly crosslinked photoresists as mould for the industrial fabrication of single metallic micro parts and the effective removal of hybrid materials for substrate rework process or nanoimprint stamp cleaning will be presented. In combination with this specific etching tool this technique shows the high potential to make the plasma-assisted removal ready for the industrial production environment.

[1] http://www.muegge.de/products/plasma-systems/stp-2020

[2] http://www.microresist.de/projects/mst_polyaetzen_en.html

9051-57, Session PS1

The research on pattern design that affect the well resistance

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Understanding that root cause of well Rs variation between devices is an effect of pattern design rather than that of deposition material or IIP, studies to describe such phenomenon with parameters have been carried out. We found out that direction and shape of dummy active within Rs monitoring pattern would alter the value of Rs. This is because difference in the pattern of STI bottom which mirrors the active pattern causes changes in a current path which is located at Rp of Well IIP. And, consequently this change in the current is reflected in the value of Rs. Thus, device simulation of different test designs has been carried out to further validate the above theory, and based on this result, a design guide for Rs monitoring pattern is put forth. Furthermore, it is expected that a detailed numerically analysis would enable a resistor to be manipulated through layout design.

9051-58, Session PS1

Characterization of chemically-amplified resists for electron-beam lithography

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The electron beam (EB) lithography is one of the most important candidates for the next generation lithography used for the high-volume production of semiconductor devices. For the manufacturing of semiconductor devices, a highly sensitive resist called a chemically

amplified resist is an indispensable technology. Better understanding of the properties of chemically amplified resists is essential to the application of EB lithography to device manufacturing. In this study, we investigated the properties of chemically amplified resists using a model resist, on the basis of the reaction mechanisms of chemically amplified EB resists. The resist properties such as G-value of acids, stopping power, the effective reaction radius for deprotection, and backscattering coefficient were determined. The details of characterization will be reported. On the basis of the obtained parameters, the trade-off relationship between resolution, line width roughness (LWR), and sensitivity will be discussed.

9051-59, Session PS1

Improved adhesion of novolak and epoxy-based resists by cationic organic materials on critical substrates for high-volume patterning applications

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A variety of resists and polymer materials have to processed on several kinds of substrates, whereas silicon is one but not the mainly used substrate. Since the generated resist patterns have to resist following additive (e.g. electroplating, physical vapour deposition (PVD) by sputtering or evaporation) or subtractive procedures/ processes (e.g. wet or dry etching) – resists are processed on a variety of substrates to manufacture step by step the final device. Silicon - a semiconductor – as substrate is used for wet and dry etch processes e.g. also for the manufacture of micro parts or also for the additive procedure PDMS mould fabrication. III-V semiconductor substrates based on GaAs, InP or GaP or a combination of these are mainly used in microelectronic and optoelectronic applications, e.g. for the manufacture of LEDs. Typical substrate surfaces for electroplating processes are TiOx, gold or copper as seed layer often used in combination with SU-8. Other substrates are silicon dioxide, ITO, glass or ceramics for etch processes. For the patterning of the resists and pattern transfer processes an excellent resist adhesion on the used substrate is a condition precedent. Less adhesion of the resists on the substrates lead to defects in the resist pattern design and the desired pattern transfer process like wet or dry etching, electroplating, PVD and lift-off can not be done without any defects.

In order to improve the resist adhesion on substrates and when HMDS as adhesion promoter can not be used SurPass adhesion promoter was introduced to the fabrication processes. SurPass is a waterborne, non-hazardous cationic organic material that promotes adhesion by modifying the surface energy of the substrate material without deposition, chemical change, or impact on electrical properties. Depending on the nature of the resists either SurPass 3000 or SurPass 4000 is recommended to use. SurPass 3000 is recommended to use in combination with an epoxy based resist, e.g. SU-8 and it works perfectly for the SU-8 mould preparation on e.g. gold substrates. SurPass 4000 is recommended to use in combination with novolak based resists and works perfectly on silicon or typical III-V semiconductor substrates. The application and use of SurPass adhesion promoter on several substrates will be presented. After the development of the resist patterns no additional process step is required and the substrates are ready for the subsequent pattern transfer processes.

[1] www.dischem.com

[2] W. Erfurth, A. Thompson, N. Ünal “Electron dose reduction through improved adhesion by cationic organic material with HSQ resist on an InGaAs multilayer system on GaAs substrate” Proc. SPIE 8682, Advances in Resist Materials and Processing Technology XXX, 86821Z (March 29, 2013); doi: 10.1117/12.2018121

9051-60, Session PS2

Modeling acid transport in chemically-amplified resist films

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As the feature sizes in microelectronics circuitry continues to decrease, it is becoming increasingly important to study processes occurring at the nanoscale in lithographic films. These processes are significant factors in determining the final feature size and line-edge roughness. Recent ITRS reports also emphasize the need for quantitative models that predict the behavior of the resists under different imaging and process conditions, and facilitate the screening of resist materials and process development.

We investigated the controlling physical and chemical processes in chemically amplified resist (CAR) films of poly(4-hydroxystyrene-co-tertbutyl acrylate) resin. The resin was loaded with 1 to 4 wt% of photoacid generator, and acid catalyst was activated with flood exposure to deep ultraviolet light (254 nm). Deprotection reactions (post exposure bakes) were carried out for times ranging from 5 sec to a few hours on a bake plate. These reactions were always implemented at temperatures below the polymer’s glass transition. Deprotection of tert-butyl acrylate moieties was monitored with infrared absorbance spectroscopy. Data were analyzed by modeling the reaction-diffusion processes with stochastic simulations. The simulations assumed that deprotection is very fast, so mobility of acid catalyst in the polymer resin was the rate limiting factor in describing the observed deprotection kinetics. We modeled acid hopping with two types of random walks that reproduce either Fickian or anomalous (sub-diffusive) transport. The experimental deprotection rates show fast reaction at short times, slow reaction at long times, and a stronger-than-linear dependence on the acid concentration. These findings are consistent with observations from other literature studies. The simulated deprotection rates using Fickian diffusion capture the correct time scale, but they underestimate the short-time conversion, overestimate the long-time conversion, and exhibit a linear dependence on acid concentration. Inclusion of additional reactions (such as acid trapping) does not improve the agreement between simulation and measurements. However, the simulations based on anomalous acid transport show near quantitative agreement with experimental data at all temperatures and acid loadings, provided that a slow acid loss mechanism is included in the algorithm (a phenomenological second-order annihilation process). Significantly, this model requires only two free parameters - an anomalous exponent ($\gamma < 1$) and characteristic time (τ). Anomalous diffusion implies that polymer dynamics are controlling the reaction kinetics in glassy CARs. The parameters extracted from these simulations and their scaling with temperature are remarkably consistent with other studies of probe diffusion in glass formers.

9051-61, Session PS2

The investigation of hybrid nanoparticle EUV photoresists: Influence of electrolyte solution on the particle size change

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With the development of nanofabrication and shrinkage of feature size for semiconductor device, photolithography technology that can provide high resolution patterning is required. Research in short wavelength lithography, especially for extreme ultraviolet lithography (EUV), is attracting considerable attention. The next generation EUV photoresists should combine high etch resistant, high imaging quality and appropriate light absorption. Previous results in our group showed that hybrid nanoparticles composed of inorganic metal oxide core and organic ligands had excellent dual tone photo-patterning performance under EUV

exposure. A record lowest dose of 4.2 J/cm2 for EUV photoresists with negative patterning has been achieved.

This presentation is focused on the investigation of dual tone patterning mechanism with hybrid inorganic/organic photoresists. It is hypothesized that the particle size change of nanoparticles leads to their solubility difference in the developers before and after exposure, and thus forms high sensitivity photo-patterning. In the current presentation, hafnium oxide (HfO2) modified with acrylic acid (AA) was prepared and the influence of different electrolyte solutions on its particle size change was investigated. The chemical composition of HfO2/AA nanoparticle was analyzed with Fourier transform infrared spectroscopy (FTIR). Inorganic content of the nanoparticle was measured by thermo-gravimetric analysis (TGA). The average particle size and zeta potential of the nanoparticle in different electrolyte solutions were measured by dynamic light scattering (DLS). The results show that addition of different concentrations of sodium chloride (NaCl) and magnesium chloride (MgCl2) decreased and increased the hydrodynamic diameter of HfO2/AA in the water, respectively, with little variation of pH in the solution. Increased concentration of tetramethyl ammonium hydroxide (TMAH) caused the zeta potential of nanoparticle to change from positive to negative and its hydrodynamic diameter to increase dramatically from 40 nm to 165 nm. In addition, the influence of triflic acid on the size change of nanoparticle was also studied. Increasing concentration of triflic acid led to the decrease of particle size and zeta potential. The combined influence of triflic acid and TMAH on the particle size change was then investigated. This research provides for the first time fundamental study about the inherent nature of hybrid nanoparticle photoresists, their behavior in solution, and framework to start thinking about optimization of development under various conditions of solution and pH. The results shown in the paper are helpful to promote the understanding of dual tone mechanism.

9051-62, Session PS2

Deprotonation mechanism of ionized poly(4-hydroxystyrene)

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Chemical amplified resist using an acid catalyst chain reaction has been used as a mainstream material for the mass-production. Since the reaction mechanism in EUV resist is radiation induced reaction, the elucidation of the mechanism is an important issue. Poly(4-hydroxystyrene) (PHS) is widely used as base polymer of the resist, because it is a proton source of the acid generation used for the chemical amplification mechanism. The enhancement of deprotonation efficiency is important factor to increase the sensitivity of resist. Although the deprotonation of PHS is assumed to be similar to that of phenol derivatives, the mechanism of PHS deprotonation is still unclear because of the presence of the polymer effect (adjacent effect) and the low solubility of PHS in halogenated carbons and alkanes in which radical cations of solutes are produced commonly in radiation chemistry. In this research, pulse radiolysis of PHS was carried out to directly examine the deprotonation rate constants (kDP) in various solvents of radical cations for fundamentals of the deprotonation mechanism of PHS. The dependence of solvent properties such as polarity and proton affinity on deprotonation is clarified. The influence of several additives such as sulfoxides and amides on the deprotonation of PHS was also investigated to clarify the fundamentals of the enhancement of deprotonation efficiency from the PHS radical cation.

Pulse radiolysis was performed in ISIR, Osaka University by using LINAC (28 MeV, electron pulse width 8 ns) to observe short lived intermediates of PHS after ionization. Xe flash lamp was used as an analyzing light source. The analyzing light was transmitted to the optic lens and mirrors, sample cell, monochromator (Ritsu MC-10N) and, photodiodes [Si (350–950 nm) and InGaAs (950–1600 nm)]. The signals from the photodiode were measured using a digital phosphor oscilloscope (Tektronix DPO7254).

The mechanism of deprotonation of PHS cations in solutions was investigated by observing the transient absorptions. The radical cations of PHS which are proton source of acid in the chemically amplified resist are produced through hole transfer from ionized solvents. The formation of multimer radical cations as charge resonance band of multimer cation is observed in near-infrared region (900~1600 nm). The cationic species of PHS then cause deprotonation.

The deprotonation of PHS in the solvents with low proton affinities (<850 kJ/mol) is mainly controlled not by a solvent characteristic, but by an intramolecular interaction in the polymer. The correlation is shown similarly to the case of the PHS film system. On the other hand, the fast deprotonation within the 8 ns EB pulse was observed in dimethyl sulfoxide and formamide. In the diluted solutions of dimethyl sulfoxide and formamide, the deprotonation is observed directly. With increasing the sulfoxide and amide concentration in PHS/cyclohexanone, the deprotonation is clearly accelerated. The obtained second order kDP was about 2?108 M-1s-1 which is 10~102 order smaller than a diffusion controlled reaction. It is considered that the deprotonation by sulfoxide and amide is blocked by the PHS polymer entanglement that derived from the intramolecular hydrogen bond.

9051-63, Session PS2

Numerical analysis for resist profile after thermal process in display manufacturing

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The screen size growth of mobile displays is accompanied with the drastically increased resolution. A display should have high pixel resolution to meet demanding readability and legibility expectations. The manufacturing process should be advanced to meet final device requirements. One of the important process steps is post-development hardbake, where resist reflow is used to tune the final profile which influences follow-up processes. Moreover, 3D resist profiles become one of critical design factor for mechanical and optical properties of display pixels. The resist reflow is the main time- and temperature-dependent effect of post-development bake process step. Since resist is in transitional state (crystalline glassy / amorphous rubbery / viscous melt) the resist profile dynamics are very complex and predictive modeling is necessary. The model presented in this paper is based on lattice-Boltzmann method, where the resist is considered as multicomponent (polymer-solvent) and multiphase (solid-liquid-vapor) mixture. Simulated resist profile dynamics with time is analyzed in dependency of material parameters (solvent diffusivity and evaporation rate, polymer solid fraction and adhesion with substrate). Temperature-dependent parameter descriptions are used for model calibration. Validation against experimental data shows good model consistency and predictability, demonstrating the benefit of simulation in process development and optimization.

9051-64, Session PS2

Photoresist analysis to investigate LWR generation mechanism

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Semiconductor industries continuously requires size-seeking on lithography. In the past, lithography resolution was minimized by

shortening wave length of exposure system from 436nm to 193nm, in addition, applying immersion process. This trend enhances optical contrast to improve photoresist pattern resolution. Recently, this technology stream is down speeding, since delay of EUV mass production insertion. Therefore, it is getting more important to improve photoresist pattern quality by exposing ArF immersion process combining with process trick such as multiple patterning. Since optical contrast gets weaker for required target, well-controlled patterning photoresist reaction is important to achieve necessary resolution and its pattern roughness control.

In this study, we investigated photoresist patterning mechanism in order to use this knowledge for further photoresist development. Current ArF photoresist is composed by acryl based polymer with leaving group, photo-acid-generator (PAG) to catalyze reaction of leaving group and quencher for air-born contamination suppression and photospeed control. We investigated photoresist patterning mechanism step-by-step and its variation by using spectroscopy such as MS, IR, NMR, and so on. We quantified polymer leaving amount, distribution of reactant so on. This result would accelerate not only photoresist performance improvement, but also improvement and simplification of device production process and photoresist quality controls.

9051-65, Session PS2

Decreasing curing temperature of spin-on dielectric by using additives

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Spin-on dielectric (SOD) is widely used in semiconductor industry, to form insulating layers including shallow trench isolation (STI) or inter-layer dielectrics (ILD). SOD has several advantages over high density plasma chemical vapor deposition (HDP-CVD) for manufacturing process, such as less defect and higher throughput. However, both SOD and HDP-CVD have a drawback, which is a high temperature curing process required to make pure silicon oxide layers. High temperature curing could cause high stress and thermal distortion. These disadvantages become more problematic as the semiconductor device shrinks. To resolve the problem, we tested several additives to reduce the curing temperature. It was found out that certain compounds were effective to convert SOD polymer into silicon oxide, therefore the curing could happen at lower temperature. We also observed that the SOD containing additives has less shrinkage of film thickness when cured, and higher etch resistance during a wet etch process. These results, as well as the curing temperature lowered, are benefit to make better insulating layers. Further investigation is on the way to optimize the formulation conditions, according to the requirements of manufacturing processes.

9051-67, Session PS2

Study of acid diffusion behaves form PAG by using topcoat method

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To date, we have conducted research on measurements of simulation parameters for ArF resists. The following parameters were the focus of our research:

- Development parameters
- PEB parameters
- Dill's ABC parameters
- The quencher parameter

We entered these parameters into a lithography simulator and performed ArF resist simulations, then optimized the ArF resist material and process based on these results. This paper reports on our study of methods for measuring the diffusion length of photogenerated acid during exposures. We applied a coat of TC (a second layer) containing PAG on the PAG-free ArF resist layer (the first layer), then performed the exposure and PEB. The acid generated during the exposure in the TC diffused into the lower ArF resist layer (the first layer) when the PEB was performed. Developing this sample removed only the areas with the TC and the parts of the first layer into which the acid had diffused. We obtained the acid diffusion length based on the film loss quantity observed following development [1] (see Fig. 1). We repeated this measurement while varying the exposure value, then calculated the diffusion coefficient of the acid. Fig. 2 shows the exposure value, acid diffusion length, and the results of fitting with Fick's equation. As part of the research reported here, we also made measurements to determine how a PAG characterized by different anion sizes and quencher additives might affect the diffusion coefficient of the acid. We entered the measured values into the PROLITH simulator to explore the effects of acid diffusion on pattern profile.

9051-68, Session PS2

Fluidity dependence of deprotonation kinetics of chemically amplified resist

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The ionizing radiation such as EUV and electron beam (EB) has been one of the most promising exposure sources for the technology of semiconductor miniaturization. It is important to investigate the reaction mechanism of the exposed resist concerning short-lived intermediates. Therefore, the radiation chemistry of resist has been investigated in the various resist model compounds for the improvement of resist performance. Poly(4-hydroxystylene) (PHS) is one of the typical resist constituent for EUVL and EBL for the proton source of chemically amplified resist. Although direct observation of intermediate in a solid state is desired, it is technically difficult to observe solid state of PHS by pulse radiolysis because of the low transmittance of analyzing light (visible~ near-infrared). Thus, we investigated the viscosity dependence on deprotonation dynamics of PHS in the concentrated solutions by using pulse radiolysis technique to assume the deprotonation in the solid state.

PHS concentrated solutions (about 10?60 wt%) were sealed in a quartz cell. Ionization was induced by pulse radiolysis methods which were performed by using electron beam from the LINAC at ISIR, Osaka University (28 MeV, 8 ns pulse width) and Hokkaido University (45 MeV, 50 ns pulse width).

Ionized PHS forms positively charged state [radical cation (PHS?+)]. Two type (fast and slow) deprotonations of PHS?+ are suggested. The latter one depends on the molecular motion. A rate constant of the aggregated PHS?+ [(PHS) n?+] formation and decay which is identical to that of deprotonation (kD) is determined. The slow formation process of (PHS) n?+ was clearly observed. It is suggested that the yield of (PHS) n?+ increases with PHS concentrated due to the delay of the deprotonation from PHS?+. In addition, with increasing PHS concentration, reaction rate constant of deprotonation of PHS?+ and (PHS) n?+ decreased. For these reasons, it is suggested that deprotonation reaction is more slowly in a PHS concentrated solution in order to reduce the molecular entanglements and intermolecular interactions. The deprotonation reaction of solid state of PHS is expected more than ?s order.

9051-69, Session PS3

Inorganic resist materials based on zirconium phosphonate for atomic force microscope lithography

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New inorganic resist materials based on metal complexes were investigated for atomic force microscope (AFM) lithography. Phosphonic acids are good for self-assembly because of their strong binding energy. In this work, zirconium phosphonate system are newly synthesized for spin-coatable materials in aqueous solutions and leads to negative tone pattern for improving line edge roughness. Low electron exposure by AFM lithography could generate a pattern by electrochemical reaction and cross-linking of metal-oxo complexes. It has been reported that the minimum pattern results are affected by lithographic speed, and the applied voltage between a tip and a substrate.

9051-70, Session PS3

Tailor-made inorganic-organic hybrid polymer materials for advanced micro- and nanolithography processes and production

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Advanced micro- and nanolithography processes are constantly evolving from academic R&D environment towards real production technology. For the easy, cost-effective and reliable manufacture of micro- and nanopattern, the availability of suitable materials plays a crucial role to satisfy the numerous requirements from state-of-the-art as well as future patterning technologies. Besides application motivated specifications, the technical compatibility to various micro- and nanofabrication technologies is an additional but essential aspect to be considered for the development of commercial material solutions.

In this contribution, we will highlight recent material innovations developed at micro resist technology GmbH which are based on the class of UV-curable hybrid polymers, i.e. inorganic-organic materials obtained by sol-gel chemistry [1]. These non-toxic tailor-made materials are highly suitable for realizing micro-optical applications such as camera lenses, LED's, waveguides, etc. [2]. Hybrid polymers such as OrmoComp® do not only meet the constantly growing expectations for the material's optical performance due to their excellent transparency and non-yellowing behavior. They also exhibit a high thermal, mechanical and chemical stability as well as a high UV-sensitivity. This makes them highly suitable for conventional UV-lithography, direct patterning and ink-jet printing for industrial productions at the micro scale.

Furthermore, high throughput nanofabrication is enabled by inorganic-organic hybrid polymers like OrmoStamp®, which can be used for the fabrication of working stamps in thermal and UV-based nanoimprint lithography (NIL) and therefore can serve as cost efficient alternative to quartz stamps [3]. The OrmoStamp® formulation was adapted to minimized release forces by incorporation of fluorinated chemicals, which severely improved the replication from the master original due to decreased mechanical load during demolding with enhanced release-properties due to fluorine-components. This optimized composition makes OrmoStamp® compatible with NIL polymers as well as all hybrid polymers developed by micro resist technology GmbH. Thus, the ability to easily generate specialized transparent molds with optimized release-properties at low-costs [4] allows NIL to be employed for the replication of micro- and nanopattern in hybrid polymers such as OrmoComp® or OrmoCore for a variety of applications, e.g. nanofluidic devices [5] or optical ring resonators [6].

In summary, tailor-made polymer solutions were developed for enabling innovations in micro- and nanolithography and related technologies. By giving different examples, we demonstrate that this material class will enable innovative applications and increase the acceptance of advanced technologies being used in industrial productions.

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9051-71, Session PS3

Organic-inorganic hybrid resists for EUVL

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According to ITRS-2011, resists are one of the critical areas for the development for EUVL. They should exhibit high resolution, low line-width roughness (LWR), and high sensitivity. However, many inherent problems such as acid diffusion, post exposure instability exist in the currently used chemically amplified resist (CAR) technology. The present project encompasses the design and development of resists that are directly sensitive to photons without utilizing the concept of CARs. These new resist materials; while highly sensitive to photons of various wavelengths, function as chain scission resists to attain the 16 nm node and down to 10 nm. In this program, we have successfully developed and tested different polyoxometalates (POMs) cluster based hybrid resists that show resolution down to 20 and even 16 nm line patterns under electron beam exposures. POMs are a class of inorganic materials consisiting of discrete, soluble, anionic metal oxide clusters of early transition metals, especially W, Mo, V and Nb. POMs show strong absorption spectra in the deep UV region and because of the high atomic number of the metals in POMs, their absorption cross section for X-rays and high energy e-beam radiations is typically much greater than that of organic materials.

Our initial results showed high sensitivity of POM-organic polymer blend resists towards e-beams and these materials would therefore be useful for EUVL down to the 20 nm node and below. High resolution patterning of POM-organic polymer blends was carried out using 20 KeV e-beam lithography. In one of the experiments, hybrid blend resist of PMMA with [(n-C4H9)4N]2[Mo6O19] cluster was patterned for 20 nm line using 20 KeV e-beam lithography and developed in 1:3 MIBK for 30 s followed by 15 s in IPA. Exposed regions of PMMA-[(n-C4H9)4N]2[Mo6O19] resist film readily dissolved in an aqueous MIBK developer while the unexposed regions were maintained as such. We obtained 20 nm L/4S, L/2S patterns which were not observed in control experiments done using pure PMMA polymer resist at comparable exposure doses, below 100μC/cm2.
We have studied few more POM-organic blends resists as explained above by using different molybdenum POMs [(n-C4H9)4N]4[Mo8O26], [(n-C4H9)4N]4[P2Mo18O61] and H5PV2Mo10O65.H2O with MAPDST homo polymer and copolymers, which proved useful down to the 16 nm L/S node as well.

Our main goal is to make POM-organic hybrid polymer resist materials which involve two steps: 1) preparation of POM-organic monomer by covalent attachment of styrene based organic monomers with [(n-C4H9)4N]2[Mo6O19] cluster and 2) homo or co-polymerization with MMA and MAPDST monomer which contains a sulfonium group. The expected advantages of these hybrid resists include enhanced mechanical properties of thin films, enhanced thermal stability, high contrast and enhanced etch resistance, thus making them suitable candidates for EUVL resists. These hybrid resists are directly sensitive

to deep ultra violet (DUV) /extreme ultra violet light (EUVL) and e-beam irradiation without utilizing the concept of chemical amplification (CARs). Moreover, they are expected to meet the requirements of high throughput with no significant changes in EUV fab manufacture. Details of synthesis, e-beam and EUV exposures will be presented.

9051-72, Session PS3

Development of high-carbon spin-on hard masks for high-resolution lithography

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Spin-on carbon (SoC) hard mask materials are widely used for high resolution pattern transfer to silicon substrates. The SoC HM formation process is cheaper as they employ regular wafer processing tracks compared to other alternate deposition methods such as chemical vapor deposition (CVD) of amorphous carbon (ACL). Polymers used in SoC HM formulations use high carbon containing organic polymers with good solubility in casting solvents to meet high etch resistance required during fluorocarbon based plasma etch processes. Several issues such as pattern wiggling and how to overcome those issues are already described in the literature.1-2 In this publication, lithographic performances of a group of high carbon SoC HM formulations will be reported. In addition, coating, etch, defect and filling properties of some of the formulations will be described.

1. Lin et al., J. Photopolym. Sci. Technol. 24 (2011) 503-510

2. Glodde et al., Proc. of SPIE Vol. 7972, 797216-1 to 797216-8 (2011)

9051-73, Session PS3

Effective resist profile control for 20nm node and beyond

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As the critical pitch and critical dimension (CD) continue to shrink, the optical intensity distribution between different patterns becomes more complicated. For the 20-nm logic node and beyond, it is difficult to improve the resist resolution and maintain the same resist sidewall profiles for different patterns. For example, when a high-resolution resist is developed to meet the hole-pattern requirement, the trench pattern would easily suffer T-top induced scum. Improving resist resolution and profile simultaneously is necessary for low k1 manufacturing.

In this paper, we introduce new techniques to deal with the trade-off between resist resolution and profiles. New floatable PAG, floatable additives, and monomer groups for profile modification are discussed. Based on X-SEM results, the original T-top profile can be improved without resolution loss using this new approach. With the help of floatable PAG, the trench scum can be improved from 73% to an undetectable level. Moreover, optimizing the polymer with a more hydrophilic monomer can improve the scum from 73% to 7%.

9051-74, Session PS3

Study on resist performance of chemically-amplified molecular resist based on noria derivative and calixarene derivative

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The trade-off relationship between sensitivity, resolution and line edge roughness (LER) is the most serious problem in EUV lithography. To meet these strict demand for next generation lithography, novel materials must be developed for chemically amplified resists.

As the size of resist patterns is reduced, the molecular size of the resist materials becomes more important. In the case of the polymer resist, the resolution and LER are likely to be inferior to those of the molecular resist because of the difference in molecular size. If a resolution of less than 22 nm is fabricated using polymer- based resist materials, the line width corresponds to 5-6 molecules of the polymer. Thus, the reduction of the grain size is believed to be a fundamental improvement in the ability to consistently obtain lower LER because molecular resists have no dispersion of molecular weight. Moreover, the reduction of the molecular size is an inevitable trend in order to resolve ultra-fine patterns. As above-mentioned, molecular resists is likely to be superior to polymer resists because they might influence the resolution and LER of the resist pattern.

In this study, we developed positive-tone chemically amplified molecular resists based on a Noria derivative and a calixarene derivative. We evaluated the lithographic performance using EUV and EB in order to explore the potential of them as a positive-type EUV and EB resist.

Noria derivative resists and calixarene derivative resists were used as a resist. Propylene glycol mono methy ether acetate (PGMEA), propylene glycol methy ether (PGME), Ethyl lactate (EL), Dyglyme were used as casting solvent and without further purification. Triphenylsulfonium trifluoromethansulfonate (TPS-nf) were used as acid generator and without further purification. Resist solutions were spin-coated onto Si substrates at 3000 rpm for 30 s to form thin films. The resist samples were exposed to EUV and EB. After the exposure, they were baked in the temperature range of 110 ˚C for 60 s. Then, the resist performance of them was evaluated using EUV and EB.

When the pillar[5] arene resist containing 10 wt% TPS-nf was used, a semi-isolated pattern with the line width of 20 nm (pitch: 100 nm) was delineated. In addition, The etching rate of the noria derivative and calixarene derivative resists was similar to that of conventional resist materials such as ZEP520A and UV?. Thus, noria derivative resists and calixarene derivative are promising candidates for the resist material for nanolithography such as EB and EUV lithography although further development of high performance resist based on noria derivative and calixarene derivative are essential.

9051-76, Session PS3

SRAF window improvement with under-coating layer

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ArF immersion lithography has been extended by many resolution enhancement techniques. Furthermore, the multi-patterning with NTI (Negative-Tone Imaging) technique is extending the optical lithography beyond 20nm node. To effectively achieve the lithography, the bright field masks of attenuated phase shifter must be required for wider process window. For the bright field mask-making, high resolution negative-tone resist is strongly demanded from the industry. The sub-resolution assist feature (SRAF) on mask requires about 40nm resolution for 1x nm node. The negative-tone resist resolution of SRAF patterns is regulated by pattern collapse during developing process. Especially, the collapse is strongly related to an aspect ratio, which number is “resist thickness” divided by “feature size”. To make small SRAF patterns, resist thickness is continuously reducing; however, the thinning is limited by the margin of an absorber film etching. To make small SRAF patterns with high aspect ratio, an under-coating material has been developed for the prevention of pattern collapse1. The under-coating material improved the resist pattern resolution. A negative-tone resist on the under-coat showed 30 nm isolated line pattern on mask without pattern collapse, as shown in figure 1. The resist thickness was over 130 nm. Namely, the under-coat application overcomes the aspect ratio 3. Pattern collapse is related to the under-cutting resist profile as well as aspect ratio. In figure1, 35nm isolated line has the under-cutting on Cr surface. On the other hand,

no under-cutting profile was observed on the under-coating layer. The improvement of SRAF resolution with under-coating was also evaluated. The test layout can evaluate 2D SRAF pattern with various length values and various width value. We employed a negative-tone resist with 130 nm coating thickness with and without under-coating on Cr film. The minimum SRAF without under-coating was practically 80nm width, 120 nm length and 130nm thickness, as shown in figure 2(a). Smaller SRAF showed the pattern collapse as shown in SEM image. It will be unacceptable for the advanced mask making. On the other hand, the minimum SRAF with under-coating was 46nm width, 300nm length and 130nm thickness nevertheless the same resist was employed. The under-coating can dramatically improve the SRAF window as shown in figure 2(b). In this paper, we will report the mask-making performance with a novel under-coating as well as SRAF window improvement, such as CDU and so on.

9051-77, Session PS3

Development of new xanthendiol derivatives applied to the negative-tone molecular resists for EB/EUVL

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We have been developing negative-tone molecular resists based on calix[4]resorcinarene derivatives. In our previous study, we could confirm the excellent patterns with high resolution and small LER by using this resist by EB/EUVL. However the pattern collapse was shown at sub 30 nm half-pitch, so it should be improved.

So we reported the new negative-tone molecular resists based on the new xanthendiol derivatives. The new xanthendiol derivatives were easily synthesized by the condensation of aldehydes and dihydroxyaromatic compounds. We found 13-biphenyl-13H-benzoxanthen-3,10-diol, MGR202, was showed the good applicability to the raw material for the resist for EB/EUVL. The molecular weight of MGR202 is only 467, but coat ability is good because of amorphous compound. Solubility for the coating solvents, PGMEA and PGME, and the glass temperature of 130 degree celsius (°C) are also good.

We reported the EB patterning result showed that the resist containing MGR202 on an organic layer substrate could resolve the 30 nm half-pitch pattern. However by optimizing formulation and conditions, we found the resist containing MGR202 could resolve the 20 nm half-pitch pattern without pattern collapse. Furthermore 15 nm half-pitch patterns were partially resolved.

We will also present the EUV patterning result at the presentation.

9051-78, Session PS3

Organic coating material tuning for CMP

Su Yu Chung, TSMC Taiwan (Taiwan)

When critical dimension (CD) shrunken to that of the 16-nm node and beyond, planarization of the under-layer resist is increasingly important for both the critical and the non-critical layers. For non-critical layers such as implant, planarization is required to reduce the under layer over-etch that will lessen the silicon substrate damage. For critical layers, planarization can improve the depth of focus and the CD uniformity. Spun-on-coating (SOC) has advantages in high throughput and low cost as compared to other deposition processes but it suffers from thickness biases between dense and isolated topographic features on the substrate. This is the fundamental challenge that needs to be met.

In this paper, we introduce a new CMP process with new SOC material formation. The new formulation includes a new polymer structure to improve its adhesion to the substrate. New cross-linker and catalyst are also introduced. From post CMP X-SEM image check (Fig. 1), the within-die thickness bias can be reduced to 3 nm from 137 nm.

9051-79, Session PS3

Chemical shrink process for NTD (Negative Tone Development) resist

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While EUV lithography is expected as emerging technology, still several efforts are required to utilize in actual device production. In such situation, extension of immersion ArF lithography is expected. NTD (Negative Tone Development) process is one of the solutions. The advantage of NTD over standard PTD (Positive Tone Development) process is reported by many researchers. .

However, practical CD (Critical dimension) of NTD is over 30nm even using i-ArF, additional technic to reduce CD has been required.

For this purpose, NTD shrink process has been developed. NTD shrink process is categorized in chemical shrink process and is composed with 1) coat ShM (Shrink Material), 2) apply mixing bake and 3) develop by DIW or organic solvent. The experimental result was reported in SPIE 2013.

By the way, chemical shrink process is commonly used in PTD process also. One of the benefits of PTD shrink is there is no shrinkage shift on pitch variation of patterns.

While on the other hand, occasionally ID bias are seen in NTD shrink process. In this paper, we will discuss the cause and show how to address this subject.

Pattern pitch effect on PTD Shrink process is shown in Fig. 1-1 and 1-2. There is no significant ID bias (Isolation-Dense bias). The ID bias of NTD shrink process is shown in Fig.2. It is clearly seen that shrinkage increase by lower pattern pitch.

By comparing PTD and NTD, it can be conclude that pattern topology is not the cause of shrink variation in NTD. The difference of resist in pattern was summarized in Table-1.

In order to equalize resist condition in NTD pattern, the easiest way is to apply flood exposure to decompose PAG (Photo Acid generator) or apply PDB (Post Development Bake) to decompose PAG. The experimental result using PDB was shown in Fig.3.

We are acquiring data for further discussion at the conference.

9051-80, Session PS3

Novel polymeric sulfonium photoacid generator and its application for chemically-amplified photoresists

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Photoresists are the key materials for the manufacturing of semiconductor device. Chemically amplified resists (CARs) which involved the photoacid generator (PAG) have been widely used since 1980s because of the high sensitivity. The inherent incompatibility between the polymer matrix and small molecular PAGs leads to problems including PAG phase separation, non-uniform initial PAG and photoacid distribution, as well as acid migration during the post-exposure baking (PEB) processes. The polymeric PAGs based resist systems which incorporated the PAG units into the main chain showed improved lithographic performance, such as faster photospeed and higher stability, lower outgassing, and lower LER than corresponding blend resists. In this paper, with poly (4-hydroxylstyrene) (PHS) as raw material, a new type of polymeric photoacid generators (PAGs) was synthesized with sulfonuium triflate groups bonded onto part of the benzene rings. The phenolic hydroxyl group was partly esterified to improve its solubility in common organic solvents for resists. Upon irradiation to light, the sulfonium units in the polymer effectively decomposed to generate sulfonic acid. The properties of the novel polymeric PAGs were investigated. Chemically

amplified photorsists can be formed by the polymeric PAG and other film forming material containing acid labile groups.

9051-81, Session PS3

Evaluation of novel hydrophilic derivatives for chemically amplified EUV resists

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EUV lithography is the most favorable process for high volume manufacturing of semiconductor devices beyond 1X nm half-pitch. Many efforts have revealed effective proton sources in acid generation in EUV resists, and the effective proton generation and the control of the generated acid diffusion are required to improve the breakthrough of the of the resolution ? line width roughness ? sensitivity(RLS) trade-off. To clarify the lithographic performance of these derivatives, we synthesized the acrylic terpolymers containing novel hydrophilic derivatives as model photopolymers and exposed the resist samples based on these polymers to EUV and EB radiation. On the basis of the lithographic performances of these resist samples, we evaluated the characteristics of hydrophilic derivatives upon exposure to EUV radiation. We discuss the relationship between the chemical structures of these derivatives and lithographic performance.

9051-82, Session PS3

ArF photoresist polymers with nitrogen or sulfone moieties for negative tone development process

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Negative tone development (NTD) has been investigated extensively, driven by the needs for new materials and processes to achieve smaller feature sizes. NTD process can exhibit increased optical contrast due to the use of bright mask to largely covered layer such as C/H and narrow trench layer with ArF immersion exposure, whereas it has been found that positive tone development process with dark mask do not provide such contrast. Polarity change type photoresists with organic solvent developers has been studied as a candidate for ArF NTD, because large contrast in dissolution rate can be obtained by the polarity change of resist polymers when de-protection reaction occurs. Although cross-linking type negative photoresists stand as the competitor of NTD, lack of contrast and swelling of the resists causes detrimental effects on the lithographic performance.

In NTD process, it is important to optimize the combination of photoresist polymers and developers, because it affects the dissolution rate of polymers and lithographic patterns. Another advantage of the NTD process is that the conventional polyacrylate photoresist system can be applied to the process without further altering the resin. However, as there are certain differences between the NTD and conventional PTD process, the resin system and the component of the photoresists should be investigated thoroughly.

In this study, we designed photoresist polymers containing nitrogen moieties or sulfone moieties to see the effect of heteroatoms on the lithographic process. Nitrogen-containing photoresists have been designed to study the quencher-bound photoresist system. Also, we have incorporated sulfone moiety into the backbone of the resin itself to obtain a highly compatible poly(vinyl sulfonate) and poly(vinyl sulfonamide) photoresists.

A series of polymers with different molecular weights and monomer compositions were prepared to investigate the effect of polymer structure on the lithographic performance in NTD process. Conventional ArF photoresist polymers (Ref) were also synthesized for comparison purposes. It was found that there are optimum molecular weights of polymers to give good lithographic performance. Among the polymers with nitrogen moieties, polymers (PAM) with 2-(dimethylamino)ethyl methacrylate monomeric unit were found to be soluble in n-butyl acetate (NBA), an organic developer and were applied for lithographic patterning tests. Photoresists containing the PAM exhibited poor lithographic performance, possibly due to the large amount of acid-quenchable amine moieties in the polymers. When the photoresists were prepared with acid additive to neutralize the amine moieties, the lithographic results could be improved to obtain C/H patterns.

Among the polymers with sulfone moieties, polymers with N-(1-adadantyl)vinyl sulfonamide (PSA) or N-(1-adadantyl)vinyl sulfonate (PSO) moieties are soluble in NBA. Negative tone patterning of the photoresists containing the polymers with sulfonamide and sulfonate moieties could be achieved by using NBA developer. Lithographic performances of photoresists with sulfonate-containing polymers (PSO) were close to those with Ref polymers and much better than those with sulfonamide-containing polymers (PSA).

9051-83, Session PS3

Development of novel protecting derivatives for chemically amplified extreme ultraviolet resist

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EUV lithography is the most favorable process for high volume manufacturing of semiconductor devices at 1X nm half-pitch and below. Many efforts have revealed that the effective proton generation and the control of the generated acid diffusion are required to improve the breakthrough of the RLS trade-off. For the development of EUV resists, the novel protecting derivatives were designed. To clarify the lithographic performance of these derivatives, we synthesized the acrylic polymers containing these derivatives as model photopolymers and exposed the resist samples based on these polymers to EUV/EB radiation. On the basis of the lithographic performances of these resist samples, we evaluated the characteristics of novel protecting derivatives upon exposure to EUV/EB radiation. We discuss the relationship between the chemical structures of these derivatives and lithographic performance.

9051-84, Session PS3

Development of antistatic film for electron-beam lithography

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We have developed antistatic film for electron beam lithography.

This time, we report about its antistatic performance and other properties.

9051-85, Session PS3

High-chi organic block copolymers for directed self-assembly

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Directed self-assembly (DSA) of block copolymers (BCP) provides a materials-based resolution enhancement method to extend the capability of optical, EUV and electron-beam lithography. Block copolymers, consisting of covalently-linked incompatible chemical blocks, phase-separates into periodic nano-scale domains of chemical contrast. Combining the self-assembled chemical contrast from block copolymer and lithography-defined guiding prepattern, DSA of block copolymers sub-divides and/or rectifies the lithography prepatterns and therefore, increase spatial frequency, reduce feature dimensions, and improve the uniformity. PS-b-PMMA has been widely used for DSA in the labs and pilot lines because it is easy to process and its morphology is well-controlled. The half pitch of PS-b-PMMA, determined by its molecular weight, volume fraction and interaction parameter, can scale down to ~ 10nm by reducing the molecular weight of the block copolymers. Further scaling down the molecular weight of PS-PMMA results in disordered phase separated domains. Therefore, a block copolymer with higher chi between two blocks to form ordered phase separated domains at lower molecular weight is highly desirable for scaling.

In this paper, we report an organic high-chi block copolymer system to extend the scaling beyond PS-b-PMMA. The phase-separated morphology and orientation of the domains were controlled by the composition of the block copolymers and underlayers. Perpendicularly oriented block copolymer domains were achieved by spin-coating of block copolymer solution on the orientation control underlayer followed by a short bake. Results on the scalability, thin film morphologies, domain orientation control, pattern transfer and directed self-assembly of this block copolymer system will be discussed.

9051-86, Session PS3

EUV resists prepared from compounds containing bismuth, tellurium, and tin

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It has been demonstrated that inorganic resist systems, such as the hafnium oxide nanoparticles developed by Inpria and Cornell, can serve as high resolution EUV photoresists that maintain moderate to good sensitivity. Here we present the synthesis and preliminary EUV sensitivities of Molecular Organometallic Resists for EUV (MORE) that contain Bismuth, Tin and Tellurium. These post transition metal nuclei have high EUV optical density (OD) so that they can utilize a high fraction of the incident photons. Additionally, compounds made from these elements exhibit reaction pathways supported by metal-centered free radicals and by the multiple oxidation states.

We will describe three technical approaches for utilizing compounds containing Bismuth, Tin and Tellurium to prepare EUV resists, for a total of nine new EUV resist platforms (Figure 1).

Approach 1: Many metal-phenyl bonds, such as a bismuth phenyl bond, are readily cleaved homolytically via light or heat. This characteristic was utilized through the incorporation of polymerizable olefins such that a free radical polymerization may be initiated by an EUV photon in the exposed regions.

Approach 2: Many metal-phenyl bonds are acid cleavable. This property was utilized by synthesizing metal phenyl oligomers that have decreased solubility as compared to their analogous monomers. These oligomers were then formulated with a PAG. When acid is generated in the exposed regions the acid cleaves the metal phenyl bond and is consumed in the reaction. This reaction is not catalytic in acid, and therefor resolution should not be limited by acid diffusion.

Approach 3: In this approach, we use oligomers at higher oxidation state and utilize carboxylate anions bound to the metal centers. We propose that the primary mechanism for photodecomposition of these compounds is decarboxylation. Compounds in this materials set have demonstrated EUV sensitivity and none linear contrast curves reminiscent of those for traditional resist systems (Figure 2).

9051-87, Session PS4

Novel spin-on metal hardmask materials for filling applications

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Hard masks are indispensable materials during pattern transfer to the desired substrates in the semiconductor manufacturing process. Primarily there are two types of hard mask materials - organic and inorganic - and they can be coated on to substrates either by a simple spin-on process or by a chemical vapor deposition (CVD) or sputtering process. Most inorganic hard masks such as SiO2, SiON, SiN, TiN are deposited using the CVD process.

Future nodes require hard masks with high etch resistance as the designs move from horizontal to vertical (3D). We have reported novel spin-on metallic hard masks (MHM) with significantly higher etch resistance than SiO2.1-2 In addition to high etch resistance, they are easy to remove using wet etch chemicals. The spin-on process offers high through put and commonly used spin tracks can be used thereby reducing overall process costs when compared with CVD.

Via-fill performance is also an important attribute of hard mask materials for these future nodes. Organic spin-on materials, both siloxane- and carbon- based, are used in filling applications of deep via or deep trench fill, such as those found in LELE double-patterning schemes. Inorganic materials deposited by either chemical vapor deposition (CVD) or atomic layer deposition (ALD) have higher resistance to oxygenated plasma than organic materials, but are hindered by their poor filling performance. Therefore, novel MHM materials having both good filling performance and higher resistance to oxygenated plasma than organic materials would be of value in some filling applications. The present paper describes specific metal oxides useful for filling applications. In addition to basic filling performance and etch resistance, other properties such as optical properties, lithography, outgas and shelf life via forced aging will be discussed.

Fig. Filling performance of AZ® MHM Sample A in the 75nm dense vias at 600nm depth.

9051-88, Session PS4

Novel silicon hard mask design for collapse margin improvemnt

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As the critical pitch and critical dimension (CD) continue to shrink, the line collapse margin has become more and more important. For the 20-nm logic node and beyond, due to the resist resolution limit, negative-tone development (NTD) has become a possible approach. Un-like positive tone development (PTD), NTD pattern is formed by removing the unexposed resist with solvent and preserving the exposed resist. The latter is made possible by making the exposed resist more polar, more hydrophilic, and less soluble to the NTD solvent. Due to the resist polarity switch in the exposure area, the polarity mismatch between the resist polymer and the Silicon hardmask (Si-HM) can sometimes cause pattern collapse.

In this paper, we introduce a new floatable polymer to the Si-HM to reduce polarity mismatch. The additive polymer contains acid-labile group for polarity switch when contacted to acid in the exposure area. Comparing to conventional Si-HM, the floatable additive approach improved the collapse margin 15%.

9051-35, Session 12

Manufacturability considerations for graphoepitaxy DSA

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Implementation of Directed Self-Assembly (DSA) as a viable lithographic technology for high volume manufacturing will require significant efforts to co-optimize the DSA process options and constraints with existing work flows. These work flows include established etch stacks, integration schemes, and design layout principles. The two main flavors of DSA, chemoepitaxy and graphoepitaxy, each have their own advantages and disadvantages. Chemoepitaxy is well suited for regular repeating patterns, but has challenges when non-periodic design elements are required. Graphoepitaxy has intrinsic benefits for design flexibility, but the guide patterns occupy valuable area.

In this paper, we characterize the process window for graphoepitaxy DSA with respect to such design considerations. We will present data showing how the process window for graphoepitaxy DSA can be influenced by the size, shape, and spacing of DSA confinement wells, which implies a trade-off between design flexibility and process stability. These experimental measurements are correlated with the results of SCFT simulations that provide insight into the mechanism of process variations. These studies not only help us to better understand DSA processing, but also enable the calibration of simulation models, which can in turn be used to generate DSA-friendly layouts. We will pay particular attention to the impact of process sensitivities on edge placement variation due to both CD and overlay contributions, line edge roughness and defectivity. Finally, we discuss the specific challenges posed by graphoepitaxy DSA from the viewpoint of a manufacturing foundry.

9051-36, Session 12

Formation of sub-7 nm feature size PS-b-P4VP block copolymer structures by solvent vapour process

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Block copolymer have already received considerable attention as a next generation lithography to overcome the limitations of conventional lithographic techniques. Diblock copolymer (DBCP) self-assembly at interfaces enables the generation of nanoscale structures in a parallel, scalable, bottom-up fashion with important applicability in the nanofabrication industry. The high Flory-Huggins parameter (? ~0.34) of PS-b-P4VP at room temperature makes it an ideal BCP system for self-assembly and template fabrication in comparison to other BCPs since the feature size can be decreased to < 5 nm values. Such high ? BCP system requires precise fine-tuning of interfacial energies achieved by surface treatment and that improves the wetting property, ordering, and minimizes defect densities. Herein, we describe the microdomain orientation of different molecular weight PS-b-P4VP BCP thin films on silicon and on various hard mask substrates induced by solvent vapour annealing. This route is scalable to a wide range of PS-b-P4VP systems allowing size variation via ? (chi) parameter engineering/ domain modification and the feature size is demonstrated as small as sub-7 nm. The effects of the casting and annealing solvents, annealing temperature and time etc. have been demonstrated in terms of ordering, pitch size and coverage of the film on substrate. The substrate is covered with sub-20 nm to sub-7 nm features with perpendicular lamellae of thickness around 25 nm. No surface treatment is required for the microphase separation of the blocks. A novel, simple and in situ hard mask technology that can be used to generate nanowire features on a substrate surface is demonstrated. The technique combines a block copolymer inclusion method that generates nanowires on substrate and which can further etch to fabricate silicon nanowires. These lamellar nanostructures can be used to design devices for high-density and high performance sensor or memory devices.

9051-37, Session 12

New materials for directed self-assembly for advanced patterning

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Directed Self-Assembly (DSA) of block copolymers is a promising advanced patterning technology at sub 10 nm technology nodes. Although DSA promises high resolution, low line edge roughness (LER), and cost benefits, a number of constrains and challenges remains for its implementation, including low defectivity, effective throughput, reliable pattern transfer, and ease of integration with complementary metal-oxide semiconductor processing. Poly(styrene-block-methyl methacrylate) (PS-PMMA) has been widely studied in DSA and applied in various applications including line/space and contact hole patterning and uniformity repair to demonstrate the potential of DSA to extend optical lithography. However, the relatively weak segregation strength of PS-PMMA limits its capability to pattern small features with low LER at low defectivity. This paper presents material and formulation solutions to overcome some of the limitations with current chemoepitaxy materials, including improved materials for PS-PMMA processes and new block copolymers with strong segregation strength (high ?) to extend chemopitaxy processing beyond the limits of PS-PMMA.

9051-38, Session 12

Orientation control of high-X block copolymers using polymeric topcoat surface treatments

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High-? block copolymers, attractive for their ability to self-assemble into sub-10 nm microdomains, typically suffer from orientation issues relative to a substrate, caused by surface energy mismatching. This effect can be partially mitigated using substrate surface treatments, however these approaches are unsuccessful for most high-? polymers. Polymeric top coat surface treatments offer a simple technique to modify the surface energy at the top interface. The present work focuses on a new methodology developed to process and evaluate top coat materials in a reproducible manner. A library of these materials can be quickly screened by this technique to determine the block copolymer wetting behavior and identify a suitable “neutral” top coat. The top coats can be deposited by spin coating and are subsequently thermally annealed to produce vertically-aligned block copolymer structures. The polymer top coats have been successfully shown to orient several high-? block copolymers possessing an inherently high etch selectivity and sub-10 nm features. The process used to evaluate the top coats has been proven to be amenable to various other polymer systems.

9051-39, Session 12

Enhanced characterization of BCP-based DSA processes using innovative CD SEM analysis

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Contact holes are amongst the most difficult structures to resolve through traditional lithographic means. As a consequence, directed self-assembly (or DSA) is gaining significant industrial interest now that a number of DSA strategies using block copolymers (BCPs) have shown some promise at generating either small, uniform, or increasingly dense contact arrays.

The positive attributes of DSA with a BCP include its resolving power as well as the fact that it is a complementary strategy that can be employed with both 193i and/or EUVL. It does, however, have some significant concerns that must be assessed and addressed before DSA is considered to be HVM-ready. These include design decomposition, pattern placement error, material supply chain maturity, integrated defect density, the exact 3D / morphological nature of the resulting patterns, and finally the metrology associated with all of these key parameters.

As shown in Figure 1, we set out to use a model grapho-epitaxial pre-pattern to evaluate the quality of a single-hole contact shrink process when using a PS-b-PMMA BCP. Our goal was to understand and optimize our DSA-based defect density.

In this paper, we will describe the materials, processing conditions, and integration components that go into the fabrication of our simplified test vehicle. We will share our analysis of BCP fingerprint patterns generated under those process conditions and cross-correlate them to the results from our hole-shrink test vehicle in order to illustrate the performance difference (including defect control, CDU, registration, and pattern placement error). This was achieved using several new Hitachi CD SEM applications which will be described.

9051-40, Session 13

Extending lithography with advanced materials *(Invited Paper)*

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Material evolution has been a key enabler of lithography nodes in the last 30 years. This presentation will explore the evolution of anti-reflective coatings and their transformation from materials that provide only reflection control to advanced multifunctional layers. It is expected that complementary processes that do not require a change in wavelength will continue to dominate the development of new devices and technology nodes. New device architecture, immersion lithography, negative-tone development, multiple patterning, and directed self-assembly have demonstrated the capabilities of extending lithography nodes beyond what anyone thought would be possible. New material advancement for future technology nodes will be proposed.

9051-41, Session 13

Spin-on organic hardmask materials for topo-patterned substrate

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Underlayer (UL) processes which include chemical vapor deposition (CVD) and spin-on underlayers play a very important role for pattern transfer from exposed photoresist to the substrate. With device shrinkage and increasing device complexity (FinFET, 3D integration, etc.), the demands on the UL increases for such properties as wiggle resistance, etch controllability, thermal resistance, planarization, and gap filling. In particular, planarization and gap fill properties on topo-patterned substrate is of increasing importance in UL materials. CVD processes generally give better wiggle performance and thermal resistance, but poorer planarization and gap filling than spin-on UL processes. In addition, CoO (Cost of Ownership) of CVD process is higher than that of a spin-on UL process. Thus spin-on process development has received increased attention recently as an attractive alternative to CVD processing.

In this work we focus on an investigation of spin-on underlayer materials which show good planarization and gap filling. Material properties and planarization/gap fill evaluation results are discussed. In addition, other properties such as wiggle resistance, etch resistance, and thermal resistance are also discussed to provide a comprehensive overview of these materials as an UL.

9051-42, Session 13

EUV lithography and etching performance enhancement by EUV sensitive Si hard mask (EUV Si-HM) for 1Xnm hp generation

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EUV lithography has been desired as the leading technology for below

Hp20nm. However, the source power, masks and resist materials still have critical issues for mass production. Especially in resist materials, RLS (Resolution, Line edge roughness and Sensitivity) trade-off is the key issue for EUV lithography. To overcome this issue, we have succeeded to develop organic type resist under layers (ULs). The ULs can reduce RLS trade-off issue for single layer process. The ULs can work as lithography performance enhancement layer, and it is used with CVD-HM for device manufacturing. On the other hand, Tri Layer process with spin on hard mask materials is another candidate process.

In applying tri-layer process, we are focusing on inorganic type under layers which mainly containing Si atoms. This Si type hard mask (Si-HM) can perform not only as the lithography performance enhancement layer for fine pitch, but also as the etching hard mask against bottom layer (spin on carbon : SOC). In this presentation, we propose our new Si-HM concepts to achieve high sensitivity, wide process window and good line edge roughness. The key point of our concept is introducing of EUV-sensitive unit in Si-HM. Our EUV-sensitive unit strongly promotes acid generation from PAG in EUV photo resist. Especially, in EUV NTD process, EUV-sensitive unit can perform as the adhesion enhancer between Si-HM and photo resist at EUV exposed area.

As this result, hp19nm L/S pattern and hp24nm C/H pattern were successfully achieved by applying the EUV sensitive Si-HM in EUV PTD process. Especially, as compared to organic UL, the EUV sensitive Si-HM showed 5~10% higher sensitivity and 10~25% wider process window (DOF and EL) with keeping ultimate resolution. Moreover this EUV-sensitive Si-HM could also enhance the ultimate resolution to Hp22nm L/S in EUV NTD process. On the other hand, from the view point of etching hard mask, around hp 20 nm L/S photo resist pattern could be transferred to SOC layer through Si-HM successfully. We will present the concepts and performances of our latest EUV sensitive Si-HM for 1X nm generation in EUV lithography.

9051-43, Session 13

Spin on lithographic resist trim process optimization and process window evaluation

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The demands imposed by shrinking design rules for sub 20 nm technology on lithographic resolution are driving many avenues of research and development in an attempt to provide a robust and affordable solution for high volume manufacturing. Currently, pitch splitting techniques, such as self-aligned double and quadruple patterning (SADP or SAQP) and litho-etch litho-etch …(LELE…), are being used to bridge the gap to next generation lithographic techniques. Cost of ownership (CoO), process window improvements and defectivity are opportunities and concerns for extensions of these approaches, such as resist sliming on sidewall-image transfer (SIT) processes like SADP or SAQP. A spin-on resist slimming approach is implemented with several line/space resists to explore process window and CoO improvements compared with dry processes. The effects of typical process conditions and incoming variability are studied using a custom design of experiments. The optimized process is then used to evaluate process window gain compared to the process of record.

9051-44, Session 13

A chemical underlayer approach to mitigate shot noise in EUV contact-hole patterning

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Shot noise is a significant issue in EUV lithography. Especially in printing small area features like contact holes, shot noise will become so severe that it largely impacts contact hole CD size variation. This brings about frequently discussed topics: LCDU (Local CD Uniformity) issue and LCDU-sensitivity tradeoff. Basically shot noise is a physical issue; it mainly depends on incident energy. This paper describes efforts to alleviate this issue through a chemical approach: special EUV Underlayer (UL) materials design.

EUV UL absorbs EUV photons and generates secondary electrons, which go back to the photoresist and react with PAG to produce acids and expose the photoresist from the “underside”. This is also called the “back exposure” effect. A novel component “Buffer” was introduced into EUV UL formulations to balance back exposure energy from UL at different incident dose positions. Measured back exposure dose from UL shows less variation (6σ/mean) compared with shot noise of resist absorbed dose. Thus summed energy variation will be suppressed, namely shot noise is reduced. Currently “back exposure” dose of EUV UL with best “Buffer” shows 1.04% deviation (6σ/mean), which is much lower than that of shot noise of resist absorbed photons. Through reported shot noise model, we calculated final shot noise after taking “back exposure” into account. Results suggest by using EUV UL with best “Buffer”, 10% sensitivity improvement and 4.3% shot noise mitigation can be achieved simultaneously.

Novel metal hardmasks (MHM) have been reported to improve photoresist sensitivity around 20~30%. Using a resist/EUV UL/MHM stack in the calculation, 30% sensitivity improvement and 13.4% shot noise suppression can be expected. This will be a very promising path to break LCDU-sensitivity tradeoff. The shot noise mitigation ratio may be not large enough, but it is quite important for current situation since in near future, large jump of EUV source power can’t be expected. Maintaining or suppressing shot noise while simultaneously improving sensitivity will bring great benefits to EUV lithography HVM process. Actual lithographic evaluations also prove new EUV UL improves 16.5% and 19% LCDU at 30nm hp contact holes compared with industry evaluated EUV UL formulation on slow and fast EUV resists respectively.

9051-45, Session 13

Anti-spacer double patterning

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With extreme UV not ready for HVM for 20nm and 14nm nodes, double patterning options, such as LELE (Litho-Etch-Litho-Etch) and SADP (Self Aligned Double Patterning), which allow extending the use of 193nm immersion lithography beyond the optical resolution limits, are being employed as options for critical layers of 20nm and 14nm nodes. The LELE option requires very stringent overlay capability of the optical exposure tool which can be difficult to achieve. The spacer scheme of SADP starts with a conformal film of material around the mandrels and then etched along the mandrel sidewalls to form the patterns with doubled frequency. SADP, while having the advantage of being a self-align process, adds a number of process steps and strict control of the mandrel profile is required.

In this paper, we will demonstrate a novel technique- ASDP (Anti-Spacer Double Patterning), which uses solely spin-on material to achieve the self-aligned double patterning. After the resist patterning, an ASDP material is spun on to create the developable spacer. Then another layer of material is coated on the wafer and processed to generate the 2nd pattern in between the 1st resist pattern. We were able to define 37.5nm half pitch pattern features using dry 193nm exposure tool with an effective k1 = 0.17. We also demonstrated the ability to define an

asymmetric pattern from a symmetric layout using this technique. In this paper we will review the capability of the process in terms of CD control, LER, and comparison to other lithography options.

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9051-46, Session 14

Optimisation of fullerene-based negative tone chemically amplified resist for extreme ultraviolet lithography

Andreas Frommhold, Dong Xu Yang, The Univ. of Birmingham (United Kingdom); Xiang Xue, Nano-C, Inc. (United States); Yasin Ekinci, Paul Scherrer Institut (Switzerland); Richard E. Palmer, Alex P. G. Robinson, The Univ. of Birmingham (United Kingdom)

While the technological advance of Next Generation Lithography (NGL) technology steadily continues, further progress is required before successful insertion in high volume manufacturing is possible. A key issue is the development of new resists suitable to achieve higher lithographic resolution with acceptable sensitivity and line edge roughness. Molecular resists have been a primary focus of interest for NGL because they promise high resolution and small line edge roughness (LER), but no suitable resist candidate has emerged yet that fulfills all of the industry's criteria. We have previously shown first extreme ultraviolet lithography (EUV) exposures for a new fullerene derivative based three-component negative tone chemically amplified resist with suitable properties close to or within the target range of the resist metrics as set out in the International Technology Roadmap for Semiconductors for 2016.

Here we present the results of our efforts to optimize the EUV lithographic performance of this fullerene derivative based resist system especially with regards to LER. Fullerene resist films were prepared by mixing the components and spin coating on silicon substrates with a custom-made carbon underlayer. Solutions have been formulated in ethyl lactate. Films were exposed by EUV interference lithography at the XIL beamline at the Paul Scherrer Institut in Villigen, Switzerland. Influences on lithographic performance that were studied include fullerene purification, crosslinker material, post application bake and post exposure bake conditions, developer and addition of quencher. Figure 1 shows the response curve of the resist for two different purification methods as well as an intermediate mixture of the two materials. For example, studying the influence of the developer it was found that when using cyclohexanone with a development time of 15s and followed by an IPA rinse, resist lines exposed on a 36 nm pitch at 20.8 mJ/cm2 caused swelling resulting in a LER value of 6.20 nm (figure 2 left). Substituting for 2-heptanone the swelling could be suppressed to give lines of the same resolution at 21.2 mJ/cm2 with an LER of 4.28 nm (figure 2 right). Figure 3 shows the latest version of the resist that went through further purification, resulting in an LER of 2.5nm at 22 nm halfpitch, and 3.2 nm at 18 nm halfpitch.

9051-47, Session 14

Patterning chemistry of HafSOx resist

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The material Hf(OH)4-2x-2y(O2)x(SO4)2y?zH2O, commonly known as HafSOx, is an aqueous-based inorganic resist that has enabled leading lithographic performance with characteristics including line-width roughness < 2 nm and resolution below 10-nm half pitch. The material can be effectively patterned via electron-beam, ArF, and EUV exposure. In this presentation, fundamental chemical processes contributing to the performance of the material will be considered. The HafSOx system is one of many new families of inorganic films from the Center for Sustainable Materials Chemistry that is deposited from solutions containing nanosized clusters. These films consistently exhibit atomically flat surfaces, high atomic densities, and minimal defects. The HafSOx system can be quite dynamic. At appropriate peroxide and sulfate concentrations, however, sufficient solution stability can be achieved for realizing reproducible patterning results. Wet-chemical methods, ICP techniques, Raman spectroscopy, small-angle X-ray scattering, and computational methods have been applied to solutions and films under these conditions to identify and characterize the molecular-level compositions and species that are present. Surprisingly, only limited amounts of peroxide, i.e., peroxide:Hf < 1:2, has been found to be bound to Hf in both the precursor solutions and the thin films. As peroxide is the radiation-sensitive ligand in the system, this low concentration sets up competitive dehydration processes that affect sensitivity limits. These dehydration processes can be active both before and after exposure as well as during development. This dehydration has been monitored and quantified via variable-temperature QCM analyses, thermally programmed desorption, and measurement of contrast curves. During development in TMAH(aq), sulfate is found to readily migrate from the films. This migration sets up an additional competitive process between condensation/dehydration and dissolution of the resist. This competition largely necessitates the use of a concentrated TMAH(aq) solutions to effectively develop the resist. Consideration of the individual steps contributing to the performance of HafSOx as a resist provides a reasonably detailed, quantitative understanding of the system that is also useful for formulating design principles and developing next-generation, improved materials.

9051-48, Session 14

Photolithographic properties of tin-oxo clusters using EUV light (13.5nm)

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It has been demonstrated that inorganic resist systems, such as the hafnium oxide nanoparticles developed by Inpria and Cornell, can serve as high resolution EUV photoresists that maintain moderate to good sensitivity. Here we present the synthesis and preliminary EUV sensitivities of Molecular Organometallic Resists for EUV (MORE) that contain Bismuth, Tin and Tellurium. These post transition metal nuclei have high EUV optical density (OD) so that they can utilize a high fraction of the incident photons. Additionally, compounds made from these elements exhibit reaction pathways supported by metal-centered free radicals and by the multiple oxidation states.

We will describe three technical approaches for utilizing compounds

containing Bismuth, Tin and Tellurium to prepare EUV resists, for a total of nine new EUV resist platforms (Figure 1).

Approach 1: Many metal-phenyl bonds, such as a bismuth phenyl bond, are readily cleaved homolytically via light or heat. This characteristic was utilized through the incorporation of polymerizable olefins such that a free radical polymerization may be initiated by an EUV photon in the exposed regions.

Approach 2: Many metal-phenyl bonds are acid cleavable. This property was utilized by synthesizing metal phenyl oligomers that have decreased solubility as compared to their analogous monomers. These oligomers were then formulated with a PAG. When acid is generated in the exposed regions, the acid cleaves the metal phenyl bond and is consumed in the reaction. This reaction is not catalytic in acid, and therefore resolution should not be limited by acid diffusion.

Approach 3: In this approach, we use oligomers at a higher oxidation state and utilize carboxylate anions bound to the metal centers. We propose that the primary mechanism for photodecomposition of these compounds is decarboxylation. Compounds in this materials set have demonstrated EUV sensitivity and non-linear contrast curves reminiscent of those for traditional resist systems (Figure 2).

9051-49, Session 14

Inhomogeneity of PAGs in resist film studied by molecular-dynamics simulations for EUV lithography

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As feature sizes on semiconductor devices continue to get smaller, resist materials are required to meet the challenging requirements for patterning sub-20 nm features, sizing dose of less than 20 mJ/cm2 and line width roughness (LWR) below 2 nm. Deficient power of Extreme ultraviolet (EUV) light source will in effect require higher sensitivity for resist materials at EUV lithography. High-sensitive resist materials suffer from the shot noise effect which deteriorates the resolution and LWR/line edge roughness (LER) of resist materials. So it is very important to minimize the LWR/LER of resist patterns.

Inhomogeneity of resist components in resist films are frequently listed as causes of LWR/LER in addition to shot noise. However there are no direct evidences of inhomogeneity. Thus, information on the inhomogeneity should be valuable to control it and obtain the lower LWR/LER and higher resolution of resist patterns.

In this paper, the inhomogeneity of resist components in resist films has been studied using molecular simulations. Molecular dynamics (MD) is a computer simulation of physical movements of molecules by numerically solving the motion equations for a molecular system interacting with MD force fields. MD may provide the atomistic and molecular views of resist inhomogeneity.

To simulate MD of the photoacid generators (PAGs), the specific force fields were defined by using the quantum mechanical calculation and were used for the MD simulations. To simulate the resist film, 3-dimensional periodic condition was used to construct the amorphous models consisting of polymers and PAGs. Evaluated polymers are phenolic polymers, methacrylic polymers and hybrid (which includes phenolic and methacrylic units) polymers, of which molecular weight ranges from 1,000 to 10,000. Evaluated PAGs are typical onium salts such as triphenylsulfonium triflate and triphenylsulfonium nonaflate and PAG composition is 20 wt % to 100 % polymer weight. MD simulations of the amorphous models were performed for several nanoseconds under the conditions of canonical ensemble (NVT) where numbers (N), volume (V) and temperature (T) are conserved and isothermal-isobaric ensemble (NPT) where N, pressure (P) and T are conserved, after minimization of total energy. The simulated results shows directly the inhomogeneity of PAGs located in resist films. PAG shows inhomogeneity of not only the localizations but also the motions of PAGs. Volume of trajectories of PAG anions varies in order of magnitude and depends upon the molecular environments surrounding PAG such as free volume in the resist films.

In the conference other inhomogeneity such as PAG cations and chemical properties of PAGs will be discussed.

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9051-50, Session 14

A platinum-fullerene complex for patterning metal containing nanostructures

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Metal containing carbon structures have attracted considerable attention due to their novel properties and potential in a wide range of applications such as catalysis, energy conversion/fuel storage, photodetectors and nanobiotechnology.1 Fullerene derivatives are one such candidate where metal atoms can be incorporated either inside the cage (endohedral fullerenes) or attached to the outside of the cage (exohedrally functionalised fullerenes). Fullerene has been found to fragment under electron beams and form an amorphous insoluble structure, and both pure C60 and fullerene derivatives have been reported as high-resolution negative tone electron beam resists.2 Thus it is of particular interest to combine metal incorporation, with the resist properties of fullerene derivatives, to create an unique patternable metal containing carbon nanostructure, and in addition modify the lithographic performance by introducing an energy absorption enhancement due to the presence of metal ions/atoms.3

Here we present a fullerene-based metal containing e-beam resist by incorporation of a platinum complex into the base material of a fullerene derivative (Figure 1(a) and 1(b)). Both the platinum containing fullerene derivative (C60-Bipy-Pt) and the control material without platinum (C60-Bipy) were dissolved in chloroform and spin-coated onto a silicon substrate. The materials were then exposed with an electron beam and developed in monochlorobenzene (MCB) or cyclohexanone. A sensitivity study showed that the incorporation of platinum significantly increased the sensitivity by a factor of 2.1 at 20kV (Figure 1(c)). Whilst the doses required for the base material are significantly in excess of industrial targets, it is clear that this non-chemically amplified system has enjoyed a significant enhancement in secondary electron generation through the incorporation of a single platinum complex in to the derivative. With 30kV electron beam exposure, dense lines with pitch size down to 32 nm were successfully resolved for C60-Bipy-Pt (Figure 2), showing very high resolution of this material. Sub-3 nm (3?) line width roughness (LWR) was achieved for the platinum containing material at all pitch sizes. ICP plasma etching was used to transfer the high-resolution resist patterns of C60-Bipy-Pt to the silicon substrate. Fine lines with 32 nm pitch size were successfully transferred into the underlying silicon, showing a high aspect ratio (Figure 3).

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9052-1, Session 1

3D optical laser lithography: No limits? *(Keynote Presentation)*

Martin Wegener, Karlsruher Institut für Technologie (Germany)

Three-dimensional (3D) direct laser writing (DLW) can be seen as the 3D counterpart of planar electron-beam lithography. 3D DLW has become a commercially available workhorse. However, it also used to be subject to certain seemingly fundamental limitations. In this review, we emphasize three aspects of recent progress.

(i) Stimulated-emission-depletion (STED) DLW is inspired by progress in optical lithography and has led to spatial resolution beyond the Abbe diffraction barrier, especially in the problematic axial direction. For example, STED-DLW has enabled 3D polarization-independent visible-frequency broadband invisibility cloaks, visible-frequency 3D complete photonic-band-gap materials, and 3D gold quadruple-helix metamaterials. (ii) By using the liquid photoresist as the immersion liquid, 3D “dip-in” DLW allows for structures with heights well beyond the working distance of the microscope lenses used. For example, this has enabled pentamode mechanical metamaterials, which can be seen as elastic solids approximating the properties of liquids. (iii) Galvo-mirror based DLW has boosted the accessible writing speeds by two orders of magnitude. For example, this has enabled the fabrication of extreme 3D auxetic dilational metamaterials that can be seen as anti-liquids. Samples with sub-micron features and, at the same time, a height of 1.6 mm have been achieved. We have recently also successfully combined aspects (i) and (ii) and, independently, aspects (ii) and (iii).

9052-2, Session 1

Going wide in the cloud: Why scalability matters in a simulation-driven world *(Keynote Presentation)*

David Pellerin, Amazon Web Services (United States)

This engaging talk will cover recent trends in cloud-based computing for high-performance technical and scientific applications. Simulations are now being run at massive scale in the cloud to solve the most vexing problems in engineering, life science, pharmaceuticals, big data analytics, and global finance. The talk will include real-world examples of scalable simulations being performance across industries, and will conclude with predictions about the future of cloud-based design and layout verification and why scalability matters for increasingly complex EDA and semiconductor production workflows.

9052-3, Session 2

The saga of sigma: influences of illumination throughout lithography generations *(Invited Paper)*

Bruce W. Smith, Rochester Institute of Technology (United States)

The role of illumination in optical lithography has been central in making lambda/5 resolution now commonplace. The tailoring of the source shape to meet increasing demands of imaging has been commercially practiced for over twenty years. Optimization of partial coherence through source shaping has however been explored for nearly a century first by Köhler and Zernike (in the 1920’s and 1930’s), followed by Hopkins, Wolf, and Offner (in the 1950’s and 1960’s) and more recently by Goodman and others (in the 1980’s and 1990’s). Today, sophisticated co-optimization of source partial coherence with the mask function (through SMO) and the lens pupil plane (through multiple domain optimization, MDO) is a critical tool used to achieve manufacturable lithography resolution at the edge of physical limits. This paper will provide a historical look into how illumination, partial coherence, and source shaping has influenced optical lithography. Aspects relative to future lithography generations at DUV and EUV wavelengths are also explored, including illumination influences to 3D effects for 1x nm device generations.

9052-4, Session 2

The impact of mask absorber profiles (M3D) and resist profiles (R3D) in immersion and EUV lithography

Jo Finders, ASML Netherlands B.V. (Netherlands)

With Critical Dimension Uniformity requirements in optical lithography getting tighter and tighter, phenomena that previously could be ignored now need a detailed understanding and control strategy. Amongst those are the effects introduced by the finite height of the mask absorber and the finite resist height. We will explain them by analyzing wafer Critical Dimension (CD) data through focus and dose and categorizing those using simple figures of merit: Best Focus difference across features, Bossung tilt and local dose sensitivity. In the first part we will study the phenomena and show a methodology and gauges to discriminate between M3D and R3D. This will enable the end-user to judge the effects, which are highly application dependent, and choose to put the effort for future nodes either on M3D or R3D or both. In the second part we will focus on the solutions:

• For M3D

o We will show experimental and simulated optimization of absorber thickness around the nominal working point to minimize M3D effects.

o We will study how variations of the nominal mask profile across field (e.g. Quartz etch depth) will affect the imaging properties, especially Image Plane Deviation.

• For R3D:

o We will study on which metrology technique can deliver the required profile information. Obviously scatterometry is a prime candidate.

o We will study how to simulate the effect of sidewall angle change through dose both for “Abby” type of simulators (e.g. Hyperlith) and for simulators to be used in computational lithography.

o We will study the interaction with the scanner (e.g. MSDz) and process (e.g. PEB), which will allow us to pinpoint parameters for a feed-back loop to influence the resist profile.

We will focus on immersion lithography but will show the extendibility of some of the work to EUV.

9052-5, Session 2

Topographic and other effects on DUV/EUV pattern fidelity

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The ability to incorporate topographic and other effects of previously patterned layers in ground rule formulation could potentially lead to

significant cost savings and shortening of time needed for technology ramp-up. The effect of topography coupled with the diminishing depth of focus (DOF) associated with design node shrinks could become a significant yield detractor. With migration of transistor architecture from planer CMOS to 3-D FINFETs, such topographic effect could potentially pose a major challenge for future EUV process even when the NA (Numerical Aperture) is significantly lower than those used in current immersion DUV processes. In this paper we review how sets of ground rules for a given layer can be modified to include imaging artifacts caused by underlying topography generated during the processing of previous layers. Initially we study standard immersion ArF processing, then we extend the methodology to evaluate the potential issues with EUV lithography in the presence of topography. For example, Fig. 1 shows effect of FIN width on a trench(contact holes) CD patterned over the FIN and it is observed that for a patterned space target of 40nm CD, FIN width less that 50nm changes the litho CD to a lower value in EUV lithography. We compare the the nature and magnitude of the topography effects of such results with DUV imaging and show how future ground rule development might need to incorporate the layout information of the previously patterned layers.

9052-6, Session 2

Next-generation multi-wavelength lithography: survey and roadmap

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Multi-color lithography holds the promise of attaining sub-10 nm half pitch geometries using near-UV to DUV optical imaging. The technique evolved from stimulated emission depletion microscopy (STED).(1) In the analogous lithography at least one wavelength activates the photoresist that another one or more deactivates. Increasing the intensity of the deactivation pattern decreases the size of activation into a sub-10 nanometer pixel to be used for direct write, projection or interference lithography. While numerous researchers(2-16) are examining this technique for 3D-imaging our research extends this to sub-10 nm semiconductor lithography using High Volume Manufacturing (HMV) tools that can be used for multi-patterning without removing the substrate from the chuck, creating Directed Self Assembly guide posts, writing imprint plates and EUV masks. Since the need for this type of imaging is immense and the current solutions poor like EUV, e-beam and multi-patterning with 193 nm we believe this technique will have a huge direct and indirect impact on the electronics industry. The technique requires the merging of physics, chemistry and optical engineering.

This technology is currently limited by the lack of availability of photoresist materials that then must be developed.

The limitations in current chemistries is because stimulated emission is not the only light-driven process that occurs when a molecule is in the first excited state, S1. Excited-state/excited-state absorption is a pathway that can compete with stimulated emission. Higher excited states typically undergo more rapid reaction or intersystem crossing (ISC), and so can lead to increased reactivity rather than the desired decreased reactivity and there is the potential for reverse-ISC or the formation of reactive intermediates with diffusion limited solvated electrons. In current resists relatively thick films needed for subsequent masking lithographic radical photoinitiators and PAGs do not have high extinction coefficients, so that they can be imaged. Consequently, these molecules tend to exhibit strong EEA at the same wavelengths that would be used to drive stimulated emission. Thus, irradiating with a second color of light tends to increase the reactivity of these molecules rather than inhibiting it. (2)

This paper reviews the need for this lithography, surveys the research to date (2-16) and looks forward to what it will take to implement it into HVM. We will focus on possible viable physical chemical pathways (2) and will show up-to-date results from our ongoing work. We will also describe the tools needed to explore this technology such as transient absorption and luminescence spectroscopy and, specifically, the interference lithography resist development apparatus we've assembled at the University of New Mexico to provide resist screening and the apparatus we are using at the University of Maryland to explore direct write.

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9052-7, Session 3

Advanced 3D-modeling to improve best-focus shift detection and process control

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The objective of this paper is to extend the ability of a more stable control of the best-focus shift to further improve the overall process control of the 28nm Metal layer. A method to better control complex 2D structures for this node will be described. Challenges are coming from the fact that the structures that limit the process window are mainly of 2D nature and they are difficult to monitor. Within the framework of this study the emphasis is on how to predict these process-window-limiting structures upfront, to identify root causes and to determine easier monitoring solutions to enhance the process control.

To address those challenges, the first step is the construction of a reliable Mask-3D and Resist-3D model. Advanced 3D-modeling allows for better prediction of process variation upfront and to highlight critical structures impacted by best focus shifts, which are difficult to nearly impossible to be detected by usage of the current thin-mask model.

The best-focus shift detection will be discussed throughout the study. It relies on the application of the created model to determine those structures that are most sensitive to focus shifts. Furthermore, a

discussion on the correlation between results on 1D and 2D structures will be given, which is based on detected features with advanced models, and it includes an analysis on experimental measurement data. The final discussion also contains an intra-field analysis.

9052-8, Session 3

Study of lens heating behavior and thick mask effects with a computational method

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As the technology node shrinks, new challenges on lithography have been brought by not only the tight design rule but also the new techniques that enable the patterning. Best focus shifts (BFshifts) induced by thick mask effects, for example, cannot be ignored anymore due to the small feature size on the photomask. At the same time, the use of bright field mask on contact layers is appreciated with good image quality; while the resulted high reticle transmission along with more localized source energy distribution make it suffer from pronounced lens heating effects in many cases. While thick mask effects and lens heating create different problems on the image quality, they both cause certain phase errors on the wavefront, from where we can study their behavior and make necessary correction strategies.

Although lens heating and thick mask effects can be generalized in terms of the resulted wavefront errors, in principle they are case-specific. Variables such as the illumination source, mask tone, pattern geometry, etc. are all closely related to the phase error of the wavefront, and therefore influence the wafer CD. In this paper, we will examine the lens heating behavior and thick mask effects (i.e., M3D) in different conditions defined by various variable setups.

For the former, it is known that lens heating is a function of source shape, mask spectrum, reticle transmission, exposure dose, field size, etc. The amount of aberrations, as well as the resulted CD variations and displacement errors shall have their own signatures. Unlike the random error brought by process variations, the heating effect leads to a systematic CD offset, which could be considerably large from our experiment. Thus we found it necessary to study the lens heating induced aberration more thoroughly by extending our scope to different cases, with respect to mask tone, illumination, device, etc. For example, asymmetric strong off-axis illuminations heat the lens locally and unevenly. Thus larger aberrations are expected when compared with symmetric sources. Also, memory cell uses more regular design, mostly with a single pitch. Its mask spectrum usually features clear diffraction orders. On the contrary, random logic tends to scatter its diffraction orders on the whole pupil area with a distinctive zero's order. Due to such device-wise diffraction-order signatures, we assume that their responds to the heating shall differ.

As for the latter, the thick mask induced best focus shifts under different mask tones and mask types shall vary. We will examine the BFshift signatures with respect to dark tone, bright tone, PSM and binary mask. Also, it would be of interest to check the relationship of these two effects in a certain case, e.g., bright tone and dark tone masks.

9052-9, Session 3

Scanner performance predictor and optimizer in further low-k1 lithography

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Extreme low-k1 lithography has been realized by a combination of imaging technology, which includes resolution enhancement technique and source and mask technology, and process technology such as multiple patterning and directed self-assembly. Those imaging technologies have been available for some time, multiple patterning is coming into wide use, and directed self-assembly may be a practical solution for 20nm generation and beyond. In any case, the amount of allowable lithography error is still proportional to the final pattern size, such as 20nm or below. We have developed variety of application software coordinating on the various imaging technology and process technology in conjunction with powerful scanner tuning knobs to meet such tight requirements.

Until now, calculation of allowable printing errors has been based on building up an error budget for each component, such as critical dimension uniformity (CDU), optical proximity effect error, overlay error or line edge roughness. Now, at such small feature sizes, the mathematical approximations for such error budgets, e.g. a root sum square of Gaussian errors, is probably not accurate enough. Additionally, single-component error budgets fail to account for cross-coupling of different errors. Therefore, edge placement error (EPE) will be a critical metric to explain lithography performance. Interference effect between various error components and compensation mechanism can be taken into account in the EPE budget.

In order to achieve the EPE criteria for 20nm and beyond, in addition to improvement of fundamental scanner performance such as lens aberration, overlay performance, and focus control accuracy, the following items need to be established.

1. Effective error compensation mechanisms using various scanner tuning knobs

2. Computational based scanner lithography performance prediction

3. Robust process design based on predicted scanner performance.

4. Feedback scanner control from metrology tools.

Therefore, the application software should have capability to cover these four items. In addition to that, speed and user friendly interface to be realized.

One example of these applications is lens thermal aberration prediction and feedback to robust process design methods such as source mask optimization. In this flow we can modulate mask pattern and/or illumination source shape to minimize the amount of thermal aberration and/or impact of thermal aberration on lithographic performance.

In this paper, we discuss how we realize this and other technologies with the application tools for imaging system setup on the scanner. The setup process includes freeform pupilgram generation, pupilgram adjustment, thermal aberration control, CDU and overlay control in conjunction with metrology tools.

9052-10, Session 3

Imaging control functions of optical scanners

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Until now, the calculation of allowable printing errors has consisted of building up an error budget for each component, such as critical dimension uniformity (CDU) optical proximity effect (OPE) error, overlay error or line edge roughness. Now, at such small feature sizes, the mathematical approximations for such error budgets, e.g. a root sum square of Gaussian errors, is probably not accurate enough. Additionally, single-component error budgets fail to account for any potential cross-coupling of different errors. Therefore, edge placement error (EPE) has become a critical metric to explain lithography performance, since it is affected by all of the existing imaging error components. Also, interference effects between various error components and compensation mechanisms can be taken into account in the EPE budget.

To achieve control of the EPE components, various scanner parameters (such as aberration, distortion, focus, etc.) need to be controlled with minimal side effects between themselves. The Nikon scanner system has integrated various new and existing subsystems towards the explicit

goal of controlling, compensating, and reducing overall EPE error. This is achieved as follows:

1) Advanced compensation of thermal lens effects

One of these subsystems is a reticle bending system used to compensate for the thermal focus error across the exposure slit without causing astigmatism error. This is used in tandem with other adjustment mechanisms in a scanner, such as standard lens control system and deformable mirror, to minimize residual aberration error due to heating. This entire team of adjustment mechanisms is controlled by the Lens Control (LC) unit in our scanner system.

2) Implementation of Custom Lens Control.

Even after applying an aberration correction dictated by the LC, some non-correctable residual aberration error may exist. In order to maintain reasonable process margin, the Custom-LC function applies additional counter-aberrations in order to minimize the side effect due to the residual aberrations. This compensation may include dynamic adjustments made to dose and focus, potentially including dynamic through-scan adjustment.

3) Dynamic (through-scan) Distortion Adjustment.

The Dynamic Lens Control System has been used to minimize high order components of shot distortion. For example, the high order components of distortion induced by the thermal reticle deformation, which can be a dominant factor of the standard overlay performance, are mitigated with this compensation.

By using these technologies, the amount of thermal impact to EPE can be minimized. The actual effects and results of each function are evaluated on a Nikon scanner system, and the results will be reported.

9052-11, Session 3

Experimental validation of rigorous, 3D profile models for negative-tone develop resists

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The extension of 193nm immersion lithography to the 14nm node and beyond directly encounters a significant reduction in image quality. One of the consequences is that the resist profile varies noticeably, impacting the already limited process window. Resist top-loss, top-rounding, T-top and footing all play vital roles in the subsequent etch process. Therefore, a reliable rigorous model with the capability to correctly predict resist 3D (R3D) profiles is acquiring higher importance. In this paper, we will present a calibrated rigorous model of a negative-tone develop resist. Resist profiles can be well simulated through focus and dose, and good matches to the experimental wafer data are validated. Such a model can not only provide early investigation of insights into process limitation and optimization, but can also complement existing OPC models to become R3D-aware in process development.

9052-12, Session 3

Wafer sub-layer impact in OPC/ORC models for advanced node implant layers

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From 28 nm technology node and below optical proximity correction (OPC) needs to take into account light scattering effects from prior layers when bottom anti-reflective coating (BARC) is not used, which is typical for implant layers. These effects are complex, especially when multiple sub layers have to be considered: for instance active and poly structures need to be accounted for.

A new model form has been developed to address this wafer topography during model calibration called the wafer 3D+ or W3D+ model. This model can then be used in verification (using Tachyon LMC) and during model based OPC to increase the accuracy of mask correction and verification. This paper discusses an exploration of this new model results using extended wafer measurements (including SEM). Current results show good accuracy on various representative structures.

9052-13, Session 4

Optical lithography: Enabling grey scale and binary microoptics for applications in advanced manufacturing, life sciences, defense, and communication *(Invited Paper)*

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No Abstract Available

9052-14, Session 4

193nm immersion lithography for high-performance silicon photonic circuits *(Invited Paper)*

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Large-scale photonics integration has been proposed for many years to support the ever increasing requirements for long and short distance communications as well as package-to-package interconnects. Amongst the various technology options, silicon photonics has imposed itself as a promising candidate, relying on CMOS fabrication processes. While silicon photonics can share the technology platform developed for advanced CMOS devices it has specific dimension control requirements. Though the device dimensions are in the order of the wavelength of light used, the tolerance allowed can be less than 1% for certain devices. Achieving this is a challenging task which requires advanced patterning techniques along with process control. Another challenge is identifying an overlapping process window for diverse pattern densities and orientations on a single layer.

In this paper, we present key technology challenges faced when using optical lithography for silicon photonics and advantages of using the 193nm immersion lithography system. We report successful demonstration of a modified 28nm-STI-like patterning platform for silicon photonics in 300mm Silicon-On-Insulator wafer technology. By careful process design, within wafer CD variation (1?) of <1% is achieved for both isolated (waveguides) and dense (grating) patterns in silicon. In addition to dimensional control, low sidewall roughness is a crucial to achieve low scattering loss in the waveguides. With this platform, optical propagation loss as low as ~0.7 dB/cm is achieved for high-confinement single mode waveguides (450x220 nm). This is an improvement of >20% from the best propagation loss reported for this cross-section fabricated using e-beam lithography. By using a single-mode low-confinement waveguide geometry the loss is further reduced to ~0.12 dB/cm. Secondly, we expect to observe improvement in within-device phase error in wavelength selective devices, a critical parameter which is

a direct measure of line-width uniformity improvement due to the 193nm immersion system. In addition to these superior device performances, the platform opens scenarios for designing new device concepts using sub-wavelength features. By taking advantage of this, we demonstrate a cost-effective robust single-etch sub-wavelength structure based fiber-chip coupler with a coupling efficiency of 40% and high-quality (1.1x105) factor wavelength filters. These demonstrations on the 193nm immersion lithography show superior performance both in terms of dimensional uniformity and device functionality compared to 248nm- or standard 193nm-based high-volume manufacture platform. Furthermore, using the wafer and patterning technology similar to advanced CMOS technology brings silicon photonics closer toward an integrated optical interconnect.

9052-15, Session 4

Lithographic process window optimization for mask aligner proximity lithography

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Process window optimization is introduced for mask aligner proximity lithography. In the past, source variation and the lack of simulation tools did not allow to use process windows for optimizing proximity lithography. Recently, telecentric illumination, source shaping ability and full 3D simulation became available for mask aligners equipped with MO Exposure Optics. Now accurate simulation and predictive process modeling allow optimizing critical lithography steps without experiments. We present results from simulation and experiment. With more than 5'000 mask aligners installed in research and industry, the proposed method will have significant impact on yield improvement and cost saving.

9052-16, Session 4

The solution to enhance i-line stepper application by improving mix and match process overlay accuracy

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Today, while semiconductor devices have adopted various processes, it is needed that exposure equipments can deal with these processes. For example, CF (Color Filter) process and ML (Micro Lens) process are applied for image sensors. In CF process, i-line exposure equipments are usually used because of sensitivity of color resists which compose color filters.

The pixel size of image sensors has been drastically shrunk because of the downsizing of mobile devices. Due to the reduction in pixel size, some technical challenges have arisen in lithography process.

One of the technical challenges is wafer distortion in BSI (Back Side Illumination) process. While BSI process has almost become the main technique in order to improve the sensitivity of sensors, wafer distortion caused by bonding and thinning in BSI process has become a major technical challenge. To tackle with this challenge, we have proposed two unique solutions: EAGA (Extended Advanced Global Alignment) and SSC (Shot Shape Compensator).

EAGA is an alignment function which can measure shapes and positions of all shots on wafers. By measuring shot shapes which are deformed by wafer distortion, we can get parameters which are necessary for shot shape compensation.

SSC is an exposure function which can control X-Y magnification difference and skew shape of projection lens to adjust exposure shot shapes to the shot shapes on distorted wafers. To realize SSC system for i-line stepper, new compensate mechanism called two-dimensional Alvarez is adopted.

These new lithographic techniques, EAGA and SSC, can reduce overlay residual drastically. For example, it is estimated that under 40nm residual can be achieved by using this solution while over 100nm residual by conventional system. This solution can realise the lithography to boost yield of BSI image sensors with high pixel density.

Another technical challenge in lithography process is to improve alignment accuracy. In BSI process, conventional alignment system would deteriorate alignment accuracy since BSI process requires an alignment system which can detect alignment marks located on the back side of thinly grinded Si wafers. To enhance alignment accuracy, we have offered a new alignment system with infrared light. Owing to the high transmittance of infrared light to Si, the new alignment system with infrared light can improve alignment accuracy, which has possibilities to simplify BSI process.

In addition, the productivity is also one of the technical challenges. It is deteriorated by high exposure dose resulted from the inhibition of polymerization by oxygen in color resist. To address this challenge, we have provided a low oxygen exposure system. Exposure dose can be reduced in low oxygen environment, which can largely contribute to the productivity improvement of image sensors.

Above mentioned lithographic solutions to technical challenges are explained in detail, and some exposure results applied those solutions are also presented, mainly on the application for image sensor.

9052-17, Session 4

Study on built-in lens mask lithography

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Cost effective micro lithography is demanded for fine micro devices. However, the resolution of conventional proximity exposure is not sufficient below several micron feature size under deep depth of focus. On the other hand, reduction projection system is enough resolution but the cost of the tool is too much high compared with proximity exposure tools.

To solve the requirement, we newly propose novel optical lithography using built-in lens mask to enhance resolution and depth of focus in conventional proximity exposure system. The built-in lens mask consists of additional patterns with multi-level phase compensation structures to realize built-in diffraction micro lens on the mask plate. The exposure light is diffracted by the additional slit patterns having modified phase transcription. As a result, focused optical image is obtained on the focus plate without conventional optical lens system of the tools.

To verify the effects, the optical performance is simulated by numerical analysis and the mask structure is designed. The computational works predicts that the resolution will be enhanced by almost 3 times compared with the conventional proximity lithography. To confirm the performance of the built-in lens mask, experimental study is carried out using conventional proximity exposure tool by i-line source through newly proposed built-in lens mask. 2 micron line pattern under 50 micron focus depth is successfully transferred on resist. It is confirmed that the built-in lens mask lithography successfully enhances resolution and depth of focus. In addition, .the depth of focus for each pattern is designed individually.

We believe that the built-in lens mask lithography is promising for cost effective micron and / or submicron lithography system for micro structured devices. We believe that the built-in lens mask lithography is promising for cost effective micron and / or submicron lithography system for micro structured devices. Also, it is expected to have equivalent performance compared with reduction projection lithography.

9052-54, Session PS1

Estimation of 1D proximity budget impacts due to light source for 40nm half-pitch node and next advanced node

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The laser effect to the proximity error is well known in many previous studies and papers. With continued IC design shrink to half pitch of 40nm, the proximity budget control is more and more important. The goal of this paper is to describe the laser spectral bandwidth and wavelength stability contributions to the proximity budget by considering general line/space and trench pattern design. We model the photolithography response using Panoramic Technology HyperLith simulation over a range of laser bandwidth and wavelength stability conditions to quantify the long term and short term stability contributions on wafer-to-wafer, field-to-field and intra-field proximity variation. Finally, we determine the requirements for current system performance to meet patterning requirements and minimize the laser contribution on proximity within a half-range of 1.5nm proximity budget. This paper also discusses how the wafer lithography drivers are enabled by ArFi light source technologies.

9052-55, Session PS1

In-situ aberration measurement method using a phase-shift ring mask

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An in situ aberration measurement method using a phase-shift ring mask is proposed for lithographic projection lenses. A two dimensional (2D) phase-shift ring, as shown in Figure 1, is designed as the measurement mask. A linear model between the aerial-image intensity distribution and the aberrations is built by principal component analysis and multivariate linear regression analyses. Compared with AMAI-PCA method [1], in which a binary mark and aerial images at the through focus plane are used for aberration extraction, the aerial images of the phase-shift ring contain more information. This provides the possibility to eliminate the crosstalk between different kinds of aberrations. Therefore, the accuracy of aberration measurement is improved. Simulations (Figure 2) with the lithography simulator Dr.LiTHO show that the accuracy is improved by 15% and 5 more Zernike polynomials can be measured compared with AMAI-PCA. Moreover, the speed of aberration measurement is improved because less aerial images are required using the new 2D mask.

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9052-56, Session PS1

Design for feature size reduction and depth of focus improvement of optical lithography

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The lithography requirements for reducing feature size and improving depth of focus has been given much attention. Reducing exposure wavelength and increasing numerical aperture (NA) is a direct method to reduce the feature size, but depth of focus (DOF) will decrease sharply. Recently, deep ultraviolet lithography (DUVL) and extreme ultraviolet lithography (EUVL) are introduced to conflict the contradictions. However, it is very difficult in optical element manufacture and coating film fabrication under deep or extreme ultraviolet wavelength. This is the result that fabrication accuracy in such wavelength could not be realized easily. On the other hand, an inevitable problem is that the diffraction nature of light prevents us from achieving sub-diffraction or nanometer resolution in photo-lithography. In this paper, we propose a novel approach to reduce feature size and improve depth of focus simultaneously based on the stimulated emission depletion (STED) technology, which could be performed in visible wavelength. As we know, STED was theoretically described in 1994, and then became widely used in microscope for resolution enhancement. To our knowledge, scientists have made a great breakthrough in resolution enhancement and the resolution reach the new record of 5.8nm. It is a fantastic idea that some pioneering scientists transplant the concepts of STED to develop a novel lithography system with visible light wavelength. Some significative works have been published. As used in lithography machine, DOF is a crucial parameter of lithography system. A common method to extend DOF is realized by inserting a binary diffractive optical element (BDOE) in front of high NA objective lens under radial polarization illumination. However, increase of feature size is always unavoidable. Axicon is a favorable optical element for achieving long non-diffractive beam. Here we take use of the phase distribution of axicon as a phase modulation. Double annular shaped radially polarized beam is utilized as photo-initiation beam in STED technology, while the double annular shaped azimuthally polarized beam is performed as photo-inhibition beams, which inhibits photo-polymerization of the photo resisit. Both of the beams will experience phase and amplitude modulation before combination and then projected to the sample with same objective lens. After focusing by a high numerical aperture objective lens, two beams will impinge on the photoresist with the process that a STED microscope scanning on a sample. Based on the vector diffraction theory, the focal spot from these two beams is investigated in details. Simulation results show that the proposed method can achieve 10? DOF and the horizontal size of 0.34?, which beyond the diffraction limit when objective lens with NA=0.95 is introduced. The spot can always be focused on the photoresist although the photoresist is not very smooth under the condition of high motion due to the enough DOF. This work can find applications in three dimensional lithography and nano-fabrication.

9052-57, Session PS1

A defocus measurement method for an in-situ aberration measurement method using a phase-shift ring mask

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An in situ aberration measurement method using a two dimensional (2D) phase-shift ring mask has been proposed for lithographic projection lenses, which is more accurate and faster than AMAI-PCA method [1]. The defocus of the aerial image of the 2D mask is the main source of the measurement error of this method. In this paper, the impact of the aerial-image defocus on the aberration measurement accuracy of this method is analyzed. A measurement method for defocus is proposed, in which the residue of the principle component analysis process is used as the criteria. The flowchart of the method is shown in Figure 1, where F means a defocus position of the aerial image. After the defocus is accurately measured, the most suitable linear model, which plays a very important role in the aberration measurement method, can be determined. Simulations with the lithography simulator Dr.LiTHO show that the accuracy of the defocus measurement method is about 1nm. The aberration measurement method can detect 12 terms of Zernike coefficients (Z5~Z16) with maximum error of 1m?, when the suitable linear model is used (Figure 2).

References

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9052-58, Session PS1

Alternative lithographic methods for variable aspect ratio vias

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The foundation of the economics of the semiconductor industry has historically been driven by scaling. Device size reduction is enabled by increased pattern density, enhancing functionality and effectively reducing cost per chip. Aggressive reductions in memory cell size have resulted in systems with diminishing area between parallel bit/word lines. This affords an even greater challenge in the patterning of contact level features that are inherently difficult to resolve because of their relatively small area and three dimensional image. To accommodate these trends the semiconductor industry has shifted toward the implementation of elliptical contact features. This empowers designers to maximize the use of free space between bit/word lines and gate stacks while preserving contact area; effectively reducing the minor via axis dimension. It is therefore critical to provide methods that enhance the resolving capacity of varying aspect ratio vias for implementation in electronic design systems. Simulation data of non-traditional lithography techniques such as optical vortex masks and intentionally induced aberrations will be presented as means to augment ellipticity. It is shown that illumination parameters and source-mask optimization methods can be employed to maximize process window while manipulating aspect ratio through feature density.

9052-59, Session PS1

Process window enhancement using advanced RET techniques for 20nm contact layer

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In the 20nm tech node, it is challenging for simple resolution enhancements techniques (RET) to achieve sufficient process margin due to the significant coupling effect from dense features. Advanced computational lithography techniques including Source Mask Optimization (SMO), thick mask model (M3D), Model Based Sub Resolution Assisting Feature (MBSRAF) and Process Window Solver (PW Solver) are required for mask correction. The goal is to have an OPC solution that not only converges at nominal condition, but also performs well at process window condition. In many cases, it is observed that with small change in OPC parameter, the mask correction could have big change therefore making OPC tuning challenging. On top of this, different patterns have different optimum source map and different optimum OPC solution path. The need for finding a globally optimal OPC solution becomes important.

In this work, we are introducing a holistic solution including source and mask optimization (SMO), MBSRAF, conventional OPC and Co-Optimization OPC, in which every technique plays a unique role in process window enhancement: SMO optimizes the source and find the best source solution for all critical patterns; MO (from SMO) provides entitlement performance with the current source on critical patterns; Co-Optimization provides the optimized location for scattering bar; MBSRAF and OPC adopt all the information from advanced solvers and perform as an optimized production solution.

With this approach, we will demonstrate that with holistic RET solution process window can be significantly improved for 20nm contact layers.

9052-60, Session PS1

The mitigation of mask roughness via pupil plane filtering for interference-like lithography

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Line edge roughness (LER) present on the photoresist patterns is seen as one of the most important challenges for advanced technology nodes. While the stochastic resist kinetics and the processing remain to be the dominant contributors, roughness originating from the mask is gaining more attention for imaging conditions with large mask error enhancement factor (MEEF). The roughness transferred from the mask to the wafer depends on factors such as the illumination wavelength, numerical aperture of the system, and the source shape. The contribution is usually in the low frequency range, which is particularly detrimental to the electrical device performance. This paper investigates the mitigating effect of pupil plane filtering on mask roughness transfer for interference-like lithography conditions. The filtering technique requires small partial coherence for the illumination source and can be in either transmission or in phase. The latter utilizes an orientation dependent focus shift, thereby degrading the printing of features in one direction without significantly impacting the printing in its orthogonal direction. Experiments were performed using a commercial 193 nm scanner equipped with a wavefront manipulator and a mask that had vertical line space patterns with edge roughness programmed over various amplitudes. Experimental results showed significant mitigation when an optimized phase filter was inserted at the pupil plane. The focus dependency of the mitigation is also shown by simulations.

9052-61, Session PS2

Understanding the critical challenges of self-aligned octuple patterning

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Self-aligned multiple patterning (SAMP) technology has been an active research topic recently, however, the industry-wide interest to extend it to the self-aligned octuple patterning (SAOP) scheme seems to be limited. Apparently, the process complexity (and cycle time) and cost issues are the major barriers to its large-scale implementation. On the other hand, our understanding of its detailed process characteristics, lithographic performance, and layout issues is still on the very early stage of technology development. In this paper, we shall present a detailed study on SAOP process flow and tone, cost structure, mask strategy, and layout decomposition/synthesis. This will help our industry to understand the potential challenges of this technique and make a wise decision when picking up the right patterning solution for the future technology nodes.

A schematic illumination of a 2-mask negative-tone SAOP (nSAOP, mainly for back-end applications) processes is shown in Fig. 1, wherein three iterative spacer steps can increase the pattern density by a factor of eight. A disadvantageous signature of this SAOP process is the repeated pattern transfer steps (to transfer spacer patterns to the underneath layer to avoid the asymmetric spacer profile). Also, a tight control of CD uniformity of various types of features is required from the beginning of the process to ensure a good multiple-pool CD performance in the following steps. Therefore, one important part of our paper will be focused on analyzing the multi-modality of CD populations and

identifying those bottleneck features.

The final patterns of an nSAOP process consist of four groups: (partially trimmed) mandrel, gap space, first spacer and second spacer. According to the dimensional characteristics of various types of features, a 2-mask layout decomposition algorithm is developed and shown in Fig. 2. To increase the 2-D design freedom, 3-mask SAOP layout decomposition is also discussed in our paper. An additional mask will be introduced to form auxiliary patterns overlapping the first spacers after the original mandrels are removed (or overlapping the second spacers after the first spacers are removed). The critical questions to be answered include what is the best mask strategy (e.g., the mask number) and when/how to introduce the multiple mask steps in order to achieve the maximum 2-D pattern flexibility, etc.

9052-62, Session PS2

An edge-placement yield model for self-aligned multiple patterning

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In logic device manufacturing, self-aligned multiple patterning (SAMP) can be used to generate the grating structures, while several 193i (or one EUV) cut processes help to form the desired fin/gate structures. In our previous paper [2], an overlay yield model was developed by considering the misalignment events only. In this paper, a generalized edge-placement yield model taking the effects of cut-hole CD and grating-line CD variations into account will be developed.

A schematic description of the lines affected by a misalignment (X), cut-hole CD variation (Y), the A-B line CD variations (Z1) and the line C CD variations (Z2) in a cut process is shown in Fig. 1. The Gaussian probability density functions of X, Y, Z1 and Z2 are assumed. Here we also assume CD variations of all lines obey the same Gaussian distribution. Since the edge-placement errors can be tightly controlled such that only two edge lines are affected when an error event happens. One is the edge line to be cut and the other is the edge line right next to the cut hole. Although the edge-placement error is a random event (e.g., its direction can be either up or down), only one direction needs to be considered (e.g., downward in Fig. 1) if they are symmetric. Naturally, we assume X , Y, Z1 and Z2 are independent such that their joint probability density function can be readily ontained.

Here POF(x,y,z1, z2) is the probability of failure as a function of misalignment x, cut-hole CD variation y, the A-B line CD variation z1 and the line C CD variation z2. The relation between POF and the cut-hole misalignment/CD is shown in Fig. 2(a) wherein only the horizontal misalignment and CD is considered. Figs. 2(b) and 2(c) depict the POF curves for separate lines (i.e., A-B or C). However, the yield of the whole cut process is determined not just by one affected line. Moreover, POF functions of the two affected lines are not independent variables. Therefore, a joint POF function must be constructed by examining the combined physical impact of a misalignment event and CD variations on both affected lines (see Fig. 3). In this paper, we shall calculate the edge-placement yields of SRAM fin and gate patterning process. The yields of 4-mask 193i cut process and 1-mask EUV cut process will also be compared.

9052-63, Session PS2

Dual photoresist complimentary lithography technique produces sub-micro patterns on sapphire substrates

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The dual photoresist complimentary lithographic (DPCL) technique combined with the inductive-coupled-plasma with reactive-ion-etching (ICP-RIE) treatment has great potential applications to create the patterns on the variety of hard and brittle substrate materials, such as sapphire, quartz, SiC and LiNbO3 due to the technique uniqueness. In this paper, we used this DPCL technique followed by the ICP-RIE treatments to obtain the sub-micron patterns etched on the entire surface of commercial available sapphire substrates of 2 and 4-inch diameter. The minimum diameter of the etched pits and the width of the trench was about 500 nm after the ICP-RIE treatments.

An inorganic photoresist of GeSbSnOx (GSSO) composition was coated on an organic photoresist to define the patterns recorded by direct laser writing. The pattern features could be either the continuous trench or the isolated pits dependent on the pattern designer. GSSO is an innovative inorganic photoresist material and its properties are not well-known. After deep studies, the GSSO is found to have strong resistance to be etched under the O2 plasma atmosphere during ICP-RIE but is easily to be etched under the plasma atmosphere containing the chloride. However, the organic photoresist has the opposite etching characteristics when it encounters the same atmosphere plasmas. We take advantage of complimentary etching characteristics to adopt both photoresists with the proper operational procedure in etching sequence to generate the designed patterns on sapphire surface. We report the physical and chemical characteristics change during the processing procedure.

The GSSO film on the organic photoresist was prepared by reactive sputtering of 3-element metal target with O2. The different sputtering conditions affected the microstructure of the sputtered film, which exhibited different developing rate with the developer. We are studying the relation between the microstructure and process conditions to find the working window and to optimize the photoresist performance. The instruments, including differential scanning calorimetry, thermal gravimetric analysis, X-ray diffractometer, X-ray photoelectron spectroscopy and field emission scanning electron microscopy, were applied to measure the thermal property, crystallinity, electron affinity and surface morphology situation of the oxide photoresist and entire photoresist structure. We also accomplished a simulation code to calculate the temperature profile in a DPCL structure at applied laser pulses when the optical constant and thickness of each layer material were known. With the aid of simulation codes, we can acquire more inside and transition knowledge on the material behaviors treated by laser. It can help to better understand the interaction between the laser and photoresist material.

9052-65, Session PS3

TCO less dye sensitized solar cell lithographic methods for injecting the electrolyte

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Typical Dye-sensitized solar cells(DSSC) are composed of mesoporous TiO2 nanocrystals electrode on transparent fluorine-doped tin oxide(FTO) substrate, sensitizers on the TiO2 nanocrystals, platinum(Pt) on the FTO substrate as a counter-electrode, and iodine/iodide electrolytes between the two transparent conducting oxide(TCO) substrate. But two transparent conductive oxide(TCO) substrates are estimated to be about 60[%] of the total cost of the DSSCs. Currently novel TCO-less structures have been investigated in order to reduce the cost. We suggested a TCO-less DSSCs which has titanium layer electrodes. Titanium layer electrodes are formed by electron-beam evaporation method. And we proposed the formation of hole for injecting the electrolyte of DSSC by using lithographic method. The sizes of holes are 1um, 2um, and the intervals of holes are 1um, 2um. Finally, we prepared the 0.45 cm2 DSSC device and analytical instruments such as electrochemical impedance spectroscopy, scanning electron microscope were used to evaluate the TCO-less DSSCs.

9052-66, Session PS3

UV-LED exposure system for low-cost photolithography

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Since the early 1960s optical lithography has played a central role in the advancement of semiconductor process technologies which in turn has fueled the development of integrated circuits (ICs) and more recently micro/nano-electro-mechanical systems (M/NEMS). However, the high cost of lithography tools and associated infrastructure requirements, limits the access to this critical technology only to state-of-the-art laboratories. As a result, widespread dissemination of lithography technology beyond microelectronics towards other engineering disciplines and fundamental sciences, and possible applications therein are inherently limited due to the cost factor. To address this problem, we have developed a low-cost, portable, light-emitting diode (LED)-based UV exposure system which makes photolithography possible even in a basic laboratory.

Our prototype lithography system employs only off-the shelf components including UV-LEDs (380 nm), microcontroller, digital-to-analog converter (DAC) and power transistors. It is also equipped with a digital user interface (LCD and keypad) and permits accurate electronic control on the exposure time and power; which were not possible in earlier demonstrations of UV-LED lithography with manual control of exposure time and single exposure power. The lithography system developed in this work offers flexibility on adjusting both control knobs i.e. exposure duration (0.5-60s) and power (1-30mW/cm2); therefore, the exposure dose can be properly varied depending on process requirements. We verified the functionality of the system by performing large area patterning of both thin (~1μm) and thick (~20μm) i-line resists on 4-inch bare silicon wafers. Successful pattern transfers (lithography and etch) were also achieved on wafers with silicon oxide. The minimum feature size attained was ~10μm using a transparency mask, which may be further reduced by optimizing process conditions and using a high resolution quartz photomask.

Compared to traditional contact lithography tool, our UV-LED lithography system is significantly cheaper (less than $500), simple to construct using readily available components, does not require complex infrastructure to operate and offers full control on exposure parameters. The system is portable, compact and can be set-up in any basic laboratory. Such reduction in system cost and complexity renders UV-LED lithography as a perfect candidate for microlithography with large process windows typically suitable for MEMS and microfluidics applications.

9052-67, Session PS3

Micro-optics: Enabling technology for illumination shaping in optical lithography

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After wavelength shrinkage to 193nm and optimizing projection lenses to the highest level, shaping the illumination light, also referred as pupil shaping, was the next powerful measure to further reduce half-pitch in optical lithography. Starting from simple annular (ring) and off-axis illumination, the optical designers soon realized that a more sophisticated light source shaping is required to minimize residual aberrations and diffraction effects. Shaping the light source allows to optimize the optical path from reticle to wafer to reduce or balance aberrations and diffraction effects. Shaping the light source also allows to increase the process window and to stabilize critical lithography steps.

First attempts to use micro-optics for illumination light shaping in projection lithography started in the early 1990s. Wafer-based technology became available for manufacturing of planar micro-optics in UV-transparent Fused Silica. The development of micro-optical components had been promoted in the 1990s by government funded research projects in Germany, Switzerland, the US and Japan. Optical designers from lithography companies then integrated both, refractive and diffractive micro-optical components in their illumination systems to further improve projection lithography.

Diffractive optical elements were the first choice to combine a high degree of freedom in light shaping and a high diffraction efficiency. Refractive microlens arrays were the first choice to provide uniform flat-top illumination for light mixing of divergent light. Micro-optical elements for pupil shaping soon evolved from a simple flat-top illumination to annular, dipole, quadrupole, multipole and very sophisticated freeform illumination settings. Micro-optical illumination became standard in optical lithography. However, their usage in projection lithography had its practical limits. Dedicated diffractive optical elements had to be manufactured on demand for each different mask set.

The next major step forward was to combine refractive and diffractive optical elements with a programmable micro-mirror array, referred as FlexRay (ASML). The programmable micro-mirror array allows to change illumination settings on the fly. Similar micro-mirror concepts are now realized in EUV lithography systems. Micro-optics has proven to be decisive key enabling technology for optical lithography over the last 15 years. Future micro-optical elements will also comprise polarization properties, allowing to shape polarization. Design, manufacturing and applications of refractive, diffractive and reflective micro-optics in optical lithography will be discussed.

9052-68, Session PS4

Feasibility study of production by full-chip application of model-based mask data preparation

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As we go forward into advanced process nodes, it is known that shot count explosion and the decline of mask CD linearity by the smaller feature size which will be real issues for mask making.

So far, Mask Data Preparation using Model Based approach (MB-MDP) has been introduced as one of the key solutions for the issues.

The functionality and effectiveness have been proven, but data on scalability has been limited.

This paper describes the result of mask writing by using a full-chip test data which correspond to the 14nm process node and D2S TrueMask® MDP.

The feasibility of using MB-MDP in a real mask production flow and its benefits are confirmed.

9052-70, Session PS4

Model-based pattern dummy generation for logic devices

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The insertion of SRAF(Sub-Resolution Assist Feature) is one of the most frequently used method to enlarge the process window area. In most cases, the size of SRAF is proportional to the focus margin of drawn patterns. However, there is a trade-off between the SRAF size and SRAF printing, because SRAF is not supposed to be patterned on a wafer. For this reason, a lot of OPC engineers have been tried to put bigger and more SRAFs within the limits of the possible. The fact that many papers about predicting SRAF printability have been published recent years reflects this circumstance.

Pattern dummy is inserted to enhance the lithographic process margin

and CD uniformity unlike CMP dummy for uniform metal line height. It is ordinary to put pattern dummy at the designated location under consideration of the pitch of real patterns at design step. However, it is not always desirable to generate pattern dummies based on rules at the lithographic point of view.

In this paper, we introduce the model based pattern dummy insertion method, which is putting pattern dummies at the location that model based SRAF is located. We applied the model based pattern dummy to the layers in logic devices, and studied which layer is more efficient for the insertion of dummies.

9052-71, Session PS4

Adaptive OPC approach based on pattern grouping algorithm

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OPC (Optical Proximity Correction) has been employed for over decade to address local lithographic printing effects. With the intensive scaling down of the designs as well as the increasing complexity of layout routing, lithographic process is being pushed to its theoretical limit and it has led to continuously shrinking DoF (Depth of Focus). Complex OPC model components are hence included into optical lithography simulation to ensure tolerable CD (Critical Dimension) variation and sustainable DOF of concerned layouts. For example, very complicated segmentation needs to be applied in mask correction, which comes at the cost of long runtime and requires an effective approach to consolidate the adequacy of model components during the flow of correction parameter tuning.

In this paper, an approach was demonstrated to improve the accuracy and efficiency of OPC parameter tuning for mask correction. The approach starts with analyzing the evaluation points in post-OPCed database to identify those intolerable variations, followed by a pattern similarity grouping for the above intolerable layouts. A weighting index table was established based on such as the magnitude of CD variation, target CD dimension, dissection type and run length, for prioritizing the problematic variations. Then the corrective parameters are accordingly optimized to reduce the variation on highly prioritized patterns. During the iteration flow of OPC parameter optimization, the use of pattern similarity grouping for the problematic layouts greatly reduces turn around time.

9052-72, Session PS4

Study of the pattern aware OPC

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It's critical to address the yield issues caused by process specific layout patterns with limited process window. RETs such as PWOPC are introduced to guarantee high lithographic margin, but these techniques cost high run-time when applied to full-chips. There's also lack of integrated solution to easily identify, define comprehensive patterns and apply different controls and/or constraints over these patterns through different stages of OPC/RET process.

In this paper, we study a pattern aware OPC flow that applies PWOPC or specific corrections locally to layouts with critical and yield limiting patterns. The Cadence pattern aware process window OPC (PAPWOPC) flow and hotspots tagging capability are evaluated for 50 nm node logic devices.

We use the following PAPWOPC flow for our study. 1) In database, we define edge patterns using basic pattern types and define patterns for hotspots with complex 2D geometries through Cadence Squish patterns. We do the pattern classification and matching to specify the potential hotspots in the full chip. 2) For these specific patterns, we apply flexible pattern based parametric control over different OPC/RET stages. For example, we apply pattern based edge bias for layer optimization and tune the optimal target points and edge segmentations for different patterns to achieve optimal result. 3) For non-critical patterns, we apply the normal OPC and rule based assist features. For the critical patterns, PWOPC that supports two levels of EPE band controls, dose range variation for multiple models and fine EPE band control over different patterns is applied. Model based assist features (MBSRAF) can also be applied selectively to different patterns to achieve considerable process window improvement. 4) The verification flow is used to extensively check the hotspots for potential violations. The potential hotspot patterns are collected and reused to identify and fix hotspots in future layouts of the same process.

For our study, we are able to apply the pattern based controls over different stages of PAPWOPC, optimize the layout; fine tune the evaluation point and segmentation; use MBSRAF on certain hot spots; apply different dose range and EPE band for critical patterns. We compare the full chip PAPWOPC run with normal OPC and full chip regular PWOPC that applies CD based EPE tolerance. Normal OPC has many yield related issues with under dose and over does conditions. Although the full chip PWOPC proves to be an effective way for user to do a simple, full chip PWOPC without specifying complex pattern controls, it causes great amount of run time penalty and does not achieve optimal process window. Overall, PAPWOPC achieves the best process window, especially over the hotspots, without sacrificing turnaround time. The study demonstrates the benefit of the new flow with fine grained process window controls over different patterns and speeds up the turnaround time of hotspots fixing

9052-73, Session PS5

The advanced verification methodology for OPC model via distance calculation in 3D image parameter space (DC-3D-IPS)

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In this paper, we present an advanced verification methodology for distinguishing the root cause of the model error and verifying the coverage of the model. This newly introduced methodology involves so called Distance Calculation in 3D normalized Image Parameter Space (DC-3D-IPS). This approach is applied to an example system in order to distinguish the causing factor of OPC model error among absence of samples, immature CM1 fitting, or both. From the results, we can select appropriate next process for improving current OPC model error, such as adding appropriate samples or more optimizing calibration parameters. This proposed verification method is tested with the several cases of the most recently developed sub 20nm logic device.

9052-74, Session PS5

Full-chip model-based OPC verification by using rigorous model

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As design rule of devices are getting smaller, it is hard to obtain enough process window like DOF, EL. In aspect of device integration, lithography processes which are included in etching process became more and more important. It has been claimed that photo resist profile is closely related with etch bias and vertical profile. Resist top-loss and bottom slope seriously affect after-etching profile. In order to address these problems, new model based verification method is necessary for preventing hot spots.

In this paper, we propose more practical method of model based verification using rigorous simulation and wafer verification results. Highly accurate model is obtained by physical model fitting with minimal experimental data set. After that, virtual data are extracted from rigorous simulation model for applying full chip model based verification modeling. Basically, 2 data sets will be needed for verification of 2-level model, for detecting resist top-loss and bottom-slope. Finally this article shows comparison results of model based verification and real wafer inspection. And also, we try to prove that the newly proposed method is another good candidate to address existing problems such as pinching and bridging after post etching and CMP process

9052-75, Session PS6

Effect of mask 3D and scanner focus difference on OPC modeling and verification

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A robust optical proximity correction (OPC) model must include process variation to be most effective in volume manufacturing. Normally, calibration of an OPC model is applied based on data from a single scanner. However, scanner and mask three dimension (3D) effects have been found to effect printing performance and OPC model effectiveness. OPC model tolerance is improved if the fingerprints of different scanners are matched as closely as possible. Scanner source maps or boundary conditions can cause focus differences between isolated and dense features for different scanners. The scanner used to build a robust OPC model should have a minimum focus difference between isolated and dense features. Mask 3D effects must be included in OPC model building. In this work the effects of focus differences between nested and isolated features for OPC model building will be quantified. In addition, mask 3D effect contributions to OPC models will also be illustrated. OPC model tolerance to variation will be shown using data from multiple scanners and mask topographies and methodologies to optimize OPC models will be presented.

9052-76, Session PS6

Combining lithography and etch models in OPC modeling

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With constant shrinking of device critical dimensions (CD), the quality of pattern transfer in IC fabrication depends on the etch process and the exposure process fidelities, and the interaction of lithographic and etching processes is no longer negligible. Etch effect correction with accurate models has become an important component in optical proximity correction (OPC) modeling and related applications. It is now commonly accepted that the lithographic and etch effects should be modeled and corrected in a sequential and staged way: a resist (or lithographic) model should be created and used for lithographic effect compensation, and an etch model should be created and used for etch effect compensation. However, there can be various degrees of separation of these two modeling stages. In order to optimally capture the significant variation in the post-development resist patterns and post-etching patterns, it is helpful to integrate these two processes together for the OPC model calibration practice. In this paper, we analyze the integrated simulation approach in OPC modeling where the entire resist model information is made fully accessible in the etch modeling stage to allow the possibility of resist and etch co-optimization, e.g. through adjusting the resist model to optimally fit the etch data. Furthermore, the integrated simulation technique is integrated into a verification flow to simplify the conventional staged flow.

9052-77, Session PS6

Fast rigorous modeling applied to wafer topography effects for optical proximity correction

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Reflection by wafer topography and underlying layers during optical lithography can cause unwanted overexposure in the resist [1]. In most cases, the use of bottom anti reflective coating limits this effect. However, this solution is not always suitable because of process complexity, cost and cycle time penalty, as for ionic implantation lithography process in 28nm Fully-Depleted Silicon-on-Insulator (FDSOI) technology. As a consequence, computational lithography solutions are currently under development to simulate and correct wafer topographical effects [2], [3]. For ionic implantation source drain (SD) photolithography step on Silicon-on-Insulator (SOI) substrate, wafer topography influences resulting in implant pattern variation are various: active silicon areas, Poly patterns, Shallow Trench Isolation (STI), SOI areas and topographical transitions between these areas. In 28nm FDSOI SD process step, the large number of wafer stack variations involved in implant pattern modulation implies a complex modeling of optical proximity effects. Furthermore, those topography effects are expected to increase with wafer stack complexity through technology node downscaling evolution. In this context, rigorous simulation can bring significant value for wafer topography modeling evolution in R&D process development environment. Unfortunately, classical rigorous simulation engines are rapidly run time and memory limited with pattern complexity for multiple under layer wafer topography simulation.

A presentation of a fast rigorous Maxwell's equation solving algorithm integrated into a photolithography proximity effects simulation flow is detailed in this paper. Accuracy, run time and memory consumption of this fast rigorous modeling engine is presented through the simulation of wafer topography effects during ionic implantation SD lithography step in 28nm FDSOI technology. Also, run time and memory consumption comparison is shown between presented fast rigorous modeling and classical rigorous RCWA method through simulation of device hotspots. Finally, integration opportunity of such fast rigorous modeling method into OPC flow is discussed in this paper.

9052-78, Session PS6

Bringing SEM-contour based OPC to production

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One of prerequisite to build OPC models of quality is to gather with a SEM a lot of critical dimension (CD) data covering various process conditions and layout configurations. Using SEM image contours is a

very interesting alternative to address the problems of data collection and improve the characterization of complex 2D structures. So far the few papers [1-4] describing this technique were motivated to ameliorate the technique or to establish its benefits but no mature application has been demonstrated, probably because of the difficulty to get reliable contours and to deal with this new type of data.

The scope of this work is to present an OPC solution based on SEM image contouring with the purpose of being implemented in production (see figure 1,3). Our goal is to present a specific flow aimed at addressing the main challenges of working with SEM contours. The objective is also to assess the quality of the contour based model with respect to a reference model using traditional CD measurements calibrated upon the same experimental conditions.

The OPC models target 28nm node Active layer and are calibrated across process windows. Extreme resist shrinkage upon measurement with the SEM e-beam as well as the asymmetric qualities between horizontal and vertical edges within the image required to verify carefully the matching between contour and conventional CD measurements (see figure 2). Furthermore this work investigates the importance of site selection (number, type, image space coverage) for a successful contour-based OPC (see figure 4). It also highlights the complexity of combining 2D sites, containing each hundreds of edge placement errors (EPE), to get well balanced image parameter space (IPS) signatures in term of coverage and redundancy.

The comparison of conventional and contour based models takes into account the calibration and verification performances of both models with a possible cross verification between model data sets. In addition the data collection effort including the data analysis and cleaning as well as the overall data quality were added to the benchmark. The difference between the two models is also examined qualitatively by analyzing the major contributors to EPE in both cases. Specific advantages of contour based model are also discussed.

9052-79, Session PS6

A stochastic approach to SRAF printing prediction

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Sub-Resolution Assist Features (SRAFs) are extensively used in optical lithography to expand the manufacturing process window. These additional shapes are narrow lines or small rectangles placed adjacent to primary shapes in order to create denser and more uniform environment that facilitates relatively isolated primary features show more dense-like behavior. The placement, size and shape of the SRAFs have to be carefully optimized to maximize their positive effect on the manufacturability and at the same time prevent them from transferring to photoresist. SRAFs printing into silicon can be a considerable source of yield loss overwriting the benefit of the increased process window.

The key step towards fine-tuned SRAFs is the identification and elimination of the assist features that are likely to print. One of the commonly used methods is based on the aerial image simulation at empirically defined process conditions. The aerial image intensity in the spaces between target shapes is compared to a threshold estimated based on wafer data. The method typically requires extensive wafer data collection to empirically determine appropriate process conditions (overdose, mask writing error, focus and aerial image threshold) used in simulations to mimic a real process in a fab. The empirical approach is very costly in terms of time and resources and at the same time doesn't give an insight into the details of the SRAF printing process.

In this work the process of SRAF printing is approached from the point of view of the litho process variation. Indeed, the SRAF printing is a stochastic effect observed as sporadic SRAF transfer to photoresist due to random spatial and temporal variation of process conditions. Main contributors to the random nature of SRAF printing are dose variation, mask writing errors, variation of resist properties, focus variation etc. In our approach the process variability is considered separately for the exposure dose, mask error, and focus. A stochastic model describing SRAF printing probability depending on these parameters is set up in analytical form. The model is calibrated using SRAF shapes that have relatively high probability to print in order to minimize amount of the wafer data needed for calibration. After the calibration is done the model is used to setup adequate SRAF printing detection conditions (overdose, mask writing error, focus) to catch SRAFs that are printing with probability higher than a desired level.

The model's predictions are compared to wafer data. Advantages and limitations as well as peculiarities of the model calibration are discussed and compared to other methods.

9052-80, Session PS6

The benefit of mask written by model-based mask database preparation (MB-MDP) on advanced node

Chain Ting Huang, United Microelectronics Corp. (Taiwan)

In order to achieve wafer process window on advanced node, mask shape had become more and more complex. So, the mask writing time, the pattern accuracy (especially for the corner rounding and assistant feature) and the mask CD uniformity (CDU) were played a very important role. We should get wider DOF and smaller MEEF when the mask shape is more close to the OPC result.

In this paper, we will compare the mask written by Model Based Mask Database Preparation (MB-MDP) with conventional one. The mask written by MB-MDP will not only reduce the mask writing time by overlapped shot counts, but also improve the accuracy of small feature and corner rounding. It will also get better mask CD uniformity. Finally, we will also compare the AIMS and wafer printing result to prove the MB-MDP's benefit.

9052-81, Session PS6

Resist toploss modeling for OPC applications

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As Critical Dimension (CD) sizes decrease for 32 nm technologies and beyond, resist loss increases and resist patterns become more vulnerable to etching failures. Traditional OPC models only consider 2D contours and neglect CD height variations. Rigorous resist simulators can simulate a 3D resist profile but they are not fast enough for correction or verification on a full chip. However, resist loss for positive tone resists is mainly driven by optical intensity variations which are accurately modeled by the optical portion of an OPC model. In this article, we show that a Calibre CM1 resist model can be used to determine resist loss by properly selecting the optical image plane to calibrate to. The resulting model can simulate resist loss well as shown in Figure 1.The model can then be used to identify toploss hotspots on a full chip and in some cases to correction of these patterns. In addition, the article will show how the model can be made more accurate by accounting for some 3D effects like diffusion through height.

9052-82, Session PS7

Improving on-wafer CD correlation analysis using advanced diagnostics and across-wafer light-source monitoring

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With the implementation of multi-patterning ArF-immersion patterning for sub 20nm integrated circuits (IC), advances in equipment monitoring and control are needed to support on-wafer yield performance. These in-situ equipment monitoring improvements, along with advanced litho-cell corrections from on-wafer measurements, enable meeting stringent overlay and CD control requirements for advanced lithography patterning. The importance of light-source performance on lithography pattering (CD and overlay) has been discussed in previous publications. [1-4] Recent development of Cymer ArF light-source metrology and on-board monitoring enable end-users to detect, for each exposed wafer, changes in the near-field and far-field spatial profiles and polarization performance, [5-6] in addition to the conventional 'optical' scalar parameters, such as bandwidth, wavelength and energy. The major advantage of this capability is that the key performance metrics are sampled at rates matched to wafer performance, which is critical for correlation with on-wafer performance for process control and excursion detection.

In this work, we present a new technique for characterizing patterning impacts due to changes in light-source performance. This technique provides a significant improvement in characterization of patterning sensitivity and allows decoupling contributions from other process or equipment. Wafer patterning experiments have been carried out in imec facilities, using an XLR660 laser and NXT:1950i ASML scanner, with controlled changes to bandwidth, wavelength and energy performance within the wafer. The changes in patterning performance are characterized using scatterometry and top-down CD SEM, showing excellent correlations between light-source data and on-wafer photoresist CD, CD uniformity and SWA for typical patterning geometries for ~40nm half-pitch. The characterization technique discussed in this paper significantly improves the correlation quality between the light-source data and wafer patterning by increasing the measurement signal-to-noise. Finally, this paper discusses the requirements for improved light-source control for further shrink extensions of multiple-patterning ArF immersion lithography.

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9052-83, Session PS7

Study on abnormal intra-field CD uniformity induced by Efese-tilt application upon complex leveling scheme

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We observed up to 6 nm abnormal ADI CD gradient trend-down in Y-direction (scan direction) on strictly repeating Via-hole patterns across 8mm x 6mm chip area under base line (BL) photo condition where Efese tilt is applied. Upon thorough analysis, we attribute this CD trend-down to Efese tilt ill functioning upon complex wafer topography and leveling jump. An "effective Efese tilt" model is proposed and verified to give an insight of the safety zone for applying Efese tilt for future reference.

With best-energy-best-focus exposure, repeated Via-hole patterns within an 8mm x 6mm chip region clearly shows an abnormal CD trend-down of about 6nm from top to bottom in Y-direction . No such CD variance is observed in X-direction.

Location dependent focus shift is checked upon measuring "top", "middle", "bottom" pattern on FM (focus matrix) wafer and shows no defocus among. Regional defocus is thus ruled out as the origin. Mask writing error is also directly verified in the area of interest and the result seems normal. This indicates mask CD variance is not causing the abnormal local CDU issue.

It turns out this localized CD non-uniformity is only observed on incoming topography wafer, as non-patterned film-stack wafer suffers little to none from the same issue. As we turn our focus back onto the difference in leveling map, air gauge (AGILE) function is applied to BL wafer to see if surface topography information in the area of interest is real and if it impacts local CDU. The leveling of BL wafer with AGILE turns out as nearly the same with that of film wafer.

Without the +30nm 'fake' local leveling jump, abnormal CD trend-down stopped appearing after AGILE application. On the other hand, even without AGILE application, turning Efese-tilt off also cures the abnormal local CDU. It is clear that it's the combination of leveling jump and Efese-tilt results in the observed CD abnormality.

Targeting identical ADI CD, larger dosage is normally required for a heavier Efese-tilt, this indicates the region of CD trend-down might be experiencing a gradual climb of actual Efese-tilt through scanning. Based on this understanding, we propose an 'effective Efese-tilt' model explaining this phenomenon from a perspective of continuous leveling-induced effective Efese-tilt during exposure scan.

Within a single shot scan, to compensate for wafer topography, stage movement involves not only z-axis translation but also x/y-axis rotation. Through the cross-section of a wafer stage during scan with Efese-tilt off, It forms a normal tilt of wafer stage. With Efese-tilt on, a fixed tilt is superposed onto the normal tilt, forming continuous change of "effective Efese-tilt" corresponds to the continuous change of CD from top to bottom. This effect however is only directly observable when the superposed effective Efese-tilt variance is large enough.

To verify our model, we examined local CDU on wafer of another Via layer of 'leveling flip' topography on the same Efese-tilt setting. We observed the reverse effective Efese-tilt phenomenon that agrees with the model where local CD trends up from top to bottom.

In conclusion, Efese-tilt application upon none ideal incoming wafer topography could cause extremely significant intra-field CDU issue. Leveling calibration with air gauge is thus strongly recommended with Efese-tilt enabled layer as it often depresses

fake leveling jump signal. Never the less one should watch out for any abnormal leveling data that could result in high spatial frequency change in superposed stage posture through scanning so as to avoid Efese-tilt specified CDU issue. It is also worth noticing that as OPC model is setup on non-topo film stack wafer, when verifying the model on topo wafer, the CD impact from "effective Efese tilt" shall not be ignored.

9052-84, Session PS7

Pattern environment impact on wafer of metal layers with high-NA process on advanced node

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In the High NA process, pattern environment will become very aggressive because of scattering effect. Especially on metal layers, maybe it will cause pattern bridge when the pattern density is varied. We need to find out the root cause and have a good solution.

In this paper, we analyze the root cause by checking the pattern density influence on mask CD and wafer printing CD. We design the different pattern density layout to measure the mask CD error, use AIMS to measure the aerial image CD and print wafer to check the real result. Then, we try to add some assistant feature and use Prolith to simulate whether having the improvement.

9052-85, Session PS8

Closing the loop in lithography simulation by adding capabilities for accurate modeling of SEM

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Optical lithography simulation is an indispensable part of device and process development in the semiconductor industry. Simulations can accurately predict the aerial image for a specific combination of resists, mask and optical systems, and can simulate the resist development. The most widely used method to measure nanopatterns is scanning electron microscopy (SEM). However, image formation in the SEM is a complex process; there is no simple way to determine the relationship between the SEM image and the shape of the resist line. Electron scattering in the 3D pattern, the setup of detectors, beam voltage and current, and the scanning parameters of the beam affect the appearance of the SEM image. In addition, extracting sizes and wall angles from an SEM image is a complex problem in itself. This creates a gap in correlation of the simulation results produced by optical simulators and the experimental SEM results.

In this paper, we present simulations where the first principles of physics were used to simulate both the aerial image and scanning electron microscopy. Such extended simulations create the capability of directly comparing the simulated results, which are SEM images, with the actual SEM images. The simulation is comprehensive, involving: the optical source, mask, aerial image, 3D absorbed energy in the resist, resist development, interaction of the primary electron beam with the 3D resist pattern, electron scattering from the pattern, generation of fast and slow electrons, their trajectories to the detector, as well as detector properties. The result of the simulation produces an SEM image.

The HyperLith simulator was used to simulate the aerial image and the resist profile. The result of the simulation was 3D resist lines. The CHARIOT simulator was used to model the SEM image of the resist pattern. In addition to electron scattering, it is capable of simulating charging and resist shrinkage. The input file format of the CHARIOT software was updated to be compatible, so that the 3D resist profile from HyperLith software could be used as input for the CHARIOT to simulate SEM image. Results of simulations are discussed.

9052-86, Session PS9

Effective simulation for robust inverse lithography using convolution-variation separation method

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As critical dimension shrinks, pattern density of integrated circuit gets much denser and lithographic process variations become more pronounced. In order to synthesize masks that are robust to process variations, the average wafer performance is optimized via minimizing the expectation of the difference between the desired pattern and the output pattern with respect to process fluctuations. This method takes into account process variations explicitly and is easily accomplished. However, it needs to calculate a large number of optical images under different process variations in each iteration during the mask optimizing process and thus significantly increases the computational burden. Most recently, we proposed a convolution-variation separation (CVS) method for modeling of optical lithography, which separates process variables from the coordinate systems and hence enables fast computation of lithography imaging through a wider range of process variations. In this paper, we provide detailed formulation of robust ILT making use of the CVS method, and further investigate the impacts of arbitrary statistical distribution of defocus variations on the synthesized mask pattern in robust ILT.

9052-87, Session PS9

Proteus inverse lithography technology: ILT where it is needed

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Traditional segment-based model-based OPC methods have been the mainstream mask layout optimization techniques in volume production for memory and embedded memory devices for many device generations. These techniques have been continually optimized over time to meet the ever increasing difficulties of memory and memory periphery patterning. There are a range of difficult issues for patterning embedded memories successfully. These difficulties include the need for a very high level of symmetry and consistency (both within memory cells themselves and between cells) due to circuit effects such as noise margin requirements in SRAMs. Memory cells and access structures also consume a large amount of area in embedded devices so there is a very high premium to be gained from shrinking the cell area as much as possible, leading to very difficult resolution, 2D CD control and patterning process window requirements. Additionally, the range of interactions between mask synthesis corrections of neighboring areas can extend well beyond the size of the memory cell, making it difficult to fully take advantage of the inherent designed cell hierarchy in mask pattern optimization. This is especially true for non-traditional (i.e., less dependent on geometric rule) OPC/RET methods such as inverse lithography techniques (ILT) which inherently have more model-based decisions in their optimizations. New inverse methods such as model-based SRAF placement and ILT are, however, well known to have considerable benefits in finding flexible mask pattern solutions to improve process window, improve 2D CD control, and improve resolution in ultra-dense memory patterns. They also are known to reduce recipe complexity and provide native MRC compliant mask pattern solutions. Unfortunately, ILT is also known to be several times slower than traditional OPC methods due to the increased computational lithographic optimizations it performs.

In this paper, we describe and present results for methodologies, use models, to greatly improve the ability of ILT to optimize advanced embedded memory designs while retaining significant hierarchy and,

therefore, have good turnaround time. This paper will explain the enhancements which have been developed in order to overcome the traditional difficulties listed above. Comparisons of local CD control, global CD distribution, process window benefit, turn-around time and hierarchy retention will be provided. Finally, we will conclude with the outlook for further extensions and new applications of these methods.

9052-88, Session PS10

Technology for monitoring shot-level light source performance data to achieve high-optimization of lithography processes

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FDC (Fault Detection & Classification) systems are widely adopted to the lithography process, in order to improve the yield rate and availability factor of facilities.

Recently, there have been some attempts to stabilize and optimize the lithography process by using the FDC system to read and analyze the light source performance data of each wafer.

In contribution to this activity, Gigaphoton has developed two new monitoring systems called sMONITORING and eMONITORING, which provide scanner shot-level performance data of the light source (to the FDC system).

This monitoring system can be easily added to Gigaphoton's GT62A series ArF Excimer Lasers and successive models.

The sMONITORING system intercepts and provides basic shot-level monitoring data such as Wavelength, Energy, E95 Spectrum, Chamber Gas Pressure and HV.

In addition, the eMONITORING system provides shot-level beam performance data, such as Beam Profile, Pointing, Divergence, Polarization.

To obtain the beam performance data provided by eMONITORING, we have developed a new metrology module called the BPM (Beam Performance Monitor module) that can be retrofitted to our existing light source.

The BPM's beam splitter was specially designed to bend only a small fraction of the source beam, so we are able to simply install the BPM without the need for special optical alignment.

During exposure time the system automatically identifies the start and end timing of wafer and each shot based on the burst of firing signals from the scanner, and stores the measured data in sequence.

The stored data is sorted by wafer or shot, and sent to REDeeM Piece which converts the data to the user's protocol and send it to the FDC system.

The user also has the option to directly view or download the stored data through a GUI.

Compared to traditional wafer-level monitoring systems, our new monitoring system can work with shot-level data, which means to that process management can be achieved at the reticle level.

Light source data and process results can be compared at the reticle level for each location on the wafer.

Users can analyze the correlation between the obtained light source performance data and the corresponding process state, and assess critical performance item of the light source that need to be improved or optimized.

For those performance items that are not strongly correlated to the process state, users may choose to avoid unnecessary maintenance and continue operating the unit as long as that performance item continues to be within acceptable levels - ultimately contributing to the reduction of the total operating cost of the light source.

Also for the multiple light sources, we can expect our monitoring system to contribute to the comprehensive management of the time performance and gaps caused by service events.

9052-89, Session PS10

A temperature control algorithm of immersion liquid for immersion lithography

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Immersion lithography is one of the main technologies used to manufacture the integrated circuits with shortest critical dimension. In immersion lithography, temperature of immersion liquid is strictly constrained and its allowable range is less than 0.01? at 22 ?. To meet this requirement, a temperature control algorithm is proposed.

The temperature of the immersion liquid from ultra-pure water (UPW) is controlled with process cooling water (PCW) via heat exchangers. By adjusting the flow rate of PCW through the heat exchangers, the control system modulates the amount of heat exchange, so that the temperature of the immersion liquid can be properly controlled. The schematic diagram of the system is detailed in Figure 1. There is a pump in the immersion liquid pipeline, two flow-rate control servo-valves in the PCW pipeline, sensors to detect temperate flow rate and pressure before and behind each heat exchanger in two pipelines, three heat exchangers and some valves. At the same time, more valves can be added if required. All the pips, sensors, heat exchangers and other components are well chosen coated with or made of PFA or PTFE which is chemical and thermal inert so that can maintains process fluid purity and temperature. The amount of the heat exchangers is calculated to ensure enough heat transfer area. Two are behind the first flow-rate control servo-valve, one behind the latter servo-valve. Such structure combined with the algorithm can suit the high-precision requirement. The pump which forms a circular loop can increase and stabilize the flow rate of the immersion liquid into the heat exchangers while not changing the flow rate of the immersion liquid into the lithography which is rather small.

The system is multi-disturbed, time-variant, non-linear and time-delayed and its transfer function is related to the inlet temperature and flow rates of the streams through the heat exchangers. According to the character of the system, two serial controllers, each of which features a cascade structure and fuzzy PID feedback algorithm are designed. The two controllers correspond to two flow-rate control servo-valves on the PCW pipeline respectively. Besides the requirement of enough heat transfer area, two serial controllers can eliminate the influence of the temperature and flow rate disturbance of the input streams-the temperature and flow rates of two streams into the latter controller are nearly constant. The cascade structure can separate the flow rate fluctuation of the flow-rate control servo-valve from influencing the heat transfer in the heat exchanger. The inner loop adjusts the flow rate according to the set point from the outer loop which modulates the flow rate set point according to the temperature set point of immersion liquid and its practical temperature. Since the modulation of the flow rate is much faster than the temperature change, the fluctuation of the flow rate caused by the servo-valve can be ignored. The fuzzy PID feedback control algorithm can properly adjust the non-linear and time-variant system.

The simulation result shows that the precision of 0.01 degree can be realized. Better effect can be got in further research.

9052-90, Session PS10

Novel wafer stepper with violet LED light source

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A wafer stepping exposure apparatus applied for a wafer and a mask is provided. A surface of the wafer has a photoresist. One of a plurality of

regions on the wafer has a size similar to a size of a pattern zone of the mask. The wafer stepping exposure apparatus includes a wafer table, a mask table and a light source. The wafer table is used to fix the wafer. The mask table is used to fix mask. The mask and the wafer table may have relative motion with each other so that the pattern zone is aligned to one of the regions. In addition, the mask table being fixing the mask is directly contacted with the wafer table being fixing the wafer or only has a vacant space from the wafer table. The LED light source offers a light beam being used to penetrate the pattern zone to expose the photoresist. Besides, a method for wafer stepping and exposure is will be presented in this conference.Exposure result by using IP3600 resist and violet LED light (wave length 360nm to 410 nm) will be present in this conference. .

9052-91, Session PS10

Illumination system without scanning slit for lithographic tools

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The 193nm step-and-scan lithographic machines are the dominant exposure tools for commercial chip manufacture by now. The step-and-scan lithographic illumination system has a scanning slit which could not only control the exposure field size but also assist the wafer to complete scanning process with high uniformity. The scanning slit is comprised by four blades which are drive by four electric actuators. The 193nm step-and-scan lithography sets very strict demands on scanning speed and dimensions of the blades. For example, in the 193nm hyper NA1.35 lithographic machine, the scanning range is about 22mm; the maximum speed of the two slits scanning in the Y direction is 2800mm/s; it only allows the scanning slit to stabilize its scanning speed in 10ms. The scanning slit satisfying the mechanical and dynamic demands is very complicated. Furthermore, the vibrations must be minimized and isolated to prevent from influencing the optical components. This paper presents a 193nm lithographic illumination system without utilizing scanning slit.

The system mainly includes these following optical elements: a beam expander, a micromirror array (MMA), a fast scanning mirror (FSM), a collimating lens, an aperture array, a microlens array (MLA) and a condenser. The MMA has many micromirrors which could rotate individually along two mutually perpendicular axes, and a MMA controller can controller the rotation angles of the micromirrors of the MMA. The FSM has a rotatable mirror, and a FSM controller could control the rotation angle of the rotatable mirror. The mask is right behind the condenser. The beam emitted from the light source firstly passes through the beam expander. Then, the expanded beam is incident on the MMA. The incident beam is separated into many sub-beams by the micromirros. When these sub-beams are reflected by those micromirrors which have different rotation angles, and each sub-beam has a particular direction of propagation. After reflected by the FSM, the sub-beams pass through the collimating lens, and form a light distribution (named illumination mode in the lithography) on the aperture array. The aperture array contains lots of small rectangular apertures which have the same dimensions. After passing through the aperture array, the MLA and the condenser, the light beams form a rectangular and uniformity area on the mask. The MMA controller controls rotation angles of the micromirrors on the MMA, and traditional, circular, dipolar and quadrupole illumination modes can be form on the aperture array by the sub-beams. After the illumination mode is formed, the MMA controller keeps the micromirror still. The FSM controller controls the rotatable mirror of FSM to change the position of the formed light intensity distribution on the aperture array, and that will change the light beam amount blocked by the aperture array. When the rotatable mirror of the FSM rotates at a certain angular speed, the illuminated area can realize scanning process. System layout is calculated, and scanning process is simulated by the presented system. The simulation results show the system is feasible for the 193 nm lithographic machine.

9052-92, Session PS10

Glass ceramic ZERODUR® enabling nanometer precision

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The IC Lithography roadmap foresees manufacturing of devices with critical dimension of < 20 nm. Overlay specification of single digit nanometer asking for nanometer positioning accuracy requiring sub nanometer position measurement accuracy. The glass ceramic ZERODUR® is a well-established material in critical components of microlithography wafer stepper and offered with an extremely low coefficient of thermal expansion (CTE), the tightest tolerance available on market. SCHOTT is continuously improving manufacturing processes and it's method to measure and characterize the CTE behavior of ZERODUR®. This paper reports on the improvements of the three dimensional CTE homogeneity measured to single digit ppb level for a ZERODUR® cube of 200mm edge length with significant progress compared to the identical investigation reported in 2004. Additionally simulation calculations based on a physical model are presented predicting the long term CTE behavior of ZERODUR® components to optimize dimensional stability of precision positioning devices. The ever tighter CTE specification for wafer stepper components are calling for ongoing improvements in CTE measurement accuracy. First measurement results are presented for the Advanced Dilatometer targeting at < 3 ppb / K absolute accuracy which is currently in development at SCHOTT. The paper explicitly demonstrates the capability of ZERODUR® to enable the extreme precision required for future generation of lithography equipment and processes.

9052-93, Session PS10

Improvements in energy timing control (ETC) for XLR 660xi systems

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As chipmakers continue to reduce feature sizes and shrink CDs on the wafer to meet customer needs, Cymer continues developing light sources that enable advanced lithography, and introducing innovations to improve productivity, wafer yield, and cost of ownership. In particular, the architecture provides dose control, improved spectral bandwidth stability, both of which enables superior CD control and wafer yield for the chipmaker. The XLR 640ix is the next generation of argon fluoride (ArF) light sources, and the first to provide flexible power output to meet ever-increasing productivity demands, particularly for double patterning applications. It has the unique capability to operate in a range from 60W for typical immersion applications, to 90W for higher dose or higher throughput applications.

The XLR 660ix also incorporates new energy controller technology for improvements in spectral bandwidth stability, energy dose stability, and wavelength stability. Figure 1 illustrates the marked improvement in wavelength control with the new controller vs. the legacy controller. This translates to improved CD control and higher wafer yields. The authors will discuss the impact that these improvements will have in advanced lithography applications.

9052-94, Session PS10

Advanced excimer laser technologies enable green semiconductor manufacturing

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In recent years, 'green' has been a pervasive topic throughout the world and in all industries. Green initiatives are now mandatory and force manufacturers to not only maintain corporate responsibility, but to positively impact the bottom line. Our industry is not excluded and it affects semiconductor equipment as a whole?both tool manufacturers and users.

We Gigaphoton, a laser manufacturer, have been leading the drive towards creating a greener, more environmentally-friendly product. Green is an integral part of our business and development strategy, because our mission is to deliver the most effective and efficient solutions for high-volume manufacturing where the consideration of green is most critical. The focus of green is not only about conserving resources and eliminating waste, but also concerned with total operational cost. Gigaphoton continues to extend its expertise in green technologies and has developed its EcoPhoton program to significantly reduce the environmental affects and the overall cost of operations. The estimated cost for utilities for lasers, which includes electricity consumption, gas consumption and heat management, will be approximately 30% of the total cost of operation.

To address this issue, Gigaphoton utilizes highly-efficient Injection-Locking technology, and has developed a new chamber and a new technique for gas usage optimization. This new chamber enables 10% less electricity consumption by reducing head inductance of discharge circuit and balancing the operation point. Also, a new technique for gas usage optimization can reduce the amount of gas needed by 50% and realizes zero down time for gas refill, by thorough analysis of laser performance and automatic feedback to gas control.

These technology achievements are based on Gigaphoton's R&D strategy for more than a decade. In 2004, Gigaphoton introduced the highly-efficient Injection-Locking technology. To achieve the high throughput and resolution needed by scanners, excimer laser light sources are required to produce high power and narrow spectrum beams. However, when power is increased, the spectrum width tends to widen. To overcome this challenge, Gigaphoton introduced the world's first Giga Twin™ platform with Injection-Locking technology. The Giga Twin platform utilizes two identical chambers. The first chamber, called the master oscillator, generates the narrow spectrum "seed" light. This light is then fed into the second chamber, called the power oscillator, which through the Injection-Locking technology is able to amplify the seed light to higher powers without widening the spectrum. It is more difficult to development compared to alternative solutions, but from an efficiency and scalability perspective it is undeniably the most ideal solution for high power operations in high-volume manufacturing environments.

Further, a new hybrid laser system that utilizes a solid-state laser is under development. This system will require a maximum power of only 36kW compared to 60kW on the current system. This presentation will discuss Gigaphoton's various solutions that enable green manufacturing, reduction of the overall cost of operations, less energy consumption, utilization of gas modules with less volume and refill requirements, and Helium-free lasers, all of which also contribute to minimizing down time for maintenance.

9052-18, Session 5

Automated sample plan selection for OPC modeling

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The success of model-based resolution enhancement techniques, including optical proximity correction (OPC) and source mask optimization depends on accurate modeling of lithography, resist and etch processes. The formalism of OPC modeling is empirically driven, with generalized kernel models fit to observed dimensions on a set of calibration patterns known as a sample plan. Typically designers select a set of a few hundred of patterns from a large pool, in the order of a few hundred thousand, for fitting via scanning electron microscope (SEM) measurements. Screening the SEM data for quality is a bottleneck in the technology development cycle. Reducing the number of patterns used can save time for analysis by roughly linear time and increases the likelihood of good measurements on the remaining patterns across the optical field. Of course the selection of patterns impacts the quality of models according to typical metrics such as cumulative CD error across a verification set. Current practice involves a combination of engineering judgment and bucketing methods to insure that chosen samples cover bins in image parameter space (i.e. measured values of imax, imin, slope and curvature), which is time-consuming and prone to over-fitting ([1],[2]). Moreover to ensure early market entry and better data coverage, turn-around time is becoming more critical. Recent research results report to address these problems via clustering in distance space derived from image pixels between points and sometimes image parameter space to eliminate redundancy ([3]-[6]). Unfortunately, data compression based on clustering cannot be used alone, because this would lead to arbitrary pattern exclusion due to the large test masks sizes.

On the other hand, clustering-based on diffraction orders and lithographic difficulty estimation (LDE [7]) have been shown to deliver excellent results selecting patterns for large scale source optimization ([8]). In this paper we show that such techniques can be further extended to automatically select sample plans. Our method uses a novel mathematical formulation that incorporates model insight and expertise in flexible objective functions which are co-optimized for higher accuracy. In addition to diffraction order-based clustering and LDE, image parameter distributions and pattern orientation/dimension are also taken into account. This ensures that the resulting automatic sample plan is at least of equivalent quality to the manual sample plan, but generated in a shorter time due to the full automated nature of the method.

Experiments comparing the models generated with the traditional manual method (POR) and the automatic proposed approach exhibit equivalent quality (see Figure 1), with the important benefit that the automatic approach is at least 5x faster.

9052-19, Session 5

Manufacturable conversion for freeform mask patterns using eigen-direction transformation

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Inverse lithography technology (ILT) is a model-based mask correction approach which employs a calibrated model with mathematical algorithms to optimize the mask patterns according to a pre-designed objective functions. ILT allows maximum degrees of freedom in mask pattern shapes to give better litho-performance than conventional segment-based OPC methods. However, such freeform mask patterns are difficult for real mask making and an extra step called Manhattan conversion is required to convert the curvilinear shapes into polygons with only 0? and 90? edges. To have better shape approximation with less litho-performance degradation, the ILT mask patterns after Manhattan conversion contain extensive segments and jogs which increase mask writing time and deteriorate mask CD control.

In this paper, an eigen-direction mask pattern simplification method is proposed to have more compact approximation with less performance degradation. The method exploits the eigen-directions of a curvilinear shape to obtain the closet rectangle approximation. To calculate the eigen-direction of pattern, an input pattern represented by multiple vertexes is first rasterized to a pixel-based pattern. The position of the geometrical center of a pattern is obtained by averaging all pixel coordinates. For the case of the geometrical center inside the pattern, two eigen-vectors belonging to the directions of the maximum and minimum standard deviation of a rectangle can be calculated by applying

the Hough transform, and subsequently the ratio of the eigen-values is equivalent to the ratio of edge lengths. For the case of the geometrical center outside the pattern, an innovative binary-recursion-pattern-split algorithm is applied to decompose a curvilinear pattern to several rectangles with minimum deformation. The pattern with an outside center will be split to two parts along the direction of minimum standard deviation and the calculation will be recursively run to obtain new eigen-vectors and eigen-values of each pattern.

9052-20, Session 5

Decreased shot count from shot overlapping and model-based fracturing for edge-based OPC layouts

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Resolution enhancement techniques such as Optical Proximity Correction (OPC) have enabled the semiconductor manufacturing industry to continuously shrink the critical dimension of integrated circuits. This results in increasingly complex masks and processing techniques leading to excessively long mask write times. In previous work, we proposed a model based fracturing algorithm allowing for shot overlap aimed at layouts resulting from pixel based OPC. In doing so, we minimize mask write time by directly determining the shot location, size and dosage from the curvilinear OPC mask.

In this work we propose a model-based fracturing algorithm for rectilinear masks, such as those resulting from edge-based OPC. Our approach to shot count reduction is to determine the shot information such as location and dose by using a mask manufacturing model and by allowing shots to be overlapped. Our proposed method differs from current model-based techniques as it can readily tradeoff between shot count and edge placement error (EPE) by adjusting two input parameters.

Our proposed approach transforms the fracturing problem to covering polygons with overlapping rectangular shots, which is known to be NP-complete. As such we heuristically cover the polygon with overlapping shots which we have empirically found to result in lower rectangle count than optimal polygon partition without overlap. Next we incorporate the forward scattering and resist model by setting up a least squares problem that seeks to minimize the mask error and to determine the best dose for all placed shots. Finally, we heuristically update the locations of the shot edges by computing the EPE between the simulated and desired contours.

We have tested our algorithm on 4 layout clips of an SRAM chip with the largest clip being a 400μm x 400μm, 900,000 polygon layout. We fractured this layout with a non-overlap commercial package and our proposed algorithm with two sets of input parameters. The commercial package resulted in 3.78 million shots and a weighted average EPE (WAEPE) of 0.77. Our proposed fracturing with the highest fidelity results in only 2.6 million shots, a 31% reduction in shot count. This fracturing suffers from a minor degradation in fidelity with the WAEPE increasing by 10% from 0.77nm to 0.82nn. The fracturing with the lowest shot count resulted in only 1.7 million shots, a 53% improvement; this increases the WAEPE by almost 50% to 1.02nm.

We repeated these test on the 3 smaller layout clips; the smallest clip is 20μm x 16μm with 400 polygons while the largest one is 44μm x 43μm with 2,400 polygons. The fracturing with the highest fidelity reduces the shot count by 12-14% compared to the non-overlap commercial package and only a minor degradation in fidelity. The fracturings with the lowest shot count reduces the shot count by 37-47% but a much larger degradation in fidelity with the WAEPE increasing from 0.3nm up to 1.03nm; nevertheless, the weighted average EPE is barely above 1nm. Our algorithm is able to create fracturings that are competitive with a commercial package in both shot count and WAEPE.

9052-21, Session 5

11nm logic optical lithography with OPC-lite

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The CMOS logic 22nm node is being done with single patterning and a highly regular layout style using Gridded Design Rules (GDR). Smaller nodes will require the same regular layout style but with multiple patterning for critical layers. A “line/cut” approach is being used to achieve good pattern fidelity and process margin.[1] As shown in Fig. 1a, even with “line” patterns, pitch division will eventually be necessary.

For the “cut” pattern, Design-Source-Mask Optimization (DSMO) has been demonstrated to be effective at the 20nm node and below.[2,3,4] Single patterning was found to be suitable down to 16nm, while double patterning extended optical lithography for cuts to the 10-12nm nodes. Design optimization avoided the need for triple patterning. Lines can be patterned with 193nm immersion with no complex OPC. The final line dimensions can be achieved by applying pitch division by two or four.[5]

To address mask complexity and cost, OPC for the “cut” patterns was studied and relatively simple OPC was found to provide good quality metrics such as MEEF and DOF.[2,3,4] This is significant since mask data volumes of >500GB per layer are projected for pixelated masks created by complex OPC or inverse lithography; writing times for such masks are nearly prohibitive.

In this study, we extend the scaling using simplified OPC to the 11nm node for the contact pattern. This layer is traditionally very difficult since it connects one upper layer (metal-1) to two lower layers (diffusion and gate). The test block is a reasonably complex logic function with ~100k gates of combinatorial logic and flip-flops.

Simulation results show that 11nm contact patterns should be possible with optical lithography and double patterning at 46nm gate and 32nm metal-1 pitches. An example of double patterning coloring is shown in Fig 1b.

Experimental demonstration of the contacts using design optimization, OPC-Lite, and conventional illuminators at the 11nm node dimensions will be presented. Lines were patterned with 193nm immersion with no complex OPC. The final line dimensions were achieved by applying pitch division twice.[5]

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9052-22, Session 5

Model-based OPC using the MEEF matrix II

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We begin with recalling the principles that are used in the traditional OPC algorithms. The primary goal of model-based OPC is to minimize EPE

(Edge Placement Error). In reality, most full chip level OPC algorithms are based on a simple linear approximation to the change of EPE of a particular fragment, i-th fragment, with respect to a mask displacement F(n)_i of the i-th fragment, from the n-th OPC iteration to the (n+1)-st: EPE(n+1)_i=EPE(n_i + S(n)_i*F(n)_i where S(n)_i is a scalar converting factor from an incremental mask fragment movement to its impact on the contour change. After the n-th iteration, the EPE associated to the i-th fragment EPE(n)_i is known. With a carefully selected or calculated converting factor S(n)_i, we can then directly calculate the needed incremental mask displacement F(n)_i of the fragment by setting the EPE(n+1)_i=0 in the above equation. In order to improve EPE convergence, one can use various sophisticated methods to gauge EPE of a fragment and to estimate the converting factor for this fragment. Such methods, like Calibre's process window aware OPC operations and Calibre's feedback controller options, are proven effective for production. However, the simplicity of the traditional algorithms is coming at a price. It purposely ignores the fact that the change of the contour at any given measuring site on the wafer is actually a collective result of moving all fragments on the mask nearby. This cost starts to show up in the 28nm node technology and beyond. We have seen cases where a neighboring fragment may contribute more to a particular EPE than its corresponding fragment does. To address aforementioned limitations, we recall and continue Nick Cobb and Yuri Granik's work [1] on matrix OPC which was carried out to address the problem in neighboring fragments aware OPC. They defined a meef matrix in terms of partial derivatives of resist profile at evaluation points on a wafer along the normal direction of a fragment of the target layout, with respect to incremental displacement of fragments on mask. We call such a directive a cross-meef, and denote the meef matrix by M={meef(i,j)}, where i means the ith evaluation point on the wafer and j the jth fragment on the mask. We further denote by F={F(j)} the vector of the incremental displacements of all fragments on the mask and by E={E(i)} the vector of the EPE changes at all evaluation points on the wafer in response to the mask movement F. Our matrix OPC approach is then based on the linear approximation E=M*F to the non-linear transformation from a mask change F to a change in wafer contours gauged by EPEs. The mathematical derivation of this linear approximation can be found in Mentor's earlier research work [1] on matrix OPC. There have been reports showing that such linear approximation is reasonable and effective in real cases. The novelty of this paper advances the existing work in several ways, with implementation of a new flow of carrying out matrix OPC in a wake of demands by the the 20nm technology node and beyond. In summary, our experiments with real layout clips, show the following: * The proposed approach improves EPE convergence with fewer OPC iterations in terms of the RMS and of the worst EPE. * It is fully compatible with all Calibre's existing, in-use OPC techniques and algorithms, including MRC solvers, nominal condition OPC, PWOPC, tagging techniques, and tiling algorithms. * It can be used with resist models and 3D mask models. * The run time addition is reasonable and tolerable for full chip applications.

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9052-23, Session 6

Immersion lithography extension to sub-10nm nodes with multiple patterning

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Immersion lithography with 193 nm exposure light continues to be the only means for the high volume manufacturing of critical layers in the semiconductor industry. Recently, SADP (self aligned double patterning) techniques have been used to realize sub-20 nm half pitch patterns of memory and logic devices.

A major question arises whether further multiple patterning techniques such as SAQP (self aligned quadruple patterning) or SAOP (self aligned octuple patterning) can be made useful for memory and logic devices to enable us to reach sub-10 nm half pitch patterns

To investigate the feasibility, this paper will show experimental demonstrations of sub-10 nm patterning using 193 nm immersion lithography and multiple patterning techniques. We show the formation of lines and spaces with half-pitches of ~13 nm and half-pitch patterns of 9 – 6 nm by SAQP and SAOP techniques. We will also show how to apply cutting lithography technology to the lines and spaces.

For the cutting, the narrow pitch of cutting holes is an issue for optical lithography. Simple extension of LELE (Litho-Etch-Litho-Etch) method for cutting hole pattering will requires LELELELELELE = (LE)^6 or more LEs in the sub-10 nm region. However, this is not realistic scenario when costs are considered. Instead, we investigate the feasibility of cross-SADP (SADP in the x and y directions) and other techniques for generating cutting holes on predetermined grid points, and trim exposures to select the holes.

For this experimental demonstration, we use Nikon S622D immersion scanner with highest level overlay accuracy and Tokyo Electron cutting edge process tools (LITHIUS Pro-i, Tactras and TELINDY PLUS IRad).

In addition to covering the technological aspects of the sub-10 nm node using these multi-patterning schemes, this work will also discuss the cost issues as compared with other potential solutions.

9052-24, Session 6

Hybrid lithography for triple-patterning decomposition and e-beam lithography

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As we advances into 14/10nm technology node, single patterning technology is far from enough to fabricate the features with shrinking feature size. According to International Technology Roadmap for Semiconductors in 2011, double patterning lithography is already available for massive productions in industry for sub-32nm half pitch technology node. For 14/10nm technology node, double patterning begins to show its limitations as it has to introduce too many stitches to resolve the native conflicts. Stitches will increase the manufacturing cost, lead to potential functional errors of the chip, and cause the yield lost. In practice, people always want to minimize the number of stitches to make the lithography process more reliable and productive.

Triple patterning lithography (TPL) is a natural extension for double patterning lithography, which adopts one more mask to accommodate all the features in a layout, and potentially reduces most of the stitches introduced by double patterning lithography. However, for complex designs, stitches for TPL are inevitable to resolve coloring conflicts. For some TPL unfriendly designs, even with stitches, the layout cannot be decomposed into three masks. There have been many TPL related works discussing about TPL decompositions algorithms and stitch minimizations. People are beginning to discuss quadruple patterning for some TPL unfriendly designs. However, the cost to introduce one more mask is high. Solutions combining the merits of different lithography techniques, and having reasonable cost and productivity will be more welcomed in practice.

E-Beam is a well-known powerful technique to fabricate various "hard" layouts, where traditional immersion lithography technique fails. It is a maskless lithography where the desired patterns are directly ejected into the wafer with a charged particle beam. It is one of the emerging technologies to beat the diffraction limit for current optical lithography system. What hurdles the E-Beam lithography from being used in practice is its low throughput. Different from traditional immersion lithography, where all the features can be printed once the masks are ready, different features have to be printed sequentially using E-Beam

lithography.

In this paper, we investigate combining the merits of triple patterning lithography and E-Beam lithography for complex standard cell based layout. We devise an approach to optimally identify all the “hot spots” that need stitches, or the locations that are not TPL decomposable. After that, these hot spots are classified according to different patterns (characters). The character projection (CP) E-Beam lithography can be used to fabricate some or all of these patterns, with the tradeoff of throughput and cost specified by chip designers. The cost of using TPL decompositions with stitches, TPL decompositions combined with E-Beam without stitches, and TPL decompositions combined with E-Beam with limited number of stitches are thoroughly discussed and compared. The approach runs in polynomial time, and is expected to highlight the advantages of using hybrid lithography for advanced technology node.

9052-25, Session 6

Metal1 patterning study for random-logic applications with 193i, using calibrated OPC for litho and etch

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We have used a Metal1-layer test block (related to N20 and N10 random-logic applications), to study a number of fundamental issues that are important with respect to final-pattern fidelity and through Process-Window (PW) robustness. N20 and N10 correspond to Poly/Metal1 pitches of 90/64nm and 64/48nm respectively, where N20 uses planar technology and N10 uses FinFet technology. As the effects of etch are more complicated than imposing a single uniform bias on the after-litho pattern, our study includes evaluation both after-litho and after-etch. We have primarily concentrated on Metal1, but additional work has also been done on Via0 and Local-Interconnect (LI) layers, especially to investigate triple-patterning decomposition.

This work focuses on the following key elements:

1. Automated multi-patterning decomposition for Double & Triple patterning applied on bidirectional (2D) Metal1, non-uniformly distributed Via0 and unidirectional (1D) LI.

2. Assist (SRAF) placement solutions, considering both Rule-based and Model-based SRAF approaches. We also looked into assist printability, including whether and how printing assists are transferred after etch.

3. (Calibrated) Model-based OPC, where a resist OPC model has been calibrated and verified at nominal and through PW conditions. Also at the etching stage, we followed a model-based OPC approach.

4. Computational PV-band evaluation, hot-spot detection analysis, and printability optimization. Through-focus performance predicted by the OPC-software has been complemented with results from a rigorous lithography simulator (also using a calibrated resist model). These computational predictions will also be compared to experimental data.

5. On-wafer analysis (for Metal1), through PW and including variation of some of the critical design rules, as for example pitch or gap sizes. The on-wafer evaluations made use of SEM-image contour metrology (next to traditional CD-SEM measurements), which we found particularly useful for 2D-type patterns.

In this paper, we will give an overview of our results, and conclude on the best approach we obtained for the items listed above. This study should also provide some insights in whether and how current patterning solutions at 193i can be extended to still smaller dimensions and pitches.

9052-26, Session 6

Pattern fidelity in multiple-patterning process

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Advances in patterning techniques have enabled the extension of 193-immersion lithography to sub-20nm technology node. Double-patterning techniques, especially Self-aligned type DP process, have become nominal process for fine pattern fabrication below resolution limit of 193 immersion as EUV is not yet ready for high volume production. The challenge remains in the refining of pattern fidelity on smaller pattern through Self-aligned multiple patterning. LER on core-pattern in SADP is most important category to control CD uniformity (CDU). CDU on line pattern is relatively stable, however, pitch-walking often occur in SADP process. We found in previous study that LER on core-pattern affected strongly on CDU, and realized enough minimized CDU on SAQP by using ultimate low LER resist for core-pattern [1]. Furthermore, and smoothing was quietly effect to improve local CDU[2].

In this paper, we will report that realistic observation methodology of LER behavior and robust technique for smoothing to gain enough good CDU through Self-aligned Multi-Patterning.

9052-27, Session 6

Joint optimization of source, mask, and pupil in optical lithography

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In ultra low-k1 era of optical lithography, one primary limitation of process window is the noticeable difference in best focus (BF) among various feature sizes. Rigorous 3D mask experiments have confirmed that mask topography is a leading cause due to the fact that the thickness of the mask absorber produces phase errors among different diffraction orders.

Unfortunately, the rigorous electromagnetic field (EMF) modeling used to describe light diffraction from the mask generally involves intensive computation, which limits the wide adoption of rigorous 3D mask modeling for practical large layout simulations in advanced resolution enhancement techniques (RETs) such as source and mask optimization (SMO). Additionally, although SMO is a powerful and effective technique which provides more flexibility regarding both the mask design and illumination configuration adjustment, it is inadequate to control the phase in the lens pupil. In order to compensate for the phase errors induced by mask topography effects, additional degrees of freedom are required in terms of phase manipulation, namely to incorporate the phase parameter into source and mask optimization.

In this work, a combined source, mask and pupil optimization (SMPO) approach is developed as an alternative to maximize the process window. The proposed scheme takes advantage of the fact that pupil phase manipulation can partially compensate for thick mask topography effects. We first design the pupil wavefront function by incorporating primary spherical and astigmatism aberrations through the Zernike polynomials, since these two aberrations have a large impact on linewidth through focus. We treat the aberrations as independent, normally distributed random variables, so the Zernike coefficients are determined by the statistical probability of aberration terms appearing over a range as the phase control and adjustment. This caters for not only the nominal condition or certain aberration but optimizes over a range of variations. Next, the objective function takes expectations of a weighted sum of the nominal and the aberration terms to optimize the average performance of layouts. We apply nonlinear conjugate gradient algorithm to achieve optimal source-mask pair under the condition of aberrated pupil. To evaluate the performance of the proposed SMPO algorithm, we apply it to 1D lines/spaces pattern with different pitches of vertical and horizontal configurations, as well as to 2D features, and compare the optimization

results with the SMO with ideal pupil. The following figures present one of the results. It is observed that the proposed method leads to better performance with a) fewer pattern errors, particularly under the circumstance of spherical aberration, as shown in Fig. 1 and Fig. 2; and b) larger average exposure-defocus window, as illustrated in Fig. 3.

9052-28, Session 6

Efficient source polarization optimization for robust optical lithography

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As the critical dimension (CD) of integrated circuits shrinks into the deep sub-wavelength realm, semiconductor industry has to rely on low-k1 optical lithography to further improve the lithographic resolution. Source optimization (SO) technique is one of the key resolution enhancement techniques (RET) to modify the intensity distribution of light source. SO methods can be either applied independently or combined with the mask optimization giving birth to the source-mask-optimization (SMO) methods.

Recently, the pixelated sources with flexible profile and intensity were realized by the development of freeform diffractive optical elements (DOE). Consequently, a set of pixelated SO and SMO approaches were proposed to enhance the lithographic imaging performance. However, these prior SO and SMO methods fell short to take into account the polarization optimization (PO) thus limiting the degrees of freedom during the optimization procedure.

Source polarization was proven having considerable influence on the illumination optimization and lithographic imaging performance. Hansen first introduced the polarization variables into the SMO flow to develop a source-mask-polarization -optimization (SMPO) approach. Although effectively extending the dimension of solution space, Hansen's method had three inherent drawbacks. First, this method was based on a scalar imaging model, which is no more accurate enough for lithography simulation with numerical aperture (NA) larger than approximately 0.6. Second, this method applied a non-analytic and discrete SMPO algorithm, so that difficult to approach the global optimum. Finally, this approach was a trial and error method that decided the variable updates based on the imaging performance evaluated on different imaging planes. Thus, this optimization strategy led to slow convergence and time-consuming calculation.

To overcome these limitations mentioned above, this paper develops a pixelated gradient-based polarization optimization approach to improve the robustness of the lithography systems to the process variations, thus extending the process windows (PW). It is noted that the proposed PO algorithm could be applied independently or potentially inserted into the current SMPO flow. The proposed PO framework is formulated using a vector imaging model, which is capable of explicitly incorporating the polarization variables, as well as effectively improving the simulation precision. A forward optimization algorithm is used to iteratively modify the polarization angles, while the gradient of the cost function is used to navigate the optimization directions. In order to maintain the manufacturability, the polarization angles are imposed to be selected from several discrete levels. A post-processing method is also developed to further reduce the complexity of the optimized polarization angle patterns.

Another contribution of this paper is to develop an efficient cost function for the optimization framework to speed up the proposed PO algorithm. The proposed cost function is designed as the square of Euler distance between the modulated target pattern and the average aerial image over a certain defocus range. Due to its computational simplicity, the proposed PO algorithm will achieve two-fold speedup compared to the method using a traditional cost function. Simulations illustrate that the proposed PO algorithm can effectively improve the PWs of the lithography systems, and exhibit superior convergence efficiency.

9052-29, Session 7

Characterization and mitigation of overlay error on silicon wafers with nonuniform stress

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Process-induced overlay errors are a growing problem in meeting the ever-tightening overlay requirements for integrated circuit production. While uniform process-induced stress is easily corrected, non-uniform stress across the wafer is much more problematic, often resulting in non-correctable overlay errors. Measurements of the wafer geometry of free, unchucked wafers give a powerful method for characterization of such non-uniform stress. We will describe an optical metrology tool which can measure the geometry of in-process wafers. Wafer geometry data can be related to In-Plane Distortion (IPD) of the wafer pulled flat by an exposure tool vacuum chuck, which in turn relates to overlay error. This paper will explore the relationship between wafer geometry and overlay error by deliberately creating stress variations on silicon wafers that we term Engineered Stress Monitor (ESM) wafers. A process has been described [1] that allows the creation of ESM wafers with nonuniform stress and includes many thousands of overlay targets for detailed characterization of each wafer. Because the spatial character of the stress variation is easily changed, ESM wafers constitute a versatile platform for exploring non-uniform stress. Fig. 1 shows results from an ESM wafer where the center area is under higher stress than the outside area. Fig. 1a shows Predicted Residual Overlay errors derived from wafer shape measurements, while Fig. 1b shows the residual errors measured from actual overlay data. The qualitative agreement between Figs 1a and 1b demonstrate the potential for using wafer geometry measurements to characterize process-induced overlay problems. We have taken this idea further by using the wafer shape derived data to improve overlay error by novel feed-forward to the exposure tool. We conclude that appropriate wafer geometry measurements of in-process wafers have strong potential to characterize and reduce process-induced overlay errors.

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9052-30, Session 7

Analysis of overlay errors induced by exposure energy in negative-tone development process for photolithography

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Endless challenge to make device smaller, faster, and more efficient always spurs lithography equipment manufactures to develop more advanced lithography tool. However, the next generation lithography technologies such as extreme ultraviolet, X-ray proximity printing and electron beam still have not been mature to use in mass production. Naturally, the ArF immersion lithography era has been continuing and its applications have been developed to overcome the current technical challenges. One of most promising application technology, negative tone development (NTD) process with positive resist and organic solvent-based developer enhances image contrast and uses a light-field mask to make same feature in opposition to positive tone development (PTD). Due to extremely high transmission rate of a light-field mask, absorption of exposure energy on a mask becomes imperceptible. However, the exposure energy transmitted through the mask influences

not only lens heating but also wafer heating. Overlay budget by wafer heating becomes a considerable amount in NTD process. In this paper, to clarify overlay change induced by wafer heating in NTD process, five different levels of exposure energy are applied and the overlay errors are deteriorated by increasing energy. Due to wafer heating, the remarkable correlation between Y-overlay errors and scanning direction are observed. Especially, Ty, RK8, and RK12 have mostly considerable correlation with scanning direction. In NTD process, to avoid this phenomenon, exposure energy has to be minimized. In case scanning direction dependency in overlay is not prevented by minimization of exposure energy, fingerprint correction in wafer field is able to reduce this overlay error.

9052-31, Session 8

Hybrid OPC modeling with SEM contour technique for 10nm node process

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Hybrid OPC modeling uses both CDs from 1D line and space patterns and contours extracted from complex 2D patterns was measured by a Critical Dimension-Scanning Electron Microscope (CD-SEM). Recent studies have addressed some of key issues needed for the implementation of contour extraction, including methods for contour averaging, contour alignment, and image quality of the contour. In this study, pattern contours obtained from CD-SEM images were used to complement traditional site driven CD metrology for the calibration of OPC models for the 10 nm node, developed in Albany Nano-Tech. The performance and accuracy of this model were compared with that of conventional OPC model, which was created with traditional CD metrology. Model stability and pattern specific benefit of contour modeling was examined.

Accuracy of the model was defined as total error root-mean-square (RMS). RMS was calculated by a combination of CD error RMS and Contour error RMS, assuming a given weighting, as shown in equation (1), (2) and (3). As a result, total error RMS was improved from 4.9 nm to 4.6 nm by hybrid modeling. CD error RMS of hybrid modeling was 5.6 nm, which was almost same as conventional modeling (5.4 nm). On the other hand, contour error RMS was much improved from 4.3 nm for the conventional model to 3.2 nm for the hybrid model. In conclusion, accuracy of OPC models for the 10 nm node can be improved by using pattern contours obtained from CD-SEM image. Additionally, hybrid models exhibited smaller difference between optical and resist images.

9052-32, Session 8

Improving 3D resist profile compact modeling by exploiting 3D resist physical mechanisms

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The useful depth of focus has become comparable to the resist film thickness as the 193nm immersion deep UV lithography technique is pushed to its resolution limit, with a consequence that the resist profiles may deviate from ideality. In some weak image areas, serious resist top loss or footing often occur, which, in turn, can result in killing defects in the subsequent etch processes. Since conventional 2D OPC modeling does not handle 3D resist profile, the phenomenon and practical needs have spurred extensive research activities in the past few years to simulate 3D resist profiles with compact models for full-chip OPC applications. The reported approaches more or less borrow the physical mechanisms in rigorous optical lithography models which include 3D resist profile simulation but runs too slow for full-chip applications. A simple approach is to build individual 2D models at different image depths either based on actual wafer measurement data or virtual simulation data by an already calibrated rigorous lithography model. Application of any of the individual 2D models to downstream OPC/LRC tools is straightforward. However, the relevant image depths need be determined in advance due to the discontinuity nature of the methodology itself. The physical commonality among the individual 2D models may deviate from each other as well during the separate calibration processes. A second approach assumes that the 3D resist profile formation is dominated by optical image variation across the resist film thickness while resist material properties specific to height position are ignored. Despite its simplicity, it's prediction on 3D resist profile may be inaccurate when resist materials property is not uniform, especially when surface effects are not negligible.

The aforementioned drawbacks were addressed in this work by adopting more physical simulation mechanisms from rigorous simulation methodologies while keeping the model form compact for full-chip applications. To that end, the bulk image is calculated by using one set of retained Hopkins kernels. Optical intensity can be assessed at any image depth without accuracy compromise. With an accurate bulk image, a simplified model for chemically amplified resist is used to simulate resist behavior. The resist models contains acid generation, acid-base neutralization, lateral and vertical diffusion. Boundary conditions at the resist interface used to account for surface effects. The model is formulated in a continuous form so that a model slice at any image depth is readily available to use after calibration. While the calibration data is collected with discrete image planes, all planes are calibrated simultaneously using one set of resist parameters to guarantee physical commonality among them. Moreover, the calibration is done stepwise carefully to ensure the optical part to account for optical effects and resist model to account for resist effects. The calibrated model is compared against the rigorous model, showing that critical resist profile failures can be successfully predicted. In addition to regular model validation process, a measure of resist model separability is used to judge resist model quality. It is shown that the resist model can be carried to a different lithography process with same resist setup but a different illumination source without model noticeable accuracy degradation. The work shows that the accuracy of compact 3D resist models is improved by adopting more physical resist mechanisms.

9052-33, Session 8

Resist profile simulation with fast lithography model

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A traditional approach to construct a fast lithographic model is to match wafer top-down SEM images, contours and/or gauge CDs with a TCC model plus some simple resist representation. This modeling method has been proven and is used extensively on OPC models. As the technology moves forward, this traditional approach has become insufficient in regard to lithography weak point detection, etching bias prediction, etc. The drawback of this approach is from metrology and simulation. First, top-down SEM is only good for acquiring planar CD information. Some 3D metrology such as cross-section SEM or AFM is necessary to obtain the true resist profile. Second, the TCC modeling approach is only suitable for planar image simulation. In order to model the resist profile, full 3D image simulation is needed.

Even though there are many rigorous simulators capable of catching the resist profile very well, none of them is feasible for full-chip application due to the tremendous consumption of computational resource. The authors have proposed a quasi-3D image simulation method, which is suitable for full-chip simulation with the consideration of sidewall angles,

to improve the model accuracy of planar models.

In this paper, we extend the quasi-3D image simulation to directly model the resist profile with AFM and/or cross-section SEM data. Resist weak points detected by the model generated with this 3D approach are verified on the wafer. The application to etching bias prediction will also be covered.

9052-34, Session 8

Modeling the lithography of ion implantation resists on topography

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With emerging technologies, such as fin-based field-effect transistors (finFETs [1]), the structures which define the functionality of a device have added one dimension in the patterning and are now three-dimensional. In the case of finFETs, the fins stand up from the insulating substrate such that the gates are wrapped around them (figure 1). The benefit lies in the improved electrical performance of the transistor channel compared to a planar case where the active area is coplanar with the field oxide. One major drawback, however, lies in the CMOS patterning, where any CMOS ion implantation patterning needs to selectively expose alternate fins to allow for p- and n-doped regions. The ion implantation mask is usually a photo-developable resist, much like the photoresists used in etch patterning. This resist needs to print over topography, and fully clear the fins that are to be implanted. To date, very few resist models take dense topography and interaction with different materials into account.

In this paper we present resist models on topography with relevant materials and dimensions for finFET devices compatible with nodes down to 10 nm. We investigate the influence of different materials and of the additional optical complexity due to the topography and density of the gates and fins.

9052-35, Session 8

Analytical etch modeling and correction for highly polymerizing processes in sub-2x CMOS nodes

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Resolution Enhancement Techniques compensate process related deformations induced by lithographical and etch steps. A lot of efforts were spent on the accurate prediction of the lithographical steps which allowed the fast development of performing OPC engines, the creation of advanced model forms for optical systems and resists, and the integration of second order effects such as flare, mask thickness, film stack dependence… On the other hand little developments have been done for etch compensation whereas such effects weighs on the CD control budget. More precisely 2-dimensional environments have an increasing influence on the CD of a specific line. The direct 1-dimensional environment described by a CD, space couple is no longer sufficient to predict accurately the etch effect.

Based on data measured on 28nm silicon at Shallow Trench Isolation (STI) etch step, we show the limitations of the traditional table driven approach by exhibiting some common 2-dimensional design configurations where CD errors can be very large. We explain why these limitations are intrinsic to the table-based correction and that a change in methods is necessary to accurately compensate etch process in sub 2x technology nodes.

Based on the same dataset, we introduce a new method for building a simple analytical model that accounts for all 1-dimensional structures with minimal error. Then we present a method to implement this model in an effective OPC flow compatible with production requirements. The flow is optimized for runtime and hierarchy conservation. The accuracy of our model is finally verified on a selection of 2-dimensional designs and its quality is compared to that of the standard approach.

9052-37, Session 9

Fast detection of novel problematic patterns based on dictionary learning and prediction of their lithographic difficulty

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As the semiconductor technology feature sizes shrink to follow Moore's law, the complexity of the lithography process increases, making the screening for problematic design patterns tedious and thus prone to incompleteness. The design rules become more difficult to establish and check, and can be too restrictive for efficient design and still be missing patterns. Early detection of novel patterns is a critical aspect of the design space coverage testing. Pattern matching approaches proposed as alternatives ([1]-[5]), suffer from a lack of generalization and require a very large collection in order to cover the space.

In this paper we demonstrate that an overcomplete basis (dictionary) can be learned to represent the reference patterns sparsely and allow to detect novel patterns as the ones that cannot be expressed sparsely in that basis. We furthermore provide a compressed representation of the patterns, which can be recovered using few linear combinations of measures obtained from a sensing matrix incoherent with the learned dictionary. The computational complexity for testing a new pattern boils then down to O(s K p), with s the sparsity level, K the dictionary size and p the measures sensed, whereas traditional nearest neighbor search is O(N d), with N the number of reference patterns and d their dimension.

To detect the problematic patterns, we subsequently use a new technique that uses active learning ([6], [7]) to progressively sample the novel patterns, and to select the minimal set needed to predict hotspots, ensuring optimal sampling density. We estimate the boundary of failure regions using a classification formulation, where Gaussian processes ([8]) are used to model the underlying printing difficulty function. The algorithm learns a set of patterns whose printing difficulty lie above or below a certain threshold of this underlying function by sequentially sampling candidate patterns that are highly ranked according to a scoring function. This process refines the boundary between failing and non-failing regions. By providing for every pattern its distance to the boundary and confidence bounds, it can estimate failure region sizes and the minimum distances between patterns across the boundary.

In experiments, a dictionary is learned using a selected macro (ABC) and then sparse coding, using this dictionary, is performed on another macro (DEF). A reconstruction error for the DEF patterns larger than the maximum reconstruction error of the ABC patterns flags them as "novel" (Figure 1). Figure 1 also illustrates that, compared to exact matching, our approach can provide up to 1000x speedup in testing.

Gaussian processes model either ORC hotspots or Litho Difficulty Estimator (LDE [9]), as they exhibit high correlation. The LDE threshold at which patterns start failing can be discovered using the conditional probability distribution of ORC hotspots given LDE. The selected threshold yields a low miss rate of 3.34%. From the whole dataset, only 14.93% of the data is needed to predict ORC hotspots with an F1-score of 95% (Figure 2, left). Using LDE we reduce the sampled data to 6.35% (Figure 2, middle). When using the random scoring function to emulate the traditional classification methods we need 53.77% of the data (Figure 2, right).

9052-38, Session 9

Pattern-based full-chip process verification

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This paper discusses a novel pattern based standalone process verification technique that meets with current and future needs for semiconductor manufacturing of memory and logic devices. The choosing the right process verification technique is essential to bridge the discrepancy between the intended and the printed pattern. As the industry moving to very low k1 patterning solutions at each technology node, the challenges for process verification are becoming nightmare for lithography engineers, such as large number of possible verification defects and defect disposition. In low k1 lithography, demand for full-chip process verification is increasing. Full-chip process verification is applied post to process and proximity correction (PPC) or optical proximity correction (OPC) steps. The current challenges in process verification are large number of defects reported, disposition difficulties, long defect review times, and no feedback provided to PPC or OPC. The technique presented here is based on pattern based verification where each reported defects are classified in terms of patterns and these patterns are saved to a database. Later this database is used for screening incoming new design prior to PPC or OPC step.

As shown in Fig.1, process verification technique presented in this paper consists of three major flows: a. conventional PPC or OPC verification of post PPC or OPC layout, b. pattern classification of 3rd party defect locations (markers), and c. pattern matching of critical patterns with pre-PPC or pre-OPC layout (equivalently extension of design rule check). Figs. 2 and 3 show the results of pattern based classification and disposition.

In summary, the novel technique presented here has many applications in semiconductor manufacturing including but not limited to standalone OPC verification, pattern based disposition of printed wafer inspection results, etc. In this paper, we present several different flows of pattern based process verification.

9052-39, Session 9

Characterization of 1D layout technology at advanced nodes and low k1

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I. GRIDDED D ESIGNS AND THEIR IMPLEMENTATIONS

Highly regular gridded designs have been widely adopted [1] as a key component for continued advances in lithographic resolution in an era of limited progress in lithography hardware. With a given process technology tool set, higher pattern density (lower k1) and quality are achieved using gridded design rules (GDR) in comparison to conventional 2D designs. GDR is necessary for designs with k1 approaching the theoretical Rayleigh limit ? 0.25.

A highly effective implementation of GDR is the lines+cuts approach discussed in [2], [3], [5] and elsewhere. As shownin Fig. 1, excellent results at very advanced nodes can be achieved by this double-patterning process, where lines are created first, then cuts are patterned on top as required by circuit connectivity. A specialized optical proximity correction tool called OPC-Lite [4] is used to achieve good CD uniformity across all cuts.

An alternative approach is also possible, where lines are pre-cut as needed and patterned in a single step. The advantage is a simpler and less expensive process, achieved at the cost of some reduction of resolution and pattern fidelity Fig. 2. As inthe case of Lines+Cuts we use OPC-Lite [4] to compensate for proximity effects. Unlike Lines+Cuts, in case of pre-cut lines we have to deal with linewidth variation and line-end pullback.

Both can be minimized but not completely eliminated with OPC-Lite.

II. EXPERIMENTAL VERIFICATION

In the final paper we will present experimental results for 1D GDR designs using pre-cut lines at k1 values ranging from 0.6 to 0.276 corresponding to 45nm to 20nm nodes at ArF NA1.30. Based on our simulations and OPC we expect to achieve good pattern quality and manufacturabilty. The precut lines approach to GDR will likely show somewhat lower resolution in comparison to double patterning Lines+Cuts.

III. SUMMARY AND CONCLUSIONS

We presented an alternative implementation of 1D GDR,which uses a single patterning step to define pre-cut lines. With the use of OPC-Lite, high pattern quality at low k1 values is expected. In comparison to the Lines+Cuts approach to 1D GDR, the pre-cut lines alternative offers lower process complexity and cost at somewhat diminished capability. This tradeoff may be of interest to some manufacturers under certain equipment set and cost constraints.

9052-40, Session 10

Rigorous and fast simulation method for electromagnetic light-scattering computations with complex illuminations

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In computational metrology and computational lithography a rigorous simulation of light scattering off masks or patterned wafers becomes more and more urgent.

This is due to shrinking feature sizes and increasing accuracy demands. Prominent computation methods for such near field simulations are RCWA, FDTD and FEM (finite elements). Often, costly near field simulations are required for a large number of incidence angles. To keep the numerical effort reasonably small one typically performs a rigorous computation for a small number of incidence directions only. The optical response of the entire illumination is then obtained by interpolation techniques such as the non-local Hopkins approach or other higher order interpolation schemes. However, to satisfy the more and more challenging accuracy demands the number of required near field simulations is constantly growing to sample the entire illumination pupil correctly.

In this paper, we propose a new method based on FEM which allows to keep the numerical effort small even for high numbers of incidence directions. The key idea is to numerically treat the unit cell of the periodic structure as an isolated scatterer at first. The periodic solution can then be gained by an iterative coupling of the field over the originally periodic boundaries of the unit cell. The numerical advantage of this approach is that only a single assembly and decomposition of the isolated scatterer is required independently of the incidence direction. This reduces the overall memory and cpu usage immensely.

9052-41, Session 10

Availability study of extended and CFD-based mask 3D model for next-generation lithography technologies

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In next generation lithography technologies using high NA lithography tools, the importance of Mask3D analysis method increases more and more because the explosive increase of effects of structure on mask is not avoidable. To analyze that complicated phenomena, an electromagnetic filed simulation method is applied, such as FDTD, RCWA and FEM. The complex structure of mask increases the computation time of traditional simulation method with spatial grids due to the restriction of the grid shape for satisfying the calculation precision.

We have investigated a CFD-based and explicit method, which is based on the Constrained Interpolation Profile (CIP) scheme, for Mask3D analysis in optical lithography. This scheme is characterized by high accuracy to maintain the phase of propagating waves with less phase error from numerical dispersion. The CIP scheme can reduce the number of grid points in complex structure because the restrictions of grid distance are relaxed rather than other methods with spatial grid. Therefore, the CIP scheme can also reduce the calculation time of EUV mask topography simulation efficiently by using sparse grid.

In this paper, we study the feasibility of CIP scheme applying a non-uniform and sparse grid structure to the convex-structured multilayer. Finally we propose how the grid generator can reduce the number of grid points especially in EUVL mask topography simulation.

9052-42, Session 10

Rapid, accurate improvement in 3D mask representation via input geometry optimization and crosstalk

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We report an approach to improve the performance of 3D mask models relative to thin mask models based on a physical perturbation of the input mask geometry. We show that small, direct modifications in the input mask stack slope, edge location, and corner rounding can result in model calibration and verification accuracy benefit of up to 30%; in all cases exceeding the accuracy of the thin mask alternative. The methodology is demonstrated on 4 test cases from 20nm generation layers and below, for both hole layers and primarily line and space layers. All final mask optimization results from this approach are shown to be valid within measurement accuracy of the dimensions provided by the manufacturer. We highlight the benefits of a more accurate description of 3D EMF crosstalk in model calibration and impact as a function of mask dimensions. The result is a useful technique to align 3D mask model accuracy with physical mask dimensions and scattering via model calibration.

9052-43, Session 10

Fixing the Focus Shift Caused by 3D Mask Diffraction

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As smaller and smaller features are printed with optical lithography for advanced nodes Kirchhoff's thin mask approximation used for OPC does not provide an acceptable accuracy anymore due to diffraction effects on the thick mask. One of the most observed effects of the thick mask diffraction is the focus shift it creates for different patterns. When bossung curves (CD plots with respect to focus) of various patterns are observed from rigorous simulations or from actual wafer data one can notice that each pattern has a different focus center. Some patterns may have bossung curves that are shifted to the right and others may be shifted to the left (Figure 1). This significantly reduces the common depth of focus (DOF) for which all patters will print with acceptable dimensions. Even though each pattern by itself has an acceptable DOF, the common DOF may not be acceptable.

Several extensions to the thin mask approximation have been developed that model this behavior accurately, such as boundary layer approximations and domain decomposition methods. These methods provide a more accurate approximation than the thin mask model while still computationally efficient to be used for full chip optical proximity corrections (OPC). Even though these approximations model and predict the focus shift accurately, to the best knowledge of the authors no method have been published to use these modeling capabilities to automatically fix this focus shift during OPC.

In this paper we provide an optimization method to fix the mask 3D induced focus shift during OPC. We will show that Cadence mask 3D model can predict this focus shift fairly accurately and we will show how we use this model in OPC to fix the focus shift. In this method we optimize sub-resolution assist features (SRAFs) using Cadence mask 3D model. SRAFs are optimized during OPC so that the final mask layout will have reduced mask 3D induced focus shifts, which significantly improves the common DOF for the entire layout (Figure 2).

9052-44, Session 10

Impact of topographic mask models on scanner matching solutions

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Of keen interest to the IC industry are advanced computational lithography applications such as Optical Proximity Correction of IC layouts (OPC), scanner matching based on optical proximity effect (OPEM), and Source-Mask Optimization (SMO) used as advanced reticle enhancement technique. The success of these efforts is strongly dependent on the integrity of the lithographic simulators used in computational lithography optimizers. Lithographic mask models used by these simulators and their interactions with scanner illuminator models are key drivers impacting the accuracy of the image predications, and as a consequence, the accuracy of the computational lithography solutions.

Much of the computational lithography work involves Kirchhoff mask models, a.k.a. thin masks models, simplifying the treatment of the image fields in the mask near field. On the other hand, rigorous imaging models for hyper-NA scanner require that the interactions of the fields with the mask topography be accounted for, by numerically solving Maxwell's equations. The simulators used to predict the image formation in the hyper-NA scanners have to rigorously treat the topographic masks and the interaction of the mask topography with the scanner illuminators. Such imaging models come at a high computational cost and pose challenging accuracy vs. compute time tradeoffs. Additional complication comes from the fact that the solution performance metrics used in computational lithography tasks show highly non-linear response to the optimization parameters. Finally, the number of patterns used for advanced computational lithography tasks such as OPC, OPEM, SMO range from tens to hundreds increasing. These requirements determine the complexity of the lithography optimization tasks. The tools to build first-principle imaging optimizers are available, but the quantifiable benefits they might provide are not very well understood.

To quantify the performance of OPE matching solutions, we have compared the results of various imaging optimization trails obtained with Kirchhoff mask models, to those obtained with rigorous, Finite Element solver of Maxwell's equations. In both sets of trails, we used pattern samples consisting of large number of patterns, representative of the computational lithography tasks commonly encountered in hyper-NA imaging. During these trails, we have adopted imaging conditions representative of the advanced scanner illuminators. We evaluated the topographic mask approach by comparing the OPE matching solutions obtained with simplified Kirchhoff model, to the results of rigorous

calculations involving topographic mask models.

In this report we present topographic OPE matching and discuss its impact on accuracy when used to optimize hyper-NA imaging. By comparing OPE matching results obtained under various conditions, we draw conclusion on the accuracy of topographic OPE matching vs. the results obtained with thin mask models. We present various examples representative of the scammer image matching for patterns representative of the current generation of IC designs.

9052-45, Session 10

Joint optimization of mask, optical, and photoresist models for computational lithography

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The computational models used for optical proximity correction for lithography include optical, mask, and photoresist models that correspond to components and process steps in lithographic wafer patterning. The optical models describing lithographic imaging are primarily based on the physical description of the optical system and the wafer film stack. Computational models of the lithographic mask involve the drawn pattern shapes with corner rounding and bias parameters to describe the mask patterning process and well as the physical description the mask, including the mask film stack information for three-dimensional electromagnetic field modeling. Owing to complexity of the resist exposure and development process, the computational models for the photoresist contribution to the final critical feature dimension are largely empirical, though the modeling algorithms emulate the observed photoresist behavior such as acid quenching and diffusion. The empirical parameters in the photoresist model are optimized to minimize the error between the measured and simulated critical feature dimensions.

Although it is generally desired to separate the contributions of mask, optical, and resist components to obtain a physically correct description of each and improve model extrapolation capability, in practice the complete model separability is not possible owing to model algorithm approximations and to uncertainties in the measurements of the physical parameters. Thus even with careful measurements of the mask corner rounding and film stack, the optical system, and the wafer film stack, the empirical portion of the overall model, i.e. the resist model, contains not only the intended photoresist patterning contribution but also mask and optical imaging effects. The traditional approach in determining the computational lithography model involves optimizing mask, optics, and resist parameters separately in “stages” by minimizing the error between measured and simulated feature dimension data. The drawback of this approach is that the final model may depend on the order in which the calibrations are performed and that the final model may not be globally optimum. In this work, a comprehensive model calibration approach is investigated where optical and mask parameters that are frequently compensated by the resist model parameters are jointly optimized along with the resist parameters. The model fit error to calibration data as well as model error on verification data that are not used in the optimization are compared for the two approaches. The calibrated mask and optical parameters obtained with both approaches will also be compared to measured values of the physical exposure process attributes that the model parameters are intended to capture.

9052-46, Session 11

Computational lithography platform for 193i-guided directed self-assembly

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The goal of this paper is to explore the computational lithography implications of DSA and the impact of DSA patterning schemes on Design For Manufacturing (DFM). There are many high quality 193nm DSA patterning papers that focus on regular patterns such as Line and Space (L/S) gratings or contact hole arrays. As an extension of our previous publications [1,2], we will emphasize computational issues related to patterning circuit-relevant design constructs for Lines & Spaces (L/S) as well as vias and to explore whether 193nm optical lithography can be used in conjunction with DSA as an viable Resolution Enhancement Technique (RET).

There have been many questions raised in the industry that are critical to answer in order for DSA to be accepted as a viable patterning technique. Some of the more important questions to answer are as follows: Are DSA patterning process windows are large enough to support high volume manufacturing; Can DSA be used to reduce mask counts observed in 193 immersion multiple patterning approaches; How can defect formation be minimized by using specific design strategies and computational lithography solutions; Finally, is it possible to adapt 2D compact to improve runtime but make them sufficiently accurate in three-dimensions to be useful for full chip pattern correction and verification?

In an attempt to answer some of these questions, we have built DSA test masks that are were generated using our internal computational lithography toolset. These test masks enable us to tune our algorithms and recipes for guiding pattern printing as well as to study 193nm-based DSA patterning through model validation macros and to assess whether particular design styles are more desirable. In this work, we will report on three main aspects of DSA patterning using results from our testmasks.

First, we focus on identifying the potential computational issues for DSA such as, the tradeoff of different full chip capable GP patterning correction approaches that will impact run time as well as accuracy; the tradeoffs between different versions of fast DSA models on accuracy, sensitivities to guiding pattern profiles and computational speed; the validity of a sophisticated 2D fast DSA model to replace rigorous 3D model in full chip prediction of DSA features and defects.

Second, we present wafer demo of DSA solution for circuit-relevant patterning of DSA via and L/S. Experimental wafers results from test masks are used to correlate modeling results and enable the calibration of fast DSA models to validate their predictive powers. It also allows us to study the tradeoff of printability as well as defect density dependence on design styles of circuit-relevant patterns and their design restrictions.

Last, we will also explore if there is any secondary physical/chemical effects of DSA patterning by characterizing special design macros in the DSA test masks. Feasibility of doing compact modeling of these effects will be discussed.

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9052-47, Session 11

Applying ILT mask synthesis for co-optimizing design rules and DSA model parameters

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During early stage development of a DSA process, there are many unknown interactions between design, DSA process, RET, and mask synthesis. The computational resolution of these unknowns can guide development towards a common process space whereby manufacturing success can be evaluated. This paper will demonstrate the use of existing Inverse Lithography Technology (ILT) to quickly co-optimize these multitude of parameters.

ILT mask synthesis will be applied to a varied hole design space in combination with a range of DSA model parameters under different illumination and RET conditions. The design will range from 40 nm pitch doublet, triplet to random DSA designs with larger pitches, while various effective DSA parameters of shrink bias and rounding will be assumed for the DSA model during optimization. The co-optimization of these parameters under different SMO solutions and RET conditions (dark/bright field tones and binary/PSM mask types) will also help to provide a complete process mapping of possible manufacturing options. The lithographic performances for masks within the optimized parameter space will be generated to show a common processable space with the highest possibility for manufacturing success.

9052-48, Session 11

Rigorous simulation and optimization of the lithography/directed self-assembly co-process

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The directed self-assembly (DSA) of block-copolymers is a promising avenue for the extension of optical lithography to smaller technology nodes. It can be used both to replicate and to rectify lithographically generated patterns such as lines and spaces or contact holes. Despite a number of early advances, however, the requirements for the lithography process are not fully understood. Specifically, a rigorous computational lithography/DSA framework is still in its infancy. With this study, we aim at closing this gap by providing a litho/DSA co-simulation approach that allows for the investigation and optimization of the mutual process. For that purpose, we present an example of a contact hole rectification through grapho-epitaxy DSA. In the first step, the 193i-lithography process for the guiding structure is broadly optimized in terms of standard lithographic process window maximization. The so obtained profile—using a full resist model—is then passed on to a particle-based Monte-Carlo simulator, which uses a coarse-grained polymer model. This molecular model mimics the relevant material characteristics including the macromolecular architecture, the geometry of the confinement, incompatibilities and surface tension differences between the blocks, all of which are experimentally accessible. The simulation is hence qualified to obtain the morphology of the directed self-assembly.

The proposed modeling strategy exhibits two main advantages over self-consistent field techniques: First, it reveals additional information about the kinetic pathway of structure formation. Second, it intrinsically accounts for thermal fluctuations. For that reason, our simulations provide direct insight into the generation and annihilation of defects during the self-assembly. This information, in turn, can be used to optimize the lithography process such that the resulting guiding structures show a minimum susceptibility to DSA defects. In addition, line edge roughness (LER) as a result of DSA can be quantified and can also be considered during the lithography layout and process stages.

In contrast to conventional lithographic process windows that are defined by acceptable deviations from the target CD, the combined process is chiefly limited by the occurrence of defects. Equilibrium defects are mainly determined by the topography of the guiding structures. Most importantly, an insufficient commensurability between the guiding structure and the intrinsic length scale or period of the DSA material inevitably leads to a defective pattern. But also the limited height, oblique sidewalls and footing or top-rounding of the guiding structure may introduce additional irregularities. Even if the equilibrium density of defects were vanishingly low due to a proper match of guiding structures and DSA material, defects would kinetically arise during the structure formation process in the DSA material and depend on the DSA process parameters such as annealing time and temperature. Moreover, thermal fluctuations give rise to structure variations. While lithographic process variations vastly lead to gradual pattern degradations, the DSA step and the potential defects associated with it introduce a more volatile behavior, rendering a process either feasible or entirely unfit. In this work, we accordingly characterize and quantify the combined process performance and its determining factors. Appropriate metrics and representations for the common process window are derived.

9052-49, Session 12

Critical assessment of the transport of intensity equation as a phase recovery technique in optical lithography

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We apply the transport of intensity (TIE) phase imaging technique to through-focus aerial images in order to recover effective phase at the wafer plane for different illumination polarizations. We use AIMS measurements taken at 193nm for various phase shift masks to study the dependence of recovered phase on mask type, geometry and boundary conditions. The validity of the phase recovery method is tested for different illumination conditions and against other phase recovery algorithms. Once the phase has been recovered, the complex fields are used to determine the effective thin mask boundary layer model that best approximates thick mask edge effects.

9052-50, Session 12

Extremely-long life and low-cost 193nm excimer laser chamber technology for 450mm wafer multipatterning lithography

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193 nm ArF excimer lasers are widely used as light sources for the lithography process of semiconductor production. 193 nm ArF exicmer lasers are expected to continue to be the main solution in photolithography, since advanced lithography technologies such as multiple patterning and Self-Aligned Double Patterning (SADP) are being developed. In order to apply these technologies to high-volume semiconductor manufacturing, the key is to reduce the Cost of Operation (CoO) and the laser downtime. To reduce the CoO, life extension of consumable part is an important factor. Moreover, to reduce laser down time, it is also important to reduce the maintenance frequency of consumable part. The chamber life time of the excimer laser is a main factor to decide the CoO and downtime. Therefore, we are developing the new technology to extend the life time of the laser chamber.

A laser chamber is filled up with argon gas, fluorine gas, and neon buffer gas. A high voltage is impressed to one pair of electrodes in a laser chamber, and an ArF excimer laser is lasing by discharge excitation. Moreover, it is necessary to generate and maintain the stable discharge for the efficient lasing. In order to achieve the stable discharge, the laser chamber is equipped with the pre-ionization function that provides the necessary amount of electron to electric discharge space.

The main factors limiting chamber life time is electrode ablation by the discharge. The chamber electrode will be consumed by discharge in proportion to a laser pulse count . If chamber electrode consumption exceeds an acceptable value, electric discharge will become unstable and laser performance will be deteriorated. Then, laser performance deterioration exceeds an acceptable value, and the chamber reaches the end of it's usable life.

To extend the chamber lifetime, we have developed the specific electrode "G-electrodes" that reduce consumption of a main discharge electrode. [1],[2] "G-electrodes, which are metal electrodes with specially treated surfaces, make discharge stable, decrease electrode consumption, and extended the laser chamber life.

Furthermore, in this time, we have developed the extended life chamber that implemented the following new technologies:

1. Generating stable discharge by pre-ionization strengthening

2. Applying "G-electrodes", having developed for main discharge electrode to the pre-ionization electrode in order to reduce consumption

Those new technologies enable to supply the stable pre-ionization to the discharge space for a long period and to stabilize discharge. Therefore, electrode consumption is decreased, laser performance energy stability is stabilized over a long period of time, and the chamber life is extended. The electrode consumption of the conventional and new chamber is shown in Fig.1. By implementing those new technologies, the electrodes consumption decreased, the expected chamber life time will be increased by 1.8 times compared with the conventional chamber life time. We will report the chamber durability performance that has reflected the new technology and field data.

9052-51, Session 12

Flexible power 90 w to 120 w ArF immersion light source for high-volume semiconductor lithography

Russell Burdt, Cymer, Inc. (United States)

Semiconductor market demand for increased performance at lower cost continues to drive enhancements in excimer lightsource technologies. Improved stability and increased output power are required of the lightsource to support immersion, multi-patterning, and 450 mm wafer applications in high volume semiconductor lithography at the 32 nm node and beyond.

Cymer has developed a lightsource capable of switching nominal power between 90 W and 120 W in less than 5 seconds, built upon the production-proven, high reliability XLR 600ix platform. Wavelength and energy stability, using smaller exposure windows, meet or exceed stability specifications for the current-generation Cymer light source. The flexibility in output power allows throughput to be maintained while running high dose resists, including the capability to change dose from lot to lot.

Facilities power consumption of the flexible-power lightsource at 120 W is the same as the power consumption of the XLR 600ix operating at 90 W.

Extensive design qualification of the high power lightsource was performed during the 3rd quarter of 2013. The test protocol was designed to fully stress the entire operational space of the system in wavelength, bandwidth, energy, repetition rate, and duty cycle. This article reports on the high-level light source design, and various aspects of system performance highlighting stability, versatility, reliability, and system-to-system repeatability.

9052-52, Session 12

Immersion scanners enabling 10nm half-pitch production and beyond

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According to current photo lithography roadmaps pattern shrinking by utilizing multiple patterning techniques will continue to 10 nm half pitch (hp) node and beyond. Nikon's advance future immersion lithography tool, which builds upon the technology advancements of the NSR-S620D/S621D/S622D, has been developed to satisfy the aggressive requirements of 10 nm hp node and subsequent generations.

The key design challenges for future immersion scanners are delivering further improvements to product overlay and CD uniformity, while continuously enhancing productivity in order to improve cost of ownership. In this session, the new features of Nikon's future immersion scanners and the latest relevant data will be presented.

For overlay accuracy, specifically to meet customers' requirement for Edge Placement Error (EPE), Nikon has developed innovative new features (or technologies) for future immersion scanners. One of the key factors in improving overlay is shot distortion; in order to improve shot distortion Nikon's future scanners are equipped with newly developed state of the art projection lenses. The overall overlay improvements have been made possible by not only minimizing lens distortion via advancements in lens manufacturing techniques, but also by reducing thermal aberration, which is especially important in the actual device production. In addition Nikon has also added a new function for more effective reticle heating distortion compensation. In order to improve wafer grid performance, we redesigned out wafer tables to improve thermal stability. Nikon has also further improved the reticle bending system in order to minimize induced field curvature due to reticle thermal aberration.

The new features described above, in addition to the matured Streamlign platform, have enabled Nikon's future immersion scanners to deliver highest accuracy and stability. Nikon is positively confident that the future immersion scanners will provide the best solutions for 10 nm hp node and beyond.

For future productivity enhancements, we are sometimes required to discuss new technologies such as 450mm immersion scanners.

9052-53, Session 12

Extending ArFi immersion scanner capability in support of 1xnm production nodes

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Device shrink is the key drive of the semiconductor industry for decades to enable cheaper and faster electronic devices with more functionality and lower energy consumption. As well in the past as in the years to come ASML is fueling the device shrink with its lithography equipment generation after generation. In order to secure shrink path to 1x nm nodes for its customers, ASML is continuing to extending the ArF immersion roadmap to compliment the EUV roadmap.

For this reason around the end of 2013 an updated version of the NXT ArF immersion platform is scheduled to be releases that will contain various improvements in terms of on-product overlay and focus control, as well as productivity and defectivity improvements.

In this paper we will be reviewing performance data measured on multiple systems of this latest immersion system, as well as look ahead at further extensions for continued support of the industry roadmap.

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9053-1, Session 1

Lithography-induced limits to scaling of design quality *(Invited Paper)*

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Quality and value of an IC product are functions of power, performance, area, cost and reliability. The forthcoming 2013 ITRS roadmap observes that while manufacturers continue to enable “potential” Moore’s-Law scaling of layout densities, the “realizable” scaling in competitive products has for some years been significantly less. This talk will consider the question, “To what extent should this scaling gap be blamed on lithography?”

Non-ideal scaling of layout densities has been attributed to (i) layout restrictions associated with multi-patterning technologies (SADP, LELE, LELELE), as well as (ii) various ground rule and layout style choices that stem from misalignment, reliability, variability, device architecture, and electrical performance vs. power constraints. Certain impacts seem obvious, e.g., loss of 2D flexibility and new line-end placement constraints with SADP, or algorithmically intractable layout stitching and mask coloring formulations with LELELE. However, these impacts may well be outweighed by weaknesses in design methodology and tooling. This paper examines how (i) standard-cell library architecture, and layout guardbanding for automated place-and-route; (ii) performance model guardbanding and signoff analyses; (iii) physical design and manufacturing handoff algorithms spanning detailed placement and routing, stitching and RET; and (iv) reliability guardbanding all contribute – hand in hand with lithography – to a newly-identified “design capability gap”. We will also consider how to better answer the fundamental question of how specific aspects of process and design enablements truly limit the scaling of design quality.

9053-2, Session 1

A pattern-driven design regularization methodology

Jason P. Cain, Norma P. Rodriguez, Advanced Micro Devices, Inc. (United States); Jason Sweis, Frank E. Gennari, Ya-Chieh Lai, Cadence Design Systems, Inc. (United States)

Design and Technology Co-Optimization is a lengthy process which strives to maximize the advantages for both sides. In design we would like to see as few restrictions as possible and allow more flexibility to the designers. In manufacturing technology we would like to see the widest possible process window for yield and yet maintain tight control of the various performance specifications. The two realms must converge on a set of rules that establish the boundaries comprehensively and ensure predicable results. The rules alone, however, have become increasingly difficult to establish and express as we move down technology nodes.

The addition of pattern matching to compliment the design rule checking process is now a well established process. As pattern matching technology has matured we have seen new capabilities and applications that enable a broader use in-design (i.e., during the process of creating and optimizing a physical design). In-design use has its own set of requirements for tight integration, speed, accuracy, and ease-of-use. The productivity for designers can be improved when rules described as patterns can be used for guidance and/or checking while constructing the design. Using a combination of design rule driven and pattern driven tools allows a correct-by-construction approach. Auto-correction and regularization of layout when errors are found provides a powerful methodology to address very complex 2D scenarios.

This paper will describe a methodology for analyzing unique pattern constructs in a design. This methodology will be applied to two different design styles to analyze and report the types and frequency of pattern constructs used. One design will be based on a more regularized design style while the other will be a baseline based on a more standard design style. Systematically quantifying the usage and spread of patterns used in a given design can identify irregular cases that should be fixed or minimized. A way to systematically define unique pattern constructs will be discussed based on a novel topological pattern type (also referred to as “squish” patterns). Strategies to minimize the numbers of unique pattern constructs will also be discussed.

A useful in-design methodology requires a mechanism to pass actionable feedback back to designers. This paper will describe a simple methodology to enforce the regularization of design. Patterns identified as targets for regularization can be easily found in design and simple optimization rules can be applied to the matching layout. Examples of how the latest technologies in pattern matching can be used to drive the design methodology efficiently will be discussed.

9053-3, Session 1

Systematic physical verification with topological patterns

Vito Dai, GLOBALFOUNDRIES Inc. (United States); Ya-Chieh Lai, Frank E. Gennari, Cadence Design Systems, Inc. (United States); Edward Teoh, Luigi Capodieci, GLOBALFOUNDRIES Inc. (United States)

Design rule constraints (DRC) are the industry workhorse for constraining design to ensure both physical and electrical manufacturability. Where DRCs fail to fully capture the concept of manufacturability, pattern-based approaches, such as DRC Plus, fill the gap using a library of patterns to capture and identify problematic 2D configurations1. Today, both a DRC deck and a pattern matching deck may be found in advanced node process development kits. Major electronic design automation vendors offer both DRC and pattern matching solutions for physical verification; in fact, both are frequently integrated into the same physical verification tool.

In physical verification, DRCs represent dimensional constraints relating directly to process limitations. On the other hand, patterns represent the 2D placement of surrounding geometries that can introduce systematic process effects. It is possible to combine both DRCs and patterns in a single “topological pattern” representation. A topological pattern has two separate components: a bitmap representing the placement and alignment of polygon edges, and a vector of dimensional constraints. For example, the bitmap visually and intuitively captures the concept of “tip-to-side”, whereas the constraint vector captures the tip-to-side distance, the line-end edge length, and the line-end adjacent edge length. The topological pattern is unique and unambiguous; there is no code to write, and no two different ways to represent the same physical structure. Furthermore, markers aligned to the pattern can be generated to designate specific layout changes for improving manufacturability, e.g. pull-back the line end.

In this paper, we describe how to do systematic physical verification with just topological patterns. Common mappings between traditional design rules and topological pattern rules are presented. We describe techniques that can be used during the development of a topological rule deck such as: projection, i.e. taking constraints defined on one rule, and systematically projecting it onto other related rules; splitting, i.e. systematically separating a single rule into two or more rules, when the single rule is not sufficient to capture manufacturability constraints; enumeration, i.e. creating test layout which represents the corners of what is allowed, or not allowed by a rule; optimization, i.e. improving manufacturability by systematically changing certain patterns; and

profiling, i.e. quantifying how a design pushes design rules. The performance of running a topological pattern deck on a full chip design is presented.

9053-4, Session 1

Synthesis of lithographic test patterns through topology-oriented pattern extraction and classification

Seong-Bo Shim, SAMSUNG Electronics Co., Ltd. (Korea, Republic of) and KAIST (Korea, Republic of); Young-soo Shin, KAIST (Korea, Republic of)

While a new semiconductor technology is being developed, lithography options such as numerical aperture, illumination, and film stacking on a wafer are optimized with an ideal goal of defect-free image during a mass production.

Test patterns that are used for this process should be comprehensive for high coverage of actual patterns as well as compact for smaller time for optimization.

The proposed method to achieve this goal is outlined in Figure 1.

Each test layout is decomposed into patterns, which are then classified.

A set of test patterns are identified from classified patterns, which are then used for optimizing lithography options.

The proposed pattern extraction is illustrated in Figure 2(a).

A list of regions (each marked by a small box) that may cause lithographic defect is identified; they are typically where layout topology changes, e.g. a region of abrupt change of metal pitch and a region where two line ends are close.

Patterns are then extracted with each mark of region as a center.

This is compared to conventional pattern extraction shown in Figure 2(b), which extracts patterns at regular geometric intervals and yields much larger number of patterns.

A few methods have been proposed for pattern classification.

Bitmap-based method is most convenient, but using grids as a unit of computation inherently causes quantization errors due to grid snapping.

The proposed method shown in Figure 3(a) overcomes this limitation by converting an image to multi-dimensional vectors and then using CLARANS for classification.

The result of this method applied to Figure 2(a) is shown in Figure 3(b).

Test layouts we take as input of proposed method shown in Figure~ref{fig: layout_anatomy} eventually determine the quality of test patterns.

We may explore various options while we generate the layouts such that we end up with more variety of patterns.

Examples are the amount of white space, via insertion scheme, and so on; they will be investigated as a part of our study.

9053-5, Session 1

Systematic data mining using a pattern database to accelerate yield ramp

Edward Teoh, Vito Dai, Luigi Capodieci, GLOBALFOUNDRIES Inc. (United States); Ya-Chieh Lai, Frank E. Gennari, Cadence Design Systems, Inc. (United States)

Pattern-based approaches to physical verification, such as DRC Plus, which use a library of patterns to identify problematic 2D configurations, have been proven to be effective in capturing the concept of manufacturability where traditional DRC fails. As the industry moves to advanced technology nodes, the manufacturing process window tightens and the number of patterns continues to rapidly increase. This increase in patterns brings about challenges in identifying, organizing, and carrying forward the learning of each pattern from test chip designs to first product and then to multiple product variants. This learning includes results from printability simulation, defect scans and physical failure analysis, and is important for accelerating yield ramp.

Using pattern classification technology and a relational database, GLOBALFOUNDRIES has constructed a pattern database (PDB) of more than one million potential yield detractor patterns. In PDB, 2D geometries are clustered based on similarity criteria, such as radius and edge tolerance. Each cluster is assigned a representative pattern and a unique identifier (ID). This ID is then used as a persistent reference for linking together information such as the failure mechanism of the patterns, the process condition where the pattern is likely to fail and the number of occurrences of the pattern in a design. Patterns and their associated information are used to populate DRC Plus pattern matching libraries for design-for-manufacturing (DFM) insertion into the design flow for auto-fixing and physical verification. Patterns are used in a production-ready yield learning methodology to identify and score critical hotspot patterns. Patterns are also used to select sites for process monitoring in the fab.

In this paper, we describe the design of PDB, the methodology for identifying and analyzing patterns across multiple design and technology cycles, and the use of PDB to accelerate manufacturing process learning. One such analysis tracks the life cycle of a pattern from the first time it appears as a potential yield detractor until it is either fixed in the manufacturing process or stops appearing in design due to DFM techniques such as DRC Plus. Another such analysis systematically aggregates the results of a pattern to highlight potential yield detractors for further manufacturing process improvement.

9053-6, Session 1

Layout pattern-driven design rule evaluation

Yasmine A. Badr, Univ. of California, Los Angeles (United States); Ko-wei Ma, NVIDIA Corp. (United States); Puneet Gupta, Univ. of California, Los Angeles (United States)

Restricting the occurrence of low printability layout patterns is hard to achieve using simple 1D design rules. This has resulted in popularity of lithographic hotspot detection, pattern-checks (e.g. DRC+ from Global Foundries) in addition to complex 2D design rules. Although intuitive reasoning would recommend the elimination of these poor printability patterns in the standard cell design phase, prohibiting these patterns from the intra-cell routing layers can lead to an increase in area. Thus, we propose a framework PatternDRE (Pattern-Driven Design Rule Evaluation) to assess the interaction between design rules and layout patterns.

PatternDRE generates a virtual standard cell library, given a set of design rules as well as the netlists of the standard cells. Using the netlists and the generated pin locations, PatternDRE generates routing options for each net, where each routing option is a Single Trunk Steiner Tree. Then the conflicting routing options (from different nets) are resolved in order to produce all valid routing solutions for the cell. A routing solution is expressed as tiles, where each tile is a layout pattern containing several track segments, which are then expressed as binary strings by the pattern translator. The process of matching the patterns to detect the undesired patterns becomes an XOR operation. Then the pattern occurrences -in the estimated routing solutions- are counted. Although the framework performs the counting on estimated wiring solutions (rather than actual layouts), the resultant pattern counts are compared to those obtained from a 45nm cell library, and the correlation is 0.8475, which shows that this approach is a good prediction of pattern occurrence in actual layouts (without being tied to a specific router).

Two use models of PatternDRE are explored in this work. First, implications of prohibiting these patterns in standard cell design are studied. PatternDRE performs routing estimation, restricting the usage of undesired layout patterns. The resulting cell layout estimates are evaluated in terms of area, yield and variability metrics. Second, the framework is used to study the probabilistic relationship between design

rules and the existence of the undesired patterns. Some design rules will lead to a higher probability of the hot spot patterns and thus will result in lower printability. Hence, using the framework, design rules can be optimized for the reduction of probability of hot spots in the intra-cell routing layer.

In this work we develop a framework for layout pattern-driven design rule exploration. We show the use of PatternDRE framework to assess rule-pattern interactions in a 45nm technology and cell library.

9053-7, Session 2

Bridging the gap from mask to physical design for multiple patterning lithography *(Invited Paper)*

David Z. Pan, The Univ. of Texas at Austin (United States)

Due to the delay of EUVL, multiple patterning techniques have been used to extend the 193nm lithography to 22nm/14nm nodes, and possibly further. There are many studies on MPL layout decompositions at the mask synthesis stage to resolve the coloring conflicts, minimize the stitches, balance the mask density, or even mitigate the undesirable overlay effects. Meanwhile, there are studies showing that it is very important to consider the multiple patterning implications at earlier physical design stages so that the overall design and manufacturing closure can be reached. In this paper, we will show some recent results and propose a unified physical design methodology for standard cell compliance, pin access, routing, and placement to bridge the gap from mask/layout decomposition to physical design, while accommodating various requirements from double/triple patterning lithography in certain “correct by construction” manner.

9053-8, Session 2

Demonstrating production quality SIT-aware routing for the 10nm node

Lars W. Liebmann, IBM Corp. (United States); Vassilios Gerousis, Paul Gutwin, Mike Zhang, Cadence Design Systems, Inc. (United States); Brian Cline, ARM Inc. (United States); Gustavo Tellez, IBM Corp. (United States)

The practical resolution limit of double patterning techniques based on interdigitating two gratings, commonly referred to as ‘litho-etch-litho-etch’ (LELE), is reached when the intra-level alignment error exceeds acceptable process tolerances causing yield limitations due to effects such as dielectric breakdown due to minimum insulator violations. While LELE in theory should be able to extend the resolution of a 193nm immersion lithography tool capable of printing a 80nm pitch grating all the way down to 40nm, these alignment errors force a pitch below roughly 50nm to use a double patterning technique with reduced pattern misalignment, often referred to as self aligned double patterning (SADP), using sidewall image transfer (SIT). As discussed extensively in this conference (Yuansheng, Proc. SPIE. 7641) SIT based double patterning imposes significantly complex design restriction to ensure layout decomposability into mandrel and block mask shapes and to guarantee the manufacturability of these mask patterns. The complexity of the design restrictions arises from the fact that the two mask patterns used in the SIT process, the mandrel onto which the sidewall spacers are deposited and the block mask that is used to trim the sidewall patterns into useful 2-d layout patterns, are only very abstractedly correlated to the intended layout drawn by the designer. As seen with all layout intensive frequency doubling techniques (alternating phase shift, litho-etch-litho-etch, and sidewall image transfer), additional measures need to be taken in the design to ensure layout decomposability into the two component masks. In litho-etch-litho-etch (LELE) double patterning this is achieved by decomposing the design, either explicitly or implicitly through odd cycle checking, as part of conventional design rule checking. The complex decomposition and abstract pattern correlation in SIT make layout decomposition in the design space inefficient, especially for automated design tools such as routers used to wire standard cell logic designs. It is therefore desirable to reduce the complex design restrictions of SIT to a set of design rules which can be coded into a commercial router to achieve an efficient routing solution. A critical aspect of this work is the inverse correlation of rule simplicity and achievable routing density, i.e. complex design rules lead to theoretically denser layouts but impede routing efficiency to a point of not being practical.

This paper shows how SIT patterning constraints for the 1x wiring levels of the 10nm node have been reduced to a set of 2-color mapping and line-end stagger rules. The applicability of these rules to actual product designs is demonstrated in experiments conducted using early samples of ARM’s 9T library. The data presented show that the SIT-aware routing solution developed under the IBM-Cadence routing collaboration efficiently yields product quality density in uni- as well as bidirectional wiring solutions. Further results demonstrate how different wrong-way wiring constraints can be used to balance patterning quality versus routing efficiency.

While significantly more work remains to be done in readying the physical design environment for 2nd generation double patterning techniques, this work demonstrates the value of early engagement between EDA tool developers, IP providers, and semiconductor fabricators.

9053-9, Session 2

A fast triple-patterning solution with fix guidance

Weiping Fang, Synopsys, Inc. (United States); Peter De Bisschop, IMEC (Belgium); Marco A. Hug, Srini Arikati, Erdem Cilingir, Synopsys, Inc. (United States); Julien Mailfert, IMEC (Belgium) and Katholieke Univ. Leuven (Belgium); Kevin Lukas, Synopsys, Inc. (United States); Weimin Gao, Synopsys, Inc. (Belgium) and IMEC (Belgium)

Logic manufacturers are increasingly looking towards a triple patterning solution for their 10nm node Metal1 layer, and possibly for Via0, and local interconnect layers as well. Given the nature of NP-completeness for the 3-colorability problem, a challenge is how to go beyond a standard cell to efficiently decompose a layout at a block or chip level. Using decomposed or pre-colored standard cells does not always mean decomposable standard cell layouts can be placed next to each other. Posing constraints on how cells can be placed next to each other could cause area loss. A preferred way is to perform the decomposition at a block or chip level.

We have successfully developed a triple patterning decomposition methodology that can effectively decompose an entire layout block or a chip. This system first builds a graph. A node in the graph is a polygon in a layout and an edge between two nodes means two corresponding polygons are less than the same mask spacing apart. It then tries to reduce and partition the graph without changing its 3-colorability property. The main techniques used are removal of nodes with a degree of two or less and breaking the graph into individual bi-connected components. Each bi-connected component is a sub-graph where there are at least two disjoint paths between any two nodes of the sub-graph. A graph is then 3-colorable if and only if all bi-connected components are 3-colorable. To color the reduced graph, we adopt a hybrid approach with a fast heuristic for coloring and an exact coloring algorithm for backup and conflict verification. Figure 1 shows a successful decomposition of a 50 row Metal1 block. The decomposition alone including graph reduction and coloring took less than 1 second.

Unlike an odd loop in double patterning, a triple patterning coloring conflict can’t be represented in a single loop. Another challenge for triple patterning is then how to report errors that the user can effectively use to fix them. Figure 2 illustrates what we output as an error if there is coloring conflict. For each reduced sub-graph, the system finds a minimum number of edges that are needed to remove in order to make

the sub-graph colorable. We call such a minimum set of edges together with their connecting polygons a minimum fix guidance. The system finds all of such minimum fix guidances for the user to choose from – we call that maximal minimum fix guidance. In Figure 2, the graph includes a K-4, a complete sub-graph of 4 nodes. K-4 is the smallest graph that is not 3-colorable. For K-4, every edge is a minimum fix guidance, and the maximal minimum fix guidance is the entire K-4. However, Figure 2 shows a graph that is more complicated than K-4, and our system successfully identifies all minimum fix guidance – not all K-4 edges.

We believe this system is the first of its kind, both in terms of performance and in terms of useful error output. In this paper, we present our solution along with different testing results.

9053-10, Session 2

Benchmarking process integration and layout decomposition of directed self-assembly and self-aligned multiple patterning techniques

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Despite the significant progress of directed self-assembly (DSA), the prospect for its insertion into high-volume semiconductor manufacturing is yet to be explored. DSA is a cost-effective process that enables frequency multiplication using standard IC fab equipment, while still lacking commercial EDA/design systems to support its implementation and suffering from defect related issues. Instead of the line/space patterning application, the major interest in DSA process is its hole shrinking capability and self-aligned hole density multiplication, e.g., for cutting 1-D grating structures. One reason is the difficulty of controlling the chemical “fringe-effect” chaos at the edges of any non-closed templates. Such a process issue is nevertheless absent in self-aligned multiple patterning (SAMP) as its spacers always form regular 1-D close loop around the mandrel, thus enabling a predictable cut-mask design/processing. The DSA shrinking capability, is not necessarily more competitive than other well-known approaches such as SAFIER, RELACS, spacer fill, etc.

As a proven patterning solution for NAND and FinFET devices, self-aligned multiple patterning (SAMP) is more practical for random 2-D polygon patterning. However, the SAMP process complexity and costs (or cycle time) continue to draw criticism from many lithographers. Therefore, it is worthwhile to take a closer look at process integration issues and layout strategy of these two patterning techniques. Many critical questions remain unanswered, e.g., what is the optimal mask strategy (including mask number per critical layer, process tone, etc.) for each technique, which technique is the best for different semiconductor sectors, and what are the consequent impacts on their process integration and layout decomposition/synthesis? To answer these questions, a comparative analysis of DSA and SAMP techniques (e.g., resolution capability, process complexity/cost and performance, layout decomposition/synthesis) will be reported in this paper.

9053-11, Session 2

Self-aligned quadruple patterning-friendly routing

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SAQP (Self-aligned Quadruple Patterning) is one of the most promising techniques in 14nm node and beyond.

However, construction of feasible layout configurations is very difficult since wafer images must satisfy tighter constraints than LELELE triple patterning due to its distinctive process.

In this paper, we propose a new routing method for feasible SAQP layout.

Our method performs detailed routing by correct-by-construction approach and offers compliant layout configuration without any pitch conflict and worries about overlay error in trim lithography.

In order to confirm the effectiveness, we carried out computational experiments.

9053-12, Session 3

Challenges in OPC and design at 20nm and below *(Invited Paper)*

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A fierce challenge faced by OPC in 20nm and below is to accurately predict all types of patterning failures and to solve them before a mask is built. In earlier nodes, the lithography process simulation including off-focus, off-dose, and mask error was sufficient to find litho-hotspots, and the rules developed to prevent other failures such as assist-feature printing or post-etch failures were not causing gross degradation in lithography process window so they were easily accommodated. At 20nm and beyond, many important features have been added to the OPC to avoid these types of failures including design retargeting, model-based assist feature generation, and resist profile aware RET & OPC. While these features require a lot of optimization in the OPC recipe, they are also sensitive to unforeseen failures on new design styles. In order to address the challenge of making OPC robust to new design styles, additional tools such as repairOPC with advanced OPC solvers are also introduced while continuing to ensure robustness of the individual recipe features across an unseen set of design layouts.

9053-13, Session 3

Accurate lithography hotspot detection based on PCA-SVM classifier with hierarchical data clustering

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With the continuous shrinking of technology nodes, layout patterns become more sensitive to lithography processes and degrade manufacturing yield. Lithography hotspots are forbidden topologies that need to be identified and eliminated during physical verification. Various design for manufacturing (DFM) techniques have been proposed to avoid these hotspots. In the meantime, there are resolution enhancement techniques (RET), such as optical proximity correction, phase-shift mask, and off-axis illumination, to improve the printability of problematic topologies. However, for deep sub-wavelength process, preventing lithography hotspots is still challenging and it requires accurate physical verification to identify these hotspots for yield improving.

In physical design and verification stages, the hotspot detection problem is to locate hotspots on a given layout with fast turn-around-time. Conventional lithography simulation obtains pattern images by complicated lithography models. Although it is accurate, full-chip lithography simulation is computational expensive, and thus cannot provide quick feedback to guide the early physical design stages. Recently, pattern matching based and machine learning based hotspot detection have become popular candidates. Although pattern matching based methods are accurate and fast, how to properly define hotspot patterns is still the main issue. Machine learning based approaches enlarge the possible topologies for hotspots, therefore can improve the detection rate. However, it also increase the false alarms, which means some reported hotspots are not real hotspots.

In this paper, we propose a high performance hotspot detection approach based on PCA-SVM classifier. Support Vector Machine (SVM) is a data learning model, and Principle component analysis (PCA) is a technique for feature extraction and data reduction. Combining PCA with

SVM helps to improve the detection accuracy significantly. The main contributions include:

• We propose a multi-level PCA-SVM based data learning flow that can extract critical layout information through mathematical analysis.

• We present a two-stage hierarchical data clustering approach to partition the layout data, such that irrelevant data can be processed by different classifiers for both efficiency and accuracy improvement.

• We apply several data compression techniques to enhance the performance of PCA-SVM, including data sampling for hotspot/non-hotspot imbalance, and dimension reduction for encoded layout data.

• The experimental results show that our approach effectively maximizes accuracy and minimizes false alarms at the same time, where more than 80% of hotspots on all given testing layouts can be identified successfully.

A sample of the input layout clip is shown in Fig. 1. A Frame corresponds to the ambit or context area associated to its center. A Core, if indicated, corresponds to the central location where a hotspot appeared; otherwise the clip is free of hotspots. Fig. 2 shows our hotspot calibration flow. Given the training layout clips, we first decompose the layout patterns into small fragments based on Hanan grids, and collect a set of hotspot fragments and a set of non-hotspot fragments. We adopt the fragmentation based pattern characterization method to encode fragments, in which each fragment is represented by a Fragment Vector. Next, we apply hierarchical data clustering to group similar fragments together based on their topological information. Fragments in each cluster are sampled for data balancing and then sent to our PCA-SVM based learning process. Finally, a set of hotspot classification models will be calculated for the use of the detection process.

9053-14, Session 3

Model-based multilayers fix for litho-hotspots beyond 20nm node

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Sub-20nm node designs are getting more sophisticated, and printability issues become more critical which need more advanced techniques to fix. It is mandatory for designers to run lithography checks before tapeout, and it is very challenging to fix all of the generated hotspots manually without introducing unintentional hotspots, or DPT violations.

This paper presents a methodology for fixing hotspots on DPT layouts, using the same engine used for detecting hotspots. The fix is based on DRC and DPT constrained minimum movement of edges causing the hotspot, which guarantees that the fix does not violate any of the specified DRC or DPT constraints, nor does it need recoloring.

The fix is extended along multilayers to fulfill the specified DRC and DPT constraints and guarantees circuit connectivity along the layers stack. This multilayers approach fixes hotspots that were impossible to fix previously.

This methodology is demonstrated on industrial designs, where single and dual layer hotspots were fixed and the fixing rate is reported.

9053-15, Session 3

Configurable hotspot fixing system

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Hotspot fixing technology emerged to solve various patterning problems caused by low-k1 lithography, such as pinching, bridging and line-end shortening, at a design stage. Recent simulation technique can also find more hotspots caused by etching as well as lithography process. In order to fast clean up such hotspots at the design stage, automatic hotspot fixing techniques grow greatly important to cutting-edge devices beyond 40nm node [1] [2]. A rule-based fixing could be effective for hotspots which have enough rooms for moving its pattern following a rule table prepared in advance though it is unable to completely remove hotspots on dense or complex patterns. Besides, a highly-coherent optical condition with both complicated source and mask with sub-resolution assist feature (SRAF) make it more difficult to fix hotspots by the simple rule-based approach.

Therefore, a configurable hotspot fixing system has been developed to automatically remove hotspots even on the dense and complicated layout to be exposed under the highly-coherent optical condition. Firstly, in order to avoid violating a design rule after pattern modification for fixing hotspot, an overall analysis is made about how much of minimum width and space is available from the layout itself. The configurable functions in the system can easily make various modified pattern candidates, such as not only resizing but also SRAF or dummy pattern, adjustment of nearby line-end or corner position and their combinations, without violating design rules determined by the analysis. The optimum pattern is selected from the candidates based on the cost function which is defined by the lithography simulation and design rule checker (DRC).

Comparison of hotspot fixing rate and processing time is made between conventional and the proposed method for metal layer with dense and complicated patterns. As a result, the configurable hotspot fixing system is found to be the most promising in terms of the fixing rate and processing time. In our report, the details of our proposed system and results will be discussed.

9053-16, Session 3

Smart source, mask, and target co-optimization to improve design related lithographically weak spots

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As patterns continue to shrink to physical limits, advanced Resolution Enhancement Technologies (RET) encounter increasing challenges to ensure manufacturable Process Window (PW) margins. For advanced logic devices, the manufacturable k1 value typical for the most advanced L/S patterns is about 0.28 and for contact patterns is about 0.33, which is pushing ArFi imaging process margins. Moreover, due to the wide variety of pattern constructs typical of logic device layers, we find lithographically weak patterns either in simulation or from wafer results despite Source and Mask co-Optimization (SMO) and advanced OPC being applied. These weak patterns become a difficult obstacle for OPC/RET engineers trying to ensure adequate patterning process margin.

In order to overcome these design related lithographically weak spots, designers need lithography based simulator feedback to early on evaluate design rules and RET/OPC engineers must co-optimize the overall imaging capability and design lithography target. To meet these needs, a new optimization method called SmartDRO (Design Rule Optimization) has been developed. SmartDRO utilizes SMO's Continuous Transmission Mask (CTM) methodology and unique optimization algorithm including design target variables in the cost function. The optimizer can find the optimum source shape, OPC mask as well as the recommended lithography target.

In this paper, we introduce a new optimization flow incorporating SMO's SmartDRO capability to optimize the layout within the cell to improve the manufacturable process window. First of all, we verify the original design layout utilizing an OPC verification tool (Lithography Manufacturability Check - LMC) or from wafer exposure data. Once the lithographically

weak patterns are found, a SmartDRO job is setup including the limiting patterns. SmartDRO then, optimizes these weak patterns' target layer and outputs an optimized layout. After the optimization, there are two approaches depending on the pattern type: For standard cell layouts, designers will use this lithography based simulation feedback from the RET engineers to re-draw the cell design accordingly. For back end of line (BEOL) metal routing layers, because the original design has been generated by an automatic routing tool, the rules from the optimized layout are extracted. A pattern search and match tool is used to find all the similar patterns in the layout and the targets are modified using the newly generated rules based on SmartDRO generated recommendations.

With these flows, we demonstrate low k1 imaging improvement using SMO with SmartDRO to gain manufacturable process windows for both standard cell and random patterning for sub-20nm logic metal routing layers.

9053-17, Session 4

Layout induced variability and manufacturability checks in FinFETs process

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As the semiconductor technology shrinks down to sub 45nm and bellow, a layout context effect of standard cells caused by the surrounding neighbor cells has critically impacted on the circuit performance and power. A layout context effect is mainly introduced by 1) stress-induced impacts e.g. SiGe source/drain, STI (shallow trench isolation), 2) dopant density-induced impacts e.g. WPE (well proximity effect) and (LOD) length-of-diffusion, 3) lithography/etch-induced impacts e.g. lithographic proximity due to poly-to-poly space, OD-to-OD space or non-rectangular pattern shape, 4) mechanical impact e.g. CMP (chemical mechanical polishing), and so forth.

Even though the importance of a layout context effect on planar devices has been widely understood, its study on 3D devices, in particular FinFET, has relatively not been published yet. In recent researches, Fin-related stress at 3D FinFET devices highly increases and results in defect formation. Moreover, the intrinsic transistor shape differences of FinFET, for instance, the discretized diffusion (OD), the dummy poly on OD, the vertical Fin shape, the wrapping gates and so on, result in somewhat different trends of stress and process variations in standard cells.

In this paper, we analyze the sensitivity of standard cell layouts in FinFET design in terms of various stresses and process variations and apply them to our System-on-Chip (SoC) to get a robust design against variation, power and performance. In order to characterize the sensitivity of standard cells in the timing and leakage power due to the layout dependent effects (LDE), LDE Electrical Analyzer is used.

We first rank standard cells based on their sensitivity of layout context effect in FinFET design, then provide the quantified data to integrate into margin definition in cells, and finally optimize our SoC design for the best trade-off among variations, power and performance.

9053-19, Session 4

Rigorous layout optimization for array edges of periodic contact patterns using negative-tone development

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We have discussed the need of a rigorous mask optimization process for a 2x nm node DRAM contact cell layout yielding mask layouts that are optimal in process performance, mask manufacturability and accuracy. In this paper, we have shown the step by step process from analytical illumination source derivation, a NTD and application tailored model calibration to layout optimization such as OPC and SRAF placement. Finally the work has been verified with simulation and experimental results

9053-20, Session 4

An in-design DFM flow with pattern compaction for 16nm FinFET SoC design

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The upcoming sub-20nm semiconductor process introduces lots of advanced resolution enhancement technologies. Among them, double patterning technique (DPT) decomposing a mask into two or more masks is the utmost prominent method to print layouts since the minimum pitch becomes less than the resolution limit for single patterning. At the expense of sub-resolution-limit printing, DPT induces more process variation, e.g. mask misalignment, stitch insertion etc., and design related issues, e.g. coloring-aware physical design, conflicting with via enclosures, etc. Therefore, the DPT and DFM (design for manufacturing) sign-off should be well integrated into design flow in order to validate the design robustness against process variations. In addition to DPT issues, the introduction of FinFET in 16nm makes custom designs as well as digital designs more difficult to be closure. A conventional model-based DFM check is used to calculate multi dimensional numerical formulae to estimate printed image on a wafer. Thus, it is accurate yet require expensive computational resources; model-base DFM checks take a few hours for just a few hundred square micron layers even with a state-of-the-art CPU. Since a current SoC (System-on-Chip) design has more than several billion transistors and its chip size is a square millimeter or centimeter-level, it is somewhat difficult to be used with a given design TAT (Turn-Around-Time).

Furthermore, a conventional DFM sign-off flow detects all possible manufacturing failures at around final stage of the design steps. This construct-by-correction (find-and-fix) approach inherently is an easy and straightforward way to fix manufacturing problems in design. However, if the possible hot spots are too many, it requires many iterations between physical design step (usually detailed routing but even upto placement) and the final DFM sign-off step.

To achieve a considerable reduction of TAT, we develop an in-design DFM flow in our 16nm FinFET SoC design. Our flow uses a pattern matching technique to concurrently avoid manufacturing hot spots during physical design stages with a correct-by-construction manner. Pattern libraries are made from several modelbased DFM tools: model-based lithography and etch simulation tools, a CMP (chemical mechanical polishing) simulation tool, and a layout dependent effect (LDE) checker.

Since a pattern matching technique relies on a set of pre-defined hotspot patterns, the accuracy is highly proportional to the number of patterns. However, too many patterns result in high overestimate rate and make TAT increase. To cope with the challenge, pattern library are abstracted by identifying similar patterns and optimizing pattern groups. Moreover, we rank manufacturing weak patterns based on their criticality. High ranked critical patterns can be converted into restricted design rule (RDR) and thus be removed from the beginning of the design.

9053-32, Session PWed

Decomposition-aware layout optimization for 20/14nm standard cells

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Double Patterning Technology (DPT) requires layout designs to be

decomposed from one to two individual mask layers. The decomposition is achieved manually and/or automatically using EDA tools. Each DPT-compliant layout design can be decomposed in multiple ways. These decomposition solutions can be systematically, automatically, and quickly evaluated for manufacturability using a decomposition-aware scoring methodology.

This paper presents the layout design improvements for 8, 9, 11, and 13-track 20nm and 14nm standard cells using a decomposition-aware scoring methodology. The methodology first evaluates a DPT-compliant layout based on a set of DPT-specific metrics that have been defined from characterizing the sensitivity of layout parameters to manufacturability. Once a characteristic function is obtained, it is then normalized to a scoring scale from 0 to 1, in which 1 is the optimum. The DPT-specific metrics include misalignment-induced spacing variability between two adjacent oppositely-colored features, the density differences between the two decomposition mask layers, and stitching-induced variability. Often, optimizing one metric may degrade another. The scoring methodology enables the evaluation of the design and manufacturability trade-offs in two ways. One, it prioritizes the DPT-specific metrics such that the critical layout-induced manufacturability concerns are addressed first during layout-fixing. Two, a composite score is used to assess the overall manufacturability improvements resulted from the design changes. The composite score assumes that the individual metrics are independent from one another and is computed as the product of the individual scores for each DPT-specific metric. Evaluating the composite score is beneficial since the manufacturability of a design is dependent on not only the individual changes in the layout but also all the changes combined.

An illustration of the layout design improvements using the decomposition-aware scoring methodology is presented for a 9-track standard cell. The original layout design has 3 stitches. The number of stitches is quantified as a stitch density score of 0.71. To improve the design, the stitches are eliminated. However, at the cost of improving the stitch density score from 0.71 to 1, the density difference score worsens from 0.74 to 0.70. The composite score quantifies this trade-off and shows an improvement from 0.53 to 0.70, indicating that the stitch-free design has better manufacturability.

9053-33, Session PWed

Resist profile aware source mask optimization

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The control of resist profile has become very important in advanced lithography, as it plays a critical role in determining the post-etch final CD's. Although the resist profile is co-related to the resist chemistry and is normally tuned under certain baking/developing conditions, it can also be optimized by engineering the optical intensity distribution through the resist thickness. One such method is the resist-profile aware OPC, in which the resist top CD's are calculated and their edge placement errors are added into the cost function of OPC. As a result, the final mask layout shapes are tailored for a better top CD control, while the bottom CD contour accuracy is reasonably maintained. In addition to the mask layout shapes, the illumination source also has a significant effect on the image intensity distribution and thus opens another way for resist profile engineering.

In this paper, we present the approach and results of resist profile aware source mask optimization (SMO). Similar to the conventional SMO approach, the resist profile aware SMO is meant to seek the optimized source/mask combinations based on certain cost functions constructed from the image properties over a given set of critical pattern clips. In this new approach, the cost functions include the image properties calculated not only from the resist bottom image planes, but also from the top image planes. Consequently, the optimized source and mask shapes are a good balance between the process window for the bottom CD's, and top CD control to ensure a straight resist profile favorable for the etching process. We built up the flow of resist profile aware SMO and implemented this approach on a 1x nm node back-end layer. Two best candidate sources, SMO1 and SMO2 were generated from the conventional SMO flow and the resist profile aware SMO flow, respectively. As shown in Fig. 1, the SMO1 source exhibits the best overlapped process window calculated based on 10% bottom CD variations. Although SMO2 has a relatively smaller overlapped DOF evaluated at bottom CD, it gives rise to a smaller top CD-to-bottom CD difference as shown in Fig. 2, indicating a more straight resist profile. The simulation results were verified by measuring the bottom CD's of all the critical pattern clips from the FEM wafers exposed with the candidate sources. The resist profile was also checked by X-SEM images from selected patterns. The wafer data have shown good matching with the simulation results, indicating that the resist-profile aware SMO is a feasible approach to optimize the illumination sources for a reasonable bottom CD based process window as well as favorable resist profiles.

9053-34, Session PWed

Fast lithographic hotspot identification and monitoring

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As the semiconductor industry moves through the nodes to lower k1 lithography, process window is being constantly eroded. One solution that is already widely used to overcome this obstacle is multi-patterning. However, this solution has cost and cycle-time implications not to mention overlay challenges that become formidable beyond double patterning. Thus, semiconductor designers try to minimize required lithography steps by moving to ever more aggressive reticle enhancement techniques (RETs) and source-mask optimization (SMO) all the way to inverse lithography (ILT) that may be required at the low 1xnm Logic node. While these techniques increase process latitude, it is becoming very difficult to predict patterning failure and extensive modeling and simulations are required to identify design hotspots that may limit process window. In latter technology nodes, effects that were considered second order are starting to impact the process window (e.g. mask 3D effects and mask process variation). In this paper we are suggesting a method that allows for identification of lithographic weak points (a.k.a. hot-spots) using optically generated aerial imaging rather than aerial simulations. One benefit of using optically generated aerial imaging for identifying hot-spots is the inclusion of difficult-to-quickly-simulate effects (e.g. mask 3D effects) as well as actual mask variation effects. Another benefit is cycle time. The data can be quickly obtained at the mask shop right after mask fabrication without the need to move mask to wafer fab, print the wafer and review it.

In addition, aerial images can also be taken periodically at the wafer fab, monitoring the effect of mask degradation on existing hotspot as well as identifying any new hotspots resulting from the degraded mask.

This paper summarizes gathered experience from several different use cases demonstrating how these yield impacting hot spot events may have been identified using optically generated aerial image of the mask. We are also suggesting the use of this capability in practice.

9053-35, Session PWed

Robust and automated solution for correcting hotspots locally using cost-function based OPC solver

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In the previous work1, we introduced a new technology called Flexible Mask Optimization (FMO) which was successfully used for localized OPC correction. OPC/RET techniques such as model based assist feature and process window based OPC solvers have become essential for addressing critical patterning issues at 2x and lower nodes. With FMO flow, critical patterns were identified, classified and corrected using advanced techniques only in localized areas. One challenge with this flow is that once the hotspots are identified, user still has to come up with the OPC solution to address the hotspots. This process can be cumbersome and time consuming as different type of hotspots with new designs may require different recipes causing delays tapeout. What is required is a robust, powerful and automated OPC technique that can handle various types of hotspots so that automatic hotspot correction flow can be established.

In this work, we are introducing a new cost function based OPC technique called Co-optimization OPC which can be used to correct various types of hotspots with minimum tuning effort. In this approach, the OPC solver simultaneously solves for all the segments in a patch including main and sub-resolution assist features (SRAF) with additional user defined cost function constraints such as MEEF, PV band, MRC and SRAF printability. Unlike conventional OPC solvers, Co-optimization solver can also move and grow SRAF which further improves the process window. Key benefit of Co-optimization OPC solution is that it can be used as a standard recipe to resolve many different hotspots encountered across various designs for given layer.

In this study, we will demonstrate that Co-optimization OPC can be successfully used to address various types of hotspots across designs for N28 metal layers as an example. This layer has been particularly challenging as it uses single exposure lithography with k1 of near 0.3. Aggressive RET solutions are required to address the patterning challenges for this layer. Finally, we will report on implementation of the Co-Optimization OPC Recipe within the FMO framework for hotspot correction.

9053-37, Session PWed

An improved coloring algorithm for layout decomposition in self-aligned multiple patterning

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Spacer based self-aligned multiple patterning (SAMP) is a promising technology to scale IC devices to 7nm half- pitch nodes. However, the related industry-wide EDA progress (e.g., layout decomposition/ synthesis) has been mainly focused on SADP process, and only a few groups reported their work of developing SAQP coloring algorithms for some simple layout examples, or degenerating SAQP/SASP layout decomposition into a SADP problem. Generally speaking, these research activities are still on their early stage of technology development and a lot of more effort is needed to build a mature EDA ecosystem for a timely implementation of SAMP technology.

In this paper, we shall propose a new coloring algorithm for both 2-mask and 3-mask negative-tone (for backend application) SAQP and SASP processes. Besides the mandrel and cut masks, a third 2-D mask (spacer-expansion mask) is introduced in the 3-mask process to generate assisting patterns overlapping the first or the second spacers. This extra mask can help to improve our 2-D design freedom. Given that the minimum line and trench CD are both W (usually defined by the spacer width), the new coloring algorithm is developed based on two assumptions:

(1) The minimum space between any two trim mask patterns is larger than W (see Fig. 1 (a) and Fig. 2 (a)) and the generated sub-graph fits the regular arrangement shown in Fig. 1 (c) for SAQP process (or Fig. 2 (c) for SASP process).

(2) In SAQP process, the minimum space (generated from two separate mandrels) between two spacer1 features is larger than 3W (see Fig. 1 (b)). In SASP process, the minimum space (generated from two separate mandrels) between two spacer2 features S_S2≥3W (see Fig. 2 (b)). Consequently, the generated SAQP sub-graph fits the feature arrangement shown in Fig. 1 (c), while the SASP sub-graph fits the arrangement shown in Fig. 2 (c). Other situations will be discussed in our paper as well.

Under above two assumptions, we only need to assign colors to layout features according to the arrangement shown in Fig. 1 (c) and Fig. 2 (c). The decomposition flow using this coloring algorithm for both SAQP and SASP processes are shown in Fig. 3 and Fig. 4 respectively. A 22nm metal1 standard cell was successfully colored and decomposed using a negative-tone SAQP coloring algorithm (see Fig. 3). In addition, four possible coloring schemes are generated, and the second scheme (enclosed by the red frame) is consistent with the decomposition result reported in our previous work. This indicates that the new algorithm is more powerful than what we developed before. Nevertheless, it should be pointed out that in Fig. 3 we do not show the steps to generate assisting mandrels and to fix those “hot” spots that may violate the lithography principles (e.g., resolution limit). For example, those features too close to each other may be merged together to form resolvable patterns. Another layout cell was also successfully colored and decomposed using a negative-tone SASP coloring algorithm. In Fig. 4, we only show one of six possible coloring schemes, namely, the scheme that was already reported in this conference last year.

9053-38, Session PWed

Work smarter not harder: How to get more results with less modeling

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In this paper we study the importance of accurate model-based simulation on characterization of the integrated circuit performance. We analyze device sensitivity to process variability and its impact on circuit timing. We show that only a small fraction of devices whose characteristics are significantly affected by process variability actually have correspondingly significant effect on the overall circuit performance. We suggest several ways to use this observation to improve robustness of circuits.

We see that a significant fraction of devices is affected by the layout context and should be considered sensitive. However, and it is especially true in large designs, only a small fraction of these devices is critical for the circuit performance. Obviously, to make the design more robust we have to avoid devices which are both sensitive and critical. One has several alternatives to achieve this goal:

1) Re-route the critical path to avoid the sensitive instance and instead use an instance that is not in the sensitive set. This approach attempts to modify the critical set to avoid overlap with the sensitive set.

2) Replace or improve sensitive critical instance with another cell that is less process sensitive. This attempts to remove critical instances from the sensitive set by reducing their process sensitivity.

We plan to further study feasibility of these and other approaches, as well as extend our analysis to more designs of different types.

We would like to also note that for most sensitive devices, the exact characterization of their parameters is not particularly important. This suggests that approximate modeling techniques can be used to speed up and simplify the simulation tools when they identify sensitive devices. Only once the set of sensitive and critical devices is identified, accurate modeling of those few instances becomes necessary.

9053-39, Session PWed

Scanner correction capabilities-aware CMP lithography hotspot analysis

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CMP effects on manufacturability are becoming more prominent as we move towards advanced process nodes, 28nm and below. It is well known that dishing and erosion occur during CMP process, and they strongly depend on pattern density, line spacing and line width [1]. Excessive thickness or topography variations can lead to shrinkage of process windows, causing potential yield problems such as resist lifting or printability issues.

When critical patterns fall into regions with extreme topography variations, they would be more sensitive to defects and could potentially become yield limiters or killers. Scanner tools compensate and correct topography variations by following the given profile [2]. However the scanner exposure window size is wider compared to local topography variations in design. This difference would generate new lithography focus sensitive weak points which may be missed. Experiments have been conducted as shown in Fig 1. Design under manufacturing has been subjected to scanner tool topography focus corrections. Despite of the corrections, Site B topography height has worsened while site A and C shown some improvements. As a result, additional improvements need to be done to meet manufacturability requirements.

In this paper, we will present the work done in GLOBALFOUNDRIES´ 28nm process targeted on topography induced lithography focus shifts. We will share the results on best focus exhibiting strong correlation to the CMP topography for a reference set of lithography critical patterns. The paper would propose how this CMP topography information can be utilized to derive layout or design changes to minimize the topography impact on depth-of-focus or process optimization to meet these challenges.

We will discuss following topics in this paper:

1) Correlation results between optimal focus selection and topography using same reference set of lithography critical patterns at high and low topography regions

2) Analysis and fixing focus sensitive lithography weak points at high or low and high to low topography transition areas based on scanner topography correction

3) Design-for-Manufacturing (DFM) recommendations[3] on reducing total topography variations to minimize the topography impact on depth-of-focus

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9053-21, Session 5

Pattern-based lithographic-target optimization using a predictive yield model

Rani S. Ghaida, Piyush Pathak, GLOBALFOUNDRIES Inc. (United States)

The modification of drawn layout shapes to improve the printability of lithographic target, commonly known as retargeting, is necessary to achieve acceptable yield and process window in today’s technology. Existing retargeting methods are generally classified into model-based and rule-based approaches. Model-based retargeting, which rely on simulation of the manufacturing process to guide iterative layout perturbations, are more accurate but have an underlying high computation cost making them impractical for full-chip application. In contrast, rule-based retargeting uses pre-defined rules that associate layout configurations with fixed layout perturbations. To keep the run-time reasonable, only a limited set of layout configurations, typically of limited complexity, can be covered by rules. This limitation introduces difficulty in addressing complexity associated with variable context for particular configurations and also introduces inaccuracy to the retargeting process. In this paper, we propose a methodology for pattern-based and context-aware retargeting guided by a predictive yield model. First, yield models are built for relatively simple layout configurations (e.g., tip-to-side configuration [d4] shown in Figure 1) along their dimension range. A pattern-yield model, combining individual yield models of layout configurations within the pattern and across its boundary, is developed and calibrated using printability simulation. The solution of layout-configuration dimensions corresponding to the case of maximum pattern-yield is determined and necessary layout perturbations are implemented. The proposed methodology was validated through a qualitative comparison of its results – when applied on critical patterns – to those obtained using model-based retargeting. The paper also includes a comparison of the methodology with rule-based and model-based retargeting to highlight its advantages and limitations.

9053-36, Session 5

Lithography yield estimation model to predict layout pattern distortions with a reduced set of lithography simulations

Sergio Gomez Fernandez, Francesc Moll Echeto, Juan Mauricio, Univ. Politècnica de Catalunya (Spain)

This paper proposes a yield estimation model to evaluate the lithography distortion in a printed layout. The yield model presented relates the probability of non-failure of a lithography hotspot (p_i) with the manufacturing yield loss. Note that we consider only as a hotspot those pattern constructs with excessive variation under lithography printing. Hence, the yield is computed as follows.

Ylh = p1•p2•••pNh = prod(p_i) = exp(-lambda_i)

where the parameter lambda_i represents the difficulty to print the hotspot (distortion). The lambda parameter is obtained through lithography simulations using the Process Variation Index (PVI) obtained with the LFD tool from Mentor Graphics. Since it is not possible to have an exact analytical expression that relates the lambda factor and the PVI index, we propose a simple function that relates the lambda parameter and the PVI index.

lambda_i = 0 if PVI_i <= PVI_min,

S*(PVI_i - PVI_min)/(1 - PVI_i) if PVI_min < PVI_i < 1

The PVI_min parameter refers to the minimum variation index that produces yield loss and the parameter S is a scaling factor that must be adjusted to give reasonable estimates of yield loss according to the technology employed and the process conditions. The scaling parameter S is obtained from the estimation of the yield of different layout styles. This yield estimation is obtained from delay measurements

of a test circuit implemented in a CMOS 40nm technology where the yield is defined as the number of circuits not meeting the given timing constraints. The measured chip contains the same test circuit implemented following two different layout styles, a totally 1D layout and a totally 2D layout to better predict the yield.

In a given layout there are millions of different pattern constructs which makes full lithography characterization unpractical. Therefore, to simplify and reduce the number of lithography simulations, we identify a number of relevant pattern construct classes. We propose a pattern simplification where we only consider the parts of the neighboring shapes that cause significant distortion (i.e. sharp shapes). Moreover, we consider that two pattern constructs are equal if they suffer the same type of degradation, i.e., if they belong to the same class. We consider 33 basic classes where the PVI of each class is computed through individual simulations and the PVI of other pattern constructs are estimated combining the simulated basic classes.

The yield estimation model can be employed to fairly compare the lithography distortion occurred on different layout configurations. We compared different circuits using a fully regular layout (F1D), 2D layout with poly 1D (H1D) and a fully 2D layout (F2D) for a 40nm technology node. Results show that the F1D has a nearly 20% yield improvement compared to the F2D layout design, but with the cost of an area overhead between 35-70% depending on the circuit. The H1D design achieves the same area results than the F2D but with only a 10% yield loss compared to the F1D and hence the H1D obtains the highest number of good dies per wafer (GDPW).

9053-23, Session 6

Technology-design-manufacturing co-optimization for advanced mobile SoCs *(Invited Paper)*

Geoffrey Yeap, Da Yang, Qualcomm Inc. (United States)

In the last six years since the advent of iPhone, there has been an explosive growth in smartphones with an insatiable demand for data speeds, device features, sleek form factor and longer battery life. The smartphones have evolved into the largest platform in the history of mankind, and become the product driver for the semiconductor industry.

Advanced mobile devices such as smartphones are complex systems with the overriding objective of providing the best user-experience value by harnessing all the technology innovations. Most critical system drivers are better system performance/power efficiency, cost effectiveness, and smaller form factors, which, in turns, drive the need of system design and solution with More-than-Moore innovations. We need to continue to drive increased requirements for processing and integration while maintaining low power and meeting thermal challenges through holistic system scaling.

In this talk, we highlight how the co-optimization strategy influenced architecture, device/circuit, process technology and package, in the face of growing process cost/complexity and variability as well as design rule restrictions. Examples will be provided to illustrate how choices are made in light of co-design of hybrid-design rules, transistor and BEOL metal/via stack and IP/core design requirements for optimal cost structure, power/performance, manufacturing yield ramp and time-to-market for 28nm, 20nm and 16/14nm.

9053-24, Session 6

Optimizing standard cell design for quality

Chi-Min Yuan, Dave Tipple, Jeff Warner, Freescale Semiconductor, Inc. (United States)

To date, majority of the papers presented in this Advanced Lithography conference focused on how to print smaller features, so a chip can accommodate more transistors and provide higher functionality. Consumer chips for personal computers and cell phones are two obvious examples of such chips, with smaller chip size and higher circuit speed being two primary characteristics. In a different market such as the safety-related automotive market, “smaller and faster” are replaced by “tougher and living longer”. Here, a chip has to endure a wide range of operating temperature from -40C to 150C, and have an extremely low field failure rate over 10+ years. To design such a quality-centric chip, different design techniques from those applied to consumer chips are required.

In this paper, we discuss some of the physical design practices we employed to improve the quality of a chip. The target designs are standard cell libraries, which are basic building blocks of a chip. The topics we plan to cover include

- optimizing pin design to improve routing accessibility and via redundancy,
- quantifying tradeoff between contact redundancy and cell speed, and
- fine-tuning cell designs with reliability-related design rules.

Also, standard cell libraries of 40nm with different design styles are benchmarked to show the difference in their design quality, and how they lead to final chips of different projected yield and quality level. An example of such benchmark is to study the PO pitch distribution from all standard cells in a library, as shown in Figure below. Even though these two libraries are designed with the same foundry design rules, different design strategies are used and so lead to different PO pitch distribution and thus CD variation. Chips designed with a library of larger CD variation will have a higher failure rate, especially at extreme timing corners, over the lifetime of a chip.

9053-25, Session 6

Analysis of process-induced electromigration and design-friendly compact model in 16nm FinFET SoC design

Yongchan Ban, Chang-Seok Choi, Yongseok Kang, Woo Hyun Paik, LG Electronics Inc. (Korea, Republic of)

Higher current density with technology shrinking causes the motion of metal atoms, electromigration (EM), in response to the electron current, and it can eventually cause a long term circuit failure through resistance increase or opens of metal interconnects. Therefore, EM becomes one of the utmost critical reliability challenges at high performance IC designs with deep-submicron process technologies.

Since the performance of a power network has a direct impact on overall timing and functionality, many researches have posed on a DC current induced EM of power/ground network. Meanwhile, an AC current induced EM on clock and logic signals becomes a significant problem even in the presence of reverse-recovery effect. Compared to power network, clock and logic signal interconnects are much narrower (mostly drawn up to the minimum width and space) and suffer from fast switching and large driving current from FinFETs. Thus, the high current density on those signal interconnects can cause a serious failure.

Moreover, the thin signal interconnects are prone to process variations: due to lithography and dry etch processes, the lines can be narrower or distorted against the design intent, and due to CMP (chemical mechanical polishing) process, the signal lines can be further shallower. Those horizontal and additional vertical thickness decreases exacerbate the signal EM problem. In sub-20nm node design, the signal interconnects are likely to be patterned with double patterning technique (DPT) with the two lithography and two etch processes. Since DPT essentially appends more variations due to subsequent process steps and non-uniform topography to be patterned, the signal line could be more exposed to EM failure and yield reduction.

In this paper, we analyse EM tolerance of signal interconnects, characterize process-weak (EM-weak) layouts and optimize our signal lines to mitigate EM problem in 16nm design. For applying to full-chip design, we propose a new compact model for fast estimating EM failure. A commercial tool is used in order to validate our compact model in EM

problem. Based on our compact model, we can easily detect the EM-weak signal lines and optimize them by avoiding EM-weak pattern during CTS (clock tress synthesis) and detail routing steps. Pattern matching technique is involved for filtering EM-weak patterns in our 16nm design.

9053-26, Session 6

Design technology co-optimization for a robust 10nm solution for logic design and sram

Boris Vandewalle, Bharani Chava, Sushil Sakhare, IMEC (Belgium); Mircea V. Dusa, ASML (Belgium)

With the density requirement expected for 10nm node the pressure on patterning continues to get higher. The front end of line adopting a regular layout (mostly unidirectional), most of the complexity needed for a functional chip ends up in the interconnect layer and Metal1. Assuming that Extreme Ultra Violet Lithography (EUVL) will not be ready for the early stage of 10nm production but expected only for high volume manufacturing, we proposed to study how we can extend the ArF immersion lithography for Metal1 to sustain the development of the technology as well as the early production phase, while remaining compatible to EUVL single patterning solution. We will show how close interaction between design, process and computational lithography lead us to a Metal1 triple patterning solution using Negative Tone Develop (NTD), and how the same design solution can be supported by EUVL single patterning. A peculiar attention will be port to line end printability performance (in both configuration: tip to tip and tip to line), since we believe it is a key parameter to define the best compromise between lithography performance and design density.

9053-27, Session 7

Physical verification and manufacturing of contact/via layers using graphoepitaxy DSA processes

Juan Andres Torres, Kyohei Sakajiri, Mentor Graphics Corp. (United States); David Fryer, Mentor Graphics Corp (United States); Yuri Granik, Yuansheng Ma, Mentor Graphics Corp. (United States); Polina Krasnova, Mentor Graphics Corporation (Russian Federation); Germain Fenger, Mentor Graphics Corporation (Belgium); Seiji Nagahara, Tokyo Electron Ltd. (Japan); Shinichiro Kawakami, Tokyo Electron Kyushu Ltd. (Japan); Benjamen M. Rathsack, Tokyo Electron America, Inc. (United States); Gurdaman S. Khaira, The Univ. of Chicago (United States); Juan J de Pablo, University of Chicago (United States); Julien Ryckaert, IMEC (Belgium)

For the past decade significant work has been done in the area of directed self assembly. Synthesis of materials permitting well controlled polymerization has permitted the evaluation of grapho and chemo-epitaxy processes, focusing in defectivity studies and parametric aspect ratio of the guiding patterns.

This paper extends the state of the art by describing the practical material's challenges, as well as approaches to minimize their impact in the manufacture of contact/via layers of random configurations using a grapho-epitaxy directed self assembly process.

Three full designs have been analyzed from the point of view of layout constructs. A construct is an atomic and repetitive section of the layout which can be analyzed in isolation. Specifically in the case of grapho-epitaxy, the effect of neighboring structures is limited to structures that occupy the same "DSA group". However, DSA groups are sensitive to the lithography process used for their manufacture.

Results indicate that DSA's promise to full chip production is mainly in its ability to be resilient to the shape of the guiding pattern across process window conditions, the paper present results that suggest that self assembly can still be guaranteed even with high distortion of the guiding patterns when the guiding patterns have been designed appropriately for the target process.

If DSA is coupled with a high resolution imaging system like EUV or direct write, it has the potential to give rise to pattern-matching based methods for design, physical verification and manufacture. However in this paper we focus on a 14 nm process based on 193i lithography. Due to the nature of the optical system we present evidence to the need of counting with DSA compliance methods and mask synthesis tools which consider the pattern dependencies of adjacent structures a couple of microns away.

Finally, an outlook as to the guidelines and challenges to DSA copolymer mixtures and process are discussed highlighting the need for larger molecular weight copolymers with a larger L0 or a mixture of homo polymer and diblock copolymer to reduce the number of defects of arbitrary hole configurations.

9053-28, Session 8

Automated fill modification to support late-stage design changes

Jeff S. Wilson, Mentor Graphics Corp. (United States); Greg Davis, Mentor Graphics Corp. (United States) and Design to Silicon (United States); Anderson Chiu, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan); Ricky Yang, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan) and Design to Silcon (United States); Yao-Jen Chuang, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

One of the most critical factors in achieving a positive return for a design is ensuring a design meets the performance specification, but also produces sufficient yield to meet the market demand. The goal of design for manufacturing (DFM) technology is to enable manufacturing requirements to be addressed during the design process. At advanced nodes, new manufacturing requirements such as double patterning compliance, and new design features such as FinFET transistors, increase both the complexity of metal fill placement and the sheer number of fill elements. While new cell-based, DP-aware, and timing-aware fill technologies have emerged to provide the designer with automated fill engines that support these new fill requirements. Design changes that arrive late in the tapeout process (as engineering change orders, or ECOs) can have a disproportionate effect on tapeout schedules, due to the complexity of replacing fill. If not handled effectively, the effects on file size, run time, and timing closure can significantly extend the tapeout process. Fill is required and done late in the design process so it will impact a customer's Time to market. The run time for fill is influenced by the performance of the fill engine, the efficiency of the fill rule deck, and the design methodology employed by the design team. File size is a critical factor in both run time and the ability to move fill databases between design environments. In this paper, the author examines changes to design flow methodology, supported by new fill technology, that enable efficient, fast, and accurate adjustments to metal fill late in the design process. We present an ECO fill methodology coupled with the support of advanced fill tools that can quickly locate the portion of the design affected by the change, remove and replace only the fill in that area, while maintaining the fill hierarchy. This new fill approach effectively reduces run time, contains file size, and minimizes timing impact, all of which are critical factors to ensuring time-to-market schedules are maintained.

9053-29, Session 8

Yield-aware decomposition for LELE double patterning

Yukihide Kohira, Univ. of Aizu (Japan); Yoko Yokoyama, Chikaaki Kodama, Toshiba Corp. (Japan); Atsushi Takahashi, Tokyo Institute of Technology (Japan); Shigeki Nojima, Satoshi Tanaka, Toshiba Corp. (Japan)

LELE type double patterning enables us to fabricate smaller features without using advanced technologies such as extreme ultraviolet (EUV) lithography. Recently, although triple patterning is often discussed, it is currently not easy to adopt it due to issues related to manufacturability such as misalignment of masks. In LELE type double patterning, a layout pattern is decomposed and assigned to two masks so that each can be formed on a wafer by an exposure. The yield which affects manufacturing cost much depends on a layout pattern decomposition. A layout pattern decomposition method needs to have an ability to obtain a layout pattern decomposition which achieves higher yield.

In layout pattern decomposition for LELE type double patterning, a component in a layout pattern can be partitioned into smaller features and features can be assigned to distinct masks. Adjoining features assigned to different masks are requested to have an overlap area, which is called a stitch, to take an overlay error into account. The existence of a stitch affects the yield since the actual wafer images are degraded even if OPC (optical proximity correction) is applied. Our problem is to find an optimum layout pattern decomposition that achieves higher yield.

In order to find a better layout pattern decomposition, various methods have been proposed. However, most of the existing methods do not take the yield into consideration but the minimum number of stitches. Moreover, how a stitch is inserted is not well-defined in these methods especially when a variety of widths of line patterns is large.

The minimum stitch length is usually given in the design rule. Although the higher yield is achieved if the minimum stitch length is set to large enough, there is a trade-off between the yield and the existence of decomposition. A stitch satisfying the minimum length constraint may cause a hotspot. A narrow short stitch is more fragile than a wide long stitch, and the yield degradation caused by a stitch is mitigated by increasing the length or area of the stitch.

In this paper, we propose an efficient algorithm which obtains a yield-aware pattern decomposition for LELE double patterning. First, stitch-candidates which help not to degrade the quality of wafer image are extracted. In our proposed algorithm, one stitch-candidate is defined in each interval where a stitch can be inserted without violating the design rule. A stitch-candidate may cross each other when the width of a line pattern is large, but is independent of other stitch-candidates, that is, no design rule violation occurs in any stitch selection obtained from the defined stitch-candidates. Then, a minimum cost stitch selection which derives a feasible yield-aware layout pattern decomposition is obtained from the stitch-candidates. By using the cost of a stitch which reflects the quality degradation on wafer image appropriately, a layout pattern decomposition which maximizes the yield is obtained by a minimum cost stitch selection. In our method, a stitch-candidate is defined when its length can be larger than or equal to the minimum length, and the cost of a stitch is defined by using the area of a stitch after assumed overlay error to reflect the yield degradation.

9053-30, Session 8

A generalized model to predict Fin-width roughness induced FinFET device variations using the boundary perturbation method

Qi Cheng, Jun You, Yijian Chen, Peking Univ. (China)

FinFET and Tri-gate MOSFETs has been adopted in IC fabrication owing to their superior gate control capability. However, process variations such as line edge/width roughness (LER/LWR) are a serious concern and will become more troublesome as devices are scaled down. There has been a long interest in device society to understand and model FinFET device variability, although its detailed introduction to lithography engineers occurred only recently. On the other hand, the reported model was still incapable of directly correlating the current fluctuation with fin width roughness (FWR). Even it can be used to predict the potential variations, tedious calculations of the induced current fluctuation do not help us to gain much insight into their physical correlation. Therefore, in this paper we shall present a generalized model to correlate FWR with FinFET current variations using the boundary perturbation method.

As shown in Fig. 1, the line width roughness will result in continuous (spatial) variation of the fin width along the channel of a FinFET. Following our previous model, the electric potential ϕ in a FinFET channel (with FWR) is separated into $\phi 0$ and $\phi 1$, as shown in table 1. The zeroth-order solution ($\phi 0$) corresponds to the no-FWR device behavior and the first-order solution ($\phi 1 \ll \phi 0$) describes the FWR effect. Correlating the electric potential variation with drain current fluctuation is achieved by introducing some approximation shown in table 1. FWR induced drain current fluctuation ΔIds is analytically derived and shown in equations (1)-(2). Fig. 2 is a flow chart demonstrating how ΔIds is calculated using the boundary perturbation method (e.g., the 0th order Poisson's equation and 1st order Laplace equation, as well as their boundary conditions). The total electric potential is: $\phi=\phi 0+\phi 1$, and ΔIds can be readily calculated by inserting $\phi 0$ and $\phi 1$ into equation (1) (see Fig. 2). Other key device parameters such as subthreshold slope (S.S.) and DIBL can be solved based on ΔIds.

A typical low-frequency FWR fluctuation shown in Fig. 3 is used in our model calculation and TCAD simulation. The potential along the channel direction (0,y) at the middle of fin (x=0) are compared with TCAD simulation in Fig. 4(a). Re.1 is defined in (3) as the relative error (compared with TCAD simulation) of the electric potential calculated by our model, reaches its maximum value at about y=7 nm (Fig. 4(b)). Fig. 5 shows the accuracy of the approximate formula (4) of the inversion charge density, described by Re.2 in (5). Apparently, higher Vg values result in more significant errors of the inversion charge density in the channel. ΔIds defined in (1) for various device parameters are verified with TCAD simulation in Fig. 6, which shows a satisfactory agreement. It is evident that the accuracy of our model decreases with the amplitude of FWR fluctuation, while affected by the doping concentration and oxide thickness as well. More calculation results and discussions about the current fluctuation will be reported in the paper.

9053-31, Session 8

Hotspot fixing with localized layout modification technique for litho-etch-litho-etch double patterning

Yoko Yokoyama, Keishi Sakanushi, Toshiba Corp. (Japan); Yukihide Kohira, Univ. of Aizu (Japan); Atsushi Takahashi, Tokyo Institute of Technology (Japan); Chikaaki Kodama, Toshiba Corp. (Japan); Satoshi Tanaka, Shigeki Nojima, Toshiba Materials Co., Ltd. (Japan)

It has been a long time since single patterning with an ArF immersion exposure tool reached its physical limit. Double patterning technology (DPT) is one of the promising techniques for 28nm technology node and beyond. For Litho-Etch-Litho-Etch (LELE) process, layout design needs to be decomposed into two masks and lithography and etching process are proceeded twice respectively. Comparing other types of DPTs, LELE type DPT is known to have an advantage of layout flexibility.

Even with matured design rules, OPC, and process recipe, it is known that there is always a risk of hotspots especially for advanced technology nodes. For LELE, there are two problems when a hotspot, which is not fixable by tuning OPC, is detected on a wafer or during verification by lithography simulation for a decomposed mask. One is repeating a data preparation flow including decomposition, OPC, and verification by lithography simulation is quite time consuming. This is because even

small layout modification may cause influence layout decomposition over a whole area. The other is a risk to introduce new hotspots at different locations. After re-decomposition of layout to fix detected hotspots, brand new hotpots may be detected where there is initially no hotspot, which makes it very difficult to completely eliminate hotspots. Considering two problems mentioned above, conventional concept of hotspot fixing is inefficient and a new way to solve the problems are required.

In this paper, a new method to fix hotspots with layout modification of limited area is presented. A space between neighboring polygons at hotspots are examined and classified based on its design regulation. Using the obtained information, polygons creating a hotspot and their surroundings, which don't affect layout decomposition of a whole area, are extracted and called "unlocked" polygons. Those polygons in "unlocked" region are tried to be modified by shifting positions, changing shapes, being assigned to another mask, or split into two masks with stitches without affecting "locked polygons" in a strategic way in order to fix hotspot.

Once influence on layout decomposition is localized and re-decomposition of a whole area becomes unnecessary, layout decomposition, OPC, and verification by lithography simulation require only for a limited area around hotspots. Therefore, the proposed method can reduce not only turnaround time to fix a hotspot but also the number of iterations since it prevents generation of hotspots at new locations.

Conference 9054: Advanced Etch Technology for Nanopatterning III

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9054-1, Session 1

Model-aided plasma process development: met, unmet and to be made promises *(Keynote Presentation)*

Mark J. Kushner, Univ. of Michigan (United States)

The development of plasma processes is increasingly being aided by first principles modeling of reactor and feature scale phenomena. While past promises of fully integrated plasma based CAD tools have perhaps not been met, unexpected insights and guidance from modeling have greatly enhanced the development process. In this talk, progress in the use of modeling in process development will be briefly reviewed with emphasis on more recent advances addressing scaling of plasma tools to 450 mm, influence and control of VUV fluxes in conductor and dielectric etch, and control of reactant fluxes through the use of pulse power.

9054-2, Session 1

Where is plasma patterning going from here? *(Keynote Presentation)*

Ying Zhang, Applied Materials, Inc. (Taiwan)

Plasma etching has been taking more critical roles in nanopatterning started around ~45-32nm nodes. If dimension shrinking into deep nanometer regimes is a given, the main reasons for plasma etching being more critical are: (1) the lithography technology trend changed its slope by having introduced “double/multiple patterning” schemes; (2) variety of new materials have been used, such as high-k metal gate and its related integration schemes, e.g., gate last approaches, or SiGe, and III-V compound semiconductor materials; and (3) 3D transistor structures, e.g., FinFETs, or 3D NAND flash memory cells, have been replacing traditional planar devices. With these 3 reasons being continued to expand at fast speeds as technology nodes moving to 10nm, 7nm and beyond for density, device performance, and power reductions, what are the key challenges for plasma etching patterning? Can process fine tuning based on current plasma etch tool technologies alone be able to carry out tasks for the industry to extend to 7nm, 5nm, and beyond? Do we truly need any new type of plasma sources, such as “low electron temperature” types of plasma sources to realize some challenging tasks, e.g., Atomic Layer Etching (ALE)? In this talk, some of the key challenges and perspective solutions on processes, process integrations, plasma etching systems, based on the above listed 3 reasons will be reviewed and discussed.

9054-3, Session 1

Fabrication challenges in patterning of 12nm half-pitch ultralow-k dual damascene copper interconnects *(Invited Paper)*

Jasmeet S. Chawla, Alan Myers, Richard Schenker, Kanwal Jit Singh, Robert Turkot, Hui Jae Yoo, Intel Corp. (United States)

We demonstrate an integrated process flow for electrically yielding 12 nm half-pitch dual damascene interconnect structures in ultralow-k interlayer dielectric (ILD) and copper based metallization. The patterning is realized by spacer based pitch quartering scheme using standard 193 nm immersion lithography. In this presentation, we focus on process issues in fabricating sub-17 nm interconnect features like line undulation, line collapse, pattern asymmetry, via bottom corrosion and pattern distortion by metal fill. We identify key defect modes and provide solution paths for these process issues to result in functional interconnect.

Line undulation results when the strength of the ILD being patterned cannot withstand the stress of the sacrificial hardmasks (HMs) during the patterning process. Driving force of line undulation is directly correlated to the mechanical properties like elastic modulus and stress build-up during patterning of HMs and ILD. Mechanical properties of ILD and HMs are shown to depend on process conditions like plasma etch and ash chemistry.

Line collapse is observed post wet clean processing of ILD during trench and via patterning. Line collapse is demonstrated to increase with decrease in ILD mechanical strength, increase in pattern aspect ratio, non-uniform drying, and decrease in contact angle of the wet chemical on dielectric material.

Pattern asymmetry, or unequal trench CDs, is inherent to spacer based pitch quartering patterning scheme that results in three different trench widths. Symmetric patterning is enforced by over tightening the control limits of patterning processes like deposition thicknesses and etches of backbone, spacers and hardmasks.

Aggressive scaling of via sizes requires using aggressive dry and wet etches that increases the metal corrosion at via bottom than previous generations’ schemes that can be solved by an improved integrated via etch and cleans flow. Sub 17 nm feature scaling and use of mechanically weaker ultralow-k ILD also amplifies the impact of plasma based metal fill on patterned dielectric. Metal fill results in distortion of the pattern (ILD height shrink, CD increase) if using aggressive plasma gas chemistry and power.

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9054-5, Session 2

Effect of etch pattern transfer on local overlay margin in 28nm GATE integration

Onintza Ros, Pascal Gouraud, Bertrand Le-Gratiet, STMicroelectronics (France); Erwine Pargon, Lab. des Technologies de la Microélectronique (France); Christian Gardin, Julien Ducoté, STMicroelectronics (France)

One of the main process control challenges in logic process integration is the contact to gate overlay. Loads of efforts have been done in run to run (High order process corrections) and scanner control (baseliner control loop) to keep overlay within the very tight specifications defined; such as, 7nm mean+3sigma.

Thorough budget breakdown, along with proper in line overlay metrology, secures overlay control and yield. However, despite the many improvements done at lithography level, still several stringent yield/ overlay limitations are seen.

It is known that process integration can lead to specific overlay distortion (CMP, thermal treatment etc…) which are usually partly handled by high order process corrections at scanner level. In addition, recently we have shown that etch process can also lead to local overlay distortions, especially at the wafer edge [1].

In this paper we dig into another overlay distortion level which can happen during etch processes. We will show that resist cure steps during gate etch processes affect lithography defined profiles leading to local pattern shifting. This so-called gate shifting is being characterized by etch process partitioning during a typical High-K metal Gate patterning with spin-on carbon and SiARC lithography stack onto a high-K metal gate / polysilicium / oxide hard mask stack.

We will show that modifying the resist-cure / SiARC open chemistry strongly contributes to gate shifting reduction by an equivalent of 3nm overlay margin.

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9054-6, Session 2

Gate double-patterning strategies for 1Xnm node FinFET devices

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The purpose of this work is to develop a double patterning strategy resulting in polycrystalline silicon (poly-Si) gate lines with a critical dimension (CD) of 20nm at pitch 62nm for 1x technode FiNFET devices.

From bottom to top, the gate stack features the poly-Si layer to be patterned, a conventional mask of 40nm silicon dioxide and 70nm amorphous carbon (a-C). On top of the a-C, the hard mask (HM) is the level in which the double patterning is defined, before transferring the pattern to the underlying layers. A first lithography step defines the photoresist (PR) lines necessary to pattern the gate. A first etch aiming at transferring these lines into the HM is then applied. After stripping the resist, a second lithographic exposure is applied, resulting in a pattern whose purpose is to cut the lines defined at the previous stage. It is only after the second etch and strip that the rest of the stack can be etched further.

The second patterning of the process described above relies on the use of 193nm PR. Given the fact that the pitch is as small as 62nm, the first image of the double patterning exercise must however be printed with extreme ultraviolet (EUV) lithography. This exposure results in rough resist lines which have a CD of 28nm and a thickness of 60nm. The use of EUV thus imposes a triple challenge to the corresponding etch step. First, the photoresist budget is significantly reduced with respect to the previous node. Second, the line width roughness (LWR) of 5.5nm measured on the EUV PR must absolutely be reduced for gate applications. Third, the CD of the lines must be reduced from 28nm in the resist to 20nm below.

This work focused on possible solutions to overcome these three challenges. To do so, different HM stacks and patterning strategies have been investigated. Their influence on the efficiency of the pattern transfer, on the uniformity on 300mm wafers and on the LWR values have been studied. The process ultimately chosen addresses the limited PR budget by having a very thin SiOC HM top layer ; once the top layer is opened, an etching chemistry perfectly selective to this first HM material must be used to open a thicker layer which constitutes the bulk of the HM stack. Combining this approach with a pre-etch plasma curing of the EUV PR allowed a successful pattern transfer with LWR values improved by ~30%. As far as the lateral dimensions are concerned, spreading the CD reduction on several layers of the stack allowed to obtain gates of 20nm width.

9054-7, Session 2

28nm FDSOI high-k metal gate CD variability investigation

Latifa Desvoivres, CEA-LETI-Minatec (France) and STMicroelectronics (France); Pascal Gouraud, Bertrand Le-Gratiet, Régis Bouyssou, Rossella Ranica, Benjamin Dumont, Isabelle Thomas, STMicroelectronics (France)

Contrary to 28nm bulk technology, 28nm FDSOI technology presents simple architecture and performs better devices performances. 28nm FDSOI devices highly depends on gate CD morphology because electrical effective gate length is driven by metal gate CD. High-k metal gate etching is therefore a key point to achieve these requirements. As standard gate first integration is used, developing a gate etch process becomes more and more critical. Gate profiles and metal gate CD control are mandatory and variability has to be mimimized across the wafer (WiW), wafer to wafer and lot to lot.

In this paper, we will focus on metal gate CD variability investigation. Once polysilicon gate profiles are frozen, metal gate profiles adjustement is achieved, based on scatterometry metal gate profiles measurements, TEM analysis and electrical results*. Thanks to this methodology, a metal gate etching process has been tuned on 300mm industrial platform LAM Kiyo CX and EX tools.

This work was perfomed at ST Crolles 300 facility in collaboration between STMicroelectronics & CEA/LETI.

*28 nm FD-SOI Metal GATE profile optimization, CD and undercut monitoring using Scatterometry Measurement, R. Bouyssou, B. Le Gratiet, P. Gouraud, L.Desvoivres, G. Briend, B. Dumont, 2013 SPIE proceddings.

9054-8, Session 2

Highly-selective etch gas chemistry design for precise DSAL dry development process

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To meet the needs of the device scaling trend, patterning technologies for critical dimension control less than 20 nm is required. For 1X nm pattern formation beyond the conventional optical lithography limit, it is necessary to use double (or multiple) patterning process which increases the process cost. Directed-self assembly (DSA) of block copolymer is one of the most attractive candidates for 1X nm pattern formation process and 12.5 nm hp patterns are formed using polystyrene-block-poly(methyl methacrylate) (PS-b-PMMA) [1]. DSA lithography?(DSAL) process using PS-b-PMMA needs selective removal of PMMA to PS, which is called “development process”. A wet development process is applied successfully for contact hole shrink process [2]. Although this method can remove PMMA selectively, pattern collapse will occur for line and space pattern resulting from surface tension of developer solvent.

On the other hand, although a dry development process is expected to solve this problem, selective removal of PMMA is difficult because PMMA is a similar organic polymer to PS. Dry development processes using Ar plasma and O2 plasma have been reported and their selectivities were 3.9 and 1.7, respectively [3]. However in our case, higher selectivity is needed for etching the underlayer with PS as mask.

In this study, we focused on the difference in the oxygen contents of PS and PMMA. PMMA has more oxygen in the film than in PS, so we designed the gas chemistry to realize the selective PMMA etch by using this difference of the oxygen content. We studied carbon containing gas plasma, because carbon radical will deposit on PS which does not contain oxygen. On the other hand, carbon radical will react with the oxygen in the PMMA to make volatile COx, therefore selective PMMA etch to PS can be realized. Carbon containing gases CO and CO2 were

selected and compared with O2.

PMMA and PS thin films were formed on Si wafers to evaluate blanket film etch rates. The thickness of PMMA and PS pristine films were 340 nm and 240 nm, respectively.

We used 100 / 13.56 MHz dual frequency superimposed (DFS) capacitive coupled plasma (CCP) system[4]. The film thickness was measured by ellipsometry to obtain the etch rate and selectivity.

Etch rates of PS and PMMA using O2 plasma were 375 and 880 nm/min, respectively, so selectivity was 2.3. In the case of CO2 plasma, selectivity was 2.5 which is a little larger than O2 plasma. In the case of CO plasma, both the etch rates of PMMA and PS decreased drastically. The etching of PS stopped, and highly selective PMMA etch to PS was achieved.

DSA lithography dry development of hole shrink pattern was successfully realized by designing the etching gas chemistry based on the difference of material structure of PS and PMMA.

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9054-26, Session 2

Line-width roughness reduction strategies for patterns exposed via electron-beam lithography

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With the constant down-scaling of features in the semiconductor industry, Line Width Roughness (LWR) is considered as the factor limiting the miniaturization. In recent years, several papers showed the importance of LWR reduction in order to meet the ITRS[a] requirements for the sub-22nm technological node (sub-2nm LWR). This topic is well documented for Extreme Ultra Violet (EUV) lithography, which is currently the most mature next-generation lithography (NGL) technique. In this article, we assess the capability of ebeam/multibeam lithography, which remains a serious competitor for NGL, to print 32 nm half-pitch line and space resist patterns with the lowest LWR. We propose several strategies including the writing strategies and the introduction of underlayers, to reduce resist pattern LWR. We also investigate the effect of post-lithography treatments to mitigate the resist LWR. Finally, the transfer of the reduced resist pattern LWR is evaluated during the subsequent plasma etching processes involved in the gate stack patterning.

All the exposures of this study are made with a Vistec shaped-beam tool SB3054DW with an acceleration voltage of 50kV. The resist used is the current reference resist (positive CAR) designed for the 5kV multi-beam lithography Mapper equipment. The plasma etching transfer into the gate stack is performed in a DPS II Centura 300 inductively coupled plasma etch tool from Applied Materials. The final objective is to transfer the complete protocol developed on 50kV exposures to 5kV multi-beam exposures. All the LWR measurements are made with a Hitachi CDSEM HCG4000 and a power spectrum density fitting method is used to obtain unbiased values of LWR[b] as well as spectral information on the LWR.

The experimental results show the effectiveness of writing strategy using biased patterns to decrease the resist pattern LWR. Various post-lithography processes (such as thermal processing, plasma treatments, and in-track surfactant rinse) already developed for 193-nm methacrylate based photoresists[c] were tested on the ebeam resist used in this study. Surprisingly, plasma treatments such as HBr or H2 plasmas that were very efficient to decrease 193nm PR pattern LWR[d],[e] have no significant impact on this ebeam resist. In our case, thermal processing is the most promising post lithography treatment with a 20% LWR decrease. Other post-lithography treatments combining several strategies together are under investigation to push further the limit of ebeam resist LWR mitigation.

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9054-9, Session 3

Advanced patterning: plasma etch challenges and solutions *(Invited Paper)*

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Innovative approaches are required in logic and memory device and backend patterning of the sub 20 nm nodes. Double and multiple patterning are being used for an unprecedented number of layers. The approaches depend strongly on the particular integration schemes and device requirements. All have in common the drive for a new level of precision, repeatability and productivity.

In this paper, plasma etch solutions to meet these stringent requirements for global and local CD uniformity as well as repeatability with high productivity will be presented. A new level of control and repeatability of all critical etch process parameters in the space and time domain has been achieved by combining hardware, process and software into a system level approach. Reaction conditions are being controlled locally across the wafer to achieve results that respond to the performance requirements upstream and / or downstream in the process flow. At the same time, wafer to wafer repeatability and chamber matching require minimum hardware variability and carefully engineered process sensitivities. Line edge and width roughness requirements demand that the etch process reduces the incoming values for a wide range of frequencies. This translates into a need to increase the accessible process window.

These advances allows advanced plasma etch reactors to play an increasingly important role in the patterning process in close interaction with lithography and deposition technologies.

9054-10, Session 3

30nm pitch compatible, stepwise hydrogen anneal for LER reduction of silicon nanowires *(Invited Paper)*

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Future scaled CMOS technology beyond FinFET or tri-gate will require that the gate be fully wrapped around the channel, due to the improved electrostatics afforded by this geometry. A gate-all-around (GAA) structure by its nature typically requires that the nanowire channels be suspended prior to gate stack deposition. Successful fabrication of suspended nanowire arrays is therefore a prerequisite to the implementation of GAA devices.

To achieve competitive current density, however, a dense array of nanowires is needed. Patterning of tight pitch array poses many challenges. When the pitch is reduced, line width and edge roughness (LWR/LER) of the pattern is increased due to resist scumming. This increased LER can be a significant fraction of the required critical dimension, leading to line merging or breakage. Even with optimized

conditions for resist patterning and pattern transfer, reducing LER below 1 nm remains difficult.

Further LER reduction, however, could be accomplished by smoothening of the patterned SOI itself. While hydrogen anneal has been shown to smoothen silicon fins and suspended silicon nanowires, its application for pitches below 50 nm is limited. The situation is even more difficult for fully suspended structures required for GAA devices. This is due to the fact that hydrogen annealing process is not self-limiting, and silicon diffusion is accelerated at high curvature, rough surfaces. With the increased LER at reduced pitch as well as the fact that suspended nanowires have all of their surfaces free for silicon diffusion, dense arrays of nanowires are often destroyed by agglomeration during the smoothening process.

To address this issue, we develop a novel, stepwise LER smoothening process compatible with nanowire pitches below 50 nm. The hydrogen annealing is done in two steps. In the first, non-suspended anneal, only silicon from sidewalls are allowed to move. This is followed by the second, suspended anneal; where silicon from all surfaces are free to redistribute. During the first anneal, where the top and bottom surfaces are pinned by hardmask and bottom oxide respectively, the high spatial frequency roughness of resist LER transferred into the SOI sidewalls is smoothened into long-range, smooth steps. These side-smoothened nanowires are then fully suspended before the second anneal. Since silicon from all surfaces is now free to redistribute, further smoothening and reshaping of the nanowire profile can be obtained. More importantly, with the pinch-off points removed by the first anneal, nanowires are able to withstand this suspended anneal without agglomeration and breakage.

With this sequence, all lithographically yielding nanowire arrays can be smoothened, even with the increased LER at reduced pitch. We successfully fabricate ultra smooth, suspended nanowires with pitches down to 30 nm and LER better than 0.8 nm (SEM instrument limit). In addition, this technique should still be applicable to patterned pitches beyond the current lithographic limit, as well as possibly to other crystalline channel materials.

9054-11, Session 3

The influence of the initial LWR, CD, and EUV-resist composition on LWR evolution by H2 plasma treatment

Peter De Schepper, Efrain Altamirano-Sánchez, Terje Hansen, Stefan De Gendt, IMEC (Belgium)

Extreme UV-lithography and the developed photoresist-material for sub-32nm features face many challenges. Controlling line edge and width roughness has become such key challenge. In order to meet the ITRS specifications a drastic LWR-improvement is needed. Experimentally, it has been demonstrated that plasma treatment can improve the LWR. The best LWR that currently can be achieved with EUV lithography is around 3 nm for 30nm lines and spaces. In particular, plasmas are known to modify the chemical and structural properties of 248nm en 193nm photo resist through synergetic interaction between VUV irradiation and plasma's reactive species. However, also plasma treatment is making slow progress in mitigating LWR sufficient to meet the requirements. Therefore, more fundamental research is needed to determine the key-contributors of this LWR convergence. Extensive research showed already the influence of various plasma conditions/chemistries and chemical conditions on the roughness mitigation of both 248nm and 193nm photo resist technology.

This paper will show the roughness mitigation of 30nm lines after H2 plasma treatment. The exposed EUV samples were generated with the state of the art ASML NXE:3100 scanner. Preliminary results (supporting figure 1c and d) indicate the influence of initial LWR and CD-results on roughness reduction after H2 treatment . In addition, changes in LWR, focused on 30nm lines and spaces, are correlated with the chemical properties and morphological stability of the EUV photoresist polymers (supporting figure 1a and b).

Moreover, blanket resist samples are used to correlate the EUV-resist compositions with the improvement of roughness after plasma treatment. The EUV photo sensitive polymers, through the use of various (wavelength) filters, were selectively exposed to H2 plasma species including photons in the VUV wavelength range. Furthermore, spectroscopic ellipsometry (SE), atomic force microscopy (AFM), Fourier-transformed infrared spectroscopy (FTIR), Raman spectroscopy, x-ray reflectivity (XRR), x-ray photoelectron spectroscopy (XPS) and glass transition temperature (Tg) characterization will be used to confirm the changes in chemical properties of these EUV photo sensitive polymers. Also the correlation between these chemical changes and the roughness improvement will be presented. The experimental results in this work provide new insight into the understanding of LWR-evolution.

9054-12, Session 3

Line roughness formation during plasma etching: mechanism and reduction

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In this paper, the effect of plasma etching on Line Width Roughness (LWR) is presented and compared by using conventional SiO2/Si3N4/SiO2 (ONO) hard mask combined with or without a-Si capping layer to achieve ultrafine and smooth sub-30nm gate for nanoscale devices. The authors have investigated the evolution of the LWR from e-beam lithography to subsequent plasma etching processes including hard mask opening and poly-silicon gate patterning. It was found that severe roughness was formed on the gate lines when PR patterns were directly transferred into underlying ONO hard mask stack even if fairy high etch selectivity of SiO2 and Si3N4 to PR can be achieved by optimizing process parameters. Thus, the final poly-silicon LWR directly is strongly dependent on the lithography and plasma etching steps preceding the gate etching. The formation of severe roughness can be attributed to following causes a) weak etch resistance of PR due to fairly thin thickness to achieve high resolution, b) rough poly-silicon surface plays a significant role and it can affect etching profile of hard mask stack and end point detection. In particular, incoming ions can be deflected to strike at both PR and hard mask sidewalls, which leads to a fast etch in the side direction by ion bombardment during plasma processes, and c) after hard mask opening, its etching profile is not irregular and asymmetric due to rough poly-silicon surface effect, which leads to more severe roughness when hard mask result is transferred into underlying poly-silicon gate. By introducing a-Si capping layer, PR patterns can be firstly transferred to the material by using HBr/O2 plasma, such that etching effect of PR to hard mask can be reduced greatly. Hard mask etching shows a smooth line without any deformation responding to a decreased LWR. On the other hand, by replacing poly-silicon with a-Si material, both deflected ions and hard mask etching effects on subsequent gate patterning can be negligible, such that LWR of hard mask and final gate lines can be minimized significantly.

9054-13, Session 4

Plasma etching and integration challenges using alternative patterning techniques for 11nm node and beyond *(Invited Paper)*

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For 11nm and below, several alternatives are still potential candidates to meet the patterning requirements [1]. Spacer patterning, Mask Less Lithography (ie ebeam lithography) and Direct Self Assembly are

alternatives under development at CEA-LETI. We have demonstrated the integration of these alternative techniques in front end of line and back end of line levels [2, 3, 4]. Common challenges such as minimum achievable CD, CD control through the integration steps, mask budget and LWR were compared for these alternatives techniques.

First we will present an example of spacer patterning integration in the case of Fin etching for Tri-gate on SOI technology. CD lower than 10nm (Figure 1) were achieved by optimizing the spacer patterning integration flow. We had to consider the impact of the non-symmetrical spacers on the micro-loading effect during the Si Fin etching step. We have compared two integration schemes, with and without additional layer in the stack (buffer layer), in term of CD control and profile.

Then, the work done on ebeam lithography will be reviewed by giving an example for 11nm High K Metal Gate patterning. Due to lower resist budget compared to optical lithography, the CD control in the case of ebeam lithography couldn't be achieved with a resist trim only approach. Thus, Additional steps were developed to reduce CD down to 11nm (Figure 2). A review of the etching sequence will be detailed

Finally recent progress on DSA integration at the contact / Via level will be presented. Our DSA process is based on graphoepitaxy approach by using PS-b-PMMA block copolymer from Arkema. After a selective removal of the PMMA block, we etch the brush layer and transfer the DSA pattern into a stack composed of a trilayer and metallic or dielectric under layers (Figure 3). Several challenges such as CD control, pattern fidelity and integration robustness will be discussed

To conclude, spacer patterning, maskless lithography and DSA are very promising techniques. Specific etching process steps and integration modifications were developed at CEA-LETI to integrate these techniques successfully in a CMOS flow.

The work on Spacer patterning and ebeam lithography was performed as part of the IBM-STMicroelectronics-CEA/LETI-Minatec development alliance. The work on DSA was performed in the frame of the IDEAL collaborative program.

9054-14, Session 4

Double patterning strategies for advanced CMOS processing *(Invited Paper)*

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As described by the ITRS roadmap and Moore's law the dimensions for semiconductor structures reduce steadily. Smaller pitches require advanced lithography in order to be resolved. At todays date, pitches of the order of 45 nm even challenge EUV based lithography and overlay performance. Hence, double patterning approaches like Self Aligned Double Patterning (SADP) and Litho-Etch-Litho-Etch (LELE) are established. Several additional prints like, core, cut, pad or block are required to pattern the FEOL and BEOL structures. Double patterning at contact level results in an integration area called Middle of Line Patterning (MOL). The multiple patterning and the reduced resist thickness require advanced stacks and etch approaches. Within this presentation the different approaches and results used in a N28 till N10 logic technology are shown. At fin etching the intrinsic asymmetry caused by a double patterning will be discussed. For gate etching the choice of hard mask stack to achieve 20 nm gates will be explained. At MOL a triple 193i patterning is used in combination with a self-aligned contact etching. Finally, a possible scheme for making SADP based dual damascene structures is explored.

9054-15, Session 4

Etch challenges for DSA implementation in CMOS via patterning

Patricia Pimenta Barros, Sebastien Barnola, CEA-LETI (France); Ahmed Gharbi, CEA-LETI-Minatec (France); Maxime Argoud, Isabelle Servin, CEA-LETI (France); Xavier Chevalier, ARKEMA SA (France); Christophe Navarro, Arkema S.A. (France); Eugenie Martinez, Commissariat à l'Énergie Atomique (France); Raluca Tiron, CEA-LETI-Minatec (France)

The optical limitations of standard lithography lead to investigate other patterning techniques for the future technological nodes (sub-14nm). Among the different approaches explored, Directed Self-Assembly (DSA) of block copolymers is one of the most promising solutions due to its simplicity and its low manufacturing costs [1].

We previously demonstrated that cylindrical block copolymers can be implemented in via patterning level on 300mm wafers, by using graphoepitaxy technique [2]. This approach allows to shrink lithographically defined contact holes or to generate contact multiplication with high resolution holes (~15nm).

In this paper, we will present recent progress to achieve a robust etch process for the transfer of DSA via patterns in usual CMOS integration flows. The implemented DSA process is based on a graphoepitaxy approach by employing an industrial PS-b-PMMA block copolymer from Arkema with a cylindrical morphology. After a selective removal of the PMMA block, we etch the brush layer and transfer the DSA pattern into a stack composed of a trilayer and metallic or dielectric underlayers (fig. 1). All results presented here have been performed on the DSA Leti's 300mm pilot line.

The first challenge for a robust DSA etch process involves in removing all PMMA block before transfer. In our process baseline, an acetic acid treatment is carried out to open PMMA holes. However, current studies showed that PMMA is not totally removed by only acetic acid treatment [2, 3]. Furthermore, this kind of wet development is not compatible with NTD resists which could be used for graphoepitaxy techniques in some integration flows. That's why we also investigated the possibility to remove all PMMA block by only dry etching. Chemistries based on H2 or CO gas have been studied for a selective dry removal and seem to be very promising (fig. 2). We have compared the performances of different dry PMMA removals with acetic acid developments. In this study, the potential of a dry PMMA removal have been shown for cylindrical PS-b-PMMA copolymers but it also could be used for lamellar PS-b-PMMA copolymer for which wet development causes collapse issues [4].

Then, the transfer of DSA via patterns will be discussed in terms of CD control, pattern fidelity and PS film thickness to achieve good etching performances. A study of CD uniformity and defectivity has been addressed to evaluate the process window of DSA approach after graphoepitaxy and after etching. We especially had to optimize the brush layer etching step by investigating new chemistries to better control CD and thus to increase our process window (fig.3).

Finally, the transfer of DSA patterns into complex stacks composed of SiN, SiO2 or TiN has been explored and demonstrated the capacity to implement block copolymers in different CMOS integrations (fig.4). The several etching processes developed here have successfully demonstrated the possibility to use PS-b-PMMA copolymer lithography for CMOS via patterning level.

The research leading to these results has been performed in the frame of the industrial collaborative consortium IDeAL.

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9054-16, Session 5

Large-radius neutral beam-enhanced chemical vapor deposition process for non-porous ultra-low-k SiOCH *(Invited Paper)*

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In accordance with the shrinking of ultra-large-scale integrated devices, a porous carbon-doped silicon oxide (SiOCH) dielectric has been developed. However, there are a lot of problems in the integration process due to the insufficient modulus of the SiOCH film with high density pores. To reduce the pores while keeping a low k-value, orientation polarization of SiOCH has to be minimized by controlling the symmetric molecular structure precisely. Neutral beam enhanced CVD (NBECVD) was well-known as the best way to control film structure and obtained SiOCH by eliminating plasma damage. However, there was not sufficient discussion about the pores in SiOCH and molecular structure. In this study, to control molecular structure in film for eliminating pores keeping low-k value by controlling the neutral beam energy and design of the chemical reaction, we developed a large-radius (370mm) neutral beam source.

For a practical NBECVD system, a large-radius neutral beam source has been developed. It consists of a large-diameter microwave plasma (MWP) source and a CVD process chamber to form SiOCH as shown in Fig. 1. The Ar neutral beam is generated from Ar ion in a MWP through the carbon plate, which has many apertures. Furthermore, in order to control Ar neutral beam energy precisely, RF (150 kHz) power is applied to the aperture plate. Then, UV and electrons from the plasma is cut off completely by the aperture plate. Dimethoxy tetramethyl disiloxane (DMOTMDS) was used as a precursor has a symmetric molecular structure composed of four Si-CH3 and two Si-O-CH3 bonds in Fig. 2. The Ar neutral beam is irradiated to Si wafer surface while directly injecting the precursor to the Si wafer surface in the CVD process chamber. Therefore, the molecular structure of DMOTMDS is maintained during deposition due to avoiding any damage from plasma and polymerization is promoted by only kinetic energy of Ar neutral beam.

Following adjusting Ar neutral beam energy by RF power and chemical polymerization path by adding hydrogen gas, non-porous SiOCH (NP-SiOCH) with high mechanical strength could be realized as shown in Table I as compared to general porous SiOCH. The electrical properties, pore diameter and mechanical strength were measured by mercury probe, small angle X-ray scattering and Nanoindentor, respectively. Next, the symmetric SiOCH molecular structure growth was evaluated by FTIR as shown in Fig. 3. It was observed that there was a sharp and large peak at 1108 cm-1 in only NP-SiOCH spectra. This peak was assigned as absorption of Si-O vibration of the symmetric SiOCH. Therefore, the symmetric SiOCH chain could be grown long and it contributed to improve k-value without pore in film. To fully understand the polymerization mechanism by NBECVD, we investigated a relation between excited state of DMOTMDS and Ar neutral beam energy using a collision model between Ar atom and DMOTMDS molecule by ab-initio calculation and experimental potential at an aperture plate during deposition. As results, a dynamic active energy for DMOTMDS by Ar neutral beam collision was estimated and it could explain well experimental evidence.

9054-17, Session 5

Gas cluster ion-beam etching for precision uniformity correction *(Invited Paper)*

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1. INTRODUCTION

It is self-evident that with continued dimensional scaling in advanced CMOS, the requirements for dimensional variability control are concurrently increasing. For multiple technology nodes, advanced control using variable lithographic exposure across wafer has been used to help control critical dimensions in the plane of the wafer. Until 22nm, the most critical dimensions in the vertical dimension have been well controlled by a single deposition or oxidation step, but now with RMG and FINFET, some critical dimensions such as fin height and gate height are affected by a combination of deposition, CMP and etch steps, requiring a new strategy for precision feature height control [1]. Here we will discuss the application of gas cluster ion beam technology (GCIB) [2] for precise correction of feature height nonuniformity issues, using proprietary location specific processing (LSP) algorithms [3].

2. RESULTS AND DISCUSSION

2.1 GCIB Etch characteristics

GCIB etching is inherently anisotropic, as the clusters are delivered to the wafer in a collimated beam. This characteristic is shown in Figure 1, where the bottom and top of a contact feature are etched 5nm by NF3 GCIB with no increase in CD or effect on top profile. This characteristic makes GCIB suitable for etching the bottom of contact holes, or for trimming of feature height independently from CD.

2.2 Dummy gate thickness control example

Multiple process steps can contribute to nonuniformity of the poly or a-Si dummy gate in the FINFET RMG flow, which can negatively impact process control of subsequent steps, as well as device performance and yield. A typical example of such a non-uniformity map is shown in Figure 2. After 150 Å LSP etch using the pre-GCIB input map, uniformity has been improved by >5x, with range reduced from 113 Å to 22 Å, and standard deviation reduced from 30 Å to 4.5 Å. We can define a correction efficiency metric as the reduction in range as a fraction of the mean etch, we find GCIB corrected the range by a factor of 61% of the etch target in this example.

3. SUMMARY

We have shown here that GCIB etching using LSP uniformity correction technology is capable of solving emerging challenges related to meeting integrated uniformity requirements of advanced CMOS devices. Here we have discussed the anisotropic characteristics of GCIB etch and shown an example of the LSP etch technique applied to 14nm dummy gate height control, demonstrating capability for >5x reduction in nonuniformity. In this talk further examples of LSP capability will be described, including characterizing the dynamic range possible with minimum etch target, sampling considerations for generating LSP input maps, and directions for advanced control to further improve corrective etch capability.

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9054-18, Session 5

Highly selective etching for next-generation device using time-modulation plasma

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New 3D transistor architecture called “FinFET” has introduced at 22nm node technology and beyond. Regarding FinFET gate etching, Fin is exposed in forming the gate. The fin may receive plasma damage until completing to form the gate. Therefore, FinFET gate etch needs much high selectivity to material on fin top, such as SiO2. In addition, at 3D corner, around cross-point of the fin line and the gate line, the etching residue is likely to remain on forming gate. Extended over etch is necessary to remove the residue with high selectivity etching to the fin top material.

Low ion energy condition provides high selectivity. However, it decreases etch stop margin with the pattern which has high aspect ratio. High ion energy extends the etch stop margin while decreases the selectivity. It is necessary to improve the trade-off between the selectivity and profile controllability. Moreover, proximity of profile between dense and isolated pattern should be minimized at the same time. The line at isolated pattern tends to be tapered profile owing to by-product deposition. The by-product control is a challenge to minimize the proximity.

Electron cyclotron resonance (ECR) plasma source have been widely used for semiconductor etching. The ECR plasma realizes low pressure operation which can minimize influence of by-product and provide long mean free path to make the profile vertical. Time-Modulation (TM) bias is also one candidate to control by-product effect. [1] The radio frequency (RF) bias applied to wafer is pulse modulated by TM bias. The RF bias plays a role of accelerating ions towards the surface of a wafer. The by-product is pumped out during OFF time of the RF bias.

Regarding FinFET manufacturing, required specification for etching has more difficulties with being aspect ratio of patterns higher. Therefore, additional technology is necessitated to obtain further high selectivity.

Dissociation control must be effective to improve the trade-off between the profile controllability and the selectivity. Excess dissociation provides deposition species and/or excess etchant. Low dissociation and plasma density operating window must be opened to acquire extra high selectivity and precise profile controllability in addition to conventional window.

Time-modulated microwave ECR plasma has been studied to control plasma density and dissociation. It has been reported that time-modulated microwave generates lower electron temperature.

In this study, we investigated etching performance of time-modulated microwave ECR plasma.

Selectivity to SiO2 is investigated for Poly-Si gate. It is found that higher selectivity to SiO2 is provided by the time-modulated ECR plasma, compared with conventional continuous wave (CW) plasma. Deposition on the gate SiO2 is analyzed by X-ray photoelectron spectroscopy (XPS).

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9054-19, Session 5

Advanced plasma sources for the future 450mm etch process

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As wafer and glass size have been continuously increased since last decade, large area plasma sources have been required in semiconductor and display processing.

Recently, the main subjects in developing a new plasma source have been the uniformity in large area, the plasma parameter control for the process optimization, and the development of new application area.

Multi-plasma sources and multi-electrode plasma sources have been suggested to overcome the plasma uniformity problem and the potential difference between the plasma and the processing surface. Also, in the case of large area plasma processing, the standing wave and skin effect have been critical problems as the applied RF frequencies have increased.

In this talk, some characteristics of large area plasma sources will be introduced with the brief review of the experimental and the simulation results, showing the required conditions.

Multi-RF feeding and multi-electrode concepts are to be suggested to enhance the plasma uniformity at high frequency and large-area plasma processing. Multi-ICP and multi Helicon sources also will be introduced for the large area processing, and the related plasma parameter control knobs will be explained. Some characteristics of large area hollow cathode discharge will be discussed. Also, the plasma heating mechanism will be discussed along with the recent experimental and theoretical results, focusing on the electron energy distribution function (EEDF), the plasma impedance, and the plasma potentials of each condition. In addition, some examples are to be presented for the control of plasma parameters through adjusting the RF frequency and power, operating pressure, gas mixing ratio [2], and other external parameters in order to optimize the process. The CST microwave studio is used to simulate the plasma profile, and compare with the experiment. A 2D probe arrays using floating harmonic method is used to monitor plasma parameters. Some asymmetry factors, affecting plasma uniformity, are summarized.

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9054-20, Session 6

Self-aligned double-patterning plasma etch challenges *(Invited Paper)*

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Pitch scaling deep into the sub micron range has driven the required linewidth resolution beyond the current available source radiation. Limited availability of next generation source radiation has been addressed by innovation in the pattern transfer processes with existing 193nm immersion equipment. A key innovation used to extend the imaging capabilities of available source radiation has been multi-patterning techniques.

Introduced to logic devices as a technique for pitch splitting of the imaging radiation and orthogonal cut for feature edge placement, multipatterning techniques have since been deployed to substantially reduce the half-pitch of minimum features on the devices. Self-aligned double patterning (SADP) has become a leading candidate process to define sub minimum groundrule trenches. Technology scaling has resulted in rapid proliferation in the number of critical levels being defined by multi-patterning techniques such as SIT.

SADP places substantial burden on the plasma processes used to define the minimum feature size. In this paper we will provide an overview of key challenges introduced with sidewall image transfer plasma processing, and a comparison of these challenges to competitive techniques including litho etch litho etch (LELE) and directed self-assembly (DSA) is made. Discussed are technical challenges such as uniform pitch definition and low and high frequency line edge roughness as well as manufacturability concerns including wafer processing cost, defectivity, and cross wafer uniformity. A comparison of state of the art plasma based pattern transfer technologies is made in light of these challenges.

9054-21, Session 6

A comparison of the pattern transfer of line-space patterns from graphoepitaxial and chemoepitaxial block co-polymer directed self-assembly *(Invited Paper)*

Dan B. Millward, Gurpreet Lugani, Ranjan Khuran, Scott L. Light, Micron Technology, Inc. (United States); Ardavan Niroomand, Micron Technology, Inc. (Belgium); Philip D. Hustad, Peter Trefonas, Shih-Wei Chang, Dow Electronic Materials (United States); Christopher N. Lee, The Dow Chemical Co. (United States); Dung Quach, Dow Electronic Materials (United States)

Block co-polymer directed self-assembly (BCP DSA) has become an area of fervent process development activity in the last few years as a potential alternative or adjunct to EUV lithography or self-aligned pitch multiplication strategies. This presentation will discuss progress in the evaluation of two DSA strategies for patterning line-space arrays at 30nm pitch: graphoepitaxial DSA with surface-parallel cylinder BCPs and chemoepitaxial DSA with surface-normal lamellar BCPs. An evaluation of pattern transfer into hard-mask and substrate films will be made by consideration of line and space CDs, line profile of cross-sectional SEM images, and comparison of relative LWR between the flows. The processes will be benchmarked against Micron's process used in manufacturing it's commercially available 16nm NAND part.

9054-22, Session 6

Fabrication of large arrays of sub-10nm features for bit-patterned media *(Invited Paper)*

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Bit patterned media (BPM) offers a path to higher density magnetic recording. It relies on successful fabrication of large arrays of single-domain islands with single-digit dimensions in a high volume, cost effective manner. A viable patterning approach considered by many for fabricating BPM disks is nanoimprint lithography, which requires templates with the same sized features needed on the final disks.

Feature sizes and densities on BPM templates with areal densities above 1Tdot/in2 are well ahead of those on the semiconductor roadmap, and therefore the fabrication processes depart significantly from conventional lithography. In addition, large arrays of such high density features must cover the entire area of a disk (65 or 95 mm diameter) on continuous circular tracks with no band stitches. A comparative advantage for BPM pattern generation is its fairly loose defect tolerance that could accept defect densities several orders of magnitude higher than those found in semiconductor applications.

Our template fabrication strategy has undergone two major transitions: (1) hole-tone to pillar tone and (2) hexagonal close-packed (HCP) to high bit-aspect-ratio (BAR). The transition to pillar tone templates, while requiring a tone reversal for subsequent pattern transfer, addresses the issues related to the flow capability, mechanical stability and etch resistance of nanoimprint resists. High BAR islands, which have smaller bit pitch than that of HCP islands of the same areal density, are preferred by the current head and servo technologies of disk drives.

To generate the large arrays of sub-10nm features in circular tracks on a high BAR template, we independently fabricate circumferential lines (rings) and radial lines (spokes), and cut one set of lines using the other set as a mask. To achieve this, we employ a combination of rotary-stage e-beam lithography, directed self-assembly block copolymer (BCP), self-aligned double patterning (SADP) (for half-pitches ~10 nm or less that are not well served by current mature BCP systems), nanoimprint lithography, and cross-line patterning (line cutting). Other new techniques, such as block-selective infiltration synthesis are used in the fabrication sequence.

We have successfully demonstrated fabrication of BPM templates with nanoimprintable arrays of high BAR features with ~7nm half pitch for areal densities 1.6 Td/in2 and above.

9054-23, Session 6

Directed self-assembly of PS-b-PDMS into 193nm photoresist patterns and transfer into silicon by plasma etching

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Block CoPolymer (BCP) self-assembly creates periodical patterns with features sizes eventually below 10 nm. On plain substrates, ordering is only obtained in grains not larger than a few micrometers but self-assembly in trenches of a pattern (so-called graphoepitaxy) can create long-range order between the polymer micro-domains. As a result, such directed self-assembly (DSA) approaches may be used in some ultra-high resolution patterning processes in the microelectronics industry.

Due to its ease of processing, a large majority of the lithographic BCP work reported so far concerned PS-b-PMMA. Researchers show now increased attention to BCP with a high Flory-Huggins (?) parameter (high incompatibility between the two blocks) owing to their improved resolution (possibility of sub-10 nm features) and natural tendency to create highly ordered patterns. Among those, PS-b-PDMS is particularly attractive due to the high plasma etch resistance of the PDMS block compared to the PS one.

In the present study, we report on graphoepitaxy and etching experiments made with cylindrical PS-b-PDMS within standard industrial-like photolithography stacks. Used templates, fabricated on 300 mm diameter silicon wafers, are composed of three layers: Spin-On-Carbon (SOC), Silicon-containing Anti-Reflective Coating (SiARC) and 193 nm photolithography resist. About 60 nm deep trenches are first made by plasma etching in the SiARC/SOC stack using the 193 nm photolithography resist mask (Fig. 1 of Additional Supplemental File). These trenches are then used to confine the BCP and guide the self-assembly of horizontal PDMS cylinders. Wetting conditions allows to avoid the interfacial PDMS wetting layer at the bottom and lateral interfaces after the solvent annealing step.

Finally, dedicated pulsed plasma etching conditions were developed in order to reveal the BCP patterns, transfer them into the remaining SOC layer under the trenches and finally transfer them unto the underlying silicon substrate (Fig. 2 and 3 of Additional Supplemental File). 15 nm half-pitch dense line/space features are formed with a height up to 105 nm and an excellent critical dimension control during each etching step.

In conclusion, long-range order line/space features could be produced by using horizontal cylindrical high-? BCPs combined with industry-type photolithography stacks.

9054-24, Session PTues

Litho resist rework influences on Cu metal layer patterning with TiN-hard mask

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The use of TiN-Hardmasks for Cu metal layer patterning has become a common technique for trench first metal hardmask (TFMH) integration schemes.

Resist rework influences the chemical and physical behavior of the TiN hardmask and therefore the final result of the dual damascene etch process in terms of critical dimension (CD) and trench taper determining the electrical metal sheet resistance.

Within this paper, the effects of three different litho rework strip procedures on subsequent TiN hardmask and dual damascene etching, using O2, H2N2 and H2O plasma processes, are compared. Furthermore, the interaction of the rework process with the CD tuning capabilities in dual damascene etch are evaluated. Summarizing the data, a stable process flow for wafers with and without litho rework is shown, eliminating litho CD rework offsets, resulting in metal trench processing with tight geometrical and electrical distributions.

9054-25, Session PTues

Spin on carbon using fullerene derivatives

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Progress in lithographic resolution has made the adoption of extremely thin photoresist films necessary for the fabrication of '2x nm' structures to prevent issues such as resist collapse during development. While there are resists with high etch durability [1], ultimately etch depth is limited by resist thickness. A possible solution is the use of a multilayer etch stack. This allows for a considerable increase in aspect ratio. For organic hardmasks a carbon-rich material is preferred as carbon possesses a high etch resistance in silicon etch plasma processes. A thin silicon topcoat deposited on the carbon film can then be patterned with a thin photoresist film without feature collapse, and the pattern transferred to the underlying carbon film by etching. This produces high aspect ratio carbon structures suitable for substrate etching. In terms of manufacturability it is beneficial to spin coat the carbon layer instead of using chemical vapor deposition [2], but the presence of carbon-hydrogen bonds in typical spin on carbon leads to line wiggling during the etch. We have previously introduced a fullerene based 'spin on carbon' (SoC) with high etch durability and reported on material characterization [3, 4]. Here we show recent advances in material development and work towards commercialization. The low hydrogen level in the material allows for high resolution etching without wiggling.

Hard mask solutions were prepared by dissolving the fullerene derivative in cyclohexanone and adding crosslinker at a ratio of 1:1 by weight. With a 50g/L solution 4-inch silicon wafers were covered with a homogenous carbon film with few defects at a thickness of 115 nm. Spin coating conditions were 1000 rpm for 60s. After spinning the carbon layer is baked on a hotplate to crosslink the film. To improve the etch resistance of the material, fluorene epoxy instead of the previous novolac was tested as crosslinker. As the fluorene has a lower Ohnishi number, superior etch performance is expected. The fluorene could successfully crosslink the carbon film although a slight higher bake temperature was necessary. Development of a low cost variant of the fullerene material is also underway and has given an additional enhancement in etch durability.

For use in an etch stack, a 20 nm silicon film was sputtered on top of the carbon. Resist patterns were written on the silicon topcoat by e-beam lithography and transferred to the silicon thin film using SF6/CHF3 ICP. The carbon layer was then etched by O2 plasma through the silicon mask and finally the pattern was transferred into the silicon substrate by the same process as the topcoat. Figure 3 shows an example of silicon etched with the 20 nm linewidth carbon mask using the SF6/CHF3 ICP. Figure 4 shows the same material after an SF6/C4F8 etch process for the same pattern and process time.

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9054-27, Session PTues

Dual-frequency mid-gap capacitively coupled plasma (CCP) for conventional and DSA patterning at 10nm node and beyond

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Patterning at 1x nm and sub-1x nm technology node is one of the key challenges for the semiconductor industry. Several patterning techniques are under investigation to enable the required 15nm and less minimum half-pitches for MPU/ASIC 10 nm technology node and beyond. The most viable techniques among them which are compatible for high volume production are: extensions of the conventional optical lithography techniques such as quadruple/octuplet patterning with 193nm immersion lithography; double patterning with Extreme UV lithography (EUVL); and the non-conventional techniques such as Directed Self-Assembly (DSA). Regardless of the technique, selective dry etching is forming a crucial part of the work flow in the patterning process. Consequently the characteristics of the dry etching process play an increasingly important role in defining the outcome of the patterning process.

In this paper, we will demonstrate the unique advantage of the dual-frequency mid-gap capacitively coupled plasma (CCP) in the advanced node patterning process with regard to etch rate / depth uniformity and critical dimension (CD) control in conjunction with wider process window for aspect ratio dependent & micro-loading effects. Unlike the non-planar plasma sources, the simple design of the mid-gap CCPs enables both metal and non-metal hard-mask based patterning, which provides essential flexibility for conventional and DSA patterning. We will present data on the conventional multi patterning as well as data on DSA patterning for trenches / fins and holes. Rigorous CD control and CDU would be shown to be crucial for multi patterning as they lead to undesirable odd-even delta and pitch walking. For DSA patterning, co-optimized Ne / Vdc of the dual frequency CCPs would be demonstrated to be advantageous for higher organic-to-organic selectivity during co-polymer etching. In addition we will demonstrate the application of a high negative DC voltage as an effective control knob for improving edge roughness and width roughness for the etched patterns both in conventional and DSA patterning.