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PHOTOMASK TECHNOLOGY GROUP

EMLC 2023 in Dresden with Record Attendance

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EDITORIAL

EMLC 2023 in Dresden with record attendance

Reinhard Galler, *EQUIcon Software GmbH*

After an absence of four years, the European Mask and Lithography Conference (EMLC) took place once again in Dresden in June this year. In its 38th edition, the conference was able to set a new attendance record with nearly 200 participants. After a forced break due to the pandemic and a very successful return to last year's face-to-face event in Leuven (Belgium), the participants were again offered a packed program from Monday afternoon to Wednesday evening with 38 oral presentations (including five keynotes and 11 invited presentations), 12 posters, and two tutorials.

To set the mood, the very first keynote talk by Giacomo Indiveri (ETH Zürich) showed alternatives for one of the major and often neglected problems of modern computer use—the excessive energy consumption of some "killer" applications. While Bitcoin miners recently outpaced the energy consumption of small nations, it is now estimated that artificial intelligence applications (language models, image generators such as ChatGPT, Dall E, etc.) will need to consume about 20 percent of global energy generation in just a few years if development continues as it is. A possible alternative could be "Neuromorphic Intelligence", i.e., a completely different computer architecture, which is oriented towards the functioning of biological brains and promises to achieve comparable performance with energy consumption reduced by a factor of 100 to 1,000. A promising component for the realization of such units is the so-called memristor. The interested reader will find sufficient further articles on this topic. For the entire process chain, this promises to be an exciting challenge about how such components can be optimally integrated into the semiconductor production process.

Further keynotes by Joe English (Intel), Christian Koitzsch (Bosch) and Dominik Thron (Infineon) about the new semiconductor fabs in Leixlip, Ireland (Intel), in Dresden (Bosch, Infineon) and in the future in Magdeburg (Intel) gave a fascinating insight not only into how the semiconductor industry in Europe will develop further under the influence of supply chain issues and new funding programs, but also into the tremendous financial and organizational challenge to build a modern semiconductor fab and to operate with profit.

The largest part of the presentations was dedicated to the current developments in mask and lithography technologies, with the greatest challenges being found in the further development of EUV lithography (extreme ultraviolet, wavelength 13.5 nm). While currently commercially available high-end electronics are manufactured in 7 nm or 4 nm processes, the roadmaps for semiconductor technologies suggest that in the next few years technology nodes

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EDITORIAL

will be called, for example, A20 or A14, corresponding to 2 nm and 1.4 nm, respectively! To be able to image such structures, the current EUV technology has to be further developed significantly in all aspects. In the case of exposure devices, the main role is currently played by a certain property of the optical system, the numerical aperture. In available devices, this value is 0.33—but to be able to image structures of an A20 or A14 process, a numerical aperture of 0.55 or greater is needed.

This means, above all, that the individual components of the optical system must become larger without sacrificing accuracy. The elements of the optical system are exclusively mirrors with aspherical surfaces and then in sizes of up to one meter in diameter. Here, the actual surface must not deviate from the ideal surface shape by more than about 20 pm on average—precision that is beyond normal comprehension. Several presentations by Zeiss and ASML showed the huge effort required to manufacture and test such an optical system or the entire exposure device.

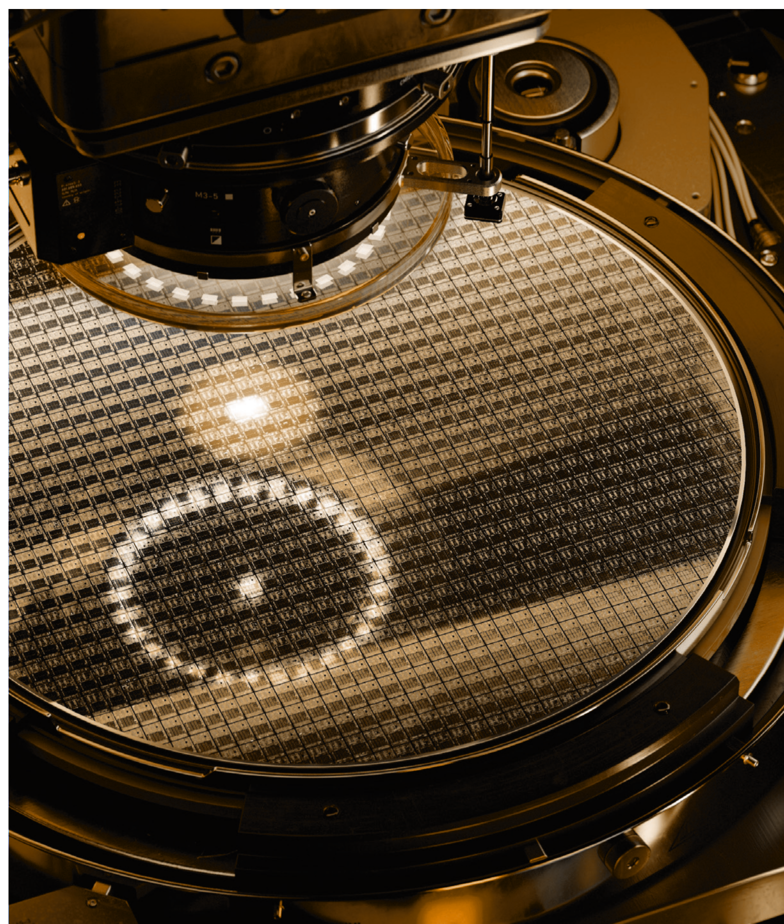
A separate session was dedicated to electron beam lithography, primarily needed for the production of masks including EUV masks. For high-end masks, multibeam mask writers from IMS Nanofabrication Vienna have been established for several years, later NuFlare Technology has also appeared as a supplier. In electron multibeam devices, mask structures are written simultaneously with a large number of partial beams (currently about 250,000). As a major advantage, the mask write time becomes independent of the size and number of micro- and nanometer structures, and a typical high-end mask can be written in about 10–12 hours or less. However, each partial beam writes a single pixel of fixed size, so in principle no structures smaller than those of pixel size can be created.

Several presentations indicated that the trend toward chips with ever larger areas and more transistors and functions (Systems on Chip, SOC) could come to an end and even reverse. Two factors in particular could be responsible for this. As structure sizes continue to shrink, the likelihood of defects increases and that reduces yields. If the chips remain smaller, on the other hand, the yield improves. A second factor is the future introduction of high-NA exposure devices (numerical aperture >= 0.55) and the anamorphic optics they require. This reduces the available area on the mask by half. If the usable area is too small for one (large) chip, the chip has to be split on two masks, which would be gladly avoided because of higher mask costs and new stitching problems. Of course, the smaller chips must then be reassembled into larger functional units using the so-called interposers. Suitable technologies for this are based, for example, on nano-imprint lithography.

A separate session for student contributions started last year, was also continued with great success. For the best contribution (oral presentation plus poster design), Carl Zeiss AG offered the Zeiss Award for Talents in Photomask Industry. This year the award went to Sean D'Silva from Fraunhofer IISB in Erlangen for his contribution "Predicting resist pattern collapse in EUVL using machine learning."

Overall, EMLC 2023 was again a very interesting conference that provided all attendees with an up-to-date cross-section of the status and perspectives in the lithography environment.

The 39th edition of the EMLC will be held in Grenoble from 17–19 June 2024.



FEATURED ARTICLE

Benefits of SEM field-of-view contour averaging for contour-based MPC modeling

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ABSTRACT

Building accurate models for Mask Process Correction (MPC) is indispensable for manufacturing masks for advanced wafer production nodes. In recent years, contour-based model calibration is being increasingly studied as a supplement to standard gauge-based modeling. In this paper, we demonstrate a data processing flow for contour calibration of MPC models to overcome the issue of noisy input contours by averaging the measured contours of repeating patterns within the SEM image field-of-view (FOV). This method not only averages out the statistical noise in the incoming FOV contours, but also allows us to make the model calibration process more efficient.

INTRODUCTION

MPC has become an integral part of the mask manufacturing processes for advanced semiconductor manufacturing nodes of 14 nm and beyond and is critical to the realization of the tight CD uniformity and CD linearity control required by those nodes[1]. Any model-based correction can only be as accurate as the model, and as such calibrating an MPC model of the desired accuracy is a pre-requisite for successful deployment of MPC in production. MPC models are typically calibrated using CD-SEM (Critical Dimension Scanning Electron Microscopy) measurements of test-patterns printed on a test mask. **Figure 1.a** shows the typical MPC model calibration flow followed in practice. In the initial phase, a comprehensive model calibration test-chip is prepared which includes test-structures that cover the range of CDs and complexity of shapes that the target mask process must be able to print within the specified error budget. Since the metrology tool times allocated for model calibration are often very limited, only a selected number of shapes (gauges) are chosen for measurement. The test-chip and the down-selected gauge file are then sent to the mask-shop for printing and metrology. After complete processing of the test-chip, metrology is performed on the selected gauges and measurements are collected. The gauge measurements are then statistically analyzed to identify and eliminate unresolved and anomalous measurements, and averaging is applied to prepare the data for model calibration. Model calibration is then performed using an optimization method of choice, where the optimizer tries to minimize the given objective functions of the model for all input gauge locations. An MPC model typically consists of e-beam and etch components to model the e-beam exposure effects and etch effects respectively, and post-etch CD-SEM measurements are used to calibrate both the components. While this has worked well for older production nodes up to 14nm, the CD uniformity and CD linearity requirements for advanced nodes of 7nm and beyond have pushed the accuracy requirements of MPC models so far that the number of CD-measurements needed to achieve the required accuracy may be much larger than a typical mask-shop can afford to allocate for model calibration.

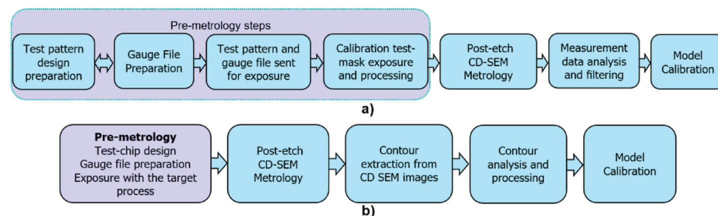

Figure 1: *MPC model calibration flows, a) CD measurement-based calibration flow; b) Contour-based calibration flow.*

In recent years, contour-based model calibration is being increasingly studied in the semiconductor manufacturing industry as a supplement to standard gauge-based modeling[2-5]. In contour calibration, the contours extracted from SEM images, instead of the CD-SEM measurements, are used as input to model calibration engine. **Figure 1.b** shows how the MPC model calibration using contour-based calibration is different from CD-measurement based calibration. Test-chip design is as important and subject to the same considerations as it is for gauge-based calibration. In the metrology phase SEM images of the gauge locations are collected possibly along with the CD measurements. In the next phase, contours are extracted from the SEM images and analyzed for their suitability for contour calibration.

In contour calibration, several model evaluation sites are placed along the measured contour in a selected region of the SEM field-of-view (FOV). The optimizer tries to minimize the overall model prediction root mean square (RMS) error over all sites on all the contours. Figure 2 shows examples of site placements for an I-shape test-structure. The simplest strategy is to place sites at uniform intervals along the measurement contours in a selected region of each input SEM image field-of-view (**Figure 2.b**), however this can result in many redundant sites which add to the computation time of each calibration run. A more efficient site placement strategy can reduce the number of sites, for example by making the site placement curvature dependent, such that parts of the contour with higher curvature get larger number of sites and vice-versa (**Figure 2.c**). As in the case with CD measurement-based calibration, the model calibrated with contour-based calibration is only as accurate as the quality of input contours. Contours extracted from SEM images are beset with noise inherent in lithography and metrology processes[2], and such contours with low signal-to-noise ratio (SNR) are unsuitable for building an acceptable MPC model as the model optimizer can get confounded by the large amount of noise and may not converge to a good model. Furthermore, it is also difficult to validate the calibrated model without having good quality contours. Contour quality can be improved by averaging contours obtained from several SEM images, but that adds to the metrology budget and may not always be feasible. Another key challenge for using contour-based model calibration is making effective use of the larger amount of information available in SEM contours compared to gauge CD measurements. One way to do this is include contours from the full field-of-view of the SEM image in calibration. Apart from the additional noise the optimizer must deal with, this also explodes the number of sites making model calibration runtimes impractical.

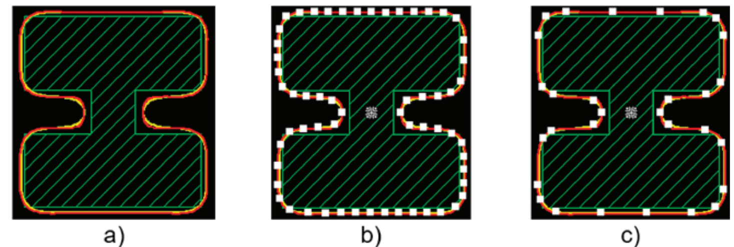

Figure 2: *Site placement for contour calibration; a) Input measured contour in yellow and simulated contours in red; b) Uniform site placement; c) Curvature based site placement.*

In this paper, we demonstrate a data processing flow to overcome the issue of noisy contours by averaging the measured contours of repeating patterns within the SEM image FOV on the calibration mask. This method not only averages out the statistical noise in the incoming FOV contours, but also allows us to make the model calibration process more efficient by using only the averaged contour to represent the patterns within a given FOV on the calibration mask. Using a simulated experiment, we demonstrate this flow on a set of 326 pattern conditions on a conventional MPC modeling test-chip. A physics-based SEM simulator, which can introduce a programmed statistical distribution of pixel noise, is used to simulate synthetic SEM images of the test chip. Two sets of simulated SEM images are generated, one with low noise levels and the second with high noise levels, and contours are extracted from both sets of images. The low noise SEM image contours serve as reference contours and the high-noise contours are used for demonstrating the averaging flow. We then calibrate two models using the high-noise contours, the first model is calibrated on the unprocessed raw contours and the second model is calibrated on the FOV averaged contours. By comparing the predictions of these two models with respect to the reference contours, the paper will establish the value of the FOV contour averaging method as a practical way to efficiently calibrate reliable mask models from noisy SEM images, specifically in cases where multiple SEM images per location are not available.

EXPERIMENTAL DETAILS

Figure 3 shows the overview of the experiment designed to demonstrate the effectiveness within FOV contour averaging for MPC model calibration. A set of 326 conventional MPC calibration test-structures consisting of lines, contacts, stretched-contacts, I-shapes and ellipses were chosen for this study. A testchip consisting of these structures and a gauge file having the location of each of them in the test-chip were prepared and input to the physics-based SEM simulator. Two sets of simulated SEM images for all the test-structures were generated: first one with low noise to serve as the ideal or reference SEM images, and the second one with higher noise. Contours are then extracted from both sets of images. The low noise contours are used as reference contours to assess the quality of models later in the experiment. The contours from noisy images are used for model calibration and two models are calibrated using these contours. The first model is calibrated using the raw contours without any processing, and the second model is calibrated using processed contours obtained by applying FOV averaging and alignment on the raw contours.

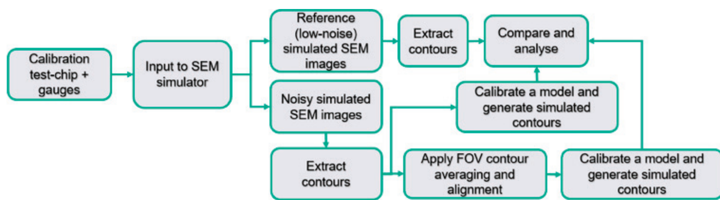

Figure 3: *Design of the experiment to demonstrate the benefits of FOV contour averaging.*

A physics-based SEM image simulator developed internally is used to generate the simulated SEM images for this experiment. This simulator first simulates the physical effects that contribute to the SNR of images captured by a SEM tool for the shapes at the input gauge locations using the parameters provided by the user. These simulated effects are then combined linearly to generate the simulated SEM image. For our experiment, the low noise images were generated by keeping the values of linear combination coefficients for the simulated noise effects relatively small. For generating the high noise images, the linear combination coefficients were tuned iteratively by comparing real CD-SEM images from a reference data set with simulated images for a small set of test-structures. After generating the SEM images, Calibre SEMSuite tool is used to extract the contours from both sets of images. First the contour extraction parameters are optimized manually using the SEMSuite graphical user interface (GUI) using a small set of simulated SEM images. The optimized parameters are then written into a configuration file which is used to extract contours from both the reference SEM images and the noisy SEM images in batch mode. **Figure 4** shows an example of reference and noisy SEM images and the contours obtained from each for an I-shape test structure. The reference SEM image has much better contrast and yields a much higher quality contour compared to the noisy SEM image.

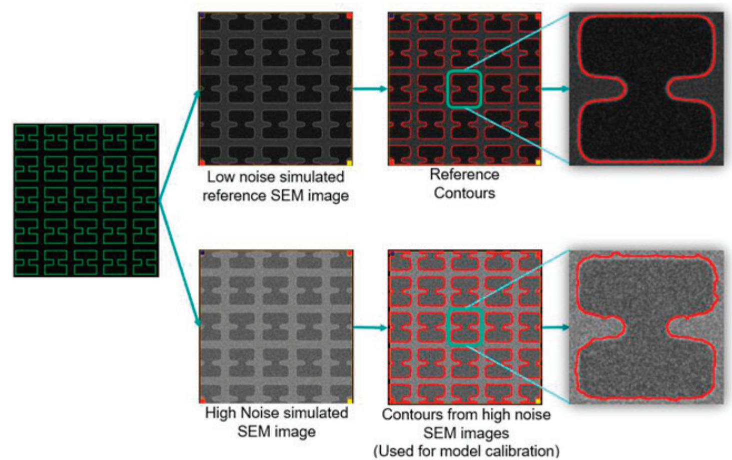

Figure 4: *Example of low noise (reference) and high noise simulated SEM images and contour extraction on an I-shape test-structure.*

Figure 5.a shows the steps of the process of averaging contours within SEM FOV. FOV contour averaging requires three main inputs: the calibration test-chip layout file, the extracted contour files (in OASIS format), and the gauge file in which the SEM image paths have been configured for each gauge. First, the spatial location of valid complete contours in each FOV is determined using the information available in the gauge file. Next, these valid contours are shifted to the central gauge location to overlay all the valid contours together. Averaging is then applied to the overlaid contours and the averaged contour is aligned with the target design to correct for any systematic misalignment between the target design and extracted contours. **Figure 5.b** shows an example of FOV contour averaging performed on contours extracted for a contact test-structure.

FEATURED ARTICLE

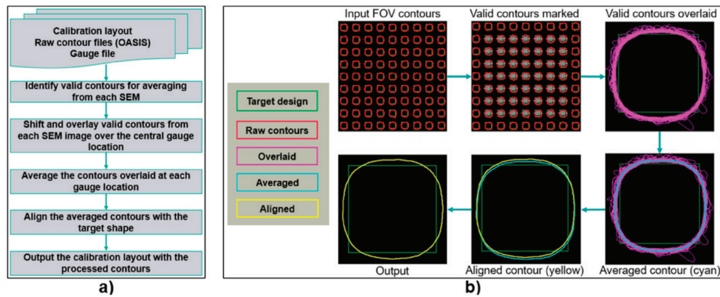

Figure 5: a) FOV contour averaging process; b) Example of FOV contour averaging on a contact test-structure.

Two models are calibrated using the noisy contours. The first model is calibrated using the raw contours which haven't been processed in any way. The second model is calibrated with the contours obtained after applying FOV averaging on the raw contours. Same model-forms and other calibration settings were used for calibrating both the models. The optimizer was run for sufficient iterations to allow it to converge to the optimum model in both cases. Also, the site placement region in both calibrations was the same. In the rest of the paper, the model calibrated with raw contours will be referred to as **Model A** and the second model calibrated with FOV averaged contours will be referred to as **Model B**.

RESULTS AND ANALYSIS

Figure 6.a shows the model calibration RMS calculated for all sites on all the input contours. Model A has a calibration RMS error of 2.64 nm and model B has an RMS of 0.793. Although the lower RMS of Model B is primarily due to the improved SNR due to averaging, it does indicate better convergence of the calibration engine to the optimum model within the constrained search space. The model convergence statistics of both the models further confirm this. For Model A, 29.4% of all sites had model error in ±1 nm range and 52.8% had it in the range of ±2 nm, while for the model B these figures are 90.1% and 99.4%.

For model validation we assess the model prediction quality with respect to the reference contours obtained from simulated SEM images with low noise. **Figure 6.b** shows the model prediction RMS error of the two models with respect to the reference contours. The simulation RMS of model A against the reference contour is 1.19 and that of Model B is 0.633, thus showing the model with FOV averaged contours has much better prediction compared to the model calibrated with raw contours.

Model B also has better coverage statistics on the reference contours with ±1 nm and ±2 nm coverage at 88.4% and 99.7% of all sites compared to those of Model A which are 53.5% and 92%.

Figure 6: a) Model calibration RMS errors of Models A and B; b) Model prediction RMS errors with respect to the reference contours for Models A and B.

Contour overlays are used for qualitative assessment of model prediction. Generally, simulated contours from the model are overlaid with the SEM images, however in this case we have overlaid the simulated contours of the two models with the reference contours extracted from the low noise images. **Figure 7** shows the simulated contours obtained from Model A and B (shown in blue and red respectively) overlaid with the reference contour (shown

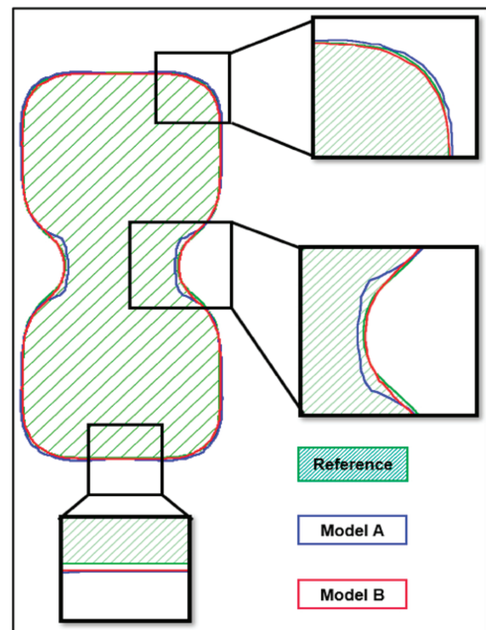

Figure 7: Simulated contours of Model A and Model B for an I-shape test-structure overlaid with the reference contour.

in shaded green) for an I-shape test-structure. As the zoomed-in cutout at the bottom shows, both the models are in quite good agreement and very close to the reference contour on longer straight segments. However, at both convex and concave corners the simulated contour of Model B is in much better agreement with the reference contour (refence contour is not clearly visible in the middle and top cutouts as the simulated contour is on the top of it) compared to the simulated contour of Model A. Contour overlays done with reference contours and the simulated contours of the two models on other test-structures used in this study show a similar picture.

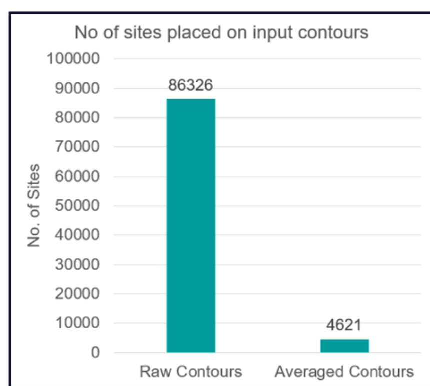

Figure 8: *No of sites placed on unprocessed and FOV averaged contours for the 326 test-structures selected for the study.*

It is also interesting to compare the number of sites that would be evaluated when unprocessed contours in a fixed region of the FOV are used for placing the model evaluation sites against the number of sites on the FOV averaged contour. Since model calibration runtime is directly proportional to the number of sites that are evaluated when contour calibration is used, it is enough to compare those numbers to draw reasonable inferences on the calibration runtimes also. **Figure 8** shows the results of such an experiment in which site placement was tried on both the raw contours and FOV averaged contours with the same site placement settings except for the site placement region of each FOV in the two runs. Sites were placed on contours in the 1x1 µm central region in the FOV of the unprocessed contours. For averaged contours, sites were placed on the entire averaged contour. The number of sites on the unprocessed contours with such a placement is 18.6 times larger than that of the FOV averaged contours. The calibration runtimes when using the unprocessed contours could thus be prohibitive.

SUMMARY & CONCLUSION

This paper proposes averaging of within field-of-view contours of repeating structures to obtain high quality contours for contour calibration purposes. The proposed method averages repeating contours obtained from the same SEM image and doesn't require multiple images of the same structure for contour averaging. Results show that MPC model calibrated on contours obtained using FOV contour averaging has better calibration RMS error and better prediction with respect to the reference contours than the model calibrated on unprocessed contours. Using FOV averaged contours in calibration also reduces the number of sites evaluated dramatically compared to using unprocessed contours with a fixed site placement region which also means reduced model calibration runtimes with FOV averaged contours. FOV averaging of contours is highly recommended where contour data from conventional gauge-based SEM images is readily available and contour calibration is essential to achieve the required model quality.

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INDUSTRY BRIEFS

SoftBank's Arm IPO attracts Apple, Nvidia, Intel, and Samsung as strategic investors

SoftBank Group Corp. has secured some of Arm Ltd.'s prominent customers, including Apple Inc., Nvidia Corp., Intel Corp., and Samsung Electronics Co., as strategic investors for Arm's initial public offering (IPO), according to sources familiar with the matter. In addition to these companies, other investors in the IPO include Advanced Micro Devices Inc., Cadence Design Systems Inc., Alphabet Inc.'s Google, Synopsys Inc., and more, said the sources who requested anonymity because the details have not been announced yet. These investors will contribute amounts ranging from $25 million to $100 million.

gameishard.gg/news/softbank-lines-up-apple-and-nvidia-as-strategic-arm-ipo-backers-2/78644/

The most advanced chips in the world: Apple to buy TSMC's entire supply of 3nm chips for 2023

The collaboration between Apple and TSMC continues to grow stronger. According to recent reports, the two companies have signed a major agreement for 3nm chips that will be used in both the A17 Bionic, which will power the upcoming iPhone 15 Pro models, and the M3 processors that will be the heart of the next generation of MacBooks. Apple has already purchased a large portion of the 3nm chips that will be produced in 2023. Some sources say this purchase was based on 90%. Now, this figure has reached 100%.

gizmochina.com/2023/09/01/apple-tsmc-3nm-chip-deal/

Intel 14th gen "Meteor Lake" 4nm node allegedly on par with TSMC's 3nm process

Intel's first EUV node is set to debut later this year with its 14th Gen Meteor Lake processors. Previously known as its 7nm node, the Intel 4 process was renamed to more appropriately highlight its performance against rival TSMC and Samsung offerings. Unlike its predecessor, it will primarily be used for the Meteor Lake Client family and select ASICs. Putting aside speculations of a delay, Intel has assured investors that its 4nm (Intel 4) node is on track for mass production later this year. William Grimm, VP and Director of Intel's Logic Technology and Development Product Engineering explained that with EUV, it is possible to control the complexity of the process, allowing for higher yields than previously expected. The Intel 4 process is the first node from the chipmaker to leverage EUV lithography. TSMC adopted the same with its 7nm class nodes several years back. IC Knowledge, a firm specializing in reverse engineering, has analyzed the performance data of the Intel 4 node, concluding that it is superior to TSMC's 5nm node and more in line with its upcoming 3nm process. The former allegedly has a transistor density higher than TSMC and Samsung's 3nm processes.

hardwaretimes.com/intel-14th-gen-meteor-lake-4nm-node-allegedly-on-par-with-tsmcs-3nm-process/

IBM unveils energy-efficient analog AI chip prototype

IBM has revealed a prototype analog AI chip that has the potential to revolutionize the field of artificial intelligence (AI) development. The chip is said to be up to 14 times more energy efficient than current industry-leading components, addressing one of the major challenges in generative AI: high power consumption.

gameishard.gg/news/nvidia-beware-ibm-has-a-new-analog-ai-chip-that-could-give-the-h100-a-run-for-its-money/53062/

AI accelerators increasing demand for HBM chips and creating new competition

The demand for AI products is rising globally in 2023, leading to an increased demand for AI accelerator chips like Nvidia's and in-house chips developed by tech companies. This is good news for memory chip manufacturers like SK Hynix, Samsung, and Micron, who have struggled due to oversupply and the pandemic. High Bandwidth Memory (HBM) is vital for AI accelerator chips, making tasks faster. As new products with advanced HBM3 and HBM3e chips are expected next year, manufacturers like SK Hynix, Samsung, and Micron are set to benefit.

Semiconductor News | August 2023 | Sourcengine

TSMC installs first EUV machine in U.S.; job opening ads posted

TSMC has installed its first EUV machine in its new fab in Phoenix, Arizona. TSMC hailed the EUV machine milestone, but said thousands more pieces of equipment needed to be installed in the new Arizona fab, and companies supplying factory equipment and services to the complex were seeking about 2,000 skilled workers.

focustaiwan.tw/business/202308190009

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2023

SPIE Photomask Technology + EUV Lithography
1–5 October 2023
Monterey, California, USA
spie.org/puv

2024

SPIE Advanced Lithography + Patterning
25–29 February 2024
San Jose, California, USA
spie.org/al

Photomask Japan
16–18 April 2024
Yokohama, Japan
smartconf.jp

You are invited to submit events of interest for this calendar. Please send to tyb@spie.org.

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Photomask Technology + EUV Lithography 2023

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