PHOTOMASK

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Creating nonideality: Enabling cross-platform process matching solutions with MPC (and a lot of hard work)

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ABSTRACT

The bulk of photomask demand is in technology nodes ≥65nm, using equipment, processes, and materials developed more than two decades ago[1]. Despite mature processes and tools, mask makers are challenged to meet continuing demand. The challenge comes not only in the forms of increased demand, but also that much of the equipment is approaching the end of its viable lifetime to support and maintain due to parts or expertise availability[2]. Mask writers in particular are problematic from a technical and financial perspective.

Modern equipment and processes can be "too good" to simply use as a direct substitute when original equipment or processes become unavailable during initial lithography and device integration, device manufacturers tailored Optical Proximity Correction (OPC) and other wafer processing conditions based on the original mask signature for multiple mask layers. Changing to state-of-the-art mask fidelity would actually represent a liability, as the altered mask character could result in device shifts, yield reduction, or even unanticipated reliability failures.

Table 1. Connecting Mask Writer Characteristics to OPC.

Layer	Mask Characteristic	Compensating OPC
Isolation	1D (through-pitch, linearity)	RBOPC: Selective Linewidth Biasing (SLB)
	2D (Corner rounding, foreshortening, complex shape replication)	Serifs, small-shape sizing, line-end flares/extensions, Hand-OPC'd SRAM
Gate	1D	SLB, thick-ox device compensation
	2D	Serifs, small-shape sizing, line-end flares/extensions, Hand-OPC'd SRAM
Metallization	2D	Line-end flares/extensions

SPIE.

Editorial

A summer like never before

Vidya Vaenkatesan, ASML Netherlands BV

Or should I say, a summer like long before? – Where summers would mean never-ending days of fun playing with children in your neighborhood, visiting local attractions, eating locally grown produce. Where in those endless days of fun, one just existed in the moment with little thought of what lies beyond. In a gradual change, with globalization and the availability of affordable long-distance transport, we saw a change in our expectation of an ideal holiday – it just became a default for so many of us to go to distant shores to disconnect and have a summer of our lifelong dreams.

But somehow, the summer of 2020 has halted us on our tracks – it feels like we have traveled back to simpler times. It is a summer where we have had to look closer to home for recreation instead of hopping on a plane and going halfway across the world to see that perfect sunset, surf that perfect wave. COVID-19 seems to have veered us off our tracks. Given what is at stake, home seems a better and safer choice compared to distant lands. In its simplicity, it is reminiscent of summers of yesteryears.

However, this nostalgia does not mask the reality of us all facing the twin threats of COVID-19 to both lives and livelihood. It has created and continues to cause insurmountable losses in terms of both health and economic woes.

Looking at the semiconductor industry that we are part of – like other industries, we will probably suffer the repercussions because the outbreak slows or suspends production among electronics manufacturers. There is the risk of workers getting infected, thereby preventing them from being onsite. While some sectors and roles can sustain operations working remotely, others will require a significant workforce onsite.

The new reality of remote working can spur growth in wired communication since continued distant work and homeschooling will stimulate demand for them. Additionally, the situation might positively impact investment, growth, and adoption of 5G, collaboration, cloud, automation technologies, artificial intelligence, and the internet of things. Just as all major economic disruptors came out of unique circumstances, COVID-19, too, has no precedent. Thus, it is difficult to estimate what the real impact of this pandemic will be on our industry.

I have no doubt that collectively, we will find a way to survive this economic situation and will be a testament to our resilience. The whole situation has shown us viable alternatives to working onsite, communicating, commuting. At an individual level, if this adversity prods us to rethink some aspects of our behavior – be it being mindful of the environment, excessive consumerism, the importance of community and relationship, and understanding that there are alternatives to the way we have been doing things so far, we would have learned something and come out wiser from of this situation.

For the rest, summers will come and go – each one bringing unique memories. But let us mark this summer as a moment of change for the better. I wish you and everyone around you safe times and good health through this period!
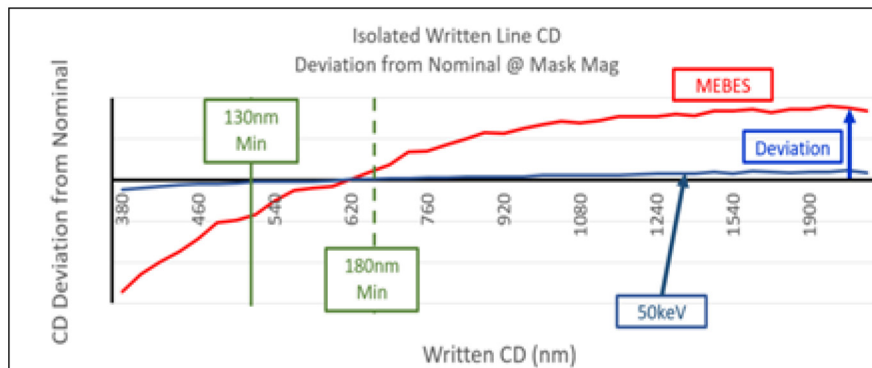
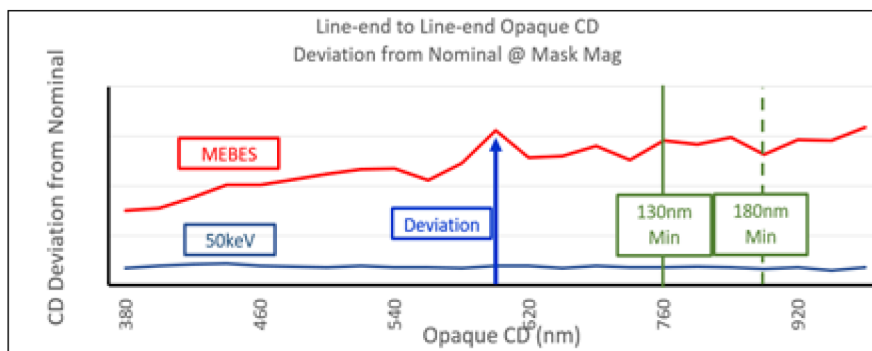Figure 1. Clear Line Linearity Differences: MEBES vs 50keV.

Figure 2. Opaque Line-end Foreshortening: MEBES vs 50keV.

To account for the improved fidelity, re-optimization of the synergistic patterning between mask, wafer lithography and etch is required. Even on mature technologies, reintegration can require costly, difficult, and time-consuming requalification. While this path has often been pursued when manufacturers declare EOL of tools, we propose instead to contain the change in the mask shop by using Mask Process Corrections (MPC)[3]. Instead of using MPC to maximize mask fidelity, as is done in advanced nodes, we use MPC to replicate the original mask non-idealities on a new mask process.

1. Background and Challenges

1.1 Background

There is considerable effort and attention devoted to developing leading-edge technology ecosystems (EUV) and advanced nodes (7nm and beyond), but a significant demand remains for mature technologies, including 65-130nm-node. Production in these nodes continues to be served by an aging mask-writer fleet, using both early-generation laser systems and first-generation e-beam writers. While 180nm-node technologies were first introduced in the late 1990's, and 130nm-node a few years later, the proliferation of derivative technologies based on the initial offerings has been locked into the same, initial mask lithography integration strategy.

Because of the maturity of these nodes, customers expect both low mask costs and rapid turnaround time (TAT) on mask production—often about 3 days from mask order submission to initial mask delivery. In addition, customers expect the fabricator to deliver product which has the same electrical behavior as historic base performance, with the additional functionality or features added in the new derivative.

Delivering this stable electrical functionality signal over multiple decades has typically locked mask manufacturers into keeping the base technologies and derivatives on the same mask writing platform. The writer's non-ideality defines a mask character which is transferred to wafer device structures.

While mask writers have always had non-idealities, early rules-based OPC (RBOPC) were implemented in 180nm-node, with more extensive and sophisticated RBOPC deployed with 130nm node. (Table 1). This recognized both that the writer non-idealities were significant relative to design groundrules, and further cemented the linkage between mask writer platform and fabricator processing. RBOPC was applied to specific lithographic levels to account for the non-idealities, so any change in mask writer would require an RBOPC update and fabricator requalification.

1.2 Challenge of running mask writers near obsolescence

With such strong incentives to maintain legacy mask-writing platforms in production, increasing resources and innovation are required to sustain this equipment, which is often greater than 20 years old. For example, electronic components are obsolete, making replacements scarce. Additionally, ensuring maintenance expertise is increasingly difficult. Therefore it is imperative to develop a sustainable strategy for ensuring continued production.

1.3 Illustrative Case: MEBES 10keV mask writers

The MEBES 10keV raster scan platform is one specific example of a mask writing toolset approaching EOL. With few remaining in commercial production, parts, servicing, and expertise issues are becoming critical. There are multiple options available to sunset these tools that can be considered.

1.3.1 MEBES elimination, option 1: Convert to more capable 1st-generation 50keV platform

One obvious solution would be to migrate production up onto a first-generation 50keV writer. At first, this appears to be quite attractive: These 50keV writers offer an approximate 80% reduction in CD 3-sigma (CDU), 70% reduction in CD mean-to-target (MTT), and a 60% reduction in residual registration.

This reduction in random variation would be desirable, but a detailed characterization of the systematic errors demonstrates the risk of this ap-
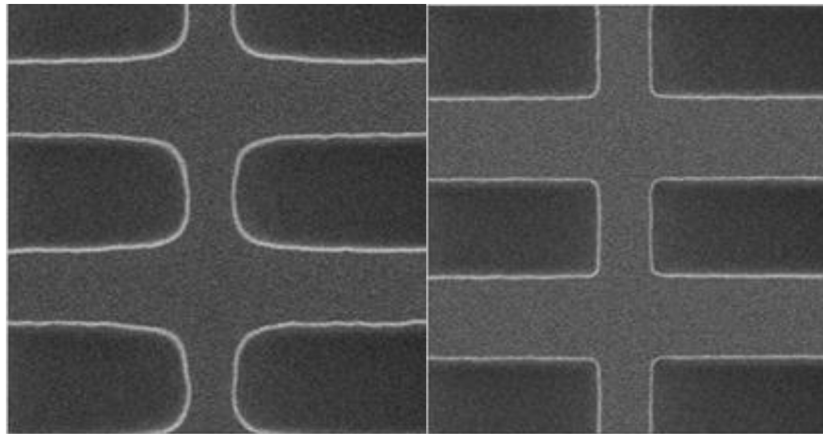
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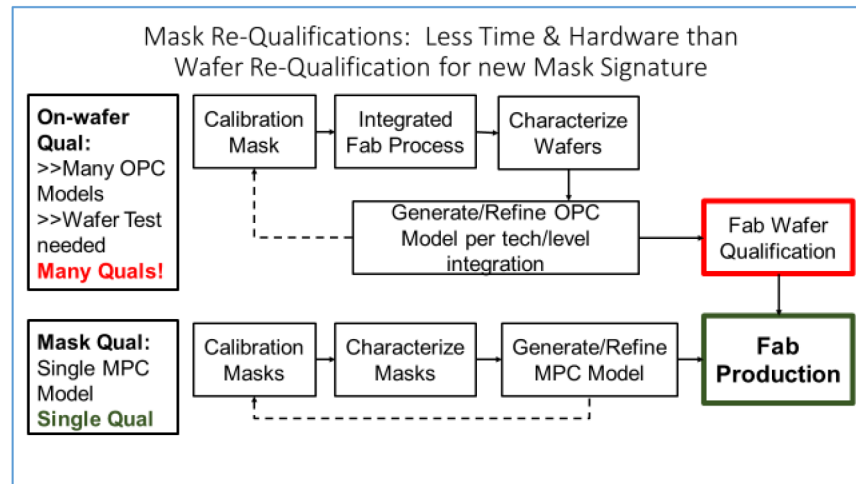*Figure 3. Corner rounding difference, MEBES (left) vs. 50keV.*

Figure 4. Proposed approach compresses multiple OPC qualifications into a single MPC keyword.

proach. The legacy MEBES writers have significant imaging non-idealities, measurable both in 1-dimensional (1D) CD and 2-dimensional (2D) fore-shortening (Figure 1, Figure 2), and in other properties, such as corner rounding (Figure 3). Depending on the application, such a change could result in device parametric shifts, yield degrade, or even reliability failure.

1.3.2 MEBES elimination, option 2: 50keV with new OPC

Since the improved fidelity associated with conversion to an improved character 50keV write platform represents significant technical risk, another choice would be to couple a mask integration change with an OPC update. This would involve significant resources in the wafer fab for each layer and technology combination to develop, evaluate, and qualify. The aggregate resources and time to deploy all-new OPC keywords would be impractical.

1.3.3 MEBES elimination, option 3: 50keV write with MPC to emulate MEBES character

Using 50keV with MPC combines the benefits of 50keV writer capability, retains the important character associated with the original MEBES writer, but avoids the delay of OPC deployments. It also confines resources and risk to the mask shop. Instead of multiple OPC deployments, only a single MPC solution is required. Finally, MPC refinement feedback loops could be completed in weeks rather than quarters (Figure 4).

Unlike MPC application on advanced nodes, where the MPC model's goal is to replicate the design data, this application seeks to replicate the non-ideality of the MEBES writer. This requires two models: The first, to describe the nonideal behavior of the MEBES writer; and the second, to model the 50keV writer. Design data would be input to the MEBES model, whose output is used as the target for the 50keV writer's model.

2. Characterizing Non-Ideality for MPC

Based on the advantages cited in Section 0, the 50keV with MPC option was chosen. This required design of a calibration vehicle for CDSEM metrology of 1D and 2D effects. Additional methods were required to insure complex shape replication by the model.

2.1 Calibration/Characterization vehicle design

Mask Process Correction model generation relies primarily on critical dimension (CD) data from 1D and 2D test structures. For 1D structures, both clear lines and chrome lines through varying linearity and pitch-space were used. For 2D structures, foreshortening CD was measured on both clear and chrome line-ends. The aggregate sample size was 5,025 sites/mask to achieve sufficient parameter space sampling.

Initial clear and opaque image CD minimum design sizes were calculated based on design limits for impacted masks (Figure 5). However, because RBOPC adds structures to minimum features (Table 1), written mask dimensions often contain sub-ground rule images. CDSEM sampling was extended to include image sizes smaller than indicated by the initial nominal model parameter space (Figure 6).
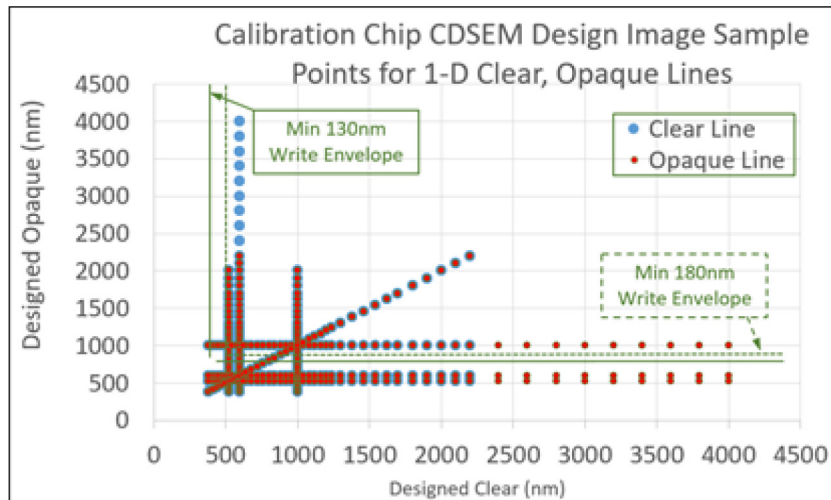
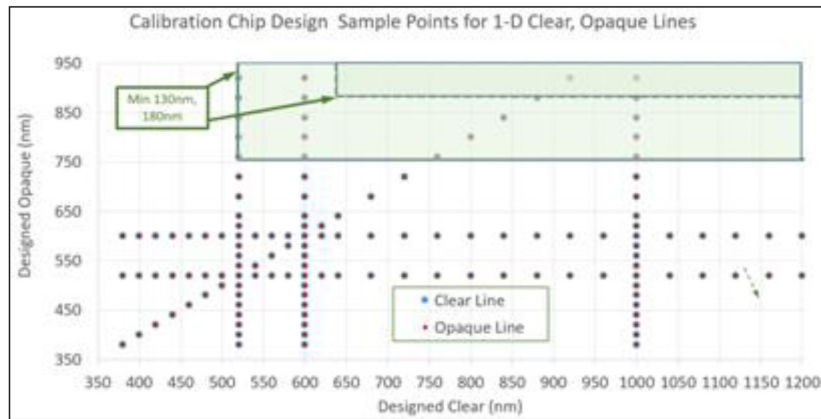*Figure 5. Calibration chip sampling parameter space, opaque and clear lines.*

Figure 6. Sub-ground rule portion of calibration chip sampling parameter space.

2.2 CDSEM Metrology Challenges

Given the significant corner rounding and imaging variation of the 2D structures, measurements of clear and opaque line-end foreshortening remained problematic. Seemingly subtle measurement gate size, algorithm, and placement changes, as seen in Figure 7, could change measured foreshortening CD on the same image by 15nm or more.

2.3 CDSEM contour calibration on complex 2D shapes

Digitized CDSEM screen captures of specific image types (inside/outside corners; line-ends; complex shapes) were used to augment the CD measurements of the calibration chip. This data improved internal parameters related to beam size, develop, and etch, making the model more accurate than CD data only.

3. Modeling and Correction Approach

3.1 Sampling

When defining mask sample plans, it was important to consider the capability and sources of variability. Multiple sample masks were measured to quantify fixed variation (tool-to-tool), as well as process variation (etch time, develop temperature). These results were aggregated to form a single "average mask", as well as to more accurately define the typical variation.

3.2 Modular MPC flow

The correction recipe consists of three major steps: MEBES contour simulation, corner fragmentation, and 50keV correction (Figure 8).

The first step simulates the mask contour of the input mask data using the calibrated MEBES model. The final 50keV tool MPC step uses this contour as its target.

Before applying the final correction, one needs to make sure MPC has enough freedom to move edges around corners and complicated 2D shapes. Therefore, additional fragmentation of edges around corners is applied such that corner rounding can be matched accurately (see Section 3.3 for details).

The final step of the flow adjusts the fragmented input data using the 50keV mask model as a correction model and the simulated MEBES contour as its target.

This flow ensures MEBES and 50keV tool and process effects are accounted for appropriately. With this modular approach, should it be necessary to manufacture using a different mask writer, only the 50keV mask model would need to be replaced. The flow described would compensate for the signature of the new mask writer/process, while the rest of the flow would remain constant.

3.3 Corner fragmentation for matching 2D shapes

Corner fragmentation of the incoming mask is critical to achieving accurate 2D shape replication. MEBES mask corner rounding requires substantial fragmentation to result in accurate replication on 50keV e-
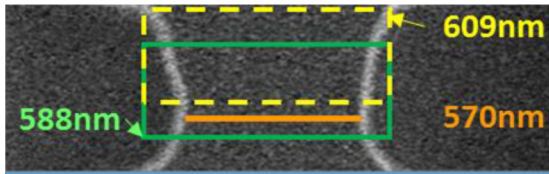
Figure 7. CDSEM metrology sensitivity to gate and algorithm. Solid Box: 50% line algorithm, center; Dashed Box: 50% line algorithm, offset; Line: Minimum distance algorithm.
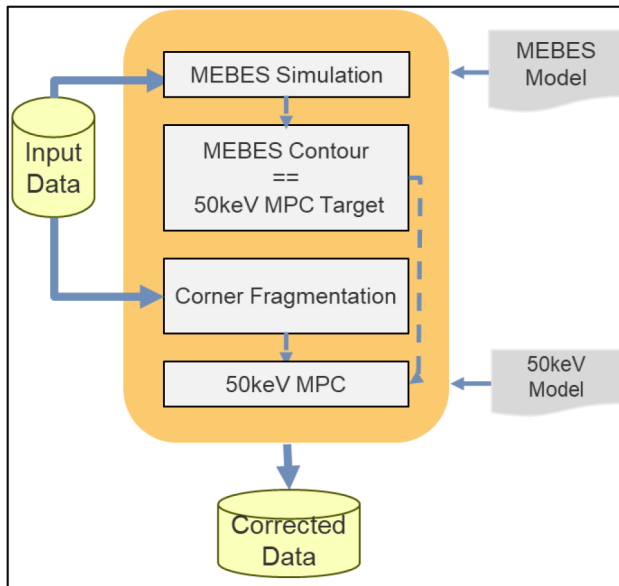

Figure 8. Tool matching MPC flow for matching a MEBES mask signature using a 50keV mask writer. By keeping the flow modular, one can easily migrate to other new mask writers by simply updating the 50keV mask model.

beam writers (Figure 3).

While smaller fragments allow for more accurate corner matching, they increase write time on the 50keV mask writer. Figure 9 shows a possible fragmentation near a convex corner where fragments increase in length away from the corner.

4. Results

4.1 Model Verification

As described above, two models are required: one for the MEBES writer and another for the 50keV writer[4].

4.1.1 Individual model verification: Model to CDSEM data

Writer models for both MEBES and 50keV platforms were compared to CDSEM data for all sampled image types. The residual model error was acceptable both for nominal and deep sub-groundrule images (Figure 10).

4.1.2 Model to CDSEM contour comparison

MPC success is typically assessed with quantitative metrics, such as linearity, or even 2D line-end-shortening. Due to the significant, unique 2D nonideality of the MEBES process, additional scrutiny needed to be applied to characterizing and reproducing the 2D characteristics. MEBES and JEOL model overlays to respective CDSEM contours (Figure 11) demonstrate the success of model corner rounding replication.
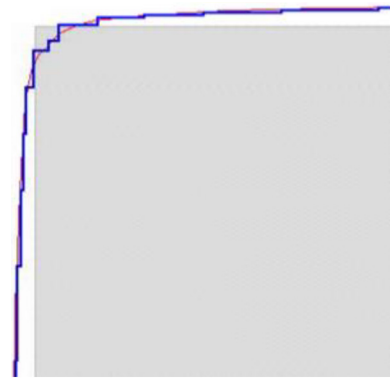

Figure 9. MPC fragmentation around convex corner. Grey: input mask shape; Continuous curve: simulated MEBES contour; Staircasing: fragmented edges after correction. Note: the input mask shape and simulated contour differ due to a large MEBES process bias.

4.2 MPC solution verification

4.2.1 On-mask CDSEM verification, 50keV with MPC, calibration chip

To verify the fidelity of the MPC solution, the calibration chip designs used for the model generation were printed with a 50keV writer. Six verification masks with MPC corrections were written on the 50keV platform, sampling two writers and two developers to capture integration variability. The same CDSEM site sampling was used for verification as for model generation.

The objective was for model deviation to be within the normal MEBES variability. This MEBES variability envelope was estimated based on the individual MEBES mask sample. Individual model deviations for all six 50keV masks with MPC were within the typical variability of the MEBES modelling population for all 1D and 2D parameters, as shown in Figure 12, Figure 13, and Figure 14.

4.2.2 On-mask CDSEM and AIMS verification, 50keV with MPC, functional 180nm logic

A section of a functional 180nm logic metallization level was measured using both CDSEM and AIMS. AIMS is typically used for defect and repair characterization, but it can also be a key metrology option for mask process development to supplement the standard CD measurements. Mask 2D and 3D effects can affect wafer print results, and can be non-linear across different feature sizes and feature types.

Sample sites were chosen to characterize significantly asymmetric environments, for example line-ends near contact lands, or lines with differing distances to nearest neighbors (Figure 15). Significant deviations from ideality were observed on the MEBES masks, by both AIMS (Figure 16) and CDSEM (Figure 18). Qualitatively, both AIMS and CDSEM observe the same trends, and the difference data from both AIMS (Figure 17) and CDSEM (Figure 19) indicate 50keV MPC to MEBES CD differences are less than typical MEBES variability.

4.2.3 On-mask CDSEM comparison: MEBES vs 50keV with MPC on complex shapes

As shown in Figure 20, the corner rounding was successfully replicated, by appropriate fragmentation application.

4.3 Production mask results

Both 50keV MPC and MEBES masks of 130nm- and 180nm-node designs, encompassing isolation, gate, metallization, and bipolar emitter layers, were shipped to the fabricator customer. As expected, mask CD 3-sigma and residual registration were both significantly superior on the 50keV platform. (Figure 21, Figure 22).
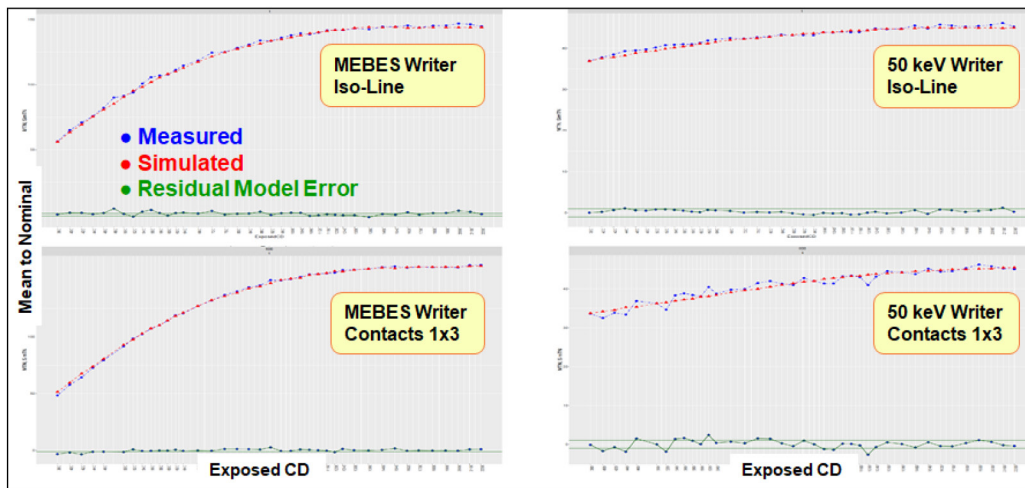
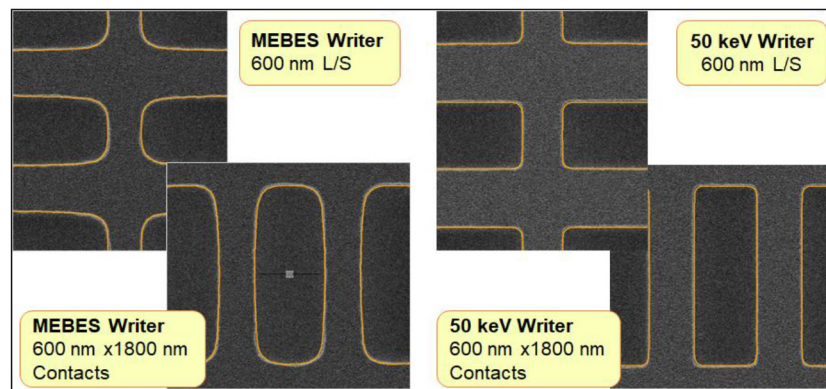*Figure 10. Model to raw data for MEBES and 50keV writers, two different image types.*

Figure 11. Model overlays to CDSEM contours.

4.4 On-wafer lithography verification

Wafer lithographic evaluations were performed to ensure interchangeability of MEBES and 50keV MPC masks. Both 1D (linearity and through pitch) and 2D (line end shortening) structures were measured. Additionally, non-MPC'd 50keV masks were provided for comparison.

As seen in Figure 23 and Figure 24, the evaluation demonstrated MEBES/50keV MPC interchangeability[5]. As predicted by modeling data, the 50keV without MPC was measurably different from MEBES.

4.5 Production cycle time impact

Overall mask processing time, including Mask Data Preparation (MDP) must be preserved to minimize disruption to mask delivery schedules or factory throughput. While adding MPC into MDP adds significant complexity, this can be mitigated through both increased parallelization and optimization of MPC by balancing complexity and accuracy with runtime. Additionally, performing Mask Process Verification (MPCv) in parallel can reduce cycle time without impacting quality.

Figure 25 displays the cumulative MDP and write times observed on several patterns written both with 50keV MPC and MEBES. 50keV write times were shorter than MEBES, but the additional MPC runtime yielded slightly longer overall processing times for the 50keV flow. More work is needed to continue to optimize MDP, MPCv, and processing time.

5. Conclusion

There is continued strong demand for masks in ≥65nm nodes. Writers originally used to manufacture these masks are approaching EOL, but possess significant, systematic non-idealities that cannot be changed without risk of device line parametric shifts, yield, or reliability failure. To migrate from one mask writer platform to another, a solution is proposed using a model from the first write platform to act as a target for MPC for the second mask writer.

The MPC solution has been successfully implemented for 130nm/180nm critical levels, meeting both technical and business requirements. Due to the novel, modular, two-model approach of this MPC solution, it is extendable for any combination of mask integration changes, as long as the operating space is within the shared capability envelope of both integrations. In addition to mask writer change, it is also applicable to other process variables that affect systematic mask character, such as etch platform or imaging resist.

Use of this method extends beyond the original EOL scenario: Mask manufacturers with a diverse fleet of writer platforms could generate a model describing each mask writer/resist/etch integration. As business demands require, the MPC solution would permit a dynamic flex from one platform to the next, permitting the mask shop improved production flexibility, while continuing to deliver interchangeable masks to the fabricator customer.

6. References

[1] "eBeam Initiative Mask Maker Survey Results," 2018. [Online]. Available: https://www.ebeam.org/docs/eBeam-Mask-Maker-Survey-2018.pdf.

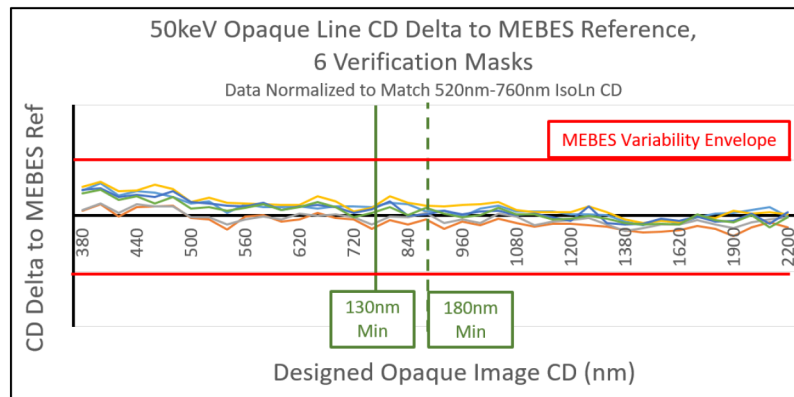[2] Kalk, F., "Renew, Retire, Replace", Toppan Photomasks, Inc.

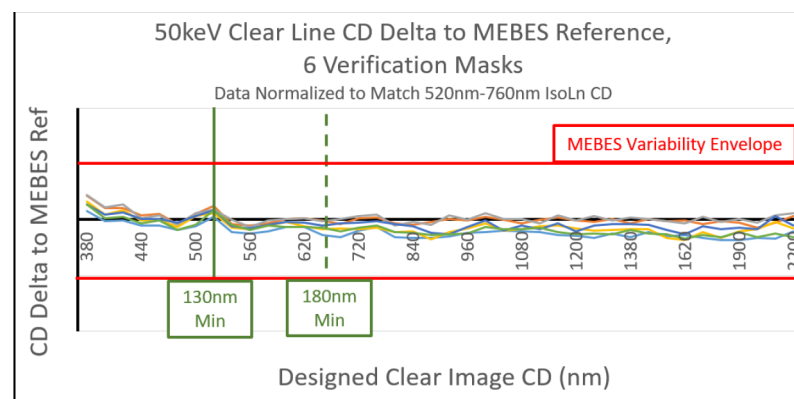*Figure 12. CDSEM verification, isolated opaque line, six masks.*

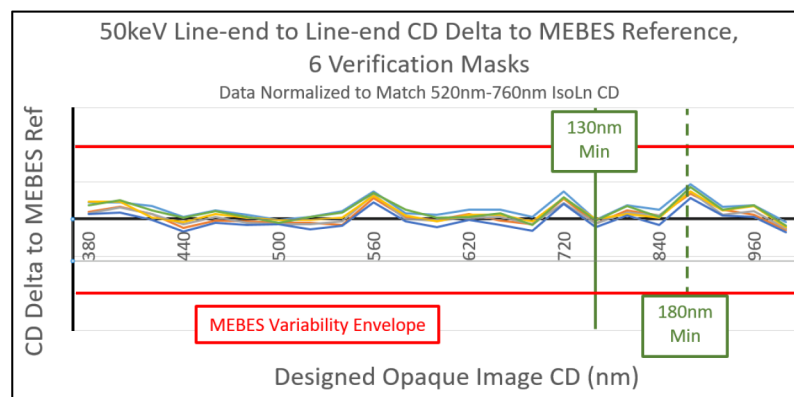*Figure 13. CDSEM verification, isolated clear line, six masks.*

Figure 14. CDSEM verification, line end to line end, six masks.

[3] Bork, I., Buck, P., Reddy, M., and Durvasula, B., "A fully model-based MPC solution including VSB shot dose assignment and shape correction," **Proc. SPIE,** vol. 9635, Photomask Technology, 96350U, (23 October, 2015).

[4] Bork, I., Buck, P., Paninjath, S., Mishra, K., Bürgel, C., Standiford, K., and Chua, G. S., "Mask model calibration for MPC applications utilizing shot dose assignment," **Proc. SPIE**, vol. 9235, 2014.

[5] Dupuis, S., Figueiredo, P., and Parrish, C., "GLOBALFOUNDRIES Internal Report," 2019.

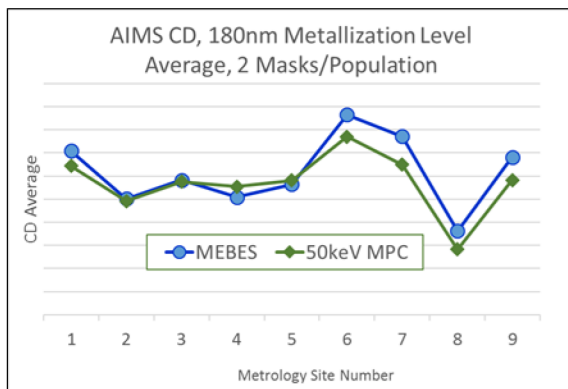Figure 15. Metallization layer logic circuitry AIMS/CD sites.

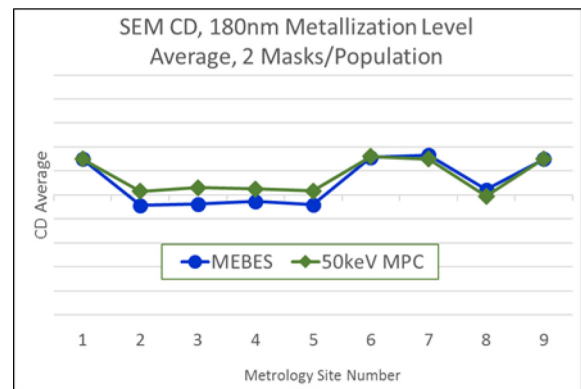Figure 16. AIMS CD, 50keV MPC vs MEBES.
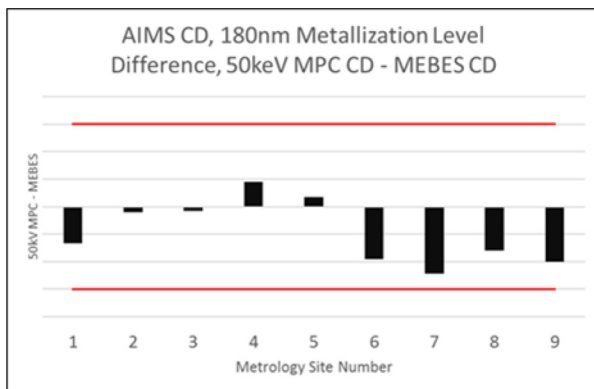

Figure 18. SEM CD, 50keV MPC vs MEBES.

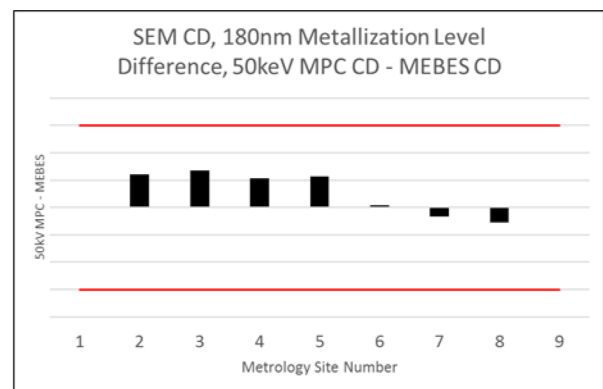Figure 17. Difference, 50keV MPC - MEBES AIMS CD.

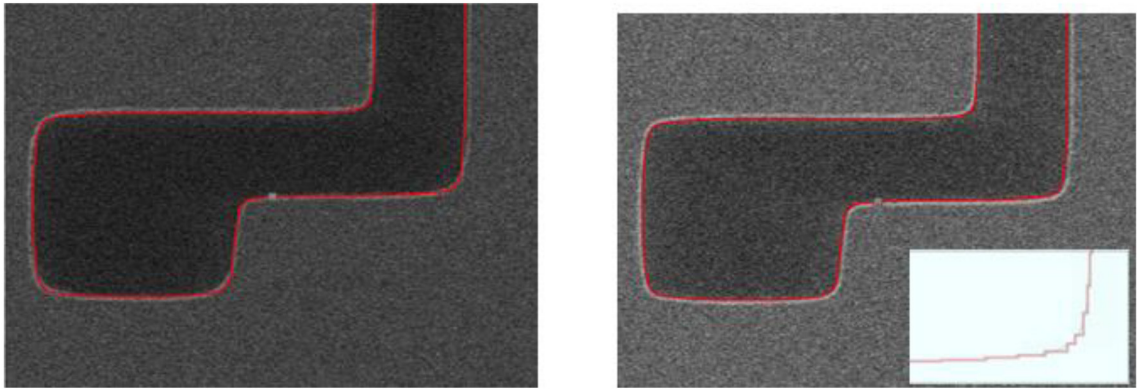

Figure 19. Difference, 50keV MPC - MEBES SEM CD.

Figure 20. Left: Mask written with MEBES. Right: Mask written with 50 keV writer. Line matching CDSEM edge is the simulated MEBES contour. The inset staircase line shows the zoomed in MPC'd output used in the 50 keV tool.
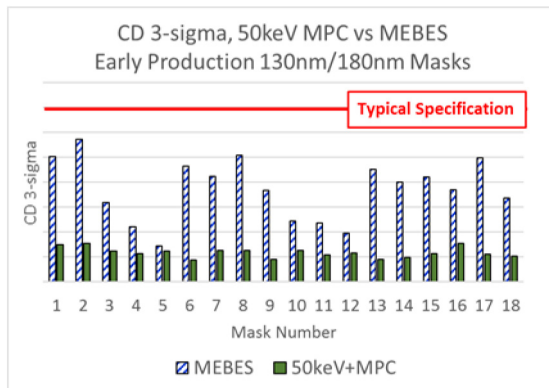

Figure 21. CD 3-sigma, early production 50keV MPC vs MEBES.
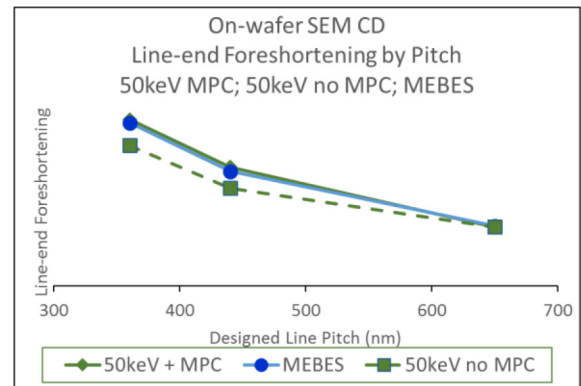

Figure 23. On-wafer CD comparison, line-end foreshortening, 50keV MPC; 50keV no MPC; MEBES.
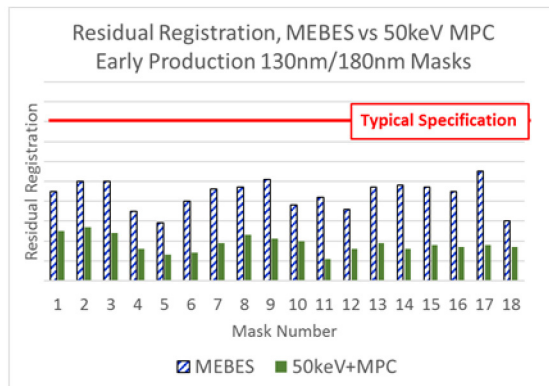

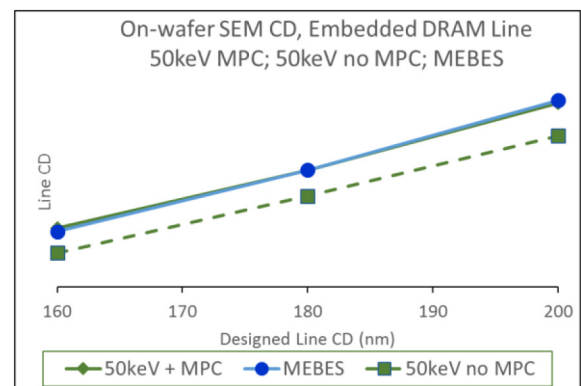*Figure 22. Residual registration, early production 50keV MPC vs MEBES.*

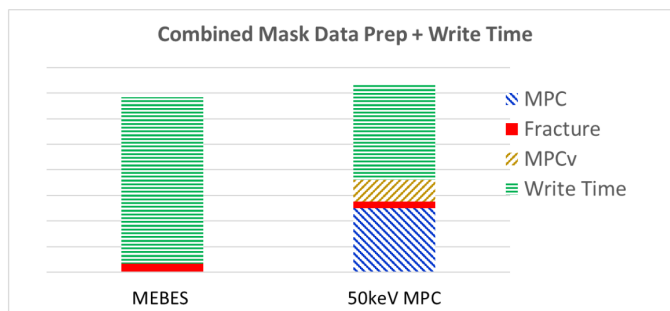*Figure 24. On-wafer CD comparison, embedded DRAM line, 50keV MPC; 50keV no MPC; MEBES.*

Figure 25. Combined MDP plus write time for MEBES and 50keV with MPC.

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Industry Briefs

■ Chip Gear is Selling Like Hotcakes

George Leopold, EET Asia

The semiconductor equipment sector is exhibiting remarkable resilience despite geopolitical concerns over an escalating U.S.-China technology cold war and a pandemic that shows no signs of abating. While monthly billings slipped in June, SEMI reported during its annual conference that June equipment bookings totaling $2.31 billion were nevertheless 14.4 percent higher than June 2019. That total kept the three-month moving average heading north throughout the first half of this year. SEMI is forecasting continuing growth through the end of this year and into next despite growing uncertainty over the pandemic and the impact of strict U.S. export controls. SEMI's equipment spending forecast released July 21 estimates China will continue outspending competitors this year and next. SEMI reckons Chinese companies will invest $17.3 billion on chip-making gear this year, perhaps building up inventory before the equipment export door is closed. According to SEMI's forecast, Chinese projected 2020 equipment spending approaches the levels recorded by South Korea in 2018 ($17.7 billion) and Taiwan in 2019 ($17.1 billion). Following a surprisingly strong 2020, with expenditures expected to hit $63.2 billion, SEMI is forecasting record annual equipment spending next year approaching $70 billion.

https://www.eetasia.com/chip-gear-is-selling-like-hotcakes/

■ Do Engineers Live Longer?

Cabe Atwell, EET Asia

It is sometimes claimed that engineers live longer. It would make a certain sense; engineering salaries are on the higher end and provide larger benefits packages while often requiring lower physical demands than other occupations. On the other hand, working in engineering can require long hours and stressful deadlines. So, do engineers tend to have longer lives? Recent studies took into account elements such as stressors most likely to cause death to have some answers for what jobs make for a longer, healthier life. Past research has shown an incredible variation in life expectancy around the United States, as much as a 33-year difference on average depending on factors such as county of residence, race, education level, and gender. Those with more education have an average longer life expectancy, as do those in the workforce, and those with higher family income. Research in applied psychology has shown that job demands affect employee health outcomes in both the short- and long-term. A 2020 study found that job control can moderate the relationship between job demands and physical and mental health — jobs with a higher degree of employee job control result in better health outcomes. When it comes to career demographics, it is important to note that these may be tied not just to the conditions of the job itself, but to the people who have access to or tend to make up that section of the workforce. However, there are aspects of the profession — job control, higher pay and benefits — that contribute to longevity. The simple answer is yes, engineers tend to have longer lives than those in many other professions, but there is always a lot more happening behind the scenes when it comes to statistics.

https://www.eetasia.com/do-engineers-live-longer/

■ EUV Mask Cleaning Process

Mark Lapedus, Manufacturing Bits, Semiconductor Engineering

TSMC has developed a new dry-clean technology for photomasks used in extreme ultraviolet (EUV) lithography that avoids the need for pellicles. "Depending on process requirements, EUV photomask is divided into two types – with pellicle and without pellicle. TSMC has chosen EUV mask without pellicle to enhance optical transmittance, thus reducing energy loss during exposure process," according to TSMC researchers James Chu, Ivence Hu and Jenna Chang. "Instead of using traditional wet clean process with ultrapure water and chemicals, fall-on particles are rapidly removed by such a dry clean technique. Meanwhile, the fall-on source is precisely located by sub-nanometer analysis technique and therefore contaminations can be excluded thoroughly. With persistent tests and optimization, the fall-on particle reduction rate achieved more than 99% in 2020," according to TSMC's researchers. "By means of fall-on analysis and contamination source elimination, the fall-on count of each 10,000 wafers decreased from hundreds of particles to single-digit particles, achieving 99% of reduction rate. Since its introduction, the amount of water saving and chemical usage saving has reached about 735 metric tons and 36 metric tons, respectively," they said. TSMC was vague in terms of how the EUV mask cleaning process works. However, TSMC filed a patent in the arena, which might provide some clues.

https://semiengineering.com/manufacturing-bits-aug-10/

Join the premier professional organization for mask makers and mask users!

About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

Individual Membership Benefits include:

- Subscription to BACUS News (monthly)
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- Subscription to BACUS News (monthly)
- One online SPIE Journal Subscription
- Listed as a Corporate Member in the BACUS Monthly Newsletter

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CALENDAR

2020

SPIE Photomask Technology + EUV Lithography
Free Digital Forum
Online Only
21-25 September 2020

2021

SPIE Advanced Lithography
21-25 February 2021
San Jose, California, USA
www.spie.org/al

Photomask Japan
26-28 April 2021
Yokohama, Kanagawa, Japan
www.photomask-japan.org

The 36th European Mask and Lithography Conference, EMLC 2021
21-23 June 2021
Leuven, Belgium

SPIE is the international society for optics and photonics, an educational not-for-profit organization founded in 1955 to advance light-based science and technology. The Society serves more than 255,000 constituents from 183 countries, offering conferences and their published proceedings, continuing education, books, journals, and the SPIE Digital Library in support of interdisciplinary information exchange, professional networking, and patent precedent. In 2019, SPIE provided more than $5 million in community support including scholarships and awards, outreach and advocacy programs, travel grants, public policy, and educational resources. **spie.org**

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You are invited to submit events of interest for this calendar. Please send to lindad@spie.org.