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Fabrication of Ta based absorber EUV mask with SRAF

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ABSTRACT

With shrinkage of device pattern, optical proximity correction (OPC) will be used for EUV lithography, which leads to need sub resolution assist features (SRAF) on EUV mask. Currently, it is difficult to fabricate EUV mask with SRAF of sub-30nm using conventional resist mask process stably. Moreover, it is necessary to improve line width roughness (LWR) of mask absorber pattern for achieving the lithographic specifications beyond hp15nm patterning.

In this paper, in order to meet the requirements of Ta based absorber EUV mask with SRAF, mask fabrication process using new structure blank is studied for sub-30nm SRAF patterning and for improved LWR of primary feature. New mask process using new blank with thinner resist and Cr based hard mask was developed. By using new mask process, resolution of absorber pattern was achieved to 30nm for SRAF patterning, and LWR was improved comparing with conventional process.

1. Introduction

EUV lithography is one of the promising candidates for next generation lithography and pattern shrinkage is expected to reach beyond hp15nm with single exposure. OPC or inverse lithography technology (ILT) will be used for EUV lithography of 0.33NA extension. Moreover, capability of SRAF to improve process latitudes of EUV lithography is reported.[1] Therefor EUV mask with SRAF of sub-30nm are needed, and EUV mask with high resolution and low LWR is required.[2] We defined EUV mask targets for 0.33NA EUV lithography beyond hp15nm patterning.

- Mask minimum primary feature size (printable limitation of 0.33NA EUV lithography): 44nm

- LWR of primary feature: 2.8nm or less

- Minimum SRAF size: 30nm line / 24nm space

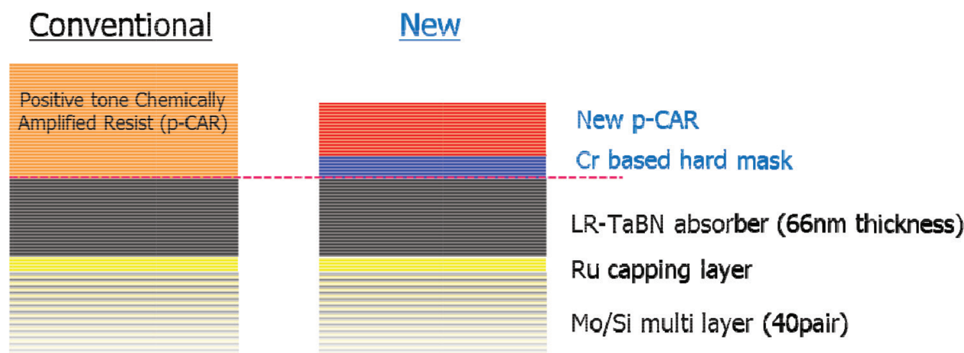

Figure 1. Structure of mask blank for EUV lithography.

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Editorial

Deep Learning is Going to Improve Mask Manufacturing Too

By **Aki Fujimura,** CEO, D2S, Inc.

Looking forward to another great BACUS program! After the keynote, the annual eBeam Initiative survey results will be presented. Following that is the Deep Learning and Data Analytics session where the discussion will center on the state-of-the-art in applying deep learning to mask manufacturing.

There's so much being said today about artificial intelligence (AI), machine learning (ML), and deep learning (DL) that it may be hard to tell what's real, and what's hype. There's certainly hype (and hope) around DL, but underneath it all, there is something very real. Having started in EDA (before it was called that!) as an AI student, I'm pretty confident that DL is a transformative technology that will have a positive impact on nearly every application of software technology.

There's been a transformation in high-performance computing over the last ten years or so. GPU-acceleration, and its ability to enable massively parallel computation at a reasonable price, is behind this transformation. There's so much silicon available for so little money (thanks in a large part to our industry) that the single-instruction, multiple-data (SIMD) style of computing is superior for many tasks – especially simulation of nature and image processing where the underlying phenomena are naturally parallel. Whenever the same physics, chemistry – and therefore mathematical equations – operate globally, and complex behavior comes only from differences in data, SIMD is the perfect approach. Especially with clock speed plateaued at around 3.5GHz, SIMD computing scales far better into the future.

The key to the success of SIMD computing is that when silicon real estate is cheap enough, programs can afford not to be so clever about carefully choosing exactly what needs to be computed, but rather compute everything – because they can. Trying to be clever about choosing carefully what to compute takes time in itself. So, employing the "just do it" approach and running a program on 3000+ processors in parallel ends up being vastly faster. I refer to this brute-forcing computation as "Useful Waste." I think of this oxymoron because we know that a large percentage of the computation isn't going to end up being useful, but we just do it because we can afford to, and it is the fastest way to go. It produces more accurate results, too.

This same principle of Useful Waste in computing was extended to neural network model of computing to create DL. When DL was enabled by GPUs, the AI and ML worlds got a huge boost. DL takes Useful Waste to a whole different level. DL inherits from ML the notion that it's okay to take a long time to train the parameters through iterative optimization so long as the execution phase that uses those parameters is short enough to be practical. DL calls the execution phase "inferencing." So long as inferencing is fast enough (perhaps on GPUs, FPGAs, or specialized Tensor Core Units), the days, or even weeks, of computing time required to train is acceptable. Of course, the training time needs to be reasonably contained, which is where GPU acceleration came in to play in enabling the sudden surge in DL successes this decade. Usefully Wasting many cycles of trial-and-error in fitting hundreds or thousands of parameters to perform massive amounts of pattern matching turns out to enable a computing approach that was never before practical.

Simply put, DL turns the classic programming paradigm on its head. Instead of writing programs that transform a set of inputs to a set of outputs, DL takes a set of inputs and outputs and produces a program that transforms like inputs to like outputs through a massive network of pattern matching. It turns out that there is a subset of computing problems that can benefit tremendously from this approach, and DL has been producing results better than any humans could program before.

That's why for me, DL is what's new. Yes, DL is a subset of ML and AI which are subsets of computing. ML and AI are very important technologies on their own. But DL is what enabled ML, AI and computing to beat a chess master, to compose music or derive art in the style of certain artists, to describe pictures, or to transcribe and to translate, and accelerate autonomous driving. Ten years ago, the best programmers in the world had a hard time writing a program that reliably distinguishes a cat from a dog with 60% accuracy. Today, any student of DL can get 95% accuracy in any similar problems as an exercise in a week. What wasn't possible before has now been made possible with DL. Even though pattern matching is a small percentage of computing, surprisingly, DL transforms a very large fraction of anything affected by software.

Of course, 95% accuracy is grossly inadequate for our world. Unlike the typical examples, even including autonomous driving, where being better than the best human may already be good enough, in our world, many of the computing problems we have are solved by algorithms already. One way or another, these programs are made to be good enough to contribute to a 7-sigma standard. For DL to contribute in our world, it takes a lot of creativity. Our community has already started to figure this out as evidenced in the Deep Learning and Data Analytics session at the SPIE EUV and Photomask Technology Conference in Monterey, CA in September, 2018. Hope to see you there!!

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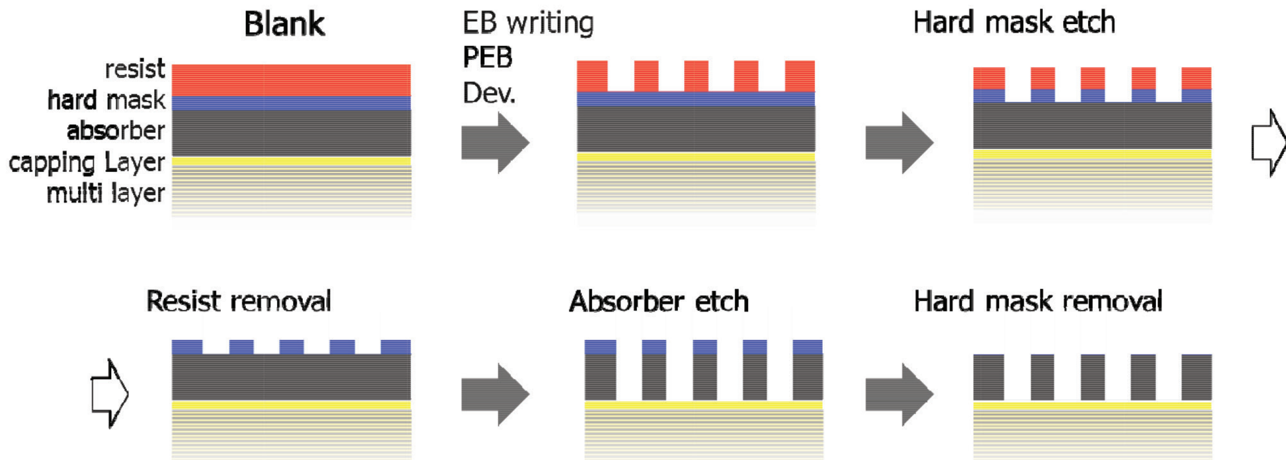


Figure 2. EUV mask process flow by using new blank.

Conventional EUV mask was fabricated by using resist mask for absorber etching. To achieve higher pattern resolution, we need to use thinner resist to avoid resist pattern collapse. But it was hard to reach EUV mask targets by using conventional mask process because of back scatter issue and absorber pattern top damage.[3][4] Moreover, LWR of conventional EUV mask were not achieved to the target that is 2.8nm or less.[3] It had been reported that fabrication process using Cr based hard mask had potential of 30nm pattern and beyond.[4] For fabrication of EUV mask with SRAF, we developed new mask process using new blank with thinner resist and Cr based hard mask.

2. Experimental Method

As shown in Figure 1, structure of EUV mask blank was changed to improve performance of resolution and LWR. We used thinner and lower sensitivity p-CAR (Positive tone Chemically Amplified Resist) to obtain high resolution and low LWR. And Cr based hard mask for absorber etching was used.

EUV mask process flow using new blank is shown in Figure 2. EUV mask process was optimized for new blank. Firstly, resist was patterned by EB writing. EB writing was carried out by EBM-9500 (NuFlare Technology, Inc.). Next hard mask was etched, and resist was removed, then absorber was etched using hard mask. Conventional dry etching processes are not suitable for new blank. Therefor each etching processes were optimized for new blank and established by using ARESTM (SHIBAURA MECHATRONICS CORPORATION). Finally hard mask was removed by using developed p ocess without Ru damaging.

EUV mask based on new blank structure was fabricated by using new mask process. And we evaluated resolution, CD performance and LWR of absorber pattern by top view and cross section SEM images.

3. Results and Discussion

3.1 Resolution

Top view and cross section SEM images of absorber pattern are shown in Figure 3. SEM images were absorber pattern of dense line, isolated space and isolated line. All patterns were achieved to target size. Significant improvement of resolution of absorber patterns was confirmed by using new process.

3.2 CD performance

3.2.1 CD linearity

CD linearity of dense line as primary feature was evaluated. Relationship between designed size and CD MTT of absorber pattern was plotted in Figure 4. CD MTT was defined by difference between measured space CD and designed size. The target of CD linearity for 44nm primary feature is 2.8nm or less from ITRS2013[5]. CD linearity was calculated by CD difference between designed size to 44nm and 120nm shown in this figure, and the result was 2.2nm. CD linearity performance was achieved.

3.2.2 CD uniformity

CD uniformity of primary feature was evaluated. Figure 5 shows CD uniformity of hp64nm and hp32nm dense line. CD uniformity was calculated as 3 sigma deviation of measured CD on mask area 104mm x 132mm. The results of both hp64nm and hp32nm dense line were 2.2nm. CD uniformity of primary feature had no dependence on pattern size. These targets are 1.8nm or less from ITRS2013[5]. These results were obtained without correction technique of EB writer. By using global CD uniformity correction, CD uniformities were estimated less than 1.8nm in both case. In other words, CD uniformity performance will be achieved by using global CD uniformity correction of EB writer.

CD uniformity of isolated pattern as SRAF was also evaluated. Figure 6 shows CD uniformity of 24nm isolated space and 30nm isolated line. CD uniformity of SRAF was almost same as hp64nm and hp32nm dense line. Therefore CD uniformity had no dependence on pattern type and its size. We confirmed CD uniformity performance of new mask process has potential to satisfy for fabrication of EUV mask with SRAF.

3.3 LWR analysis

3.3.1 Definition of mask LWR

We defined mask LWR for primary feature. Some studies about influence of mask LWR were reported.[6][7] For impact of mask LWR transfer to wafers, low spatial frequency part of line-edg roughness transfer function (LTF) was enhanced while high spatial frequency part was suppressed due to the numerical aperture limit of a scanner. From relationship between spatial frequency and LTF[6], enhanced part of normalized spatial frequency (NA/lambda) is 1 or less. For 0.33NA EUV lithography, enhanced cycle of mask roughness is 41nm (lambda/NA = 13.5/0.33) or more. As shown in Figure 7, LWR was calculated as three times standard deviation

Size [nm]	64	48	40	36	30	26	24
Primary feature Dense line target 44nm							
SRAF Isolated line target 30nm							Not OK
SRAF Isolated space target 24nm							

Figure 3. Top down and cross section SEM images of absorber pattern.

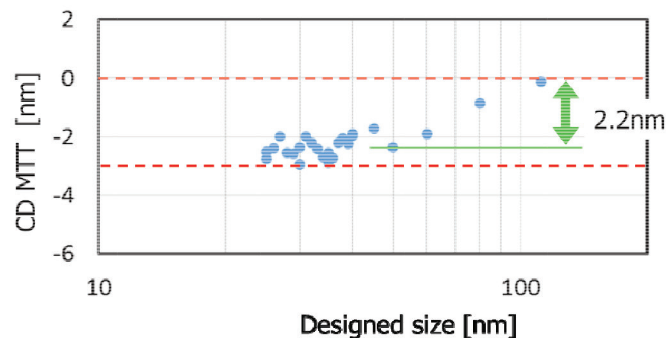


Figure 4. CD linearity of primary feature.

of averaged line widths per segment of 40nm length in this paper.

3.3.2 LWR of primary feature

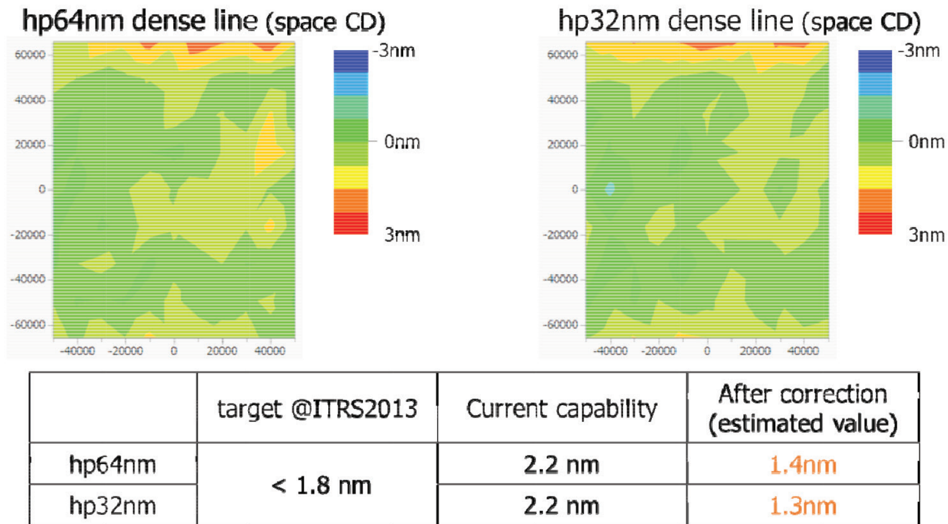
LWR of primary feature were compared between conventional and new process. Figure 8(a) shows SEM images of absorber pattern about hp64nm dense line by conventional and new process and hp32nm dense line by new process. Their LWR were calculated, and plotted in Figure 8(b). LWR of conventional process was about 5.5nm, and LWR of new process was about 3.1nm. As a result, LWR of new process was improved more than 40% comparing with conventional process. And we confirmed that LWR of primary feature for new process had no dependence on pattern size.

3.3.3 LWR of SRAF

We evaluated about LWR of isolated pattern as SRAF. Figure 9(a) shows SEM images of absorber pattern about isolated pattern by using conventional and new process. LWR of isolated pattern were compared between conventional and new process. Their LWR value were calculated, and plotted in Figure 9(b). LWR of isolated line was dramatically improved by using new process. And LWR of isolated space was almost same as primary feature. Improvement of LWR for these pattern types were confirmed by using new process.

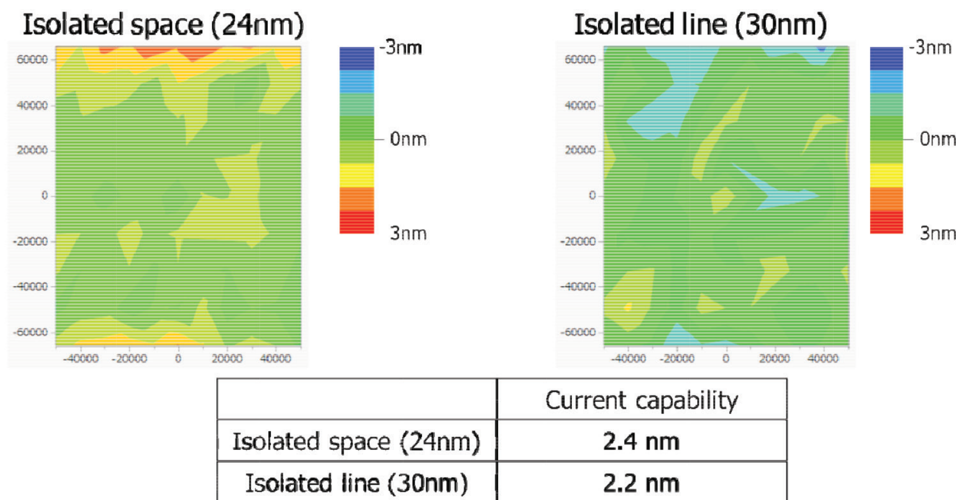
4. Summary and Outlook

New mask process of Ta based absorber EUV mask with high resolution and low LWR had been developed by using new blank with thinner resist and Cr based hard mask. Resolution of absorber pattern was achieved to targets of 44nm primary feature and 24nm-space/30nm-line SRAF. And we confirmed CD performance of new mask process has potential to satisfy for fabrication of EUV mask with SRAF. LWR of new mask process was improved more than 40% comparing with conventional process as primary feature. Improvement of LWR for primary feature and SRAF were confirmed by using new mask process. However LWR of primary



	target @ITRS2013	Current capability	After correction (estimated value)
hp64nm	< 1.8 nm	2.2 nm	1.4nm
hp32nm		2.2 nm	1.3nm

Figure 5. CD uniformity of dense line as primary feature.



	Current capability
Isolated space (24nm)	2.4 nm
Isolated line (30nm)	2.2 nm

Figure 6. CD uniformity of isolated pattern as SRAF.

feature was not achieved to the target (2.8nm or less). We will evaluate mask LWR impact on wafer, and make a study whether more improvement of LWR are necessary or not.

We developed new mask process of EUV mask with SRAF for 0.33NA EUV lithography. Furthermore improvement of defect is important to establish mask fabrication for high volume production. We will evaluate defect on EUV mask fabricated by new mask process.

5. Acknowledgement

The authors would like to thank HOYA Corporation for providing EUV mask blanks. The authors would like to thank Koji Murano, Noriko Iida, Tetsuo Takemoto and Mitsuyo Kariya of Toshiba Memory Corporation for their support of etching process and its evaluation.

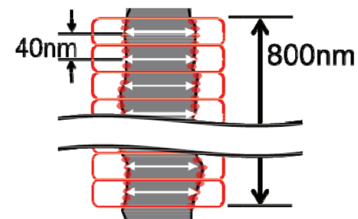
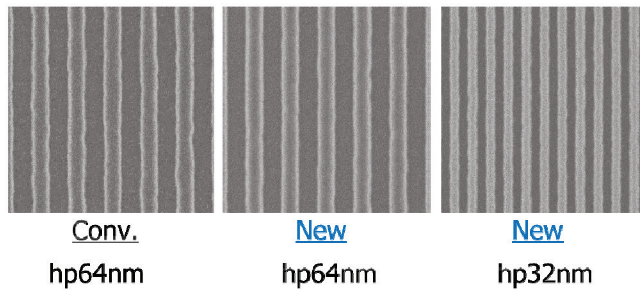


Figure 7. Diagram of calculated condition for LWR.



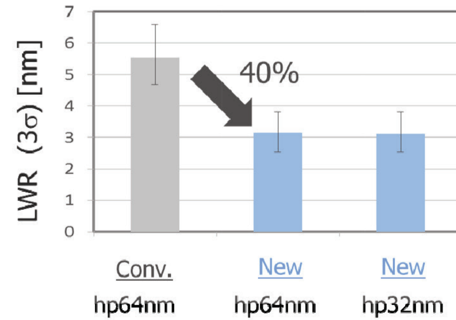
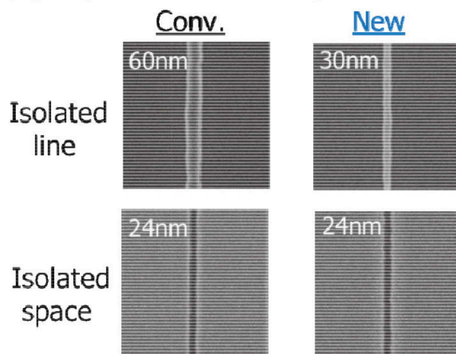


Figure 8. LWR of dense line as primary feature.



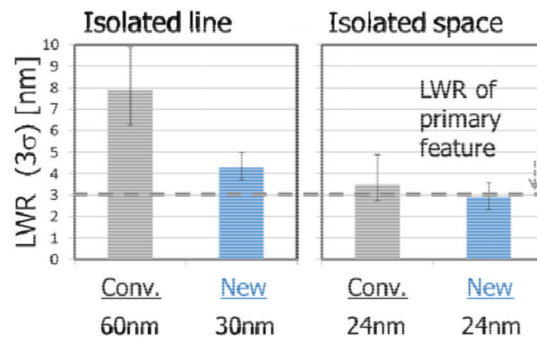


Figure 9. LWR of isolated pattern as SRAF.

7. References

[1] S. Hsu et al., "EUV resolution enhancement techniques (RETs) for k1 and below," **Proc. SPIE 9422,** 94221I (2015).

[2] T. Faure, "What's Different about EUV Masks ?" presented at eBeam Initiative "BACUS" Reception (September 11, 2017) [http://www.ebeam.org/docs/2017_ebeam_initiative_talk.pdf]

[3] Y. Inazuki et al., "Characterization of line-width roughness about 22-32nm node EUV mask", **Proc. SPIE 7748,** 774821 (2010)

[4] T. Abe et al., "Challenge for under 40nm size pattern making for EUV mask ", **Proc. SPIE 8701,** 87010R (2013)

[5] International Technology Roadmap for Semiconductors 2013.

[6] H. Tanabe, et al., "LER Transfer from a Mask to Wafers" **Proc. SPIE 6607,** 66071H (2007)

[7] C. Mack, "Impact of mask roughness on wafer line-edge roughness " **Proc. SPIE 7488,** 748828 (2009)

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Industry Briefs

TSMC says Variant of WannaCry Virus Brought Down its Plants

By **Larry Dignan,** ZDNET

A shutdown over the weekend that equated to a 3 percent revenue hit was blamed a variant of WannaCry and poor patching processes. TSMC said the virus that brought down its semiconductor fabrication plants was a variant of WannaCry. The company held a press conference and outlined what it has discovered so far.

TSMC, a major supplier to Apple's iPhone, said a "misoperation" led to the virus. TSMC had to bring plants offline on Friday and recouped 80 percent of capacity by late Sunday. The company will take a 3 percent revenue hit.

https://www.zdnet.com/article/tsmc-says-variant-of-wannacry-virus-brought-down-its-plants/

Moore's Law, China vs. Team USA, U.S. Military Lacks Leading-edge Chips

By **Rick Merritt,** EETimes

The U.S. Department of Defense is pushing for a $2.2 billion program to fund a broad range of electronics efforts. The news came at an event here where speakers agreed that Moore's Law is slowing but chip advances will continue thanks to a basket of alternatives to CMOS scaling.

The event was a coming-out party for the Electronics Resurgence Initiative (ERI), an evolving set of research programs valued at $1.5 billion over five years. They aim to counter two common enemies — the decline of Moore's Law and the rise of China.

http://eetimes.jp/ee/spv/1808/07/news025.html

Toshiba Memory Corporation Starts Construction of the First Fabrication Facility in Kitakami City, Iwate Prefecture

By **Toshiba Memory Corporation**

Toshiba Memory Corporation, the world leader in memory solutions, today held a groundbreaking ceremony for the first semiconductor fabrication facility (fab), called K1, in Kitakami, Iwate prefecture, in northeastern Japan. On its completion in autumn 2019, the facility will be one of the most advanced manufacturing operations in the world, dedicated to production of 3D flash memory.

Toshiba Memory continues to advance technologies in flash memory. The company is now leading the way forward with advances in its BiCS FLASH™, its proprietary 3D flash memory.

Demand for 3D flash memory is increasing significantly on fast growing demand for enterprise servers, datacenters and smartphones. Toshiba memory expects continued strong growth in the mid and long term. The new facility will make a major contribution to business competitiveness in corporation with Yokkaichi operations.

https://business.toshiba-memory.com/en-apac/company/news/news-topics/2018/07/corporate-20180724-2.html

ASML to Ship 20 EUV Systems in 2018

By **Nitin Dahad,** EETimes

Dutch semiconductor equipment vendor ASML said Wednesday it is on track to ship 20 extreme ultraviolet (EUV) systems in 2018 and expects to ship at least 30 more in 2019.

The company's estimates came as part of ASML's second quarter financial report, which included better-than-expected sales of EUV tools and overall sales of about $3.2 billion. "Gross margin was slightly above our guidance, reflecting the strength of our DUV and applications business and progress in EUV profitability," said ASML CEO Peter Wennink.

https://www.eetimes.com/document.asp?doc_id=1333492

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About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

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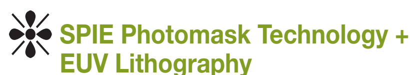

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