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Nanoimprint Lithography Methods for Achieving sub-3nm Overlay

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Abstract

Imprint lithography is an effective and well-known technique for the replication of nano-scale features. Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field/shot-by-field/shot deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate. The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

First, the authors are going to review and discuss the previous studies in this paper. Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single-level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications. In previous papers, the overlay has been addressed by applying methods that are unique to NIL. In 2018, Hiura et al. reported a mix and match overlay (MMO) of 3.4nm and a single machine overlay (SMO) across the wafer was 2.5nm using an FPA-1200 NZ2C four station cluster tool. These results were achieved by combining a magnification actuator system with a High Order Distortion Correction (HODC) system, thereby enabling the correction of high order distortion terms up to K30. The HODC system utilizes a digital mirror device (DMD) to correct distortion on a field-by-field basis. Further improvements to the system have been achieved by extending the range of the HODC system by applying a diamond-like carbon film to the wafer chuck to reduce friction. Other process variables that are unique to NIL and that can be considered as process tunable variables include imprint force and tip/tilt of the imprint head relative to the wafer substrate during exposure. These variables can be used to modulate and control the overlay errors near the imprint field edges and provide

		2021	2022-2024	2025 -->	NIL Status
3D NAND		20nm	20nm	20nm	
Stack Layers		96-128	128-192	192 -->	
LS (min HP)		20nm	20nm	20nm	
Hole (min HP)		80nm	80nm	80nm	
NIL Mask	LS	Demonstrated 14nm L/S @SPIE2018			
	Hole	Demonstrated 16nm Hole @SPIE2019			
DRAM		1Znm	1Anm	1Bnm	DRAM
LS (min HP)		16nm	14nm	12nm	• Patterning good down to 14nm • Overlay needs to be demonstrated
Hole (min HP)		24nm	21nm	18nm	
NIL Mask	LS	Demonstrated 14nm L/S			
	Hole	Demonstrated 16nm Hole			
SCM					Storage Class Memory
LS (min HP)		20nm	14nm	12--> 10nm	• Patterning good down to 14nm • Overlay needs to be demonstrated
NIL Mask	LS	Demonstrated 14nm L/S @SPIE2018			
Logic		5nm	3nm	2nm	Logic
LS (min HP)		15nm	12nm	10nm	• Patterning requires improvements in mask technology starting at 3nm • Defectivity is still challenging
Hole (min HP)		24nm	22.5nm	21nm	
NIL Mask	LS	Demonstrated 14nm L/S			
	Hole	Demonstrated 16nm Hole			

Figure 1. NIL roadmap for advanced semiconductor devices.

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EDITORIAL

High-NA EUV Lithography Challenges: Part II

Henry Kamberian, Photronics, Inc.

Last month, in the previous part of this review, I discussed the challenges of High-NA EUV lithography technology, which drives major changes to EUV masks. These challenges highlight the need for new or improved solutions in key mask-making areas, such as:

In mask data preparation (MDP), the requirement for data fracture solutions is fully vetted to ensure post-fracture data integrity of anamorphic designs including the need for intelligent OPC-aware MRC tooling. This is especially critical for design layouts with complex OPC and Inverse Lithography Technology (ILT) curvilinear features with ILT masks being important for High-NA EUV.

For EUV blanks, the requirement for substrates with new reporting metrics for thermal properties as related to overlay impact at higher source power, and for substrate flatness to meet focus and overlay as related to reticle clamping in the scanner. For novel absorber blanks, tighter controls on absorber thickness uniformity, lower defectivity, and EUV reflectivity.

In EUV mask patterning, while Multi-beam and VSB-based (albeit much slower) ebeam mask writers platforms have been the workhorse delivering current EUV mask capability, newer generation mask-writers with improved resist systems needed to meet resolution and critical dimension control requirements, especially for masks with curvilinear shapes required for ILT. Other areas of the patterning process needing innovation are etch and cleaning of novel absorbers. The EUV mask Black-Border patterning process must improve to meet tightening dimensional, placement, and EUV reflectivity controls needed to enable half-field stitching masks.

In defect inspection, resolution limitations of optical inspection systems reinforce the need for advancement of actinic inspection and even e-beam (multi-beam for speed) platforms with defect sensitivity well below 15nm. For blanks, an actinic blank inspection of EUV multilayer is still required and must improve in sensitivity and defect location accuracy – note there are even discussions of changing multi-layer materials.

For mask defect repair, current e-beam and nanomachining platforms used for repair, and considered complementary, must improve resolution and repair capability processing novel absorber materials.

Lastly, for EUV pellicle, new and improved materials are needed to meet transmission uniformity and compatibility with high-energy illumination of a High-NA system including the possibility of compatibility with post-pellicle attach defect inspection.

While I am perhaps stating the obvious, we cannot underestimate the task ahead with all these new requirements in critical mask-making areas. The industry must converge to mask technology solutions in support of High-NA EUV lithography, but simultaneously also consider the productivity, yield, and cost components of these solutions. It is vital for the industry to work together to arrive at mask technology solutions requiring greater collaboration from all stakeholders: MDP software providers, blank suppliers, mask equipment manufacturers, mask-makers, and ultimately our customers including ASML.

One example requiring considerable industry collaboration is the proposal Mark Phillips (Director of lithography hardware and solutions at Intel) made at the 2022 SPIE Advanced Lithography + Patterning conference for the industry to consider changing EUV mask blank substrate from 6-inch square to 300mm round substrates for High-NA EUV. Clearly, using a 300mm round mask would allow the use of the full exposure field size at the 4x/8x reduction ratio. Whereas processing 300mm round mask substrates would be harmonious with current wafer processing equipment, the implication in other areas of mask making is enormous. From substrate/blank manufacturing, mask patterning, inspection, metrology, repair, pellicle, and related handling, all will need significant changes made to tooling and infrastructure to accommodate 300mm round substrates, even ASML will need to change mask (or reticle) stage and related handling within the scanner.

In the past, we have seen other major substrate initiatives (i.e., 450mm silicon wafers, 9 inches, and even 6x9 inch mask) started, but eventually failed adoption for one reason or another. Such major initiatives require a well-funded and coordinated program involving the entire industry. Perhaps the 300mm round mask substrate initiative can be a supported program within the latest governmental semiconductor industry programs such as US and EU chip acts. This is something to consider!

With the 2022 Photomask Technology conference (Monterey, California) behind us, the presentations and discussions on High-NA EUV with specifics on EUV mask technology provide us with additional insight into solution paths, as we prepare for future mask technology in support of High-NA EUV lithography.

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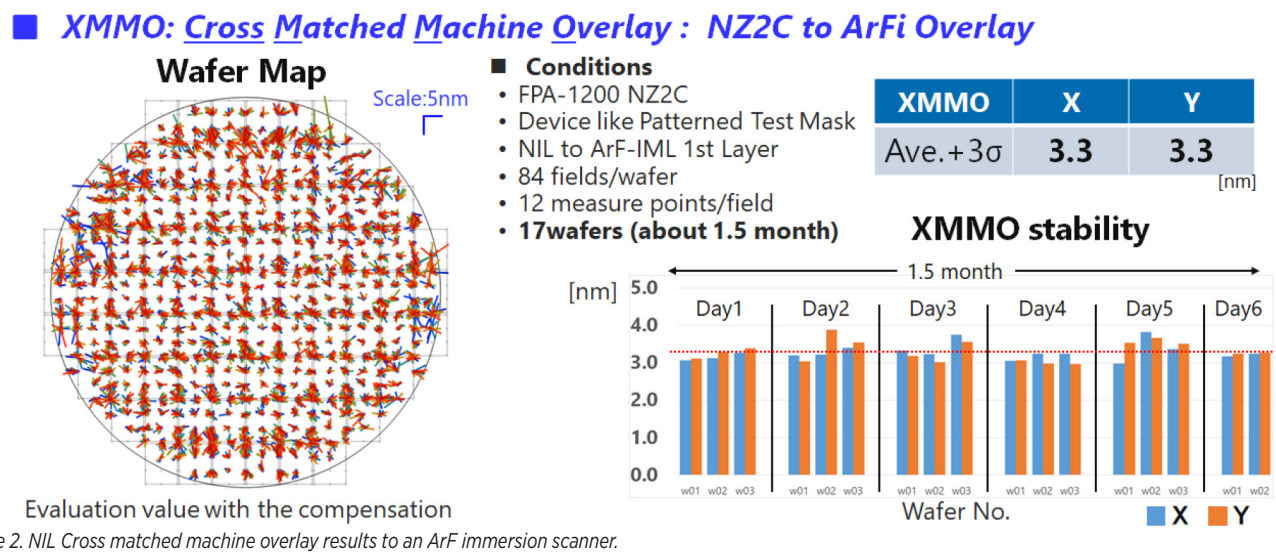


Figure 2. NIL Cross matched machine overlay results to an ArF immersion scanner.

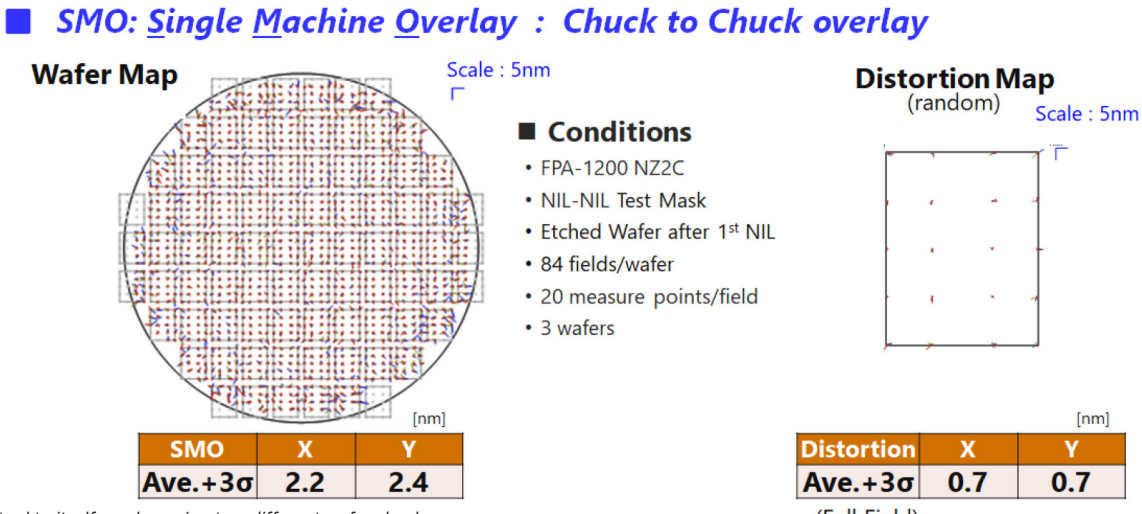


Figure 3. NIL tool to itself overlay, using two different wafer chucks.

good overlay control. An additional method to improve overlay is Drop Pattern Compensation (DPC). DPC is used to create a resist drop pattern designed to remove non-flatness originating either from the wafer/wafer chuck or pattern topography, to minimize mask bending.

Finally, it is also possible to correct distortion signatures on a wafer by fabricating a "refined" mask that takes into account the distortion signature. We show the concept of the refined mask, and the refined mask is enabling a reduction in the common distortion from the previous level. The purpose of this paper is to describe the application of the refined mask and the other methods discussed on the previous studies to realize cross mix and match overlay (XMMO) of less than 3nm.

1. Introduction

Imprint lithography is an effective and well-known technique for the replication of nano-scale features.[1,2] Nanoimprint lithography (NIL) manufacturing equipment utilizes a patterning technology that involves the field-by-field deposition and exposure of a low viscosity resist deposited by jetting technology onto the substrate.[3-9] The patterned mask is lowered into the fluid which then quickly flows into the relief patterns in the mask by capillary action. Following this filling step, the resist is crosslinked under UV radiation, and then the mask is removed, leaving a patterned resist on the substrate. The technology faithfully reproduces patterns with a higher resolution and greater uniformity compared to those produced by photolithography equipment. Additionally, as this technology does not require an array of wide-diameter lenses and the expensive light sources necessary for advanced photolithography equipment, NIL equipment achieves a simpler, more compact design, allowing for multiple units to be clustered together for increased productivity.

Previous studies have demonstrated NIL resolution better than 10nm, making the technology suitable for the printing of several generations of critical memory levels with a single mask. In addition, resist is applied only where necessary, thereby eliminating material waste. Given that there are no complicated optics in the imprint system, the reduction in the cost of the tool, when combined with simple single-level processing and zero waste leads to a cost model that is very compelling for semiconductor memory applications.

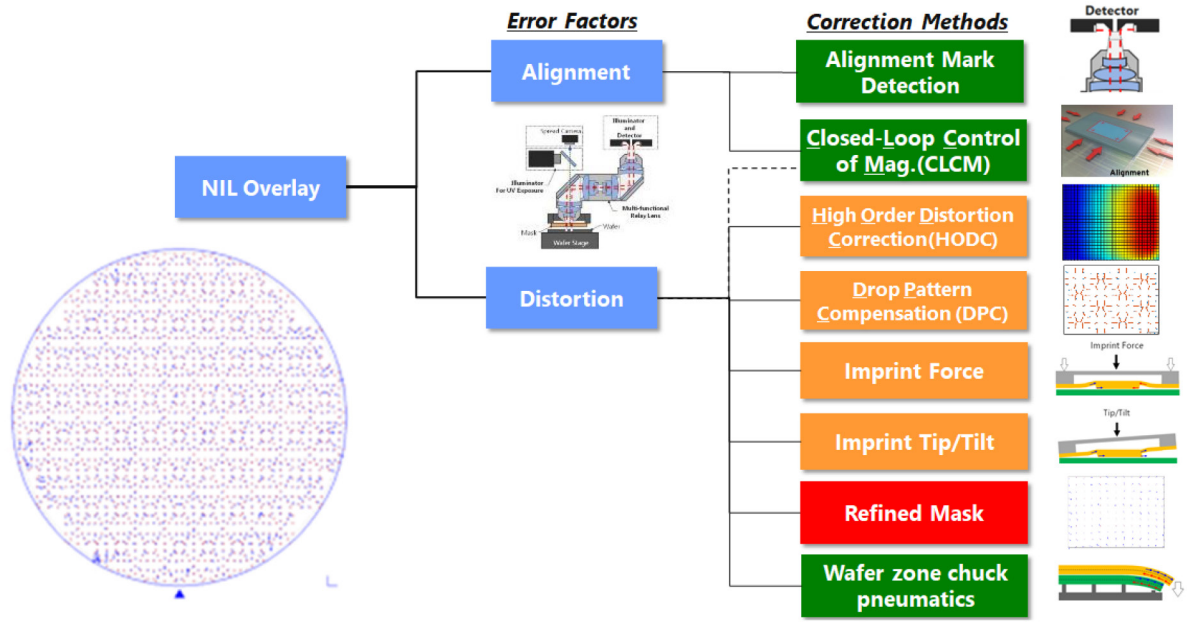


Figure 4. To address overlay in a Nanoimprint system, there are many factors that need to be considered, some of which are quite different than what is required for photolithography equipment. Generally speaking, the process can be broken down into two categories: Alignment and Distortion.

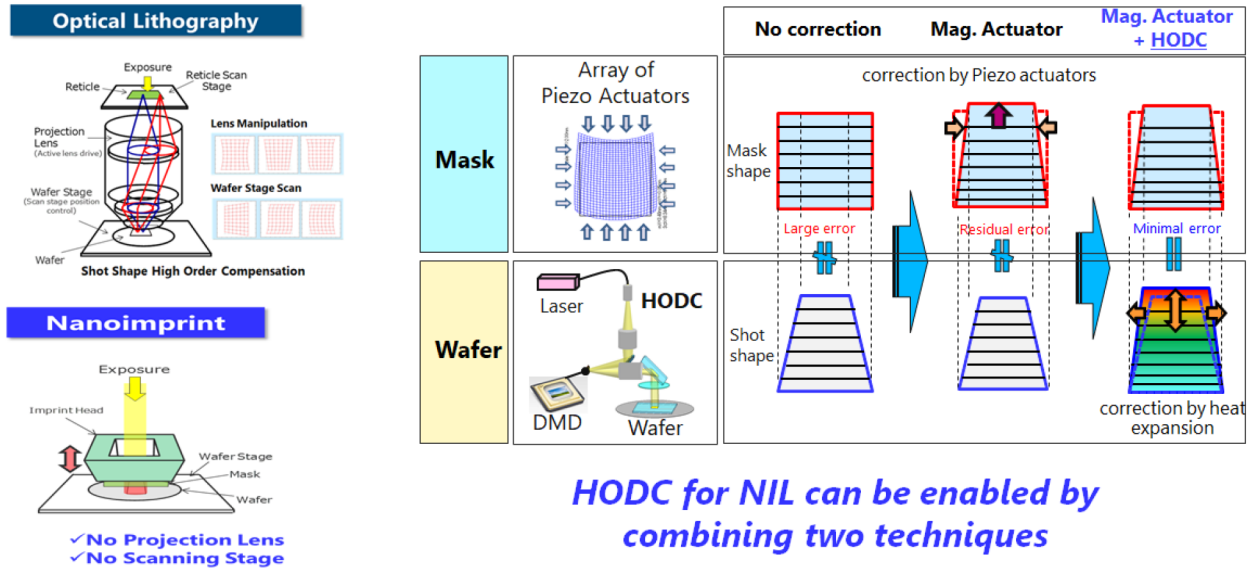


Figure 5. The HODC method uses a combination of magnification correction and heat input to address distortion.

Any new lithographic technology to be introduced into manufacturing must deliver either a performance advantage or a cost advantage. Key technical attributes include alignment, overlay, and throughput. In previous papers, overlay and throughput results have been reported on test wafers. In 2018, Hiura et al. reported a mix and match overlay (MMO) of 3.4nm and a single machine overlay (SMO) across the wafer was 2.5nm using an FPA-1200 NZ2C four station cluster tool.[10] These results were achieved by combining a magnification actuator system with a High Order Distortion Correction (HODC) system, thereby enabling the correction of high order distortion terms up to K30.

Advanced memory devices such as DRAM and storage class memory are challenging because the roadmaps call for continued scaling, eventually reaching half pitches of 14nm and beyond. For DRAM, overlay on some critical layers is much tighter than NAND Flash, with an error budget of 15-20% of the minimum half pitch. For 14nm, this means 2.1-2.8nm. DRAM device design is also challenging, and layouts are not always conducive to pitch-dividing methods such as SADP and SAQP. This makes a direct printing process, such as NIL, an attractive solution.

2. Overlay Correction Knobs

Cross-matched machine overlay (XMMO) to an ArF immersion scanner of 3.3nm has been demonstrated.[11] Stability testing has also confirmed that

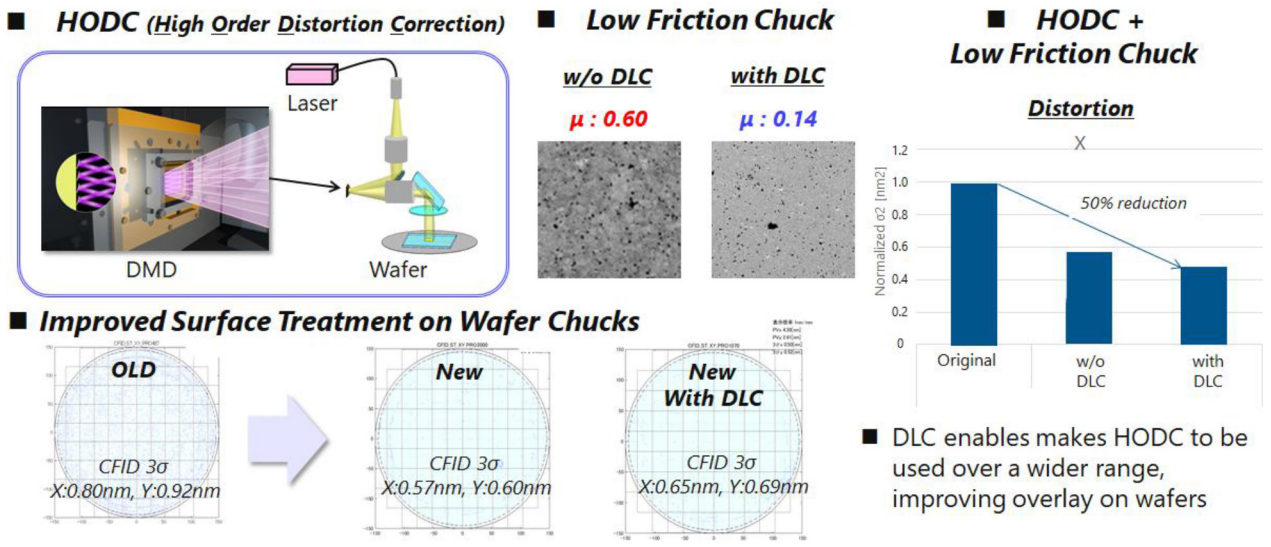


Figure 6. A DLC-coated chuck enables the use of HODC over a wider range.

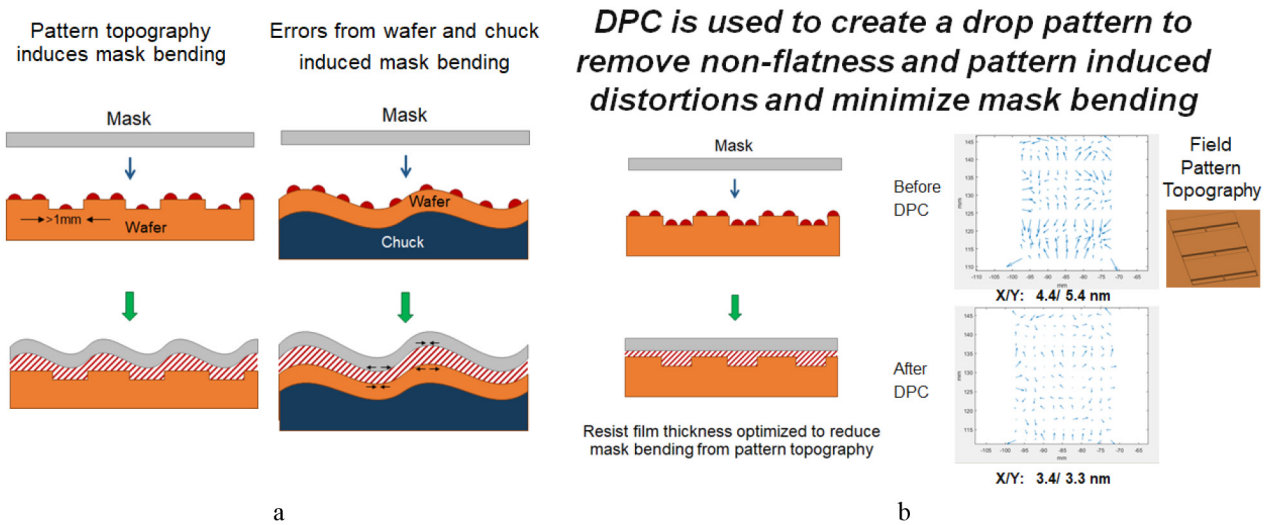


Figure 7. Drop Pattern Compensation can be used to remove topography induced from either pattern topography or wafer/chuck topography.

the performance is repeatable over a six-week period as shown in Figure 2.

Once inserted into a device flow, NIL will also need to demonstrate a good tool for itself overlay, in order to address DRAM overlay budgets. Shown in Figure 3 is a 3-wafer run in which a NIL test mask is used to demonstrate overlay on etched wafers patterned using a NIL tool. For this experiment, two different wafer chucks were used to understand the variations introduced from multiple chucks. The demonstrated overlay was 2.2nm in x and 2.4nm in y respectively, with a mean plus 3 sigma distortion of only 0.7nm.[11]

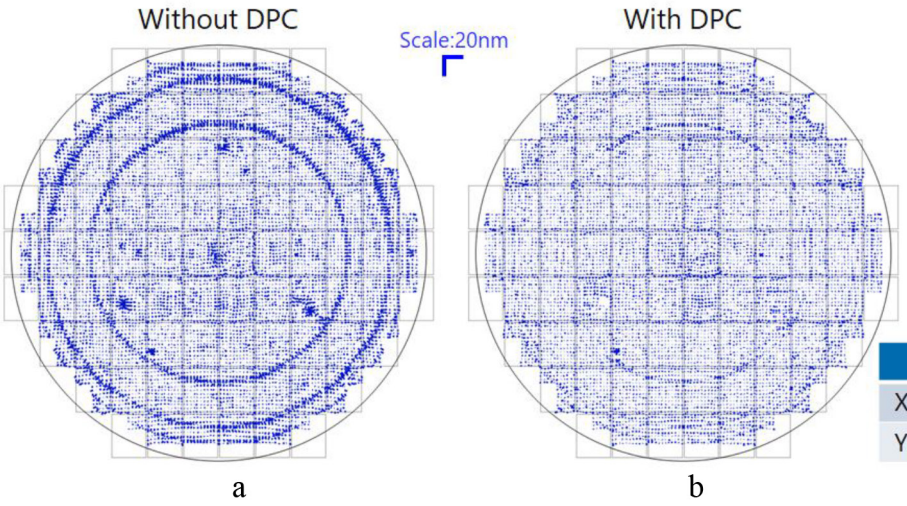
To address overlay in a Nanoimprint system, there are many factors that need to be considered, some of which are quite different than what is required for photolithography equipment. The process can be broken down into two categories: Alignment and Distortion. In the past, we have discussed alignment and our closed-loop magnification control system. In this paper, we will briefly review some of the more recent work on High Order Distortion Correction and Drop Pattern Compensation, and then move on to discuss how to imprint force, Tip/Tilt, and wafer zone pneumatics are applied to further enhance overlay capability. Finally, we introduce the concept of a refined mask for further overlay improvement. Figure 4 schematically illustrates the various tuning knobs used for NIL.

a. High Order Distortion Correction (HODC)

In optical lithography, High Order Compensation is done by manipulating both lens and stage during the exposure process. A different approach is required for nanoimprint. High Order Distortion Correction (HODC) for NIL can be enabled by combining two techniques (See Figure 5.).

- One is using Magnification actuators, which apply force using an array of piezo actuators.
- Second is Heat input, which is supplied through a DMD to correct distortion on a field-by-field basis.

Further improvements to HODC have been realized by applying a diamond-like carbon (DLC) layer on the wafer chuck. HODC is a method in which distortion is modified with heat deformation of wafer field shape. The friction of the wafer chuck surface has a strong relationship



	w/o DPC	w/ DPC
X : 3-sigma	3.8	2.5
Y : 3-sigma	3.8	2.4

Figure 8. Reduction of chuck-induced distortion after applying DPC.

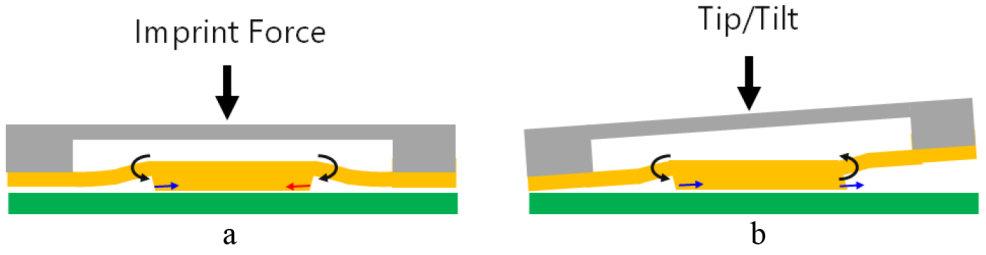


Figure 9. a) Imprint Force. b) Tip/Tilt.

with the control range. We adapted a DLC-coated chuck to realize low friction.[12] Doing so reduces the coefficient of friction from 0.60 to 0.14. The improvement is illustrated in Figure 6.

b. Drop Pattern Compensation

Next, we describe how resist drop patterns can be used to enhance overlay. Drop patterns are necessary to fill mask features and typically create a uniform resist film across a NIL stepper field. As shown in Figure 7a, a drop pattern over either pattern topography or existing wafer and chuck topography can induce mask bending, which results in unwanted distortion.

Drop Pattern Compensation or DPC is used to create a drop pattern to remove non-flatness and pattern-induced distortions and minimize mask bending. In a previous publication, mask bending and distortion resulting from pattern topography were minimized with a drop pattern (Figure 7b) designed to reduce mask bending.[13] Before DPC, the field pattern topography has a noticeable effect on distortion. After applying DPC, the distortion is significantly reduced.

In a similar way, DPC can also be used to remove the distortions resulting from chuck non-flatness. Pictured in Figure 8a is a distortion map of an older design chuck. Distortion is noticeable in the areas that define the lands and lift pins on the chuck. By applying DPC, the distortions are again significantly reduced from about 3.8nm to 2.5nm (Figure 8b).

c. Imprint Force, Tip/Tilt, and Wafer Edge Pneumatics

Next, we discuss some of the other knobs that can be used to improve overlay, particularly near the edge of the wafer. For Nanoimprint Lithography, rheology plays a large factor, making it quite different than projection lithography, in which optics plays a dominant role. This means that the way in which overlay is addressed at the edge of the wafer is also quite different than optical lithography. In general, it is important to address three parameters that can impact overlay.

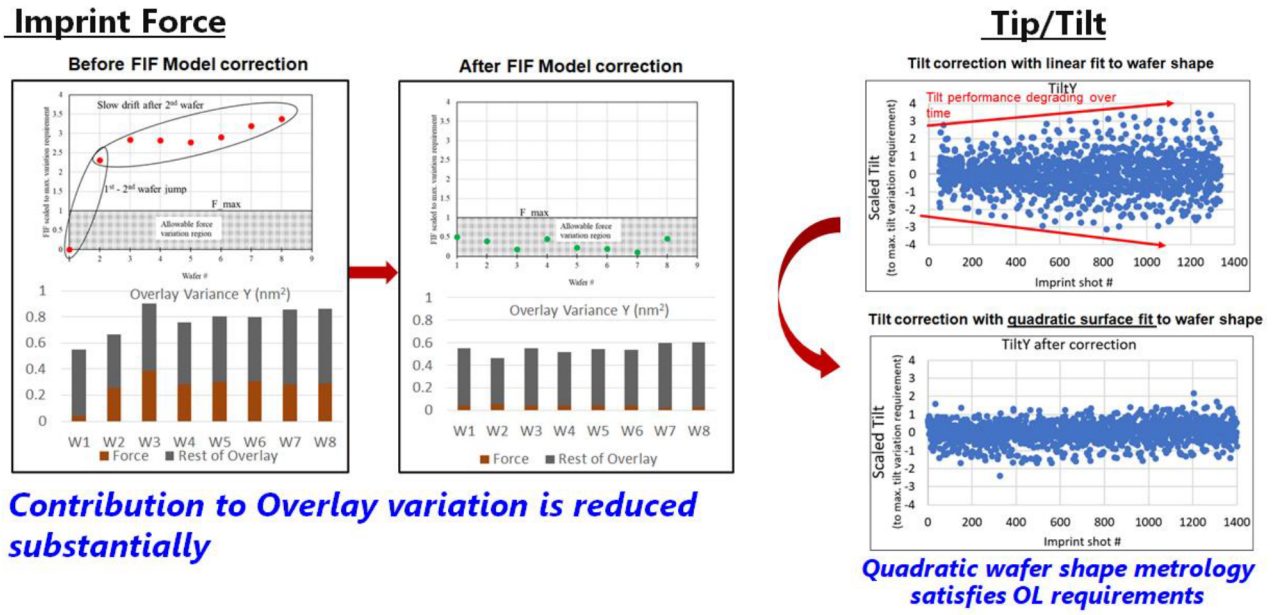
- Imprint Force
- Mask-to-Wafer Tip/Tilt
- Wafer zone pneumatics near the wafer edge

The imprint force refers to the force exerted against the substrate during UV cure (Figure 9a). If not controlled, it can induce in-plane overlay errors. Therefore, models have been developed, aided with experimental data to control overlay at the edge of a field. Similarly, Tip/Tilt describes the relative angle between the template plane & local substrate plane fit during exposure (Figure 9b). If not controlled, it can result in degrading overlay performance over time. Therefore, models have been developed, in which a quadratic fit is used and fed forward to correct relative tilt for every field. The developed models have helped to significantly reduce overlay errors.

Figure 10a illustrates the reduction of drift and overlay variance as applied to imprint force. Figure 10b shows the improvement in tip/tilt control. For a more detailed understanding of these models, please see the proceedings paper by Roy et al.[14]

Imprint force applied to the substrate induces bending at the edge of the template. It is important to carefully control the force and use it to compensate for higher-order distortion errors such as k13, 14, 17, 18, and so on.

Similarly, tip and tilt can induce mask bending. Once again, the impact on edge fields is more noticeable, and tip/tilt control is critical for reducing these errors and can be used to compensate for errors near the field



a b

Figure 10. a) illustrates the reduction of drift and overlay variance as applied to imprint force. b) shows the improvement in tip/tilt control after applying the models developed.

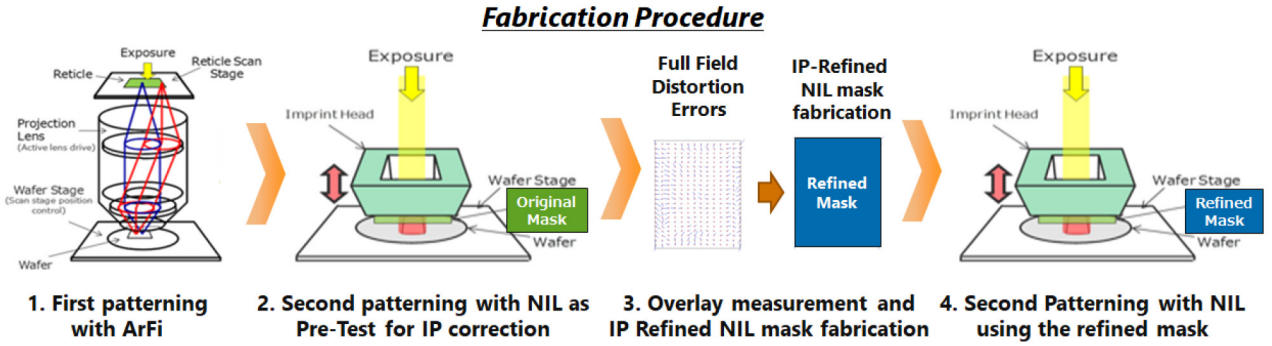


Figure 11. Schematic illustration of the refined mask procedure.

edges like k7 and k10, etc. by tilting in x and k8 and k9, etc. by tilting in y.

In particular, the wafer edge and partial fields have a larger OL error than full fields because of the wafer chuck differences between ArF immersion and NIL. Initial studies show that by controlling the wafer vacuum at the wafer edge, we can again reduce the edge field distortion. This capability represents a further opportunity to improve mix and match overlay. See the proceedings paper by Hiura et al. for a more detailed description of imprint force, tip and tilt correction, and wafer pneumatics.[15]

d. Refined mask

The final method that is currently being implemented to further correct distortion errors is the use of a refined mask. The concept is illustrated in Figure 11 and the following procedure is applied to improve cross-matched machine overlay (XMMO):

1. The patterning of a first layer using ArF immersion lithography
2. A second patterning step using nanoimprint lithography as a means of understanding image placement correction
3. A feed-forward procedure in which the common distortion of the previous layer is identified and corrected with a refined mask
4. Patterning of the second level using the refined mask, along with HODC to reduce overlay errors

An example of the application of a refined mask is discussed below. After patterning the first level with an ArF immersion scanner and printing the second level with NIL, the common distortion from the first level was identified and fed forward to create a refined mask. The original mask distortion and the corrected distortion are shown in Figure 12.

The resulting overlay map after applying the refined mask is shown in Figure 13. An overlay of 2.53nm in x and 2.12nm in y was achieved for the full fields. The overlay for full + partial fields was 3.17nm in x and 2.74nm in y. These results were obtained through a combination of the refined mask, HODC, imprint force control, and tip/tilt control.

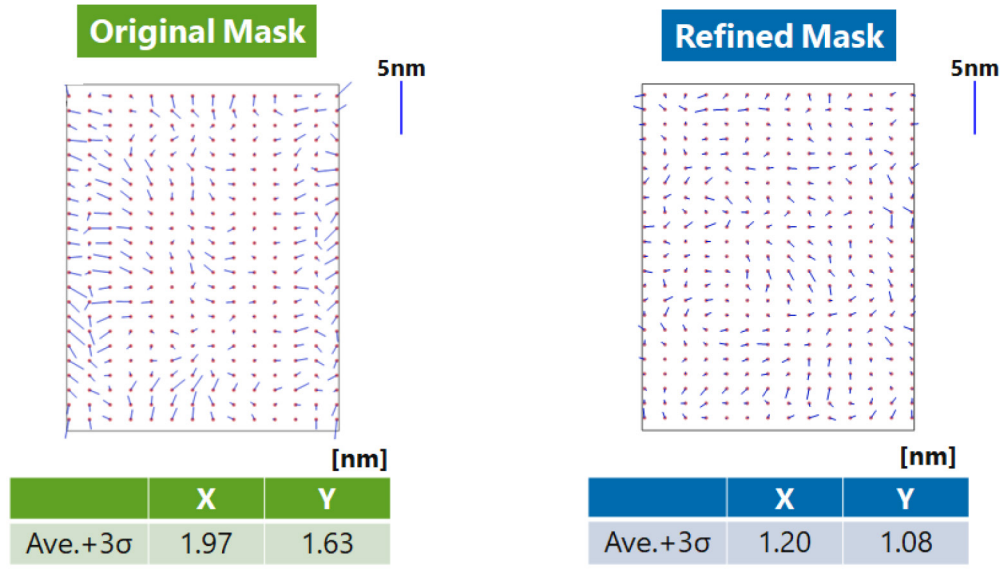


Figure 12. A refined mask was created, enabling a reduction in the common distortion from the previous level.

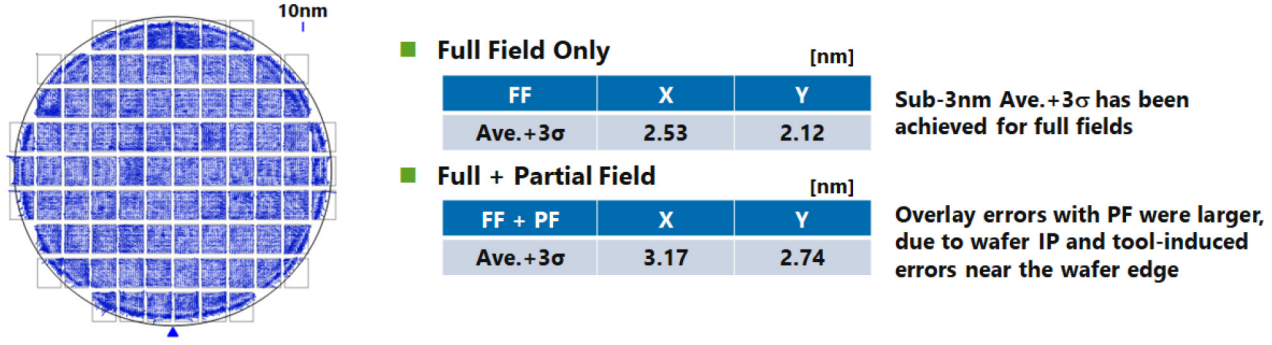


Figure 13. Cross-matched machine overlay after applying a refined mask. Full-field errors have been reduced to 2.53nm in x and 2.12nm in y, respectively.

Finally, Figure 14 illustrates the reduction in overlay errors because of applying the refined mask. The overall distortion was significantly improved, and as noted above overlay reduction was mainly observed in the full fields. Note that Drop Pattern Compensation (DPC) was not applied for these tests and will be used in the future to improve the overlay performance of the partial fields.

3. Conclusions

Advanced memories such as DRAM and storage class memory are challenging because the roadmap for DRAM calls for continued scaling, eventually reaching half pitches of 14nm and beyond. For DRAM, overlay on some critical layers is much tighter than NAND Flash, with an error budget of 15-20% of the minimum half pitch. For 14nm, this means 2.1-2.8nm. DRAM device design is also challenging, and layouts are not always conducive to pitch-dividing methods such as SADP and SAQP. This makes a direct printing process, such as NIL, an attractive solution.

In this paper, we reviewed the performance improvements related to overlay. With respect to overlay, high order distortions can be addressed by selective heating of a wafer field. In addition, we briefly reviewed how drop patterns can be used to remove distortions caused by either pattern topography or wafer/chuck topography. Other new control methods such as imprint force, mask to wafer tip/tilt, and pneumatic controls at the wafer edge were also discussed. Finally, we introduced the refined mask concept and showed how it can be applied to remove common distortion in full fields and improve cross-matched machine overlay. The overlay reduction was mainly observed in the full fields. It is important to note that Drop Pattern Compensation (DPC) was not applied for these tests and will be used in the future to improve the overlay performance of the partial fields.

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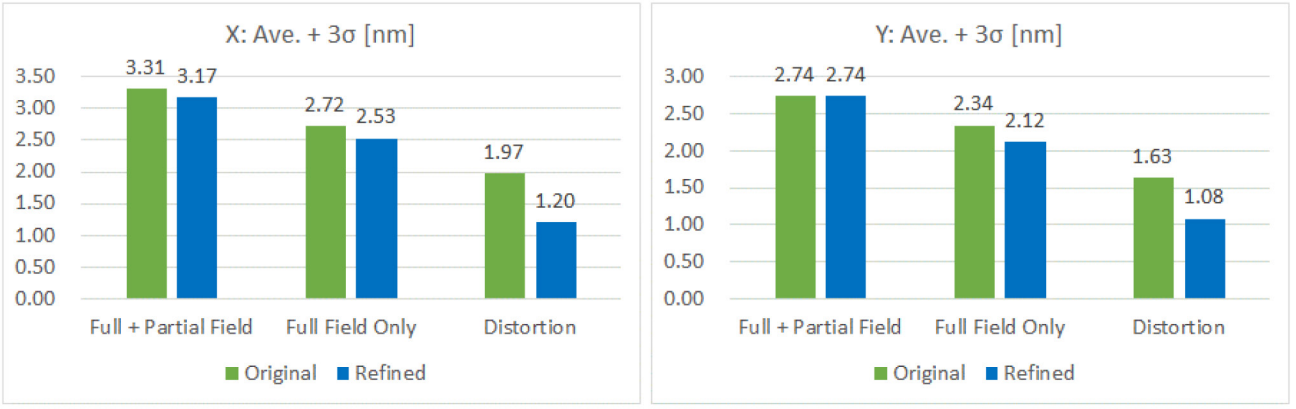

Figure 14. The improvement of cross-matched machine overlay using a refined mask. The overall distortion was significantly improved. The overlay reduction was mainly observed in the full fields. Note that Drop Pattern Compensation (DPC) was not applied for these tests and will be used in the future to improve the overlay performance of the partial fields.

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Industry Briefs

President Biden Signs CHIPS and Science Act into Law

On August 9, 2022, President Biden signed the CHIPS and Science Act (H.R.4346), which seeks to bolster the US semiconductor supply chain and promote research and development of advanced technologies in the United States. The Act is comprised largely of provisions extracted from the US Innovation and Competition Act (USICA) and its House alternative, the America COMPETES Act. The CHIPS and Science Act encompasses the most popular provisions of the USICA and COMPETES bills, but modifies and adds to those provisions, specifically mentioning:

- $52.7 billion appropriation for semiconductor incentives.
- "FABS Act" investment tax credit.
- Limits on the expansion of manufacturing capacity in China.
- Funding authorization for R&D programs.

https://www.whitecase.com/insight-alert/president-biden-signs-chips-and-science-act-law

Micron Breaks Ground on Leading-Edge Manufacturing Fab in Boise, Idaho

The company celebrates the initiation of historic $15 billion investment; construction is expected to begin early in 2023, with DRAM production slated for the second half of the decade.

Micron Technology, Inc. (NASDAQ: MU), one of the world's largest semiconductor companies and the only U.S.-based manufacturer of memory, broke ground on its leading-edge memory manufacturing fab in Boise, Idaho. This will be the first new memory manufacturing fab in the United States in 20 years. Micron marked the occasion with a ceremony attended by U.S. Secretary of Energy Jennifer M. Granholm, White House Office of Science and Technology Policy Acting Director Dr. Alondra Nelson, Senator Jim Risch, Idaho Governor Brad Little, and Boise Mayor Lauren McLean.

https://investors.micron.com/news-releases/news-release-details/micron-breaks-ground-leading-edge-manufacturing-fab-boise-idaho

TSMC to Mmass Produce Chips on Upgraded Version of 3nm Pprocess in 2023

Taipei, Sept. 12 (CNA) Taiwan Semiconductor Manufacturing Co. (TSMC), the world's largest contract chipmaker, plans to roll out chips made on an upgraded version of its sophisticated 3-nanometer process in 2023.

According to TSMC, the development of its high-end processes has been proceeding smoothly and commercial production of the 3nm process will start later this year, with the upgraded version, known as 3nm enhanced (N3E), to begin commercial production a year later.

The 3nm process started a trial run last year, with the 5nm process the latest technology for which TSMC launched mass production, accounting for 21 percent of the chipmaker's total sales in the second quarter of this year.

TSMC's 3nm family uses FinField-effect-transistor (FinFET) technology, a 3D transistor structure that allows a chip to run faster using the same amount of power or to run at the same speed on reduced power.

https://focustaiwan.tw/sci-tech/202209120012

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About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

Individual Membership Benefits include:

- Subscription to BACUS News (monthly)
- Eligibility to hold office on BACUS Steering Committee

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Corporate Membership Benefits include:

- 3-10 Voting Members in the SPIE General Membership, depending on tier level
- Subscription to BACUS News (monthly)
- One online SPIE Journal Subscription
- Listed as a Corporate Member in the BACUS Monthly Newsletter

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CALENDAR

2023

SPIE Advanced Lithography + Patterning
26 February–2 March 2023
San Jose, California, USA
www.spie.org/al

SPIE Photomask Technology and EUV Lithography
1-5 October 2023
Monterey, California, USA
www.spie.org/puv

European Mask and Lithography Conference (EMLC) 2023
19-21 June 2023
Dresden, Germany
www.emlc-conference.com

Photomask Japan (PMJ) 2023
25-27 April 2023
Online only
www.photomask-japan.org

You are invited to submit events of interest for this calendar. Please send to lindad@spie.org.

SPIE, the international society for optics and photonics, brings engineers, scientists, students, and business professionals together to advance light-based science and technology. The Society, founded in 1955, connects and engages with our global constituency through industry-leading conferences and exhibitions; publications of conference proceedings, books, and journals in the SPIE Digital Library; and career-building opportunities. Over the past five years, SPIE has contributed more than $22 million to the international optics community through our advocacy and support, including scholarships, educational resources, travel grants, endowed gifts, and public-policy development. www.spie.org.

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