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High-throughput parallel SPM for metrology, defect and mask inspection

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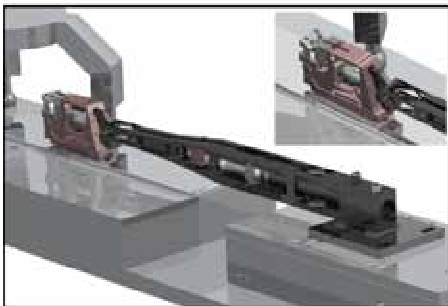
ABSTRACT

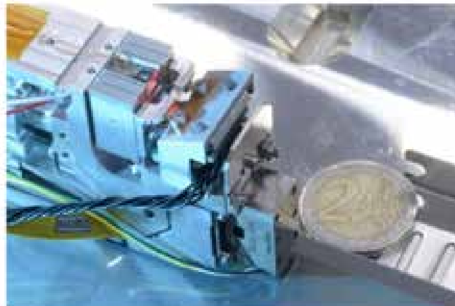
Scanning probe microscopy (SPM) is a promising candidate for accurate assessment of metrology and defects on wafers and masks, however it has traditionally been too slow for high-throughput applications, although recent developments have significantly pushed the speed of SPM.[1,2] In this paper we present new results obtained with our previously presented high-throughput parallel SPM system[3,4] that showcase two key advances that are required for a successful deployment of SPM in high-throughput metrology, defect and mask inspection. The first is a very fast (up to 40 lines/s) image acquisition and a comparison of the image quality as function of speed. Secondly, a fast approach method: measurements of the scan-head approaching the sample from 0.2 and 1.0 mm distance in under 1.4 and 6 seconds respectively.

1. Introduction

As the semiconductor industry is fast approaching the 10 nm node, demands on metrology tools are becoming ever more stringent. New methods for accurate assessment of metrology and defects on wafers and masks are emerging. A promising candidate for this is scanning probe microscopy (SPM), but it has traditionally been too slow for high-throughput applications. Recent developments have significantly pushed the speed of SPM,[1,2] but we think that for real high-throughput parallelization is needed as



(a)



(b)

Figure 1. (a) CAD illustration of one positioning arm that carries the MSPM. The inset shows the MSPM under a different angle. (b) Picture of Miniaturized SPM demonstrator, where the z-stage, cantilever holder, approach motor, and the PCB with quadrant cell for the OBD can be seen.

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Editorial

New Muscle Behind a Promising HVM Solution

Douglas J. Resnick, Canon Nanotechnologies Inc.

Three decades ago, as our industry transitioned from 1X to 4X (or 5X) projection reduction steppers, photomask technologists went on a "mask maker's holiday". With no pressure on mask feature size, binary chrome-on-glass masks ruled the day, and did so for almost two decades. With the recent requirements of phase shifting and computational approaches, the holiday has long since ended (and if asked, I'm sure many in the mask industry would ask when their holiday actually occurred).

In many respects, lithography went on a similar holiday, as DUV steppers gave way first to 193nm scanners, and were then followed by the introduction of a little water to drive up the numerical aperture and extend imaging down to half pitches as small as 40nm. Along the way, the cost per gate continued to drop, and all was well for semiconductor device manufacturers.

This euphoria came to an end recently however, caused in part, by the delayed insertion of EUVL and the resulting need to adopt density multiplication processes such as self-aligned double patterning (SADP). While the march to smaller and smaller pitches was enabled, lithography costs continued their rise and the cost/gate trend reversed at the 20nm node (See for example, International Business Strategies, 2013).

Because half pitches for NAND Flash memory now call for even more expensive self-aligned-quadruple-patterning, and logic devices now rely on multiple patterning techniques, the upward trend in cost per gate is likely to continue. These types of one dimensional patterning processes necessarily induce severe design rule restrictions, which although successfully implemented in NAND Flash and logic designs, are not easily extensible to DRAM layouts.

There are of course alternative means for addressing both scaling and cost, most notably 3-D integrated circuits. By stacking 2-D chips and connecting them vertically, it is possible to pack more functionality into the same space, improve yield and reduce cost. While promising, several issues associated with a through silicon via performance and their interactions with interconnects still need to be resolved.

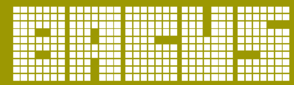
According to the ITRS Lithography Roadmap, EUVL is the leading technology designed to stop the rising costs and enable a scalable direct patterning solution. The reality, however, is that the technology is already several nodes late, and is not expected by most folks to be ready before the 7nm node. Given the improvements still required in source power, accompanied by the likely requirements of a new resist platform, it seems doubtful that EUVL can be introduced without some accompanying pattern densification scheme which does little to sidetrack cost pressures.

The gauntlet that is imprint lithography, has long been carried by a small start-up company, Molecular Imprints Inc. (MII). Extensibility has been demonstrated many times over, and has been accompanied over the years, by continued improvements in mask technology (thanks largely to DNP), throughput, overlay and defectivity. Progress, however, as a result of being a small company, was not fast enough to intersect the lithography roadmap.

In February 2014, Canon announced its intention to acquire Molecular Imprints' semiconductor business. The acquisition was finalized in April, and the folks at MII involved in semiconductor development now became part of Canon Nanotechnologies (while those working on emerging markets at MII became part of a new spin out, which retained the name Molecular Imprints).

The strategy behind the acquisition is straightforward: leverage the strengths of two separate organizations, take advantage of the resources now available to accelerate learning and quickly insert the technology into High Volume Manufacturing using a clustered module approach. Given the redundancy that is built into the NAND Flash designs, the initial market focus is non-volatile memory. The technology is easily extended to DRAM and actually offers a direct patterning solution especially for levels that do not easily lend themselves to spacer patterning processes.

As imprint outstanding issues are addressed and device scaling continues (as it inevitably will), a direct patterning solution offers great value to the industry, no matter what node is intersected. So pay attention! It's guaranteed to become more interesting in the coming years.



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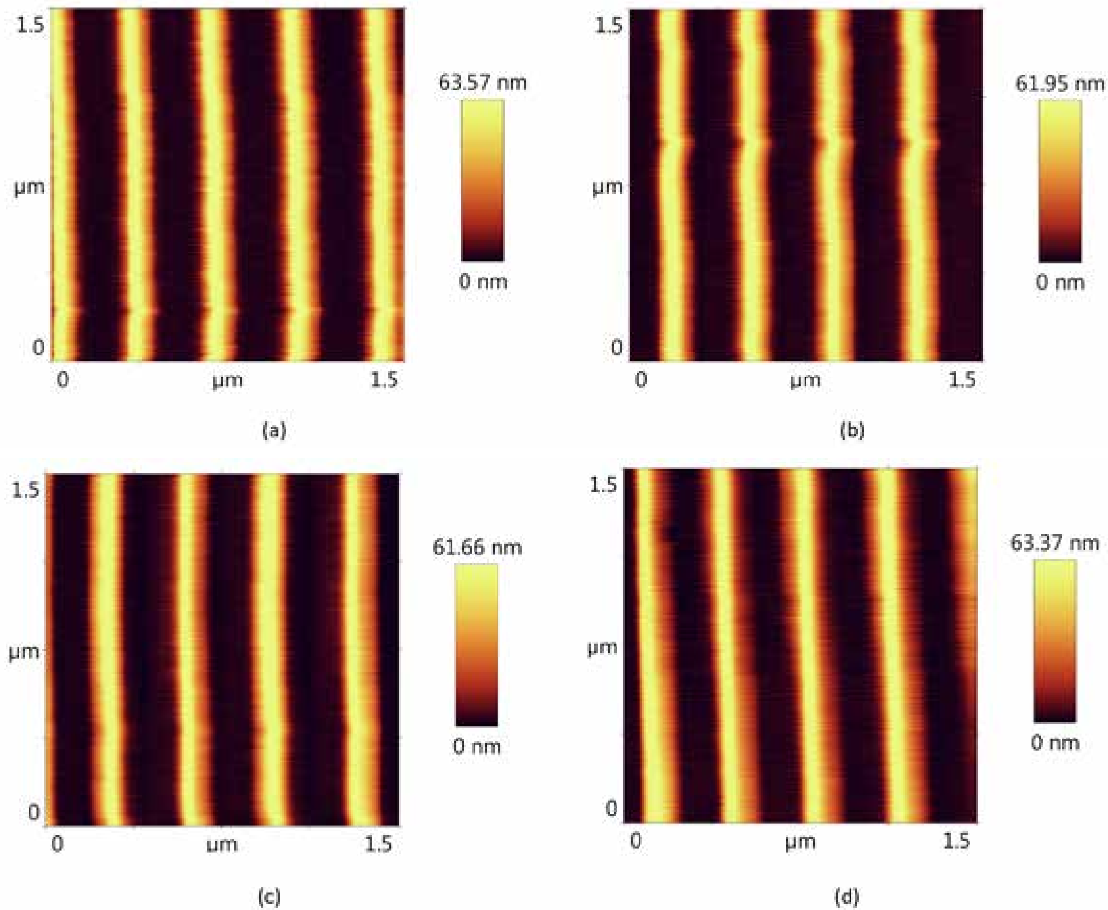

Figure 2. Scans of a dense lines pattern of TaN on a Si carrier wafer, 1.5x1.5 micrometer, 512x512 pixels, 350 nm pitch using an Olympus OMCL-AC55TS-R3 probe (1.976 MHz resonance frequency). (a) 10 lines/s. (b) 20 lines/s. (c) 30 lines/s. (d) 40 lines/s.

well. Previously we presented a high-throughput parallel SPM system,[3,4] here we will present new results obtained with this system that illustrate two key that advances are required for the successful deployment of this new class of systems.

1. Very fast (up to 40 lines/s) image acquisition: measurements of a dense line pattern on TiN (EUV mask) and a comparison of the image quality as function of speed.
2. A fast approach method: measurements of the scan-head approaching the sample from 0.2 mm distance in under 1.4 seconds and 1.0 mm distance in under 6 seconds.

The parallel SPM system consists of many miniaturized SPM (MSPM) heads that together can scan a relatively large sample, such as wafer or mask. Recently one such MSPM including an arm to accurately position it has been realized. A CAD drawing of the whole arm with MSPM and a photograph of the scan-head are shown in

The system has two critical sub-systems: a high speed parallel positioning unit[1] and high speed MSPM. The MSPM is a miniature scanning probe microscope (Size ~ 70Å~19Å~45 mm3) with a bandwidth of ~ 45 KHz and a vertical stroke of 2.1 µm. The Optical Beam Deflection (OBD) used for read-out of the probe has a noise floor of 15 fm/√Hz and a bandwidth of more than 3 MHz, which allows the use of ultra-high frequency cantilevers. During a scan, the MSPM remains stationary while the sample is moved on an XY stage.

2. Image Acquisition Performance

In Figure 2 scans of a dense (350 nm pitch) line pattern are shown for several different scan-speeds. The test sample consisted of 70 nm high TaN lines on top of a 50 nm Ru layer on a Si carrier wafer, a SEM picture of which can be seen in Figure 3. As can be seen, the image quality does not degrade significantly when going to higher scan-speeds. The lines in the SEM picture seem broader than in the AFM result, this is because the SEM contrast is mainly due to which material is at certain position, while AFM contrast is mainly sensitive to topography.

When we plot a cross-section of the lines (Figure 4) we see that although there is some variation in between measurements, even at 40 lines/s the system is limited to neither the slew-rate nor the bandwidth of the z-stage and feedback loop. When we calculate the maximum slew-rate in the shown measurement from the slope of the feature and the line-rate of the measurement we get a slew-rate of

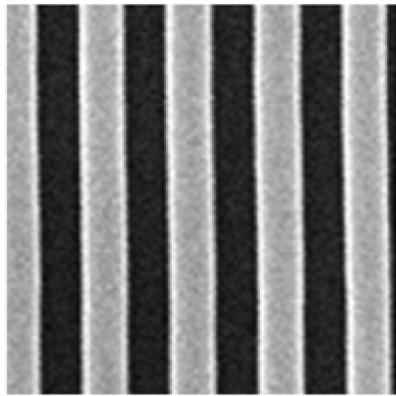

Figure 3. 1.5x1.5 μm SEM picture of the dense lines shown In Figure 2.

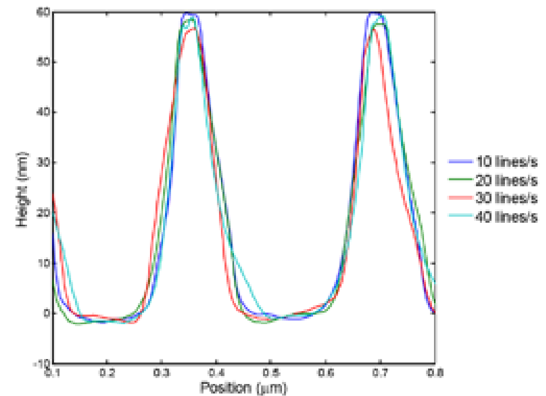

Figure 4. Detailed cross-section at 10 – 40 lines/s (from center of Figure 2). While there is some variation in the measured profile, even at 40 lines/s the system is not limited to slewrate or bandwidth of the z-stage and feedback loop

46 μm/s. This is much lower than the maximum slew rate which is determined by current output of the amplifier (100 mA), stroke of the piezo used to drive the z-stage (2.1 μm for a 150V change of input voltage) and capacitance of the piezo (60 nF): this results in a system z slew rate of (100 mA · 2.1 μm)/(150 V · 60 nF) = 23 cm/s.

The high usable (~45 kHz) bandwidth of the system is the result of the use of fast cantilevers, fast FPGA based lock-in amplifier, low noise of the OBD system, and fast z-stage of which the first resonance frequency lies above 45 kHz. This high performance of the z-actuator is due to its stiff guidance and use of counterbalance mass. Figure 5a shows the frequency response of the z-actuator. For this test, the a polytec laser vibrometer was used to measure the movement of the z-stage while sweeping the frequency of a sinewave voltage driving the z-stage's piezos. Up to 30 kHz, the frequency spectrum is virtually flat, and the first resonance peak is above 45 kHz. Figure 5b showcases the low-noise capability of the OBD; here the thermal noise peak at the first resonance frequency of a Nanoworld Arrow UHF cantilever is shown.

As can be seen, deflection noise is about 16 fm/Hz0.5, which is comparable to the values reported by Fukuma et al.[5]

3. Fast Approach Results

Apart from a high scanning speed, throughput of the parallel SPM can also be limited by the time it takes to bring the MSPM towards the sample. Since a 2.1 μm stroke of the fast z-stage is not sufficient for coarse adjustment of the distance between a sample and the cantilever, an approach stage moves the whole assembly of z-stage and OBD system in the z-direction. For this the approach motor in quick succession makes steps of about 1 μm while the z-stage is fully extended and a dither piezo drives the cantilever at a resonance frequency. If during a step of the approach motor the amplitude of the cantilever is reduced by a small amount (usually set to 15 – 35%), the z-stage quickly retracts the zstage and the fast approach is stopped, thereby preventing a crash. The system then tries to achieve the actual amplitude set-point by extending the z-stage again. If needed, at this point the system switches to a more conservative approach method where after each step of the stepper-motor the z-stage is scanned from fully retracted until the cantilever is engaged with the sample.

In Figure 6 the fast approach of the MSPM towards the sample is shown for an initial distance of 0.2 an 1.0 mm. During the majority of the approach, the cantilever is not influenced by the sample and the z-stage remains fully extended. As it comes into contact, the z-stage retracts and the approach motor stops. For about 0.1 seconds residual vibrations of the MSPM that were excited during approach are being compensated by the z-stage, after which the system stabilizes. For 0.2 mm initial distance, the system is engaged as well as fully stable in under 1.4 seconds, for 1.0 mm initial distance it takes less than 6 seconds.

4. Conclusion

We presented measurements illustrating two key advances that are required for successful high-throughput parallel SPM systems: very fast image acquisition and a very rapid approach of the sample by the scan-head. Because of low-noise (~15 fm/Hz0.5) OBD, and high (~45 kHz) bandwidth of the system image acquisition at speeds of 40 lines/s is possible with high image quality. From a distance of 1.0 mm, the system can engage and be ready for image acquisition in under 6 seconds.

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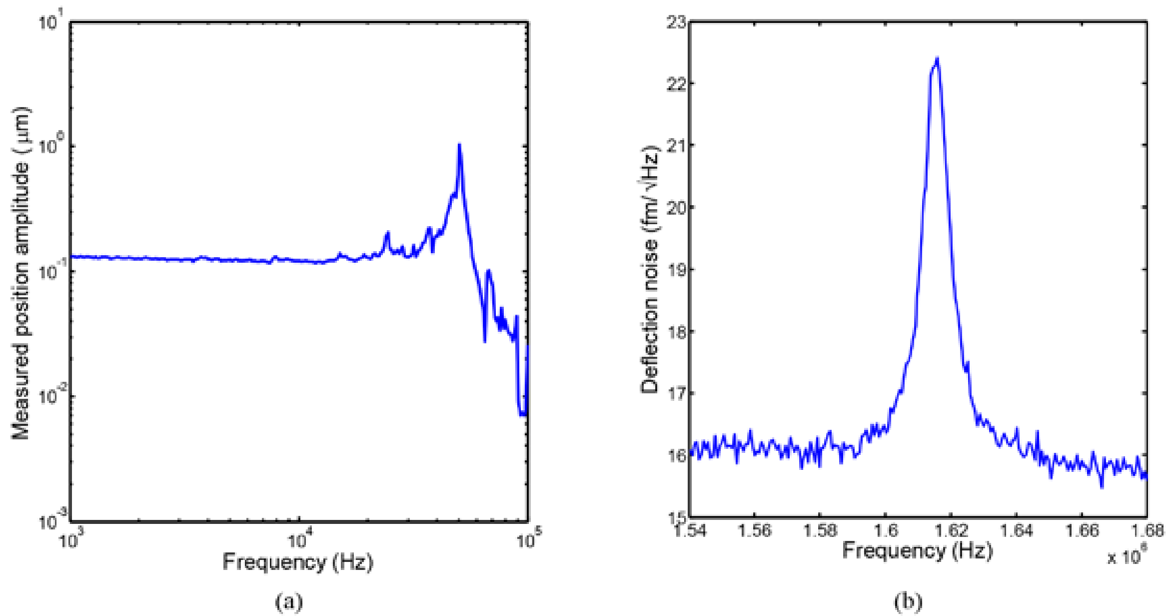

Figure 5. (a) Measured frequency spectrum of the z-scanner. (b) Measured thermal noise spectrum of a high frequency Nanoworld Arrow UHF AFM probe.

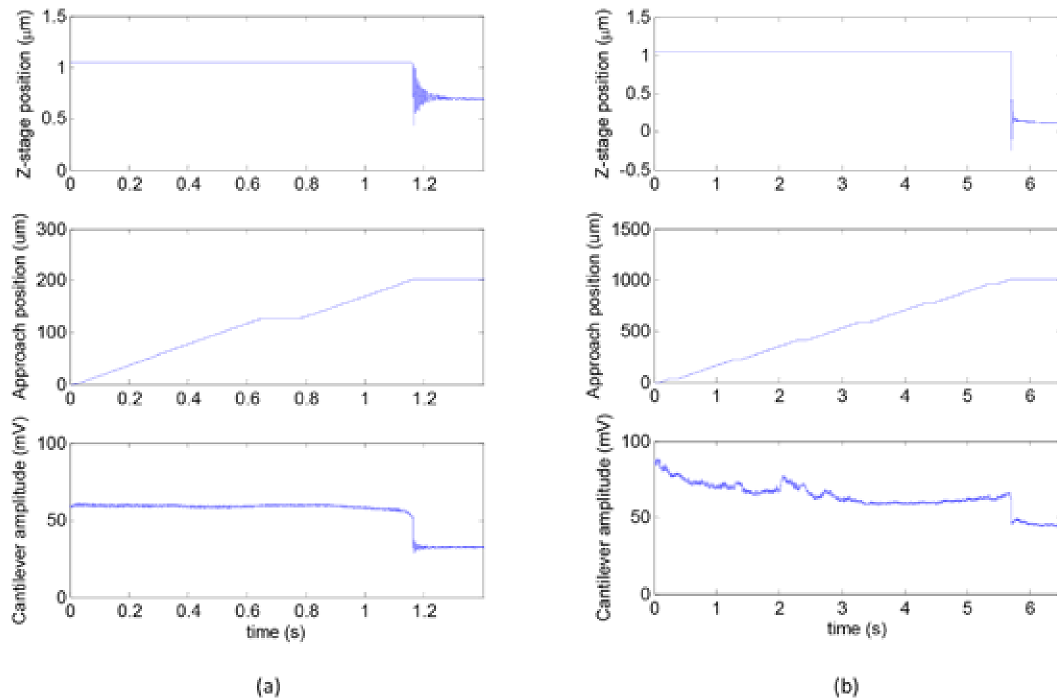

Figure 6. Fast approach of scan-head towards the sample showing position of the fast z-stage, approach motor position, and cantilever amplitude. (a) initial distance 0.2 mm. (b) initial distance 1.0 mm.

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Industry Briefs

10nm success depends on concurrent design and development

By **Tom Quan,** Deputy Director, TSMC

The Prophets of Doom greet every new process node with a chorus of dire warnings about the end of scaling, catastrophic thermal effects, parasitics run amok and . . . you know the rest. The fact that they have been wrong for decades has not diminished their enthusiasm for criticism, and we should expect to hear from them again with the move to 10nm design.

Like any advanced technology transition, 10nm will be challenging, but we need it to happen. Design and process innovation march hand in hand to fuel the remarkable progress of the worldwide electronics industry, clearly demonstrated by the evolution of mobile phones since their introduction.

To read more go to http://electroiq.com/blog/2014/09/10nm-success-depends-on-concurrent-design-and-development

Solid State Technology: Beautiful, brilliant people

By **Pete Singer,** Editor-in-Chief

It would be difficult to overstate how critical the development of a workable, high volume manufacturing EUV lithography solution is to the semiconductor industry. It is no doubt why Intel, TSMC and Samsung invested billions in ASML in 2012, and why ASML acquired Cymer in 2013.

Progress has been slower than hoped, and many are questioning if it will be ready for the 10nm generation, which is slated to go into production in late 2015/early 2016. The cover story this month looks at alternatives, including mutli e-beam and directed self-assembly.

A push to 3D devices, such as the vertical NAND, make continued scaling possible while lessening the lithography (although new challenges are created for deposition and etch technologies). The good news is that it's possible to get to 10nm and even 7nm without EUV using multi-patterning. The only question is if it will be cost effective to do so.

Earlier this year, at the SEMI Northeast Forum held in Billerica, MA, Patrick Martin, Senior Technology Director at Applied Materials described EUV as a "huge challenge" but then noted that "beautiful, brilliant people are working on this. He said "a thousand people at Cymer spend their life trying to make this work."

As moving as the argument could be, a comment from Diogenes Cicero posted right under the Editorial, refutes it, saying: Whether or not EUV is ever deployed in wafer fabs to produce ICs, it represents a catastrophic failure, surely on the scale of the SST. If we do not learn why such beautiful and brilliant people didn't devote a little more time to think about what they were doing, and why they were doing it, we are surely doomed to repeat it.

IC Insights: Process Roadmap For Memory Devices Marches On as 3D Loom

Vertical dimension to extend the life of DRAM and NAND flash as alternative memories get a closer look.

The ongoing reduction in feature sizes used to manufacture integrated circuits has enhanced memory-chip performance by increasing per-chip storage capacities, lowering power consumption, and improving the speed in which memory devices can store and retrieve data (i.e., memory bandwidth). For example, there has been a 20x improvement in the per-channel memory bandwidth of mobile DRAM over the past decade.

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