

# PHOTOMASK

BACUS—The international technical group of SPIE dedicated to the advancement of photomask technology.

Best Oral Paper - JPM13

## Improvement of EUVL mask structure with black border of etched multilayer

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### ABSTRACT

For EUVL mask with thinner absorber, it is necessary to make black border area in order to suppress the leakage of the EUV light from the adjacent exposure shots. Black border of etched multilayer is promising structure in terms of light-shield capability and mask process simplicity.

However, EUVL masks with this structure do not have electrical conductivity between the inside and the outside of black border. Inspection area including device patterns belongs to the inside of the black border. In case that quality check for EUVL masks is performed with E-beam inspection, the area is floating. As a result, electrification to mask pattern occurs and causes degradation of E-beam inspection accuracy when the mask is inspected by E-beam inspection tool.

In this paper, we refine EUVL mask structure with black border of etched multilayer in order to improve electrical conductivity. We will show evaluation results of E-beam inspection accuracy, and discuss specifications of electrically conductive black border area.

### 1. Introduction

Extremely Ultra Violet Lithography (EUVL) is the most leading lithographic technology used to fabricate 1x nm node devices. Typical EUVL mask structure is shown at Fig.1. It is stacked structure, Ta-based absorber, Ruthenium capping layer, and Molybdenum / Silicon multilayer on the Low Temperature Expansion (LTE) Substrate. And it also has backside Chromium-based layer to be fixed at EUVL tools. The thickness of patterned absorber is very effective for lithography characteristics. Thinner absorber reduces the shadowing effect, which is the

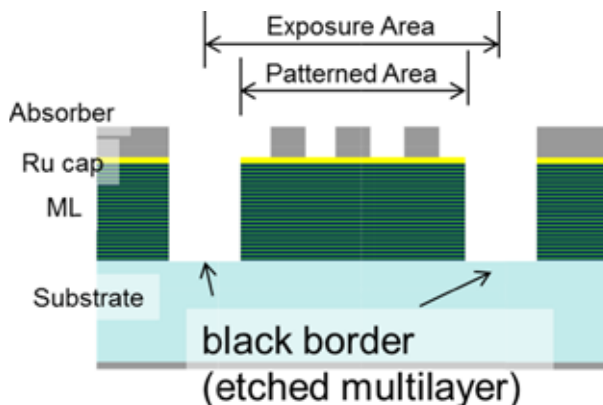


Figure 1. EUVL Mask Structure with black border.

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# EDITORIAL

## What the future holds

**Warren Montgomery, College of NanoScale Science and Engineering (CNSE)**

Depending on the timing of this article's publication, we are either attending BACUS or we are pondering the highlights of the conference. As I consider the conference, I cannot help but reflect on where we are as a lithography community. Specifically, I wonder whether EUV will finally get enough momentum to be the de facto lithography process of record, or will it simply be pushed another node?

At this point, and this should not be news to anyone, ASML has purchased Cymer and has committed an army to making the EUV source capable. If ASML is able to execute as it has with the fabulous steppers and scanners it has made over the years, then lithography may be able to continue until some of us "call it a career."

However, the scanner is not the only issue with EUV adoption, as we know; one also has to consider the state of the photomask toolsets and the photoresist. Considering photomask first, tools needed for patterned and un-patterned mask inspection need to be developed to address a killer issue: mask defects, especially in this new world without pellicles. Companies are investigating and developing approaches to avoid defects and to measure them with the existing tool sets; for example, printing wafers and using wafer inspection tools to find the defects. But is it cost effective? I am certain that companies that have a captive mask shop also have an in-house "solution" that they will implement when the time comes. One must also point out that there is a major initiative to enable EUV mask inspection called SEMATECH's EUVL Mask Infrastructure Partnership (EMI) at the SUNY College of Nanoscale Science and Engineering (CNSE) in Albany, New York. The EMI program was created to fill an industry need considered too costly for individual companies to develop independently: that is, a consortium solution.

Perhaps under the radar to this audience is the Resist Materials Development Center (RMDC) operated by SEMATECH, also based on the CNSE Campus, which was created to enable photoresist manufacturers to gain access to EUV exposure capability to facilitate photoresist development in time for EUV introduction. Photoresist makers utilize the vast EUV exposure capability resident at CNSE and SEMATECH to do research directed toward EUV photoproducts. Photoresist makers have seen a paradigm shift take place with EUV's potential introduction. Specifically, photoresist makers are no longer willing to foot the cost of having a scanner in house to develop, quality control test, and troubleshoot photoresist, developer, and bottom anti-reflective (BARC) products. The cost of operating a facility and this exposure tooling is simply too high. In prior years, an investment in an exposure system would allow photoresist testing for multiple lithography nodes; thus, photoresist makers recouped their investment. This is no longer the case since the transition to immersion lithography. Many of the companies that purchased a "dry" 193nm exposure system with, for instance, 150nm resolution found they would need another tool to reach 65nm. Now, the technology has moved to double/multiple patterning techniques which require yet another system with tighter overlay capability. One or two technology nodes, necessitating the purchase of three very expensive exposure systems, has forced at least one company to exit the photoresist business.

It seems to me that the consortium model is the only approach that will support photoresist manufacturing at a reasonable cost. The current EUV exposure tools cost almost three times as much as the typical immersion system, and that cost does not take into account support equipment, floor space, lower throughput and operating costs. It is clear that some photoresist makers believe they can address the exposure needs by working closely with their best customers. But will they be able to share the learning obtained with other customers? Will all the current photoresist makers have a place to leverage for EUV exposures? When the device maker receives an order for a prototype design that might require EUV imaging, will they remain as generous with their exposure tooling?

I will not go into a lot of detail about the resist outgassing issue associated with moving from air/water between the scanner lens to the vacuum EUV tool environment, but I think it has to be mentioned. Photoresist outgassing has basically created an industry focused on making high throughput, ASML-approved tools to enable resist outgassing testing in an effort to protect the new EUV scanners' mirrors.

The quest for EUV has kept our industry interesting. I am looking forward to hearing what comes out of BACUS (September) and then Advanced Lithography (February) regarding EUV.

Equally important in any EUV discussion is the key question: will Vivek Bakshi, President, EUV Litho Inc., Austin, Texas get the Lotus from the gentleman scientist and litho guru Chris Mack?

<http://spectrum.ieee.org/tech-talk/semiconductors/devices/i-believe-in-euvl-i-do-i-do>

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Table 1. Comparison with mask structures.

	Conventional	Bridge	CL
Schematic View			
Merit	Ready	No changes of mask blank	No changes of black border design
Demerit	-Degradation of E-Beam tool's accuracy -Particle adhesion	Wafer CD change at bridge of neighboring shot	Complex blank structure

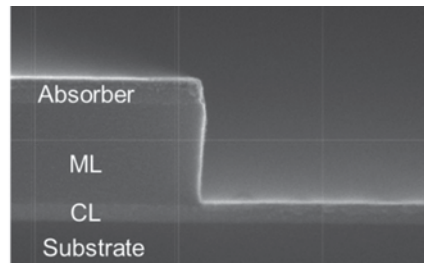
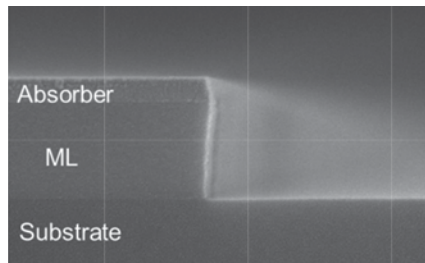


Figure 2. X-SEM images of etched multilayer.

difference of horizontal—vertical CD of printed wafer. However, thinner absorber also reduced light shielding performance, Presently, almost all EUVL masks are used with 50nm to 70nm thick absorber. The reflectivity of EUV light will be about a few percent. At EUVL process, the partial area of printed pattern is exposed by not only intentional shot but also neighboring shot and the CD of this area is changed because of poor shading capability. To avoid this effect, it is suggested that EUVL mask structure with multilayer etched black border.<sup>[1]</sup> It is promising structure in terms of light-shield capability and mask process simplicity. Black border process is ready.<sup>[2]</sup>

However, EUVL masks with this structure do not have electrical conductivity between the inside and the outside of black border, the inside area is floating. It causes degradation of E-beam inspection accuracy when the mask is inspected by E-beam inspection tool. On the other hand, EUVL masks are exposed by EUV light and electrons arise by photoelectric effect at EUVL process. It may cause the adhesion of particles in EUVL tool.

In order to assure the quality of EUVL masks by EB-based tool, sidewall measurement and defect inspection are carried out. At early phase of manufacturing without EUV-AIMS, Lithography simulation technology with 3D mask image is used for repaired pattern assurance. To evaluate 3D image of EUVL mask, Mask SEM with T-MOL is used that top-view and tilted SEM images are obtained and sidewall angle of absorber is calculated.<sup>[3]</sup> On the other hand, defect inspection for EUVL

masks needs higher inspection sensitivity than DUV masks. EB inspection will be main channel for hp 1x. Model EBEYE-M is used for defect inspection.<sup>[4]</sup>

In actual case, when Mask SEM with T-MOL observes EUVL mask with multilayer etched black border, image drifting occurs due to charging effect. Moreover, Model EBEYE-M evaluates EUVL mask with ML etched black border. But inspection image is too dark to inspect with suitable sensitivity. These issues are induced by electrically separated structure. To clear up them, refined structure of EUVL mask is needed.

## 2. Proposal of improved mask structure

In order to improve conductivity between inside and outside of black border, we propose two types of mask structure. Table 1 shows conventional type and two proposed types; bridge type and CL type.

Bridge type is that absorber and multilayer are not etched at a partial region of black border like bridge. This type doesn't need any changes of mask blank and process. Only black border design is changed. But at this type, printed wafer CD will be changed at the bridge position of neighboring shot. So when we use this type, we need to consider a countermeasure against CD change at bridge position.

CL type is also proposed. CL means conductive layer, and at this type, conductive layer is inserted between multilayer and substrate. This type needs so complex blank structure. However unlike bridge type, this type needs no changes of

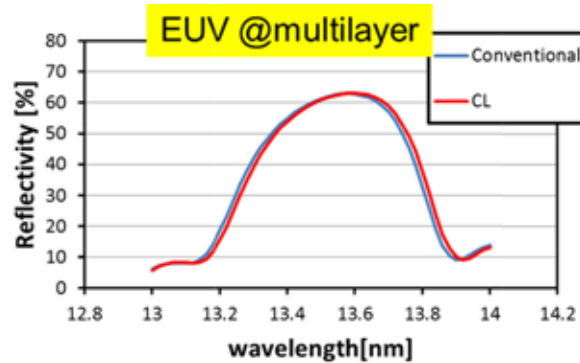


Figure 3. EUV reflectivity at multilayer.

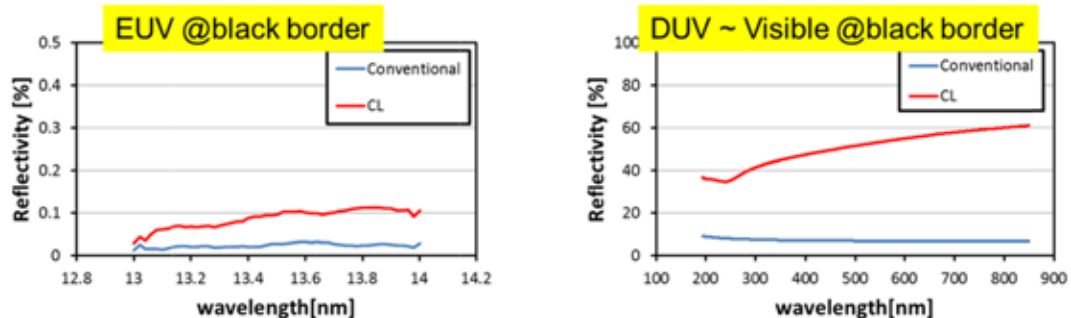


Figure 4. EUV/DUV-Visible reflectivity at black border.

black border design and has no CD changing points.

### 3. Basic characteristics

CL-type blank structure is not evaluated enough. So firstly, we evaluate basic characteristics of CL type blanks: black border process, reflectivity for EUV and DUV, and surface roughness.

#### 3.1 Black border process

Black border process is carried out by AREA™ (Shibaura Mechatronics). If conductive layer is also etched during black border process, the conductivity will be lost. Fig.2 shows the cross section images of processed each CL type and conventional blank. It looks that the thickness of conductive layer does almost not decrease after black border process, so conductive layer works as a good etching stopper.

#### 3.2 EUV/DUV reflectivity

Fig.3 shows the reflectivity of EUV light at ruthenium surface on multilayer. Mean peak reflectivity of CL-type is almost the same as conventional and acceptable.

Fig.4 shows the reflectivity of EUV and DUV to visible wavelength at black border. At EUV wavelength, CL type is slightly higher than conventional, but the value of reflectivity is very small and acceptable for black border. DUV reflectivity increases by inserting CL. However, DUV light from the light source will be blocked at HVM of EUVL. It may not be a serious problem.

### 3.3 Surface roughness

Large surface roughness causes degradation of LWR of printed wafer CD. Thus, it is very important property for EUVL mask. Surface roughness is evaluated AFM. Fig.5 shows ruthenium surface images compared with conventional CL-type blank. The difference of surface roughness rms value is only 8pm. These values are very small.

### 4. EB-based measurement/inspection performance

Already noted above, sidewall angle measurement and defect inspection are carried out for quality assurance of EUVL masks by E-beam.

#### 4.1 Sidewall angle measurement

Fig.6 shows pattern images of mask SEM with T-MOL compared between each type EUVL mask.

It is already shown that image drifting occurs at conventional type. However, clear images are obtained at both bridge and CL type EUVL mask. Image drifting is improved with conductive structures.

And we evaluate about repeatability of sidewall angle measurement. Fig.7 shows static repeatability versus distance from black border.

At conventional type, measurement was impossible. So there are not plots of conventional type. However at both bridge and CL type, measurement is possible with good repeatability.

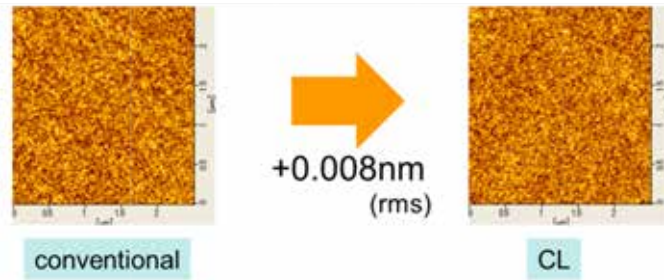


Figure 5. Surface roughness of each blank.

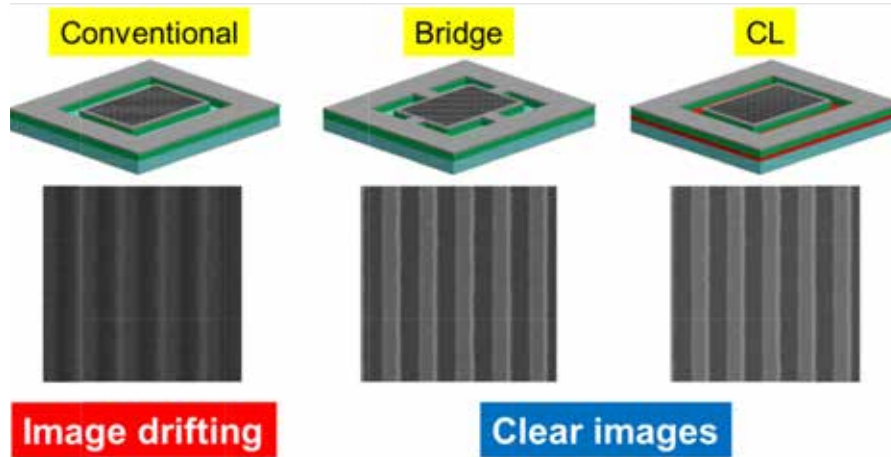


Figure 6. Images of mask SEM with T-MOL.

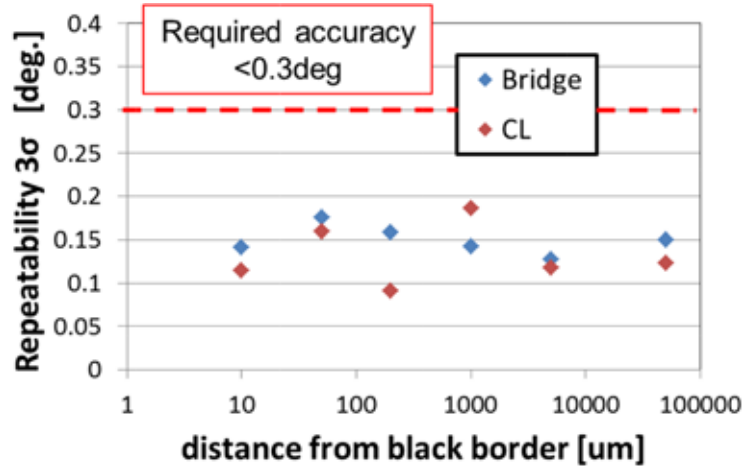


Figure 7. Static repeatability of sidewall angle measurement.

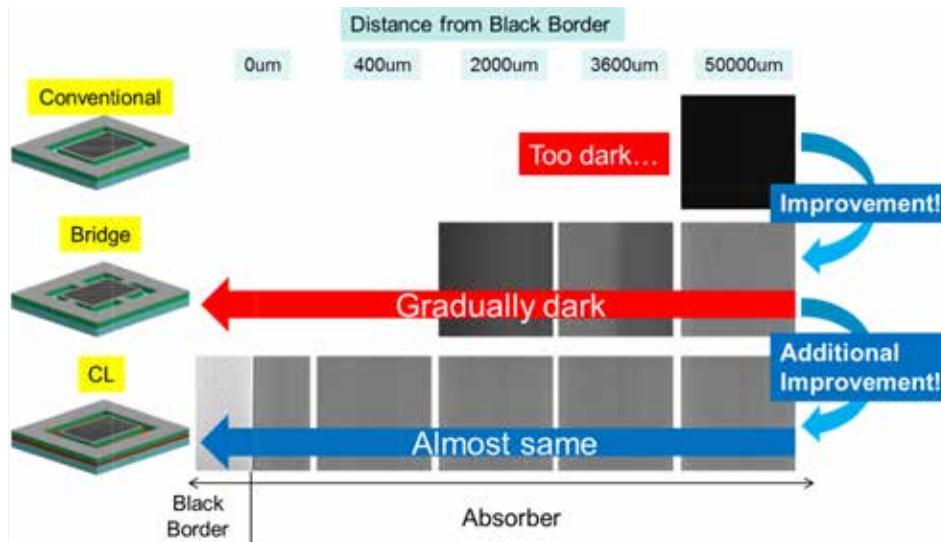


Figure 8. Inspection images of modes EBEYE-M.

#### 4.2 Defect inspection

Fig.8 shows inspection images of Model EBEYE-M for defect inspection. It already shows that inspection image is too dark to inspect at conventional type. At bridge type, we can obtain brighter image than conventional. It is improve by changing to conductive structure. But the images gradually darken as the evaluated position comes close to black border. It caused degradation of inspection sensitivity. However, at CL type, there is same image brightness from center to edge of patterned area. Thus, only CL type can be inspected with suitable sensitivity at all patterned area.

#### 5. Summary

In this paper, we proposed and evaluated refined EUVL mask structures to improve electrical conductivity between inside and outside of black border.

Conventional type cannot be measured and inspected by EB-based QA tools. At bridge type, sidewall angle can be measured, but defect inspection is unable. Thus, bridge type can be used for hp 2x while EUVL masks are inspected by optical inspection tool and qualified by 3D-SEM and Lithography simulation, although it needs countermeasures for printed wafer CD change at bridge of neighboring shot.

CL type is necessary for hp 1x when Model EBEYE-M is used as defect inspection tool. However, CL type has large DUV reflectivity and slightly larger surface roughness than conventional so we have to evaluate wafer-printing process with CL type EUVL mask.

#### 6. Acknowledgment

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# Industry Briefs

## ■ SEMI Reports Second Quarter 2013 Worldwide Semiconductor Equipment Figures; Billings US\$ 7.55B

SEMI reported that worldwide semiconductor mfg equipment billings reached US\$ 7.55B in Q2/13. The billings figure is 3% higher than Q1/13 and 27% lower than the same quarter a year ago. The data is gathered jointly with the Semiconductor Equipment Association of Japan (SEAJ) from over 100 global equipment companies on a monthly basis. Worldwide equipment bookings were \$9.17B in Q2/13, 5% lower than the same quarter a year ago and 18% higher than the figure for Q1/13. Most of the regions report a drop in the equipment spending ranging from -5 % (Japan) to -53% (Korea). The exception was China, reporting equipment spending growth of 32%.

## ■ ASML Lands Rising EUV Equipment Orders; Looking to Expand Capacity

### Digitimes

ASML's new EUV system, the NXE:3300B, has obtained 18 orders. In order to meet customer demand, the vendor is looking to boost its production capacity for EUV tools. ASML indicated that acquiring Cymer will help accelerate the development of the company's EUV equipment. ASML expects to deliver a 250W source for its EUV machines in 2015, and produce 125 WPH. By end of 2013, ASML's EUV machines will come with an 80W source and enable a throughput of 58 WPH, the firm disclosed. ASML is now capable of delivering a 55W source for its EUV systems. A 55W source translates to an EUV throughput of 43 WPH. Industry watchers generally believe that 10nm FinFET will be the first process for which chipmakers hope to switch to EUV. EUV tools can be utilized for both 12 and 18 inch wafers, and the watchers expect mass production of EUV for 18 inch wafers to kick off in 2018.

## ■ TSMC 12-inch Fabs Running at 75-80% of Capacity

### Digitimes

The capacity utilization rates of 12-inch fabs at TSMC have dropped to 75-80% recently as slow demand for high-end smartphones in the global market has resulted in reduced chip orders, according to sources. The current stage of capacity ramps for 28nm process at TSMC has come to an end, driving down the capacity utilization rates of the 28nm lines at the foundry houses, sources noted. While TSMC is believed to have continued building up the capacity for its 20nm process, volume production of the 20nm process is not expected to come until 2014, sources contended. TSMC is expected to see its capacity utilization continue sliding in Q4/13 when IC vendors begin to step up efforts to adjust their inventory levels, sources noted.

## ■ GlobalFoundries Triples Tax Credits in NY

### Adam Sicho

GlobalFoundries Inc. has doubled the incentives it can receive from New York state taxpayers committed back in 2006, in exchange for a computer-chip manufacturing plant that is now located in the town of Malta. The factory and its outgrowth drive a 20 percent increase in the area's average manufacturing wage since 2009. GlobalFoundries has grown far beyond initial projections, enabling the company to triple its pile of potential tax credits, from \$600 million in the original agreement to \$1.76 billion at present. The latest boost of tax credits stems from a new research center GlobalFoundries is building on the same site as its computer-chip manufacturing plant. This spring, the company began building a \$2.1 billion "technology development center," expecting roughly 1,000 jobs to be created. As a result, the company gained access to more tax credits, worth up to \$455 million. In all, GlobalFoundries is now in line to receive \$2.42 billion from the state effectively doubling the original package of \$1.25 billion of grants and tax credits, which was a record even back then. In addition, GlobalFoundries has received \$813 million in breaks from the Saratoga County Industrial Development Agency, primarily from sales taxes.

GF employed 2,100 employees at the start of this year. Another 1,000 or so are expected by the end of next year. The company's capital spending to-date is about \$8.5 billion. GlobalFoundries, a spinoff of Advanced Micro Devices Inc., is owned by the government of Abu Dhabi in the United Arab Emirates.

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The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

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