PHOTOMASK

BACUS—The international technical group of SPIE dedicated to the advancement of photomask technology.

BACUS
N • E • W • S

OCTOBER 2012
VOLUME 28, ISSUE 10

Photomask Japan 2012
Best Oral Paper Award

A study of closed-loop application for logic patterning

Hidemichi Imai, Shingo Yoshikawa, and Hideyoshi Takamizawa, Dai Nippon Printing Co., Ltd. (Japan), 2-2-1 Fukuoka, Fujimino-shi, Saitama 356-8507, Japan

Bertrand Le-Gratiet, Alice Pelletier, and Frank Sundermann, STMicroelectronics, Crolles (France)

Ute Buttgereit, Thomas Trautzsch, and Thomas Thaler, Carl Zeiss SMS GmbH (Germany)

Erez Graitzerd, Carl Zeiss SMS Ltd. (Israel)

ABSTRACT

Optical lithography stays at 193nm with a numerical aperture of 1.35 for several more years before moving to EUV lithography. Utilization of 193nm lithography for 45nm and beyond forces the mask shop to produce complex mask designs and tighter lithography specifications which in turn make process control more important than ever. High yield with regards to chip production requires accurate process control.

Critical Dimension Uniformity (CDU) is one of the key parameters necessary to assure good performance and reliable functionality of any integrated circuit. There are different contributors which impact the total wafer CDU, mask CD uniformity, resist process, scanner and lens fingerprint, wafer topography, etc.

In this paper, the wafer level CD metrology tool WLCD of Carl Zeiss SMS is utilized for CDU measurements in conjunction with the CDC tool from Carl Zeiss SMS which provides CD uniformity correction. The WLCD measures CD based on proven aerial imaging technology. The CDC utilizes an ultrafast femto-second laser to write intra-volume shading elements (Shade-In ElementsTM) inside the bulk material of the mask. By adjusting the density of the shading elements, the light transmission through the mask is locally changed in a manner that improves wafer CDU when the corrected

Continues on page 3.

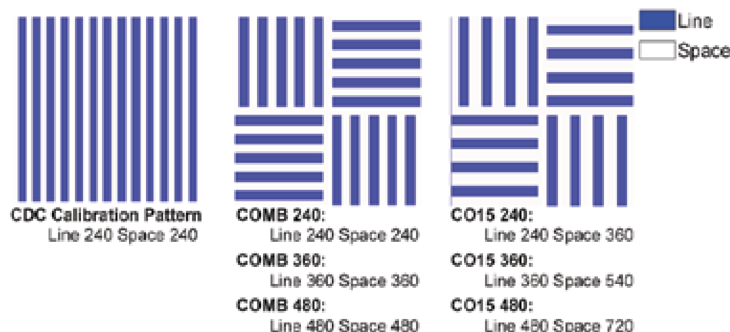

Figure 1. Pattern types over the mask.

PHOTOMASK 2012 AWARDS
—see page 3

TAKE A LOOK INSIDE:

INDUSTRY BRIEFS
—see page 11

CALENDAR
For a list of meetings
—see page 13

Editorial

A 40-year Perspective

Ken Rygler, Rygler and Associates, Inc.

First, a hello to my many friends and colleagues in the photomask industry. For personal reasons, I have had to excuse myself from my heretofore regular participation in BACUS, SPIE, Semicon, ISS, etc for the past two years. Perhaps the only virtue of a personal crisis is the perspective it brings, and how it seems to reduce the seemingly intractable challenges we face in this industry, to rather pedestrian status.

To try to "catch up", I read the last dozen BACUS newsletter editorials which also caused me to reflect on the last 25+ years I've spent in the photomask industry and the 40+ years in the microelectronics food chain.

I won't bore you with how I persuaded DuPont to enter the photomask business in 1986 but it actually seemed like a good idea at the time. Improved EDA tools and workstations were driving the ASIC business, and mask volume. Maskmaking capital intensity was increasing by an order of magnitude, principally driven by the shift from optical to e-beam pattern generation. Smaller, local maskmakers (which second-sourced the then mostly captive [80/20, captive/merchant]) would have difficulty raising enough capital. And the captives (IDMs today) were facing significant capital demands in their core semiconductor design and manufacturing business, leaving less for maskmaking equipment. Globalization was beginning to become a force to be reckoned with, yet no global maskmakers existed. And, as always, maskmaking was becoming increasingly complex: the "5X holiday" was ending, requiring increasing investments in R&D. In sum, it looked like a golden opportunity for DuPont, which was trying to expand its footprint in the electronics industry.

When we decided to take DuPont Photomasks public in 1996, Wall Street seemed to agree with our hypotheses, and we watched the stock price quintuple from its IPO price in 2 years. Within four years, the stock price returned to the IPO price as the many challenges facing merchant photomask producers were made manifest. Despite a massive captive to merchant shift (20/80, captive/merchant) and consolidation, profitability remained elusive. Rising design costs torpedoed the ASIC market. Pellicles extended mask life, reducing backups and repeats. The cost of e-beams and inspection tools skyrocketed, while OPC and PSM drove up write and inspection times and material costs. Foundries with internal mask operations reduced the merchant TAM. The captive to merchant trend began to reverse (e.g. Micron), further reducing the merchant TAM.

So, what have we learned and will those lessons help us with today's challenges? First, everything (except maybe us) lives far longer than most everyone expects. I recently won a wager made 5 years ago with a technologist far more knowledgeable than I, regarding what lithography technology will be used at 22nm. He took EUV, I took optical. Lesson: don't bet against optical. Despite the industry's fast pace, semiconductor engineers are incredibly resistant to change and I have seen numerous examples of new products and technologies with seemingly compelling economic or technical arguments, fail to unseat an incumbent. Incumbency and adequacy are powerful competitors and you can lose a lot of money finding that out for yourselves.

A second lesson (also related to lesson one) is "nice from far but far from nice". We've seen so many "shiny new pennies" come down the lithography road. Each would typically bring with it a fresh set of acronyms and the promise of enabling scaling the seemingly impenetrable optical lithography wall at __nanometer (readers: feel free to fill in a number). Whether hard X-ray, IPL, EBDW (a.k.a maskless), SCALPEL, soft x-ray (a.k.a EUV), etc., none have supplanted optical. Today, it's DSA, lithography in a bottle. As we got closer to each of these, a unique set of problems emerged and, at the end of the day, engineers would always prefer to deal with the devil they know. A related lesson is that changing the name of a

(continues on page 10)

BACUS

N • E • W • S

BACUS News is published monthly by SPIE for BACUS, the international technical group of SPIE dedicated to the advancement of photomask technology.

Managing Editor/Graphics Linda DeLano

Advertising Lara Miles

BACUS Technical Group Manager Pat Wight

■ **2012 BACUS Steering Committee** ■

President
Wolfgang Staud, *Applied Materials, Inc.*

Vice-President
John Whittey, *KLA-Tencor MIE Div.*

Secretary
Artur Balasinski, *Cypress Semiconductor Corp.*

Newsletter Editor
Artur Balasinski, *Cypress Semiconductor Corp.*

2012 Annual Photomask Conference Chairs
Frank E. Abboud, *Intel Corp.*
Thomas B. Faure, *IBM Corp.*

International Chair
Naoya Hayashi, *Dai Nippon Printing Co., Ltd.*

Education Chair
Artur Balasinski, *Cypress Semiconductor Corp.*

Members at Large
Paul W. Ackmann, *GLOBALFOUNDRIES Inc.*
Michael D. Archuletta, *RAVE LLC*
Uwe Behringer, *UBC Microelectronics*
Peter D. Buck, *Toppan Photomasks, Inc.*
Brian Cha, *Samsung*
Kevin Cummings, *ASML US, Inc.*
Glenn R. Dickey, *Shin-Etsu MicroSi, Inc.*
Thomas B. Faure, *IBM Corp.*
Brian J. Grenon, *Grenon Consulting*
Jon Haines, *Micron Technology Inc.*
Mark T. Jee, *HOYA Corp, USA*
Bryan S. Kasprowicz, *Photronics, Inc.*
Oliver Kienzle, *Carl Zeiss SMS GmbH*
Wilhelm Maurer, *Infineon Technologies AG*
M. Warren Montgomery, *The College of Nanoscale Science and Engineering (CNSE)*
Abbas Rastegar, *SEMATECH North*
Emmanuel Rausa, *Plasma-Therm LLC.*
Douglas J. Resnick, *Molecular Imprints, Inc.*
Steffen F. Schulze, *Mentor Graphics Corp.*
Jacek K. Tyminski, *Nikon Precision Inc.*
Larry S. Zurbrick, *Agilent Technologies, Inc.*

SPIE

P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 360 676 3290
Fax: +1 360 647 1445
SPIE.org
help@spie.org

©2012

All rights reserved.

Photomask 2012 Awards

The **2012 BACUS Prize Award**

was presented jointly to

Mr. Kevin MacLean and **Mr. Roger Sturgeon**
In recognition of their contributions in mask data preparation through the creation and commercialization of the Computer Aided Transcription System (CATS), the first universal mask data preparation platform. For much of the last three decades CATS has served as one of the primary tools in mask data preparation. CATS took mask data preparation away from designers and put it in the hands of mask manufacturers allowing translation between mask write and inspect tools as well as enabling mask pattern and jobdeck optimization to improve mask precision and reduce write time.

The **2012 BACUS Lifetime Achievement Award**

was presented to

Mr. Richard Larson
In Recognition for his Contributions to the Photomask Industry 1973 – 2008 and to Honor his actions exemplifying: Leadership by Example, Mentoring, and Operations Excellence

1st Place Best Oral Presentation

Future mask writers requirements for the sub-10nm node era, Mahesh Chandramouli, Nathan E. Wilcox, Andrew T. Sowers, Damon M. Cole, Frank E. Abboud, Intel Corp. (United States) [8522-55]

2nd Place Best Oral Presentation

Interaction of 3D mask effects and NA in EUV lithography, Jens Timo Neumann, Paul Gräupner, Johannes Ruoff, Winfried Kaiser, Reiner Garreis, Carl Zeiss SMT GmbH (Germany); Bernd Geh, Carl Zeiss SMT Inc./ASML-TDC (United States) [8522-107]

3rd Place Best Oral Presentation

EUVL mask repair: expanding options with nanomachining, Emily E. Gallagher, Gregory R. McIntyre, Mark Lawliss, IBM Corp. (United States); Tod E. Robinson, Ronald R. Bozak, Roy L. White, RAVE LLC (United States) [8522-56]

1st Place Best Poster Presentation

Effect of radiation exposure on the surface adhesion at Ru-capped MoSi multilayer blanks, Göksel Durkaya, Abbas Rastegar, Aron Cepler, Hüseyin Kurtuldu, SEMATECH North (United States) [8522-39]

2nd Place Best Poster Presentation

Impact of EUV photomask line-edge roughness on wafer prints, Zhengqing J. Qi, Emily E. Gallagher, Amy E. Zweber, IBM Corp. (United States); Yoshiyuki Negishi, Tasuku Senna, Satoshi Akutagawa, Toshio Konishi, Toppan Photomasks, Inc. (United States); Gregory R. McIntyre, IBM Corp. (United States) [8522-96]

3rd Place Best Poster Presentation

Direct dose map synthesis for raster-based multiple electron-beam systems, Amyn A. Poonawala, Synopsys, Inc. (United States); Lars H. Bomholt, Synopsys Switzerland, LLC (Switzerland)[8522-94]

The winner of the iPad (random drawing of all those who voted throughout the week) was: **Ralph Klaesges** with Carl Zeiss SMS GmbH (Germany)

iPad sponsored by

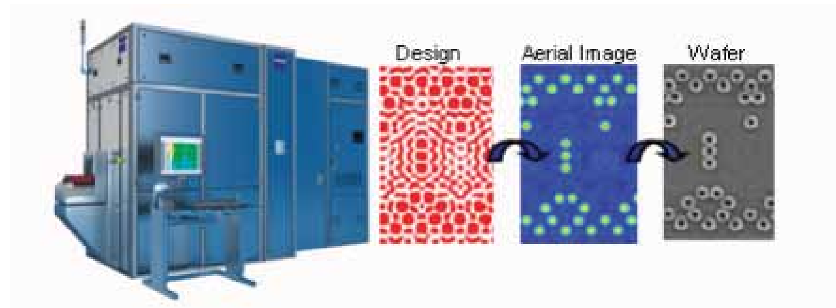

Figure 2. WLCD measures the CD on mask as it is relevant for printing, simplifying the CD measurement especially for complex mask design.

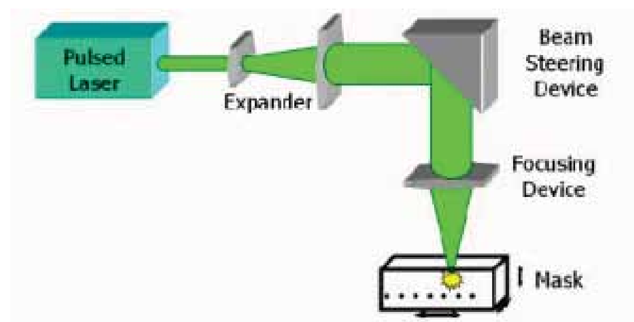

Figure 3. CDC Process: At the focal point of the laser beam a pixel is created. Quartz density is altered, and so is the local index of refraction. Each pixel acts as a scattering element.

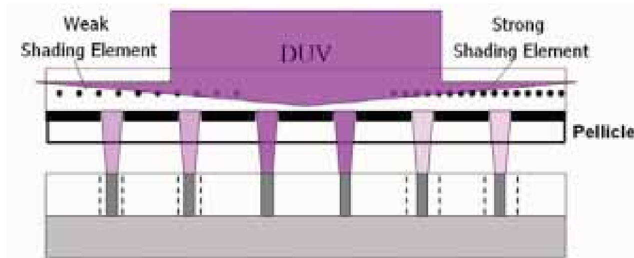

Figure 4. Applying shading elements to the mask reduces light transmission locally and effectively reduces the local dose. This causes all features to print at a CD closer to target.

mask is printed.

The objective of this study is to evaluate the usage of these two tools in a closed loop process to optimize CDU of the mask before leaving the mask shop and to ensure improved intra-field CDU at wafer level.

Mainly we present the method of operation and results for logic pattering by using these two tools.

1. Introduction

Further extension of 193nm lithography to the next technology nodes, staying at a max NA of 1.35, pushes the lithography to its utmost limits. Various techniques are required to drive the resolution to the theoretical limits. The k1 factor comes close to 0.25 which leads to a tremendously increased Mask Error Enhancement Factor (MEEF). This means that CD errors on mask are getting highly amplified on wafer. Process control becomes a key factor to success to maintain a high yield in production.

One key parameter to ensure a high and reliable functionality for any integrated circuit is the critical dimension uniformity (CDU). There are different contributors which impact the intra-field CD performance at wafer such as mask CD uniformity, scanner fingerprint, resist process etc. In the present work we focus on improvement of mask CD

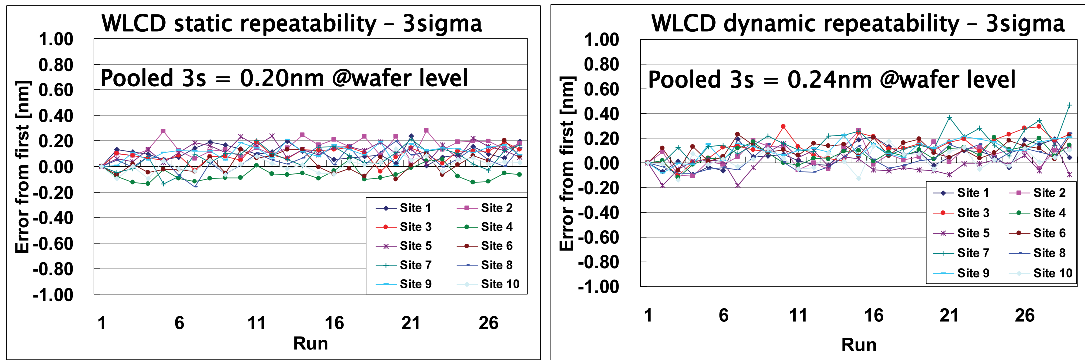

Figure 5. WLCD measurement repeatability, static and dynamic

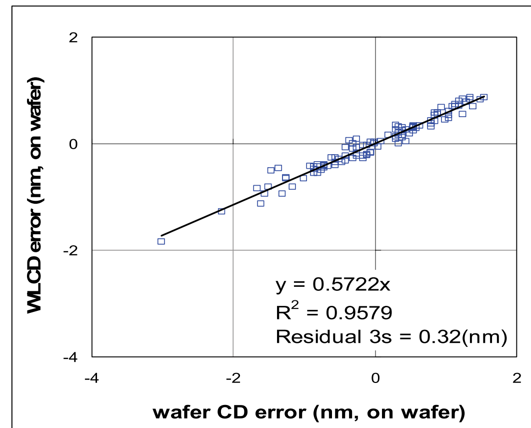

Figure 6. CD correlation between wafer data measured by scatterometry and WLCD aerial image CD.

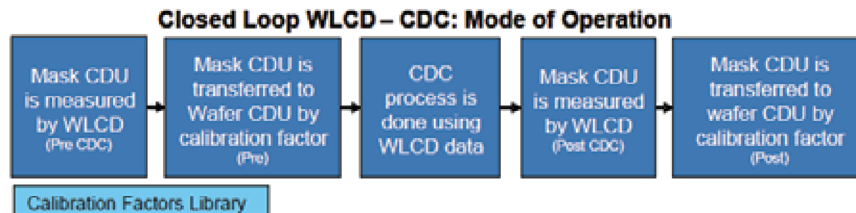

Figure 7. Operation mode for closed loop WLCD - CDC process.

signature which is one of the main contributors to intra-field CD uniformity. The mask CD uniformity has been measured by WLCD which is based on proven aerial image technology. Based on this CD input the CD uniformity was corrected by CDC32™ and afterwards verified by WLCD measurement.

We used a test mask to investigate the impact of CDC on different features performing the CDC correction based on the CDU input data of one specific reference pattern. Furthermore, we performed CD uniformity correction on production masks for 40nm node logic gate layer and 28nm logic gate layer. Additionally, we have investigated the registration impact after CDU correction.

2. Experimental Set-up

2.1 Mask description

We used line and space pattern on a ESPM6% test mask. Figure 1 shows CDC calibration pattern and 6 additional patterns.

The COMB and CO15 were measured in vertical and horizontal orientations. We used 6 pattern structures to confirm CDC correction effect for logic patterning.

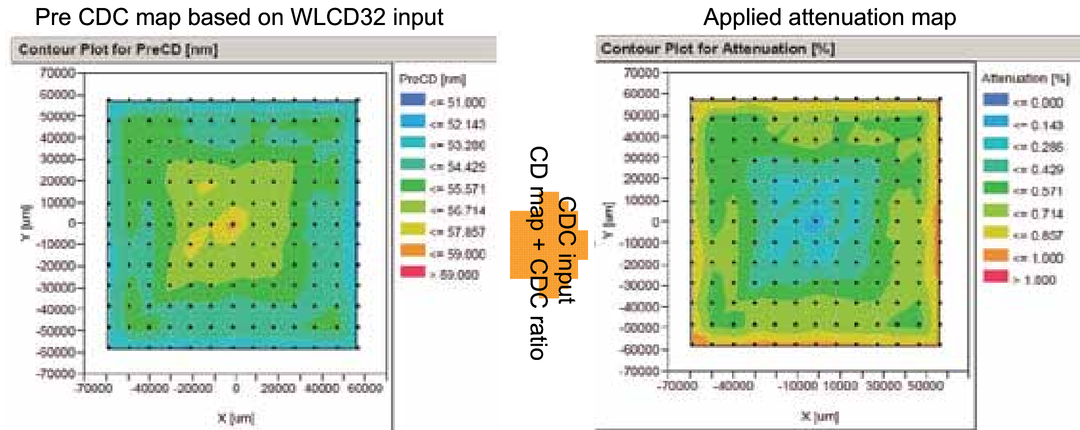

Figure 8. CD uniformity map measured by WLCD and attenuation map at CDC32™.

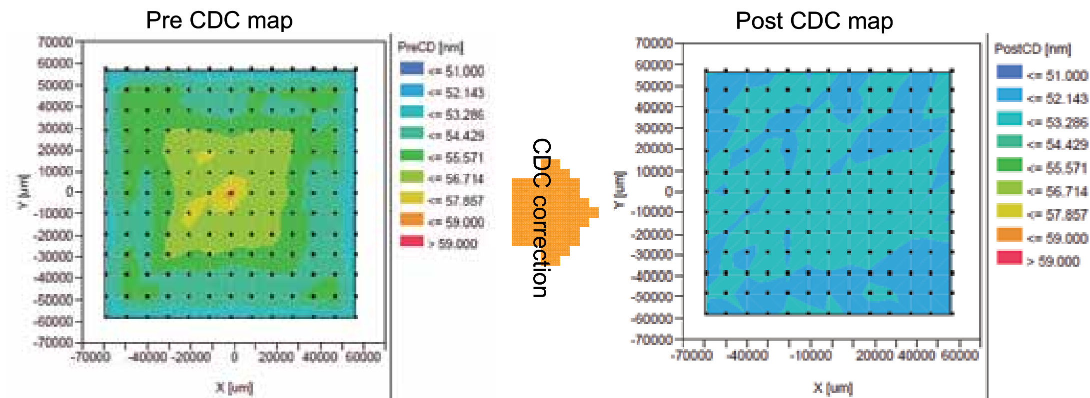

Figure 9. CD uniformity map before (left) and after (right) CDC process for calibration pattern

2.2 Mask Metrology - WLCD Aerial Image CD Measurement

Zeiss Wafer Level CD metrology system WLCD is based on proven aerial imaging technology. It measures the CD on the mask in the wafer level plane as it is relevant to printing (see Figure 2).[1, 2]

By doing that it captures optical proximity effects and optical MEEF effects induced by the scanner illumination. The use of the WLCD significantly simplifies the CD measurement especially for complex mask designs and complex 2D features.

The WLCD is equipped with new Zeiss 193nm imaging and illumination optics. The LITO™-grade optics has extremely low aberrations and comes close to the quality of the scanner optics. The variable NA allows measurements up to a scanner equivalent NA of 1.4. A new 193nm laser is used for ultra fast CD measurements of several hundred CD's per hour. The tool is equipped with two user defined aperture planes for off-axis illumination in order to illuminate the mask under the same conditions as a scanner. FreeForm illumination devices support SMO technologies.

For CD measurement the user can define several regions of interest within the field of view, which allows CD measurements on arbitrary features. The WLCD has CD repeatability below 0.25nm at wafer level.

2.3 CD Control - CDC32™

The CDC32™ process utilizes shading elements inside the mask bulk to attenuate the light during the wafer exposure. The CDC process creates small pixels that consist of QZ with a different morphology which create a slightly different refractive index (delta n). This delta n causes a small amount of scattering outside of the scanner objective pupil and hence causes attenuation.

The CDC32™ process basic set-up is described in Figure 3.

In order to improve intra-field CD uniformity, shading elements of specific attenuation level or pixel density are applied to each specific area in the mask. Figure 4 shows the relevant shading elements.

In this work we focused on the use of mask CDU data as input for the wafer intra-field CD uniformity improvement.

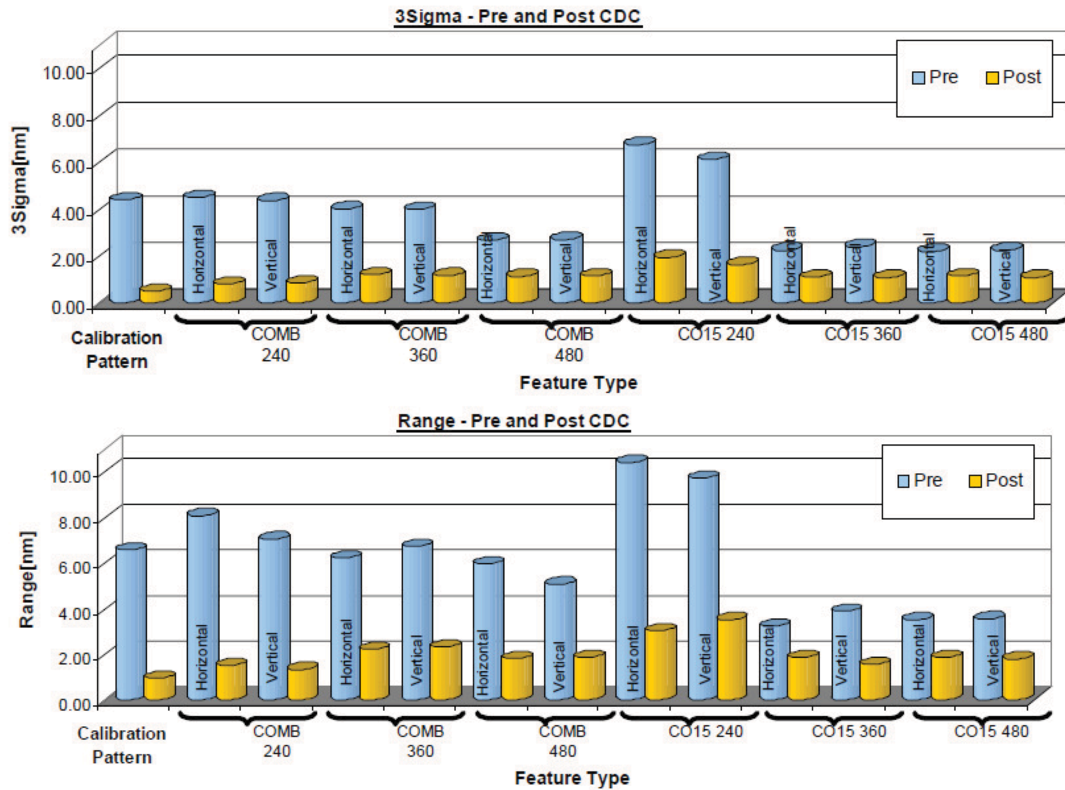

Figure 10. CD uniformity 3sigma (upper) and range (bottom) - pre and post CDC.

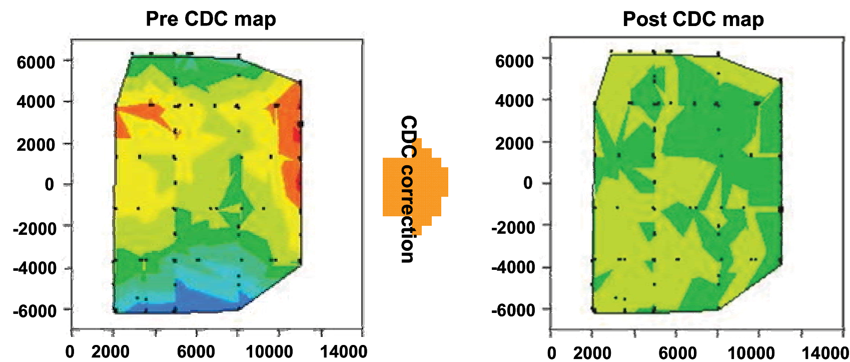

Figure 11. CD uniformity map before (left) and after (right) CDC process for 40nm logic devices.

3. WLCD Performance Confirmation Result

3.1 Measurement repeatability

We confirmed static measurement repeatability and dynamic measurement repeatability for WLCD.

We used line and space (200nm 1:1) on EPSM 6%. Measurement cycles are 30 times within one loading. Measurement sequences are as following.

- Static measurement: auto focus -> measurement just focus -> auto focus

- Dynamic measurement: auto focus -> measurement just focus -> move next die

Figure 5 shows WLCD measurement repeatability results. Static measurement repeatability pooled 3sigma is 0.20nm on wafer level and dynamic measurement repeatability pooled 3sigma is 0.24 nm on wafer level.

3.2 Wafer data - WLCD correlation

Figure 6 shows a high quality linear correlation of WLCD to wafer data. WLCD captures the CD in the aerial image plane and not in the resist. Wafer data is in the resist. For correlation result, the slope value is not 1 due to mainly resist MEEF effects.

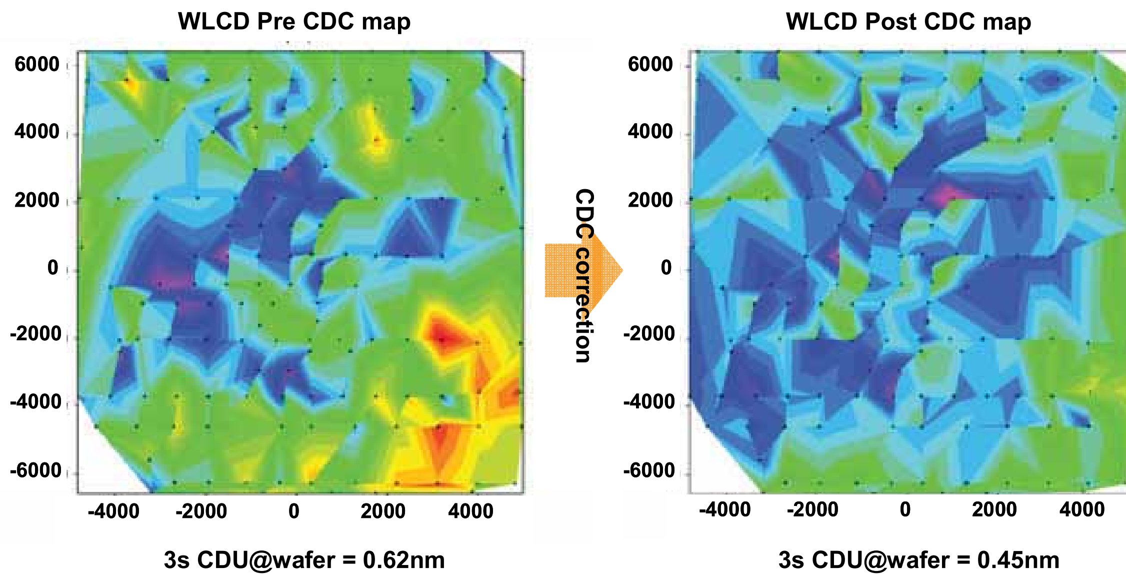

Figure 12. WLCD CD uniformity map before and after CDC process for 28nm logic device.

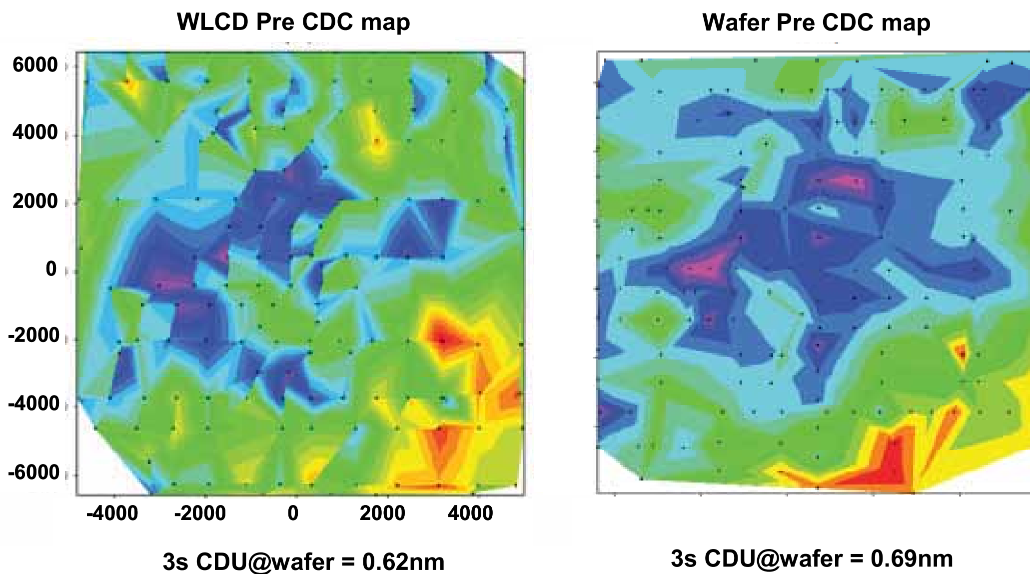

Figure 13. Comparison between WLCD and wafer CD uniformity map before CDC process.

4. CD Uniformity Improvement

The CDU tuning was performed with CDC32™ using WLCD mask metrology data as input. To maximize the intrafield CD uniformity improvement on wafer a calibration step was applied and the process was split into two steps:

- Calibration step
- CD uniformity correction step

In the calibration step the calibration factors between WLCD aerial image CD and wafer data as well as the CDC ratio, which determines the CD change as function of applied attenuation, have been derived. The derived calibration factors can be stored in a library for future process use. The CD uniformity correction step utilizes the CDC32™ based on the WLCD data scaled with the calibration factor. The closed loop WLCD/CDC32™ process flow it schematically shown in Figure 7. The complete process is described in more detail in an earlier paper.[3, 4]

The scaled CD uniformity data measured by WLCD have been used as input for the CDC32™ and the required attenuation map to flatten the CD signature was calculated

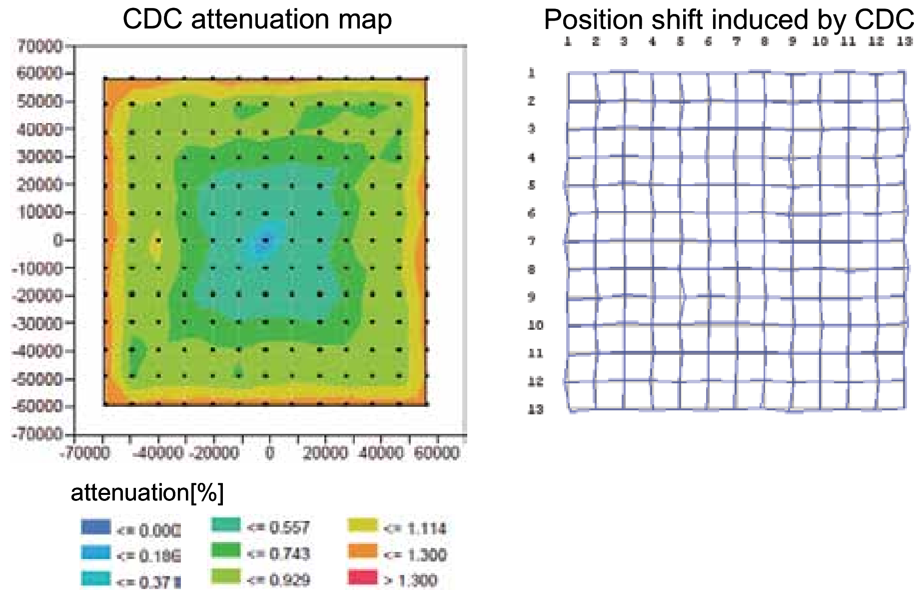

Figure 14. Attenuation map at CDC32" and position shift induced by CDC process.

and applied to the mask (see Figure 8).

Figure 9 shows that the CD uniformity was significantly reduced for calibration pattern (line and space, 240nm 1:1) applying the CDC process. The overall 3sigma uniformity was reduced from 4.37nm to 0.48nm, which is 89% improvement.

Figure 10 shows impressively that the CD uniformity was significantly reduced for all other pattern features applying the CDC process. For all pattern features, 3sigma and range of CD uniformity were significantly improved as well (up to 82% improvement) and all 3 sigma values are below 1.93nm post CDC. These results demonstrate that the CDC process is effective for CD uniformity improvement of logic patterning, which has several pattern sizes. This is a very important result.

We confirmed effect of CDC process for logic devices, namely a 40nm node and a 28nm logic gate mask. Figure 11 shows that the CD uniformity of 40nm logic gate devices was significantly reduced from 2.01nm pre CDU to 0.50nm post CDU (3sigma at wafer) by CDC process. The overall 3sigma uniformity was improved by 75%.

Figure 12 shows the CDC correction results for the 28nm logic layer for WLCD. The mask showed already a very good pre-CD uniformity of 0.62nm 3sigma at wafer level. This CDU value could be further improved by CDC application down to 0.45nm. This is an improvement of 27%.

Figure 13 shows the correlation between WLCD data and wafer data before CDC correction. The CD signature looks similar for WLCD and wafer. Unfortunately the wafer post data had not been available at the time of paper completion.

The demonstrated results show impressively that the closed loop WLCD/CDC™ is very effective for logic pattern application.

5. Position Shift by CDC Process

The CDC utilizes an ultrafast femto-second laser to write intra-volume shading elements (Shade-In ElementsTM) inside the bulk material of the mask. Then, our concern of CDC process is if it has an impact on the pattern position. We investigated the position shift for a mask where the CD uniformity 3sigma was reduced from 4.37nm to 0.48nm, which is 89% improvement. Registration measurement tool is IPRO3. Measurement repeatability 3sigma of IPRO3 is 1.3nm. Figure 14 shows CDC attenuation map and position shift induced by CDC process. Position shift residual 3sigma is below 2nm (x is 1.76nm, y is 1.17nm).

The result is measured by multi point alignment with scale and orthogonality removed. This confirms that the impact of CDC on registration is low.

6. Summary and Conclusion

In the present work we have focused on intra-field CD uniformity improvement by improving mask CD signature utilizing WLCD for mask CD metrology and CDC32™ for CD uniformity control. Furthermore, we investigated the impact of CDC on pattern position shift.

It was shown that the WLCD has a good correlation to wafer and an outstanding CD repeatability of below 0.25nm at wafer level. The WLCD provides a reliable input for CD uniformity correction and is the tool of choice to verify the CD uniformity improvement after CDC32™ treatment.

Furthermore, it was shown that the CDC32™ improves the CD uniformity significantly. This was shown on a test mask representing the pattern variety of a logic pattern. The intra-filed CD uniformity was reduced by 89% for the reference pattern. For all other pattern sizes, CD uniformity was improved as well (up to 82%).

Furthermore, a significant 3 sigma CD uniformity improvement was demonstrated on production devices for 40nm node logic gate layer as well as for the 28nm node logic gate layer.

Additionally, we confirmed that position shift residual 3sigma induced by CDC is under 2nm.

This leads to the overall conclusion, that the CD control based on the closed loop WLCD/CDC32™ is effective for logic patterning.

7. References

[1] Sven Martin, Holger Seitz, Wolfgang Degel, Ute Buttgereit, and Thomas Scherübl, "WLCD: A new System for Wafer Level CD Metrology on Photomasks", **Proc. SPIE Vol. 7272,** pp. 72722T-72722T-9 (2009).

[2] F. Dufaye, S. Gough, F. Sundermann, V. Farysa, H. Miyashita, L. Sartelli, F. Perissinotti, U. Buttgereit, S. Perlitz, and R. Birkner, "Mask phase and transmission variation effects on wafer critical dimensions for nodes 65nm and 45nm", **Proc. SPIE Vol. 7545,** 75450M (2010).

[3] Ute Buttgereit, Robert Birkner, Mark Joyner, Erez Graitzer, Avi Cohen, Hiroyuki Miyashita, Benedetta Triulzi, Alejandro Fasciszewski Zeballos, and Carmelo Romeo, "CD uniformity correction on 45-nm technology nonvolatile memory", **Proc. SPIE Vol. 7638,** 76383K (2010).

[4] Ute Buttgereit, Robert Birkner, Erez Graitzer, Avi Cohen, Benedetta Triulzi, and Carmelo Romeo, "Process Window improvement on 45 nm technology Non Volatile Memory by CD uniformity improvement", **Proc. SPIE Vol. 7823,** 78230C (2010).

EDITORIAL *(continued from page 2)*

technology doesn't make the problems easier to solve: EUV is still X-ray, maskless is still e-beam direct write.

What's in lithography's future? Who knows, but I would bet on two things: first, optical will dominate. Second, optical won't dominate to the complete exclusion of everything else. The industry will bifurcate (or trifurcate?) or segment, as we marketing people like to say. EUV (SXPL) is probably too costly and too late to have anything but a relatively limited role but it will have a role. Mulltibeam maskless (EBDW) may play a more important role in maskmaking than on silicon. Imprint lithography (full disclosure: I am a small shareholder in Molecular Imprints) could play a role in nonvolatile memory (NAND flash and/or its successors), as that market is highly elastic, and it is aggressively pursuing magnetic disk drives. Imprint is inherently inexpensive.

And, finally, what does all this mean for maskmakers, merchants in particular? As always, the challenges seem greater than ever. Most of the challenges I mentioned in the fourth paragraph remain: higher design costs and fewer ASIC/SoCs, growth of foundries with in-house mask capability, more IDMs making masks in-house, etc. In addition, the challenges of extending optical even further with exotic pixelated masks, new OPC sizes and shapes, etc., and the new lithography technologies on the horizon, will fragment maskmakers' scarce R&D and capital resources. It will take all the cleverness and ingenuity merchant maskmakers can muster to survive in this environment, let alone return the cost of capital. Yet these maskmakers are a prime example of Darwinian survival, and somehow will endure.

N • E • W • S

Sponsorship Opportunities

Sign up now for the best sponsorship opportunities

Photomask 2013 —
Contact: Lara Miles, Tel: +1 360 676 3290; laram@spie.org

Advanced Lithography 2013 —
Contact: Teresa Roles-Meier, Tel: +1 360 676 3290; teresar@spie.org

Advertise in the BACUS News!

The BACUS Newsletter is the premier publication serving the photomask industry. For information on how to advertise, contact:

Lara Miles
Tel: +1 360 676 3290
laram@spie.org

BACUS Corporate Members

Acuphase Inc.
American Coating Technologies LLC
AMETEK Precitech, Inc.
Berliner Glas KGaA Herbert Kubatz GmbH & Co.
FUJIFILM Electronic Materials U.S.A., Inc.
Gudeng Precision Industrial Co., Ltd.
Halocarbon Products
HamaTech APE GmbH & Co. KG
Hitachi High Technologies America, Inc.
JEOL USA Inc.
Mentor Graphics Corp.
Molecular Imprints, Inc.
Panavision Federal Systems, LLC
Profilocolore Srl
Raytheon ELCAN Optical Technologies
XYALIS

Industry Briefs

Global chip R&D spending on the climb

Spending on research and development by semiconductor companies worldwide is expected to grow 10 percent in 2012 to a record high of $53.4 billion, according to market analysis firm IC Insights (Scottsdale, Ariz.).

IC Insights predicts that worldwide semiconductor sales will increase 3 percent in 2012 to an annual total of $329.8 billion, up from $321.4 billion in 2011. This will put R&D spending at 16.2 percent of the total revenue.

A dozen semiconductor companies spent more than $1.0 billion each on R&D in 2011. Intel was the leader with $8.35 billion of R&D spending in 2011, approximately three times the spending of Samsung Electronics Co. Ltd.

Worldwide semiconductor spending leaders in 2011 with spending above $1 billion. Source: IC Insights

U.S. companies accounted for 57 percent of worldwide semiconductor R&D spending in 2011, followed by suppliers based in Japan at 17 percent; Europe, 10 percent; Taiwan, 8 percent; South Korea, 7 percent; and mainland China, 1 percent. Integrated Device Manufacturers (IDMs) accounted for about 66 percent of R&D spending by semiconductor companies in 2011, while fabless suppliers represented 29 percent and pure-play foundries made up the remaining 5 percent of the total.

Semiconductor R&D spending has been moving higher for three decades as the complexity of chip manufacturing and design has increased with miniaturization.

R&D spending as a percent of semiconductor sales by chip companies was typically 7 to 8 percent in the late 1970s and early 1980s. R&D-to-sales ratios grew to around 10 to 12 percent of revenues by the early 1990s and then jumped to over 15 percent during the last decade, reaching a record 17.5% in 2008, according to IC Insights.

SK Hynix joins EUV metrology research effort

DRAM and flash memory chip provider SK Hynix has joined the Sematech consortium's EMI partnership to develop metrology tools used to spot defects in advanced masks needed for extreme ultraviolet lithography.

Sematech launched the EMI (EUVL Mask Infrastructure) partnership in 2010 to tackle infrastructure gaps for EUV lithography in mask metrology. It will fund the development of new metrology tools.

In joining the group, Sungjoo Hong, head of SK Hynix's R&D division, said, "We expect to play a key role in accelerating the commercialization of EUV technology by supporting the development of critical metrology tools to enable defect free masks."

Stefan Wurm, Sematech's director of lithography, said the roll out of EUV lithography will be hastened by the development of new tools for spotting mask defects.

Sematech and equipment maker Carl Zeiss are collaborating to develop a new tool called an actinic aerial image metrology EUV system that is expected to be deployed when the advanced lithography technique reaches volume production, Sematech said.

The tool will support 16-nm half-pitch technology node requirements and beyond. It is expected to be ready for production in mid-2014.

Intel's Bohr sees path to 10-nm chips

Intel Corp. has found a way to create a 10-nm process technology using immersion lithography. In addition, the processor giant is on track to start making chips in a 14-nm process technology before the end of next year, an Intel fellow said in a talk here.

The 10-nm process would debut in 2015 or later. It would require quadruple patterning for some mask layers but "it's still economical," said Mark Bohr, director of Intel's technology and manufacturing group, speaking to EE Times after a talk at the Intel Developer Forum here.

Bohr did not reveal details of either Intel's 14- or 10-nm process plans. His comments focused only on technical feasibility.

The company has long worked to develop extreme ultraviolet (EUV) lithography and recently agreed to invest $4.1 billion in tool maker ASML to drive it forward. "EUV is very important to us, and that's why we invested in ASML, but we have multiple paths that we pursue such as immersion with multiple patterning," Bohr said.

Intel expects to use at least double patterning in some layers of some chips at 14 nm. If immersion is used at 10 nm, more layers will require double patterning, and some will even require quadruple patterning, he said.

At 14 nm, Bohr said, "the increased wafer costs [associated with double patterning] is still being offset by improved density, so our cost per transistor continues to go down with each generation on a very steady trend."

That trend would continue, he suggested, even if immersion is used at 10 nm. As of today, "EUV is later than I would like, and I can't count on it for sure," he said.

"We are probably the last company continuing to stay on a pace of having a new process technology every two years or so," Bohr said in his talk.

Join the premier professional organization for mask makers and mask users!

About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

Individual Membership Benefits include:

- Subscription to BACUS News (monthly)
- Complimentary Subscription *Semiconductor International* magazine
- Eligibility to hold office on BACUS Steering Committee

spie.org/bacushome

Corporate Membership Benefits include:

- Three Voting Members in the SPIE General Membership
- Subscription to BACUS News (monthly)
- One online SPIE Journal Subscription
- Listed as a Corporate Member in the BACUS Monthly Newsletter

spie.org/bacushome

Calendar

2013

SPIE Advanced Lithography

24-28 February 2013
San Jose Convention Center and
San Jose Marriott
San Jose, California, USA
spie.org/al

SPIE Photomask Technology

10-12 September 2013
Monterey Marriott and
Monterey Conference Center
Monterey, California, USA
spie.org/pm

SPIE is the international society for optics and photonics, a not-for-profit organization founded in 1955 to advance light-based technologies. The Society serves nearly 225,000 constituents from approximately 150 countries, offering conferences, continuing education, books, journals, and a digital library in support of interdisciplinary information exchange, professional growth, and patent precedent. SPIE provided over $2.7 million in support of education and outreach programs in 2011.

International Headquarters
P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 360 676 3290
Fax: +1 360 647 1445
help@spie.org • SPIE.org

Shipping Address
1000 20th St., Bellingham, WA 98225-6705 USA

SPIE Europe
2 Alexandra Gate, Ffordd Pengam, Cardiff,
CF24 2SA, UK
Tel: +44 29 2089 4747
Fax: +44 29 2089 4750
spieeurope@spieeurope.org • www.spieeurope.org

You are invited to submit events of interest for this calendar. Please send to lindad@spie.org; alternatively, email or fax to SPIE.