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Second Place Best Poster

EUV mask defect mitigation through pattern placement

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ABSTRACT

One of the challenges of EUVL is to bring EUV mask blank defect levels to zero. With uncertainty on when defect free masks may be routinely available, we explore a possibility for effectively using defective EUV mask blanks in production with a defect avoidance strategy. The key idea is to position the pattern/layout on the blank where the defects do not impact the final wafer image. Assuming that layout designs contain some non-critical areas in which defects can be safely positioned, it may be possible to align these regions with a given, small set of defect positions mapped from an imperfect mask blank.

Using a few representative assortment of current-node, full-chip layout patterns we run multiple trials against real blank defect maps with various defect counts successfully. Our goal is to assess the probabilities that defect avoidance will work as a function of mask blank defect count, and by lithography layer.

1. Introduction

While similar to conventional optical lithography in many respects, Extreme Ultraviolet Lithography (EUVL) impacts many supporting infrastructure technologies beyond the exposure tool itself. In addition to the disruptive changes in exposure tool technologies—reflective optics, exotic light sources, vacuum environment—infrastructural technologies impacted include needed new resist and etch processes, new mask materials, new mask blank and finished mask inspection tools, mask handling in the absence of pellicle, and so on. Challenges in all of these supporting areas must be resolved before practical high volume EUV production is real.[1]

Continues on page 3.

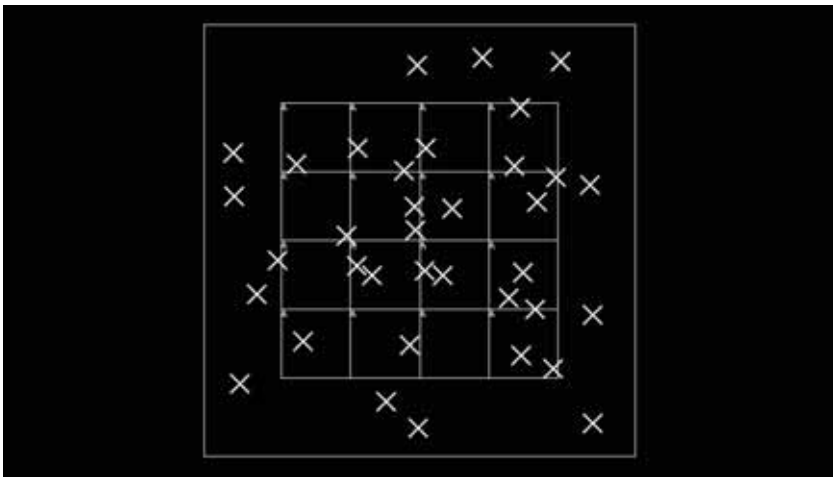

Figure 1. Example mask blank (outer square) with defects (X's) and an arrayed mask layout pattern (inner rectangle grid).

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TAKE A LOOK INSIDE:

SPIE

EDITORIAL

Change the Process

Mark T. Jee, HOYA Corp, USA

Semiconductor sales are booming, equipment sales are strong, materials are in high demand…so why do many of us like to give in to a sentiment that this recovery will be short-lived? While the overall economics of our nation and the world affect the semiconductor industry, in the midst of the one most formidable recoveries in the last 20 years, people and businesses alike choose to endorse the feel that the other shoe has to drop. This year's Photomask Technology conference is wrapping up and attendance is flat from last year and certainly not at the highs of 2007. Does this portend what may be in our future? Earlier this year, the scheduled Lithography Asia Korea conference was postponed because of severe reduction in the number of submissions. In reaction to this news, it was pointed out that March 2010 was the 2nd best month all time for semiconductors. There appeared to be optimism in the semiconductor industry, which has not translated into the return to the attendance patterns at conferences. Companies not willing to subscribe to a new wave of irrational exuberance, cut back non-essential travel and activities, gladly citing the economic conditions. And the participant numbers signal that many conferences may just be what they seem to be—non-essential, not meeting the needs and expectations of the prospective attendees. So are we to reexamine our Photomask Technology Conference to ensure its continued relevance? We are willing to be self-critical, but this is not what the sponsors can take to their bottom line. We need to be more constructive than that.

Certainly, there are circumstances beyond our small enclave that we cannot control, to keep us down, however successful our refocusing efforts may be. But the speakers at BACUS 2010, from the keynote talk on, agreed that there are no "bad" conditions in which to do business. One needs to keep their eyes open, to quote Frank Kalk.

When the semiconductor sector seems to be healthy, why does the general business environment project depression? Do these companies that are healthy really believe that better days are ahead? With the cash piling up, moves are made to expand into existing businesses (software, wireless chips) rather than invest in new projects or hiring. A glimpse into this thinking is the recent comment from Intel CEO Paul Otelllni: "I think this group does not understand what it takes to create jobs. And I think they're flummoxed by their experiment in Keynesian economics not working." Was he chiding his mask shop? No, the group he was speaking of does not do business in the Santa Clara, but wonders about it in our Nation's capital. Mask shops have no plans to run economic stimuli; instead, they thrive on efficiency. But they also need directions. Which one of the NGL's is worth investing, and which one is just the stimulus money?

Some may see the "investment" of capital by governments and big sponsors into the semiconductor industry as a part of a solution. Is this "stimulus" money that we believe in because it happens to benefit our industry creating jobs and betting on strategies that are not guaranteed? For every "wise" investment there are usually others of more dubious quality.

Unemployment remains as stubbornly high, as the lack of clarity in the NGL solutions, prompting some to rely on the Fed further easing money supply. The solutions proposed by those who can supposedly fix the problem seem not to quite work yet, still, we have been unable to change the process: neither the economy, nor the IC manufacturing. This is one root of our current economic malaise—the conceit of those that believe more spending, taxing and (design) rule-making can force-feed economic expansion or take us further down the shrink path. Now that experiments may be failing, those who cheered the stimulus are asking the Federal Reserve to save the day: on the Wall Street and on the ITRS roadmap. Mr. Bernanke and Mr Otellini should tell them politely but firmly that their job is to maintain a stable level, not to turn bad policy into wine.

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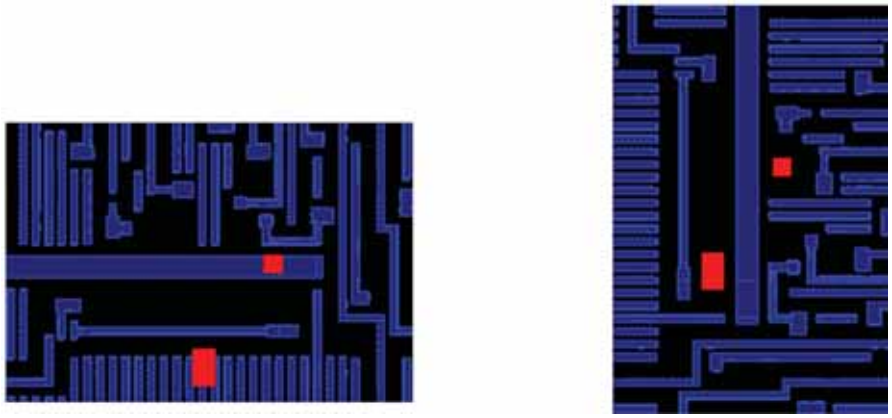

Figure 2. With space defining absorber (a darkfield mask) the layout pattern can be rotated and repositioned so that both defects fall into "harmless" areas, as shown in the right hand image.

One of the most significant infrastructural changes brought on by EUVL is the change from optical transmission masks to the reflective masks needed for EUVL. To maximize reflection at 13.5nm wavelength, the mask blanks contain a Bragg reflector constructed from a stack of 40 to 50 Mo-Si alternating layers. Each of these 4-5 dozen component layers, (in addition to other material layers such as Ru cap layer, TaN absorber layer, CrN conductive layer), is a discrete processing step with a cumulative opportunity for adding defects.

Early EUV mask blanks contained thousands of defects. With first generation mask-blank inspection methods limited to detecting 80nm defect size the trend of detectable defects showed steady progress, with defect counts dropping to hundreds by 2007. However, improving blank inspection capabilities reveal an increasing number of previously undetected but relevant defects. Increasing the detection to 50nm from 80nm raised the defect count by more than an order of magnitude.[2] The relevant defect levels on EUV blanks will remain unknown until EUV blank inspection tools are capable of resolving them. In spite of steady progress in EUV blank manufacturing technology, it is quite possible that EUV blanks will not achieve zero defectivity by the time they are needed for production.

If EUV mask blank defects are not resolved by EUV high-volume production then some method will be required to deal with defective mask blanks. The complex multilevel structure of the blanks may make mask blank repair, certainly below the top mask blank layer, all but impossible. An alternative approach is to render the defects harmless by shifting the mask layout on the blank so that all defects occur where they cannot impact the resulting image on the wafer image. We call this "defect avoidance."

2. Experiment

Our experiment is to test the defect avoidance method to a set of mask layouts constructed from real circuit designs applied to a set of ten defect maps measured from actual EUV mask blanks. Seven mask layouts were derived from an assortment of lithography-layer designs shrunk to 11-22nm node dimensions. To maximize filling the EUV exposure field (26mm X 33mm) relatively small circuit layouts were arrayed edge-to-edge, with no intervening frame space between array instances. For this experiment the dispositional area was confined to be under the mask absorber layer, which corresponds to either the defined feature or space of the mask layout, depending on the process tone. The dispositional area also includes the region outside of the arrayed mask layout, where defects do no harm. The measured defect maps were converted to layout patterns with rectangles corresponding to the location and X and Y dimensions of the measured defects for each mask blank. An acceptable alignment of a mask layout with a mask blank takes place when all of the defects land entirely within dispositional features or regions.

For these trials, the freedom to locate acceptable alignments was limited to shifting the mask layout pattern within a range of +/- 200 µm in X and Y, in each of four orientations: 0, 90, 180, 270 degrees. For each trial, a layout representing the dispositional area for a mask layout and a second layout containing the defect features for a mask blank were compared over the degrees of freedom. The seven mask layouts were tested against the 10 defective mask blanks for a total of 70 trials.

Synopsys' CATS mask data preparation tool was used to find the alignment within the acceptable range that matches the defect map to the disposition locations. A minimally acceptable match is detected wherever all defects are enclosed. In some cases, several minimally acceptable locations are found, from which the location that provides the largest enclosure margin can be identified. For proof of concept, when one or more acceptable alignments are found for a current orientation, no further orientations are tested.

The computations were executed in distributed mode, involving up to 64cpus, with a maximum runtime of 146 minutes. All design data was encoded in OASIS data files placed in an extended jobdeck.

3. Results and observations

Table 1 summarizes the results of our 70 trials. For each trial 'NA' indicates that no alignment was found within the +/- 200µm range in X and Y in any of the four orientations. 0 indicates an alignment found on the first orientation, 90 indicates that an alignment was found on the second orientation but not in the preceding orientation, and so on. The total number of defects on each blank is tabulated in row 2, the largest dimension of the biggest defect on row 3. The last two rows show data for two early runs used to develop the methodology with designs larger than 22nm (and these rows of data are not included in our summary statistics).

Taken together, a defect avoidance strategy with these 10 mask blanks and the 7 mask layouts provides many alternative effective pairings among them – all these designs have at least 2 blanks on which they can be realized, and every blank is usable on 3 or more designs. Blank 8 was the hardest to deploy, where pairing with 4 layouts was not possible. Design C was the hardest to fit

Table 1. Summary of defect avoidance trials.

	Blank 1	Blank 2	Blank 3	Blank 4	Blank 5	Blank 6	Blank 7	Blank 8	Blank 9	Blank 10
Total Defects	10	23	31	33	36	40	43	47	53	55
Largest Defect (nm)	206	1726	800	1456	926	446	610	3690	270	146
Design A	0°	0°	NA	NA	0°	NA	0°	0°	180°	0°
Design B	0°	0°	0°	0°	0°	0°	NA	NA	NA	NA
Design C	0°	0°	NA	NA	NA	NA	NA	NA	NA	NA
Design D	0°	0°	NA	NA	270°	NA	NA	NA	0°	0°
Design E	0°	0°	0°	0°	0°	0°	90°	NA	270°	0°
Design F	0°	0°	0°	0°	0°	0°	0°	90°	0°	0°
Design G	0°	0°	0°	0°	0°	0°	0°	0°	0°	0°
Pipecleaner 1	0°	0°	0°	0°	0°	0°	0°	0°	0°	0°
Pipecleaner 2	0°	0°	90°	0°	0°	0°	0°	180°	180°	0°

on a blank, where pairing with 8 blanks was not possible. If we randomly had just one of these mask blanks on hand, and tried to fit it to one layout picked at random, we would have had a 70% chance (49 successes out of 70 trials) of getting a usable combination. This suggests for a production environment, a reserve of some number of mask blanks must be kept on hand at all times to ensure high probability of pairing it to the next design in the door.

The +/- 200µm limit on translation degrees of freedom was chosen for experimental expediency. Wherever the mask layout is smaller than the available exposure field the translation range can be increased to position the layout anywhere within the exposure field, which will increase the probabilities of a successful alignment. To first order, if the probability, p, of finding a fit within a 400 x 400 range is, say 30%, for a particular defective mask blank and pattern, doubling the range in both axes to 800x800 quadruples the number of possible alignment locations thus increasing the probability to $1-(1-p)^4$; thus in this example increasing the chance for successful alignment from 30% to 76%.

Increasing the dispositional area in the mask layout is another opportunity to further increase the probability for successful alignments to avoid defects. With real mask layouts the frame space between die placements could be declared "safe" for defects (depending on user requirements) and included in the dispositional area. Similarly, regions containing non-critical features, such as dummy fill patterns, could be added to the dispositional area, as well as additional areas declared by design to be immune to the presence of defects.

As seen in figure 3 there is some correlation between defect size and difficulty in finding an alignment. However this data suggests that some layout pattern types contain a sufficient number of large disposition areas in which to safely align a mask blank with an enormous defect. A fit was not possible with Layout "C" on 80% of the mask blanks, but a suitable alignment was made with a blank containing a relatively large defect.

In some additional testing that was done with our customer on their actual designs, we were able to find solutions for most of the layers attempted. However, we found some difficulties in a dense polysilicon layer that included filler and dummy features. We believe that if the mask defects were allowed to fall within the filler feature regions (outside of absorber pattern) the prospects for finding a fit would improve, however, this experiment has not been done as of yet.

4. Conclusions and future directions

Allowing for the relatively small sample of mask blanks, and the fact that most of the mask layouts used in this study were concocted from designs for less advanced nodes by way of shrinking them, the prospect for using defect avoidance methodology to make use of defective masks looks promising. With current levels of mask defectivity, a mask shop must plan on maintaining a reserve of some number of mask blanks to maximize its chance of finding a blank to pair with each new design. With the data collected in this study the chance of finding a useful pairing with one blank is 70% (49/70). Based on this number the probability of getting an effective pairing with one of N mask blanks is $P = 1 - (0.3)^N$. Thus to achieve a 99% probability of pairing to the next (unknown) design of any type we would need to have at least 4 mask blanks on hand. Recall that one design (C) could be paired with only 20% of the blanks. To insure 99% probability to fit this "worst case" design 21 mask blanks would be needed on hand ($0.8^{21} = 0.0092$ = probability of not finding a fit). Risk is further mitigated by choosing the "worst mask" wherever possible—that is to use the mask with the most or largest defects as early as possible—thus leaving the better masks for the next (unknown) layout.

One factor that may lower the apparent effectiveness of this method is that current EUV mask and mask blank inspection tools do not use AIMS-based inspection (with actinic illumination).[3] It may turn out that the actual number of critical defects is substantially larger than what is currently possible to detect[4] by indirect optical, SEM, and AFM methods, and the probabilities of pairing the blanks to designs may therefore go down.

To enable a practical defect avoidance method the mask blank inspection tools must be able to accurately locate defects on the blank. This means that the mask blanks must embody fiducial marks on which to reference defect locations. Similarly, mask writing tools must align the circuit layout with respect to these alignments marks. The accumulated alignment tolerance between the inspection tool and the mask writing tool must be accounted in defect avoidance, most likely by enlarging the effective area of the defects.

An obvious next step is to empirically validate the effectiveness of defect avoidance by fabricating an EUV mask and measuring the performance on printed silicon. Depending on actual results and the expected trend in defect reduction, design-driven methods to expand the defect dispositional area on each layout design may help improve the practical application of defect avoidance.

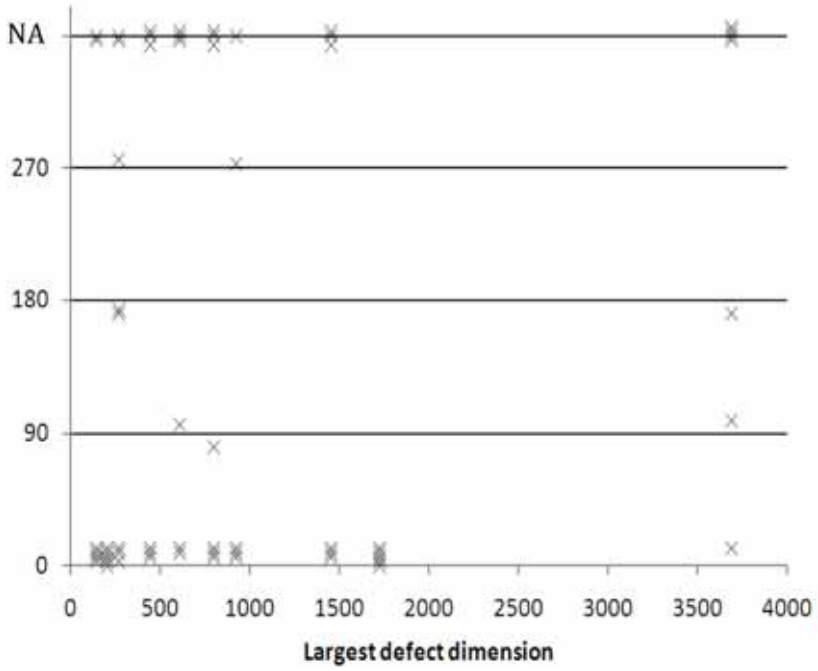

Figure 3. Alignment success vs. maximum defect size.

5. Acknowledgments

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EDITORIAL (Continued from page 2)

If the thoughts that we may never come back, or this is as good as it gets, are true, we have to admit – we get what we deserve. For further wisdom we can do worse than consider what the former Prime Minister Tony Blair had to say on stimulus, Keynesianism and re-regulation, "Ultimately the recovery will be led not by governments but by industry, business, and the creativity, ingenuity and enterprise of people. If the measures you take in responding to the crisis diminish their incentives, curb their entrepreneurship, make them feel unsure about the climate in which they are working, the recovery becomes uncertain."

To push the BACUS Photomask Technology Conference beyond the current crossroads, your steering committee will be making the necessary adjustments. Please continue to support your local photomask conference and consider that your thoughts are as important as your sponsorship.

Industry Briefs

Business News Mix(ed)

The incoming flurry numbers is good, yet many prefer to subscribe to the notion that past results do not guarantee future performance. "Bookings declined slightly in August, but 2010 is still on track to be a record growth year for semiconductor equipment", noted Stanley T. Myers, President and CEO of SEMI. Right after the BACUS Photomask 2010 Symposium, the National Bureau of Economic Research announced that the longest U.S. recession since World War II ended in June 2009. Yet, it appears that we are already heading into our typical cycle. The latest book-to-bill figures could indicate that the sector has reached its cycle peak, with August bookings down slightly from July's high of US$1.86 billion to US$1.81 billion (but still 195.5% higher than the same period a year-ago). The equipment sales recovery had started in May 2009, according to SEMI. Worldwide installed capacity is to grow 7% in 2010 to 14.4 M wafers per month. Fab construction spending is up 125% in 2010 to $4.5B and up 22% in 2011 to $5.5B. 22 facilities (including MEMS, LEDs and R&Ds) to begin construction in 2010: 13 LED fabs, 4 Foundries, 2 Memory and 1 for System LSI. While spending on equipping facilities is to increase by ~133% to $33.9B in 2010 and by ~18% to $39.8B in 2011, which will see 28 facilities to begin operations: 13 for LED, 5 for Foundries and 4 for Memory, Gartner warns of chip correction in second half of 2010 [WSJ Market Watch]: Chip sales are poised to jump more than 30% this year, but the industry is likely headed for a "modest" softening in the second half of 2010. In 2011, analysts see only a 4.6% rise in revenue. Intel lowered its sales forecast, citing weaker-than-expected demand in the consumer PC market. "Early strength in the PC market and supply constraints" have made the DRAM industry "very profitable," with revenue poised to jump 82.5% to nearly $42 billion this year. "However, during the second half of 2011 we expect a DRAM downturn in 2012 as sales decline 29%".

This rings in an interesting change in the global Semiconductor Industry: After over 20 years of stasis in the pecking order of IC manufacturing revenues, it looks like Samsung's remarkable rise in performance might see the company overtake current leader Intel as soon as 2014, based on the company's semiconductor revenue rise of 13.5% CAGR from 1999-2009. Intel has seen revenue CAGR of 3.4% for the same timeframe. If Samsung continues with this growth rate, IC insights' data suggests that the company will overtake Intel in semiconductor sales in 2014.

Multiple E-beam - A Lithography Alternative?

By **Mark Osborne,** FabTech News

Lithography track specialist, SOKUDO has joined the new industry and research multi-partner program IMAGINE run by CEA-Leti developing maskless lithography for IC manufacturing. Under a three-year project, TSMC and STMicroelectronics are working to potentially bring maskless lithography developed by MAPPER Lithography into the mainstream.

"E-beam has the potential to be a viable technology for many sub-22nm lithography layers in logic/foundry semiconductor manufacturing," noted Tadahiro Suhara, SOKUDO president and CEO. "SOKUDO is taking a comprehensive approach to being prepared for coat/develop track process readiness in multiple sub-22nm lithography technologies, including immersion ArF lithography extensions, EUV and e-beam lithography. The CEA-Leti IMAGINE collaboration brings together a focused effort to enable production-worthy e-beam lithography, including multiple resist manufacturers key to sub-22nm process development. The experience of CEA-Leti in e-beam technology combined with SOKUDO's coat-and-develop track expertise will help secure the necessary process infrastructure for multi e-beam lithography.

Concerns remain that both immersion with double printing and EUV lithography will be too expensive for many types of IC device requiring fabrication below the 22nm node and therefore e-beam technology could supplement lithography requirements in the future.

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Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

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Calendar

2011

SPIE Advanced Lithography

27 February-4 March
San Jose Marriott and
San Jose Convention Center
San Jose, California, USA
spie.org/al

Late submissions will be considered by conference chairs.

SPIE Photomask Technology

19-22 September 2011
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and Monterey Conference Center
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