

PHOTOMASK

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Photomask Best Poster

Transparent and conductive backside coating of EUV lithography masks for Ultra Short Pulse laser correction

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1. ABSTRACT

In order to improve on-product-overlay, the image placement performance of a photomask can be corrected and improved through a multiphoton absorption process. This is possible with an ultra-short pulse laser focused into the glass substrate of the mask, from its backside. For optical masks, this is a well-established technology by using the RegC system from ZEISS. Applying this technology to EUV mask requires a backside transparent coating, still electrically conductive for chucking (according to SEMI SPEC). Using nanometers thick Cr and Ni, their oxide and nitride forms, in different stoichiometric forms if need be, we have developed a backside coating with the required optical transmission, sheet conductance, and mechanical durability, and demonstrated femtosecond correction through it. The proposed backside transparent coating designs can be extended to other metals, such as Ti, Ta, Mo and compounds, such as carbides and borides.

2. Introduction

Photolithographic masks, especially for Extreme Ultraviolet (EUV) lithography have to fulfill the highest demands with respect to defectivity, CD uniformity, mask flatness, and especially image placement (registration) as well as mask-to-mask overlay. These challenges require highly precise techniques for the production of extreme ultraviolet (EUV) masks^{1,2}. It is already known that an

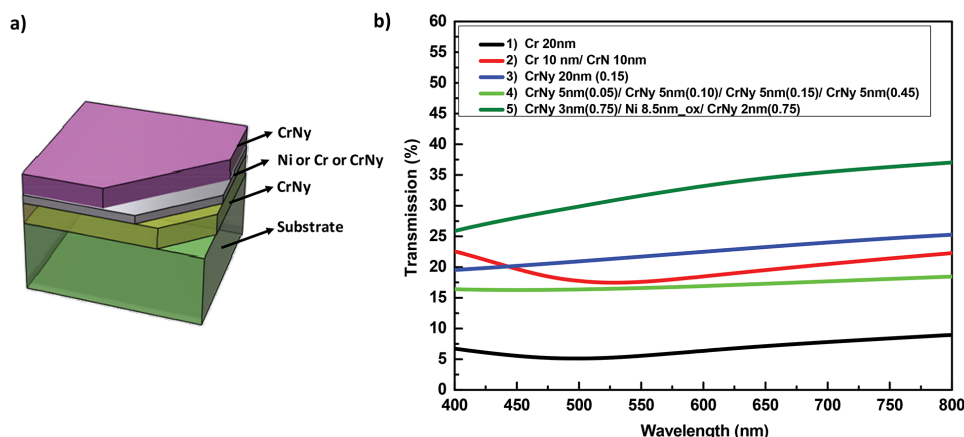


Figure 1. a) structure of backside transparent electrode (BTE) coatings; b) transmission spectra of different structures optimized over the visible region.

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EDITORIAL

T-minus 5 4 3 2 1...

Larry Zurbrick, *Keysight Technologies, Inc.*

I've always been fascinated with the rapid progress that the aerospace industry made over the course of the short period of its first 66 years. From Wilbur and Orville Wright's first flight in 1903 in a heavier than air craft to the Project Apollo landing of men on the moon in 1969, it was accomplished within a person's lifetime. (My grandfather no doubt read about the Wright brothers' flight in a newspaper and watched the Apollo 11 landing of men on the moon on TV, not to mention that TV was also invented and commercialized during his lifetime.) Truly a breathtaking advance in manned flight.

The invention of the integrated circuit process is attributed by some to Jack Kilby, Kurt Lehovec, Robert Noyce, and Jean Hoerni between the years 1958 and 1960, although the invention or idea of the integrated circuit itself can be traced back almost a decade earlier. Tremendous progress in device and process technology has been made in the past 58 years. The initial progress observation was first summarized by Gordon Moore in 1965 who anchored the starting point in 1959.

Lithography has and continues to support the IC industry. It can be argued that lithography has advanced at a similar or faster rate over the past 58 years than the first six decades of the aerospace industry. We have advanced from contact printing wafers using silver halide based emulsion photomasks with "white" light to utilizing a wafer scanner operating at an extreme UV wavelength. There appears to be any number of parallels that can be drawn between these two industries. The Wright brothers had a small team to accomplish their first flights. Mask design and mask making 58 years ago could be accomplished with a small team and minimal investment. The moon landing and safe return to Earth required enormous teams coordinated across many industries to first invent, then build the necessary infrastructure and finally execute the moon mission. After the recent joint Photomask Technology and Extreme Ultraviolet Lithography conference in Monterey, I was left with the impression that we are accomplishing a similar feat in solving both the technological and commercial challenges of EUV lithography. Like the moon mission of decades past, we have and continue to invent and build the lithography infrastructures needed in enormous teams across the entire lithography supply chain.

Both endeavors required the vision and determination to reach their goals. The difference is that man only went to the moon on 11 missions and lithography has already advanced more than 11 node "missions" between 1980 to today. Today, our industry is now at the execution phase of its EUV mission. It's time to launch!



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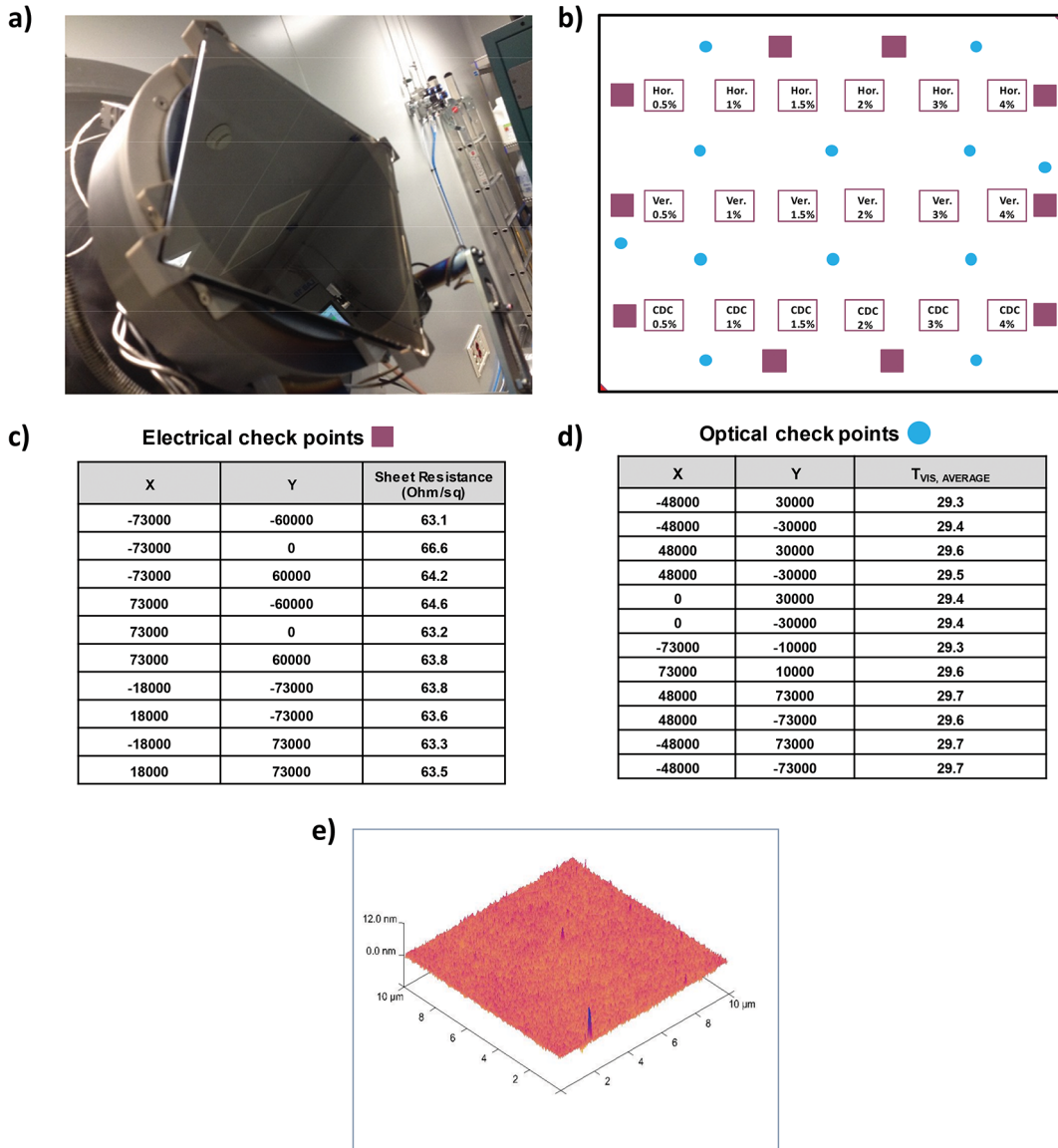


Figure 2. a) photograph of sputter deposited BTE on 6"x6"x6mm ULTE substrate; b) optical and electrical check points; c) values of sheet resistance and d) optical transmission; e) AFM image of the coating on fused silica substrate over a scanned area of 10x10 μm.

optical photomask can be modified in a controlled manner in order to correct image placement signatures, by applying ultra-short laser pulses into the substrate by using the RegC system from Carl Zeiss^{3,4}. This compensation occurs through multiphoton absorption of incident light from the backside of the mask. Thus applying this technology to EUV masks requires a backside coating sufficiently transparent at the wavelength of the ultra-short laser pulses.

Importantly, an extremely careful handling and chucking of EUV mask is necessary in order to avoid mechanical abrasion and the formation of particles, which may deteriorate the function of an EUV lithography system. In order to fulfill these handling requirements, EUV masks are held by an electrostatic chuck in the scanner. As the substrate of EUV masks is a dielectric, usually glass or a semiconducting material, an electrically conducting layer has to be deposited on the backside, in order to be able to electrostatically hold the substrate. Therefore, in order to allow image placement correction by ultra-short pulsed laser technology, the backside

coating has to be optically transparent and electrically conductive at the same time.

Ultrathin metals, if sufficiently thin, their nitrides, oxides, borides, carbides or combinations, become transparent while still being electrically conductive. In this paper, we introduce backside transparent electrodes (BTEs) for EUV masks consisting of multilayer films made of ultrathin Ni, Cr, nitrides, and oxides having different compositions and thicknesses. Different compositions are obtained by varying the atmosphere during deposition. For example, during deposition of Cr one can obtain different CrN_x stoichiometry by varying the ratio of N₂ and Ar during the sputtering process. Though we show results on Ni and Cr, the concept can be extended to any other suitable metals and combination of nitrides, oxides and borides and carbides of proper stoichiometry.

The multilayer BTEs typically have an optical transmission of 20-50% and an electrical sheet resistance (R_s) of 50-150 ohm/

sq. The coating exhibit high mechanical resistance and durability, which are confirmed through abrasion, adhesion and scratching tests. We also demonstrate pixel writing through such coating, enabling the technological path to correction and tuning of image placement on EUV masks.

3. Results

3.1 Structure, Optical and Electrical performances of the electrodes

The geometry of the proposed multilayer BTEs are shown in Fig 1a. Different structures were investigated having different number of layers, different materials, and composition. For the experiments, we deposited and studied in detail the BTEs on ultralow thermal expansion glass (ULTE) substrate. Among the materials used, Ni, Cr, Cr nitrides and Ni oxide were mostly investigated, though the approach can be extended to other metals (e.g. Mo, W, Ti, Zr, Hf, V, Nb, Ta) and compounds (borides and carbides). Previous work had shown that metallic films such as Ni and Cr in its extremely thin form (<10nm) are transparent to light even in the UV (ultraviolet) and IR (infrared) spectra⁵. Moreover, they exhibit superior electrical conductivity (low R_s). However as metallic films are highly reflective, it is already known that oxide/nitride undercoat and overcoat layers can reduce their reflection and in turn enhance optical transmission^{6,7}.

In our study, CrNy having different stoichiometry is used. CrN is widely used in different applications, including back side coating of lithography masks, thanks to its high mechanical resistance and adhesion properties^{8,9}. In addition, the material is non-toxic and highly chemical resistant. During sputtering of Cr, depending on the ratio of N_2 and Ar gases, CrNy having different stoichiometry with y varying from 0 to 1 or even more than 1 can be obtained. The critical parameter is the ratio between the flux of N_2 and total flux (sum of N_2 and Ar), i.e. $N_2 / (N_2 + Ar)$ ratio. The larger this ratio the larger the y value.¹⁰

Fig 1b. shows the optical spectra of the optimized electrodes over visible spectra. Two types of electrodes were studied. In the first configuration, a thin film of partially oxidized Ni (8.5nm) is sandwiched in between CrNy layers where $y=0.45$. The oxygen (O_2) diffusion length in Ni is about 2.5 nm. Beyond this value, the oxidation is minimum and this ensures the environmental and chemical stability of the remaining metal. A CrNy under coating layer of 3nm and overcoat of 2nm are also applied over the Ni/NiO_y structure. It is evident from the figure that the electrode maintain more than 30% transmission over the visible spectra together with a R_s of 94 ohms/sq. In the second configuration, we prepared and tested multilayer structures of CrNy having different compositions. The total thickness of all the structures was kept below 20nm, and all maintained transparency more than 15% in the visible. The BTE structures are compared with prior results on transparent electrodes containing at least one Cr metal layer. The R_s of the different structures was measured in between 50-150Ω/sq. (Table 1).

Note that the final composition of CrNy depend on the equipment used. That means that for the same value of y set during the process, the atomic ratio between Cr and N may vary. In addition, the electrical and optical properties of the film may depend on the equipment and target materials, not only by the deposition conditions. The developed BTEs can be further improved in terms of optical, electrical and mechanical properties by using sophisticated and industrial equipment. Nevertheless, the paper clearly shows that specifications are already met for EUV lithography masks.

Planarity or uniformity of the backside coating is important for photolithographic masks, especially for EUV. In order to verify the uniformity, the BTEs are deposited on large 6"x6"x6mm ULTE mask blanks and its electrical and optical performance are verified at different points. Figure 2a shows the image of the mask blank after deposition. The electrical and optical check points are indicated in Fig 2b. The corresponding values are in Fig 2c and 2d for an optimized optical transmission-electrical resistance (conductance) trade-off. Their limited variation indicate high uniformity, especially considering that our deposition equipment is for research purposes and not industrial production. The surface morphology of the deposited film is also analyzed. Fig 2e shows the Atomic Force Microscopic (AFM) image of the same coating deposited on fused silica substrate, and measured over 10x10μm. The Root Mean Square (RMS) roughness of the coating measured is <0.5nm, which confirms that the coating is atomically smooth.

3.2 Mechanical Resistance Performance

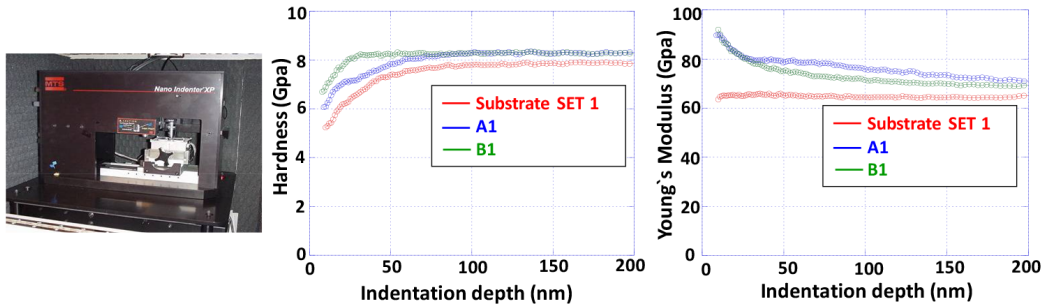
In addition to being electrically, conductive and optically transparent BTEs for EUV optical elements have to be mechanically durable. This is because of the strong forces between the BTE and the pins of an electrostatic chuck that may lead to indentation and scratching. In addition, the mask is subjected to strong lateral acceleration that may result in abrasion for the BTEs. The mechanical durability is associated to the use of nitrides, borides and/or carbides in the structures.

In order to study the mechanical resistance of the coatings, nanomechanical characterization including mechanical properties, static-load spherical indentation, and nanoscratch test were performed. The effect of temperature on mechanical properties of the coating during BTE deposition was also investigated. Figure 3 shows details of some of the tests performed. In fig. 3, coatings A1 and B1 represent the BTEs deposited at low (130°C) and high temperature (300°C), respectively, while substrate SET 1 represents the blank ULTE glass substrate.

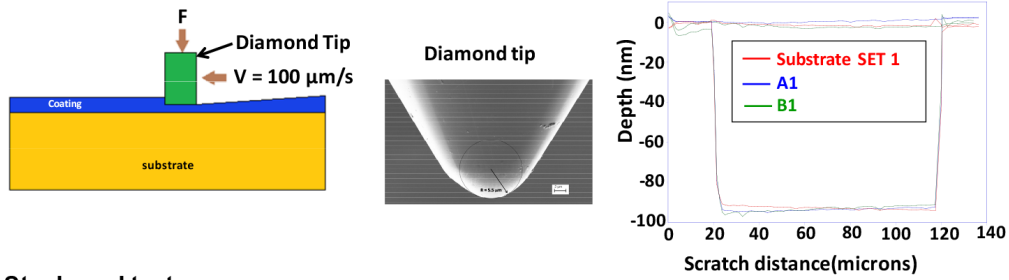
Static-load indentation and nanoscratch tests were carried out in a Nano Indenter XP (MTS-Keysight) as in Fig 3a. The hardness and Young's modulus evolution of the samples as function of the tip displacement (depth) was determined by nanoindentation by using a Berkovich diamond tip. The measurements were carried out using the Continuous Stiffness Measurement (CSM) operation mode, controlling the AC load to give a 2nm harmonic displacement amplitude at 45 Hz. Samples were allowed to thermally equilibrate with the instrument until the drift rate measured was below 0.050nm s⁻¹. For each sample, a total number of 15 indentations were carried out at a constant strain rate of 0.050 s⁻¹, up to a maximum penetration depth of 200 nm. A Poisson's ratio of 0.25 was supposed for all the samples. Nanoscratch tests were carried out using the same diamond conical tip with constant load = 8 mN, scratch length = 100 μm, and scratch tip velocity = 10 μm/s. For each sample, a total number of 15 nanoscratches were carried out. The scratch depth and the residual scratch depth profiles as function of the scratch distance are reported.

Figures 3a shows the hardness and Young's modulus evolution as function of the tip displacement into the surface, respectively. As it can be seen from these figures, significant differences are observed between the three samples. Coated A1 and B1 samples show higher hardness values than substrate sample in all the indentation depth range, reaching an asymptotic hardness value around 8.3 GPa at an indentation depth of ~75 nm, whereas the asymptotic hardness value of Substrate SET1 is ~7.8 GPa. In the low indentation range (<75 nm) it can be seen that the hardness of sample B1 is higher than the hardness of sample A1. On the

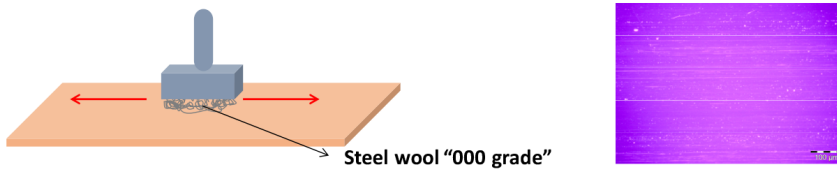
a) Nano indentation test



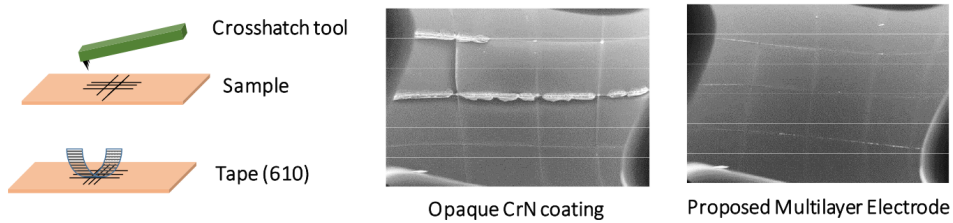
b) Nanoscratch test



c) Steel wool test



d) Cross-hatch adhesion test



e) Eraser test

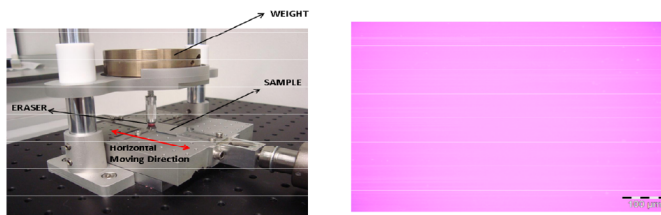


Figure 3. a) Nano indentation test results - NanoIndenter XP equipment, Hardness depth profiles, and Young's modulus depth profiles respectively; b) Steel wool test results - schematic of steel wool test and microscopic image of the coating after the test; c) Nano scratch test results - schematic of the test, SEM image of the diamond conical tip used in this work, and Scratch depth profiles respectively; d) cross-hatch adhesion test- schematic of the tool used, and SEM image of CrN coating and proposed multilayer electrode respectively after the test; e) Eraser test - Equipment used for the test and microscopic image of the coating after 100 cycles of eraser abrasion.

Table 1. Change in electrical sheet resistance of different BTE structures after Eraser test.

No.	Sample	Rs Initial (Ω /Sq.)	Rs after eraser test (100 cycles) (Ω /Sq.)	% change in Rs
1	Cr 20nm	34.6	37.2	7.51
2	Cr 10nm / CrN 10nm	107.58	101.2	5.92
3	CrNy 20nm(0.15)	246.2	249.7	1.4
4	CrNy 5nm(0.05)/ CrNy 5nm(0.10)/CrNy 5nm(0.15)/CrNy 5nm(0.45)	146.4	148.6	1.5
5	CrNy 3nm(0.75)/ Ni 8.5nm_ox/ CrNy 2nm(0.75)	94.0	97.57	3.8

other hand, the Young's modulus depth profile shows that the substrate displays lower Young's modulus values as compared to A1 and B1 coated samples.

In order to obtain representative averaged results, a total number of 15 nanoscratch tests were carried out for each sample. During the scratch, the tip penetration depth and the normal load are recorded. Figure 3b shows the schematic of the nanoscratch test using diamond tip, and the scratch depth and the residual scratch depth profiles as function of the scratch distance corresponding to the 3 analyzed samples. There are some differences in the scratch resistance and the residual scratch depth between the 3 samples. All the samples show a similar resistance to scratch because the scratch depth during the test is similar (around 93 nm). The residual scratch depth (obtained from the profiling after the scratch test) of substrate sample is close to 0 nm, thus indicating a full elastic recovery. Coated samples A1 and B1 show an appreciable residual scratch depth (around 2 nm) which evidences that in both cases the coating has been elastoplastically deformed.

In order to evaluate abrasion resistance of ULTEM substrates with coated layers under-pressure, steel wool test is also performed. Steel wool grade 000 were attached to a metal block and a pressure of 0.1MPa was applied on the coatings as shown in the schematic in Fig 3c. 100 strokes were used at 0.8Hz and damage was assessed by optical microscope. From the optical microscopic images of the coating after steel wool test as shown in fig 3c, it is clear that the coating is hard enough to prevent any dramatic change.

Cross-hatch Adhesion was performed to evaluate the adhesion of the coating to the substrate. Crosshatch tool with 3 blades from COLTS with a separation of 1mm, and Scotch Tape 610 is used for the tests as shown in Fig 3d. With respect to the thick (opaque) CrN coating, the SEM images of the semitransparent multilayer BTEs confirms that the proposed structure has high adhesion as well as produces smaller border effects than CrN.

An eraser test was also performed. This test is based on American Military Standards: MIL-C-00675, MIL-M-13508, and MIL-F-48616. An Eraser test with a pummel-rubber (\varnothing 4mm) with a pressure of 1.56 MPa was applied on coatings. 100 strokes were applied at $v = 0.5\text{cm/s}$. Damage was assessed by optical microscope and spectrometer. Fig 3e shows the microscopic images of a typical BTE after eraser test, while Table 1 the R_s of different structures after eraser test. Structures including metal/

metal nitride multilayers and metal nitride/metal nitride multilayers are compared. Structures including Ni or Cr allows achieving sufficiently low R_s and high T while the top CrN layer provides the strong mechanical resistance. The R_s value after erasure test changes for Cr, Ni/CrN and Cr/CrN multilayers, whereas the change is significantly lower ($<1.5\%$) for CrN/CrN multilayer structures. This is probably related to the lower hardness of Cr and Ni and the difference in thermal and mechanical properties of metals and metal nitrides. In any case the changes are all relatively small confirming the applicability of the technology.

There was no significant difference between coatings A1 and B1 deposited at different temperatures after the mechanical tests.

3.3 Surface manipulation with Ultrashort Laser pulses

As already mentioned, errors already introduced in the substrate during the substrate production or introduced during fabrication process of EUV optical element have to be corrected at the end of the production process of the EUV optical element. Moreover, defects may evolve in the course of the operation of an EUV mask in the lithography system. This defect compensation occurs through the rear side of the EUV optical element by applying ultra-short laser pulses into the substrate of an optical element.

In order to verify the laser writing capability of the proposed BTEs, femtosecond over a $6'' \times 6'' \times 6\text{mm}$ ULTE substrate is performed. Fig 4a shows the schematic of the experiment. Deformation elements generated by the femtosecond laser radiation are observed. Fig 4b shows the microscopic images of the substrate before and after coating deposition. It is clear from the images that there is no damage for the BTE occurring during laser writing. Moreover, further experiments showed that it is possible to write pixel less structures through the proposed BTEs at writing depth $>500\text{um}$ any coating damage.

4. Summary and Conclusions

In summary, we demonstrated that multilayer BTEs for EUV and other lithography masks can be realized by using ultrathin metals, their nitrides, and oxides. Optical transmission of 20-50% and electrical sheet resistance of 50-150 ohm/sq. can be easily achieved. We have also shown that the proposed BTEs are uniform and mechanically resistant by adhesion, abrasion, indentation and scratching tests. Finally, we have demonstrated pixel writing through the BTEs using a femtosecond laser, which enables the

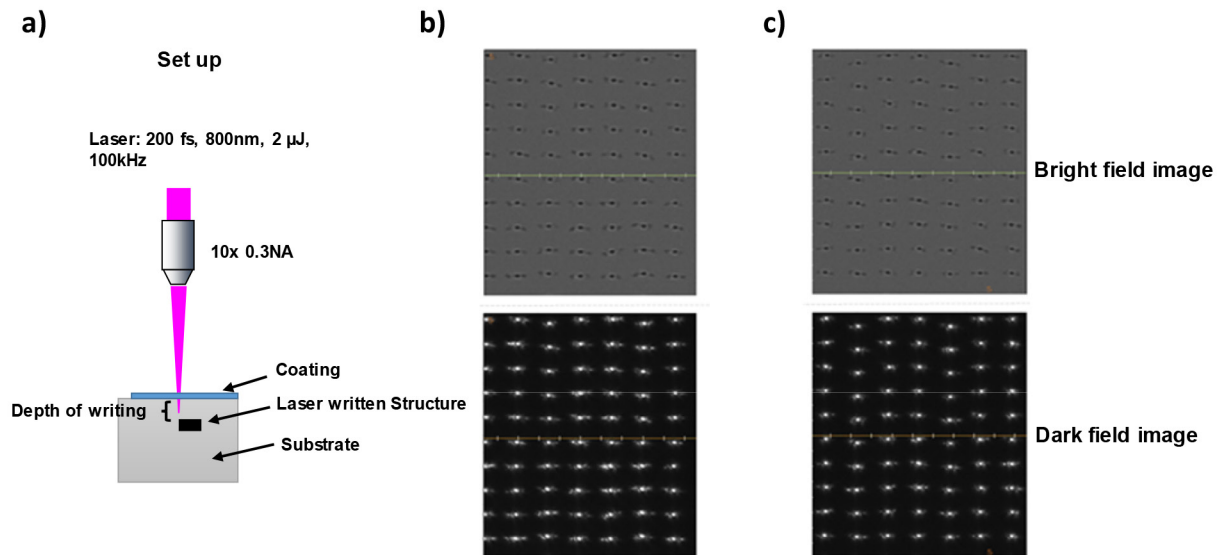


Figure 4. a) schematic of backside writing with fs laser through the proposed BTEs; b) microscopic images of the fs laser modified substrate without b) and with BTE c)

correction and tuning of image placement on EUV masks. Despite the fact that in the paper we used Cr, Ni, their nitrides and oxides, similar designs can be readily realized with similar metals, e.g. Mo, W, Ti, Zr, Hf, V, Nb, Ta, and compounds, e.g. carbides and borides. The results of this paper are thus to be considered examples and promising experiments are ongoing in our laboratory using different combinations of metals and compounds to enhance electrical, optical, and mechanical performance even further. In addition, it is worth noting that performances are limited in our experiment because of the use of research equipment. With the availability of industrial grade equipment, similar BTE designs would provide higher performance.

5. Acknowledgements

The authors appreciate the support from Carl Zeiss SMT for their collaboration in validating the proposed backside coating technology. We acknowledge financial support from Fundació Privada Cellex, and the CERCA Programme / Generalitat de Catalunya. V.P. acknowledges financial support from the Spanish Ministry of Economy and Competitiveness, through the 'Severo Ochoa' Programme for Centres of Excellence in R&D (SEV-2015-0522). We acknowledge financial support from the Spanish Ministry of Economy and Competitiveness (TEC2016-75080-R, OPTO-SCREEN).

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Industry Briefs

■ Mentor to Support TSMC 7nm FinFET Plus 12nm FinFET Process

Peter Buck, Calibre RET Tech News

Mentor, a Siemens business, announced certification for TSMC's 12nm FinFET Compact Technology (12FFC) and the latest version of 7nm FinFET Plus processes. "TSMC is pleased to work closely with Mentor, which continues to increase its value to the TSMC ecosystem by offering more features to its tool flow in support of our new 12nm and 7nm FinFET Plus processes," said Suk Lee, TSMC senior director, Design Infrastructure Marketing Division.

TSMC and Mentor worked together to make extreme ultraviolet (EUV) lithography requirements transparent to mutual customers within the Calibre design rule checking (DRC) and multi-patterning software. Calibre xACT™ parasitic extraction tool is also certified for TSMC's 12nm v1.0 and the latest version of 7nm FinFET Plus, achieving needed accuracy requirements.

The Calibre PERC™ reliability platform is the verification solution for both IP and full-chip reliability analysis, TSMC and Mentor collaborated to enable. Analog, mixed-signal and radio frequency (RF) design teams at leading semiconductor companies worldwide benefit from using the AFS platform to verify their chips designed in the latest TSMC technologies.

<https://www.mentor.com/company/news/siemens-mentor-tsmc-oip-7nm-12nm>

■ EUV Leads the Next Generation Litho Race

Solid State Technology

Confidence in Extreme Ultra-Violet (EUV) lithography is now strong, with 79 percent of respondents to the e-Beam Initiative survey, predicting it will be used in HVM by the end of 2021, a huge increase from 33 percent just three years ago. Another indication of aggregate confidence in EUVL technology readiness is that only 7 percent of respondents thought that "actinic mask inspection" would never be used in manufacturing, significantly reduced from 22 percent just last year.

Aki Fujimura, CEO of D2S, the managing company sponsor of the eBeam Initiative, sees EUVL technology receiving most of the investment for next-generation lithography (NGL), because EUV is a universal technology for memory or logic. By contrast, nano-imprint is only useful for defect-resistant designs like memory.

With practical limits on the source power, organizations are looking at ways to increase the sensitivity of photoresist to increase the throughput of EUVL. Unfortunately, there are inherent trade-offs between the best Resolution and Line-width-roughness (LWR) and Sensitivity, termed the "RLS triangle". There are various tricks to improve the resolution and roughness at a given sensitivity: optimized underlayer reflections for exposures, smoothing materials for post-develop, and hard-masks for etch integration.

A lot of work has been devoted to keeping mask write times consistent compared with last year, while the average complexity of masks continues to increase to extend the resolution of optical lithography. Even with write times equal, the average mask turn-around time (TAT) is significantly greater for more critical layers, approaching 12 days for 7nm- to 10nm-node masks.

"A lot of the increase in mask TAT is coming from the data-preparation time," explained Fujimura. "This is important for the economics and the logistics of mask shops." The weighted average of mask data preparation time reported in the survey is significantly greater for finer masks. Data per mask continues to increase; the densest mask now averages 0.94 TB, and the single mask may take 2.2 TB.

■ China IC Industry Outlook

Solid State Technology

SEMI, the global industry association, announced its new China IC Industry Outlook Report for the electronics manufacturing supply chain. With an increasing presence in the global semiconductor manufacturing supply chain, the market opportunities in China are expanding dramatically.

China is the largest consumer of semiconductors in the world, but it currently relies mainly on semiconductor imports to drive its growth. Policies and investment funds are now in place to further advance the progress of indigenous suppliers in China throughout the entire semiconductor supply chain. This shift in policy and related initiatives have created widespread interest in the challenges and opportunities in China.

With at least 15 new fab projects underway or announced in China since 2017, spending on semiconductor fab equipment is forecast to surge to more than \$12 billion, annually, by 2018. As a result, China is projected to be the top spending region in fab equipment by 2019, and is likely to approach record all-time levels for annual spending for a single region.

Join the premier professional organization for mask makers and mask users!

About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

Individual Membership Benefits include:

- Subscription to BACUS News (monthly)
- Eligibility to hold office on BACUS Steering Committee

www.spie.org/bacushome

Corporate Membership Benefits include:

- 3-10 Voting Members in the SPIE General Membership, depending on tier level
- Subscription to BACUS News (monthly)
- One online SPIE Journal Subscription
- Listed as a Corporate Member in the BACUS Monthly Newsletter

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2018

✿ SPIE Advanced Lithography

25 February-1 March 2018
San Jose Marriott and
San Jose Convention Center
San Jose, California, USA
www.spie.org/al

✿ Photomask Japan 2018

18-20 April 2018
Pacific Yokohama
Yokohama, Japan

✿ The 34 European Mask and Lithography Conference, EMLC 2018

19-20 June 2018
MINATEC Conference Centre
Grenoble, France

✿ SPIE Photomask Technology + EUV Lithography

17-20 September 2018
Monterey Convention Center
Monterey, California

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