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Etched multilayer EUV mask fabrication for sub-60 nm pattern based on effective mirror width

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ABSTRACT

With shrinking pattern size, mask 3D effects are estimated to become stronger, such as horizontal/vertical shadowing, best focus shifts through pitch and pattern shift through focus. To reduce these mask 3D effects, we have proposed etched multilayer EUV mask structure and have also reported on the fabrication process of etched multilayer EUV mask, in which line and space mask patterning has been demonstrated. And by using etched multilayer EUV mask, the reduction of mask 3D effects is experimentally demonstrated. In our previous study, we have shown etched multilayer EUV mask has enough durability against chemical erosion in suitable cleaning process.

In this work, to meet the demands of different variation on pattern in etched multilayer mask, especially fabrication process for sub-60 nm pattern based on effective mirror width in dark-field exposure is studied. 60 nm pillar pattern on mask is obtained using negative tone resist with keeping resolution of line and space pattern. We also examined CD characteristics 60 nm line and space pattern in consideration of effective mirror width. This work represents that etched multilayer EUV mask is ready for dark-field exposure of 15 nm pattern in wafer.

Introduction

With shrinking pattern size at 0.33NA EUV lithography systems, mask 3D effects are estimated to become stronger, such as horizontal/vertical shadowing, best focus shifts through pitch and pattern shift through focus.[1] It was estimated that etched multilayer EUV mask is effective in reducing mask 3D effects at 0.33NA with lithographic simulation, and it was also experimentally demonstrated with NXE3300 EUV lithography system.[2] But it was also mentioned that mask error enhancement factor (MEEF) of etched multilayer EUV mask is unexpectedly larger than conventional EUV mask. And this implies that effective mirror width of etched multilayer pattern is smaller than physical pattern width measured by CD-SEM.

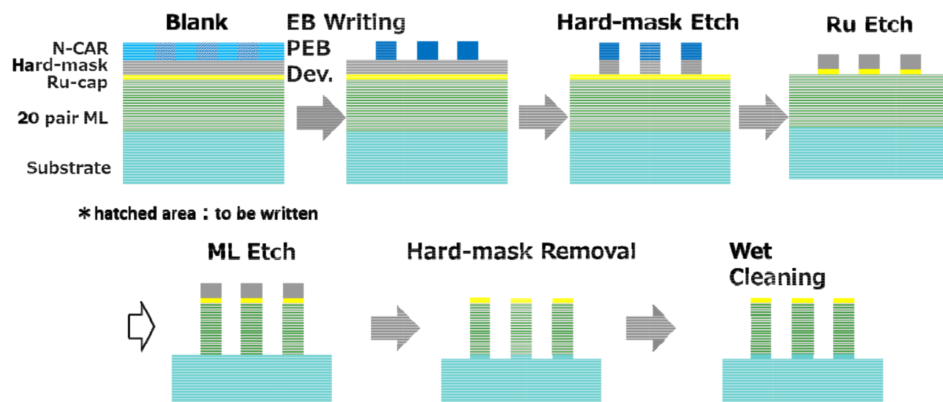

Figure 1. Process Flow.

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Editorial

Can we win EUVL Olympics?

Michael Watt, Shin-Etsu MicroSi Inc.
Artur Balasinski, Cypress Semiconductor Corp.

The Olympics have finished just a few months ago in Rio and I enjoyed watching many hours of great competition. A few weeks later while on a trip to Japan and with 14 hours to let my mind wander I began to think; what If we looked at the great semiconductor races for new technology introduction or market dominance from simple tasks to the future with EUV manufacturing, mask and pellicle production.

The question, how would some of these races and challenges compare in the Olympic arena.

The introduction of EUV is one of the most talked about subjects at all semiconductor conferences and the anticipated start is similar to holding your breath before the start of the 100 meters, when is the Usain Bolt moment that everyone wants to see? Will it be faster than we thought possible, better than before and dominate the scene for the foreseeable future? Maybe we are more like the Triathlon with multiple tasks needing to be completed amongst fierce competition. How would the marathon compare, continually having to look for something to give you more energy after a very long slog in years rather than hours.

The challenges of better power sources, mask development, pellicle design, software algorithms, uptime and availability, to name but a few. This must be the Decathlon of our business, continually having to search for more power the agility to change direction and sheer stamina to make it to the finish line.

One thing really different between the Olympics and the semiconductor races is that our disciplines do not wait for one moment of glory and, therefore, our races are by far less nerve-wrecking. Surely, we have our dose of adrenalin, but we do not bank everything on a performance lasting often less than a minute in a four-year cycle. We do not train for years and years for this one chance in a lifetime (OK, maybe two chances), to risk all this training for a day of upset stomach or a sprained muscle when that critical minute arrives. We are free to make poor decisions, and even stick to them for a long time, making a nice living all along. So, one result of this juxtaposition of the Olympics and the semiconductor business is that we are far more blessed. But while people would probably never lose their appetite to watch sports, making it a safe bet to compete in the Olympics (for those who are good enough to have that glorious moment and then deserve the everlasting glory), the patience to wait for the improved lithography systems is running thin, and the fans can be soon relegated to the basement. When we read about 200 mm fabs staging their comeback and the IoT products requiring more firmware than silicon support, we know EUVL needs to hurry, or it may not only not win, but even not make it to the finish line.

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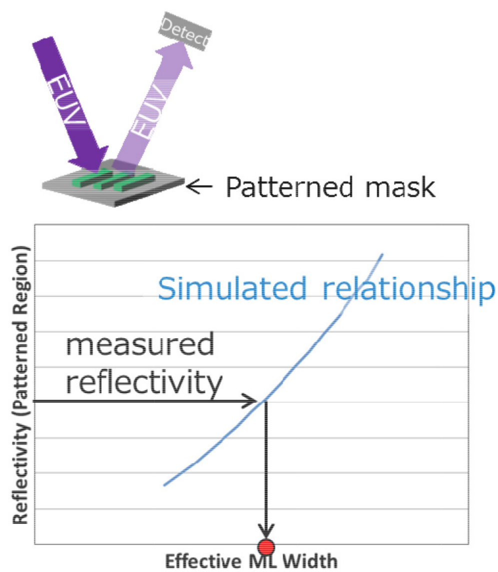

Figure 2. EUV reflectivity-based measurement.

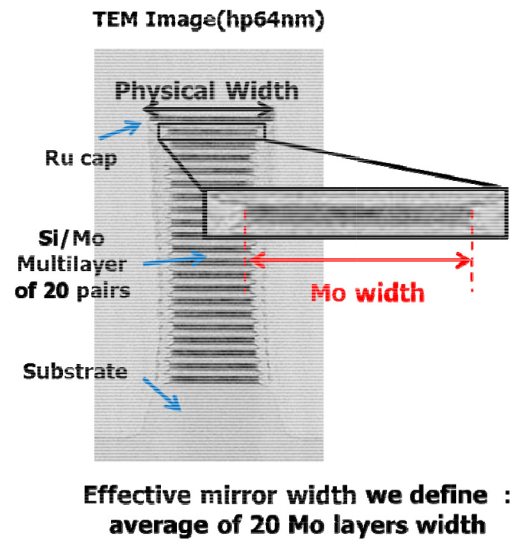

Figure 3. CD measurement form TEM image.

We have showed cross-sectional TEM image of etched multilayer EUV mask pattern, and there is silicon oxide film along the pattern sidewall as a passivation film. This is what makes the difference between physical pattern width and effective mirror width made up of Si/Mo multilayer width.[3],[4] It is necessary to consider the effective mirror width because our previous discussion of mask CD was based on physical width measured by SEM.

In order to obtain the fidelity of pattern, we designed pattern based on effective mirror width. That is, we apply mask bias equal to side wall film width to writing data. We have demonstrated dense pillar 72 nm or less collapsed using positive tone resist, but from the purpose of fabricating etched multilayer EUV mask for dark-field exposure, negative tone resist which leads to smaller writing area is better choice. Because of smaller writing area, negative tone resist process has lower writing time and less scattering electrons, which generate better pattern profile of resist.

In this work, we demonstrate a fabrication of 60 nm (15 nm on wafer) pattern in etched multilayer EUV mask using negative tone resist and evaluated etched multilayer EUV mask pattern based on effective mirror width.

2. Experimental Setup and Condition

2.1 Process flow

Fig.1 shows the process flow of etched multilayer mask. In order to fabricate fine multilayer pattern, hard-mask process is selected. 20-pair of Si/Mo multilayer, Ru-cap layer and hard-mask material are serially stacked on a substrate. Negative tone resist that is chemical amplifier resist (N-CAR) in this work on hard-mask is exposed by EB writer, and desired pattern of negative tone resist is generated after Post Exposure Bake (PEB) and pattern development process. The pattern is transferred to hard-mask and Ru-cap layer and multilayer are serially etched using patterned hard-mask. Finally hard-mask is removed and mask cleaning process is carried out.

2.2 Measuring methods of effective mirror width

In this work, we use two measuring methods of effective mirror width, one is EUV reflectivity-based measurement method and the other is measurement from TEM image. Since TEM image is not able to measure whole mask pattern, we also us EUV reflectivity-based measurement to evaluate pattern distribution in whole mask.

EUV reflectivity-based measurement is one of the model-based method and the essences of this method are noted below;

- Measuring EUV reflectivity of patterned area.
- Fitting to simulation result.
- Estimation of effective width.

EUV reflectivity is measuring method of no patterned surface using EUV light generically. In this work, multilayer lines at equal interval are patterned and EUV reflectivity of patterned area is measured. On the other hand, reflectivity simulation is carried out to obtain the relationship between effective mirror width and reflectivity of patterned area. By comparison of measured reflectivity and simulated relationship, the effective mirror width is estimated. A relationship between estimated width by this method and multilayer width is illustrated in Fig.2. It has been shown that estimated effective mirror width is well matched as effective mirror width from TEM imaging.[5]

We also use TEM image to measure the effective mirror width. Fig.3 shows our CD measurement from TEM image, and we defined that effective mirror width from TEM image is the average of 20 Mo layers width. In this TEM image, there are gray and black layers in cross-sectional multilayer pattern. We detected gray layers is silicon and black layers is molybdenum. And there is silicon oxide film along the pattern sidewall as a passivation film.

3. Results and Discussion

3.1 Pattern resolution results after cleaning

Fig.4 shows the pattern resolution results after cleaning using positive tone resist and negative tone resist by top-view SEM observation. Blue box means pattern is resolved, and red box means pattern is not resolved perfectly. The designed width on mask is in the row, and each item in the column indicates pattern categories; dense pillar, line and space, isolated line, and isolated space. Isolated line is designed that the pattern width ratio of line to neighboring line is 1:10. Isolated space is designed as inverted isolated line. Fig.5

·Positive tone resist (previous work)

Designed width	160	120	100	80	72	68	64	60	56	52	48	44	40
densePillar	OK	OK	OK	OK	NOT OK	NOT OK	NOT OK	NOT OK	NOT OK	NOT OK	NOT OK	NOT OK	NOT OK
LS	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
Iso Line	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	NOT OK	NOT OK	NOT OK
Iso Space	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK

Designed width: mask bias = 0 nm

···OK

···NOT OK

·Negative tone resist

Designed width	160	120	100	80	72	68	64	60	56	52	48	44	40
densePillar	OK	OK	OK	OK	OK	OK	OK	OK	OK	NOT OK	NOT OK	NOT OK	NOT OK
LS	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
Iso Line	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
Iso Space	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	NOT OK	NOT OK	NOT OK

Improvement

Figure 4. Pattern resolution results after cleaning.

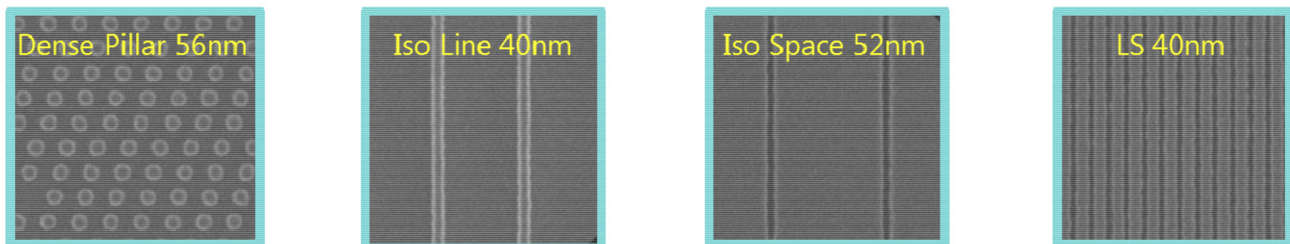

Figure 5. Top-view SEM images of pattern using negative tone resist after cleaning.

shows top-view SEM images of pattern using negative tone resist after cleaning.

56 nm dense pillar pattern using negative tone resist is obtained with zero mask bias even after cleaning. That is clear improvement in pillar pattern resolution comparing with positive tone resist we previously evaluated keeping resolution of line and space pattern.

3.2 CD characteristics based on effective mirror width

We examined CD characteristics of etched multilayer EUV mask pattern in consideration of effective mirror width. Fig.6 shows CD uniformity of etched multilayer EUV mask in whole area of 6 inch mask, and CD uniformity of hp60 nm line and space in the effective mirror width is 2.0 nm (3sigma) and effective mirror width from EUV reflectivity is 58.2 nm. This CD uniformity is derived from simulation based EUV reflectivity. CD uniformity catches up the target at 2016 < 2.2 nm (from ITRS2013) also in effective mirror width.

3.3 Etched multilayer EUV mask profile of 60 nm pattern

Fig.6 shows the SEM images of 60 nm pillar pattern based on effective mirror width. 60 nm pillar pattern is obtained without collapse even after cleaning process. Effective mirror width of this 60 nm pillar pattern is 59.7 nm from TEM image.

Summary

60 nm pillar pattern on mask is obtained using negative tone resist with keeping resolution of line and space pattern. We examined CD characteristics of etched multilayer EUV mask pattern in consideration of effective mirror width. CD uniformity of 60 nm line and space pattern is 2.0 nm at 3sigma and mean CD of it is 58.2 nm. And mean CD of 60 nm pillar pattern is 59.7 nm. Fabrication process for sub-60 nm pattern based on effective mirror width of etched multilayer EUV mask is ready for dark-field exposure.

Acknowledgement

The authors would like to thank Toshiba colleagues; Yukiyasu Arisawa for providing simulation results of EUV reflectivity and discussions, Rikiya Taniguchi for the discussion of mask metrology tools and his measurements.

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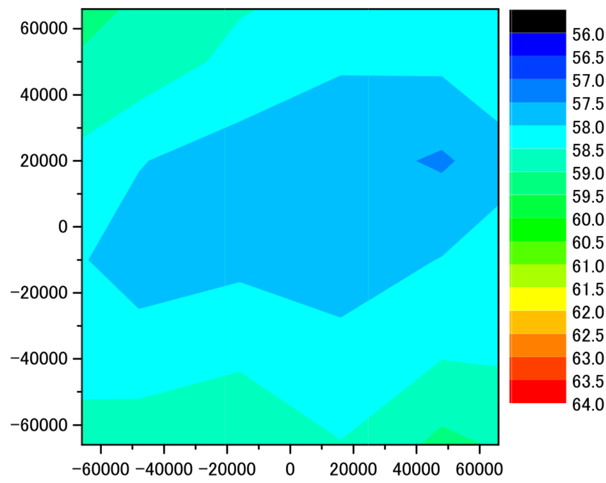
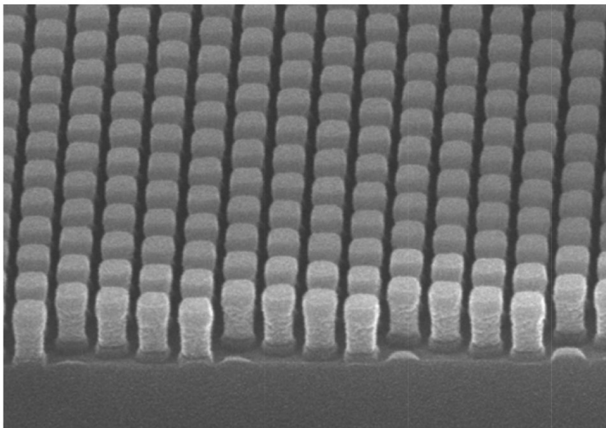
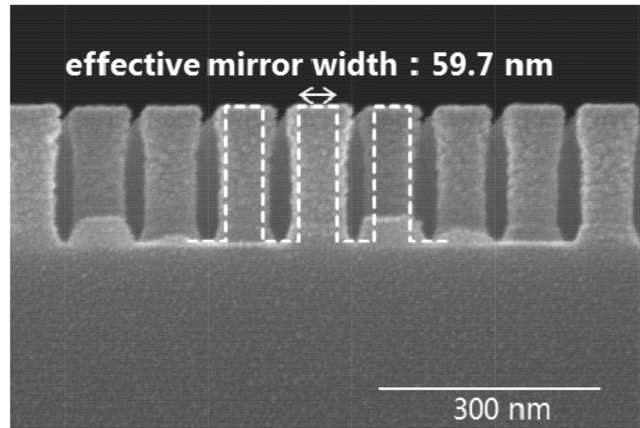


	Target @2016	Current capability
CD Uniformity	≤ 2.2 nm	2.0 nm

Figure 6. CD uniformity of hp 60nm line and space.



(a) bird's eye view



(b) cross-sectional image

Figure 7. SEM images of 60nm pillar patter.

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Industry Briefs

200mm Fabs on the Rise

Solid State Technology

One year after the debut of the industry's first 200mm Fab Outlook report, SEMI has issued an October 2016 update, with the report forecasting 200mm fab trends out to 2020. SEMI's analysts updated information on almost 200 facilities, including new and closures of existing facilities. The highest level of 200mm capacity was recorded in 2007 and the lowest following this peak in 2009. The capacity decline was driven by the 2008/2009 global financial crisis, which caused the closure of many facilities, and the transition of memory and MPU fabrication to 300mm fabs. Since 2009, installed 200mm fab capacity has increased, and by 2020, 200mm capacity is expected to reach 5.5 million wafers per month (wpm), though still less than the 2007 peak. According to SEMI's data, by 2019, installed capacity will reach close to 5.38 million wpm, almost as high as capacity in 2006. From 2015 to 2020, 200mm facilities are forecast to add 618,000 wpm net capacity.

Two applications account for the growing demand for 200mm: mobile devices and IoT. Rising fab capacity from 2015 to 2020 will be driven by MEMS devices, Power, Foundry and Analog. By region, the greatest increases in capacity are expected to be in China, Southeast Asia, Americas, and Taiwan. Another trend is also observed: 200mm fabs are increasing the capacity to provide process capability below 120nm. Higher capacity does not mean more fabs, but fewer, larger fabs. In fact, the number of fabs in 2020 is almost the same as the count seen in 2009. So 2020 capacity heads toward industry highs while in comparison 2009 had the lowest levels off the 2007 peak.

http://electroiq.com/

EUV Lithography A Double Whammy For Intel Corporation Stock

Piyush Arora

What Is EUV Lithography?

We have seen several node shrinks over the past decade, where each iteration delivered promising performance, efficiency and power gains. But we have arrived at a point where shrinking nodes further, beyond 10nm, requires sizable investments, with little performance gains to show for. So it's just not feasible anymore to keep up with node shrinks if chips are manufactured the conventional way.

Speculative reports suggest that chips manufactured using EUV lithography are up to 100 times faster than their conventional counterparts. Whether this claim is true, still remains to be seen. But the next-gen EUV lithography won't defy the laws of physics. The concerning thing for Intel is that the chipzilla was earlier hoping to manufacture 10nm chips using EUV lithography next year. None of its competitors had such an aggressive timeline. But Intel is now looking to deploy EUV lithography at the 7nm node. Samsung, Taiwan Semiconductor and GlobalFoundries plan to introduce EUV lithography along the same timeline as well. And without the EUV advantage, Intel would pretty much be at par with its competitors in terms of chip fabrication technologies. Its manufacturing lead would shrink to nothing.

Deploying EUV lithography is an expensive activity, with each alpha tool costing as much as $100 million. Intel is believed to have already spent $1 billion as of April last year on these tools. Intel ramped up these purchases in the hope of deploying the next-gen technology commercially next year. With the delay of 2 years, Intel would not be generating any returns out of its expensive equipment. It's non-cash depreciation expenses would continue to pile up over the next 2 years, causing a drag on its profitability, without seeing a single dollar in revenue. So this could particularly hurt Intel's bottom-line.

Secondly, with Intel's manufacturing lead shrinking over the next few years, ARM-based server offerings could pick up steam. Qualcomm, AMD and Cavium would get access to same EUV lithography, at the same nodes, by 2019, which could theoretically bring the performance of their chips close to Intel Xeons. So Intel may struggle to curb the growth of ARM-based offerings in the server space, leading to a loss of the revenue and profits.

Putting it all together

Intel has delayed the deployment of a technology that would have potentially aided in retaining its manufacturing lead. Now, multiple companies will have similar chip fabrication technologies by 2019-20. This would be bad for Intel, both operationally and financially. It needs to get its house in order if it wants to curb the growth of its competition.

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The 24th Symposium on Photomask and NGL Mask Technology
5-7 April 2017
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Yokohama, Japan

The 33rd European Mask and Lithography Conference EMLC 2017
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