PHOTOMASK

BACUS—The international technical group of SPIE dedicated to the advancement of photomask technology.

BACUS NEWS

NOVEMBER 2014
VOLUME 30, ISSUE 11

1st Place Best Poster - PM14

Efficient Model-Based Dummy-Fill OPC Correction Flow for Deep Sub-Micron Technology Nodes

Ayman Hamouda and Mohamed Salama, GLOBALFOUNDRIES Inc., **Hopewell Junction, NY 12533**

ABSTRACT

Dummy fill insertion is a necessary step in modern semiconductor technologies to achieve homogeneous pattern density per layer. This benefits several fabrication process steps including but not limited to Chemical Mechanical Polishing (CMP), Etching, and Packaging. As the technology keeps shrinking, fill shapes become more challenging to pattern and require aggressive model based optical proximity correction (MBOPC) to achieve better design fidelity. MBOPC on Fill is a challenge to mask data prep runtime and final mask shot count which would affect the total turn-around time (TAT) and mask cost. In our work, we introduce a novel flow that achieves a robust and computationally efficient fill handling methodology during mask data prep, which will keep both the runtime and shot count within their acceptable levels. In this flow, fill shapes undergo a smart MBOPC step which improves the final wafer printing quality and topography uniformity without degrading the final shot count or the OPC cycle runtime. This flow is tested on both front end of line (FEOL) layers and backend of line (BEOL) layers, and results in an improved final printing of the fill patterns while consuming less than 2% of the full MBOPC flow runtime.

Introduction

Design scaling is one of the most critical goals in the Semiconductor technology. This is becoming very challenging in the deep submicron nodes, where the design-to-wafer fidelity cannot be achieved without applying very aggressive Resolution Enhancement Techniques (RET) and Optical Proximity Correction (OPC) flows. This has been a key factor in achieving this amazing success story of continued exponential scaling.[1] As the photolithography approaches its physical limits, the patterning quality degrades where such a loss of image quality in optical lithography erodes the design-to-wafer fidelity on silicon. To extend the lifetime of optical lithography, integrated circuit (IC) manufacturers have been seeking all possible techniques to enhance the resolution of existing

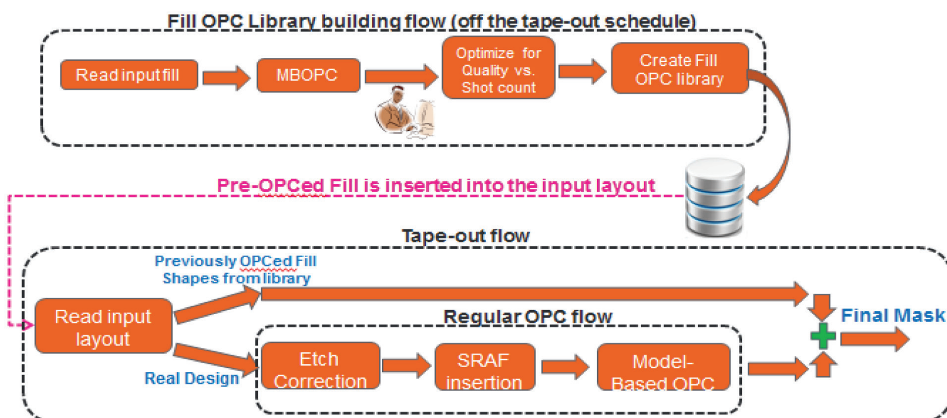

Figure 1. A block diagram describing the reference Dummy Fill flow, where the fill process compensation is done offline from the actual tape-out flow through feedback from OPC and process teams.

TAKE A LOOK INSIDE:

INDUSTRY BRIEFS —see page 8

CALENDAR For a list of meetings —see page 9

SPIE.

9235-65

Editorial

Few Words to Remember a Dear Friend ...

Frank E. Abboud, Bacus President

We at the SPIE Photomask BACUS community would like to extend our deepest sympathy to Oliver's family and friends and offer our condolences. He has touched each and every one of us in a special way. Through his work and dedication he advanced the Mask making industry and established the foundation for the next generation lithography. Through his interactions he demonstrated true partnership and professionalism that made every interaction pleasant, meaningful and truthful. We will miss him.

Below are some of Oliver's accomplishments and the footprint he left on this planet and our mask making world.

Born in Wiesbaden/Germany, Oilver Kienzle studied physics at the Technical University of Darmstadt and earned his doctorate in electron microscopy at the Max Planck Institute for Metal Research in Stuttgart/Germany.

Oliver joined the ZEISS Group in 1999. He initially worked in the former Lithos GmbH as Project Manager for electron projection lithography. After transferring to LEO GmbH, he switched to the field of electron optics for high throughput wafer inspection, which resulted in the Advanced E-Beam Modules (AEM) field of business. He had been the Managing Director of the strategic Semiconductor Metrology Systems (SMS) business unit of ZEISS since 2004. His division at ZEISS develops, manufactures, and sells equipment for photomask manufacturing and the semiconductor industry.

Working untiringly to move Carl Zeiss SMS GmbH forward, Oliver built over many years the high standing and reputation of the company among customers and partners around the globe. With his expertise and experience, his poise and strong personality, he brought about sustained success and made a great contribution to ZEISS as well as the semiconductor industry.

Beside his dedication to his job and to ZEISS Oliver loved to go fly-fishing. When he was only six years old, he received his first fishing rod. This marks the beginning of Oliver's passion, which had not stopped ever since. His another favorite occupation was photography. Oliver was passionate about the search for a matching photo motif. He collected objective lenses and guarded them jealously. The large amount of various pictures document the technophile life of Oliver and leave a lasting memory.

Dr Oliver Kienzle, Managing Director of Carl Zeiss SMS GmbH (SMS). He died unexpectedly on 27 September 2014 at the age of 49.

N • E • W • S

BACUS News is published monthly by SPIE for BACUS, the international technical group of SPIE dedicated to the advancement of photomask technology.

Managing Editor/Graphics Linda DeLano
Advertising Lara Miles
BACUS Technical Group Manager Pat Wight

■ **2014 BACUS Steering Committee** ■

President
Frank E. Abboud, *Intel Corp.*

Vice-President
Paul W. Ackmann, *GLOBALFOUNDRIES Inc.*

Secretary
Bryan S. Kasprowicz, *Photronics, Inc.*

Newsletter Editor
Artur Balasinski, *Cypress Semiconductor Corp.*

2014 Annual Photomask Conference Chairs
Paul W. Ackmann, *GLOBALFOUNDRIES Inc.*
Naoya Hayashi, *Dai Nippon Printing Co., Ltd.*

International Chair
Uwe F. W. Behringer, *UBC Microelectronics*

Education Chair
Artur Balasinski, *Cypress Semiconductor Corp.*

Members at Large
Paul C. Allen, *Toppan Photomasks, Inc.*
Michael D. Archuletta, *RAVE LLC*
Peter D. Buck, *Mentor Graphics Corp.*
Brian Cha, *Samsung*
Glenn R. Dickey, *Shin-Etsu MicroSi, Inc.*
Brian J. Grenon, *Grenon Consulting*
Thomas B. Faure, *IBM Corp.*
Jon Haines, *Micron Technology Inc.*
Mark T. Jee, *HOYA Corp, USA*
Patrick M. Martin, *Applied Materials, Inc.*
M. Warren Montgomery, *The College of Nanoscale Science and Engineering (CNSE)*
Wilbert Odisho, *KLA-Tencor Corp.*
Michael T. Postek, *National Institute of Standards and Technology*
Abbas Rastegar, *SEMATECH North*
Emmanuel Rausa, *Consultant*
Douglas J. Resnick, *Canon Nanotechnologies, Inc.*
Thomas Struck, *Infineon Technologies AG*
Bala Thumma, *Synopsys, Inc.*
Jacek K. Tyminski, *Nikon Research Corp. of America (NRCA)*
Jim N. Wiley, *ASML US, Inc.*
Larry S. Zurbrick, *Keysight Technologies, Inc.*

SPIE.

P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 360 676 3290
Fax: +1 360 647 1445
www.SPIE.org
help@spie.org

©2014

All rights reserved.

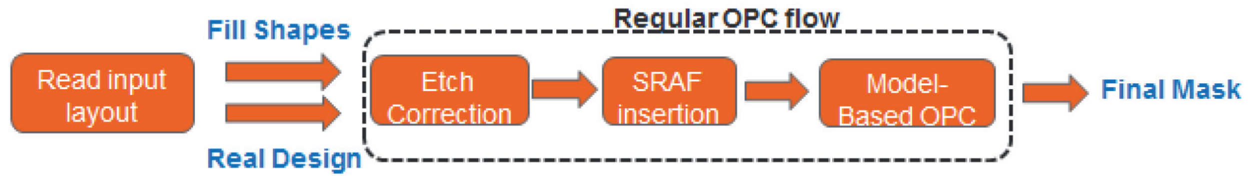

Figure 2. A block diagram describing a full-MBOPC flow, where the Dummy Fill is treated in the same manner as the actual circuit design.

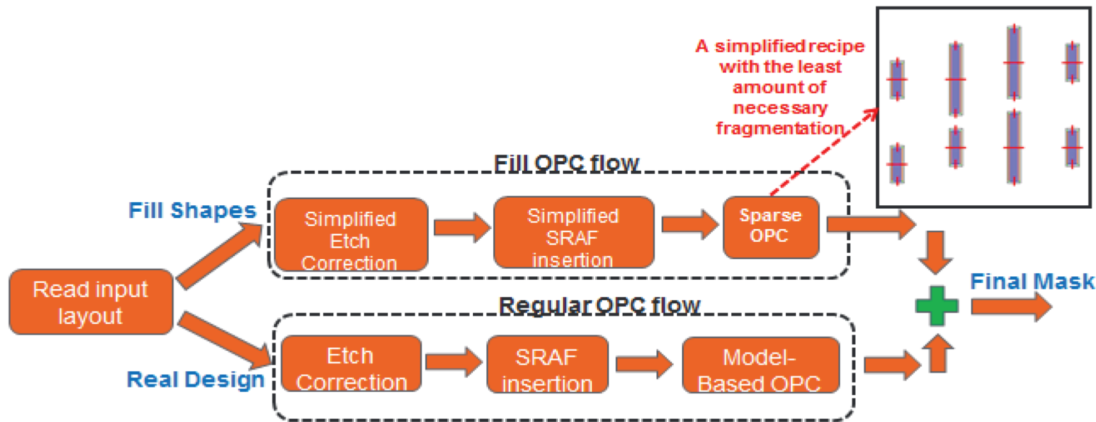

Figure 3. A block diagram describing a proposed MBOPC flow for the simultaneous correction flow for both regular design and fill handling.

systems. These techniques include using aggressive illumination, and compensating for all pattern transfer nonidealities at the mask level by applying OPC.[2,3]

Dummy-fill patterns are used to achieve a narrow density distribution on the wafer which will promote uniformity during chemical mechanical polishing (CMP) and etch.[4-6] Such processes are sensitive to local-density variations and can induce variations in both the polishing rate and the etch rate, resulting in a potential CD variation in both the lateral and the vertical dimensions. Dummy fill structures are just passive features that don't play any role in the actual circuit operation. Their main purpose is to adjust the pattern-density in specific regions of the layout that need some density increase.

In older lithography technologies, the dummy-fill feature size was larger and didn't require much correction. Only a simple bias is good enough to ensure the fill printability with a reasonable CDU. However, for the advanced semiconductor technology node such as 14 nm or beyond with their lower k1 factor, the dummy pattern design becomes challenging to print and requires more sophisticated methodologies to achieve its maximum benefit. There are design-styles for dummy fill patterns depending on their application (and proximity to actual designs). The CFILL (Customized Fill)[7] is intended for tight areas available between design spaces, where it looks very similar to the actual designs at minimum feature CDs and it needs full attention like any actual electrical design. The variation of the CFILL shape could alter both the physical and the electrical characteristics of the neighboring devices.[8,9] On the other hand, the conventional FILL is still regular and until recently it didn't need any sophisticated intervention from the OPC during tape-out. In this work, we study the necessity of model-based OPC processing for Fill Shapes, and its challenges in 10nm gate and triple patterning metal designs. We propose a new fill handling flow during tape-out that considers important metrics to the tape-out flow such as the CD Uniformity, runtime and shot count.

Model-Based Fill Handling Flow for Advanced Technology Nodes

It is of high importance to provide advanced nodes with better accuracy in fill patterning. This is particularly important near the fill-to-design transitions. The current FILL flow doesn't give the designer enough insight about what the final printing size would be, how it will be affected due to process tweaks in the fab or even due to minor design adjustments that the designer sees as necessary. Although the original intention of the reference FILL flow (Figure 1) is to provide a simple straight forward solution to the problem, it lacks three very important aspects, which are 1) the ability to control the dummy fill final printing CDs especially at fill-to-design boundaries (which are actually the most important for the designers where it is the most effective in the parasitic extraction calculations), 2) the flexibility of the dummy-fill design-update process without requiring many design-simulation iterations between the designer and the Fab's OPC and DFM groups to design their fill updates to the final (on wafer) sizes, and 3) 10nm fill designs (as we will show in a coming section) requires Sub-Resolution Assist Features (SRAFs) insertion to improve CDU. SRAF insertion parameters are tied closely to the process parameters and it's more convenient to shift it to the Fab's tape-out operations than to perform it during the FILL insertion at design stage

However, there are several advantages of the reference dummy-fill insertion flow that are really important. First, in this flow, the mask design is done offline from the tape-out flow, which means that it consumes almost no computation runtime (except for simply writing the fill to the output OPC layout file). This is a very nice benefit in any tape-out, where the fill design represents a reasonable percentage of the chip design (especially in the early phases of technology development and product prototyping). The second main advantage is the Mask shot count, where with the reference dummy-fill insertion flow the designers do not really have any moving fragments (like in OPC) that result in a big increase in the

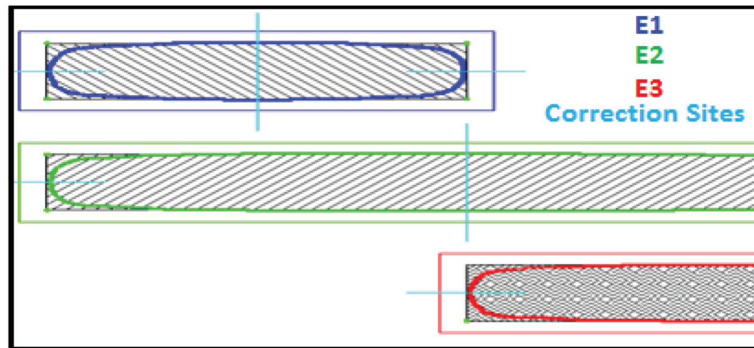

Figure 4. a 10nm-Node Dummy-Fill Print Image showing that a single site/edge Sparse OPC is good enough for achieving the required design fidelity.

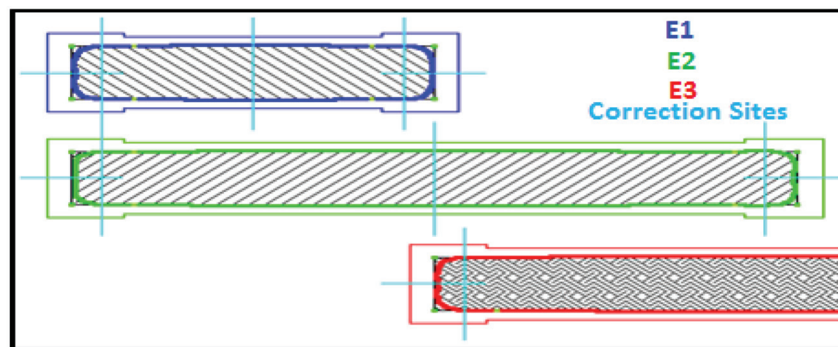

Figure 5. A 10nm-Node Dummy-Fill Print Image with a single fragment at corners showing that good design fidelity can be achieved with simplified Sparse OPC recipe but at the expense of an increased shot count.

shot count during the mask manufacturing and directly affecting the mask writing time and cost.[10] In addition, there are other advantages among which we list the simplicity of the flow and the simplicity of its implementation.

In summary, it is important that any dummy-fill handling flow would consider the following points

- Mask Tape-out runtime.
- Mask shot count.
- Its ability to achieve accurate Final Fill CDs (everywhere).
- The simplicity of the Fill-design process. And the ability to decouple the fill design from the Fill Mask shapes.
- The flexibility it provides to the designers in designing and updating their fill.

Figure (2) shows another option for a different flow for the dummy-fill handling, where it can achieve the best accuracy through applying full MBOPC handling to the dummy-fill. This could be very appealing from a final dummy-fill printing CD accuracy and the design flexibility points of view. However, the cost for this approach is very high from a Fab's operational point of view (tape-out time) as well as the definite increase in the Mask shot count due to such flow. If the fill features undergo the full MBOPC flow, then they are likely candidates to get multiple SRAFs and having complex (but not really necessary) OPC treatment which could easily blow the dummyfill shot count by an order of magnitude.

In this paper, we build our work on the points above and develop a new flow that focuses on improving the quality and the accuracy of the final dummy-fill printing CD while giving the designers and a Fab's customers the simplicity and flexibility in their fill design. This proposed flow, transfers the problem of the Mask creation process to the tape-out operations and OPC groups. Moreover, knowing that the shot count and the mask tape-out runtime are of great importance, we have developed a specific flow that has almost no effect on shot count and a very minor effect on runtime. Of course, as expected, this has to come at the expense of the necessity to build a more sophisticated flow that is capable of achieving such challenges.

Figure (3), shows the flow diagram of our proposal for an efficient and accurate Model-Based dummy-fill handling flow, where the fill still gets its Model-Based Handling and RET recipe (SRAF insertion) but through a parallel flow to the actual circuit design flow. This provides an added degree of freedom to handle the dummy-fill while still considering its own requirements. This new flow offers a big benefit, where it provides the opportunity to apply a less complex Model-Based RET and OPC recipe that can meet the needs of the fill patterning accuracy, while at the same time it respects the requirements of having a small runtime and small shot count. The FILL design is starting to look like a 90nm or 65nm design to some extent in terms of their dimensions, except for having a more regular design style and of course that it is being illuminated with an aggressive illumination that is needed for 20nm node and below. Using Aggressive off-axis illumination for such 65nm node dimensions suggests that SRAFs will be needed to support the fill CDU through process variations, which is another benefit for our proposed flow, where designers should never be burdened with the design of the SRAF solution as it is usually out of their scope and involves a lot of considerations among which is the process improvement margins as well as the how to prevent

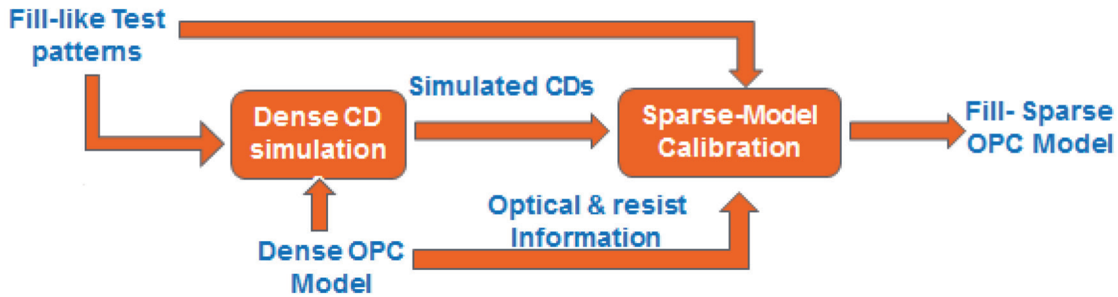

Figure 6. Dummy-Fill Sparse OPC model Calibration flow.

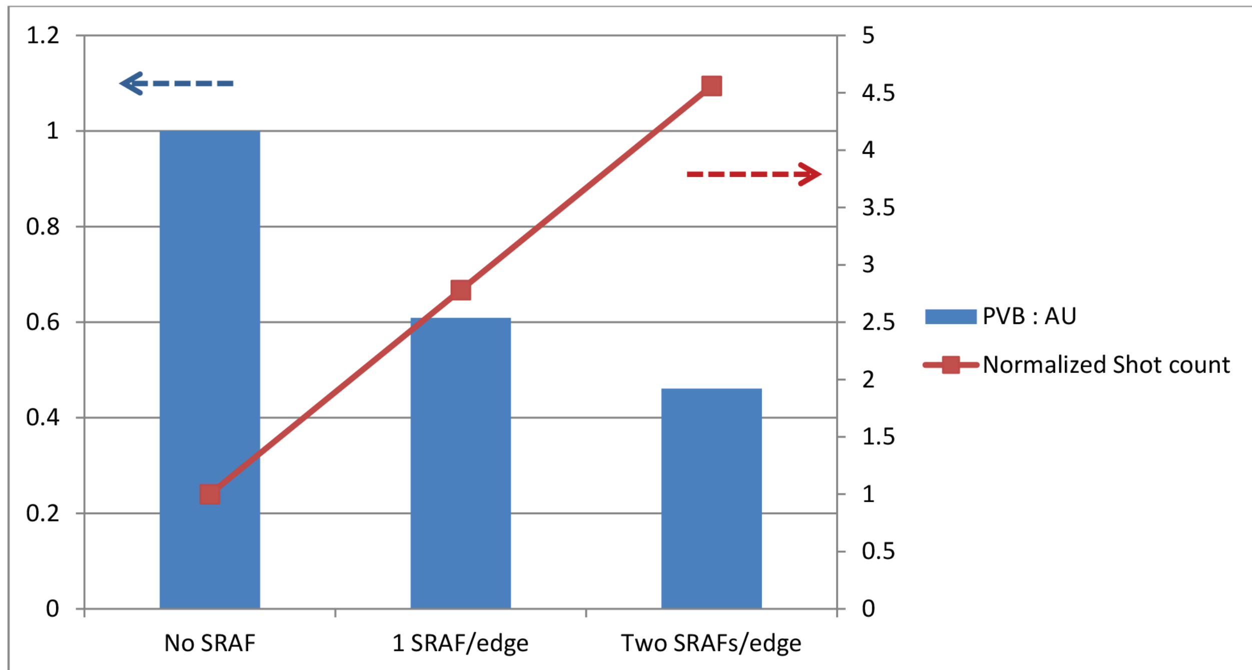

Figure 7. Process Variation bands (PVBand) width for different dummy-fill SRAF solutions and the normalized shot count increase associated with every solution.

their printability.

The actual runtime and shot count benefit comes from the ability to use a separate sparse OPC engine in the dummy-fill mask correction. Sparse OPC is known to save a lot of simulation runtime by just focusing on simulation only at the location of interest rather than simulating a full grid. Thus, transforming dummy-fill mask correction into a sparse solution would save a lot of time because it is more suitable to the fill design size and density.

Moreover, to be more careful about the mask shot count, it is possible to create a specific fill-OPC recipe that focuses on maintaining the rectangular shapes of the dummy-fill on the final mask. This is a crucial condition to minimize the mask shot count because every single break to the fill edges contributes to the overall shot count of the mask. Accordingly, it is a recommended option in the fill-OPC recipe to use a single fragment-per-edge concept, where the model is going to drive towards a zero EPE only at the center of the fragments/edges. This has a dual benefit, where it maintains the shot count to meet the same performance of the regular FILL flow as well as significantly reducing the number of simulation sites for the OPC simulation. This can further reduce the correction runtime. Figure (4) shows the print simulations for a 10nm metal fill; it is obvious that it can still print well enough even with a single OPC correction site per edge.

Even for situations where More aggressive Line End solutions for the fill is desirable, it is still possible to have a slightly more aggressive correction recipe that allows additional fragments at the corners and line-ends that will enable the creation of hammer heads for the OPC solution and accordingly achieve a better design fidelity as shown in figure (5).

In order to implement this new flow, it is essential to create a sparse OPC model that represents the lithography process as well as making sure that it covers the dummy-fill design-space well. Figure (6) shows the sparse model calibration flow, where the standard dense OPC model is used as a reference. This flow is selected because it enables a unified OPC verification strategy and possible inter-learning between actual-design OPC and the dummy-fill OPC recipes). This flow constitutes a few simple steps that are grouped together to create an automated dense-to-sparse model conversion. First, the simplified test patterns that are fully covering the dummyfill design space (i.e. the proper mask sizes, pitches and Line-End spacing). Second, these fill-mask shapes are simulated using the production dense OPC model and critical

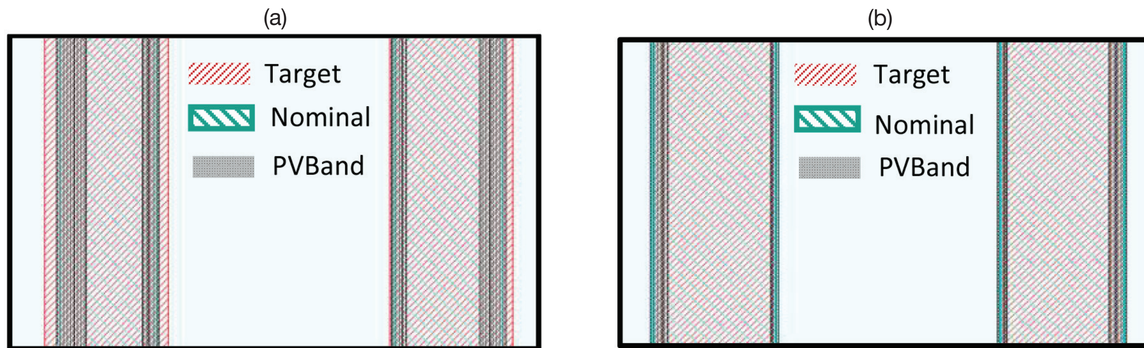

Figure 8. dummy fill printability at the edge of the array, (a) reference dummy-fill handling flow. (b) Single-site-per-edge sparse MBOPC. The nominal Contour accuracy has improved with the proposed flow and showing better fidelity to target. PVBands also have improved with the new flow, where the SRAF placement at the edge of the array is better tuned.

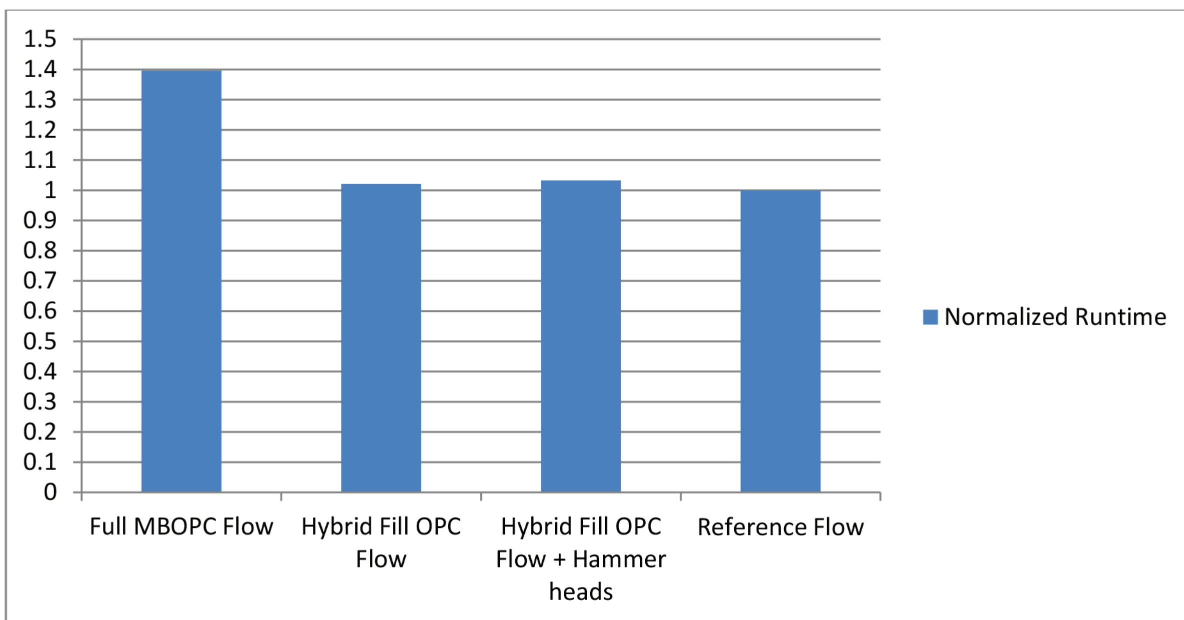

Figure 9. Normalized OPC runtime comparison for different dummy-fill handling flows.

calibration measurements are collected. Finally, these new simulation measurements are fed into the sparse model calibration step that focuses on producing predictions that are as close as possible to what the standard MBOPC flow would predict.

Experimental Results

Advanced nodes, (especially 10nm and beyond) are showing the need to apply efficient but accurate MBOPC solutions to achieve the necessary density and CD uniformity specs. Simplifying the design flow is also very desirable, where the designers need to focus only on their final (on wafer) CDs, while shifting the printability improvement (through both RET and OPC) to the Fab's tape-out process. In this work, we focus on two very critical layers of the 10nm node. The gate and metal layers are chosen for this experiment, where they require precise CDU, and the accurate printing of the dummy features to enable good control of both etch and CMP processes.

Figure (7) shows the SRAF insertion assessment for the dummy-fill feature, where both the process variation bands (PVBands) improvements as well as the shot count increase are shown simultaneously. It is obvious that as the number of SRAFs increase, the patterning immunity against process variation gets better (smaller PVBands). However, this comes as a trade off with the mask shot count, where instead of having a single fill polygon to be patterned on the mask; there will be even more associated SRAFs polygons to it. The results shown in Figure (7), suggest that a single SRAF solution is necessary to meet the required patterning robustness for the fill shapes. Any increase in the number of SRAFs is possible, but would come at the expense of shot count.

Figure (8) shows the printing accuracy at the edge of the array for the gate layer with (a) the reference dummy-fill handling flow compared to (b) our proposed single-site/edge sparse OPC dummy fill handling flow. It can be clearly observed how the MBOPC was necessary to capture the proximity effects and correct for them. It also confirms that the single-site sparse MBOPC solution is capable of capturing the proximity variations and correcting them using the minimum computation power. The improvement in the PVBands is related to better SRAF placement and due to better (accurate and larger) CD at the edge of the array.

The most obvious advantage for the proposed flow appears clearly when we compare the computational efficiency of the new flow against the full MBOPC fill-correction flow. There is virtually no increase in the overall runtime during the tape-out flow. This is a huge benefit, where being able to properly handle and correct the fill (as well as the proper SRAF insertion, which is a huge

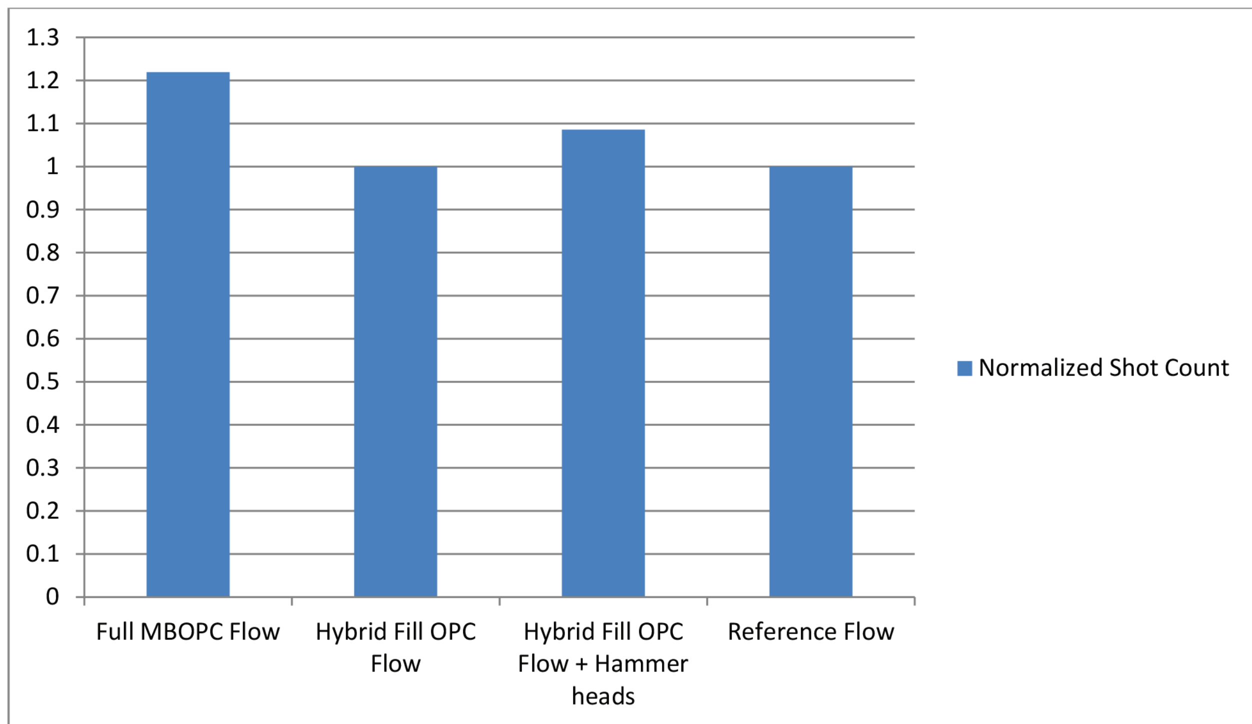

Figure 10. Normalized Mask shot count comparison for different dummy-fill handling flows.

challenge for the designers to do it offline) for almost no runtime cost is a great support to the fab tape-out operations. Figure (9) shows how the runtime for both the gate and metal levels didn't increase by more than a 2% of the runtime compared to the reference flow, while applying a full dense MBOPC solution (i.e. the same handling as the standard design) could consume up to 40% more in runtime (this value varies from a chip to another as the fill percentage starts as a larger percentage of the total chip area in the early development stages and then drops to smaller percentages as the technology reaches mature production phase).

The last important factor is the shot count comparison between the different flows. Figure (10) shows the normalized shot count for all three flows. It is obvious that there is a shot count increase (~ 22% increase) if we go to the full MBOPC handling of the fill (where the fill is treated as if it is a regular design that needs full correction), while with our proposed flow there is absolutely no increase in the shot count compared to the reference flow.

Conclusion

In this work, we revisit the fill handling strategies in the mask tape-out flow for the 10nm node. The fill dimensions are getting small enough that it requires both SRAF support and MBOPC handling to achieve the necessary design fidelity and CD control. This is very important to achieve lateral and vertical CD uniformity of the active design features. We have proposed a new flow that allows applying an independent dummy-fill correction to achieve the necessary fill CD uniformity, while keeping the mask shot count the same with only a limited increase in the computation runtime during the tape-out flow (<2%). This flow also offers the simplification of the fill-design process as it is becoming extremely complex, especially with the potential need for the SRAF support to pattern the dummy-fill structures.

References

[1] Lars Liebmann, "DfM, the teenage years." **Proc. SPIE 6925,** 692502 (2008).

[2] Lars W. Liebmann, Jongwook Kye, Byung-Sung Kim, Lei Yuan, and Jean-Pierre Geronimi, "Taming the final frontier of optical lithography: design for sub-resolution patterning" **Proc. SPIE 7641,** 764105 (2010).

[3] Yan Borodovsky, "Marching to the beat of Moore's Law" **Proc. SPIE 6153,** 615301 (2006).

[4] GuoXiang Ning; Christian Buergel; Paul Ackmann; Marc Staples; Thomas Thamm; Chin Teong Lim; Andre Leschok; Stefan Roling; Anthony Zhou; Fang Hong Gn; Frank Richter, "Reticle and wafer CD variation for different dummy pattern" **Proc. SPIE 8522,** 85222J (2012).

[5] Norma Rodriguez; Jie Yang; Bill Graupp; Jeff Wilson; Eugene Anikin, "The complexity of fill at 28nm and beyond" **Proc. SPIE 8327,** 83270Q (2012).

[6] Liang Deng; Kai-Yuan Chao; Hua Xiang; Martin D. F. Wong, "Cell-based OPC with standard-cell fill insertion" **Proc. SPIE 6925,** 69251L (2008).

[7] Louis Lin; Wei-Long Wang; Sarah McGowan, "High-fidelity dummy fill printing with repair OPC" **Proc. SPIE 8880,** 88801K (2013).

[8] Usha Katakamsetty; Colin Hui; Li-Da Huang; Lannie Weng; Peter Wu, "Timing-aware metal fill for optimized timing impact and uniformity" **Proc. SPIE 7275,** 72751P (2009).

[9] Lei He; Andrew B. Kahng; King Ho Tam; Jinjun Xiong, "Design of integrated-circuit interconnects with accurate modeling of chemical-mechanical planarization" **Proc. SPIE 5756,** Design and Process Integration for Microelectronic Manufacturing III, 109 (2005).

[10] Ayman Yehia, "Mask-friendly OPC for a reduced mask cost and writing time" **Proc. SPIE 6520,** 65203Y (2007).

N • E • W • S

Sponsorship Opportunities

Sign up now for the best sponsorship opportunities

Photomask 2015 —
Contact: Lara Miles, Tel: +1 360 676 3290; laram@spie.org

Advanced Lithography 2015 —
Contact: Lara Miles, Tel: +1 360 676 3290; laram@spie.org

Advertise in the BACUS News!

The BACUS Newsletter is the premier publication serving the photomask industry. For information on how to advertise, contact:

Lara Miles
Tel: +1 360 676 3290
laram@spie.org

BACUS Corporate Members

Acuphase Inc.
American Coating Technologies LLC
AMETEK Precitech, Inc.
Berliner Glas KGaA Herbert Kubatz GmbH & Co.
FUJIFILM Electronic Materials U.S.A., Inc.
Gudeng Precision Industrial Co., Ltd.
Halocarbon Products
HamaTech APE GmbH & Co. KG
Hitachi High Technologies America, Inc.
JEOL USA Inc.
Mentor Graphics Corp.
Molecular Imprints, Inc.
Panavision Federal Systems, LLC
Profilocolore Srl
Raytheon ELCAN Optical Technologies
XYALIS

Industry Briefs

IBM Struck a Historic and Much-Anticipated Deal to Transfer its Chip Fabs to GlobalFoundries.

Rick Merritt, EE times

Snapshot of the deal:

* IBM will transfer its fabs and about $1.3 billion in cash to GlobalFoundries.
* GF also gets ownership of more than 10,000 IBM semiconductor patents
* No layoffs or plant closures are anticipated by either company.
* GF gets an exclusive 10-year deal to supply all IBM's 22, 14, and 10 nm chips.

The deal involves IBM's East Fishkill, N.Y., fab that makes about 15,000 wafers a month mainly in 45 and 32 nm silicon-on-insulator processes. The fab is also ramping the 22 nm process used to make IBM's Power 8 processors and has some 14 nm technology in development for the follow-on generation.

It also involves IBM's Burlington, VT, fab which makes 45,000 200 mm wafers per month. The fab uses a wide variety of processes, including a 130/180 nm SOI process for RF front-ends and switches used mainly in cellphones, and a 90 nm SiGe process, mainly for power chips for a wide range of high-end applications including car radars and high-frequency radios and testers.

UMC Joins Xiamen China Foundry

Rick Merritt, EE times

Taiwan's United Microelectronics Corp. will invest about US$1.35 billion over the next five years in a new foundry in Xiamen, China. The foundry will be a joint venture with a total investment of $6.2 billion, aimed at ramping to production of 50,000 12-inch wafers a month, using 55 nm and 40 nm process technologies.

UMC already owns 86.88% of HeJian Technology (Suzhou) Co., Ltd., a foundry that makes 8-inch wafers for customers in China and other Asian countries.

The Taiwan government prevents its foundries such as TSMC from transferring their latest process technology to China, said Bill McClean of IC Insights. That's likely why the new UMC joint venture will use relatively mature 55 and 40 nm processes.

Foundries use Small Feature Size to Boost Revenue per Wafer

IC insights

For TSMC and GlobalFoundries, the dominant fraction of the sales comes from the 28 nm node and below, whereas for UMC and SMIC, it comes from a mix of 40-65 nm processes. The focus on small CDs turns out to TSMC advantage.

Among the big 4 pure-play foundries, TSMC is forecasted to have the highest revenue per wafer in 2014 at $1328, 27% higher than GlobalFoundries. UMC's revenue per wafer in 2014 is expected to be only $770 (200mm equivalent). The revenue per wafer is expected to grow +4.3% for TSMC while decreasing almost 2.8% for UMC.

Join the premier professional organization for mask makers and mask users!

About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

Individual Membership Benefits include:

- Subscription to BACUS News (monthly)
- Eligibility to hold office on BACUS Steering Committee

www.spie.org/bacushome

Corporate Membership Benefits include:

- 3-10 Voting Members in the SPIE General Membership, depending on tier level
- Subscription to BACUS News (monthly)
- One online SPIE Journal Subscription
- Listed as a Corporate Member in the BACUS Monthly Newsletter

www.spie.org/bacushome

Calendar

2015

SPIE Advanced Lithography
22-26 February 2015
San Jose Convention Center
and San Jose Marriott
San Jose, California, USA
www.spie.org/al

SPIE Photomask Technology
Co-located with
SPIE Scanning Microscopies

September 2015
Monterey Marriott and
Monterey Conference Center
Monterey, California, USA

SPIE Scanning Microscopies
Co-located with
SPIE Photomask Technology

September 2015
Monterey Marriott and
Monterey Conference Center
Monterey, California, USA

SPIE is the international society for optics and photonics, a not-for-profit organization founded in 1955 to advance light-based technologies. The Society serves nearly 225,000 constituents from approximately 150 countries, offering conferences, continuing education, books, journals, and a digital library in support of interdisciplinary information exchange, professional growth, and patent precedent. SPIE provided over $3.2 million in support of education and outreach programs in 2013.

SPIE.
International Headquarters
P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 360 676 3290
Fax: +1 360 647 1445
help@spie.org • www.SPIE.org

Shipping Address
1000 20th St., Bellingham, WA 98225-6705 USA

Managed by SPIE Europe
2 Alexandra Gate, Ffordd Pengam, Cardiff,
CF24 2SA, UK
Tel: +44 29 2089 4747
Fax: +44 29 2089 4750
spieeurope@spieeurope.org • www.spieeurope.org

You are invited to submit events of interest for this calendar. Please send to lindad@spie.org; alternatively, email or fax to SPIE.