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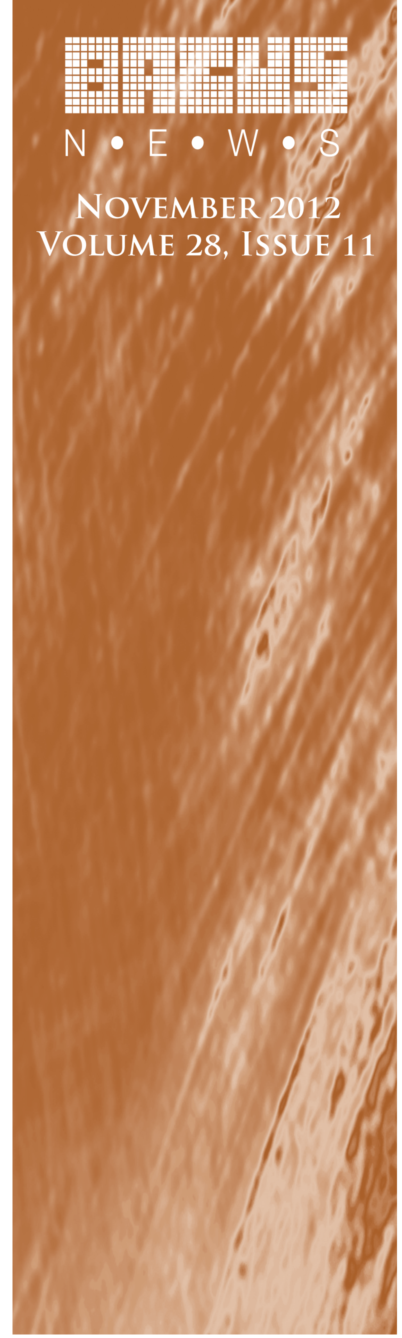

1st Place Best Paper Award - PM12

Future Mask Writers Requirements for the Sub 10 nm Node Era

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Abstract

Mask patterning capability continues to be a key enabler for wafer patterning. Mask writer performance is critical to meet reticle resolution, critical dimension uniformity, registration, and throughput requirements. Technology trends indicate that mask requirements will require higher dose resists with more complex designs producing write time growth that significantly exceeds Moore's law estimates. Sub 10 nm technology node requirements may exceed what is practically or economically achievable using conventional single beam writers. This is driving the need to explore alternative e-beam mask writer architectures for future nodes.

Several equipment suppliers are proposing new architectures for mask patterning. These approaches share the characteristic of some level of parallelism to solve the throughput challenge caused by increasing mask pattern complexity. Although parallelism is a proven approach in laser mask writers, it has not been integrated into an e-beam platform. All of the approaches for multibeam e-beam architectures have unique technical difficulties. In some cases, suppliers have produced proof of concept results to demonstrate the feasibility of their approach and address key technical risks. Although these results are encouraging, it is clear that they need more time and industry assistance to produce a commercially worthy mask writer.

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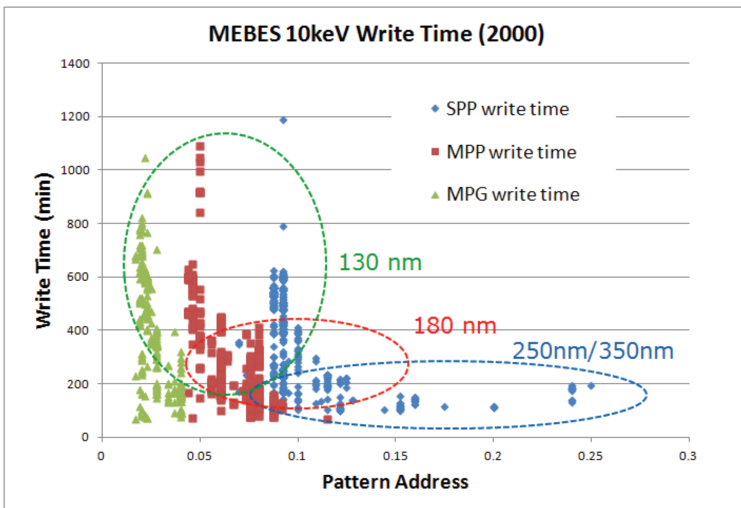

Figure 1. Write time trends of 10keV MEBES raster Gaussian beam mask writer. For a given write node, write time increases by 1/(WAU)². Supplier developed new write modes, MPP/MPG which operated on 2x/4x of the pattern grid allowing the platform to be extended to support the 130 nm node.

TAKE A LOOK INSIDE:

INDUSTRY BRIEFS
—see page 9

CALENDAR
For a list of meetings
—see page 10

Editorial

Will EUV mask defectivity be a deciding factor in the insertion of EUV lithography?

Abbas Rastegar, SEMATECH Fellow

In the past 10 years that I have been involved in EUV defectivity and the International EUVL Symposium steering committee, EUV mask defectivity has always been among the top three issues that need to be resolved for the successful implementation of EUV. While the main defectivity challenges reside in the blank and substrate, this defectivity has improved dramatically during the last decade, thanks to the continuous work of blank suppliers and SEMATECH, who have built the infrastructure, tools, and fundamental understanding of the defectivity challenges inherent in EUV. Nevertheless, many defectivity roadblocks still remain. Most of the initial infrastructure and tools developed by SEMATECH for EUV mask blanks was aimed at the 45 nm HP with extendibility to the 30 nm HP node. Today, we are discussing the insertion of EUV at the 11 nm HP node for memory applications with sub-10 nm HP targeted for other applications. Yet there are still no substrate-specific inspection tools and none are planned to be developed. We have put our trust in either actinic blank inspection tools currently being developed by Lasertec for the 16 nm HP or in some multilayer deposition tricks to enlarge (i.e., decorate) substrate defects to enhance substrate defect inspection capability, which is required to drive substrate development. Although useful for inspection of EUV mask blanks, neither of these techniques is adequate or fast enough to be used to develop key processes such as substrate CMP and cleaning, which are major contributors to substrate defectivity.

The question of who should own blank defectivity—blank suppliers or end users' consortia—is still an open one. The answer is not technical but economic. Who should invest in building the tools and infrastructure needed to improve EUV blank defectivity? In my opinion, substrate defectivity can be drastically reduced if blank suppliers are able to detect substrate defects and therefore modify their existing CMP tools and processes as well as the final cleaning processes. Current substrate CMP tools are designed for the best surface quality, but not for low defectivity; moreover, they are not as mature and controllable as wafer CMP tools. Again, the solution lies in investing in developing the proper tool and processes.

For clean tools, both the removal of sub-16 nm soft and hard defects and the extreme cleanliness of the tool, process, chemicals, and ultra-pure water are required capabilities. Again, investment in the development of new tools and technologies is critical.

Multilayer deposition tools and process are another source of defectivity in EUV mask blanks. Current multilayer deposition processes are slightly different from those initially developed by Lawrence Livermore national lab more than a decade ago. In fact, all existing ion beam deposition tools at SEMATECH and blank suppliers' sites were designed by Veeco for the 45 nm HP node. Consequently, SEMATECH and mask blank suppliers have focused their studies on reducing deposition-induced mask blank defects. As our learning about defectivity from ion beam deposition has improved, we have been able to modify existing tools to mitigate defects from the deposition process; however, there is not yet an overall design for a deposition tool for the 16 nm HP node. Many deposition-added defects come from handling, the chamber shield, and the targets, allowing them to be reduced by proper design. But again who should bear the cost of developing new multilayer deposition tools and is there enough market to attract tool suppliers to commit to building a new tool?

By improving mask defect repair and simulation techniques, the question of whether we can build a defect-free EUV blank has transformed into how many blank defects we can live with. This past year, mask shops using aerial imaging simulations have demonstrated that both e-beam and AFM-based mask repair tools can successfully repair multilayer defects on blank. Mask shops can therefore probably live with a handful of blank defects, relieving the burden on blank suppli-

(continues on page 9)

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1. Introduction

Historically single beam mask writer architectures developed in the 1970's (both raster Gaussian beam and VSB or variable shaped beam) were commercialized and met industry needs for the past 40 years. Continuous innovation by the writer suppliers extended the architecture node to node. They enabled the industry to meet the mask requirements keeping up with Moore's Law.

The industry has already experienced one landscape change. The 10keV MEBES raster architecture produced by ETEC/AMAT dominated the industry through the 130 nm node. This platform was supplanted by the 50keV Variable Shaped Beam (VSB) architecture starting at 130nm. The 10keV raster architecture was no longer extendable failing to meet resolution requirements and suffered from longer write times, as shown in figure 1. A simple equation describing MEBES raster tools write time is given by the following[1]:

$$(1)\ WT \sim \frac{Pixels}{PDR} * Rep * PC + OH = \frac{Area/_{WAU^2}}{PDR} * REP * PC + OH(PDR, Area, WAU, PC, Rep)$$

PDR=Pixel delivery rate, WAU = writing address unit, REP=repeat, PC= pass count, OH= overhead

The write time increase was consequence of Moore's law. Finer resolution required reducing the address unit with which the patterns were drawn on node to node. Due to the coarse pixel size (10-250 nm) of the MEBES, the writing grid had to be commensurate with the pattern address to avoid snapping errors impacting CDU and registration. As seen in figure 1, the pattern address shrink trend caused the writing address to also shrink resulting in longer write time by a factor of ~ $1/WAU^2$ (WAU=writing address unit). Additionally tighter resolution and CDU requirements forced a switch from a 2 $\mu C/cm^2$ PBS resist to 10-20 $\mu C/cm^2$ resists which required more repeats and/or pass count depending on write mode.

In order to counteract this, the writer supplier, ETEC/AMAT developed new gray scale[2] writing strategies. These strategies utilized multiple offset passes with writing grids which were 2x (MPP) or 4x (MPG) coarser than the pattern (input) address. The edge placement resolution is equivalent to the input address but at faster throughput (TPT). The multiple passes also allowed for higher dose without any TPT hit since number of repeats can be reduced. This enabled the platform to meet industry needs for a couple of nodes, however eventually this strategy was no longer extendable without significant changes to the raster architecture which were not implemented in time to meet industry needs.

The competing 50 keV vector shape beam tools had superior resolution primarily due to their higher accelerating voltage and offered faster write times due to the writing strategy differences. The 50keV write time can be modeled as a follows[3]:

$$(2)\ WT = \max\left(N \times \left(\frac{D}{J} + PC * t_s\right) + t_0, t_{BG}(N, PC, \ldots)\right)$$

N = *number of shots*, D = *resist dose*, J = *current density*, PC = *pass count*, t_s = *settling time*, t_0 = *overhead time*, t_{BG} = *datapath background process time*

The equation predicts that higher shot counts and pass counts result in longer write times while shorter settling times and higher beam current will reduce write times[4]. Note that there is no address unit dependence; VSB tools have a fixed small address unit resolution (0.1nm for latest tools) for shot size and placement. The small address unit of this platform allows it to absorb most grid snapping errors during fracturing to less than the minimum data grid of 0.1nm. At the 130 nm node, the performance advantages of VSB were sufficient to overcome the change cost barriers that had previously prevented the industry from migrating away from the raster beam approach. The VSB architecture has also proven to be very extendable[5] and is projected to be able to meet industry requirements up to the 10 nm node. Our projections are the single beam VSB architecture may not be easily extendable (meeting resolution with adequate TPT) past the 7nm logic node. The primary factor challenging VSB extendibility is the inability to meet lithographic capability requirements with reasonable write time.

The write time issue drives cost in terms of the number of tools needed as well as the impact of yield losses attributed to the writer. As an example, assuming a failure rate of 1 event per week, an average write time of 24 hrs results in a yield loss of 14% compared to 3.5% for a 6 hour write time. Tool reliability also needs to scale with write time in order to maintain yield. As will beshown, the primary drivers for longer write times are shot count growth and higher required dose, both of which are a result of the extension of Moore's Law.

2. Beam Blur Trends

The ITRS roadmap[6] indicates that mask feature size will continue to shrink. The need to pattern smaller features impacts several fundamental tool parameters and design choices. As shown in the following equation, MFS (minimum feature size) capability scales with the total process blur which has both beam and process components[7]. In order to reduce MFS, the total blur needs to be reduced. The beam component can be broken into two components as shown in the equation (4). The first term summarizes the effect of standard optic aberrations (chromatic, spherical, etc..) on the beam blur. Tool suppliers need to ensure that column design and manufacturing tolerances are optimized to minimize these error sources[8]. The second term (coulomb term) is unique to charged particle optics[9]. For a telecentric optical system as shown in figure 2, Dr. H. Pfeiffer has published equation (5) as an estimate of coulomb blur[10].

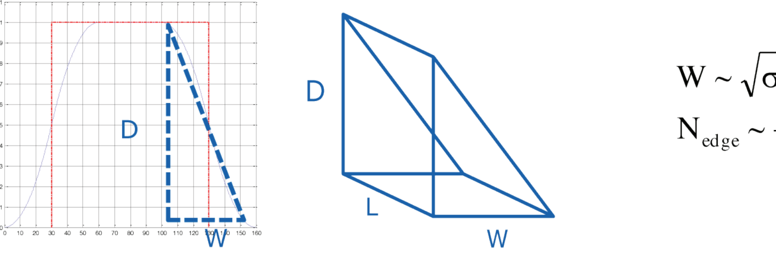
Figure 2. Geometry of Optics

$$(3)\quad MFS \sim \frac{2.4}{\sqrt{2}}\sqrt{\sigma_{beam}^2 + \sigma_{beam}^2}$$

$$(4)\quad \sigma_{beam}^2 = \sqrt{\sigma_{optical\ aberations}^2 + \sigma_{coulomb}^2}$$

$$(5)\quad \sigma_{blur} = \frac{I^{5/6} \cdot L^{5/4} \cdot M}{\alpha^{3/5} \cdot r^{1/2} \cdot U^{1/2}}\ where\ I_{\max vsb} = J \cdot A_{max\ shot}$$

I = beam current, L ~ optical column length, M=magnification, α=convergence angle, r ~object size, U = acceleration voltage, J = current density, $A_{max\ shot}$*=area of largest VSB shot*



$$W \sim \sqrt{\sigma^2_{beam} + \sigma^2_{resist}}$$

$$N_{edge} \sim \frac{1}{2} W * D * L$$

Figure 3. Dose profile at the edge approximated as a triangular prism. W is proportional to the process blur. For a given edge length L, the total number of electrons (N_{edge}) at the edge is depends on the dose (D) and W.

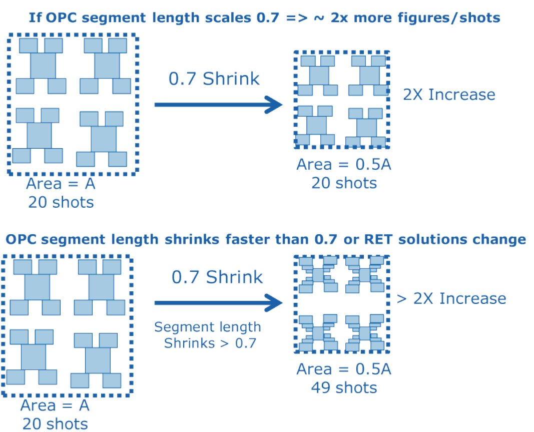


Figure 4. Impact of OPC complexity on shot count.

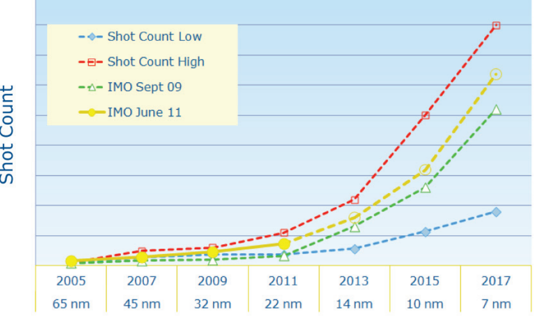


Figure 5. Shot count growth projections. Forecast is 2x increase per node.

All of the parameters need to be optimized to minimize blur, however for this discussion, beam current needs further elucidation since it impacts TPT. For a VSB system $I_{max}=J \cdot A_{max\ shot}$. Inorder to minimize I, J needs to be consistent with the maximum shot size. It is possible to achieve higher J by reducing the maximum shot size thus keeping blur constant, however this will increase shot count impacting TPT. As will be discussed in the following section, the trend is to use higher exposure doses, driving the need for higher J.

3. Dose Trends

Traditionally, shot noise considerations have been used to explain the need for higher dose. Note that the arguments presented here are rudimentary, however the general trends agree with the more sophisticated treatments in the literature.[11,12,13] The underlying assumption is image quality is dependent on the number of electrons used to expose the feature. For example, for a contact of area A, the number of electrons deposited, N= D*A (where D is dose and A = area of contact). From contact to contact, shot noise results in the N varying ~$1/\sqrt{N}$. The signal to noise ratio (SNR) is given by $N/\sqrt{N}=\sqrt{N}$. Since N=D*A, SNR gets worse with smaller MFS. Moore's law results in the contact area decreasing by 0.5 per node so the dose needs to increase 2x per node to maintain SNR from node to node, using this argument.

Another model focuses on shot noise effects at the feature edge. Edge placement variations at the feature edges are more important than variations in the bulk feature. As shown in figure 3, the number of electrons at the feature edges is proportional to the total process blur. The SNR at the edge is proportional to $\sqrt{N_{edge}}$, where N_{edge} is the total number of electrons at the edge. For improved resolution, the process blur needs to be reduced. This results in W decreasing as well requiring higher dose to keep N_{edge} constant. In practice, our observation is that dose is increasing approximately 1.4x per node[14].

4. Shot Count Growth

Moore's law predicts that the number of transistors doubles every node requiring a feature size shrink factor of 0.7. As seen in figure 4, the impact to mask complexity depends on the type of features required to pattern the silicon layer. For a 2D pattern, if the OPC segment length shrinks by 0.7, the number of figures defining a unit cell or motif remains the same. The doubling node over node should result in a 2x increase in the number of features. For some layers, more aggressive OPC such as faster scaling of the segment length or addition of assist features has lead to shot count growth more than 2x. For layers employing 1D layouts (i.e. lines and spaces), the expectations are that the figure count scales by 1.4x. Our observation (see figure 5) is that the overall shot count does increase by ~ 2x. Some layers show no or modest increase while others grow significantly more than 2x. Note that this trend is consistent with the 2.4x increasing trend reported by Spence et al. in 2006, which covered up to the 65nm node[15]. As seen in equation

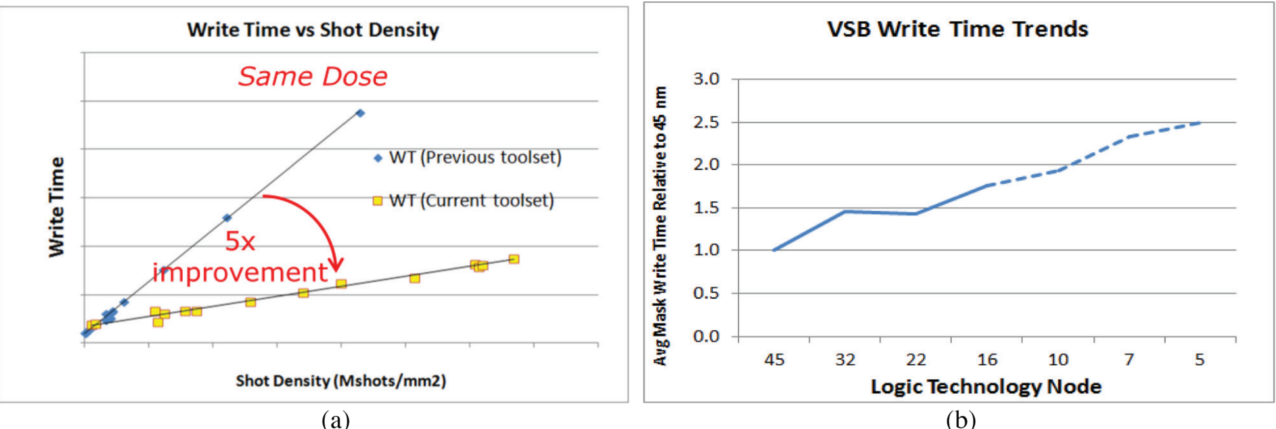
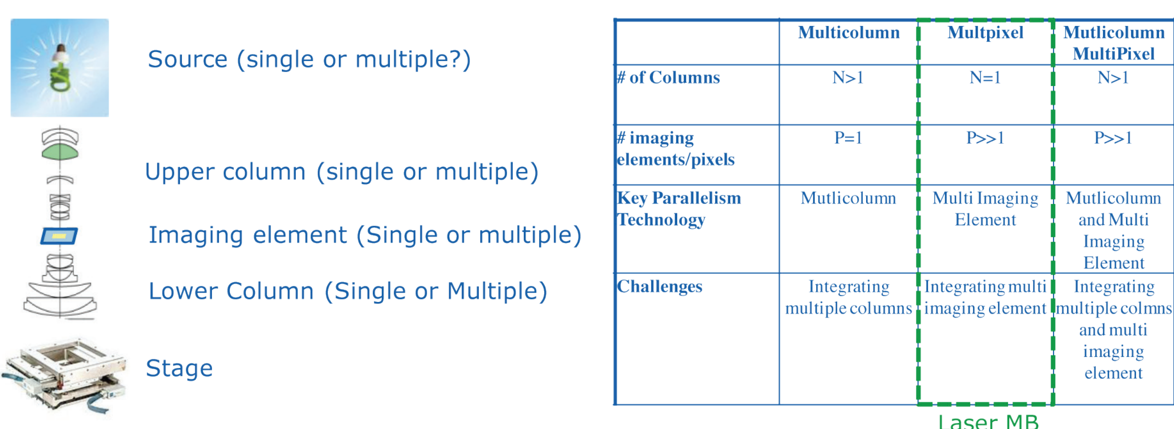


Figure 6. (a) Comparison of VSB write time versus shot count of current generation tools versus previous generations. Current generation tools are 5x faster at the same resist dose. (b) Despite TPT improvements, node over node write time has continued to increase.



	Multicolumn	Multpixel	Mutlicolumn MultiPixel
# of Columns	N>1	N=1	N>1
# imaging elements/pixels	P=1	P>>1	P>>1
Key Parallelism Technology	Mutlicolumn	Multi Imaging Element	Mutlicolumn and Multi Imaging Element
Challenges	Integrating multiple columns	Integrating multi imaging element	Integrating multiple colmns and multi imaging element

Figure 7. There are many options to use parallelism to increase the pixel delivery rate. As shown in the table, the approaches can be broken into multicolumn, multipixel or multicolumn-multipixel.

2, shot count growth can be compensated by decreasing settling times and increasing beam current.

5. Moore's Law Impact to VSB

In the previous sections, it was established that the need to reduce blur appears to be resulting in a dose increase of 1.4x per node. Additionally the shot count growth is following a 2x increase node to node. As seen in equation (2), the suppliers have to reduce t_s (settling time) and increase J (beam current) to maintain TPT[16]. Note the ability to increase J is limited by requirement to reduce blur as indicated by equation (5). Also the need to minimize the maximum shot size will result in additional shots.

The effectiveness of the supplier efforts to counteract factors leading to longer write time can be judged by the graphs shown in figure 6a and b. As seen in figure 6a, our assessment is that the latest generation tools are ~ 5x faster than the previous platforms. The 5x improvement needed to cover three technology nodes. The suppliers increased source brightness, reduced settling times and increased data path bandwidth. Despite the improvement, our experience is that the average write time has been increasing relative to the 45 node, as seen in figure 6b. In addition, an increasing fraction of the layers have write times > 24 hrs. Without additional improvements to the architecture, the average write is projected to increase > 2x by the 10 nm node. It is clear that further improvements will be needed to counteract the factors increasing write time.

6. VSB Extension Options

Recently, several suppliers have proposed applying overlapping exposures to VSB[17,18,19]. In these approaches, shot edges do not precisely align with the input data edges. Taking advantage of the inherent process blur, these approaches result in contours matching what is produced by normal fracture. They are reminiscent of the development of gray scale overlapping spot writing modes which were successfully used to extend the MEBES raster architecture.

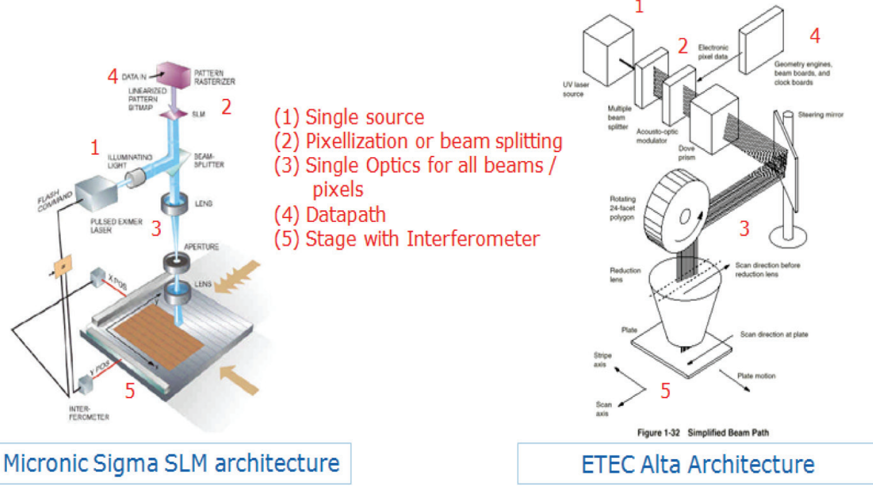


Figure 8. comparison between the highly parallel multibeam laser mask writing systems. Parallelism is achieved by patterning multiple pixels at a time (multipixel approach).

The promise of these evolutionary approaches is equivalent lithography with fewer shots and thus shorter write times.

For curvilinear ILT patterns, significant reductions in shot count and write time have been reported.[20] For these types of patterns, these approaches can reduce the unreasonably long write time (>>24hrs) to something comparable to conventional non ILT patterns. The suppliers also indicate that the shot count reduction opportunities are layout dependent. Smaller improvements are seen for conventional non ILT type patterns. It does not appear that these techniques alone can extend single beam VSB. The industry needs to consider the need to develop a revolutionary mask writer architecture which can meet the mask lithography requirement with reasonable write time.

7. Highly Parallel (Mask) Writer Architecture

Our assessment is that beam blur needs to be less than 5 nm. Additionally, the writer needs support a dose increase of 1.4x per node and a 2x increase in data volume per node with reasonable write time. Several companies are proposing new writer architectures for mask and direct write application. All the approaches are highly parallel to increase the pixel or data delivery rate. As illustrated in figure 7, there are several approaches to parallelism.

These approaches can be broadly categorized as multicolumn, multipixel and multicolumn - multipixels. In order to gain perspective on the merits and technical challenges of these approaches, it is useful to look at the laser mask writer landscape where two successful highly parallel multibeam approaches have been in production. Both the Micronic[21] and ALTA[22] systems are similar in that they employ a single source, single stage and single optical column. The multiplicity and parallelism is provided by the imaging elements as seen in figure 8.

The Micronic platform uses an SLM (spatial light modulator) to form 1 million pixels simultaneously patterning a 162x32um area. In the ALTA case, a single laser beam is split in 32 distinct beams each of which can be individually modulated and simultaneously expose the mask. These architectures demonstrate that key issues related to multiple pixels are solvable as seen in table 1. Specifically, the suppliers have shown that multipixel elements can be manufactured, calibrated and maintained in a production environment.

An architectural comparison of the current ebeam efforts is shown in table 2. The last row of table 2 attempts to categorize each approach into one of the three basic types defined in table 1. A brief description of each architecture is provided in the subsequent section.

The one low voltage approach, Mapper[23], uses a broad source which is broken up by a MEMS aperture array into 13000 individual beams Each beam goes through individual MEMS projection optics which focus, blank, and raster the beam; hence this is categorized as a multicolumn system. The low keV was partially chosen since less dose is required to expose the resist at lower ebeam energies.

The KLA-REBL[24] direct write proposal is to use multipixel and multicolumn. Each individual column is multipixel which is achieved by using a 1M-4M pixel element digital pattern generator (DPG). The DPG allows each pixel to be turned on or off enabling simultaneous patterning of a large area.

The IMS[25] approach uses a broad source which illuminates a programmable MEMS aperture array system (APS). The APS forms 262144 beams which can be individually blanked. The apertures form 20nm square beams, or shots, on the mask and the dwell time of each beam can be adjusted to vary the dose. The patterns are defined by multiple passes by different beams. This approach appears to be insensitive to a single dead pixel since a single beam only imparts a fraction of the dose at any given edge.

The Vistec[26] system uses a single column with a multi pixel approach based on VSB. Parallelism is achieved by employing a MEMS microdeflector array which simultane-

Table 1. Summary of key technical challenges and status for laser mask writers.

	Micronic Sigma	AMAT Alta
Large Field Calibration	+ OK	+ OK
Pixel/Beam Calibration OK?	+ 1M SLM pixels w/64 gray levels in reasonable time	+ 32 Beams w/16 gray levels in reasonable time
Defective Pixels/Beam	+ Some Dead Pixels OK + Pixel reliability OK	- All beams have to work + beam reliability OK
Edge Placement resolution	+ Fixed grid (1.25 nm) OK for application space	+ Fixed grid (2 nm) okay for application space
OPC feature resolution	+ OK for application space	+ OK for application space

Table 2: Comparison of current multibeam efforts using available published information.

	Mapper	KT-REBL	Vistec	IMS	Advantest	MBC
keV	5kV	50kV	50kV	50kV	50kV	5-50kV
# of Columns	1 condenser 13K projection	4	1	1	8	88
# imaging elements	13000 micro columns	1M pixels	64 VSB micro shapes	256K square beams	Cell/VSB shapes per column	1 per column
Key Parallelism Technology	13K MEMS projection column	DPG to form 1M pixels per column and multi column	MEMS VSB/CP imaging	MEMS APS	Multiple columns and stage, cell projection	Mini columns
# of Beams (Plan)	637k	4M+	64	256k	8	88
Write Mode	Raster	Raster	Vector	Raster	Vector	adaptable
Template	Multicolumn	Multicolumn & Multipixel	Multipixel	Multipixel	Multicolumn & Multipixel	tbd

ously forms 64 small VSB shots. Each of the shapes needs to be individually calibrated much like a conventional VSB system. In some ways it is an extension of current VSB patterning

The other two candidates Advantest[27] and Multibeam[8] also use a strategy employing multiple columns on a single stage. The multicolumn approach requires good matching and alignment of the columns relative to each other to maintain CD and registration control and introduces column to column matching and stitching concerns. Additionally, it should be noted that the Advantest writing strategy is fundamentally a VSB approach since their proposal is to use cell projection to pattern large areas in conjunction with ability to switch to conventionally VSB printing for features which cannot be patterned using the existing cell library.

The multibeam suppliers have come up with a variety of novel approaches in order to achieve parallelism and offer lithography at reasonable write times. The Vistec and IMS approaches follow the laser mask writer template: single source, single stage, and single column but with a multipixel imaging system. Some of the suppliers have built proof of concept or pre-alpha tools to demonstrate key elements of their technology including pixel calibration, large area calibration and ability to handle defective pixels. Many have shown encouraging lithography results; however none have demonstrated the capability to meet all of the required photomask specifications. All are several years away from manufacturing a production worthy mask writer.

8. Summary

The VSB architecture has supported the industry for almost two decades. Despite continuous improvements by the suppliers to improve write speed, higher shot counts and higher dose requirements have been leading to write time increases since the 45 nm node. Recent evolutionary innovations in writing strategies such as overlapping shots have potential to reduce the shot count; however the reductions are layout dependant and will only delay the write time increase trend. Several suppliers are proposing revolutionary new mask writing architectures to meet future requirements. The common theme in their approach is parallelism. Each of the approaches has unique technical challenges. It is clear that suppliers will need industry assistance to progress further. Our recommendation is that we continue to drive the existing VSB suppliers to make evolutionary improvements

and in parallel support development of a new revolutionary highly parallel mask writing architecture. Industry collaboration is required to focus efforts and ensure a solution is in place to meet industry needs.

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Editorial

(continued from page 2)

ers to reduce defectivity. Today we have useable EUV masks for R&D and pre-production purposes; whether sufficient low defect blanks will be available to HVM is an economic issue. If we judiciously invest in the tools and infrastructure, then we can cope with HVM demands at the 16 nm HP node.

For sub-10 nm HP nodes, however, there may be other hurdles that we do not know about. Recent discussions about changing mask magnification and/or size have direct implications for EUV mask defectivity. Many questions must be answered: "Is there a need for a thinner absorber and therefore new materials for the absorber and possibly capping layers?," "Should multilayer structures be modified and a new interlayer introduced?," "Will exposure tools continue to use electrostatic chucks and, if so, how do we deal with backside defectivity?"

I guess "EUV" is synonymous with "challenge" and that is what keeps me interested in the field. - I am, in fact, optimistic about the future. If the industry decides to go with larger magnification for EUV optics, mask makers will have fewer defectivity challenges; if magnification remains as it is, we will continue to tackle defectivity issues as we always have. For sub-10 nm EUV substrates, defects become less important as the physics of multilayer deposition will determine defect size. As a result, defectivity from multilayer deposition will become more challenging than ever.

I believe that although EUV mask defectivity will remain among the top three challenges for years to come, it will not delay EUV insertion. The history of semiconductors has taught us that our engineers always find a solution when our scientists do not see a path to the future.

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Industry Briefs

IBM Demos High-Performance CMOS on Flexible Plastic Substrates

September 17, 2012

To date, flexible circuits have offered only limited performance because plastic substrates aren't compatible with the high temperatures/harsh processes needed to make high-performance CMOS devices.

At the International Electron Devices Meeting (IEDM),IBM researchers will demonstrate high-performance state-of-the-art CMOS circuits—including SRAM memory and ring oscillators—on a flexible plastic substrate. The extremely thin silicon on insulator (ETSOI) devices had a body thickness of just 60 angstroms. IBM built them on silicon and then used a process called controlled spalling to transfer them to flexible plastic tape. The devices had gate lengths of <30 nm and gate pitch of 100 nm. The ring oscillators had a stage delay of just 16 ps at 0.9 V, believed to be the best reported performance for a flexible circuit. A slight degradation of delay for the flexible sample after the layer transfer comes from degradation of p-FET performance due to strain effects.

Chip Tool Demand Slumps in 2Q12, Though Taiwan Shines

October 1, 2012

Worldwide semiconductor manufacturing equipment totaled $10.34B in 2Q12, down -4% from the previous quarter and about -13% from a year ago, according to monthly data from SEMI and SEAJ. Bookings were also down -4% sequentially, and were off by -10% year-on-year, to $9.70B.

SEMI's most recent forecast, calls for overall chip equipment demand to slip -2.6% in 2012 to $43.53B—and only that slightly because the two biggest end-user regions are still pushing forward, in Korea ($11.48B, +32% and Taiwan ($9.26B, +8.6%). All other regions are expected to reduce their equipment spending between -15% and -29%. The final SEMI/SEAJ numbers for 2Q12 support that scenario, at least partially. Taiwan's demand for chip tools soared 83% in 2Q12 to $3.25B, leapfrogging the region back to the No.1 spot. Korea, meanwhile, slipped -22% Q/Q to $2.59B, a decline-rate in line with the other sluggish regions. The August version of SEMI's World Fab Forecast has adjusted equipment capex down for both Korea (subtracting $0.9B to $10.8B) and Taiwan (subtracting $0.4B to $8.5B).

GlobalFoundries to Fab Sand 9's MEMS Timing Products

James Montgomery, October 2, 2012

Sand 9, a Cambridge, MA-based developer of precision microelectromechanical systems (MEMS) timing technology for wireless and wired applications, is partnering with GlobalFoundries for high-volume manufacturing of its technology, which incorporates silicon-on-insulator (SOI) and through-silicon vias (TSV).

The deal also highlights GlobalFoundries' MEMS design and manufacturing capabilities, pointed out Raj Kumar, SVP for the foundry's 200mm business unit & GM of its Fab 7 facility in Singapore (formerly Chartered Semiconductor). Sand 9 projects a sparkling ~86% compound annual growth rate (CAGR) for both MEMS oscillator sales and unit shipments over the next five years (2011-2016), mostly thanks to demand from smartphones.

imec to Begin 450mm Cleanroom Construction in 2013

By **Pete Singer,** October 7, 2012

imec, the research consortium in Leuven, Belgium, plans to start construction of a 450mm pilot line next year. It is to be installed next to an existing 300mm line that houses more than $1 billion in tools, including an ASML EUV lithography tool.

The Flemish Government support of imec will enable the building of the 100 million euro cleanroom infrastructure, and help imec to further extend the investment to a total of 1 billion euro in the next 5 years. The aim is to open the new 450mm clean room facilities in 2015. Phase 1 of the project is underway in the 300mm cleanroom, designed to be 450mm compatible. Phase 2 is the installation of a new cleanroom next to the current 300mm facility. Imec expects key equipment companies will participate in the project and key fabless companies will do the fabrication in the new facilities.

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About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

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Calendar

2013

SPIE Advanced Lithography

24-28 February 2013
San Jose Convention Center and
San Jose Marriott
San Jose, California, USA
spie.org/al

SPIE Photomask Technology

10-12 September 2013
Monterey Marriott and
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