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SPIE Photomask Technology - Invited Paper

# Litho-Aware Redundant Local-Loop Insertion Framework With Convolutional Neural Network

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## ABSTRACT

With the VLSI technology shrinking to 7nm and beyond, the Redundant Local Loop (RLL), also known as via pillar, becomes a promising candidate of redundant via insertion due to its compatibility with the unidirectional layout style. Existing RLL insertion approaches only leverage rule-based heuristics for manufacturing constraints, which can no longer obtain a large enough Process Window (PW) in advanced technology nodes. It is imperative to develop new techniques to optimize lithography process window while inserting RLL to achieve a good yield. In this paper, we propose a machine learning-based litho-aware RLL insertion framework. Conventional lithography simulation requires tremendous computational resources to evaluate the lithography quality accurately, which is not feasible for process window exploration. We formulate the lithography simulation as a regression task and develop a customized Conventional Neural Network (CNN) architecture to predict the Depth of Focus (DOF), a standard metric for evaluating process window. We propose a complete ow for litho-aware RLL insertion based on the CNN model for process window evaluation. The commercial lithography simulator evaluates the effectiveness of the proposed framework. Experimental results demonstrate that our lithography model can predict the DOF with high accuracy and generalize well on unseen patterns while achieving orders of magnitude speedup compared to conventional lithography simulation. Our litho-aware RLL insertion framework can effectively improve the lithography process window with comparable runtime and insertion rate compared to the state-of-the-art method.

## 1. Introduction

With the continuous scaling of semiconductor technology nodes, redundant via insertion becomes a pivotal technology to improve yield. In advanced technology nodes with the unidirectional routing style, conventional methods of inserting redundant vias have become obsolete because they introduced metal shapes in the non- preferred direction. Fig. 1(b) shows that traditional redundant via insertion introduces Metal-3 (M3) wire bending in the non-preferred direction. To overcome this issue, Redundant Local Loop (RLL), also known as via-pillar, is proposed to ensure the consistent direction of each metal wire with the design rules while introducing redundant vias (Fig. 1(c)). Recent works[1,2] are proposed to optimize the delay and performance of chips in RLL insertion. Xu et al.[3] propose a rule-based algorithm for RLL insertion considering advanced manufacturing constraints.

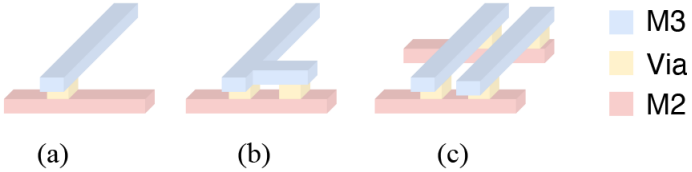


*Figure 1. (a) single via, (b) traditional redundant via insertion with wire bending, (c) redundant local loop that compatible with one-dimensional routing.*

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# EDITORIAL

## COVID and War – Horrors, Challenges, and Opportunities

**Artur Balasinski,** Infineon Technologies

History is as cruel as it is ironic – everybody knows that. In the wake of COVID-19, those who survived can now enjoy a lifestyle benefit earlier unheard of: wide acceptance of working from home and overall, computerized presence. Our lives just became more remote-controlled, quite to our own advantage as the BACUS Community making the masks, which make all this possible.

What else just became remote-controlled? Why, the battlefield. While the outcome of the fighting in Ukraine is still unknown, one thing is clear: A remote-controlled missile is as good as a tank. They cancel each other out. Some people are taking it one step further, saying that such a missile, if advanced enough, can be as good an aircraft. Such painful comparisons are taking the arms race to a completely different level, perhaps to the advantage of the military defending their territory over those trying to move in. At any rate, there seems to be a big engineering opportunity to propose a new battlefield model and maybe alleviate some of that pain and cruelty.

As scary and brutal as this new challenge for mankind currently is, perhaps there would be some other silver lining at the end of it, just as for the aftermath of COVID. Ukraine is a highly technologically capable nation, having contributed over the course of the years to mathematics, aeronautics, avionics, nuclear science, and recently, to the IT sector. This, in addition to their Cossack spirit (from the Turkic "kazak" – meaning "free man"), would make them fierce competitors, not just in war but in technology too. Many companies have currently strong footholds in Ukraine. Perhaps the blood-related attention the country is getting now will help it gain manufacturing strength in the years to come.

What can we, as the BACUS community, do about it? We should promote engineering projects and scholarships seeking out technical talent in Ukraine to foster technology development based on the resources available in that country. We should better understand the current situation at their universities and establish contacts to run joint projects. Surely the omnipotent computerized presence based on the COVID experience would come in handy. We should reach out to propose free participation in meetings and conferences as the stepping stone for mutual learning. Establishing such ties would help both our prospective partners and ourselves realize our common goals, in technology and in life.

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**Table 1. The CNN architecture.**

| Layper | Kernel | Stride | Output Size | Layper | kernel | Stride | Output Size |
|---|---|---|---|---|---|---|---|
| Conv1-1 | 5 × 5 × 4 | 2 | 124 × 124 × 4 | Pool | 1 2 × 2 | 2 | 62 × 62 × 4 |
| Conv2-1<br>Conv2-3 | 3 × 3 × 8<br>3 × 3 × 8 | 1<br>1 | 62 × 62 × 8<br>62 × 62 × 8 | Conv2-2<br>Pool2 | 3 × 3 × 8<br>2 × 2 | 1<br>2 | 62 × 62 × 8<br>31 × 31 × 8 |
| Conv3-1<br>Conv3-3 | 3 × 3 × 16<br>3 × 3 × 16 | 1<br>1 | 31 × 31 × 16<br>31 × 31 × 16 | Conv3-2<br>Pool3 | 3 × 3 × 16<br>2 × 2 | 1<br>2 | 31 × 31 × 16<br>15 × 15 × 16 |
| Conv4-1<br>Conv4-3 | 3 × 3 × 32<br>3 × 3 × 32 | 1<br>1 | 15 × 15 × 32<br>15 × 15 × 32 | Conv4-2<br>Pool4 | 3 × 3 × 32<br>2 × 2 | 1<br>2 | 15 × 15 × 32<br>7 × 7 × 32 |
| Conv5-1<br>Conv5-3 | 3 × 3 × 32<br>3 × 3 × 32 | 1<br>1 | 7 × 7 × 32<br>7 × 7 × 32 | Conv5-2<br>Pool5 | 3 × 3 × 32<br>2 × 2 | 1<br>2 | 7 × 7 × 32<br>3 × 3 × 32 |
| FC1<br>FC3 | -<br>- | -<br>- | 1024<br>1 | FC2 | - | - | 512 |

Nevertheless, such approaches can no longer obtain a large enough process window in advanced technology nodes. It is imperative to develop new techniques to optimize lithography while inserting RLL to achieve a good yield. In this paper, we propose a machine learning-based litho-aware RLL insertion framework. Conventional lithography simulation requires tremendous computational resources to accurately evaluate the lithography quality, which is not feasible for process window exploration. Considering the fact that machine learning approaches have demonstrated superior computational efficiency to traditional simulation methods, we formulate the lithography process window simulation as a regression task and develop a customized conventional neural network (CNN) architecture to predict the Depth of Focus (DOF), a standard metric for evaluating lithography process window. This proposed framework can trade-off between accuracy and runtime. The major contributions of this paper are highlighted as follows.

- The lithography process window prediction problem is formulated as a regression task without lithography simulation.
- The CNN network is developed to achieve both high accuracy and efficiency.
- Experimental results demonstrate that our framework can increase the average lithography process window by 1.8% for benchmarks at 10nm technology node with comparable insertion rate to sate-of-work.[3]

The rest of this paper is organized as follows. Section 2 reviews the basic concepts and gives the problem formulation. Section 3 provides a detailed explanation of the proposed framework. Section 4 reports the experimental results. Finally, Section 5 concludes the paper.

## 2. Preliminaries

In modern VLSI redundant via insertion, the optimization usually includes multiple objectives, such as wirelength and the number of vias. A larger number of vias and wirelength leads to a considerable timing impact of a local loop structure[4] and difficulty for post stages. In practice, the solution that neglected the above metrics may result in congestion and failure. Hence, the RLLs with less redundant vias and wirelength are preferred. We adopt the cost metric in this work, considering both wirelength and the number of vias.

**Definition 1 (Cost).** Cost $c \in \mathbb{R}$ evaluates the cost of an RLL structure with N metal layers and N — 1 via layers, which is defined as follows:

$$c = \sum_{i=0}^{N} \alpha_i m_i + \sum_{i=0}^{N-1} \beta_i v_i, \tag{1}$$

where $\alpha$, $\beta$ are user-defined parameters, $m_i$ denotes the redundant wirelength on the $i$th metal layer, $v_i$ denotes the number of redundant vias on the $i$th via layer.

In advanced technology nodes, the cost is not enough to evaluate an RLL structure. Different RLLs with similar costs may lead to distinctive yield impacts. So, we select the *depth of focus* (DOF) metric to evaluate the lithography of a pattern.

**Definition 2 (DOF).** DOF $\in \mathbb{R}$ evaluates the performance of optical lithography. It can be defined as the range of focus that keeps the resist profile of a given feature within all specifications over a specified exposure range.

In practical semiconductor lithograph, DOF generally depends on resist, process parameters, and imaged patterns. Therefore, DOF is generally obtained by lithography simulation. In this work, we introduce a lithography machine learning model to speed up the simulation ow, evaluated by Mean Absolute Percentage Error (MAPE).

**Definition 3 (MAPE).** MAPE $\in \mathbb{R}$ evaluates the prediction accuracy of the proposed lithography model:

$$\text{MAPE} = \frac{100}{n} \sum_{i=1}^{n} \left| \frac{\hat{y}_i - y_i}{y_i} \right| \tag{2}$$

where $y_i$ is the actual DOF value obtained by lithography simulation, and $\hat{y}_i$ is the predicted DOF value.

With all the metrics defined, the redundant local loop insertion in the unidirectional layout is defined as follows:

**Problem 1 (Lithography Model).** Given a dataset containing the labelled data, pairs of layout patterns, and corresponding DOFs obtained by lithography simulation, train a model that can accurately predict a given layout pattern's DOF (i.e., minimize MAPE).

**Problem 2 (Redundant Local Loop Insertion).** Given the unidirectional routing design and design rules, produce a legal RLL insertion solution with optimized insertion rate, total cost, and lithography quality.

## 3. Litho-Aware RLL Insertion Framework

### 3.1 Data Preparation

For training the proposed lithography model, a labelled dataset is needed. The dataset includes 900 randomly selected 1.04 x 1.04 mm$^2$ clips of each metal layer, and Mask Optimization (MO) has been applied to those clips to obtain the corresponding DOFs. The original layout data format (GDS II) is composed of succeeding vertex coordinate lists. Therefore, we encode these vertex coordinates into pixels. In our work, the routing solutions are based on a routing grid model, and the 1.04 x 1.04 mm$^2$ clips can be pixeled into binary images of size 52 x 52 pixels without loss. For a better representation under the optical proximity effect, 5.04 x 5.04 mm$^2$ clips centred on selected clips are pixeled into binary images of size 252 x 252 pixels. The dataset is divided into two parts: 50% are preprocessed for CNN model training, while 50% are used for validation. Rotation and are applied to the training dataset to obtain various layout patterns further.

### 3.2 Convolutional Neural Network Architecture

Convolutional Neural Networks (CNN) have been proved capable of image classification and recognition.[5] Convolutional layer, pooling layer, and Fully Connected (FC) layer are three main components of CNN architecture. The convolutional layer's parameters consist of a set of learnable filters (or kernels), with a small receptive field and apply a convolution operation to the input, passing the result to the next layer. As a result, the network learns filters that activate when it detects some specific features. Pooling

**Table 2. Notations.**

| | |
|---|---|
| $rll_i$ | $i$th RLL candidate |
| $c_i$ | the cost of $rll_i$ |
| $v_i$ | the number of redundant vias that $llc_i$ covers |
| $n_i$ | the number of vias that $llc_i$ covers |
| $p_i$ | the lithography (i.e., DOF) of $llc_i$ |
| $x_i$ | the binary variable for $llc_i$ |
| $X_j$ | the variable set for the RLLCs covering $v_i$ |
| $G_k$ | the $k$th set for RLL candidates occupying the same grid |
| $SA_k$ | the $k$th set for RLL candidates occupying conflicting SAV grids |
| $X, G, SA$ | set for $X_i$, $G_k$ and $SA_k$, respectively |
| $W_K$ | the $k$th density window |
| $n_{i,k}$ | the number of vias of $llc_i$ in $W_k$ |
| $DB_k$ | via density upper bound for $W_k$ |
| $W$ | the set of density window $W_k$ |
| δ,ε, ζ | custom parameters |

**Table 3. Benchmark Statistics.[3]**

| Metric | ecc | efc | ctl | alu | div | top |
|---|---|---|---|---|---|---|
| #via | 4013 | 4619 | 5873 | 6683 | 12 878 | 48 847 |
| #nets | 1539 | 1322 | 2062 | 2138 | 3792 | 12 988 |
| #RLLC per via | 47.3 | 39.0 | 43.7 | 32.6 | 36.0 | 35.2 |

layers extract the statistical summary of the previous layer's local regions reducing the feature map dimension. Fully connected layers are used to flatten the feature maps extracted from multiple convolution and pool operations into a one-dimensional vector to predict the final results. The CNN architecture for the DOF prediction problem is summarized in Table 1, consisting of five convolution blocks and three FC layers. The first convolutional layer filters the input vectors of size 252 x 252 with a kernel of size 5 x 5. The remaining convolutional layers with kernels size of 3 x 3 to obtain a more profound representation. Max-pooling with filter size 2 x 2 and stride 2 is applied after each convolution block. Three FC layers are applied to flatten high-dimensional feature vectors to the final result.

### 3.3 ILP Formulation

Problem 2 can be formulated as an assignment problem. In this work, we extend the ILP formulation developed in Xu et al.,[3] and add a DOF item in the objective function to improve the lithography process window. Our modifications are highlighted in blue.

$$\max \delta \sum_{x_i} n_i x_i - \varepsilon \sum_{x_i} c_i x_i + \zeta \sum_{x_i} p_i x_i \quad (3)$$

$$\text{s.t.} \sum_{x_i \in X_j} x_i \le 1 \qquad \forall X_j \in X \quad (3\text{-c1})$$

$$\sum_{x_i \in A} x_i \le 1 \qquad \forall A \in G \cup SA \quad (3\text{-c2})$$

$$\sum_{llc_i \in W_k} n_{ik} \cdot x_i \le DB_k \qquad \forall W_k \in W \quad (3\text{-c3})$$

$$x_i \in \{0,1\} \qquad \forall x_j \in X_j \quad (3\text{-c4})$$

Eq. (3) consists of three terms. The first term $\sum_{xi} n_i x_i$ is the total number of redundant vias, which improves the insertion rate; The second term $\sum_{xi} c_i x_i$ aims to reduce the overall cost of inserted RLLs; The third term $\sum_{xi} p_i x_i$ is used to improve the lithography process window of the target design. The custom parameters θ , ε, and ζ can be flexibly set to trade-off those items.

## 4. Experimental Results

### 4.1 Experiment setup

We adopt Pytorch[6] to implement the CNN model. The experiments ran on a 64-bit Linux machine with two 20-core Intel Xeon@2.1 GHz CPUs and 64GB RAM. The commercial lithography software Tachyon runs on a 64-bit Linux machine with four Intel Xeon@2 GHz CPUs and 220GB RAM.

The benchmarks from Xu et al.[3] are listed in Table 3. Those benchmarks are shrunk to 10nm technology node. This shrinkage will not affect the algorithm's behaviour since Xu et al.[3] adopts a grid-based solution strategy.

### 4.2 Lithography Model Validation

We use Adam[7] as the gradient descent optimizer for model training. The learning rate is set to 0:01, the batch size is set to 40, and the maximum number of iterations is 1000. The dropout rate is set to 0:5 to prevent overfitting. The Mean Squared Error (MSE) is used as the loss function. We set $\alpha_\iota$ ($\iota \in [0, N]$) to 1 and $\beta\iota$ ($\iota \in [0, N-1]$) to 5 in Eq. (1). δ and ε in Eq. (3) is set to 500 and 1 respectively. ζ is defined as $\zeta = e^{4(1-\frac{p}{120})}$, where $p$ is the predicted lithography.

We trained two CNN models for M2 and M3, respectively, to further improve the prediction accuracy. This will not introduce too much runtime overhead. The maximum iteration of each model is set to 1000. Their performances on training and testing datasets are reported in Table 4. It can be seen that the prediction accuracy of the two metal layers of M2 and M3 are both about 3 %. The runtime to obtain the process window using the lithography simulation tool exceeds 30 minutes, which is related to the scale of the layout. However, it takes about 5 minutes to train a CNN model, and the runtime of predicting process window is about 3.2 ms. This means that the proposed CNN model is more than 105 faster than the simulation tool, and the accuracy loss is still within a reasonable range. On the other hand, the precision losses can still be further reduced. Since the process windows of most benchmarks are 80-100, the training suffers from a date imbalance issue, hindering the achievement of high accuracy. Techniques such as data augmentation,

**Table 4. Experimental result of the CNN models on training dataset and testing dataset.**

| Dateset | Model | MAPE (%) | TpS (ms) * |
|---|---|---|---|
| Training | M2 | 2.77 | 3.42 |
| | M3 | 2.46 | 4.82 |
| | Avg. | 2.61 | 4.12 |
| Testing | M2 | 3.3 | 3.26 |
| | M3 | 3.08 | 2.94 |
| | Avg. | 3.19 | 3.10 |

**Table 5. Comparison of inserting rate (IR) and lithography process window (PW) of different RLL inserting methods.**

| Design | Xu et al.3 | | Xu et al.3 (IR-R*) | | Ours | |
|---|---|---|---|---|---|---|
| | IR (%) | PW | IR (%) | PW | IR (%) | PW |
| top | 83.00 | 79.22 | 79.24 | 80.92 | 79.62 | 82.3 |
| Ratio | 1.00 | 1.00 | 0.95 | 1.02 | 0.96 | 1.04 |

IR-R: The insertion rate is randomly reduced to close to ours.

**Table 6. Detailed experimental result on benchmarks.**

| | Xu et al.3 | | | | Ours | | | |
|---|---|---|---|---|---|---|---|---|
| Design | IR (%) | #RLL | #RpR * | T (s) | IR (%) | #RLL | #RpR * | T (s) |
| ecc | 98.26 | 2542 | 2.45 | 3.7 | 96.61 | 2733 | 2.58 | 3.7 |
| efc | 92.35 | 2799 | 2.45 | 3.9 | 87.66 | 2866 | 2.57 | 3.9 |
| ctl | 95.23 | 3543 | 2.42 | 5.4 | 92.56 | 3746 | 2.55 | 5.4 |
| alu | 80.40 | 3232 | 2.34 | 5.2 | 75.69 | 3242 | 2.52 | 5.3 |
| div | 88.12 | 7103 | 2.40 | 11.0 | 83.11 | 7315 | 2.55 | 11.2 |
| top | 83.00 | 24705 | 2.36 | 37.0 | 79.62 | 25092 | 2.53 | 37.5 |
| Avg. | 89.56 | 7321 | 2.40 | 11.03 | 85.21 | 7499 | 2.55 | 11.17 |
| Ratio | 1.00 | 1.00 | 1.00 | 1.00 | 0.96 | 1.03 | 1.06 | 1.01 |

*#RpR: redundant via number per RLL.

and optimized sampling strategies can address this concern. Due to this accuracy meets the requirements of our framework, we leave the exploration in the future.

### 4.3 Framework Validation

As mentioned in Problem 2, the goal of the RLL is to maximize the inserting rate to improve the yield and reduce the timing impact of the introduced redundant vias. With the proposed CNN model, we can predict the process window of each RLL candidate. In this way, the trade-off between the insertion rate and the lithography can be achieved. The insertion rate of the proposed framework tends to be reduced compared to Xu et al.,[3] due to that their method takes the insertion rate as the only metric to be evaluated. We added a control group (denoted as IR-R) whose insertion rate is randomly reduced to the same level as ours to control variables. The comparison of our work, IR-R, and Xu et al.[3] is reported in Table 5.

The "Ratio" is based on Xu et al.[3] as the baseline. It can be seen that we can increase the average lithography process window by 4% with comparable runtime. Compared with IR-R, we can achieve a 2% more average lithography process window with a 1% higher insertion rate, which means that our framework can effectively trade-off between insertion rate and the lithography quality.

Table 6 gives the detailed experimental result on benchmarks. One can find that the insertion rate reduction of our framework is within the acceptable range (average 4.3 %), and the runtime is comparable. Those experimental demonstrate that our litho-aware RLL insertion framework can effectively improve the lithography process quality with comparable runtime and insertion rate. As the setting of the $\varepsilon$ is flexible, we can adjust the weight of a lithography item to the requirements of real-world applications. This paradigm provides a flexible framework to meet the challenge of the DTCO methodology, which is promising at advanced nodes.

## 5. Conclusion

In this paper, we present a litho-aware RLL insertion framework. The proposed framework considers the lithography requirements in the RLL candidates selection stage. It achieves a trade-off between lithography process window and insertion rate compared with the traditional insertion algorithm. We also propose a CNN model to estimate the process window, which can be 105 faster than the rigorous simulation. The experiments show that the proposed framework can improve the average lithography process window by 1.8% on benchmarks in 10nm technology node. Future work includes developing algorithms to address data mismatch to improve the DOF prediction accuracy.

## 6. Acknowledgments

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# Industry Briefs

## Tech Chiefs Urge Congress to go Bigger and Faster by Passing Semiconductor Funding

**Daniel Flatley,** Bloomberg

CEOs of some the largest US chip manufacturers lobbied Congress to pass legislation including $52B in incentives for the semiconductor industry. The US House and Senate have been wrangling with how to combine their different version of the legislation. While the legislation has in general bipartisan support, there are a few sceptics, the most prominent one being Bernie Sanders from Vermont.

https://www.bloomberg.com/news/articles/2022-03-23/chip-producers-say-they-re-ready-to-go-bigger-and-faster

## Global Neon Gas Production Falls off a Cliff After Russia's Invasion of Ukraine

**Sam Shead**, CNBC

A few companies in Ukraine supply about 50% of the global neon gas used in the ArF (argon fluoride) excimer lasers which are crucial in the lithography machines. Russia's ongoing in Ukraine could see the production of neon fall to dangerously low levels at a time when the world is already struggling with chip shortages.

https://www.cnbc.com/2022/03/25/russia-ukraine-war-laser-neon-shortage-threatens-semiconductor-industry.html

## Shanghai Lockdown and its Impact on Global Economy

**Laura He,** CNN Business

Shanghai, the largest and most affluent city in China, is in lockdown while it tries to contain an outbreak of COVID-19 following its central government's "dynamic zero covid" policy. With more than 800 multinational corporations having their regional or country headquarters in Shanghai, the lockdown will ripple through the world economy. TSMC, for its part, runs a major semiconductor factory in Shanghai's suburb. Top Chinese chip makers SMIC and Hua Hong Semiconductor have factories in Pudong, in the east of the city.

https://www.cnn.com/2022/04/13/business/shanghai-lockdown-global-economy-explainer-intl-hnk/index.html

## Is it Time to Buy Semiconductor Stocks?

**Ian Bezek,** US News

Semiconductors have started off 2022 on the wrong foot. Through mid-April, many of the stocks have been down for more than 20%. This is of course after significant stock growth in 2020 and 2021 amid the pandemic. Is this an opportunity to buy? The author recommends eight companies amid rising inflation in the US and global chip shortages.

https://money.usnews.com/investing/stock-market-news/slideshows/best-semiconductor-stocks-to-buy-amid-a-global-chip-shortage

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**You are invited to submit events of interest for this calendar. Please send to lindad@spie.org.**