

PHOTOMASK

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Best Paper of EMLC 2012

Correcting Image Placement Errors Using Registration Control (RegC®) Technology In The Photomask Periphery

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1. ABSTRACT

The ITRS roadmap specifies wafer overlay control as one of the major tasks for the sub 40 nm nodes in addition to CD control and defect control. Wafer overlay is strongly dependent on mask image placement error (registration errors or Reg errors).¹ The specifications for registration or mask placement accuracy are significantly tighter in some of the double patterning techniques (DPT). This puts a heavy challenge on mask manufacturers (mask shops) to comply with advanced node registration specifications. The conventional methods of feeding back the systematic registration error to the E-beam writer and re-writing the mask are becoming difficult, expensive and not sufficient for the advanced nodes especially for double patterning technologies.

Six production masks were measured on a standard registration metrology tool and the registration errors were calculated and plotted. Specially developed algorithm along with the RegC Wizard (dedicated software) was used to compute a correction lateral strain field that would minimize the registration errors. This strain field was then implemented in the photomask bulk material using an ultra short pulse laser based system. Finally the post process registration error maps were measured and the resulting residual registration error field with and without scale and orthogonal errors removal was calculated.

Continues on page 3.

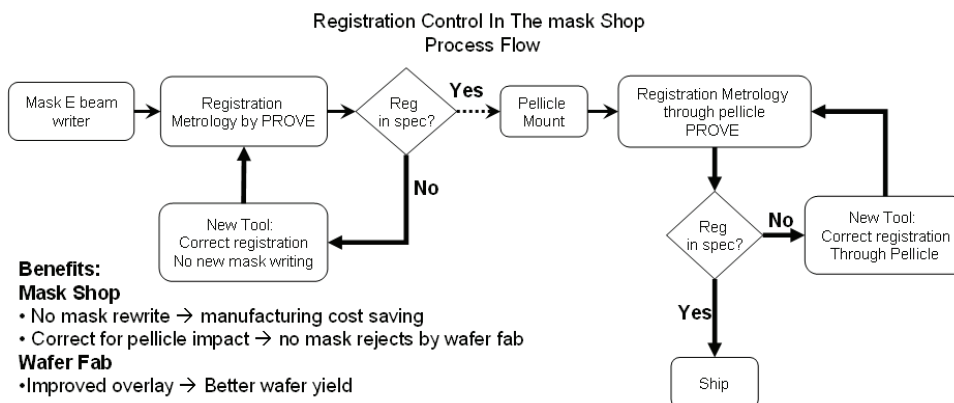


Figure 1. RegC® process flow.

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EDITORIAL

PMJ is back on track – How about the EUV?

Glenn R. Dickey, Shin-Etsu MicroSi, Inc.

It is good to see that Photomask Japan has returned after the tragic events of last year which forced the cancellation of that conference. We are hoping the strong relationship with SPIE and BACUS will be resumed and Photomask Japan can continue their role as a forum for technical achievements in the photomask industry. While the conference has resumed, we must not forget that recovery in the affected areas is far from complete. The needs of the Japanese people are still great; they can certainly use our help in many ways as they continue rebuilding their country.

As the upcoming edition of PMJ would remind us, a few years ago EUV was targeted for 32nm. Evidently, nothing came out of this. EUV is now being considered for 20nm, or perhaps 14nm, or even beyond, and at those nodes, only for limited applications for critical layers. The question remains: would it need to be pushed even more to 10nm? If EUV is indeed delayed to 14nm or 10nm, what will be the mask technology to continue Moore's Law for the earlier nodes? It looks like it will fall on optical mask technology at 193nm using all of the possible litho schemes to push optical resolution down to 20nm, or even to early 14nm, and possibly beyond, while the industry waits for the EUV roadblocks to be cleared. One of the past Editorial comments has suggested optical mask blank inspection has had somewhat of a holiday, meaning future inspection R&D investments were going to EUV. Now Optical lithography is being asked to fill in the gaps while EUV blank inspection finds a way to detect 40nm – 20nm defects. Is there a path forward to fill in the inspection gap for optical lithography at 50nm – 40nm while EUV inspection continues to develop? Artur Balasinski has written in this newsletter about the EUV Inspection roadblocks and the increasing complexity of the mask. This complexity will continue for optical lithography as well. I am told there are ways to inspect the current patterned mask to detect printable defects and then repair them and that there are necessary tools to provide defect free masks for wafer production. However, the gap is still the blank inspection. Inadequate blank inspection will result in poor mask yield and high repair costs. One would hope the technology being developed for EUV detection of small defects can be applied to the current optical technology inspection tools? John Burns and Mansoor Abbas of Synopsys in their paper "EUV Mask Defect Mitigation through Pattern Placement" (BACUS Newsletter October 2010) suggest a scheme of pattern avoidance; this will work for as long as you know where the printable defects are on the mask blank. The inspection gap question for optical mask blanks needs to be answered in 2012-2013 if optical masks are to fill in the gap until EUV is production ready. I am confident there are innovative engineers and ways to close this gap and keep the mask industry going forward.

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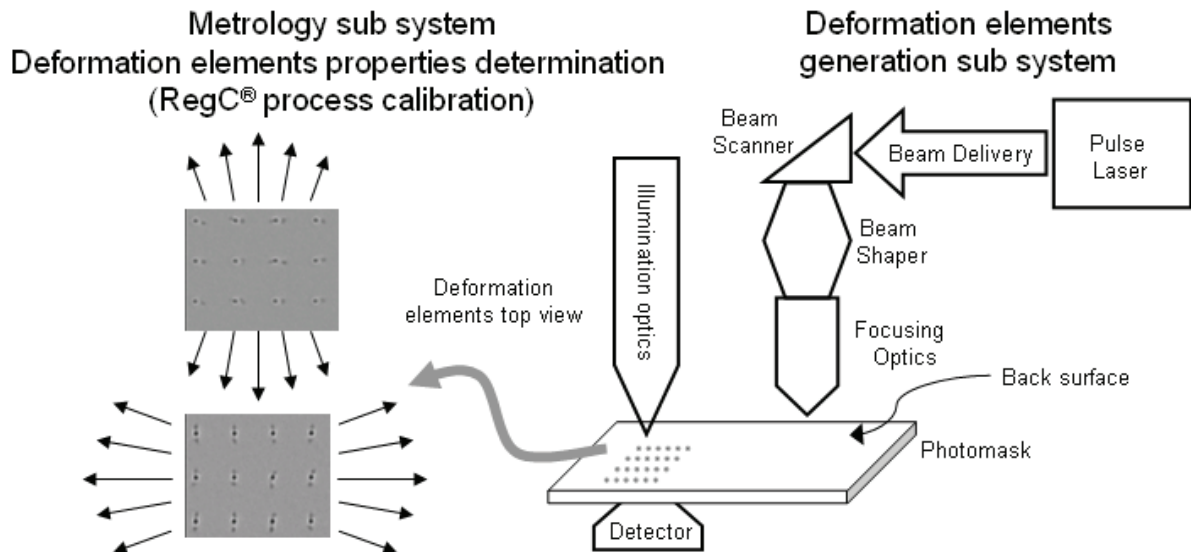


Figure 2. RegC[®] block diagram of the tool main components.

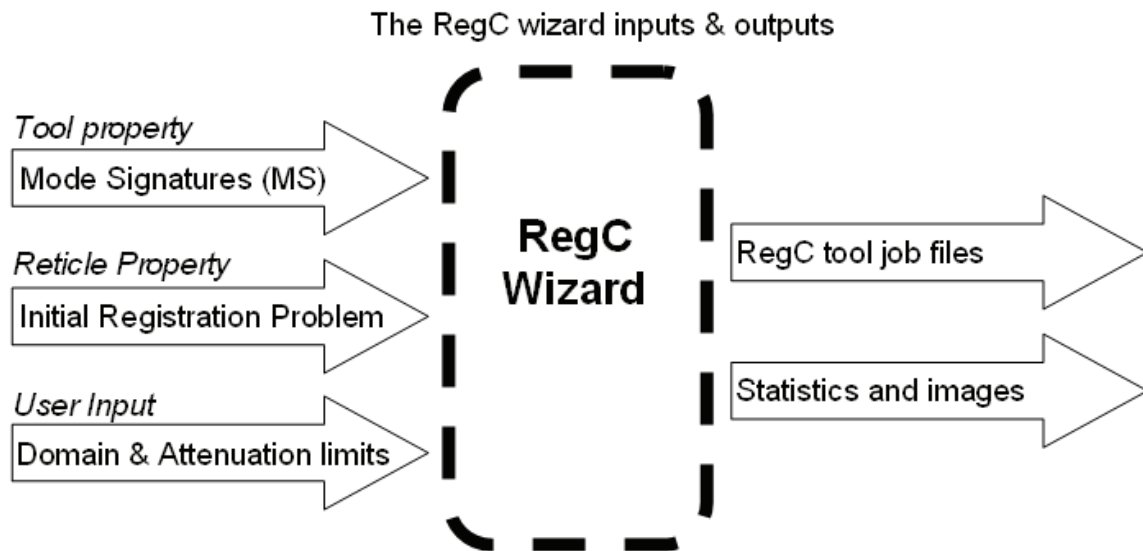


Figure 3. The basic inputs/outputs of the supporting software - RegC wizard.

In this paper we present a robust process flow in the mask shop which leads up to 32% registration 3sigma improvement, bringing some out-of-spec masks into spec, utilizing the RegC[®] process in the photomask periphery while leaving the exposure field optically unaffected.

2. Introduction

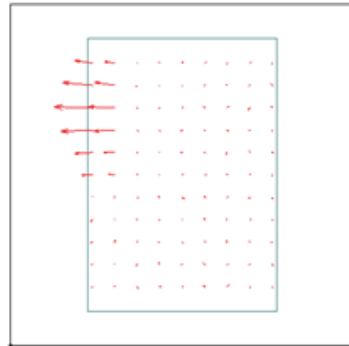
For the advanced nodes and double patterning photomasks manufacturing is becoming more and more demanding. The E-beam writers are pushed to their limits regarding image placement performance. Currently, if a mask is rejected because of image placement is out of specification, there is no way to correct for it. The mask has to be scrapped

and must be rewritten again Carl Zeiss SMS has developed a new technology named RegC[®] which enables the user (mask shop) correcting the global registration errors and improving the image placement of a manufactured mask. The process is based on a fs laser technology similar to the technology used in the CDC tools of Carl Zeiss for CD Uniformity correction.^{2,3}

The RegC[®] (Registration Control) process enables the mask maker to improve the registration performance of a mask or to bring a mask which is out of specification into specification. As a result the mask manufacturing yield is increased. Figure 1 shows the basic Registration Control process flow in the mask shop.

Example of registration compensation capabilities by scanner

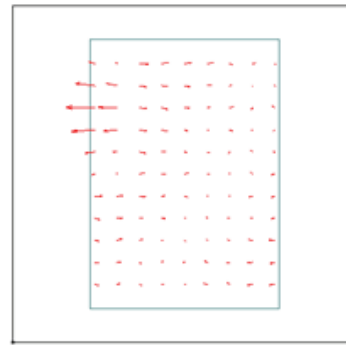
(4a) Registration error - Raw



$$X_{\text{Min}} -11.96, X_{\text{Max}} 2.00, X_{3\text{S}} 7.25$$

$$Y_{\text{Min}} -0.99, Y_{\text{Max}} 1.48, Y_{3\text{S}} 1.51$$

(4b) Registration error - S\O



$$X_{\text{Min}} -9.91, X_{\text{Max}} 3.04, X_{3\text{S}} 6.33$$

$$Y_{\text{Min}} -0.55, Y_{\text{Max}} 0.90, Y_{3\text{S}} 1.01$$

Figure 4a Shows the raw registration error. Figure 4b shows the registration error after S\O removal. Note that the large vectors on the top left have been reduced in magnitude but not significantly.

Table 1. Differences between the measured and predicted registration error 3 Sigma's.

Mask Number	3 Sigma values in nm after Scale/Ortho removal					
	Actual Measured Post		Predicted Post		Difference	
	X	Y	X	Y	X	Y
1	7.20	10.80	7.45	10.64	-0.25	0.16
2	5.90	11.30	5.76	10.56	0.14	0.74
3	6.40	11.60	6.64	10.88	-0.24	0.72
4	6.60	8.10	6.49	7.83	0.11	0.27
5	5.30	5.50	5.04	4.76	0.26	0.74

Figure 2 shows the RegC[®] block diagram. The system has two main optical sub systems. The first sub system is used to generate the deformation elements (pixels) utilizing an optical setup that includes the following main components: Pulse laser, beam delivery path, beam steering device and a focusing optics. The second sub system is a metrology system that is used to measure and characterize the properties of the generated deformation element, so-called "Mode Signature" (MS). The Mode signature will be then used as one of the inputs for the RegC[®] job computation by the dedicated software named RegC Wizard. Figure 3 shows the basic inputs and outputs utilizing this supporting software.

In this paper "fused silica", "quartz (Qz)" and mask "blank substrate" are used interchangeably.

3. The Registration Control (REGC) Principles

Intra volume laser writing at certain conditions creates a predictable deformation element in the quartz (Qz) material. This deformation can be described by a physical-mathematical model that well represents the deformation caused by RegC[®] element.

The deformed zone inside the Qz bulk is a 3 dimensional volume of fused silica which has a slightly different morphological organization of the atoms with a slightly less dense packing, or lower density. The zone with lower density expands and pushes away the adjacent atoms and thus deforms the whole bulk of the Qz piece. Due to the elastic amorphous property of fused silica this deformation

The basic RegC[®] principle

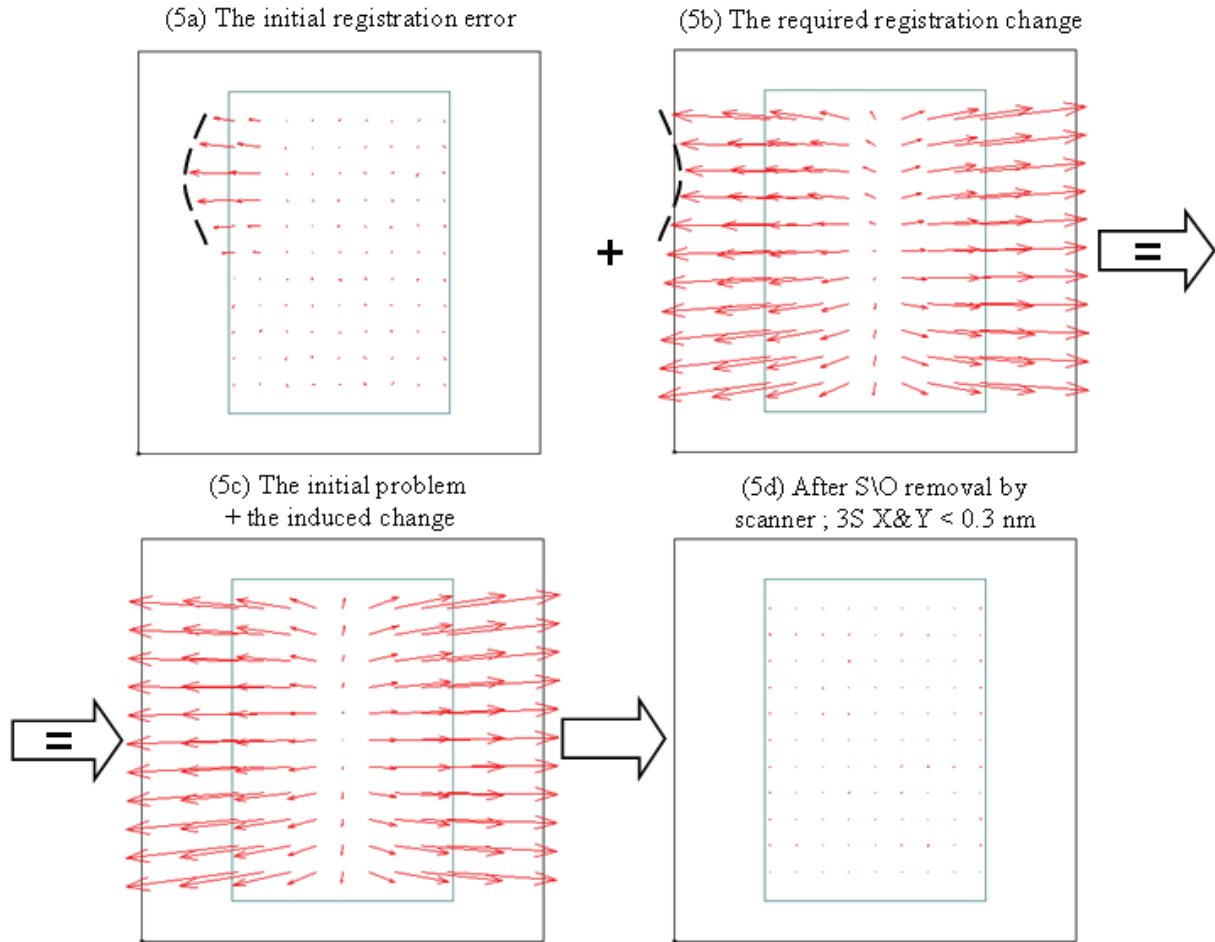


Figure 5a shows the initial registration error (raw). Figure 5b shows the required registration change in order to bring all the errors to a correctable field. The post process registration error shown in Figure 5c is the vector summation of the initial error and the induced change. Figure 5d shows very low residual error after S/O removal by scanner.

behaves almost truly elastically without critical breakage (cracks).

In other words, when considering very small deformations in the order of ppb and even ppm, fused silica behaves practically like rubber, elastically.

The special model that was developed to describe the accumulative effect of multitude pixels generated inside the Qz substrate takes into account the physical properties of fused silica such as its Young Modulus, its Poisson ratio etc. The model has been verified experimentally and provides a laser-material associated parameter, called the Mode Signature (MS). The MS defines the magnitude and angle/direction of the deformation induced by writing a laser pixel at given conditions.

The Mode Signature can be used first to calculate and predict the deformation and hence the affect on registration by writing a given array of pixels. Second and relevant for the RegC[®] process the MS can be used to calculate a

set of pixels needed to compensate for a given registration error map.

The current RegC[®] process can only induce expansion pixels. This means that the average mask dimension after the RegC[®] process will always be larger than before the process. This also means that the absolute value of registration after RegC[®] will typically be higher than the absolute registration error before the process, except for rare cases where the whole mask error was contracted relative to the target. However this is not a limitation since the target of the RegC[®] process is not to compensate for the absolute registration errors, but rather to remove only the non compensable errors as systematic linear errors which have rotational, orthogonal and scale components (in short "Scale and Ortho"). The main issue with registration errors of masks is the non compensable residuals, the registration errors which are left over after the scanner has done its job. These residuals are typically 6-8 nm 3S in advanced 40nm

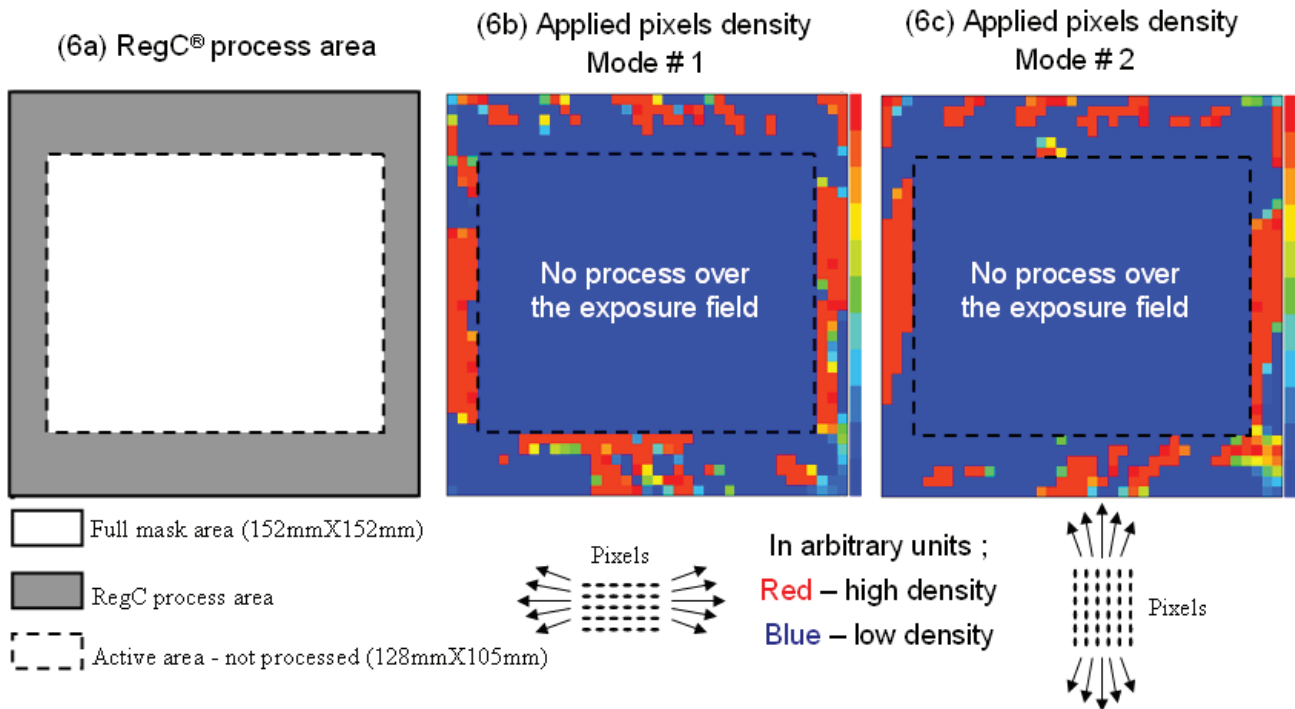
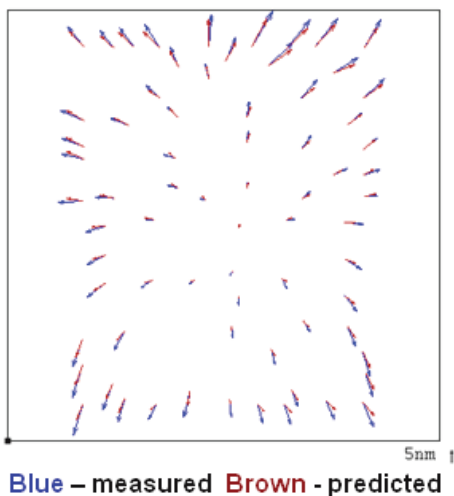


Figure 6a shows the selected area of processing over the mask. Figure 6b shows the first mode lateral pixels density distribution along with the associated deformation direction. Figure 6c shows the lateral pixels density distribution in the case of the second complementary mode utilization.

Measured and predicted registration change



Very good agreement ; $R^{*2} = 0.94$

Figure 7. The actual versus predicted registration change due to the RegC[®] process.

nodes and below. However the specs at these nodes are 4–8 nm and in sub 20 nm nodes can go down to < 4nm, especially in double patterning technologies. Therefore the task of the RegC[®] process is to decrease these non compensable residuals from ~8 nm to ~4 nm, or about 50% improvement in the 2X and 1X nodes.

Because of the importance of the scanner ability to compensate for scale and ortho, all registration metrology tools report in addition to raw registration errors also the scale and ortho (S/O) removed residual errors. These are the values which typically interest mask makers and their fab customers who are interested eventually at mask to mask overlay in the scanner.

The capability of the scanner to remove specific registration errors is shown in Figure 4 as an example.

The basic principle of RegC[®] is to take the registration error (“the problem”) shown in Figure (5a) and apply the required registration change shown in Figure (5b). The vector summation of those two will result in a new state shown in Figure (5c) that will enable higher capabilities of the scanner to remove residual errors by applying S\O as shown in Figure (5d).

4. Experimental Results

Six OMOG (Opaque MoSi On Glass, binary photomask material developed by Shin-Etsu, IBM and Toppan) production plates (28nm) were measured by a registration tool as an input for the RegC[®] job computation. The registration measurement error was estimated as 0.8 nm (long term

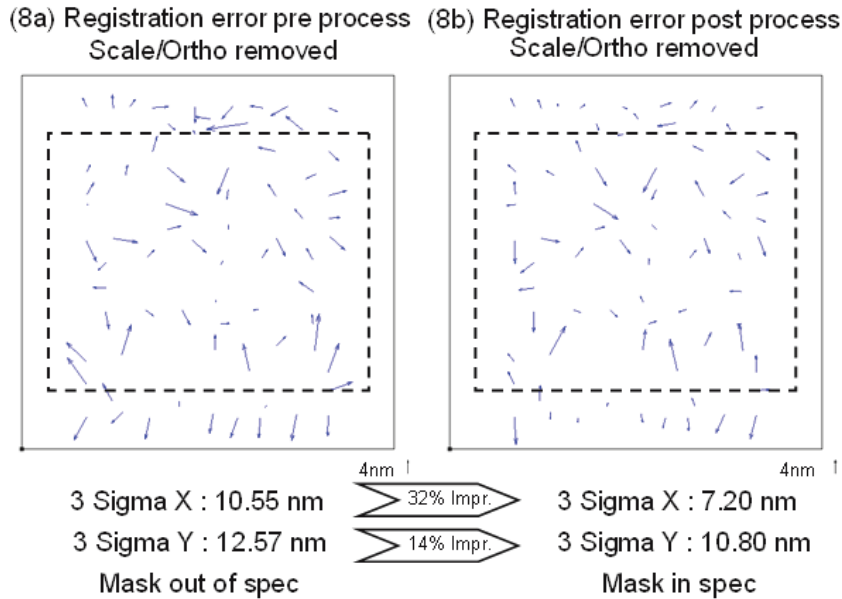


Figure 8. Pre (8a) and post (8b) RegC® process registration errors of mask number 1.

Table 2. Pre and post RegC® registration error 3 sigma and the associated percentage of improvement.

Mask Number	3 Sigma values in nm after Scale/Ortho removal					
	Pre RegC		Actual Post RegC		% Improvement	
	X	Y	X	Y	X	Y
1	10.55	12.57	7.20	10.80	32	14
2	6.80	12.60	5.90	11.30	13	10
3	7.30	13.20	6.40	11.60	12	12
4	7.80	8.80	6.60	8.10	15	8
5	7.00	6.50	5.30	5.50	24	15

and short term error components⁴). Then a pre-calculated RegC® process was applied and the plates were measured again for “Post” process registration errors.

In order to maximize the process capabilities, the actual processing was divided into two steps; each step had its own mode signature (deformation properties). Figure 6 shows the generated RegC® jobs for mask number 1 along with schematic drawing of the associated deformation direction due to the given mode utilization. Referring to the mask’s Z direction, all the six masks were processed (creating pixels) at the quartz plate center while the spoken deformation or registration change was pre-calculated and targeted to the mask absorber level.

This experiment examined two main aspects related to

the RegC® technology; the first aspect is how accurate the physical- mathematical model is and can it predict the registration change prior to the mask processing? The second is how efficient will the process be considering the constraint of processing the mask utilizing less than 42% out of the quartz area, keeping the exposure field optically unaffected. It is important to mention that in this test we were utilizing a system which is not a dedicated RegC® system for the actual processing step.

As for the accuracy of the model, Figure 7 shows on one plot the actual measured and the predicted change in registration due to the RegC® process for mask number 1. High agreement can be visually seen and it’s been quantified by coefficient of determination $R^2 = 0.94$. Moreover,

Table 1 summarizes the 3 Sigma differences between the actual measured registration errors post process and the predicted ones by the RegC wizard where less than 0.75 nm deviation can be seen.

As for the process efficiency, Figure 8 shows mask number 1 registration errors before and after the RegC® process. 32% improvement in X axis and 14% improvement in Y axis 3 sigma were observed, bringing an out of spec mask into spec.

Table 2 summarizes the improvements achieved after the 5 masks processing. An 8% -32% improvement was seen.

5. Conclusions

It was proven that a registration correction strain field can be computed using a special algorithm and that a laser based correction method can be used to effectively reduce the registration error in the mask without affecting any other mask properties.

The above reported experiments have shown that a mask which was rejected based on its registration problem can be saved and brought into spec by treating the non active area. It is recognized that a better improvement in the order of 50% could be achieved by applying the RegC® process in the whole mask area. For this purpose Carl Zeiss has developed a new process where the whole mask area is treated. In addition, more and more chip manufacturers are now specifying not only the mask registration error but also mask to mask overlay error, which adds even more challenge to the mask maker.

6. Acknowledgments

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■ On Semi, Qualcomm, Infineon Shine in Chip Rankings

By Peter Clarke

On Semiconductor registered a 49 percent sales increase in 2011 and moved into the top 25 chip companies. Qualcomm logged a 38 percent increase in semiconductor sales in 2011. Infineon's growth from continuing operations was 29 percent, according to IC Insights. Qualcomm climbed up three places to 7th place and Nvidia up five spots to 18th due to growth in its graphics and communications processor business.

The top 10 semiconductor suppliers grew 7 percent compared to 2010. Intel, through its Infineon acquisition, extended its lead as number one over Samsung which experienced a low growth of 3 percent. Many large memory companies suffered in 2011 with Micron, Hynix and Elpida all shrinking in size and Elpida registering a sales drop of 40 percent in dollar terms and 45 percent in yen. Elpida fell six places from 13th in 2010 to 19th in 2011, IC Insights (Scottsdale, Arizona) said.

■ TSMC's March Sales Take Q1 into Annual Growth

By Peter Clarke

March sales of leading foundry Taiwan Semiconductor Manufacturing Co. Ltd. on a consolidated basis took the company's first quarter sales above the equivalent figures in 2011, to NT\$37.083 billion (about \$1.26 billion), an increase of 9.5 percent over February 2012 and a decrease of 0.6 percent over March 2011. Consolidated revenues for January through March 2012 totaled NT\$105.51 billion (about \$3.58 billion), an increase of 0.1 percent compared to the same period in 2011.

■ EDA Grew 16% in 2011

By Dylan McGrath

EDA and IP vendors posted revenue of \$1.7 billion, up 10 percent compared to the third quarter and up 12.8 percent compared to the fourth quarter of 2010. For the full year 2011, EDA and IP sales totaled \$6.13 billion in 2011, up 16 percent from \$5.28 billion in 2010, according to EDAC.

EDA license and maintenance revenue for 2011, which excludes IP and services, came in at \$4.19 billion, up 14 percent from 2010. Computer aided engineering software, CAE, generated revenue of \$644.8 million in the fourth quarter of 2011, up 11.9 percent from the fourth quarter of 2010. IC physical design and verification revenue increased to \$392.4 million, up 30 percent from Q4/2010. EDAC said IP revenue grew to \$432.2 million in Q4, up 13.4 percent from Q4/2010. Services revenue totaled \$90.9 million in the quarter, up 9.8 percent from Q4/2010. Printed circuit board and multi-chip module revenue in Q4/2011 was \$139.7 million, down 15.6 percent from Q4/2010.

■ EDA Tool Aims at 10-Nanometer 3-D

By R. Colin Johnson

Reaching the advanced semiconductor process nodes at 22-nanometer and beyond requires accurate three-dimensional (3-D) models of the proposed physical structures. One of the few tools capable of modeling the ultra-compact structures of FinFETs and other 3-D transistor structures is SEMulator3D. IBM, for instance, has chosen SEMulator3D to design its FinFETs at the 22-nanometer node and beyond. The software can model the micro-electro-mechanical structures on the most advanced semiconductors such as this FinFET SRAM cells with a high-K metal gate.

The latest iteration of SEMulator3D 2012 supports 64-bit voxels (3-D pixels that can be filled with any semiconductor material) enabling ultra-accurate modeling of 3-D semiconductor structures at advanced processing nodes. With 64-bit precision, it is possible to achieve extremely fine details for designs beyond the 28-nanometer node.

■ Major Chip Maker Orders Optics for EUV Lithography

By Peter Clarke

Zygo Corp. has been awarded a \$2 million order to produce advanced extreme ultraviolet (EUV) optics from 'a major semiconductor company'. Completion of order will take nearly two years and is likely to be for use in the development of EUV lithographic process technologies.

The order is associated a microexposure tool research project called MET-5 being conducted by Sematech at the College of Nanoscale Science and Engineering (CNSE) at the University of Albany in New York State. The upgraded optics will help researchers achieve line widths of less than 16-nm in support of process development out to the year 2025, Zygo said.

The order is a follow on to a \$9 million order given to Zygo by CNSE and Sematech to develop optics for MET-5 in support of EUV resist and EUV mask developments. The development and production of the EUV mirror system are expected to take 22 months.

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About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

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