
PHOTOMASK

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EMCL10 Best Paper

E-beam induced EUV photomask repair – a perfect match

M. Waiblinger, Carl Zeiss SMS GmbH - Carl-Zeiss-Promenade 10, 07745 Jena, Germany

K. Kornilov, T. Hofmann, and K. Edinger, Carl Zeiss SMS (NaWoTec GmbH) Industriestr. 1, D-64380 Rossdorf, Germany

ABSTRACT

Due to the updated ITRS roadmap EUV might enter the market as a productive solution for the 32 nm node.¹ Since the EUV-photomask is used as mirror and no longer as transitive device the severity of different defect types has changed significantly. Furthermore the EUV-photomask material stack is much more complex than the conventional 193nm photomask materials which expand the field of critical defect types even further. In this paper we will show, that “classical” 193 mask repair processes cannot be applied to EUV material. We will show the performance of a new repair process based on the novel ebeam repair tool MeRiT® HR 32. Furthermore this process will be applied on real EUV mask defects and the success of these repairs confirmed by wafer prints.

1. Introduction

The cost involved in the production of photolithographic masks makes up an increasingly larger portion of the semiconductor industry as the technology node decreases. EUV has been discussed to be key for next-generation production techniques for several years. Issues like the EUV source, EUV resists and mask-defects have kept engineers and researchers busy for some time now. Remarkable progress was achieved for the EUV sources, where defect free masks is still a major challenge. It can be expected, that the first EUV pilot lines will go online 2-3 years from now.

From a mask maker point of view mask defects are not a new topic but the requirements for EUV are much different than for 193 nm mask types. Since the EUV-photomask is used as a mirror and no longer as a transmission device the severity of different defect types has changed

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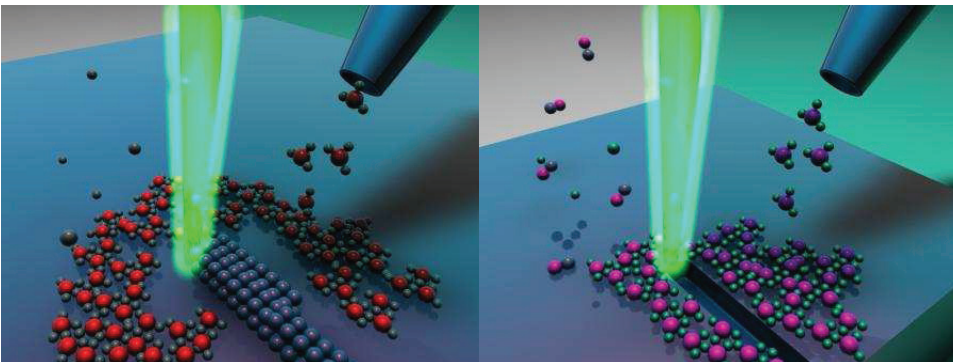


Figure 1. Basic principle for photomask repair: First the precursor molecules are adsorbed on the mask. The exposure with a focused electron beam can either start a reaction, which immobilize the precursor (deposition) or reacts with the substrate to a volatile product (etching).

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EDITORIAL

Bifurcation

(bi•fur•ca•tion /bī-fer-'kā-shen/ n. the division of something into two branches or parts.)

By Michael D. Archuletta, RAVE LLC

You know you've been in the mask industry too long when history starts repeating itself for the third time. In the mid-80's we all thought the semiconductor industry was finally "maturing." Then everything stalled in '89. Luckily, phase shift technology carried us forward and we began to get comfortable again. The 1990's lulled us to sleep with a decade of solid predictable growth and then POW, the crash in 2000. We recovered and starting talking about how we would never let that happen again. Boy, were we wrong. This past two years has been the worst ever, especially for mask makers and equipment suppliers. But that's not what I want to talk about.

I'd like to discuss what I see as the latest and perhaps the biggest yet mask industry 'bifurcation.' I'm of course referring to the perennial technology gap between Merchant and Captive mask makers from an equipment manufacturer's perspective.

Because it's my job, I do a lot of global market research and I'd like to share some interesting trends. Three years ago, the industry was hell-bent for 45nm device production, expecting by 2010 to leave the 90nm technology node to the history books. The device design forecast in 2007 showed the entry curve for 65nm and 45nm device designs right on Moore's timeline. That hasn't exactly "panned-out." Except for the top five Independent Device Manufacturers (IDMs), the global industry has been slow to adopt 65nm-45nm.

It's no secret we live in an industry where "those-who-can-afford-it-will-be-first-to-do-it." Not to mention that's been exacerbated by the recent global economic meltdown. But the push into sub-90nm technology nodes really has seen some unprecedented cost factors. Compared to 90nm, claims are a 65nm device design costs four times more to bring into production. The latest ITRS report estimates a 45nm device design is eight times more expensive. This kind of cost/price differential makes it tough not only on the device makers, but also on the price/performance proposition for device buyers.

Furthermore, at the 90nm node some other interesting things began to happen. For instance, logic speed and memory density aside, the demand for miniaturization by the electronics industry began to subside at 130nm and has flattened at 90nm. For example, cell phone keyboards don't need to get smaller, because fingers aren't getting smaller. So at least for the moment, one of the drivers for high-function smaller devices has lessened. There have also been recent advancements in 3D (multi-layer) components using 90nm technology. Device designers have become very comfortable at 90nm. During the previous "good times" a lot of money went into 90nm production technology and every yield chart shows the entire industry is really good at it.

Don't get me wrong. I'm not saying the semiconductor industry will not continue to push the technology size limits, but the emphasis is not so much to make devices smaller but to give the same size device more functionality (e.g. Quad-Core). Most of the large IDMs are working on technology roadmaps to sub-22nm using optical lithography. Of course the jury is still out on exactly how to get there (DP? Imprint? EUV? Direct Write?).

The point is, for now and the next few years, the bulk of the electronics industry demand is being served very well by ≥ 90 nm technology node devices. Recent forecasts bear this out. Surprisingly, the demand for ≥ 90 nm devices is not diminishing but growing. In bygone days, the reticle forecast for older technology nodes diminished proportionately to the ramp of new technology node production. Granted, the latest worldwide reticle forecast does show 65nm Compound Annual Growth Rate (CAGR 2008-2013) at ~36%. However, that same forecast is showing 90nm growing at a 19%+ pace. In fact, 130nm CAGR is not diminishing, but hanging in there flat at 1% growth. When you further analyze the forecast reticle volumes, the real story emerges. Year-to-year total worldwide mask volume remains flat at ~600K masks, but the demand for 90nm masks is forecast to double between now and

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Figure 2. To enable mask repair for the upcoming nodes a new ebeam based mask repair tool was developed called MeRiT® HR 32.

significantly. Furthermore the EUV photomask material stack is much more complex than the conventional 193nm photomask materials which expand the field of defect types even further. For the transition phase from 193 nm to EUV it is extremely helpful to have a defect repair tool, which can be used for the classical 193 nm and EUV technology.

Over the last years photomask defect repair by focused electron beam induced processing using the Zeiss MeRiT® MG 45 tool has become standard in practically all high-end mask manufacturing processes. This technology employs a high-resolution electron beam to induce a local chemical reaction on the mask surface. A suitable precursor gas is dispensed through a nozzle in close vicinity to the incident beam (Figure 1). Depending on the precursor chemistry, a reaction is induced by the electrons, leading to either a deposition caused by fragmentation of precursor molecules or to a reaction between the adsorbed molecules and the substrate material, resulting in volatile products and thus etching of the substrate material. The reaction is confined to the area exposed by the electron beam, so this technique allows high-resolution nanostructuring.

The MeRiT® electron beam mask repair tool provides many benefits over other mask repair techniques. These benefits have been addressed in previous papers and include the lack of irradiation damage that arises with FIB based tools, including physical sputtering and ion implantation, as well as the ability to perform repairs without creating debris, as is the case with AFM based repair techniques.^{2,3,4} The MeRiT® ebeam repair tool is the only repair tool that can perform both clear and opaque repair on a wide variety on masks.⁵

For the upcoming technology nodes the required accuracy for an ebeam based mask repair tool is quite high. Furthermore it can be expected that new mask materials will enter the market, which might require new processes and new chemistry. To serve these needs a new tool has been developed called MeRiT® HR 32 (Figure 2). The MeRiT® HR 32 is a completely redesigned tool. Due to the reduced mechanical and electronic noise, reduced drift and a small beam diameter the tool can perform high-resolution repairs. The new developed precursor management allows handling “exotic” materials and enables even very complex sequences.

3. Experimental

E-beam based mask repair is well established in any state of the art mask making technology for 193 nm photomasks. The first obvious test to apply 193 nm etches process on EUV material was not successful (figure 3). Once the absorber material is etched parasitic degradation is induced. This process continued over hours until the pattern fidelity is no longer sufficient.

Investigation with a tilted SEM showed, that the absorber dissolves between the capping layer and the anti reflective layer forming a cavity as depicted in figure 4. It is obvious, that this kind of repair technology cannot be used for any productive process.

There have been attempts to suppress spontaneous etching behavior by executing a two-step process. First the defect is repaired then the surface is passivated. For passivation, the repaired area is flooded with a passivation precursor and exposed by the electron beam again. This technology works does not work in a production environment. The reason is that the spontaneous etching modifies the sidewall on a minute timescale. For realistic

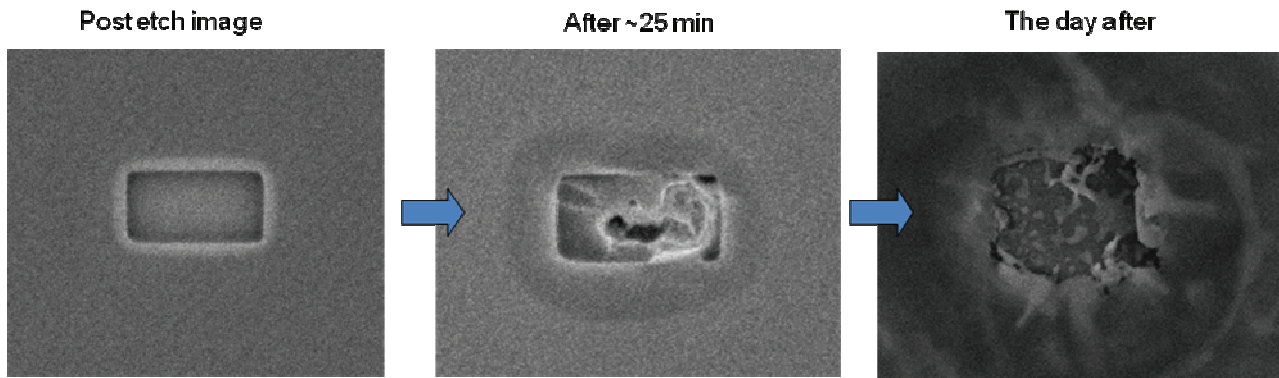


Figure 3. Basic 193 nm etch technology applied on EUV material shows strong and uncontrolled degradation of the absorber material.

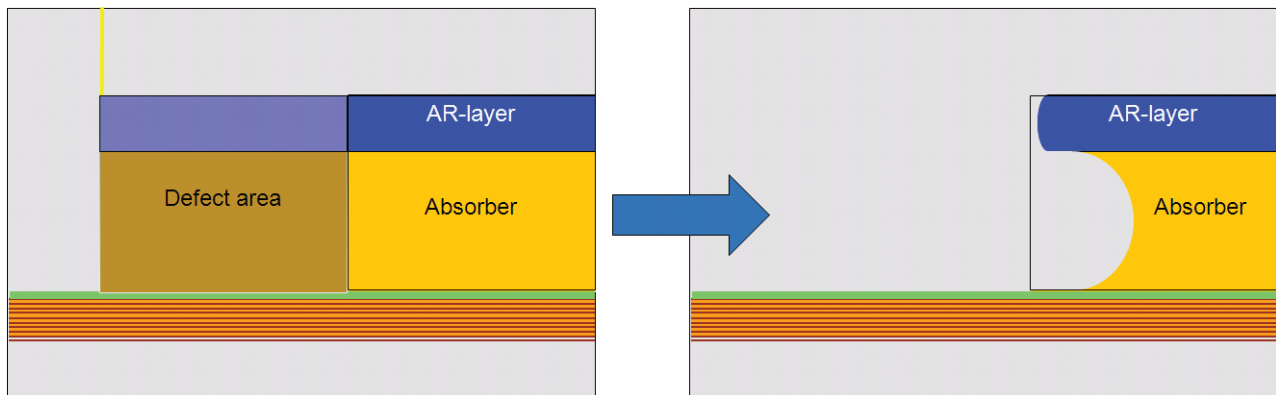


Figure 4. Basically all EUV absorber materials show parasitic degradation if etched with established etch chemistry for 193 nm photomasks.

repairs it is not unusual, that a repair takes longer than unwanted side effects need to affect the mask integrity. If the absorber degenerates faster than the repair itself it is impossible to perform a successful repair. Assuming very small and fast repairs still have the problem, that the most important area, which needs passivation is the sidewall. In best case the ebeam comes parallel to the sidewall. So at the sidewall, where passivation is most critical the passivation process has the lowest efficiency. Last but not least the passivation layer can be effected by the etch process itself. In mask production it is likely that there is more than one defect on the mask. Even if a repair was performed successfully and the defect area was passivated successfully the repair of a second defect can destroy the passivation.

This is depicted in the upper part of figure 5. In this row a large contact hole was etched into the absorber and then passivated. This process was repeated 3 times at different position from left to right. It can be observed clearly, that the first contact hole has a big “aura” which is also visible in the middle contact hole. This “aura” is due to a growing cavity below the antireflective layer. This very basic experiment shows the limitation of the two-step etch / passivation process.

To get to a process, which is more applicable in a productive environment Carl Zeiss developed a new etch process which has no spontaneous etching. Therefore passivation with all the implications is no longer required. In the lower section of figure 5 the same etch sequence was performed with the new process. None

of these etched contact holes shows an “aura”. Since the SEM image in was taken after all 6 contact holes have been etched it shows that the new process is soft enough not to damage the passivation of the first row.

To quantify the process the etch selectivity was derived. Therefore a series was etched into the EUV mask material where the etch time was varied in a laboratory environment. The depth of the etched area was than measured using AFM (see figure 6). It can clearly be seen, how first the antireflective layer is etched then the absorber itself before the etch speed slows down on the Ru-capping layer. To derive the etch selectivity the different slopes are fitted assuming a linear behavior. The so derived etch selectivity is better than 75:1.

An example for a successful EUV mask repair is depicted in figure 7. The upper left image shows a SEM image from a mask with a particle defect embedded in a sidewall line. From a repair point of view a particle defect is much more complicate than a standard absorber defect. This mask was printed and measured again on the wafer using SEM depicted in the lower left image. It can be clearly observed that the particle defect prints on the wafer. Then the mask was repaired and measured again with SEM. This is shown in the upper right image. The defect was removed almost completely. Furthermore no damage of the capping layer is visible. This so repaired mask was again printed on wafer and measured with SEM (lower right image). The wafer print confirmed that the defect was removed successfully. Furthermore no negative

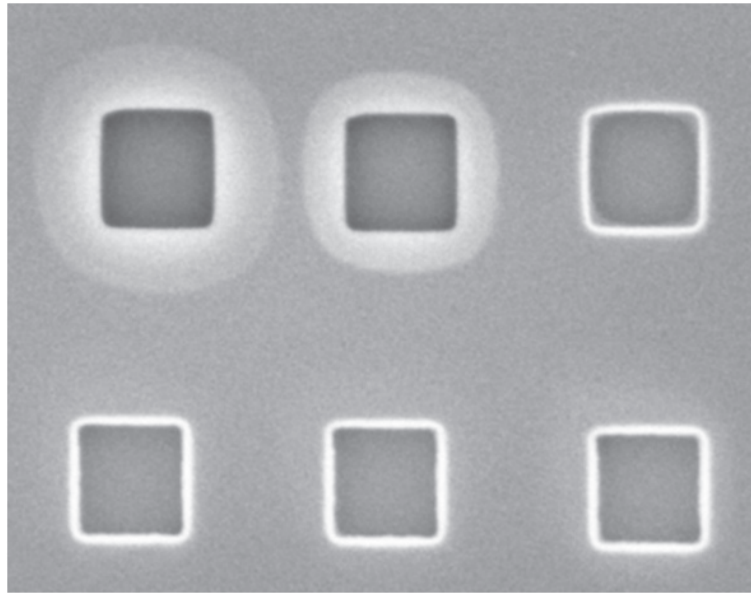


Figure 5. Two etch series have been performed. The SEM image was taken after all six boxes have been etched. The upper part was etched 1 by 1 and each hole was etched than passivated from left to right. A clear degradation can be observed. On the lower part the same experiment was repeated with the new etch chemistry. No absorber degradation could be observed in the lower part.

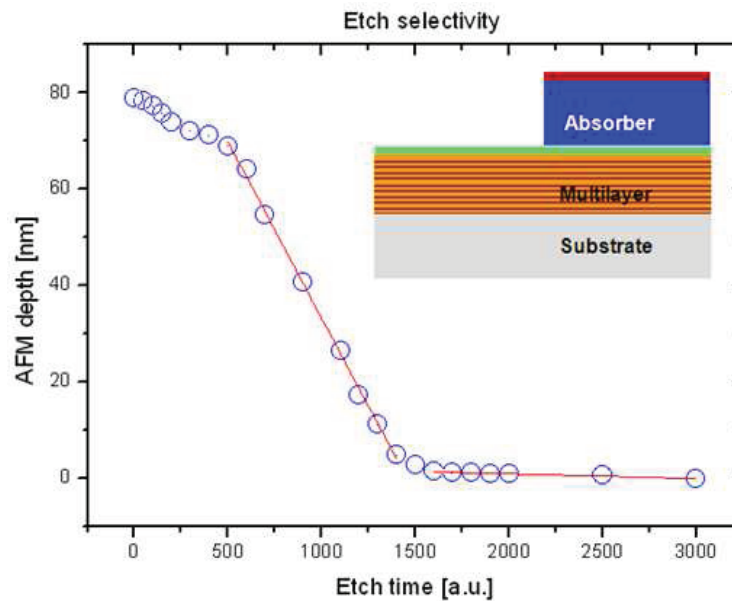


Figure 6. The etch selectivity is derived from the etch speed in the different layer. The red lines are linear fits of the etch speed in the absorber layer and on the Ruthenium capping layer. The etch selectivity is better than 75:1.

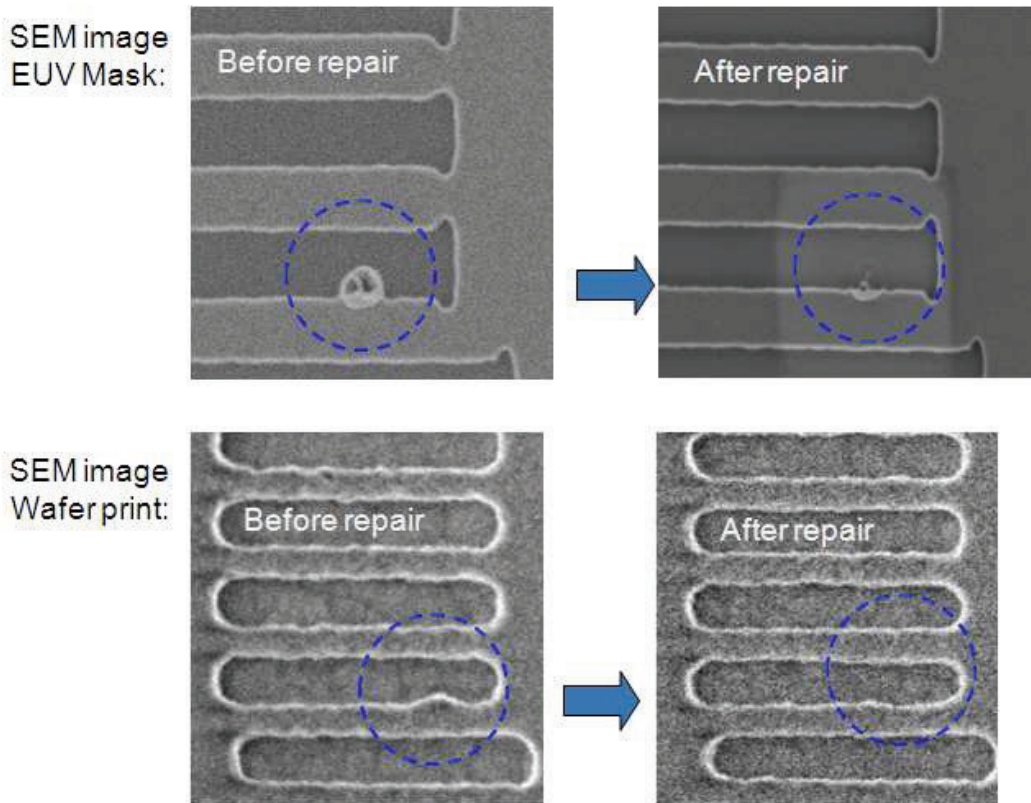


Figure 7. Example for a particle defect on a EUV mask. In the wafer print before repair shows that this defect is transferred to the wafer during the printing process. After repair the particle is removed and is no longer visible on the wafer print result.

impact of the surrounding of the repair area could be observed.

The second example shows a deposition⁶ (Figure 8). The upper left picture shows an SEM image of an absorber defect. This defect looks not so critical but in AFM (upper middle picture) it can be seen, that the absorber is thinned. In the lower left image you see an SEM image of the area as printed on the wafer. It shows that this defect is transferred during the printing process. Reason might be that the absorber material is too thin to absorb the EUV light sufficiently. This defect was repaired using a deposition process (upper right image). After repair the corresponding wafer print shows that this defect is no longer transferred to the wafer. Again no negative interference of the repair process can be observed in the surrounding of the repaired area can be observed.

4. Conclusion

The novel MeRiT® HR 32 mask repair tool has been specifically developed for electron beam induced photomask repair for 32nm and below for 193nm and EUV lithography. The significantly improved tool stability together with a new gas management system allows the development of new repair processes especially for EUV masks.

It was shown, that the well established repair processes for 193 nm masks of the previous MeRiT® MR 45 tool generation cannot be applied to EUV mask material due to parasitic degradation. The new MeRiT® HR 32 allowed the development of new EUV repair process avoiding this effect. It was shown, that this process has a very broad process window. Furthermore this process can be controlled in a way that the capping layer between the absorber

material and the reflective multilayer is not damaged. The ebeam based MeRiT® HR 32 mask repair tool enables accurate, stable and damage free repairs for 193 nm and EUV mask types, both, for the repair of clear and dark defects.

5. Acknowledgment

Thanks a lot for the hard work and effort of Ted Liang, Sang Lee and Michael Leeson from Intel Corporation.

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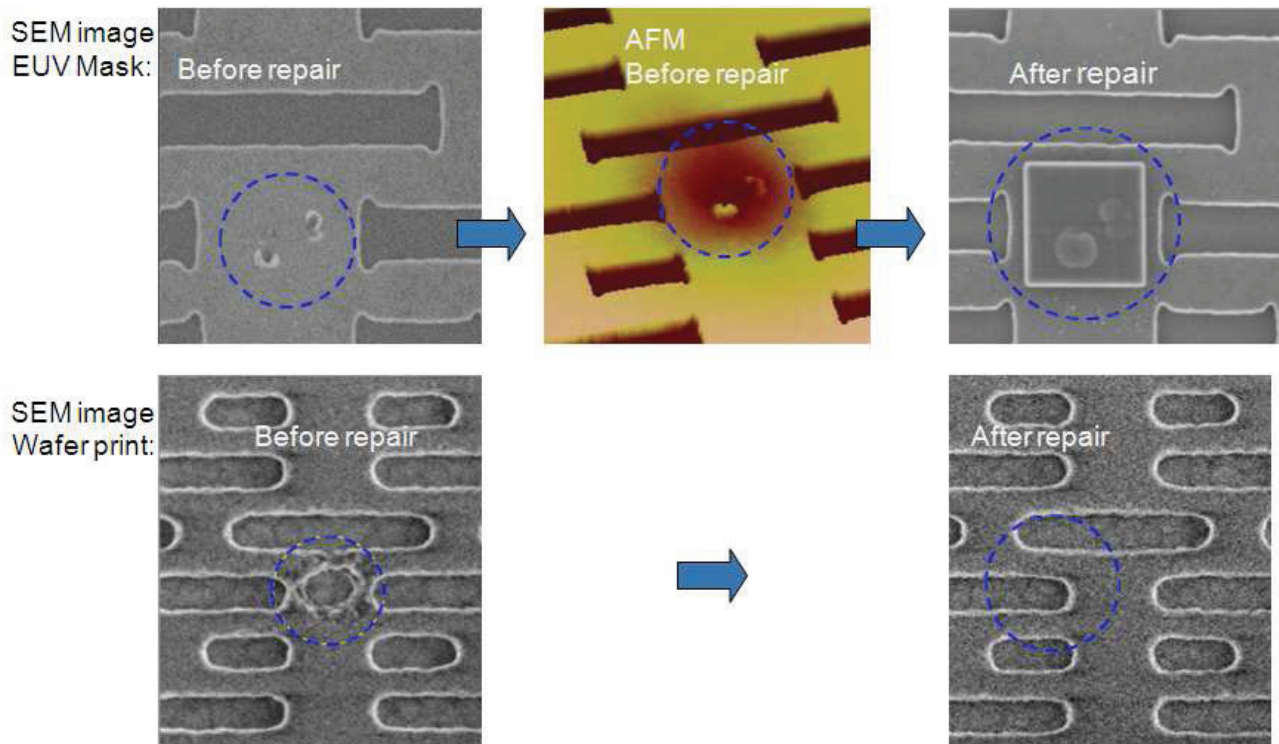


Figure 8. Example for deposition. Where the defect is almost invisible in SEM, AFM shows that the absorber is too thin, which is confirmed in the wafer print. After deposition the defect is no longer transferred to the wafer.

EDITORIAL *(continued from page 2)*

2013. When you add-up mask volume demand for 90nm, 130nm and 180nm masks, those three categories alone represent ~50% of the total demand. Through 2013, $\leq 45\text{nm}$ mask demand is only predicted to represent less than 4% of the total volume. The captive mask shops already have that kind of production capacity in place.

For most commercial mask shops, 65nm mask making is a low-yield challenge. 45nm mask making is possible but at the ragged edge of their equipment capability. All this $\geq 90\text{nm}$ mask demand should be good news for merchants, plenty of work for which they have existing equipment. Problem is the price wars over the last few years have made 90nm mask sets cheap. The reticle forecasts in fact, predict substantial drops in ASPs for $\geq 90\text{nm}$ mask sets. So even though volume may improve, revenues are likely to remain low (meaning capital budgets will remain restricted). Any merchants planning to participate in $\leq 45\text{nm}$ mask production should already be investing in next generation equipment. Trust me, their not.

Recently, many of the big captive mask shops began investing heavily in new mask making equipment. They're investing because: a.) they can afford it and; b.) because they can't afford not to. The reason IDMs maintain their own mask shops is to assure advanced mask technology

availability when it's needed. The IDM primary business model requires being first to capture premium pricing and market share. The time-to-profit trajectory for a merchant mask maker does not support capital investment too far in advance of volume production requirements. The investment lag is causing a technical gap between the merchants and captives like we've never seen before.

If this merchant/captive bifurcation continues to widen, fewer equipment buyers will be participating at the leading edge. This presents an interesting challenge for next generation equipment developers. Rising R&D costs and fewer buyers over which to amortize NRE equals substantially higher equipment prices (more bifurcation). Most equipment suppliers have come out of the downturn in "build-to-order" mode, which also means longer delivery lead-times (more bifurcation). Note that NGL equipment development has slowed appreciably and the cost/price factors being weighed are in the hundreds of millions of dollars.

As I said at the beginning, I've been around long enough to believe we'll work through this and times will improve. History backs me up on this point. But over the next five years, it's going to be very interesting watching us sort out these opportunities.

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Industry Briefs

■ Litho Generation Gap Threatens Moore's Law?

By **Mark LaPedus**, EE Times

Mark suggests that lithography is at a crossroads. Optical technology has remained viable far longer than anyone expected. Work on a successor began decades ago, however, three of the four dominant next-generation lithography (NGL) candidates - extreme ultraviolet (EUV), multibeam maskless and nanoimprint - are behind schedule. EUV, in particular, has consumed considerable R&D time and treasure but still has little to show for it, prompting calls from some circles for development efforts to be redirected elsewhere. Nanoimprint, for its part, has overlay and throughput problems, and multibeam remains in R&D. The fourth NGL candidate, directed self-assembly, is a promising research topic that is nowhere near development. The industry has long known that without a viable NGL solution - which most assumed would be EUV - Moore's Law scaling would slow and the secular growth rate of the semiconductor industry would decline. Adoption of 193-nm immersion lithography bought the industry some time to get its act together on NGL. But with timetables slipping on EUV and other next-gen solutions the top priority is still to extend 193 nm. Toward that end, chip makers are pursuing techniques such as double patterning, adding complexity and cost to an already prohibitively expensive undertaking.

ASML and Nikon have developed immersion scanners that offer higher throughput to offset double patterning's cost. But ASML has pushed back the ship date slightly for its scanner, and the two rivals are trading jabs, each claiming the other's new model does not meet advertised specifications. Once they're up to spec and available, the new scanners from ASML and Nikon could allow chip makers to extend optical lithography deep into sub-30-nm territory. But the extension of immersion to 22 nm and below is likely to add to the cost and complexity, potentially making immersion at advanced nodes uneconomical.

EUV, for its part, has been a money pit. The industry recently made the embarrassing admission that it still lacks metrology tools for EUV and now requires \$200 million or more to develop them. A preproduction EUV tool from ASML costs \$90 million. Adequate power sources for EUV aren't available, defect-free EUV masks haven't been achieved, and the resists for the technology aren't ready. Intel Corp. in 1997 led the formation of the EUV LLC consortium with a plan to commercialize the technology by 2005 for the 90-nm node, but the industry is still waiting for commercially viable EUV tools. Samsung says it believes EUV is doable by 2012, but most industry estimates put the rollout date closer to 2015. Intel now plans to extend immersion lithography down to 11 nm, and it is weighing maskless as well as EUV technology for the NGL shift.

■ Maskless Lithography - A Startup Offers Maskless Litho for PCB Production

By **Peter Clarke**, EE Times

Maskless Lithography Inc., a 2005 startup led by a group of electronics industry veterans, is offering a direct-write digital imaging technology for printed circuit board (PCB) production. The MLI-2027 direct-write lithography system is the industry's first to combine high throughput and yield with unparalleled accuracy using standard "Non-LDI" resists, the company said. Maskless also announced that contract electronics manufacturer Sanmina-SCI Corp. has accepted delivery on the first production tool after completing beta testing, validation and qualification of the Maskless MLI-2027 equipment at their San Jose facility. The company was founded by Dan Meisburger, who serves as CTO. He is joined on the executive team by CEO and president, William Elder, and COO, Edward Carignan. "In 2005, based upon our founding partners' experience in both lithography and metrology, we identified an opportunity to develop a lithography system that could deliver unrivalled value to the PCB market. We believe we have exceeded that initial vision and are now ready to share this tried and tested capability," said Meisburger, in a statement. "We are really impressed with Maskless' unique direct-write lithography tool," commented Mike Keri, vice president of operations for Sanmina-SCI, in the same statement. "The MLI-2027 has allowed us to meet highly challenging designs using conventional dry film resists at high yields and high throughput rates."

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About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

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