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3rd Place Best Oral - PM13

Your worst Nightmare – Inspection of aggressive OPC on 14nm masks with emphasis on defect sensitivity and wafer defect print predictability

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1. ABSTRACT

To prevent catastrophic failures during wafer manufacturing, mask manufacturers employ sophisticated reticle inspection systems to examine every image on every reticle to identify defects. These advanced systems inspect at resolutions typically 3x higher at the reticle-plane than advanced wafer scanners; thus enabling them to detect the small defects necessary to ensure reticle quality.

The most thorough inspection is done using a reticle-to-database comparison that ensures the reticle pattern matches the design pattern. For high defect sensitivity, the database must be carefully modeled to exactly match the reticle pattern. Further, sub-resolution OPC shapes are often at the limit of the mask manufacturing process, which adds subtle variations on such shapes across the reticle. These modeling errors and process variations can cause high numbers of unwanted detections, thereby limiting inspection system defect detection sensitivity.¹

OPC designs are expected to become more aggressive for future generations and may stress the performance of current reticle inspection systems. To systematically assess the capability of various inspection approaches and identify needed areas for improvement, a



Figure 1. "Nightmare" mask layout.

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INSIDE:

INDUSTRY BRIEFS
—see page 15

CALENDAR
For a list of meetings
—see page 16

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EDITORIAL

The Magic of Masks and Lithography

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Anton Zeilinger, the well-known Austrian quantum-physicist, recently stated “If R&D would always have focused on immediately applicable results, we certainly would have an incredible variety and sophistication of candles; but no electricity.” I cannot agree more with him. Not only as a — certainly less known — Austrian physicist, but much more as a front row witness of the shift in R&D strategies of our industry during the last 35 years. From a share holders’ & money makers’ point of view the general trend of all but a very few semiconductor companies to rather develop “another candle” in their (supposedly) safe & profitable market niches is understandable. However, the physicist in me sadly recalls the “good old times”, when a technical challenge was regarded as a chance to outperform competitors, and not as a risk to be avoided. That has been the “magic behind the gadget”, which Rick Wallace, president and CEO of KLA-Tencor, has indicated in the keynote talk at the SEMI Industry Strategy Symposium as his recipe to attract young people to science, technology and engineering. The issue definitely is not any lack of challenges. However, when financial decisions surpass technical reason, it is straightforward for competitive & bright young people to choose a career rather in business than in technology.

But there is another aspect of magic for me in particular in masks and lithography, which has and still does overcome the issue mentioned above: People have been and in general still are open to discuss and share their knowledge. Of course, some presentations show these graphs with “non-linear arbitrary units”. But I have rarely met an engineer not willing to discuss his results, as soon as he has seen my serious interest in helping him to gain a better understanding of the results’ consequences and implications. After all, masks and lithography require a multi-disciplined approach. A result clear and straightforward for a chemist could be hardly imaginable by a physicist, and both can be amazed by the assessments of an electrical engineer — let alone by the approach of an EDA code developer. Even when EUV lithography may not become mainstream and our industry may lose quite a large amount of R&D subsidies, there still will be numerous problems to be solved — maybe even more. And these problems only can be solved by the cooperation of many different and diverse minds.

As long as this kind of interaction is still possible at and promoted by the symposia of SPIE and in SPIE’s publications, I do not fear for masks and lithography to forfeit their magic. We surely need to promote this very special magic at universities, at high schools and among our friends, wherever we may encourage a young person to join our field. And we need to defend this magic of our industry against those small minds who are too greedy to share and rather risk general failure than common success.



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Column Number	Experiment Description
1	Space between vias with full common run length
2	Space between vias with partial common run length
3	Corner to corner spaces between vias of fixed sizes
4	Corner to corner spaces between vias of varying sizes
5	Space between vias and assists, full run length
6	Space between vias and assist, diagonal
7	Space between via assists
8	Space between vias in nested array structures - orthogonal
9	Space between vias arrays-staggered
10	Via corner chop 1 – Experiments with various 45 edges
11	Via corner chop 2 – Experiments with various 45 edges
12	Via corner chop 3 – Experiments with various 45 edges
13	Vias small assist study 1
14	Vias small assist study 2
15	H or I shaped Vias
16	Small Vias
17	Realistic Layout 1 with Fancy Models based Assists (SMO style assists)
18	Realistic Layout 2 with Fancy Models based Assists (SMO style assists)

Figure 2. Contact macro sample experiment table.

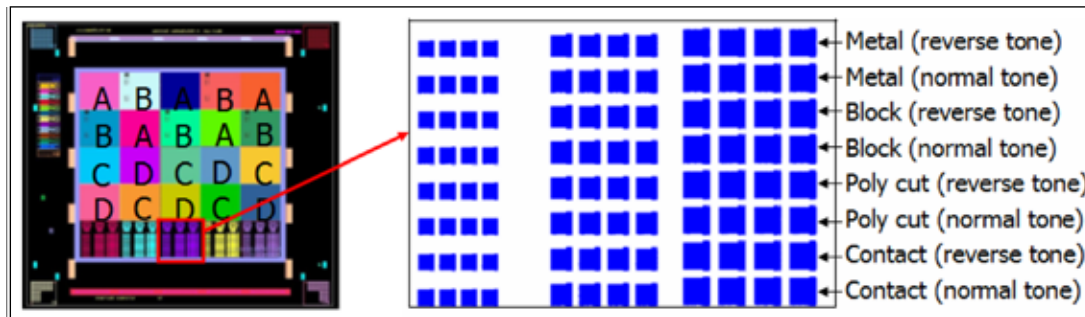


Figure 3. Nightmare programmed defect test chips.

new “Nightmare” test reticle has been designed by IBM. The test reticle contains various sizes and shapes of sub-resolution features that might appear on reticle generations from today’s 22nm to future 7nm. It also contains programmed defects to assess defect detection capability of current and future generation inspection systems.

This paper will discuss the design of the “Nightmare” test reticle, and the inspection results of the current generation reticle inspection methods with emphasis on both inspectability and defect sensitivity. The subresolution features will be ranked according to importance for advanced OPC design. The reticle will also be evaluated using wafer print simulation so lithographic impact of features and defects can be measured and compared against inspection approaches and results.

2. Introduction

As the mask industry progresses toward smaller and smaller technology nodes, the necessity for and complexity of OPC becomes more aggressive — and more critical. It has been a common practice in the world of mask inspection, to take steps necessary to make the mask ‘inspectable’ — sometimes at that expense of defect sensitivity and sometimes at the expense of robust lithographic solutions, in that OPC solutions are often modified on 14nm, 10nm and 7nm designs to accommodate inspection capability rather than lithographic needs. The relationship between MRC rules and inspection sensitivity is an

important one. The sensitivity we are driving to is in a regime where the MRC is restricting OPC solution flexibility.

With conventional reticle-plane inspection approaches, there are two primary ways to improve mask inspectability — first, by reducing the overall sensitivity of the inspection, or second, by targeting specific types of OPC structures for relaxing sensitivity requirements (“de-sense”), such as assist features, notches and nubs. The first approach carries with it, a significant risk of missing defects on primary features that may print as fails on wafer. The second, ‘rules based’ de-sense approach reduces the risk of missing defects on primary images, however, it intentionally ‘tolerates’ imperfections on RET features due to CD non-linearity compared to primary images — specifically line-end shortening, greater than normal corner rounding, or line-edge roughness. Unfortunately, de-sensing these RET features may also result in missing defects that may result in these features printing on wafer. This is especially true for SRAF features.

There are several reasons that sub-resolution assist features (SRAFS) are more important in the advanced technology nodes, but at the most basic, it’s because of two things. (1) the MEEF induced on main features due to adjacent assists is higher than it’s ever been as we push lithographic solutions to their limits, and (2) assist feature regimes are closer to the edge of printing than they have ever been to maximize process windows.² Early generation assist feature placement had very little impact on

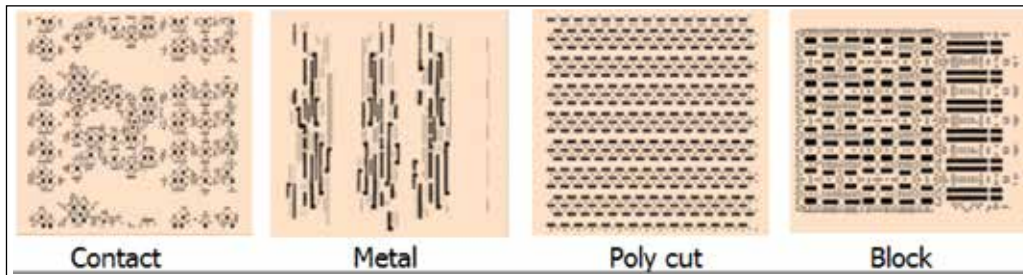


Figure 4. Nightmare base pattern types.

Diffuse Images – Shifted	Long SRAF	Large Primary CD – 1 Side
Diffuse Images – Undersized	Short SRAF	Clear Extension on Main Image Edge
Diffuse Images – Oversized	Opaque Extension in Serif	Opaque Extension on Main Image Edge
Undersized SRAF	Clear Extension in Serif	Clear Extension on Main – End to End
Oversized SRAF	Opaque Intrusion in Serif	Opaque Extension on Main – End to End
Clear Extension on SRAF-SRAF	Clear Intrusion in Serif	Clear Corner Extension
Clear Extension on SRAF-Main Image	Small Primary CD – 2 Sides	Opaque Corner Extension
Opaque Extension on SRAF-SRAF	Large Primary CD – 2 Sides	Pinholes
Opaque Extension on SRAF-Main Image	Small Primary CD – 1 Side	Pindots

Figure 5. Nightmare programmed defect types.

the printing at best focus. They were primarily there to boost the DOF, and try to make sure that all features had similar DOF (thus the reason we so rarely see any measurable impact at AIMS™ of missing assists at best focus). The more we move to complex, off-axis illumination, the more higher orders of light from the assist features help to influence the aerial image of the main feature, which creates the on-wafer image. As they participate more in the formation of the primary image, the effective MEEF has actually grown from less than 1 to greater than 4 in some cases.

Originally, SRAFS were *rules-based*. Only a single size SRAF was allowed per RET solution, so the “worst case” was used to assess the maximum SRAF size which contained significant guard-banding to ensure that they wouldn’t print. With the current *model-based* SRAF approach, the size and placement of the SRAF is optimized in every individual scenario, so the SRAFS are right at the edge of printing in all cases. For these various reasons, the risk of de-sensing SRAFs during inspection is larger. If SRAFS are bigger than expected, they are more likely to print (and affect the main feature), if they are smaller than expected, the main feature will print small.

Aggressive OPC is a double-edged sword. Where it results in improved wafer CD printability, the size and complexity of OPC features often fall at the margin of what leading edge processes can produce. Anomalies such as corner rounding and thin-line end shortening also make it extremely difficult for the reticle-plane inspection systems to exactly model the inspection database to the mask. Therefore, process errors and modeling errors on SRAF must be de-sensed. In addition, SRAFS on today’s advanced technology nodes are variable in size versus the single size features popular with rules-based OPC. Rather than rectilinear in shape, they now consist of curvilinear features, small gaps, pinched lines and assist dots – all challenges to mask processes and reticle-plane inspection modeling. Reticle-plane inspection simply compares the

inspection database to the mask, with no regard to how image quality and defects affect wafer printability. An alternative is an inspection approach that takes wafer printability into consideration.

The focus of this paper will be twofold. First, we will determine the exact capability of current reticle - plane inspection relative to the inspectability of 14nm ground rule mask images with moderate to aggressive OPC, and compare that to litho plane inspection approaches that take into account the impact of sub-resolution features and defect printability. Second, we will explore the pros and cons of each approach. A specially designed test mask, affectionately named “Nightmare,” was produced to assist in those efforts. A description of this mask will be provided in the following pages. Data depicting inspectability and defect sensitivity for each will also be provided, as well as a correlation of defect sensitivity to AIMS™ and wafer print simulation assessments.

3. Goals of this Study and Expected Outcome

There are several goals associated with this study. Some of them have been achieved and the results are presented here. Others will require significantly more time and effort and will be completed in the months to come. They are as follows:

- Characterize base reticle plane inspection capability. Specifically, determine if reticle-plane inspection has enough capability to detect critical defects without imposing overly onerous restrictions on OPC.
- Determine the benefits of litho plane inspection versus reticle-plane inspection.
- Evaluate multiple inspection approaches not on only one or two kinds of challenging features, but over a variety of very carefully chosen structures.
- Understand mask inspection rules and constraints

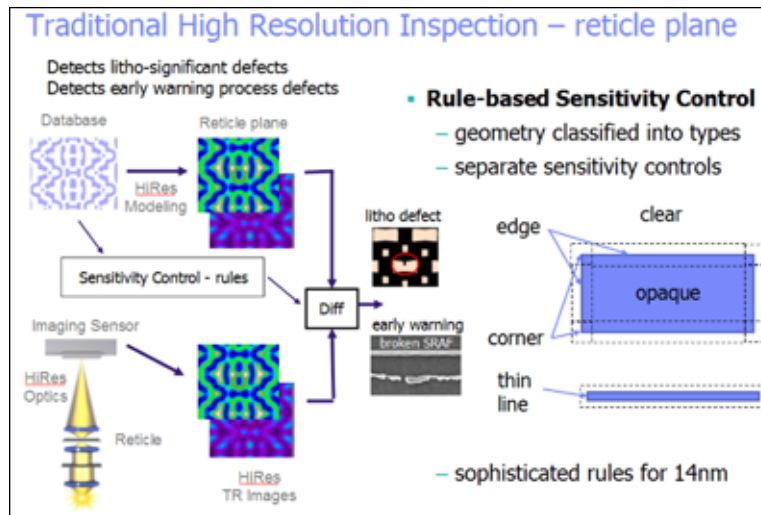


Figure 6. Reticle-plane inspection with rules-based sensitivity control.

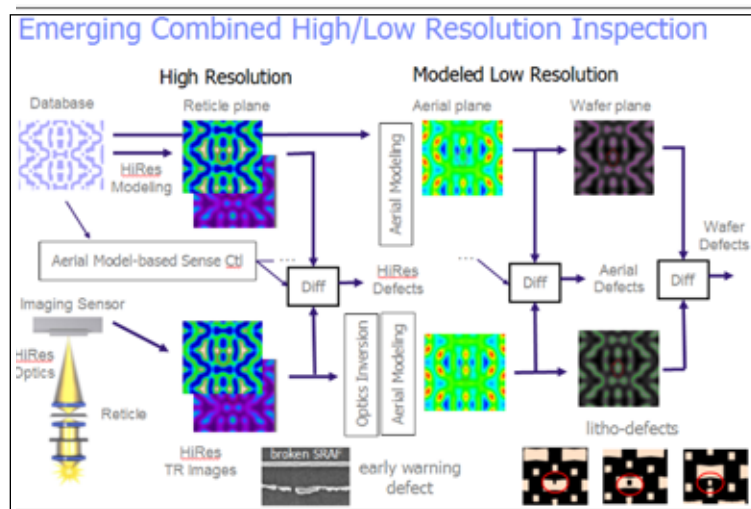


Figure 7. High/low Resolution Inspection.

‘practically’ rather than ‘theoretically’ to determine if current restrictions are real, or if they are overly restrictive based on conservative inspection tool specs.

- Define areas for mask process improvements.
- Ultimately... relax MRC constraints on leading edge technologies.

Expected Outcomes:

- Determine current reticle plane inspection capability for 14nm node and beyond.
- Determine the advantages with litho-plane inspection — inspectability and defect sensitivity — specifically on small defects on features like SRAFs which should be able to be ignored as they are expected to have a lithographic impact so small that defect repair is not required.
- Significantly improved inspectability on the inverse lithography OPC resulting in curvilinear subresolution features and assist dots.

4. Nightmare – OPC Test Mask Description

More than ever, inspection recipe optimization is critically dependent on the design and quality of programmed defect test masks. “Nightmare” is an OPC test mask specially designed to assess the capability of current and future inspection approaches, optimization of inspection recipes, and to identify areas for improvement. The mask contains a large variety of design constructs over a very wide range of dimensions, covering technology nodes from 22nm to 7nm with primary focus on the 14nm node. Four base pattern types are represented on this mask: (A) Contact, (B) Poly Cut, (C) Metal and (D) Block. Figure 1 depicts the layout of the test reticle.

Each of the base pattern macros contains an array of eighteen rows and eighteen columns. Each column in the macro represents a different MRC rule. Some of the rules are relative to minimum line/space dimensions and corner-to-corner spacing, while others apply specifically to OPC features such as SRAFS, notches and nubs. Each column is designed such that the MRC rule increases in aggressiveness as one moves from

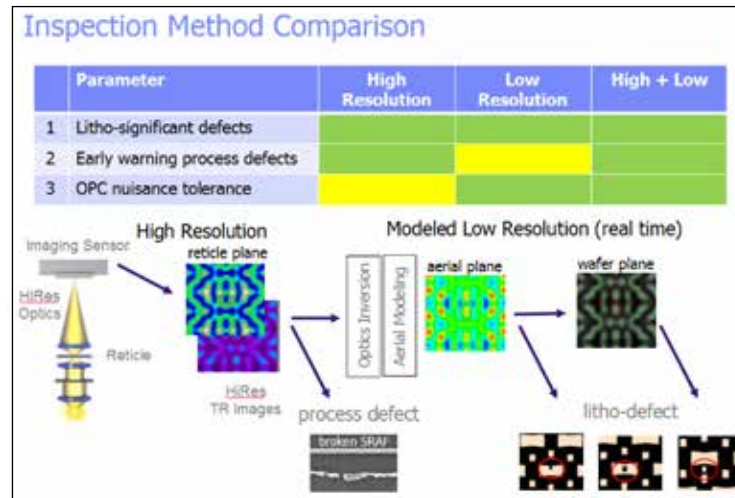


Figure 8. Inspection comparison.

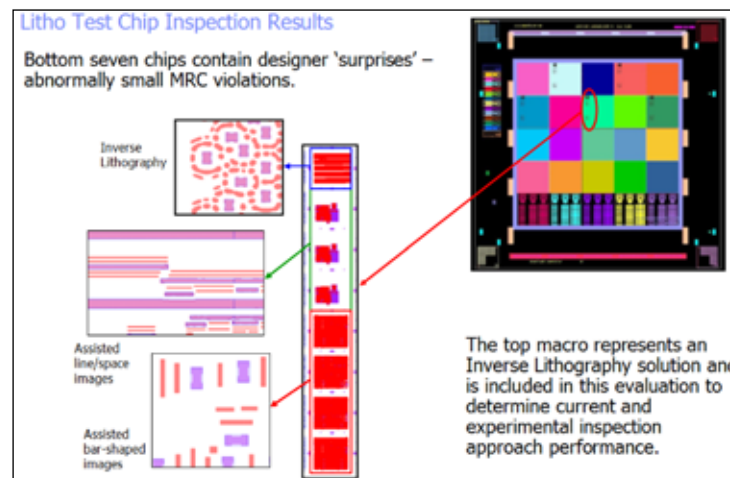


Figure 9. Nightmare 14 nm product macro.

the bottom to the top of the column. The rules at the bottom of the column represent current constraints imposed by reticle plane inspection and are expected to be highly inspectable. Violations against current MRC rules are increasingly challenging as one moves up the column – eventually becoming uninspectable due to current reticle plane capability, or due to mask process resolution limitations. Figure 2 depicts an example of the various MRC rule types across the 18 columns of a contact layer pattern. Similar macros exist on the mask for all four base pattern types. The goal of these macros is to determine where on the spectrum of OPC aggressiveness reticle-plane inspection ‘breaks’ compared to where it breaks for litho-plane inspection.

In addition to the inspectability macros, the Nightmare reticle contains several programmed defect chips. Each of the four base pattern types is represented by a separate PDM macro. The background pattern for each PDM represents the most aggressive of the design patterns that is inspectable, both within the confines of mask process resolution, and reticle-plane inspection capabilities. Each pattern was produced in both normal and reverse-tones and in three magnifications.

The largest version of the PDM represents typical 14nm node dimensions. The data presented in this paper will reflect results for one normal-tone line/space layer macro at the 100% magnification level (14nm generation). Also, 80% and 60% scales are available for future evaluations. Figure 3 depicts the location and layout of the programmed defect macros. Figure 4 depicts the base patterns for the PDM’s, and Figure 5 depicts the list of programmed defect types on the PDM’s.

5. Mask Inspection Approaches – Reticle-plane vs Litho-plane

Reticle-plane Inspection

The standard approach to mask inspection, largely employed by the industry, is reticle-plane inspection. Figure 6 is a graphical representation of how reticle-plane inspection works. In this approach, transmitted and/or reflected light is used to inspect the mask. During the inspection, high resolution transmitted and reflected images are collected by the imaging sensor on the inspection tool. They are compared to transmitted and reflected ‘reference’ images that were modeled from the mask database. The modeled images are further altered to match

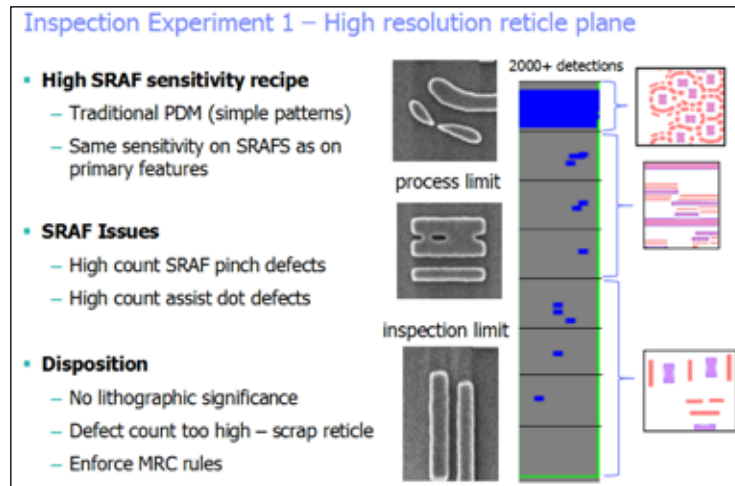


Figure 10. High resolution reticle-plane inspection with high sensitivity on SRAFS.

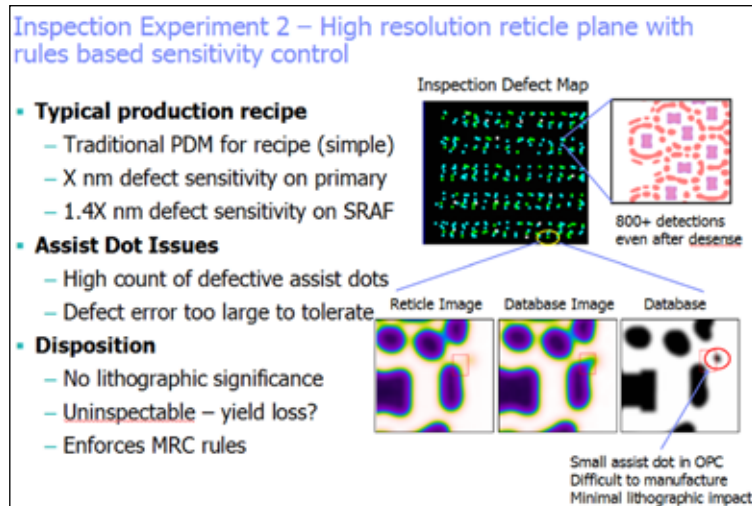


Figure 11. High resolution reticle-plane inspection with OPC de-sense on SRAFS.

the properties of optically captured mask images.³ A number of sensitivity detectors are used to detect defects based on the defect size, defect type, and placement of the defect. Examples of these are detectors specifically designed to detect isolated defects, edge defects, and critical dimension defects (size, placement), as well as detectors whose sole purpose is to detector intensity differences on hole layers.

Since reticle-plane inspection does not take into account the printability of detected defects at the wafer level, combinations of detector settings must be chosen to detect a specific linear defect size for each defect type, and all defects are treated as fails. Each fail must then either be repaired, or analyzed using AIMS™ aerial image analysis to determine printability and whether or not repair is necessary.⁴

Complex OPC adds a layer of complexity for reticle-plane inspection. The majority of SRAFS are not intended to print on wafer; however, the quantity, size, and complexity of such optical proximity features (OPC) must be inspected along with critical primary images. These OPC features are oftentimes significantly smaller than the primary dimensions on the reticle,

and many are small enough to fall on the margin of mask manufacturing process capability. Inspecting these secondary OPC features at the same high sensitivity level as the primary images often leads to thousands of “nuisance” detections and the inability to inspect the mask. To resolve this issue, reticle-plane inspection provides a series of *rules-based* sensitivity control (de-sense) options — specifically those designed to tolerate sub-resolution assist features (SRAFS), notches and nubs. With these de-sense options, the level of defect sensitivity is reduced on such features, allowing reticle-plane inspection to tolerate less than perfect features. There are two risks with this approach: first is the possibility of reducing the sensitivity below the wafer printability threshold, thereby increasing the chance of missing printable defects, and, second, and more importantly, since the desense is rules based, all features on the mask that fall within the same rule as that set for the SRAFS will also receive a level of de-sense.

Most geometries that prove problematic for reticle-plane inspection, fall at, or slightly below, the wafer printability threshold. The inspection tool will detect many of these fea-

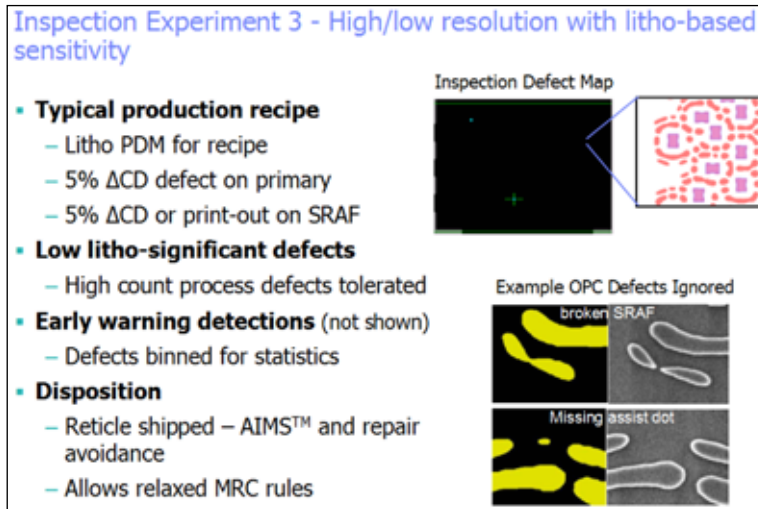


Figure 12. Litho-plane inspection on inverse lithography design.

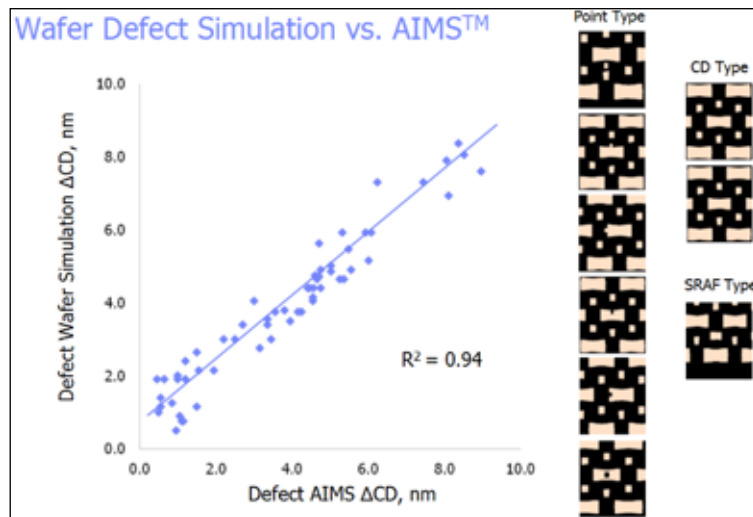


Figure 13. Defect wafer simulation vs. AIMS™ correlation.

tures as defects. Because of this, an elaborate set of Mask Rules Checking (MRC) rules are enforced to assure designs do not contain features that would lead to mask inspectability problems. These MRC rules very often restrict how aggressive a given OPC solution can be. There are rules governing the size of lines and spaces, corner-to-corner spacing, assist feature size, notch and nub depth/width, line-end to line-end spacing, space between SRAFS and so on. Needless to say, they add a measure of complexity to an already complex process. Through countless iterations of MRC test masks and day-to-day experience with emerging technologies, and through several positive changes introduced by inspection tool suppliers, the MRC rules have significantly changed over time, however, they remain a restrictive factor in the development of advanced designs.

High/Low Resolution Inspection

High/low resolution inspection is comprised of three inspection methods: 1) advanced reticle-plane, 2) aerial-plane and 3) wafer-plane.

Advanced reticle-plane inspection is similar to standard reticle-plane in that it also uses transmitted and/or reflected light to inspect the mask, and compares the resulting high resolution images to ‘reference’ images. The defect sensitivity detectors are also similar to standard reticle-plane inspection. The biggest difference between standard and advanced reticle-plane inspection is that the de-sense options used to tolerate OPC features that fall on the fringes of tool capability are aerial *model-based* rather than *rules-based*. With a model-based approach only those features that are non-wafer printable are de-sensed while the remaining features receive full reticle-plane inspection sensitivity. De-sense is no longer applied by feature size, but rather by lithographic significance.⁸

Aerial-plane inspection and wafer-plane inspection (generally “litho-plane”) are designed to detect defects of significance from the litho-plane viewpoint. When inspecting in the aerial-plane/wafer-plane mode, the need to directly de-sense OPC features with rules is eliminated. Figure 7 depicts the process by which wafer-plane inspection moves the comparison be-

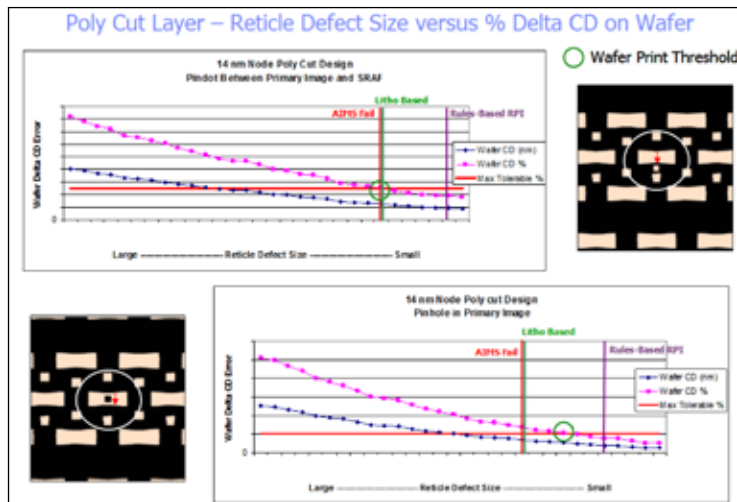


Figure 14. Isolated defects – Pindots and Pinholes.

tween the mask image and the reference image to the wafer level.

As the name implies, wafer-plane inspection moves the comparison plane to the wafer level. This is accomplished in three basic steps as illustrated in Figure 7. The first step is to collect the high resolution images of the mask and reconstruct a physical model of the mask pattern as seen by the inspection tool (Optics Inversion). Any pattern defects that may be present are also reconstructed into the physical model. The inspection wavelength is inconsequential at this point since the mask pattern recovery process depends on high resolution images, not specific wavelength of capture. This is the mask pattern recovery step.⁷ The second step uses a lithographic simulation based on Hopkins' equation to generate an aerial image of the recovered mask (Aerial Modeling). The final step applies a resist threshold to the aerial image to simulate the wafer plane which then separates printable from non-printable defects.³

Figure 8 provides a comparison between high resolution reticle-plane inspection, low resolution litho-based inspection, and a combined high/low resolution inspection method. With high-resolution reticle-plane inspection one can expect good detection of both litho-significant defects and early warning defects due to its high resolution and low noise characteristics. However, its tolerance for aggressive OPC is marginal often requiring complex de-sense rules. With low resolution inspection, the litho-significant defects are also detected, however, the early warning process defects are not detected because they are “not printable”. Even so, OPC tolerance is better. Combining these two approaches provides detection of both classes of defects while providing good OPC nuisance tolerance.

Notwithstanding, litho-plane inspection requires significant communication and coordination within the mask inspection operation to provide the necessary mask material properties, scanner illumination, and resist information needed for the simulation.^{5,6} While the wafer-plane simulation can report defects as delta CD error or edge-placement-error (EPE), the simulation is optimized for speed and is therefore not accurate enough for final defect disposition — AIMS™ measurements

are still needed, although the number of defects is likely greatly reduced vs. reticle-plane inspection of aggressive OPC.

6. Reticle-plane versus Litho-plane Inspection Results

14nm Product Macro – Inspection Experiments

The 14nm product macro on the Nightmare test mask contains three base designs. The first four rows of the macro (from the bottom) contain contact-like shapes with both assist bars and assist dots. Rows five through seven contain line/space shapes with varying sizes of assist bars. Finally, the top row of the macro contains a relatively unconstrained inverse lithography solution and is included in this study to determine current and experimental inspection approach performance on curvilinear shapes. Scattered about in the first seven rows, are intentional shapes which violate the current MRC rules. Figure 9 depicts a representation of these sub-macros.

Three inspection approaches were tested on these product macros: (1) high resolution reticle-plane inspection with high sensitivity on SRAFS, (2) high resolution reticle-plane inspection with sensitivity control applied to SRAFS and finally, (3) litho-based inspection. Figure 10 depicts the results of the high resolution reticle-plane inspection with high sensitivity on SRAFS. The inspection recipe used for this inspection was developed from a traditional programmed defect test mask with simple patterns, relatively little OPC, and no lithographic information about the defects; therefore, the recipe could not be properly optimized. To protect possible SRAF print-out, the inspection recipe used the same sensitivity on the

SRAFS as on the primary images, even though this recipe could not be verified with the simple PDM. With this recipe, the assisted line/space and bar-shaped feature inspection was exceptional with the detection only of process limit defects. However, on the inverse lithography design, there were very high levels of real assist dot and SRAF ‘pinch’ detections due to limitations of the mask making process on such small features. In this case, the reticle would be declared “uninspectable” due to MRC violations. Even so, an AIMS™ analysis of the defects

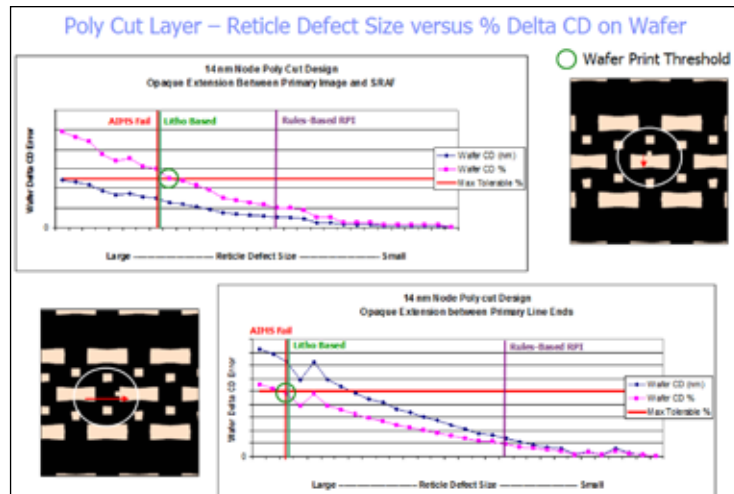


Figure 15. Opaque Extensions.

would show they have no lithographic significance, but the simple PDM doesn't allow better recipe optimization.

Figure 11, depicts the results of the high resolution reticle-plane inspection with typical sensitivity control applied to the SRAFs. The same inspection recipe was used as the previous inspection test for primary features with de-sense applied to the SRAFs. Multiple attempts were made at selecting an appropriate amount of de-sense to ignore the non-lithographically significant OPC assist dot defects and pinched SRAF defects. However, even at significant OPC de-sense, the inspection still resulted in hundreds of detections. It was concluded that high resolution reticle-plane inspection in its current state was not able to tolerate the process limited defects with reasonable de-sense.

The general net of this inspection result is that for typical 14nm node line/space and contact designs that adhere to current MRC rules reticle-plane inspection is adequate for mask inspectability. Later in this paper, is a discussion relative to defect sensitivity and whether reticle-plane inspection is detecting enough... or too many defects.

The final inspection experiment was with litho-plane inspection. This analysis was accomplished in two steps: first, an arbitrary 5% delta CD target was chosen for wafer printability determination and the litho-plane inspection recipe was optimized using the lithographically significant Nightmare programmed defect test mask to assure the detection of defects that would fail that 5% delta CD target on wafer. Next, the inverse lithography macro with curvilinear assist was inspected at those optimized settings. The end result as seen in Figure 12, was a total of two defects detected in litho-plane mode compared to greater than two thousand "nuisance" detections in current reticle-plane inspection mode. As discussed earlier, and as can be seen in Figure 10, the two thousand defects during reticle-plane inspection were small, missing, unresolved, or under-resolved assist dots and other MRC errors – all of which did not print on wafer. Using the high/low resolution inspection method allows these process defects to be detected in the reticle plane and binned together for early warning use, while the litho-significant defects are binned separately in the aerial

plane or wafer plane for appropriate disposition.

Correlation between Wafer Printability Simulation and AIMSTM on the Programmed Defect Macros; Defect Capture for Reticle-plane and Litho-plane recipes

Description of analysis approaches used in this study:

AIMSTM – The Aerial Image Measurement Systems (AIMSTM) generates an aerial image of the mask using the correct scanner exposure wavelength, numerical aperture and illumination design, with corrections for high-NA vector effects in the image formation. The aerial image is captured as a bit-map and can be analyzed for image size, peak intensity, contrast, and so on. With an appropriate threshold, AIMSTM measurements can be used to estimate the printability of mask defects, generating pass/fail data for each defect.

Wafer Print Simulations – Wafer simulation was performed using a commercial optical proximity correction (OPC) simulation tool. The simulation uses a layout file containing the designed mask data (including programmed defects). The engine simulates both scanner optical and resist imaging to predict the final on-wafer resist image. The scanner optical model utilizes exposure information including numerical aperture, illumination design, exposure wavelength, polarization, wafer film stack optical parameters, etc. The resist model is an empirical model to capture photoresist induced effects. The resist model is calibrated using measurement data collected from wafer under the same exposure conditions. A reference design (without programmed defects) was used for comparison between the target critical dimension (CD) and the CD of the defect impacted structure.

Correlation data will be presented here for selected defect types on the Poly-cut programmed defect test macro, as well as a short description of analysis approaches on two specific Contact layer defects. First, the poly-cut defect data.

Poly-cut Macro PDM Results:

Each defect type on the programmed defect test macro is represented in a range of thirty defect sizes. Each defect was simulated at best focus through wafer print analysis simulation. Due to the time needed to make an individual AIMSTM measure-

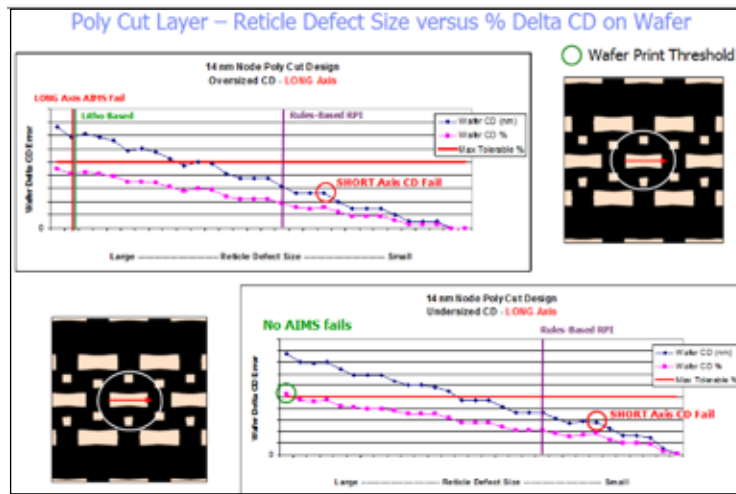


Figure 16. Critical Dimension Defects.

ment of a defect, only selected defect types and a few defects near the 5% delta CD criteria were measured. The defects to measure were determined largely from the wafer print analysis simulation. Major and minor axis measurements were made on the primary feature affected by the defect. Figure 13 shows a correlation of the wafer simulation to AIMS™ for the three types of defects shown (point, CD, SRAF). While simulation of the point defect type is challenging, the overall correlation is reasonable. Therefore, the simulation results can be used reasonably confidently.

The poly-cut macro 14nm positive-tone PDM was inspected in both reticle-plane mode and litho-plane mode. The recipes used were from the previous Experiment 1 and Experiment 3 (see Fig 10 and 12, respectively). Since the Nightmare PDM has lithographically correct defects with both wafer print simulation and AIMS™ measurements, the litho-plane recipe was optimized to find all of the defects that fail a 5% delta CD criterion (based on AIMS™ or wafer print). Because the litho-plane recipe was optimized to match AIMS™, the results seen in Figure 14, 15 and 16 show the litho-plane detection points to be about equal to the AIMS™ fail point. It is important to note that while for this test, the optimized settings match the AIMS™ fail point, the sensitivity of litho-plane inspection in general is largely dependent on that recipe optimization and any changes to that recipe may degrade the sensitivity of the recipe.

The following three charts show the detection point of each inspection method for the recipes used, as well as, the defect SEM size, wafer simulation size, and AIMS™ size. Figure 14 is for two isolated defect types; a pin-dot between a primary feature and an assist feature, and a pinhole inside a primary feature. The defect size determined to print on wafer per AIMS™ analysis is represented by the line labeled “AIMS Fail”. All defects to the left of the “Litho-Plane” line were detected by litho-plane inspection with the recipe used, and all defects to the left of the “Reticle-plane” line were detected by reticle-plane inspection with the recipe used.

Again, there is good correlation between the defect that

fails at AIMS™ and the detectability of printing defects during litho-plane inspection since a litho-correct PDM was used for recipe optimization. Whereas, for reticle-plane inspection, the recipe was optimized using a traditional method consisting of a non lithocorrect PDM and using a single defect SEM size loosely based on wafer print. In this case, this traditional reticle-plane inspection recipe tends to over detect vs. wafer print for these defects, potentially leading to excessive repair and potential yield loss.

For the pinhole defect in the primary feature, the correlation between AIMS™ and wafer printability simulation is not exact. This can be explained by the use of a calibrated resist model in the wafer printability simulation which captures resist specific effects, where AIMS™ relies primarily on the aerial image. Once again, it can be seen that the traditional reticle-plane inspection recipe is providing more sensitivity and finding more non-printing defects than may be necessary from a printable defect viewpoint.

Figure 15 depicts the results for two opaque edge defect types; an opaque extension between a primary line and an assist feature, and an opaque extension between two primary line ends. As can be seen in both graphs, there is a strong correlation between the printable defect size as determined by AIMS™, and as determined by wafer print simulation. As expected, the traditional reticle-plane inspection recipe provided the highest level of defect sensitivity – significantly higher than litho-plane inspection recipe, and perhaps too high relative to printable defects.

Figure 16 depicts the results for two critical dimension defects. The upper chart contains inspection and printability results for an oversized primary image. For this analysis, the wafer print simulation determined the affect on the major axis (x axis as depicted in the picture above) was minimal with the largest programmed defect not crossing the wafer print threshold. AIMS™ on the other hand, indicates the two largest defects as potentially printing on wafer. Again, this disagreement could be explained with the difference in approaches between the aerial imaging on AIMS™ and the resist model

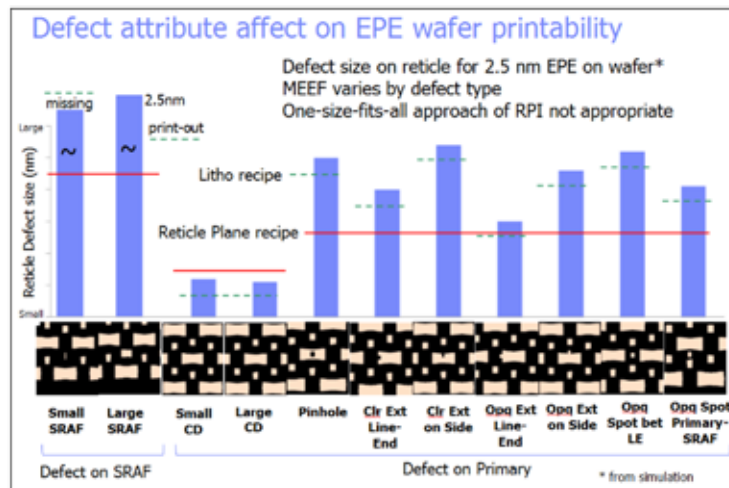


Figure 17. Defect type, size, shape, placement dependencies.

approach of the wafer printability simulation. For this defect type, the traditional reticle-plane inspection recipe detected far more defects than necessary.

For the undersized critical dimension defect, the largest defect was deemed printable by wafer print simulation however it did not fail AIMS™ measurements and was not detected by the litho-plane inspection recipe. Once again, the traditional reticle-plane inspection recipe detected a significant number of smaller defects.

Worthy of note in Figure 16 is the difference between the arbitrary 5% CD fail on the longer image axis compared to the shorter image axis. One of the reasons it takes a relatively large defect to cause an arbitrary 5% CD fail on wafer for this image is the overall size of the image itself. In this particular test case, the programmed defect is on the longer axis. If the defect had been on the shorter axis, the point of failure would be as noted within the red circle on Figure 15 rather than on the largest defects seen on the left side of the chart. The traditional reticle-plane inspection recipe for this test was not chosen based on a 5% delta CD fail on wafer, but rather it was chosen based on a single linear defect specification. As can be seen in this example, the 'one-size-fits-all' approach of traditional reticle-plane inspection recipes is inappropriate. This is further reinforced by the data represented in Figure 17. In this figure, it can be seen that the reticle size of the reticle defect that results in a 5% delta CD error on wafer (2.5nm EPE for 50nm feature size) varies depending on the type of defect, the size of the defect, the size of the feature the defect resides on, and the placement of that defect on that feature.

As show, the traditional reticle-plane inspection recipe optimized from a non-litho-correct PDM, often applies a single sensitivity irrespective of the defect type or location; this can result in over-detection of some defect types and under-detection of other types. Whereas, if a litho-correct PDM with a variety of defects (including high-MEEF defects) is used, then the inspection recipe can be better optimized to reduce over-detection and eliminate risky under-detection.

Percent CD Error versus Edge Placement Error:

There are two common metrics for CD error determination:

Percent tolerance and edge placement error (EPE). With percent CD tolerance the defect threshold is described as a percentage of the target feature. Edge placement error defines the absolute variation that any edge of the printed image can deviate from nominal.

EPE-based tolerances are more sensitive to asymmetric defects which cause overall shifting of the printed feature because each edge in the EPE approach is constrained, whereas, the CD method just specifies the difference. Figure 18 shows an example of how a fixed EPE is tougher on larger features (as a percentage of feature size) than on smaller features. Figure 19 depicts how printing defects are highlighted sooner – on smaller defect sizes with the fixed edge placement error approach rather than the percent CD tolerance approach.

In Figure 19, two defect types are evaluated – an opaque extension between two primary features, and an opaque extension between a primary feature and an assist feature. In the case of the opaque extension between two primary features, it can be seen that the contact on which the defect sits, elongates considerably, however due to the proximity of the defect to the adjacent primary feature, an impact can also be seen on that feature as well. Relative to the opaque extension between a primary image and assist feature, the defect also has an elongation effect on the primary image. In both cases, there is a noticeable shift in the center line of the printed feature. Shifts in placement of the contact can impact yield as a result of overlay offsets between the metal layers above and below. It is also noted that even if a defect fails an edge placement error tolerance, it may still fall within the acceptable tolerance for percent CD error (circled in red in the figure below). The appropriate tolerance metric is dependant on the specific process requirements of a layer and its failure mechanism.

7. Summary and Conclusions

Reticle-plane inspection using traditional non-litho-correct PDMs for recipe optimization and a single number reticle defect size criterion may be detecting some defects well below the wafer printability threshold and may be missing other litho-significant defect types (e.g. high-MEEF). Figures 14 through 17 demonstrate in some cases, a wide difference between the

Measurement	Tolerance	1X Feature Size	"In-Spec" CD
% CD	+/- 5%	50 nm	47.5 – 52.5 nm
% CD	+/- 5%	100 nm	95 – 105 nm
EPE	+/- 1.25 nm/edge	50 nm	47.5 – 52.5 nm
EPE	+/- 1.25nm/edge	100 nm	97.5 – 102.5 nm

Figure 18. Edge Placement Error versus Percent CD Tolerance.

defects detected by such a traditional reticle-plane inspection recipe as compared to those detected by a properly optimized litho-plane inspection recipe using a litho-correct PDM and litho-based criterion.

Use of a litho-correct programmed defect mask in this evaluation has provided a measure of assurance that there is relatively good correlation between wafer printability simulation and AIMS™ printability, and further, that it is possible to generate a litho-plane recipe that noticeably reduces over-detection which can avoid unnecessary repair and yield loss. Further, the recipe could be optimized differently to add detection margin vs. the printing defects. While not studied, we expect it is possible to improve reticle-plane recipes using such a properly designed litho-correct PDM.

We believe that comprehensive litho-based programmed defect test masks are needed for advanced node reticles. These test masks afford the ability to optimize inspection recipes for litho-significant defects as well as provide an opportunity to use target OPC and high-MEEF defects in the optimization.

We observed the benefits of litho-plane inspection for aggressive OPC with its ability to ignore small defects with no lithographic significance (inverse lithography example); this allows the OPC designers more latitude. With this approach, a high level of inspectability is realized on very small nonlithographically significant OPC shapes (such as curvilinear assist and small assist dots) – even if those images are not resolved perfectly – or at all, through the mask process. This provides extendibility to the mask making process.

Additionally, combining the ability to inspect in reticle-plane and litho-plane nodes concurrently (high/low resolution) provides mask manufacturers the opportunity to monitor process performance through the detection of certain non-printing defects, but only focus repair and yield efforts on wafer-printable defects

Although additional work is required, it is expected that approaches similar to the high/low resolution method will provide greater latitude in OPC with more relaxed MRC rules, thus reducing the boundaries on what can be done to improve lithographic fidelity.

While there are measurable benefits to litho-plane inspection, there are concerns as well. Litho-based inspection requires a significant infrastructure, including the need to provide sufficient lithographic information to the inspection system (such as illumination conditions, source map, stack information, and so on). In addition, the speed optimized models used by mask inspection to detect passing and failing defects may lead to false or nuisance detections, or to insufficient sensitivity to detect real defects. Finally, the methods to determine the proper threshold to use in the wafer-plane can

be challenging leading to the potential for unwanted detections or missed subtle defects.

8. Future Work

While significant progress has been made in the evaluation of current and emerging inspection methods on the specially designed litho test chips and PDM's on the Nightmare reticle, a great deal of work is still ahead of us relative to truly characterizing the limits of both reticle-plane and litho-plane inspection on a wider selection of challenging features and over a variety of chosen structures. Where the specially designed litho test macros used in this paper represent aggressive 14nm node technology, it is clear that more challenging OPC lies ahead, and with it, a greater need to minimize the level of restriction that the mask process and mask inspection capability places on designing more robust OPC. The Nightmare mask contains thousands of test cases that will allow a reasonably thorough assessment of mask process and mask inspection capability and limitations.

All of the work presented in this paper was based on a mask built on the Thin OMOG attenuator.

Additional work is required on other attenuators used for 14nm node mask production.

Further study will also allow the use of the Nightmare reticle for mask process improvement studies as it truly pushes the limits of 14nm technology as well as early 10nm, and potentially 7nm designs.

Finally, the ultimate goal of future work is to apply what has been learned about mask process and inspection to the rules that constrain our ability to design robust OPC, and to determine the best possible approach to aggressive OPC inspection.

9. Acknowledgments

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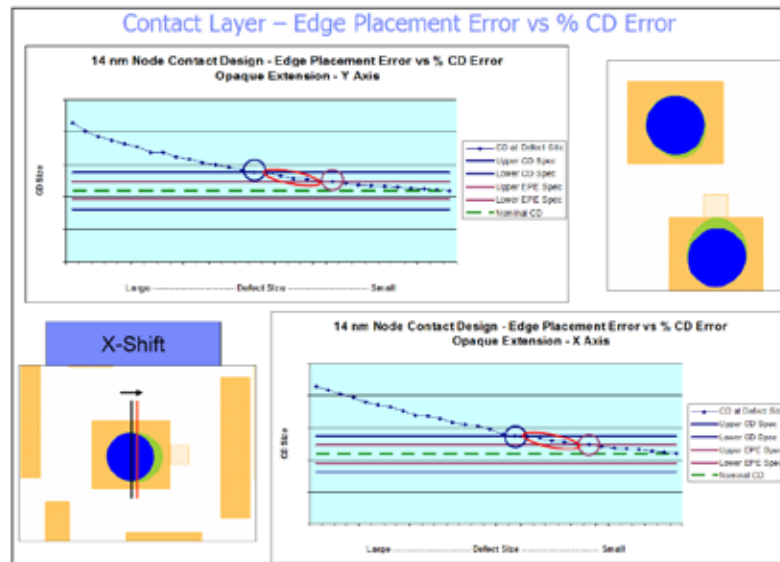


Figure 19. Edge Placement Error versus Percent CD Tolerance.

10. References

- [1] Won-Sun Kim, et al, "Implementation strategy of wafer-plane and aerial plane inspection for advanced mask manufacture" **Proc. SPIE 7379**, (2009).
- [2] Ramya Viswanathan, et al, "Process optimization through model based SRAF printing prediction" **Proc. SPIE 8326** (2012).
- [3] E. Gallagher, et al, "Wafer Plane Inspection Evaluated for Photomask Production" **Proc. SPIE 7122**, (2008).
- [4] AIMS™, a trademark of Carl Zeiss.
- [5] Carl Hess, et al, "High Resolution inspection with wafer plane die:database defect detection" **Proc. SPIE 7122** (2008).
- [6] C. Hess, M. Wihl, R-F. Shi, Y. Xiong, and S. Pang, "A Novel Approach: High Resolution Inspection with Wafer Plane Defect Detection" **Proc. SPIE 7028**, (2008).
- [7] Jin-Hyung Park, et al, "Mask pattern recovery by level set method based on inverse inspection technology (IIT) and its application on defect auto disposition" **Proc. SPIE 7488** (2009).
- [8] Ching-Fang Yu, et al, "Inspection of advanced computational lithography logic reticles using a 193nm inspection system" **Proc. SPIE 7823** (2010).



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Industry Briefs

■ The Impact on OPC and SRAF Caused by EUV Shadowing Effect

By **Fan Jiang**, Mentor Graphics, Wilsonville, OR

EUV's off-axis mask illumination introduces a special problem in EUV OPC—the shadowing effect. While there is debate about when extreme ultraviolet lithography will be ready for production, there continues to be active research and development into making every part of an EUV system work, including optical proximity correction (OPC). That's right, there is no break from the pattern distortions seen in sub-wavelength lithography. In fact, EUV introduces significant new pattern-distorting effects. As EUV has developed over the last few years, the models for these new EUV-specific effects have also developed and improved. Now that pre-production EUV scanners are in foundries and being rigorously tested, tools to correct for EUV-specific optical effects are being fully integrated and tested. There is impact on OPC caused by one of those new distortions, the EUV shadowing effect, and a model-based solution is required for managing it.

■ BACUS Photomask Co-located with SPIE Scanning Microscopy 2014

New in 2014 - SPIE Photomask Technology will be co-located with SPIE Scanning Microscopy 2014, a multidisciplinary conference for advancing scanning microscopy technologies and applications. Two conferences in one location, plus access to multidisciplinary connections and information. It will be held at Monterey Conference Center and Monterey Marriott in Monterey, California, 16 - 18 September 2014.

■ IBM Chip Sale: What Would It Mean?

By **Rick Merritt**, Silicon Valley Bureau Chief, EE Times

When IBM sold its x86 server business to Lenovo in January, the Author predicted that Big Blue might get out of hardware altogether by 2020. Looks like he may have been too conservative — a deal could come as early as this year. IBM has retained Goldman Sachs to explore possible sale of its chip division, the Financial Times reported. The company is not committed to a sale and could seek a partnership for the group. IBM declined to comment on the report, but the long-rumored move is not surprising.

■ Spansion, Post Merger, to Launch Auto SoC Mid-2014

By **Junko Yoshida**

MADISON, Wis. — Spansion, which began last summer its transformation process from a flash memory specialist to a supplier of "embedded systems solutions," reported Tuesday fourth-quarter revenue of \$313.7 million, a 40% increase from the same quarter a year ago, and up 14% sequentially.

Calling the acquisition of Fujitsu Semiconductor's MCU and analog businesses "a nice fit," John Kispert, CEO at Spansion, during a one-on-one interview with EE Times, remained optimistic about integrating two companies with vastly different cultures, geographical markets,

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