

# PHOTOMASK

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2<sup>nd</sup> place Zeiss Best Student Poster — PUV18

## The self-driving photomask Pattern degradation with larger particles on EUV pellicle

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### ABSTRACT

Particle defects placed on extreme-ultraviolet (EUV) pellicle can degrade pattern quality due to the particle defect shadowing. It is obvious that serious patterning error would be occurred due to larger particle defects on top of the pellicle, so that the effect of critical dimension (CD) degradation caused by particle defect on top of the EUV pellicle is investigated. We tried to determine the maximum allowable particle defect size with various pattern types and nodes via commercial simulation tool. Also, we set the boundaries for CD error limit of 5 % and CD non-uniformity to 0.2 nm. Based on these result, we determined the maximum allowable particle defect size for N5 and N7 nodes in order to find the proper defect control.

### 1. Introduction

Extreme ultraviolet (EUV) lithography at 13.5nm wavelength is the most preferred technology to make sub-1x nm patterning<sup>[1]</sup>. However, critical issues related to EUV high volume manufacturing (HVM) still remain. Among them, large particle defect on EUV mask is one of critical issues which can cause serious patterning error even though the EUV pellicle is required to protect the EUV mask from contamination, defects and particles<sup>[2]</sup>.

Although the number of particle defect on EUV pellicle is decreasing, many particle defects still placed on the EUV pellicle. A large particle defect on EUV pellicle can degrade pattern quality due to the particle defect shadowing, so that we investigated effect of particle defect shadowing in EUV lithography<sup>[3-4]</sup>.

As the target critical dimension (CD) becomes smaller, CD uniformity (CDU) is considered to an important factor in terms of patterning. Figure 1 shows the sizes of different patterns for different nodes. The pattern size of 5 nm node was predicted based on the previous report<sup>[5-6]</sup>.

In this study, the patterns from periodic line and space to logic patterns by using optimized illuminations are used, and patterning errors are studied.

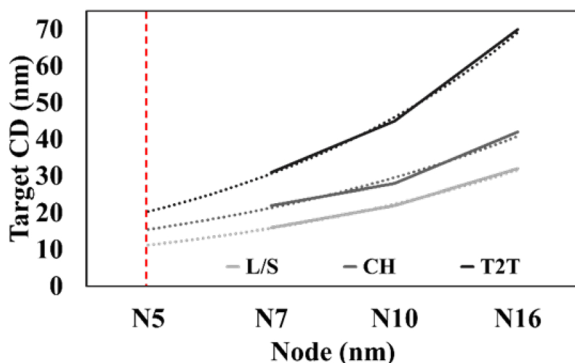


Figure 1. Pattern size for various nodes.

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# EDITORIAL

## Photomask Infrastructure - The Unsung Heroes

### Frank E. Abboud, Intel Mask Operation

It is 7:45 am at Shimbashi station and I am waiting for the Yokohama train. The train arrives, and, as expected, it is standing room only. Luckily, it is an express train so there are only a few stops. However, with every stop, more people get on the train and the squeeze is on! Closed in on all sides by other passengers, I could not help but think of the Game of Thrones scene with Kit Harington in the "Battle of the Bastards"!

After getting off the train, transferring to the subway to Minato Mirai, then taking the long three story high escalator ride, I arrived at the Yokohama Pacifico, the site of Photomask Japan 2019 in April. As usual, there was no shortage of secretarial help handing out the badges, when suddenly my muscle memory kicked into action with the constant, slight bowing every time I see someone I recognize.

As the morning session started, while I was resting in the front row seat from my seventy minute journey, I started questioning ... why am I here again? Wasn't I here not too long ago? Like last year, and the year before .... I then came to realize that I have been going to Photomask Japan since 1993, when the conference was first established. I may have missed one or two years in the past 26 events, but otherwise, I was there.

In the nineties, Japan had the largest number of mask shops in the world. Photomask Japan was an opportunity to interact with customers and suppliers in one location. Every semiconductor company had a mask shop or two: Toshiba, Hitachi, NEC, Sony, Fujitsu, Sharp, Mitsubishi, and Rohm, just to name a few. Also, many of the merchants, like DNP, Toppan, and Hoya, had more than one mask shop location. Although now the number of captive mask shops has diminished to just two (Rohm and the Toshiba Joint venture with DNP), and merchants have consolidated to one mask shop each (DNP, Hoya, and Toppan), the center of gravity for Photomask technology has not shifted away from Japan. In fact, for many mask making steps, the only suppliers are found in Japan.

For mask blanks, Hoya and ShinEtsu have dedicated resources to produce best defect free mask blanks, with continued innovation in stack materials for Phase Shift technologies. EUV blanks are orders of magnitudes more difficult to make and the only viable EUV Mask blanks are manufactured in Japan by AGC and Hoya. For mask making resist, the suppliers are all in Japan: Fuji Film, ShinEtsu, Sumitomo, Tokyo Ohka, Zeon, etc. TEL plays a major role in developing coat, develop, bake and clean equipment. For single beam writers, NuFlare and JEOL are the market leaders, while in the field of multibeam writers, the Austrian start up, IMS, has partnered with JEOL to provide the world's only high volume production tools. For etch, Shibaura and AMAT are both developing EUV tools, and as a customer I am delighted to have a choice. For inspection while Lasertec, KLA, and AMAT are supporting optical masks; only Lasertec provides an EUV actinic blank inspection tool. Many of the world's pellicles are from Japan, Mitsui, MLI (headquarter in Sunnyvale, manufacturing in Taiwan) and ShinEtsu. Yes, I have to mention that, from Europe, Zeiss supplies critical tools for the back end with AIMS (optical and EUV) and e-beam repair, and that they, along with KLA, also lead the industry in the area of XY measurement tools. However, I also must mention that Nano Imprint masks (1x!) were developed and perfected in Japan and that Japan remains the only country with such technology. The sheer amount of materials and tooling for the mask industry that are developed and manufactured in Japan, along with the level of manufacturing perfection and continuous innovation, make Japan a heaven for mask makers!

My impression of Photomask Japan this year was very favorable. At least two-thirds of the papers were new and contained useful information. The attendance may not have been at historical levels, but I think quality takes precedence over quantity. Hitachi's new Atomic Layer Etch (ALE) technique for silicon was very interesting. The talk from IMS on the multibeam writer in mask making was impressive. EUV mask metrology was a vibrant topic. Lasertec showed promising results of Actinic Pattern Inspection (API) using components of their EUV blank inspection tool. Finally, there were a number of papers on computational lithography and Mask Error Corrections (MEC).

One thing new that caught my attention was the number of papers by ASML. The introduction of the High-NA scanner and its impact on mask was very well presented. Furthermore the ~4 papers on mask-to-scanner interactions were quite interesting in terms of mechanical interface, thermal expansion, and impact on lithography. I think this field requires more attention from the mask maker community as we often do not pay enough attention to mask usage in the scanner.

The panel discussion on keeping profitable with older tools was revisited this year. Honestly, this is nothing new. Ages ago people figured out how to squeeze out a few more dollars productivity from depreciated tools. After-market service and parts are essential as few equipment makers will divert resources for older products at the expense of the new equipment.

I am glad that I once again came to Photomask Japan! This conference remains a vital forum for the exchange of ideas of the mask industry and a vital link with the semiconductor industry as a whole.



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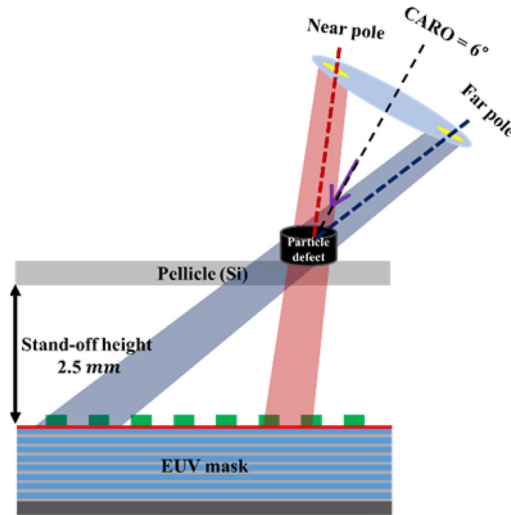
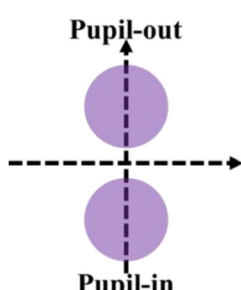

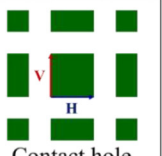




Figure 2. Scheme of particle defect on EUV pellicle

Table 1. Optimized illumination for the type and size of the pattern.

	Pattern type			
	N7	16 nm	22 nm	16 nm L/S 31 nm T2T
	N5(estimated)	11 nm	16 nm	 11 nm L/S 16 nm T2T

## 2. Simulation Condition

Figure 2 shows a schematic diagram of particle defect shadowing on top of the EUV pellicle. The distance between the pellicle and the mask is fixed to 2.5 mm. We assume that a cylindrical particle is placed on a EUV pellicle. A coherent light from the illumination system passes through the particles on the EUV pellicle, the shadows of particles appear on the mask<sup>[7]</sup>.

We used the illuminations optimized for the given types and sizes of the patterns. The simulation conditions are summarized in Table 1<sup>[8]</sup>. Figure 3 shows types of particle defects in the NXE 3350<sup>[9]</sup>. And the optical constants of materials are obtained from the data book of center for X-ray optics (CXRO) and shown in Table 2. Patterning simulation was performed using rigorous simulation tool ('EUVL-suite' of FastLitho).

## 3. Result

### 3.1 Impact on particle defect

16 nm of periodic line and space (L/S) pattern using ASML dipole (sigma in 0.7/sigma out 0.9) is considered. Figure 4

shows patterning error caused by the particle defect materials. CD variation is increased with the larger k. Here, we focused on Cr which is mostly found on EUV pellicle.

Figure 5 shows CD variation with the height of particle defect on EUV pellicle in 16 nm L/S. CD variation is increased with height until the height of particle defect is reached to 100 nm. However, it is not increased any more in the size over 100 nm. Therefore, we chose the height of particle defect on EUV pellicle was 100 nm.

### 3.2 Impact on particle defect with illuminations

16 nm of periodic L/S pattern using dipole (center 0.8/radius 0.1) is considered. Figure 6(a) shows that the patterning error dependency on the position of illumination pole. The patterning error due to defect shadowing by near pole is larger than defect shadowing by far pole. Figure 6(b) shows that CD variation is smaller when we used the ASML dipole (sigma in 0.7/sigma out 0.9) than the conventional dipole (center 0.8/radius 0.1).

### 3.3 Impact on particle defect with 7 nm node patterns

Figure 7 indicates that the maximum allowable pellicle defect

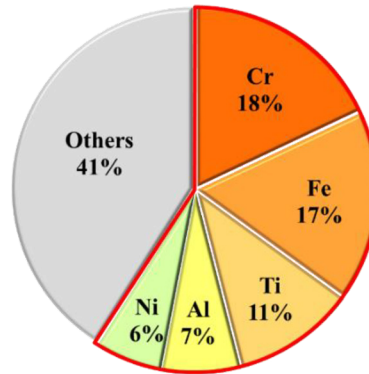


Figure 3. Defect composition of NXE 3350.

Table 2. The refractive index of the particle defect material.

Particle	Cr	Fe	Ti	Al	Ni
n	0.9325	0.9406	0.9519	1.0028	0.9482
k	0.0389	0.0522	0.0481	0.0297	0.0727
Particle	Sn	SiO <sub>2</sub>	TaN	CrN	AlO <sub>3</sub>
n	0.9415	0.979	0.926	0.9179	0.9679
k	0.0726	0.0108	0.0436	0.0392	0.039

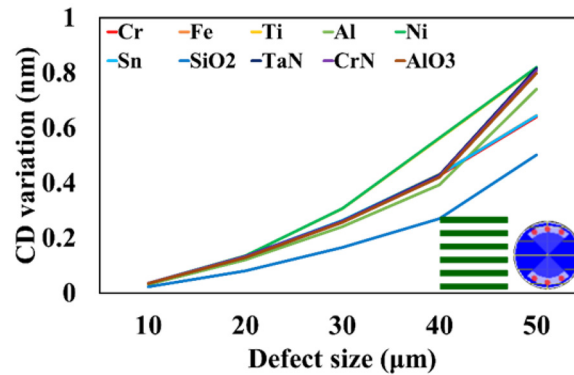


Figure 4. Impact on the particle defect materials which is attached to the surface of the EUV pellicle.

size for different 7 nm node patterns. Patterning error is gradually increased with the size of particle defect. In 16 nm L/S pattern, the size of the defect allowed up to 5 % of the target CD is about 55  $\mu\text{m}$ . In 22 nm contact hole (CH) pattern, the patterning error due to particle is smaller in the horizontal direction than in the vertical direction. Thus, the size of the defect allowed up to 0.2 nm of critical dimension uniformity (CDU) is about 40  $\mu\text{m}$ . Finally, the size of the defect allowed up to 0.2 nm of the CDU is about 30  $\mu\text{m}$  at 16 nm periodic L/S and 31 nm tip-to-tip (T2T) pattern. In the 7 nm node pattern, the CD variation is within 5 %, even if the size of the defect is as large as 30  $\mu\text{m}$ .

### 3.4 Impact on particle defect with 5 nm node patterns

Also, we determined the effect of particle defect on 5 nm node patterns with the optimized illumination conditions. Figure 8 shows that the maximum allowable pellicle defect size for different 5 nm node patterns. Patterning error is gradually increased with the size of particle defect. The size of the defect allowed up to 5 % of the target CD is about 10  $\mu\text{m}$  at the 11 nm L/S. In 16 nm contact hole (CH) pattern, the patterning error due to particle is smaller in the horizontal direction than in the vertical direction. Thus, the size of the defect allowed up to 0.2 nm of critical dimension uniformity (CDU) is about 9  $\mu\text{m}$ . For the N5 node pattern, the size of the defect must be less than 10  $\mu\text{m}$ .

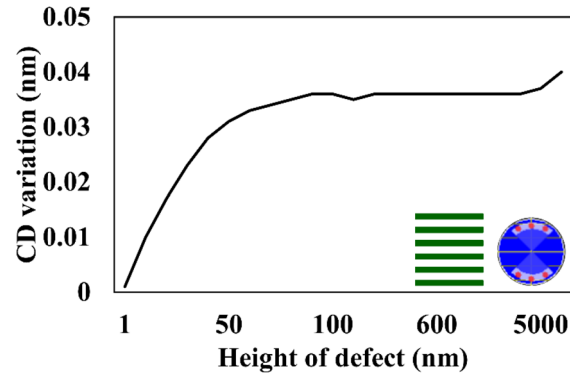


Figure 5. Impact on the height of particle defect on EUV pellicle.

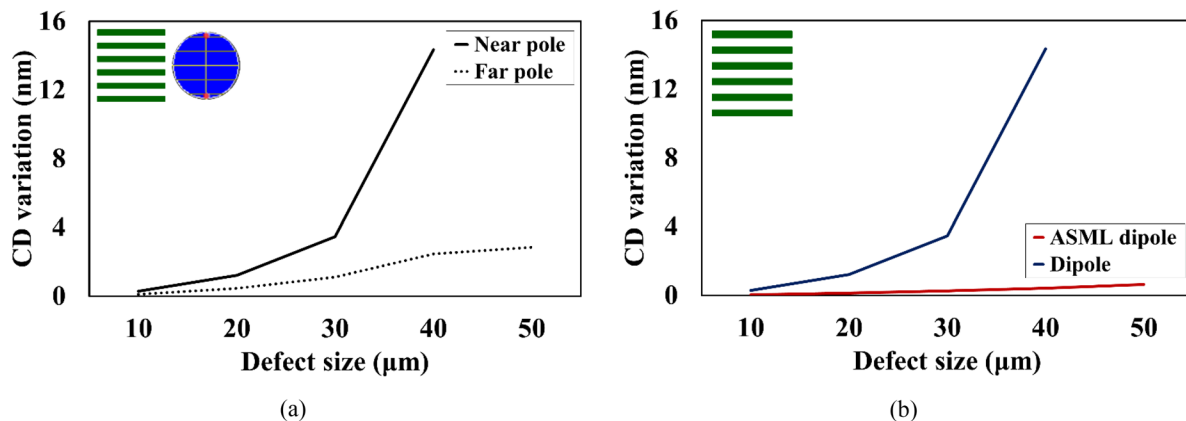


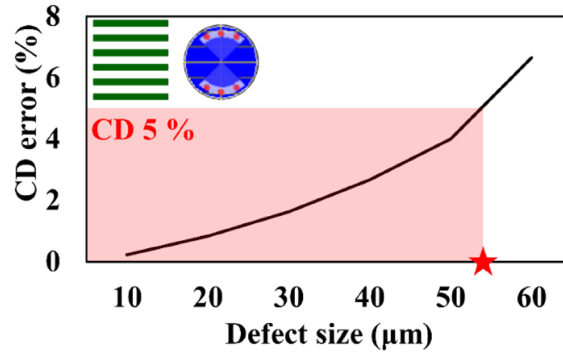
Figure 6. Impact on particle defect with illumination; (a) near vs far pole and (b) different types of illumination.

#### 4. Conclusion

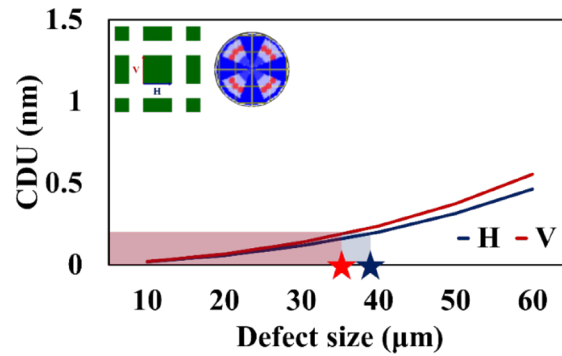
The extreme ultraviolet (EUV) pellicle is required to prevent pattern degradation as well as to protect the EUV mask from contamination, defects and particles. However, particle defects on EUV pellicle might damage the pattern. We investigated the maximum allowable pellicle defect size with various nodes, pattern types, and illumination conditions. In the N7 pattern, the CD variation is within 5 %, even if the size of the defect is 30  $\mu\text{m}$ . For the N5 pattern, the size of the defect must be less than 10  $\mu\text{m}$ .

#### 5. References

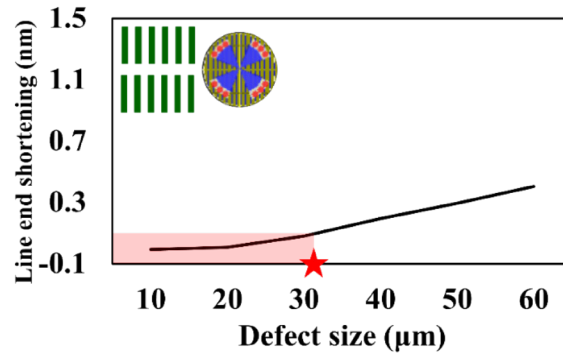
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(a)

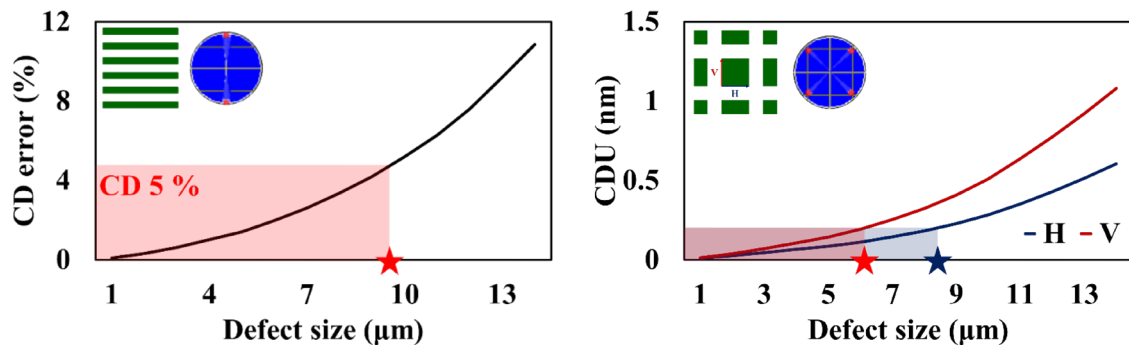


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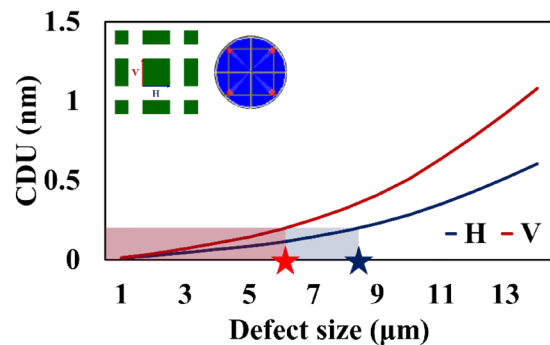


(c)

Figure 7. Pattern degradation caused by the particle defect on (EcU) V pellicle in 7 nm node patterns; (a) 16 nm periodic L/S pattern using ASML dipole ( $\sigma_{\text{in}}$  0.7/ $\sigma_{\text{out}}$  0.9), (b) 22 nm contact hole pattern using ASML quasar ( $\sigma_{\text{in}}$  0.4/ $\sigma_{\text{out}}$  0.9), and (c) 16 nm periodic L/S and 31 nm T2T using ASML quasar ( $\sigma_{\text{in}}$  0.7/ $\sigma_{\text{out}}$  0.9).



(a)



(b)

Figure 8. Pattern degradation caused by the particle defect on EUV pellicle; (a) 11 nm periodic L/S pattern using ASML dipole ( $\sigma_{\text{in}}$  0.9/ $\sigma_{\text{out}}$  1.0) and (b) 16 nm contact hole using ASML quasar ( $\sigma_{\text{in}}$  0.9/ $\sigma_{\text{out}}$  1.0).



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#### ■ Trump Administration Eases Ban on Huawei After Technology Stocks Tumble

Days after blacklisting Chinese technology company Huawei from buying American-made products, the Trump administration is now easing up. The U.S. Commerce Department restored the Shenzhen-based tech giant's ability to maintain its network, which means the company can buy equipment and complete software updates to support those who use Huawei smartphones, according to a [90-day temporary general license](https://www.npr.org/2019/05/20/724910121/after-trump-ban-huawei-phones-will-lose-access-to-google-software) issued by federal officials.

<https://www.npr.org/2019/05/20/724910121/after-trump-ban-huawei-phones-will-lose-access-to-google-software>

#### ■ Chip Roadmap Slows, Diverges

The next-generation transistor may come in Intel, Samsung and TSMC flavors. It's just one sign of how the semiconductor roadmap is fanning out as it approaches a frightening wall a few nodes ahead. Imec researchers laid out what one observer called "a Cambrian explosion" of options to squeeze advances out of silicon. They span new kinds of transistors, materials, architectures and packages.

[https://www.eetimes.com/document.asp?doc\\_id=1334689](https://www.eetimes.com/document.asp?doc_id=1334689)

#### ■ Intel Targets 2021 for 7 nm

After a long delay, Intel will start shipping its first 10-nm processors in June, consistent with the schedule the company has been communicating since last year, executives said. Intel also plans to begin shipping 7-nm processors in 2021, executives told analysts at the company's annual investor day. The 7-nm process technology will mark Intel's first use of extreme ultraviolet (EUV) lithography.

[https://www.eetimes.com/document.asp?doc\\_id=1334677](https://www.eetimes.com/document.asp?doc_id=1334677)

#### ■ Startup Delivers Embedded AI Code

Ali Farhadi is a canary in the coal mine of enterprise AI. His startup, Xnor, is among the pioneers looking for sustainable revenues in neural-networking software for embedded systems. Xnor launches AI2GO, an offering that consists of hundreds of pre-trained models tailored to run deep learning on a variety of Arm, FPGA, GPU, MIPS, and x86 processors. The 50-person startup, formed in 2017, is already running cash-flow-positive on a small set of early products, but the big challenges are still ahead.

[https://www.eetimes.com/document.asp?doc\\_id=1334695](https://www.eetimes.com/document.asp?doc_id=1334695)

#### ■ HP Enterprise Buys Supercomputer Pioneer Cray for \$1.3B

Hewlett Packard Enterprise (HPE) will be purchasing Cray to the tune of \$1.3B. The deal represents a 17 percent premium over Cray's current stock price. Cray, of course, is Cray — one of the leading companies in supercomputing, though its own role in that process has transformed over the years. In the beginning, Cray designed its own, fully custom hardware and software stacks. Today, the company functions as a high-end integrator, working with CPUs from AMD or Intel, but adding its own expertise in interconnect, software, and I/O technology to create the supercomputer stack.

<https://www.extremetech.com/computing/291586-hp-enterprise-buys-cray-for-1-3b>

#### ■ Intel CPU Shortage Expected to Ease in June

Intel's CPU shortage has hit the PC market hard the last six months, but while it's expected to linger into the back half of the year, it's also expected to start improving before too much longer. Intel made a strategic decision to de-prioritize shipments of low-end CPUs, effectively ceding some of this space to AMD. Instead, the larger company focused on its highest-end markets and first-tier partners, ensuring an adequate supply of chips to these divisions and partners, while other companies building lower-end parts have turned to AMD.

<https://www.extremetech.com/computing/290995-intel-cpu-shortage-expected-to-ease-in-june>

#### ■ Q1 2019 Semiconductor Sales Fell By 4th-Largest Decline in 35 Years

The semiconductor market may be facing a grim 2019 after the first quarter chewed the hell out of overall sales. Some seasonal decline is always expected in certain markets — anything related to desired consumer goods always takes a hit after Christmas — but the drop in revenue in Q1 2019 is one of the largest in history.

<https://www.extremetech.com/computing/290738-q1-2019-semiconductor-sales-fell-by-4th-largest-decline-in-35-years>

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15-19 September 2019  
Monterey Conference Center and Monterey Marriott  
Monterey, California, USA

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**You are invited to submit events of interest for this calendar. Please send to [lindad@spie.org](mailto:lindad@spie.org).**