PHOTOMASK

BACUS—The international technical group of SPIE dedicated to the advancement of photomask technology.

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Current understanding of the electrostatic risk to reticles used in microelectronics and similar manufacturing processes

Gavin C. Rider

This paper explains how an electric field and a reticle interact and describes the different kinds of damage that can be caused to a reticle through its exposure to electric field. It is shown why electrostatic reticle damage has changed from ESD damage (which causes yield to suddenly drop precipitously) into a gradual and cumulative form of degradation that is very difficult to diagnose. It is explained why some of the approaches that have been taken to reduce ESD damage in the semiconductor factory, such as equipotential bonding and the use of static dissipative plastics for making reticle pods, actually increase the risk of this cumulative type of electrostatic degradation in reticles. When assessing the risk to reticles and designing an effective protective strategy for reticle handling, it is shown why one must take into account the temporal characteristics of a reticle's interaction with electric field—including the effect that the reticle's immediate surroundings will have on that interaction—as well as considering the strength of any electric field in the reticle handling environment. Solutions are presented that would allow the electrostatic risk to reticles to be reduced significantly, without requiring major changes to operating procedures in semiconductor manufacturing facilities.

To view full article, https://doi.org/10.1117/1.JMM.17.2.020901

EFM damage induced in a test reticle by applying calibrated electric fields: (a) the onset of degradation by EFM type 1, with a meniscus forming at the base of the chrome line (appearing as a widening of the dark edge of the feature). (b) Complete bridging of the gap between features by chromium that has migrated through EFM type 2. (Atomic force microscope images courtesy of International Sematech).

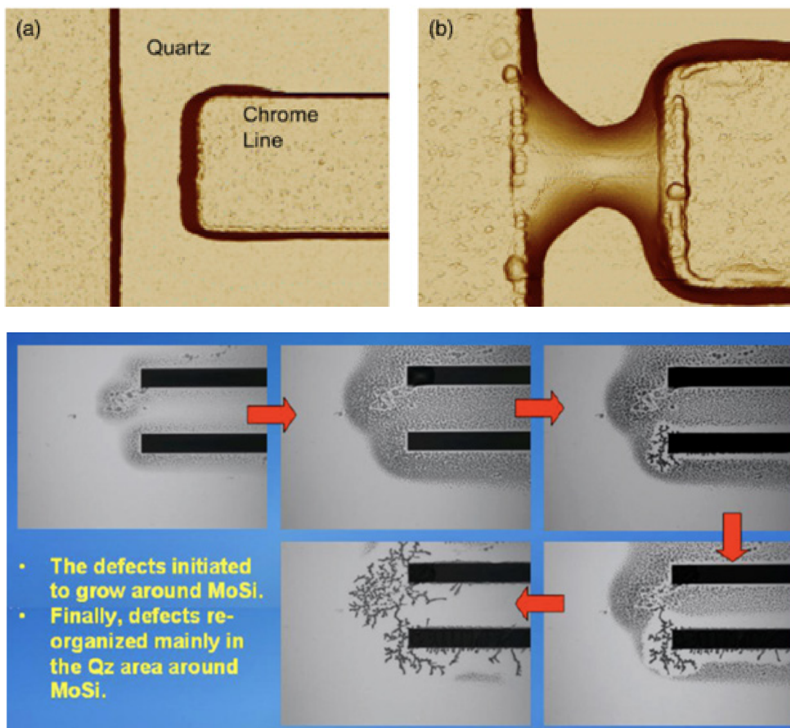

Fig. 8 The progression of haze formation in a MoSi reticle.17 Haze growth is seen to be enhanced around the tips of the lines, which is where electric field strength would be concentrated if an electric field should penetrate the reticle.

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Editorial

Cost of Ownership: A Perspective

Douglas J. Resnick, Canon Nanotechnologies Inc.

My introduction to the semiconductor industry started back in 1981 at Bell Laboratories, in Murray Hill, New Jersey. I was accepted into the VLSI group, which had just started a proximity x-ray lithography program. My assignment was to design, build and characterize a CVD system, in order to deposit a boron nitride film which served as the equivalent of a more standard photomask blank. Keep in mind that the capital equipment infrastructure that supported the semiconductor industry was still under development, so there was no option for buying a CVD system that used diborane and ammonia. The prospect of having to build the system from scratch was intriguing, so I accepted the assignment, despite the fact that I had no experience whatsoever with chemical vapor deposition processes (My graduate work focused on superconductors, and liquid nitrogen temperatures were as high as I ever needed to consider).

As I went through the process of designing and building the system, I quickly learned about the hazards of gases such as diborane and decided that additional safeguards were required to protect both myself and others in the cleanroom. The first design upgrade was a burn off furnace designed to decompose the diborane. The second was an exhausted enclosure to isolate the gases in case of a vacuum leak. The third was a diborane detector system with 0.10 ppm detection capability. The final modification involved automating the entire CVD process, in order to ensure that the process was proceeding correctly and to shut down the system in case of an excursion. Every proposed modification and upgrade was approved. From there, the tool was finished, characterized and became part of a pilot line. Throughput for the CVD system was about 25 wafers over four hours for a four micron film.

Looking back at this experience, however, I realized that through the entire process, nobody ever asked me following questions:

What are the costs for the tool upgrades?

What is the cost of ownership of your deposition process, and

What is the cost of ownership contribution to both the x-ray mask and a device level?

The first question I could have answered, since I generated the purchase orders. But this was Bell Labs in the early 1980's, and there was more than enough money to go around, so this never seemed to be an issue. I could not have answered the next two questions, however, and I suspect nobody else in the building knew the answer either. To some degree, however, that was ok, since at the time, we were all chasing resolution (It was clear optical lithography was going to fail at 0.50 micron.). All options were on the table (DUV, x-ray, ion projection, electron beam and so on) and the goal was to establish new technology that would extend the lithographic roadmap.

About ten years ago, the equation changed with the introduction of pitch splitting technologies such as Litho/Etch and spacer patterning. Now it became possible to make small features with existing litho tools, but the possibility came with a price: both technical and financial.

Now when I speak with customers, the first two questions that are asked are:

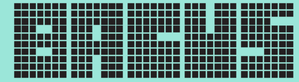
What value does your technology bring?

What is the cost of ownership?

The technical price we pay for pitch splitting comes in the way of critical dimension control and additional overlay terms (pitch walking). Despite the precision of our newest deposition and etch processes, the additional process steps used to reduce pitch introduce these types of errors. Any technology (NIL and EUVL for example) that can deliver a single litho step process has the opportunity to deliver a simplified solution with better CD and overlay control.

Cost of Ownership (CoO) cannot be answered simply, because you need to understand the particular level that requires attention and what existing technology is being used (LELE, SADP, SAQP (and with how many cut levels)) so that you can correctly compare your technology to the existing solution or future solutions. CoO might vary significantly between a 20nm half pitch contact level and an SAQP level requiring a single additional litho cut. You also need to worry about the limitations of your own process. For NIL, that might be mask life. For EUVL, that might be stochastics.

So here I am, thirty-seven years into my career, and I am perfectly capable of answering the CoO questions. Now all I need is for someone to explain why the cost pressures exist, given that memory profit margins are as high as 70% these days.



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Industry Briefs

Chip Sales Running 20% Above 2017 Pace

Semiconductor sales ran 20 percent ahead of 2017's pace through the first quarter of the year, a strong start to the year in an industry coming off record revenue, according to the Semiconductor Industry Association (SIA) trade group.

https://www.eetimes.com/document.asp?doc_id=1333249

TSMC Details 5 nm Process Tech: Aggressive Scaling, but Thin Power and Performance Gains

At a special event last week, TSMC announced the first details about its 5 nm manufacturing technology that it plans to use sometime in 2020. CLN5 will be the company's second fabrication process to use extreme ultraviolet (EUV) lithography, which is going to enable TSMC to aggressively increase its transistor density versus prior generations.

https://www.anandtech.com/show/12727/tsmc-details-5-nm-process-tech-aggressive-scaling-but-thin-power-and-performance-gains

Key Findings for the Global Lithography Systems Market

Technavio's latest market research report on the global lithography systems market provides an analysis of the most important trends expected to impact the market outlook from 2018-2022. Technavio defines an emerging trend as a factor that has the potential to significantly impact the market and contribute to its growth or decline.

According to Technavio market research analysts, the CAGR for the global lithography systems market is projected to be over 5% during the forecast period. However, the growth momentum of the market is expected to decelerate due to a decrease in the year-over-year growth.

http://electroiq.com/blog/2018/04/key-findings-for-the-global-lithography-systems-market/

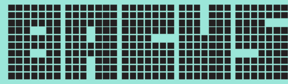
TSMC's Roadmap Full, but Thin EUV Readied for 7, 5 nm — but Gains Decline

SANTA CLARA, Calif. — Continuing to move fast in multiple directions at once, TSMC announced that it is in volume production with a 7-nm process and will have a version using extreme ultraviolet (EUV) lithography ramping early next year.

https://www.eetimes.com/document.asp?doc_id=1333244

Webcast About Enabling EUV and the Patterning Roadmap

The Solid State magazine offers the platform for this webcast. It will be held by Greg McIntyre, Director of Advanced Patterning, imec on Tuesday, June 5, 2018 at 1:00 p.m. ET.



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About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

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- Subscription to BACUS News (monthly)
- Eligibility to hold office on BACUS Steering Committee

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- Subscription to BACUS News (monthly)
- One online SPIE Journal Subscription
- Listed as a Corporate Member in the BACUS Monthly Newsletter

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CALENDAR

2018

SPIE Photomask Technology + EUV Lithography
17-20 September 2018
Monterey Convention Center
Monterey, California
www.spie.org/puv

The 34 European Mask and Lithography Conference, EMLC 2018
19-20 June 2018
MINATEC Conference Centre
Grenoble, France
www.emlc-conference.com

2019

Photomask Japan
16-18 April 2019
PACIFICO Yokohama
Yokohama, Japan
www.photomask-japan.org

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