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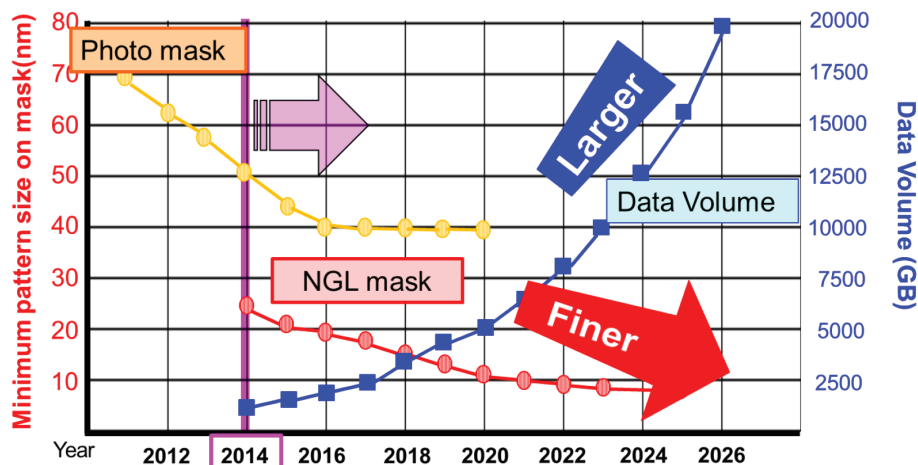
Best Paper - SPIE Photomask Japan 2014

High performance mask fabrication process for the next-generation mask production

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ABSTRACT

ArF immersion lithography combined with double patterning has been used for fabricating below half pitch 40nm devices. However, when pattern size shrinks below 20nm, we must use new technology like quadruple patterning process or next generation lithography (NGL) solutions. Moreover, with change in lithography tool, next generation mask production will be needed. According to ITRS 2013, fabrication of finer patterns less than 15nm will be required on mask plate in NGL mask production 5 years later.¹ In order to fabricate finer patterns on mask, higher resolution EB mask writer and high performance fabrication process will be required. In a previous study, we investigated a potential of mask fabrication process for finer patterning and achieved 17nm dense line pattern on mask plate by using VSB (Variable Shaped Beam) type EB mask writer and chemically amplified resist.^{2,3} After a further investigation, we constructed higher performance mask process by using new EB mask writer EBM9000. EBM9000 is the equipment supporting hp16nm generation's photomask production and has high accuracy and high throughput. As a result, we achieved 15.5nm pattern on mask with high productivity. Moreover, from evaluation of isolated pattern, we proved that current mask process has the capability for sub-10nm pattern. These results show that the performance of current mask fabrication process have the potential to fabricate the next-generation mask.



ITRS2013

Figure 1. Minimum pattern size on photomask and NGL mask.

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EDITORIAL

SEMI Advanced Semiconductor Manufacturing Conference 2015

Jacek. K. Tyminski, Nikon Research Corporation of America

The 26th Annual SEMI Advanced Semiconductor Manufacturing Conference, ASMC 2015, took place on May 3-6, 2015 in Saratoga Springs, NY. The conference was co-chaired by Matthew Wagner of Pall Corporation and Brett Williams of ON Semiconductor. I have been pleased with the quality and the range of ASMC 2015 presentations. BACUS community can benefit from inviting ASMC contributors, to exchange views and to share expertise. The short list presented below indicates some of the key players.

About 350 participants from 140 organizations were represented at this year ASMC. The conference was attended by professional affiliated with GLOBALFOUNDRIES, IBM, Intel, TSMC, Micron, ST Microelectronics, Infineon, Applied Materials, KLA-Tencor, and representatives of other device makers, tool and material suppliers, and members of academia. It featured over seventy technical presentations organized in 15 sessions, including poster session. The presentations focused on topics such as advanced equipment and materials, advanced metrology, yield enhancement, advanced patterning and design for manufacturing, advanced process control, contamination free manufacturing, defect inspection, emerging technologies, equipment reliability, data management, productivity enhancement, and factory optimization. The dominant theme of this year's ASMC was impact of patterning on IC yield in high volume manufacture.

There were three keynotes delivered during the conference. The first one was presented by Thomas Caulfield, Sr. Vice President at GLOBALFOUNDRIES, The title of his presentation was "Expanding Value Creation Through Eco-System Collaboration". This keynote shared a foundry's perspective on the forces reshaping the industry and stressed that the industry is creating new value by continued consolidation, and gaining a competitive advantage through broad IC community collaboration. The second keynote was by Frances M. Ross, Research Staff at IBM T.J. Watson Research Center, about "A Dynamic View of Nanostructure Growth". The speaker pointed out that nanostructured materials are key components of present and future microelectronic devices. The speaker discussed how electron microscopy can visualize semiconductor and metal nanostructures during their formation, providing dynamic information helping to develop new types of nanostructure.

The third keynote was by Robert Maire, President at Semiconductor Advisors, who discussed "The Semiconductor Industry at an Economic Crossroads". The semiconductor industry consolidation has created dynamics with the supply side shrinking while the demand side is increasing. It was reflected by microelectronics industry evolution from mainframes, to minicomputers, to desktops, laptops, smart phones & tablets, wearables & IOT.

The conference covered wide range of topics of interest to IC making community. In Yield Enhancement session, a team from IM Flash, Micron and Intel presented "Collapse-Free Patterning of High Aspect Ratio Silicon Structures for 20nm NAND Flash Technology". Vikram V. Iyengar discussed validation of pattern collapse model for 20 nm NAND technology through analysis of data obtained from defect analysis and electrical tests. The conclusions drawn from model resulted in dramatic reduction in pattern collapse defects.

In Advanced Patterning session, Amit Srivastava, presented work of GLOBALFOUNDRIES and KLA-Tencor team on "In-line Inspection of DRC generated Hotspots". The presenter discussed detection of hotspots using Broadband Plasma-based NanoPoint inspection. This method is a part of "silicon verification" loop implemented synchronously between design-for-manufacture and in-line inspection.

Presenting the work of IBM team, Bradley J. Morgenfeld discussed "Monitoring process-induced focus errors using high-resolution flatness metrology". The authors proposed an in-line method to measure wafer topology changes by using Patterned Wafer Geometry tool, to establish effective planarization strategies. The method features high sampling rate and, when adopted in-line, can help to stabilize patterning performance.

In 3D/TSV session, Nikon Corporation and Osaka University team presented "Precision Wafer Bonding Process for Future Cost-Effective 3DICs". Kazuya Okamoto discussed a high-precision wafer-to-wafer bonding system for three-dimensional integrated circuits. Wafer-to-wafer stacking with 1-2 micron Through Silicon Vias, requiring wafer alignment overlay under 100 nm, allows Cu-bonding of 3DICs by thermos-compression.

One of the highlights of ASMC 2015 was panel discussion moderated by Paul Werbaneth, Contributing Editor of 3D InCites. The theme of the panel was "Semiconductor Manufacturing: Keeping the Silicon Magic Alive". The panelists, Kerry Bernstein from DARPA, Danielle Merfeld from GE Global Research, Jeffrey Marks from Lam Research, Lynn Fuller from Rochester Institute of Technology, and Robert Maire, from Semiconductor Advisors, presented a range of views on the IC industry status quo, and shared their opinions on how to keep the industry vibrant and delivering values the IC users have grown to expect over the many decades of the industry success. The lively exchanges between the panelists and the conference participants reflected the relevance of panelist's opinions to the IC making community.



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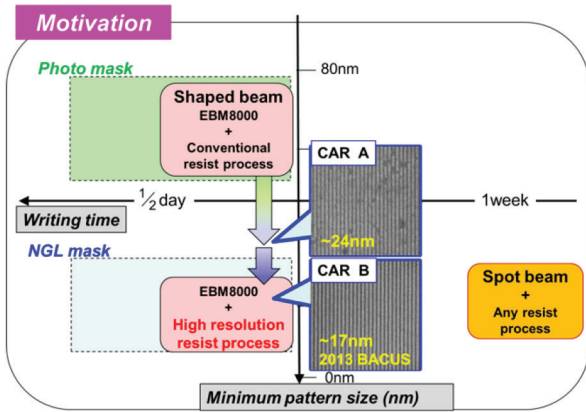


Figure 2-1. Our action plan with EBM8000.

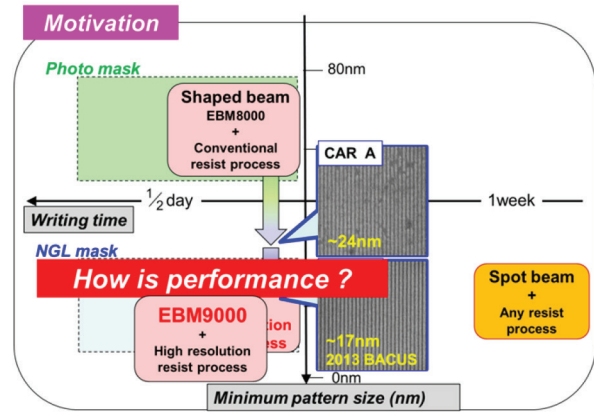


Figure 2-2. Our action plan with EBM9000 in this work.

1. Introduction

Circuit patterns of semiconductor devices have continued pattern shrinking to keep up with Moore’s law. Recently, argon fluoride (ArF) lithography combined with double patterning is most appropriate tool for lithography with a half pitch of 30nm (hp30nm). However, the resolution limit of ArF immersion system is hit a peak at 40nm. So, when pattern size shrinks below 20nm, we must use other technology like quadruple patterning process or next generation lithography (NGL) solutions.

Moreover, next-generation mask production will be needed with change of lithography tool. According to ITRS2013, sub-20nm pattern on mask will be required near future (Fig 1).¹ On the other hands, EB data volume increases exponentially accompanying finer design rules. It will swell up 10 times in ten years. So we must develop high performance mask fabrication process which has high resolution and high productivity corresponding to EB data volume.

Figure 2-1 and 2-2 show our action plan to achieve this roadmap. In this graph, vertical direction shows minimum pattern size on mask and horizontal direction is writing time to write one mask.

Now, in photomask production, from a viewpoint of quality control, we would like to write one mask within one day. And it does not change in NGL mask production either. To achieve this target, we have focused on development of EB writing and resist process.

About EB writing machine, there are mainly a spot beam type and variable shaped beam type EB writer. Spot beam type EB writer with 100kV of acceleration voltage is often used for researching the pattern resolution. Because of spot type EB writer has high beam resolution by narrowing down to 2nm beam. But spot beam EB writer is very difficult from view of writing time issue. When the full field of 6 inches mask is written, it takes more than few weeks to write one mask.⁴

Therefore, we have chosen the VSB type EB writer and chemically amplified resist (CAR). This process is widely used for photomask production but we didn’t understand a potential from the view point of finer patterning. So we examined a potential for finer patterning and achieved 17nm dense line pattern before half a year (Fig 2-1). This result means that the photomask process has the capability for NGL mask production.

Moreover, in this study, we constructed higher performance mask process by using new EB mask writer EBM9000 which is developed by NuFlare Technology (Fig 2-2). EBM9000 is equipment which has current density of 800A/cm² and a three stage deflection system. As a result, it has high throughput and high shot

placement accuracy and it is supporting a hp16nm generation’s photomask production. Our motivation is “How is performance of current mask process with EBM9000”.

From evaluation of resolution limit, we achieved 15.5nm pattern on mask with high productivity. This pattern size is required 5 years later in ITRS and we have the possibility to achieve the requirement of 2018. In addition, from evaluation of isolated pattern, we proved that current mask process has the capability for sub-10nm pattern. These results show that we get closer to NGL mask production more and more.

2. Experimental Conditions and Results

2-1. Preparation of evaluation mask

In this study, we used standard photomask blank with conductive hard mask and positive tone CAR. The reason for having used CAR is high sensitivity. The sensitivity of CAR is several times higher compared with non-CAR such as ZEP and HSQ. It is expected to write one mask included finer pattern with less than 24 hour. With regard to pattern fabrication, we used standard mask production process which includes EB writing, PEB (post exposure bake), development and etching. Table 1. shows the equipment used in each process. Every equipment including EBM9000 is currently used for photomask production. So we don’t special equipment for finer patterning in this work. After pattern fabrication on mask, pattern images were captured by CD-SEM.

Table 1. Equipment used in evaluation.

| Process | Equipment |
|-------------|--|
| Writing | EBM-9000 (NuFlare Technology) / 50kV VSB |
| PEB | ACT-M PEB (Tokyo Electron limited) |
| Development | PGSD (Tokyo Electron limited) |
| Etching | ARES (Shibaura Mechatronics) |

2-2. Result of dense line patterning

To examine the performance of current mask process, we evaluated dense line pattern which is widely used as the basis for resolution limit. Fig 3-1 shows the result of etched pattern SEM images designed 16nm dense line pattern. Writing area is 500um x 100um and SEM images captured with 1um FOV(Field of view).

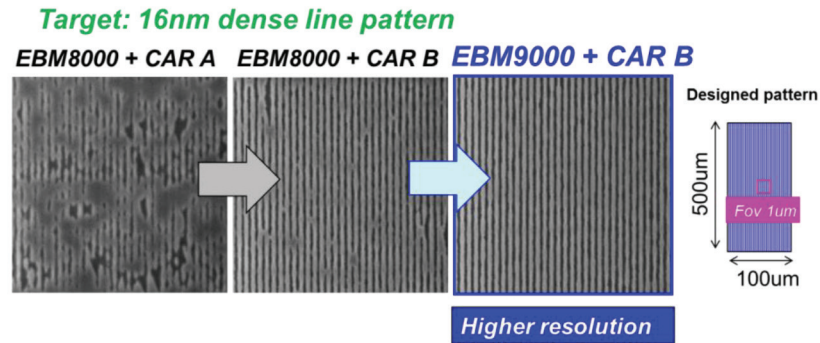


Figure 3-1. Etched pattern SEM images designed 16nm dense line pattern.

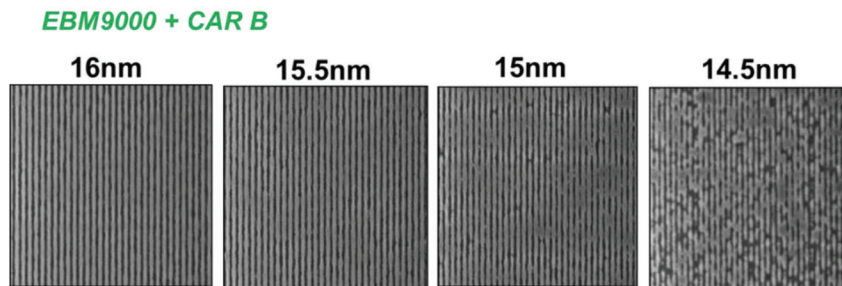


Figure 3-2. Etched pattern SEM images fabricated with EBM9000.

As a result, 16nm dense line pattern was formed without defect only in EBM9000 process. We confirmed that EBM9000 with higher shot accuracy is reflected in improving of patterning on mask. In addition we evaluated below 16nm patterns using EBM9000. This result is described in Fig. 3-2. From the result of evaluation, we achieved 15.5nm dense line pattern. According to changing EBM9000 from EBM8000, performance for finer patterning increases from 17nm to 15.5nm. 15.5nm pattern is required 5 years later in ITRS and we have the possibility to achieve the requirement of 2018.

In contrast, below 15nm patterns have defect. Especially, performance differs greatly between 15nm and 14.5nm. In 15nm pattern, shot stitching defects are observed in the x direction on SEM image. This problem is caused by systematic error of EB writer and more highly adjustment is needed. On the other hands, 14.5nm pattern is not resolved at all. So we think that resolution limit of dense line pattern on this process is around 15nm.

Next, we carried out quantitative evaluation by using image analysis which is the same evaluation as before.³ Figure 4 shows a method of the image analysis. This analysis is very simple and easy. Firstly, we converted the captured SEM images to binarized images and prepared designed image. Secondly, pattern error spots were extracted with subtraction of binarized images and designed image. In this analysis, pattern error means defects and LER. After extracted pattern error spots, we estimated "pattern forming rate" with simple calculation as equation (2.1).

$$\text{Pattern forming rate} = \left(1 - \frac{\text{Irregular area}}{\text{Evaluation area}}\right) \times 100$$

Figure 5 shows result of pattern forming rate for each pattern size. The y-axis of graph shows pattern forming rate and purple line indicates practical limit which is extracted from Gate CD control in ITRS. When pattern forming rate exceeds this line, it means the performance to apply for mask production. From the result of evaluation, pattern forming rate increases by using EBM9000. And

also in this analysis, we confirmed that current mask process with EBM9000 has the capability for 15.5nm patterning. In contrast, pattern forming rate of 14nm pattern is very low. A large gap exists between 15nm and 14nm pattern. So, we thought why below 14nm dense line patterns cannot be resolved?

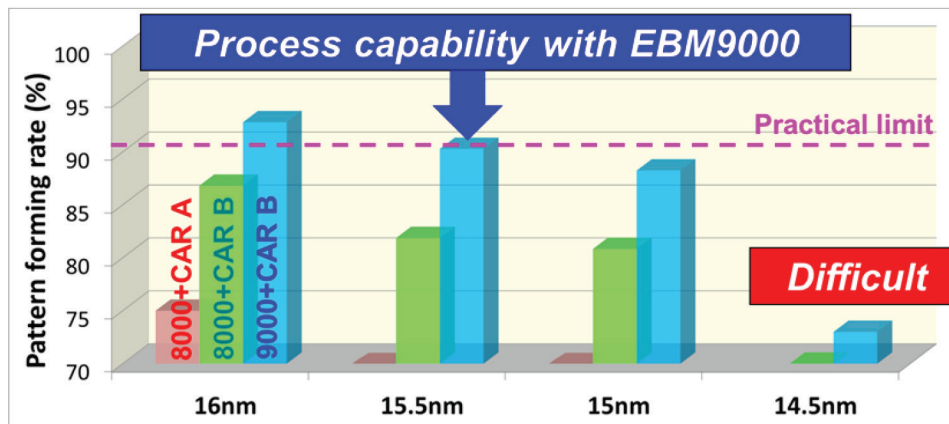
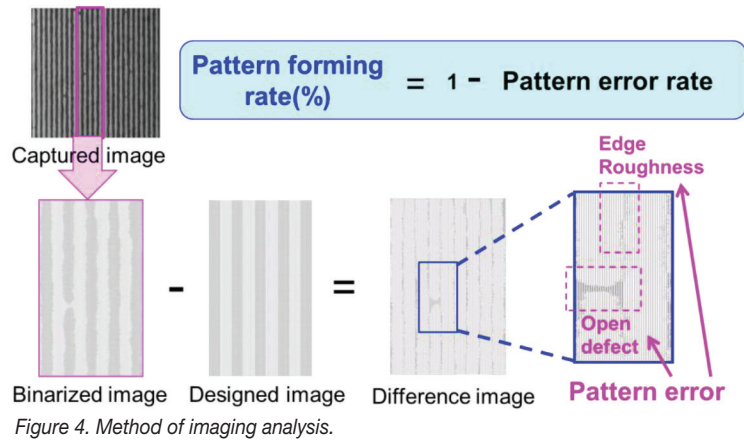
2-3. Discussion: Influence of overlapping beam tails

In next step, we discussed using energy profile simulation why below 14nm dense line patterns cannot be resolved.

VSF profile is expressed as error function which is convolution function of Gaussian. The two-dimensional beam profile at the time of writing to design data becomes such as Figure 6. Figure 6 shows the simulation result of the amount of electrons entered into the substrate in 50nm and 14nm dense line pattern. In this graph, the x-axis shows a distance between patterns and the y-axis indicates intensity of incident electrons, and green line shows process threshold. In this simulation, we calculated as beam resolution is 10nm and a backscattering estimated as 30% of incident electron energy.

As a result, 50nm described in Figure 6 (a) has high energy profile contrast between exposure area and unexposure area. In contrast, energy profile contrast of 14nm described in Figure 6 (b) is low and contrast rate decreases about 60% than 50nm. The energy profile contrast of both are decreased by the backscattering, but in hp14nm, overlapping of approximal beam tails decrease the energy profile contrast much further. This phenomenon occurs when pattern size gets near to beam resolution of EB writer. This problem can't be improved by dose control.

Here, for decreasing beam overlap, we examined using isolated pattern. We calculated the energy profile of 1:3 (space:line) isolated pattern designed 14nm under the same conditions and created this pattern on mask as the same process. Figure 7 shows simulation result and pattern forming rate of 14nm pattern. In the simulation result, the energy profile contrast of 1:3 isolated pattern is high about 60% compared to dense line pattern. This result is reflected in patterning on mask. Pattern forming rate of 14nm pattern in-



creased from 71.2% to 93.2%. This value exceeds practical limit described in section 2-2 and 14nm SEM image have no defect. So, if energy profile contrast is acquired sufficiently, below 14nm patterning is possible. But to decrease beam overlap on dense line pattern, higher beam resolution is needed.

In addition, we evaluated the ultimate resolution by using 1:3 isolated pattern. These SEM images described in Figure 8 are results of pattern forming from 11nm to 8nm. As a result, we achieved 10nm patterning with intended size and although there is a few defects, 9nm pattern can be resolved. We indicated that mask fabrication process has capability for sub-10nm patterning. Sub-10nm patterning technology may be able to apply for DSA guide patterning, wafer direct patterning or double patterning of 1:3 isolated pattern. And to achieve below 8nm pattern, we must investigate the resolution or physical limit of resist material.

3. Summary

We have investigated the capability of current mask process for NGL mask production. Especially, in this work, we tried to fabricate finer pattern by using new EB writer EBM9000 which is high accuracy.

As a result, we achieved 15.5nm dense line pattern. And from the evaluation of 1:3 isolated pattern, we proved that current mask process has capability for Sub-10nm patterning. We found two things from these results.

Firstly, EBM9000 with high shot accuracy is reflected in improvement of patterning. In NGL mask production, shot placement ac-

curacy becomes very important to the pattern formation as well as beam resolution. EBM9000 is very superior about this point. Secondly, according to decrease beam overlap, sub-10nm can be fabricated on mask with current mask process. Therefore, resist process has the capability to resolve less than 10nm pattern. These results mean that future NGL mask production is becoming much more realistic. After this study, we will increase writing area and carry out more highly adjustment about shot offset, shot gain, shot rotation.

4. References

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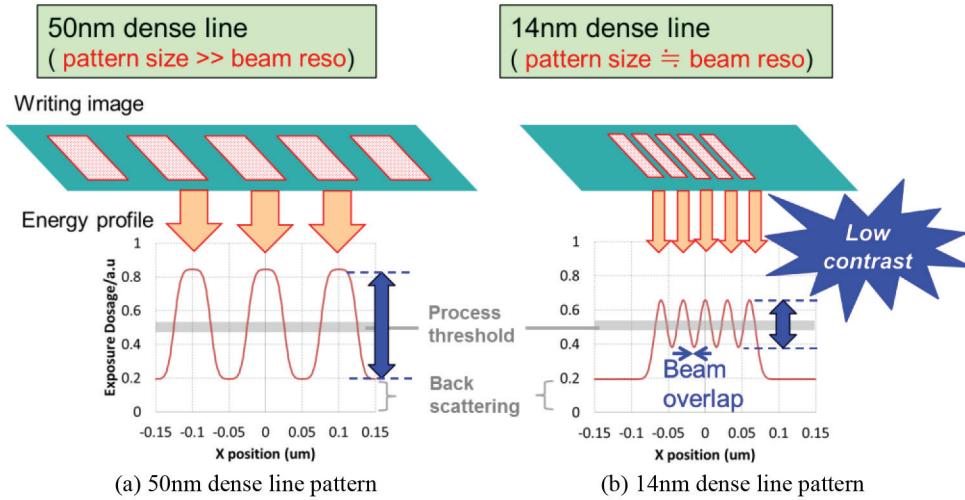


Figure 6. The energy profile simulation.

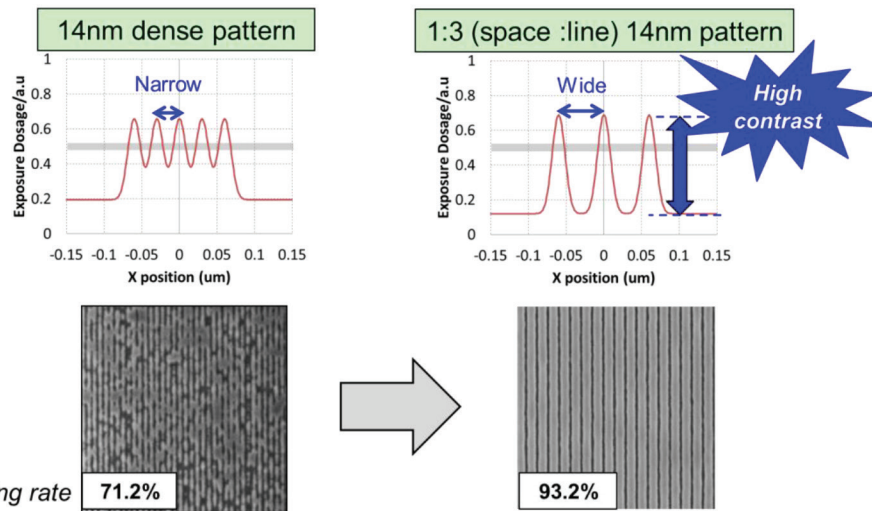


Figure 7. Examination of decreasing beam overlap.

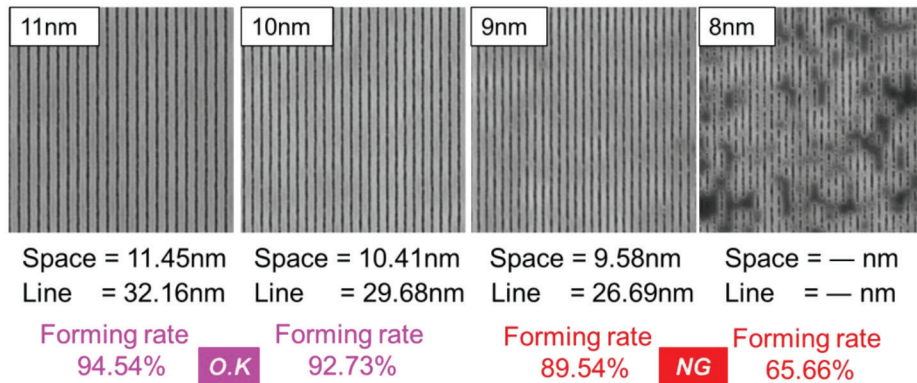


Figure 8. Performance of 1:3 (space:line) isolated pattern.



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Industry Briefs

■ JSR and imec partner to enable EUV lithography resist solutions

By: Solid State Technology

JSR Corporation, a materials company and imec, a nanoelectronics R&D center, signed a Letter of Intent (LOI) to partner in enabling manufacturing and quality control of EUV lithography materials. This partnership will be formalized by establishing a joint venture with imec as minority shareholder. The signing ceremony was held at the Embassy of the Kingdom of Belgium in Tokyo (Japan).

Imec and JSR's collaboration, will allow both companies to leverage their strengths when developing photoresist solutions. JSR will provide manufacturing technology to the joint venture including upgrading the facility at its wholly owned subsidiary in Belgium, JSR Micro NV, by installing manufacturing and analytical equipment. Imec will provide expertise and services to the joint venture for quality control on materials.

"JSR has been a strategic partner of imec for a long time, and I am excited with this intensified collaboration," stated Luc Van den hove, president and CEO at imec. "The partnership enabled through close proximity between the JSR manufacturing facility and the imec technology platform will allow our partners to gain access to best-in-class materials for next-generation technologies."

Nobu Koshiba, President of JSR Corporation, said: "JSR has successfully developed not only chemically amplified photoresists, but also newly designed chemistries with very high sensitivity and good productivity. Our strength has also extended to peripheral materials, such as multilayer materials. The industry is requesting material suppliers to prepare manufacturing infrastructure and quality control capabilities for defect-free solutions, as well as to improve photoresist performance to match EUV exposure equipment."

■ ASML reaches agreement for delivery of minimum of 15 EUV lithography systems

By: VELDHOVEN

ASML announced that it has signed an agreement with one of its major US customers to deliver a minimum of 15 ASML EUV lithography systems to support increased development activity and pilot production of future-generation manufacturing processes. The customer intends to use EUV lithography for multiple processing steps in future process technology nodes. The delivery of the first two NXE:3350B EUV systems is expected before the end of 2015. The new systems will be in addition to the existing EUV development systems already at the customer. Financial terms were not disclosed.

"EUV is now approaching volume introduction. Long-term EUV planning and EUV ecosystem preparation is greatly supported by this commitment to EUV, kick-starting a new round of innovation in the semiconductor industry. The commitment extends the planning horizon and increases the confidence in EUV," ASML President and Chief Executive Officer Peter Wennink said.

■ PHOTRONICS promotes Dr. Peter Kirilin to Chief Executive Officer

By: BROOKFIELD

Photronics, Inc. announced that as part of a long-term succession planning process, Dr. Peter Kirilin has been promoted from President to Chief Executive Officer, effective May 4, 2015 and will join the Company's Board of Directors. Constantine ("Deno") Macricostas, Photronics' current Chairman and CEO, will continue on the Board of Directors as Executive Chairman.

Join the premier professional organization for mask makers and mask users!

About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

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