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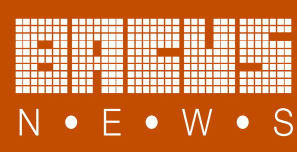

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Best Student Paper

Metal1 patterning study for random-logic applications with 193i, using calibrated OPC for Litho and Etch

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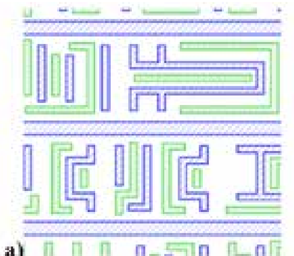
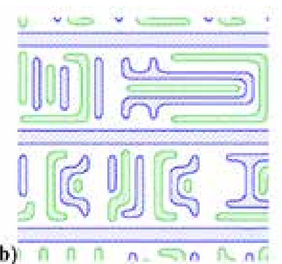
ABSTRACT

A Metal1-layer (M1) patterning study is conducted on 20nm node (N20) for random-logic applications. We quantified the printability performance on our test vehicle for N20, corresponding to Poly/M1 pitches of 90/64nm, and with a selected minimum M1 gap size of 70nm. The Metal1 layer is patterned with 193nm immersion lithography (193i) using Negative Tone Developer (NTD) resist, and a double-patterning Litho-Etch-Litho-Etch (LELE) process. Our study is based on Logic test blocks that we OPCed with a combination of calibrated models for litho and for etch. We report the Overlapping Process Window (OPW), based on a selection of test structures measured after-etch. We find that most of the OPW limiting structures are EOL (End-of-Line) configurations. Further analysis of these individual OPW limiters will reveal that they belong to different types, such as Resist 3D (R3D) and Mask 3D (M3D) sensitive structures, limiters related to OPC (Optical Proximity Corrections) options such as assist placement, or the choice of CD metrics and tolerances for calculation of the process windows itself. To guide this investigation, we will consider a 'reference OPC' case to be compared with other solutions. In addition, rigorous simulations and OPC verifications will complete the after-etch measurements to help us to validate our experimental findings.

1. Introduction

With the delay of inserting EUV into high volume manufacturing, mature 193nm immersion lithography appears to be the most reliable option to tackle the critical layers for the next Logic nodes, such as the Metal1 (M1) layer studied in this paper.[1-5] Rather than using a single exposure, as in the case of EUV, several exposures are needed to overcome the Rayleigh resolution limit determined at 193i. Indeed, multiple patterning techniques, such as LEn or SAMP (Self-Aligned Multiple Patterning), are being used today and studies on





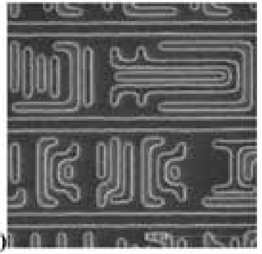


Figure 1. a) N20 M1 clip design layout example with both splits (split1 or M1A in blue and split2 or M1B in green); b) after-etch predicted contours for both splits at nominal litho conditions; c) CD-SEM picture of the complete LELE flow after-etch (into the hard mask) is shown.

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Editorial

Highlights of 25th Advanced Semiconductor manufacturing Conference

J. K. Tyminski, Nikon Research Corporation Of America

The 25th Annual SEMI Advanced Semiconductor Manufacturing Conference, ASMC 2014, organized by SEMI (http://www.semi.org/node/38316), took place on May 19-21, 2014 in Saratoga Springs, NY. The conference was co-chaired by Israel Ne'eman, Applied Materials and Oliver Patterson, IBM Microelectronics. The attendees were from GLOBALFOUNDRIES, IBM, Intel, TSMC, Micron, ST Microelectronics, Infineon , G450C, Applied Materials, KLA-Tencor, and representatives of other IC makers as well as tool and material suppliers, and members of academia. For three days, some 300 of industry professionals from around the globe networked and shared knowledge on new and best-method semiconductor manufacturing practices and concepts. The conference featured over 90 technical presentations organized in 14, dual-track sessions and a poster session. The presentations focused on range of topics such as advanced equipment and materials, advanced metrology, advanced patterning and design for manufacturing, advanced process control, contamination free manufacturing, data and yield management, defect inspection, discrete power devices and emerging technologies, equipment reliability, productivity enhancement, factory optimization, and yield enhancement. The conference included three keynotes, a panel discussion and two tutorials.

A keynote on **Advanced Manufacturing for Foundry Business** was presented by John Lin, Vice President and General Manager of Operation of G450C Consortium, assigned from TMSC. The presenter pointed out that emergence of mobile computing is reinforcing business model based on design-house and foundries collaboration. TSMC have a dominant share in all mobile components production and is gearing up for the Next Big Thing, the Internet of Things, IoT. TSMC expects that in 2017, the number of IOF devices will be equal to all the rest of integrated, digital electronics devices.

The second keynote was **Innovation Pipeline for 10nm and Beyond presented by Mukesh V. Khare**, distinguished Engineer and Director at IBM's Albany NanoTech Research Center in New York. The presenter tracked device innovation from bipolar transistors through planar CMOS to FinFET. He pointed out that the future technologies drivers are nano-wires, and Carbon Nano Tubes. Below 7 nm design node, all-around gate made from Si and C nanotubes will be required. The challenges for this technology are purity, placement control, and scalability of nano-technology devices.

The third keynote had title **From Germanium, to Gallium Arsenide, to Silicon and back again: a Perspective on the Semiconductor Manufacturing Industry** and was presented by Dean Freeman, research VP in Gartner Research. The presenter pointed out that there are over a billion devices currently connected to the internet. The trend will continue leading to the Internet of Things. Diversification of consumer electronics products will stimulate growth of IC design house/foundry business model. To succeed, the designs have to be closely linked with the foundry production lines, deepening of Design for Manufacture approach.

The conference panel discussion focused on "**25 Years of Semiconductor Manufacturing: Accomplishments, Current Challenges, Future Directions - From the Internet to the Internet of Things**" moderated by Paul Werbaneth, Contributing Editor, 3D InCites. The panelists were: Lynn Fuller, Professor, Microelectronics Dept., Rochester Institute of Technology. Dave Gross, Director, Director of Manufacturing Systems Technology, GLOBALFOUNDRIES. William Miller, Sr. Director of Engineering, Qualcomm, Robert Maire, President, Semiconductor Advisors LLC, Charlie Pappis, Group VP, General Manager, Applied Global Services, Applied Materials.

The panelist presented their views on the accomplishments and challenges facing the microelectronics industry. Among the accomplishments, they highlighted: Academic programs to train professionals for IC industry; Development of foundry business model of global reach; Pervasive creation of wealth sparked by invention and development of VLSI; Infrastructure on which information technology and the internet businesses continue to grow; Among the challenges, the panelist pointed out; Continuing need to upgrade IC manufacture infrastructure and economics of mega-fabs; Design shift of mobile devices to to 64 bit, multi-core processors; New electronics application for IoT, automotive and healthcare; Pattering at 10 nm and beyond; 3D/TSV infrastructure and device integration; Continuation of Moore's law beyond 7 nm; Device architecture and materials beyond 5 nm,

The first tutorial of conference was on **Circuit Relevant Patterning with Directed Self Assembly: Overview and Outlook** presented by Michael A. Guillorn, Manager of Nanofabrication and Electron Beam Lithography at IBM. The second tutorial was The second tutorial on **Silicon Photonics** was given by Haisheng Rong, Sr. Research Scientist, Intel Corporation.

Over its 25 year history, ASMC has become a premier forum for professional form the integrated circuit industry to meet and to exchange views on the status and the future of the industry. The conference continues its emphasis on the spectrum issues vital for the IC manufacture. The dominant themes of ASMC 2014 were: 3D/TSV performance and integration, design house-foundry alignment and business, and the future of IC and information technology. Considerable attention was devoted to patterning at nodes of 10 nm and below, with immersion ArF, combined with directed self-assembly seen as a key contender down to 7 nm node. As an attendee who has been participated in many past ASMCs, I am continuing to be very much impressed by the scope of the conference in general and the level of energy palpable in the IC industry today.

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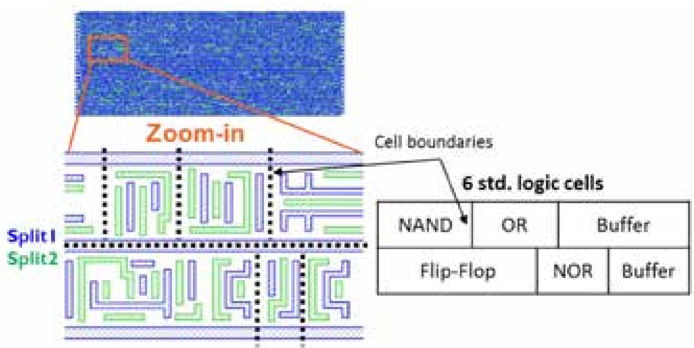


Figure 2. Clip layout of M1 design intent after-DP decomposition referring to split1 and split2, where split1 layer (M1A) contains the ground & power rails (blue color), and split2 layer (M1B) does not (green color).

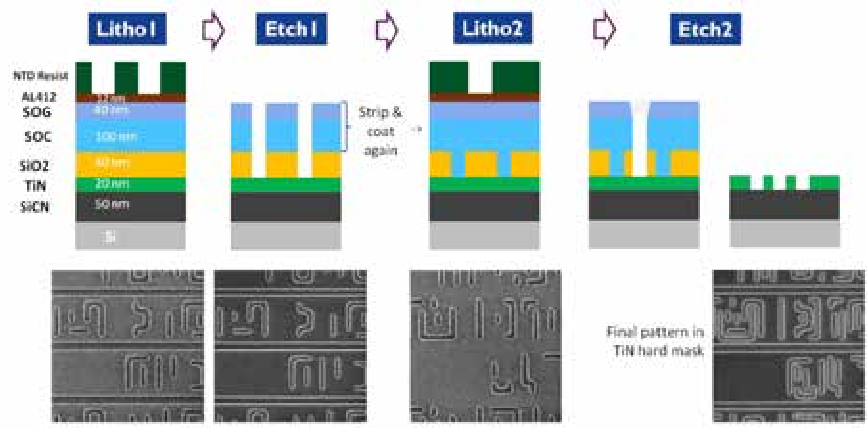


Figure 3. Etch stack & flow for NTD M1 LELE on the top row, and CD-SEM pictures captured for each patterning step after-litho and after-etch on the bottom row.

the layout decomposition capability[6-8] and printability have been reported in the literature. At N20, LELE appears a good candidate for metal-patterning. This study tries to quantify and analyze what is the after-etch printability performance of LELE for N20, from the measured *Overlapping Process Window (OPW) limiters* perspective, taking the example of an N20 Logic M1 test block that we generated. Measuring the Process Windows (PW) of a selection of test structures from this M1 block *after-etch*, we in particular wanted to know what type of structures the OPW limiters were, why they were limiting and whether improvements could be found. Our paper tries to give at least a partial answer to these questions. Where useful, we will also use the results of rigorous lithography simulations or OPC Verification software to confirm our findings and generate a better insight into the mechanisms that drive a structure to be OPW limiting. That's why, we will be able to see whether some of these mechanism types, listed below, really impact the OPW in the case of our test vehicle:

- Mask[8-10] and Resist[11-12] 3D effects.
- OPC and assist-placement optioncs[13-15].
- CD metrics and tolerances[16-18].
- ....

} Overlapping Process Window

As our test vehicle contains also a variation of DR (Design-Rules) and of OPC-solutions, we have been also able to replace some of the limiting structures by a better alternative.

We will give an overview of our results, and conclude on the OPW limiters measured after-etch, linking them to the mechanisms listed above. This study should also provide some useful insights in whether and how current patterning solutions at 193i can be extended to still smaller dimensions and pitches. We would like also to share useful approaches on how to quantify realistically the printability performance of Logic applications with the current available tools.

First, we will begin by describing our test vehicle for 20nm Logic node, named TESPA20, in somewhat more detail. The section will contain information of the design layout (Figure 1.a), OPC modeling (Figure 1.b) and the OPC variations available on the mask. Secondly, section 3 will give details on how we performed the after-etch printability evaluation (Figure 1.c), with respect to structure selection, and individual Bossung measurements on-wafer. Finally, section 4 will assess and analyze the individual after-etch OPW limiters on a 'reference OPC' case, and compare with other alternative solutions in order to see whether some of the OPW limiters we found can

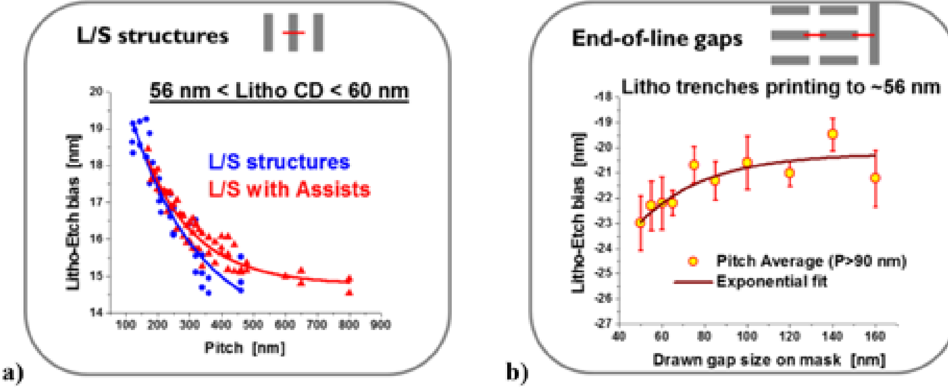


Figure 4. a) Experimental litho-etch bias measured through pitch for L/S at nominal litho conditions, b) through drawn gap size on mask for EOL at nominal litho conditions.

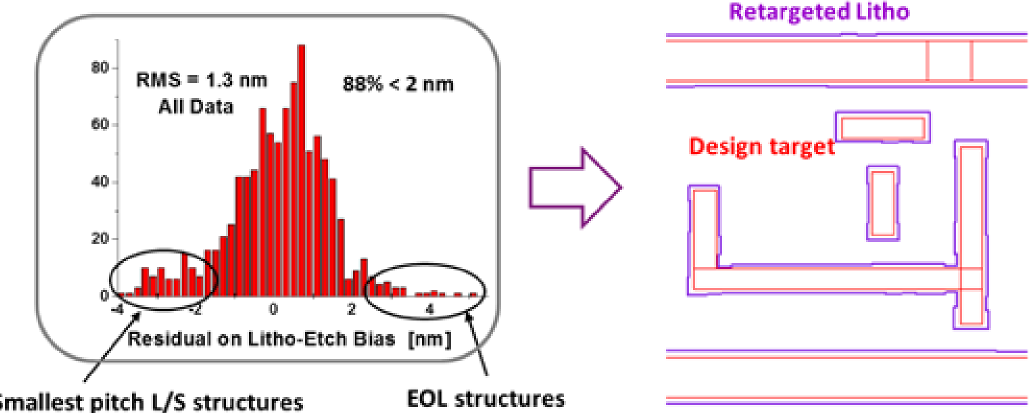


Figure 5. Calibrated litho-etch bias model residuals on all structures on the left, and clip containing the retargeted litho-target on top of the design target on the right.

in fact be removed.

2. TESPA20: A Test Vehicle for 20nm Logic Node Metal1 Patterning

2.1 Design Layout

A realistic random-logic block was created for this study (block size of 83µm by 32µm). It contains multiple rows of randomly placed Logic cells. Every standard cell of the library occurs many times within the Logic block, but every time in a different environment, i.e. surrounded by different standard cell neighbors. The N20 Logic-cell mini library that we used for making these test blocks includes ~50 standard cells representative of the three principal categories of an ASIC (Application-Specific Integrated Circuit): a) Booleans (inverter, NAND, …), b) Complex (Flip-Flop, multiplexer, …) and c) Clock (Buffer, …). Furthermore, inserted 'fill' cells (dummies without any polygon-content) account for around 20% of the total Logic block area, to mimic the occurrence of some amount of un-used area that would occur in a routed-cell application. Figure 2 illustrates some of these. A ground (Gnd) and power rail (Vdd) are running horizontally at the top and bottom edge of the standard Logic cell boundaries. The height of the Logic cell is equal to 10 times the minimum M1 pitch ('10 track' cells), the M1 minimum pitch/width are set to 64/33nm respectively. At N20, M1 still uses bidirectional (2D) polygons[19], but we allowed no stitching between the two metal-layer splits in the cells of the current test vehicle. Hence, the aggressive 2D arrangement makes N20 M1 a difficult patterning layer to be OPCed.

2.2 Modeling: OPC + EPC

We have used the state-of-the art computational tools from EDA vendors to generate proper compact models for modelbased proximity correction. We calibrated a PW model for OPC, i.e. for the litho step, as well as a model (at nominal litho conditions only) for EPC (Etch Proximity Corrections), i.e. for the etch step. We thus account for full-patterning proximity effects, enabling true PPC[20-22] (Process Proximity Corrections). Illustration of the full-patterning LELE process is depicted on Figure 3, where M1 polygons print as trenches on wafer and correspond to the absorber area on the mask (6% attenuated PSM MoSi brightfield mask), as we used a Negative Tone Developer (NTD) resist (resist film thickness of 100nm). Calibrated models for OPC are quite common, so in this sub-section we

Table 1. In-resist printed M1 split1 clip (FOV 75K) comparisons between model-based assist placement (cases A and B) and rulebased assist placement (cases C and D), where case C includes assist printability check and not for case D.

Focus [nm]	A) Model-based 1	B) Model-based 2	C) Rule-based 1 *with assist printability check*	D) Rule-based 2 *without assist-printability check*
Mask				
-60				
-50				
...	...	...	...	...
60				
70				

will emphasize more on the calibrated Litho-Etch bias model rather than the calibrated resist model. The latter has a total error RMS (Root Mean Square) below 2nm through PW.

The etch process we used intended a CD shrink of 15nm from litho to etch, but it is known that this litho-etch bias will be structure dependent, and not have the same value for all structures. This is why we need an EPC step, accounting for this structure dependency. Often rule-based EPC is used, but we decided to go for a model-based EPC (the decision is justified at the end of the sub-section). Intensive effort has therefore been put in measuring litho-etch bias data (i.e. CD after-litho minus measured CD after-etch) for a large number of different structures. We selected many structures, such as trench arrays (300 without assist, 130 with assist), trench doublets & triplets (100 and 80 resp.), and EOL structures (160) with varying pitches, widths and gaps. For a resist-model calibration, an image-parameter-space tool effectively is often used to select the calibration structures. But for etch modeling (for which such tool doesn't exist yet), our 'manual' selection simply leans on covering as best the existing combinations of pitch/width/gap on the Logic block. At nominal litho settings, the structure dependence of the litho-etch bias is quite significant, and can reach up to 8nm range, as can be seen from Figure 4. Both Figures 4.a and 4.b report the experimental litho-etch bias for L/S and EOL structures respectively, targeting CDs after-litho between 56nm and 60nm as an example. The line on the graphs is an exponential fit through the data (not the results of the EPC model fit).The biggest litho-etch bias dif-

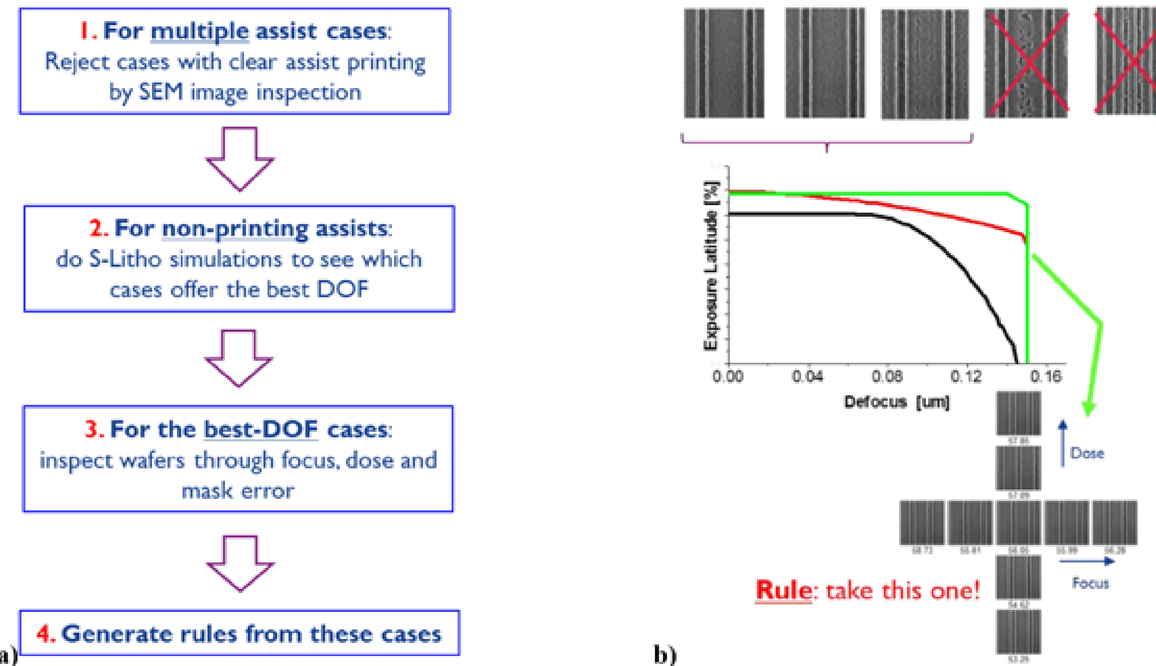


Figure 6. a) Methodology steps for generating the assist rules; b) Simplified illustrations for generating a specific rule.

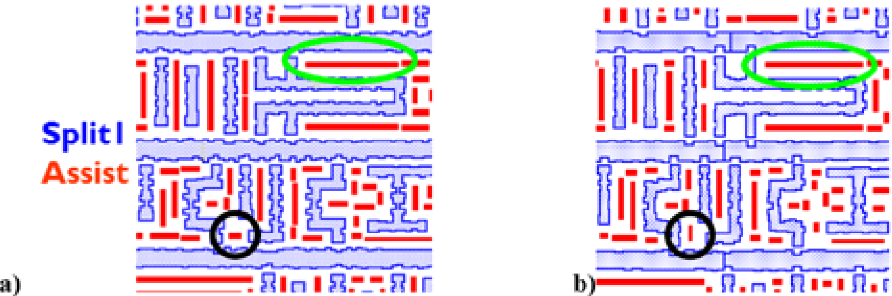


Figure 7. a) & b) OPC solutions using the generated rule-based assist placements.

ference is found for isolated trenches (pitch >300nm) versus small gaps (drawn gap size on mask <70nm). The knowledge of the dependencies observed in Figure 4 could be used to reduce substantially the amount of structures selected for the model calibration (we do believe that a model with the same accuracy could be built from much less structures), and thus the measurement time.

The residual model errors of the 'best' calibrated litho-etch bias model are plotted as a histogram for all structures in Figure 5, all litho-etch bias data referring to nominal litho conditions. The total error RMS is 1.3nm, with max. residual errors up to ~4nm. The tails of the residual-error histogram correspond to small pitch L/S structures at one side and EOL structures at the other. In a model-based EPC approach, the calibrated etch model is applied to convert the original design target into the litho-target, in a process that is similar to a normal OPC process. Figure 5 shows an example. The litho-target shapes appear now fragmented (indeed equivalent to an OPCed layer).

This example also shows how the etch proximity correction applied at e.g. corners or line-ends differs from the correction applied at straight-lines (where the correction is in fact close to the intended 7.5nm/edge bias). This directly underlines the difficulty of a rule-based etch correction approach to replicate the same shapes, and hence the usefulness of a model-based approach. The litho-target shapes that are the output of the EPC step, then become the input for the OPC step.

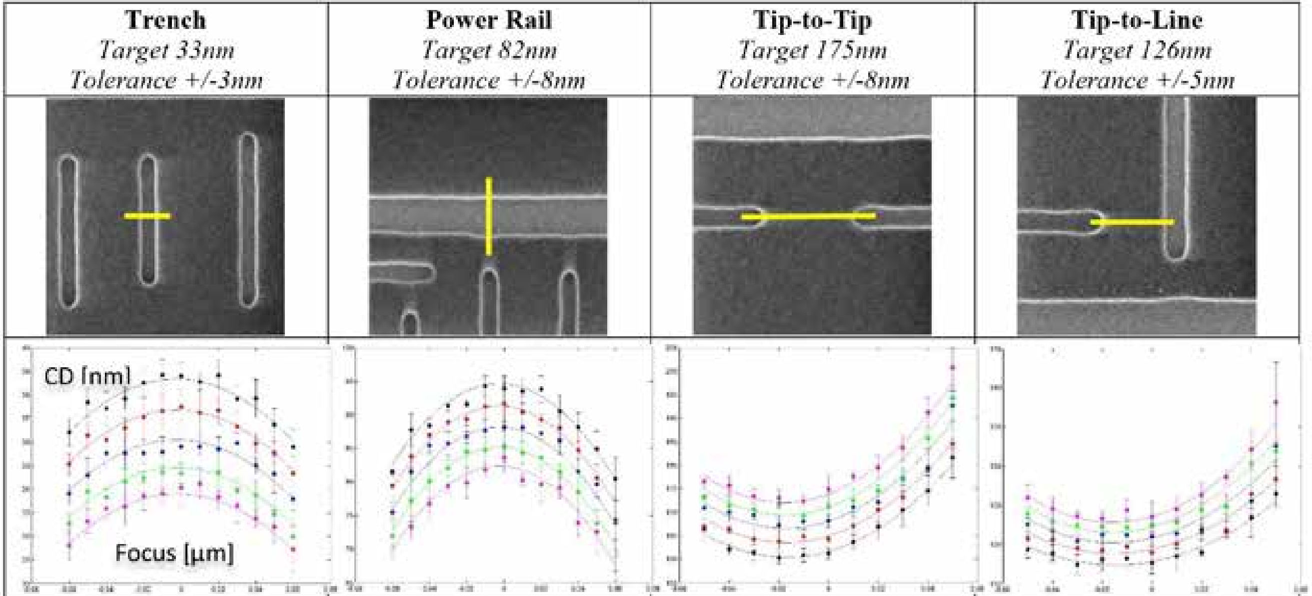
2.3 OPC and assist-placement options

Deciding on how to do the assist placement is one of the first decisions that need to be made in the OPC step, after having defined the new litho target in the EPC step. TESPA20 contains multiple OPC Logic block solutions, including different types of assist placement. We compared a rule-based assist-placement approach with several implementations of modelbased assist placement (from several EDA partners). Thus, we experimentally observed the Depth-of-Focus (DOF), that we obtained from many structures of the OPC blocks, in which the DOF of

Table 2. Selected structures for printability evaluation after-etch.

Structure types	Design Targets [nm]	Quantity
Trench: *width*	33	4
Power Rail: *width*	82	5
Tip-to-Tip: *gap size*	70/175/219/245	4
Tip-to-Line: *gap size*	70/126/128/184	12

Table 3. Individual CD-SEM (middle row) and Bossung measured after-etch (bottom row) for the four structure types with targets and tolerances (top row).



our rule-based assist solution was used, was larger than the DOF of the corresponding structures where a model-based assist placement was used. Illustration of this statement is clearly shown in Table 1, in which through-focus (in-resist, at litho) images from a M1 split1 example clip of two model-based solutions are compared with two rule-based assist placement solutions. Cases C and D (right columns) used essentially the same assist rule we generated, but in C the OPC engine was allowed to modify (and/or remove) assists from an assist printability check. In D, we did not allow this. Consequently, a number of important assists, marked in case D (green arrows/circles), are missing in most of the other solutions, particularly on the two model-based solutions A and B (left columns). As a result, the target features that are less supported by the missing assist show 'poor printability', in spite of the aggressiveness of the target features fragmentation in combination with discretized (almost gridded) assist placement (which comes at a cost for the mask shot count)

Although the assist-placement models used on TESPA20 may not have been entirely optimized, we believe that model-based assist placement faces two challenges:

- The model needs to decide where to place assists and decide how wide these assists will be. If either of these is not well chosen, the assists support the 'main features' less than what they could potential do (we will in fact return to assist model-based placement in section 4.2).
- The model needs to ensure that the assists will not print, throughout the intended PW as well as in the presence of mask errors. In our experience, the assist printing prediction is often overestimated by the model-based assistplacement engines. This results in small assist-widths or even assist removal, consequently leaving behind main structures that are not optimally 'supported'.

For a line- or trench-like patterns as our M1 application, making an assist rule is quite feasible. In view of observations as the ones shown in Figure 6 (for which, we are in variance with Reference 14), we decided to invest in a good assist rule, that would be based on both experimental data and rigorous simulation (S-Litho), and which would incorporate information on assist printing from printed wafers.

First of all, let's specify that an assist rule is essentially a table that tells how many assists, at which positions and with which width are to be placed in a certain space between two main features. The procedure, we used, to generate this ruletable

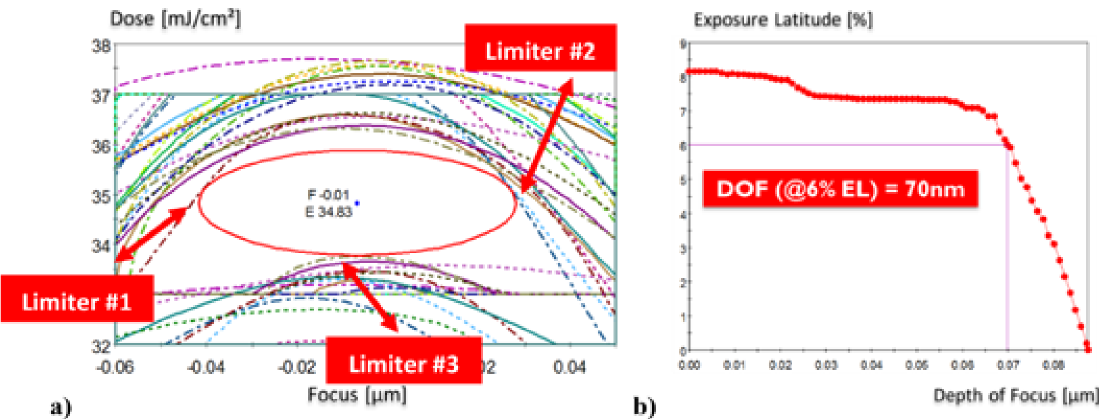


Figure 8. a) OPW obtained after superposition of all individual PW, including the elliptical shape (red circle); b) Exposure Latitude (EL) vs. DOF of the OPW.

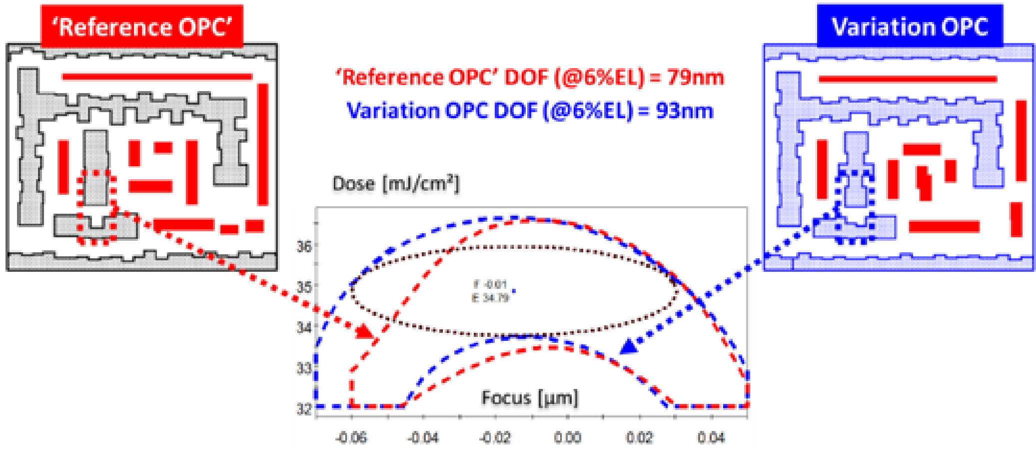


Figure 9. Measured PW performance after-etch compared between the 'reference OPC' case (left-hand side) to a 'variation OPC' (right-hand side, where the dotted-black circle gives the highest DOF associated to the best OPC solution (here the 'variation OPC' case).

is described in Figure 6. It consists of four steps:

1. As a first step, using a test mask containing many 'potential' assist-rule cases for 1D structures, we inspected a printed wafer at nominal litho conditions to filter-out (i.e. reject) 'clear' assist-printing cases. Figure 6.b illustrates this with the example of five 'starting cases', two of which are rejected in this first step. Additionally, we chose to keep cases, where there is only a 'faint' trace of assist printing, into the 'accepted' list, based on the observation that this type of assist printing was not transferred in the etch process.
2. Secondly, the non-printing assist candidates are simulated with rigorous S-Litho simulations (using a calibrated resist model) to 'rank' the remaining cases according to their DOF. Assist cases with a weaker predicted DOF would then be eliminated in a second filtering step (in the example of Figure 6.b, one of the three test rules would be eliminated).
3. Then the remaining assist candidates are inspected on wafer again, but this time through focus/dose/mask error. In this focus/dose/mask error inspection, we obviously look at the through-focus performance, but again check for assist non-printing, also at the most unfavorable combination of dose and mask error.
4. Finally, select the assist rule as the case that offers the best on-wafer performance.

A table of 20 assist rules has been defined in this way, covering a space range from 110nm up to 800nm.

Now let's see how those rules are transferred on real chip. Carefully looking at the assist arrangements on the OPC solutions in Figures 7.a and 7.b, shows us two interesting points (to be revisited in Section 4):

- *All long edges* (e.g. green circle) are supported by an assist (if the space is larger than the minimum space in our assistrule table). In such a case, application of the assist rules is fairly straightforward.

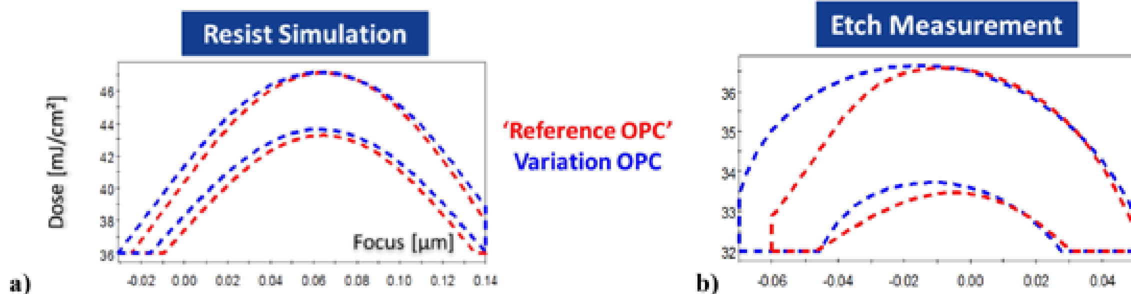


Figure 10. a) Rigorous simulation at litho of the two OPC solutions; b) Measured PW after-etch.

Table 4. S-Litho simulated 3D Views and cross-sections of the 'reference OPC' (top row) and the variation OPC (bottom row) through focus.

Negative Focus *Cross-Section / 3D View*	Best Focus *Cross-Section*	Positive Focus *Cross-Section / 3D View*

- *Complex space locations* (e.g. black circle) stress degrees of freedom for implementing the assist rules as the value of the space cannot be unambiguously defined. As a result, there are many possible assist-placement solutions that are all consistent with the rule. In section 4, we will see that such 'degenerate' solutions can still lead to significantly different PW performance and hence are not equivalent.

3. After-etch Printability Evaluation

3.1 Structure selection

The structure selection for measuring the OPW was based on a combination of both on-wafer inspection of the Logic blocks, both after-litho and after-etch, as well as standard OPC Verification checks (i.e. hot-spot, checking for a range of PW conditions). A more traditional approach would have been to reply on the results of the OPC verification only, but we chose to include also structures that were selected from a random on-wafer inspection, in case the OPC Verification had 'missed' hot spots. A total of 25 structures were eventually selected, representing four main categories, as shown in Table 2. Design targets are given for the selected structures: 33nm min. CD and 70nm min. gap size.

3.2 Individual Bossung measurements

From the selected structures, we measured individual Bossung curves from an etched wafer. In this study we limited ourselves to measurements on each of the M1 splits separately, so our OPW will not contain measurements between split1 (M1A) and split2 (M1B) structures (and hence will not be affected by M1A-M1B overlay errors). A total of 65 focus-doseconditions were measured per structure, with 15 intrafield measurements from identical structures (through scan and slit) to obtain sufficient measurement statistics. For each structure type, we list, in Table 3, the tolerances we (initially) applied for deducing the PW. The tolerances, we used, were defined as follows:

- For the trenches and power rails, the tolerance values equate to 10% of the target CD.
- However, for tip-to-line and tip-to-tip structures we used *absolute tolerance values*, and not a percentage of the targetgap CD: +/-5nm for tip-to-line, and +/-8nm for tip-to-tip cases. These values more or less reflect the tolerances that were assumed on the line-end placement when making the design rules for this metal layer: +/-5nm line-end EPE (Edge Placement Error) design-rule allowed.

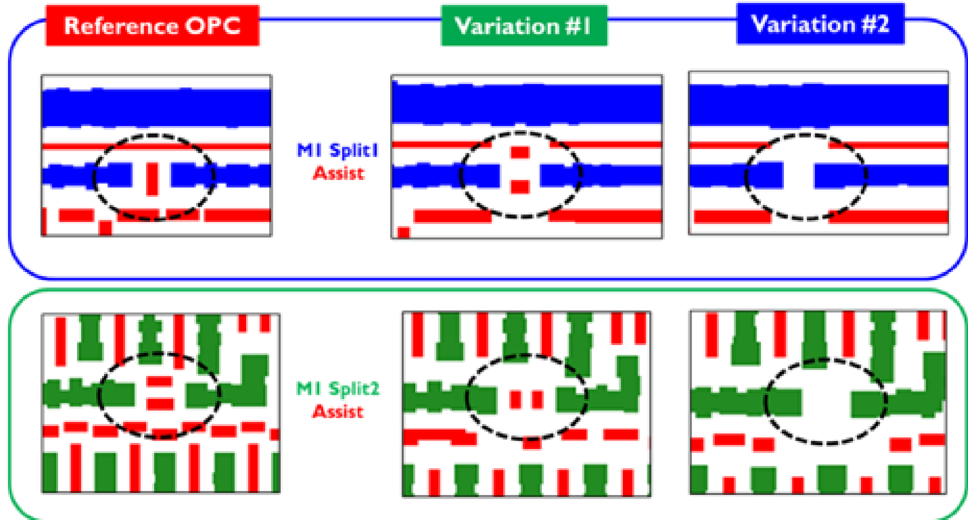


Figure 11. Two alternative OPC solutions compared to the 'reference OPC' for M1 split1 (top row, blue polygons), and M1 split2 (bottom row, green polygons) with different assist configurations (red polygons).

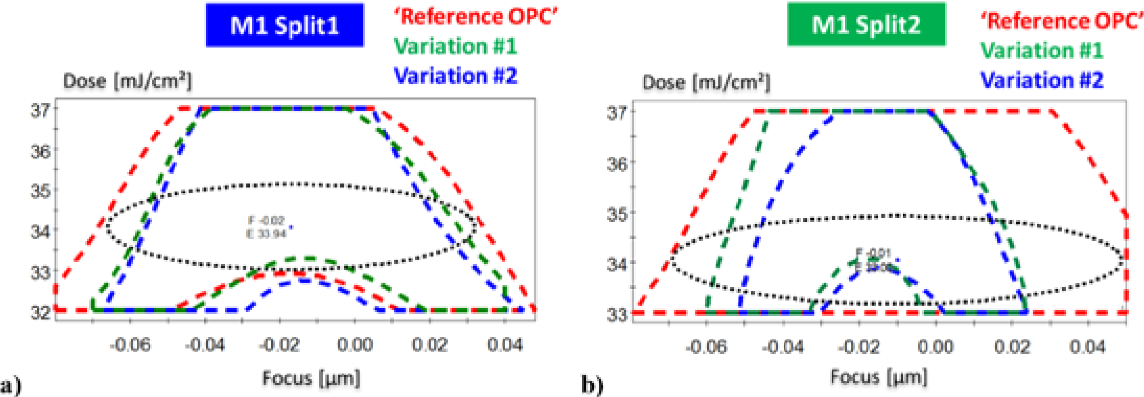


Figure 12. Measured PW performance of both M1 splits (after etch), respectively a) split1 and; b) split2, where the dotted-black circle gives the highest DOF associated to the OPC solution (here the 'reference OPC' case).

As a tip-to-tip type gap is subjected to line-end pull-back on both sides, we gave it a larger CD tolerance, whereas the tip-to-line only sees line end pull-back on one side. Although these tolerances seemed like a logical choice, we shall see in Section 4.3 that this is actually not correct for tip-to-line structures in case of a gap size, that is close to the design-rule limit.

3.3 Overlapping Process Window (OPW) after Etch

In Figure 8, we start the OPW discussion by showing an OPW example in which the 25 measured structures that are used in it all belong to one OPC variation. We will call it the 'reference OPC' case. The OPW DOF we obtained for this case, is 70nm at 6% Exposure Latitude (EL). In Figure 8.a, we highlight in red the immediate OPW limiting structures. Question now is what these limiting structures are, whether we can understand these limitations, and whether we can get a better OPW performance by 'improving' the printing performance of these structures. For this reason, we also measured the individual PWs for a number of these structures from other OPC variations that are available on our test mask. In section 4, we will take a closer look at these limiting structures, one by one, and see whether some of the available OPC alternatives could lead to an improved performance.

4. Overlapping Process Window Limiting Structures

4.1 Limiter #1: Resist 3D Effects

The limiter #1 constrains the negative focus side of the measured OPW. It corresponds to a tip-to-line structure (split1), part of the 'reference OPC' block case (red dashed rectangle in Figure 9). An alternative solution, referred to as 'variation OPC', is also shown and was measured as well. Comparing the PW performance between the two solutions reveals a stronger printability robustness of the alternative OPC solution over the 'reference OPC'. At the positive focus-side, the measured PW performances match well, but the 'reference OPC' is less performing at the negative focus side: the DOF gain obtained

Table 5. Simulated after-litho DOF (using S-Litho) and measured after-etch DOF at the three OPC solutions for limiter #2 only, M1 split1.

OPC solutions	Simulated after-litho DOF *at 6% EL [nm]*	Measured after-etch DOF *at 6% EL [nm]*
'Reference OPC'	120	103
'Variation OPC' #1	95	80
'Variation OPC' #2	98	82

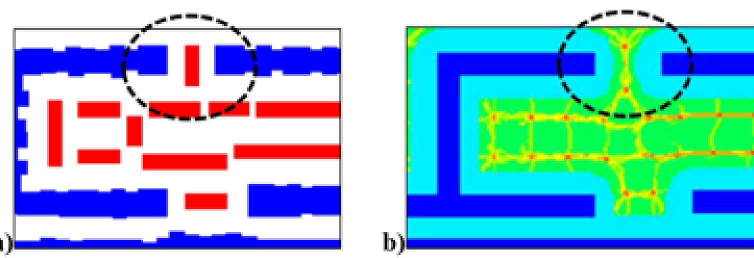


Figure 13. a) 'Reference OPC' including OPCed layer (blue polygons) and assist features (red polygons); b) Gradient map overlapped to the target features, red/yellow areas indicate the preferential position sites to place assist, whereas the light blue areas surrounding the target features represent 'no assist's lands'.

from the alternative OPC of 14nm is in fact quite significant, even though the fragmentation of the polygons (for the tip-to-line structure of interest) seems to differ only slightly. Do we understand the observed limitation?

To answer to that question, we decided to first look at the in-resist behavior of those two solutions. For that purpose, we used a rigorous simulator (S-Litho) with a calibrated NTD resist model[11], to simulate the PW at litho. We found that the after-litho PWs are quasi identical, see Figure 10.a. In contrast, the PW performance measured after-etch significantly differs on the two following points:

- Drop in PW robustness at the negative focus side.
- Best focus changes (caused by this after-etch PW asymmetry) between the two cases of about 10nm.

We have not actually measured the after-litho PWs for these two OPC solutions (yet), but if the S-Litho predicted PWs are correct, the difference between these two solutions emerges during the etch step! Can the S-Litho simulation help us to understand this?

Table 4 shows the simulated 3D views and resist cross-sections of the 'reference OPC' (top row) and the 'variation OPC' (bottom row) through focus, as simulated by S-Litho. The cross-sections are taken along the cutline (black dash line), and the tip-to-line structure of interest is encircled (black dash circle). As we are dealing with trench printing, the EOL 'gap' actually corresponds to a resist 'bridge' (red solid). It is clear that the change of the resist profile is quite dramatic through focus, and even more if looking at different (horizontal) planes in the resist itself. Such quantities are reported in[11], for the same 20nm Logic node test vehicle. This leads to the hypothesis that the limiter #1, associated to the tip-to-line structure, could be the consequence of the resist-profile, i.e. R3D effects. Reference 11 looks more in detail for this particular structure and comes to the same conclusion. Following this assumption, if the resist profiles obtained with the alternative OPC solution are different from the ones obtained with the 'reference OPC', the etch process might well behave differently on both cases, leading to the observed after-etch PWs. In the absence of experimental resist profiles for these exact structures, this hypothesis cannot be proven, but we think it is the most likely explanation of the PW asymmetry observed in Figure 10.b. Conventional OPC engines (using compact models) approximate calculations by working on one single plane in the resist stack (2D x-y plane), for computational time reasons, and hence do not have any knowledge of resist profiles. This single-plane approximation is reasonable as long as the sidewall angle of the resist remains close to 90°. As soon as we deviate from those conditions, the results of the etching process could be seriously affected and vary significantly with changes in the resist profile. If this explanation of our observed after-etch PWs for this case is correct, it logically stresses the need to account for 3D resist profile in the OPC flow. Demonstration of such capability is of great need and is currently a challenge for EDAs.

4.2 Limiter #2: Assist Solutions

Limiter #2 constrains the positive focus side of the measured after-etch OPW (Figure 8.a). It corresponds to a tip-to-tip structure (split1), a different EOL type than limiter #1. The limiting structure is viewed on the top row of Figure 11, highlighted with a black circle. Next to it, we show two alternative OPC solutions of the same structure. Looking at those structures, and observing that the assist-placement in the gap is different, it

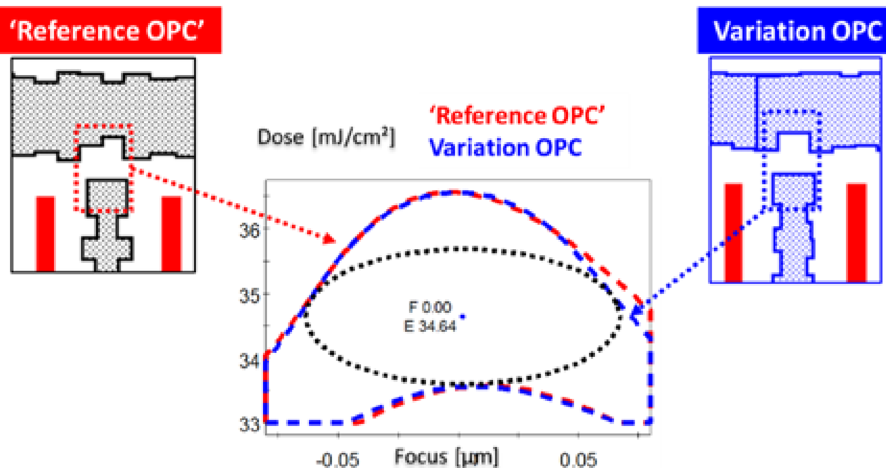


Figure 14. Measured PW performance after-etch compared between the 'reference OPC' (left-hand side) case to a variation OPC (right-hand side).

appears reasonable to assume that limiter #2 is related to assist solutions. Depending on the available gap size, assists or SRAF (Sub-Resolution Assist Feature) are inserted based on the rules we made, in order to support the two line-ends through PW. In discussing our assist-placement rule in section 2.3, we already pointed out that our rule allows different solutions in more complex configurations, i.e. when the determination of the space-width can be done in different ways (also default prioritizations on how space-widths are meshed and mapped from the algorithm placement tool can add extra variations).

On the bottom row of Figure 11, we add the second immediate OPW limiting structure. It is another tip-to-tip structure (from split2) for which different OPC solutions have found a different assist-placement. In order to see whether these different solutions offer a similar performance or not, we measured the PW of these two cases, and compared it to the PW of the two alternative OPC solutions (variation #1 and variation #2).

These measured PWs are shown in Figure 12, shown for both M1 splits and the three OPC solutions. The measurements clearly show that the two alternative assist configurations do not improve the PW performance, and even get worse when going from an alternative-assist configuration in OPC variation #1 to a no-assist configuration in OPC variation #2. The assist configuration in the 'reference OPC' case outperforms the alternative ones in both examples, with the largest DOF (at 6% EL): 103nm for split1 and >125nm for split2. So, although the alternative assist-placement examples have not provided us with a larger PW (and hence limiter #2 remains a limiter to our OPW), this comparison does show that placing assists around line-ends needs to be done carefully: even though all cases we tried are consistent with our basic assist rule (in which assist placement in EOL gaps was not separately specified), the DOF we obtain can be quite different. Consequently it would be useful to know if the rule could be refined to direct us immediately to the optimum solution.

Can simulations confirm this performance difference between the three assist-placement solutions shown in Figure 12? Rigorous resist simulations (S-Litho) indeed confirm that the best DOF performance should be expected for the assist configuration of the 'reference OPC', as we show in Table 5, where we list the DOF at 6% EL obtained from the simulation next to the measured values. The simulated DOF values are calculated at litho level, whereas the measured ones are afteretch, so the absolute values should not be expected to agree, but the trends do. Moreover, the DOF extracted from OPC Verifications after-litho is the same as the one reported on rigorous simulation for the 'reference OPC' case, i.e. 120nm. Confirming the best assist-placement case through simulations is helpful, but it would even be more helpful if we had a way of predicting the best-assist solution right away. So let us return to a model-based assist placement approach.

As an intermediate step in generating model-based assist-placement, MentorGraphics uses what they call a 'gradient map'.[14] An example is shown in Figure 13.b. Without going into detail on how this is done, this gradient map is derived directly from the litho target layer and identifies the preferential assist position, as red/yellow areas around the target structures. (The light blue areas surrounding the target features delimit a 'no-assist's land' where no assists are even considered.) Note that this map only gives directions for the *position* of the assists, but no *assist width* information. If we 'overlay' this gradient map with our own assist solution cases, generated from the rules, (i.e. compare Figure 11 and 13.b), the gradient map supports the 'reference OPC' solution as the better one. The assist configuration of the 'reference OPC' structure (encircled) nicely agrees with the information given by the gradient map, suggesting to place one vertical assist and not two horizontal ones or no assist at all. The attentive reader will notice that the gradient map still leaves some degree of freedom on how exactly to insert the SRAFs. The example of Figure 13 shows that parts of the model-based assist placement tools should potentially be helpful for e.g. improving assist-placement rules, but in this paper we will not explore this topic any further.

4.3 Limiter #3: CD Metrics & Tolerances

Lastly, the limiter #3 constrains the low middle area of the OPW (Figure 8.a). It corresponds to a tip-to-line structure (split1)

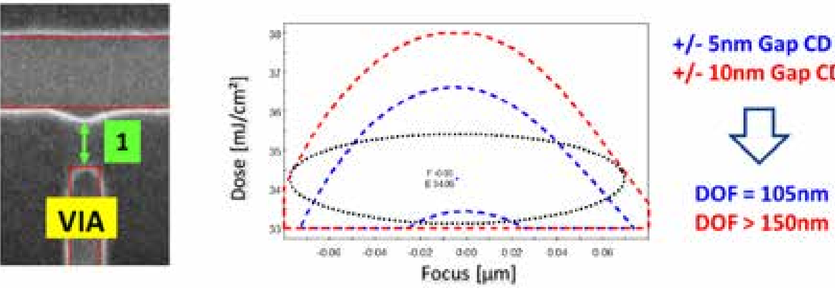


Figure 15. CD minimum gap distance detector used to flag 'shorts' (bridge hot-spot), where PW performance is being compared for two different thresholds: +/-5nm (in blue) and +/-10nm (in red).

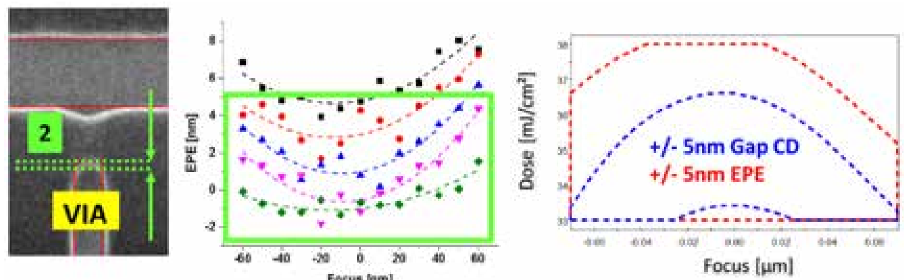


Figure 16. EPE (extracted contour from CD-SEM picture) detector to flag 'poor' overlap with Via (contact layer). The EPE Bossung distribution is plotted in the center The Bossung extracted from the EPE measurement is compared to the min. CD distance with same absolute tolerances (cartoon on the right): the EPE DOF is significantly larger.

that differs from the limiter #1 (see Figures 14 to 16): the tip is facing a power rail at the minimum gap allowed by the design rule (in our case 70nm). Again, we tried an alternative solution ('variation OPC') to compare to the 'reference OPC' case. Figure 14 shows the measured PW performance of the gap CD between the tip and line. We find that the result is almost identical for the two OPC solutions. Looking at the simulated PW performance after litho, we also find that the two OPC solutions perform the same. So it would seem that this type of structure is a genuine PW limiter.

However, if we go back to a CD-SEM image example of this structure (see e.g. Figure 15 on the left-hand side) it is apparent that we should question the tight CD tolerance (of +/-5nm) that was used in generating the PWs of Figure 14. It seems more meaningful to in fact consider two separate metrics for this type of structure, each with their own tolerance value, that are associated with the two hot-spot types that might occur here:

1. *Bridging hot-spot,* appearing when two patterns merge (hard-bridge) or get close (soft-bridge) to each other, leading to a risk for a short, a leak or a reliability issue.
2. *Pullback of the line end hot spot,* leading to a risk that the line will not connect well to the Via that it needs to contact (see Figure 15).

It seems therefore more suitable to define two separate metrics for this type of structure:

1. *Tip-to-Line gap CD bridge detector.* This CD-gap metric remains very meaningful but the tolerance of +/-5nm we used so far seems unnecessary tight if we only want to use it for detecting potential bridges or shorts. After all, if we would have printed the tip and line in different splits, we would have accepted resulting gap dimensions of the order of ~35 nm. If we therefore relax the gap-tolerance to +/-10nm, we see that the DOF dramatically enlarges from 105nm (at 6% EL) to >150nm (Figure 15). With this revised tolerance, the Gap CD PW will not limit the OPW anymore.
2. *Line-end pullback detector,* i.e. EPE of the line-end, to flag 'poor' overlap with a Via located near the line end. This metric cannot be directly measured by CD-SEM, as it corresponds to the distance from the printed edge to the *design target*. But it can be extracted from saved SEM-images using *contour-based metrology.*[16-17] Doing so for the case of Limiter #3, we obtained an EPE Bossung, shown in Figure 16, where we have used a threshold of +/-5nm (in agreement with the DR that was used to generate the line-end of M1, as explained in sub-section 3.2). The >150nm DOF we obtain with the EPE metric is much larger than the original 105nm DOF with the min. CD distance combined with a +/-5nm tolerance.

With these revised metrics and tolerances, these tight tip-to-line structures do not constitute an OPW limiter anymore.

4.4 More potential Limiters: Mask 3D Effects

Back in sub-section 4.1, we mentioned best-focus differences that were observed between the two OPC solutions, which we

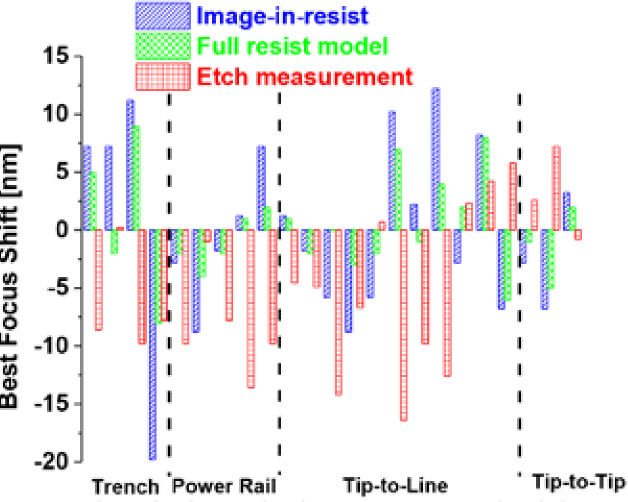


Figure 17. Best focus shift plotted against trench, power rail, tip-to-line and tip-to-tip structures, determined from image-in-resist (in blue) & full-resist model (in green) simulations, as well as from after-etch measurements (in red).

attributed to R3D-etch effects. Looking again at the OPW plot of Figure 8.a one can see that many structures seem to have a slightly best focuses, with respect to the OPW best focus. One potential reason for this could be Mask 3D (M3D) effects.

In order to (partially) answer the question whether M3D induced best focus shifts limit the OPW of our test chip, we again used a rigorous simulator (S-Litho) with a calibrated NTD resist model, to extract the individual best focuses per structure from Image-in-Resist simulations and from Full-Resists model simulations, for the structures of our OPW. Figure 17 shows the results of these simulations, as well as the best-focus values from our after-etch Bossung measurements. We observe that:

- *From Image-in-Resist simulation to full-resist model simulation,* the best-focus shift sign matches, and the amplitude is higher for the Image-in-Resist one for most cases.
- *From resist-model simulation to after-etch measurement,* the best-focus shift sign is sometimes opposite, and the amplitude varies from case to case. In the absence of experimental resist data for these exact structures, it is difficult to prove any statement on whether these differences are 'real'. We plan to look into this in further work.

To sum it up, M3D induced best-focus shifts do exist in our application examples, their absolute values being in the 5 to 10nm range. Of course, not every best-focus shift will necessarily affect the OPW: for a structure with a large individual DOF a best focus shift would have little to no consequences for the OPW. To what extent the OPW of our test vehicle is limited by M3D induced best-focus shifts is not clear at this point. This too will be a topic for further study.

5. Summary & Conclusions

It is common in the literature to separately report on the mechanism types limiting the OPW, considering only the afterlitho printability as final step for evaluating the PW performance. In our patterning study for M1 at N20, we measured the *OPW after-etch,* obtained from a selection of (mostly 2D) structures taken from a logic test block. The mask we used in this study was generated from a calibrated (PW) model for OPC, i.e. for the litho step, as well as a calibrated model (at nominal litho conditions only) for EPC (Etch Proximity Corrections), i.e. for the etch step. We thus accounted for full-*Patterning Proximity Effects,* enabling true PPC[20-22] (Process Proximity Corrections), which is more than necessary in the perspective of multiple patterning techniques to be used for the advanced Logic nodes. Next to OPC (or now PPC), we decided to invest in a good *assist rule methodology* (including placement and width info, i.e. an assist-table rules), that was based on both experimental data and rigorous simulation.

From the many potential OPW limiting mechanisms that have been reported in the literature, we identified contributions from the following four types:

- Mask 3D effects[8-10] (M3D): Attributed to the mask topography, the on-wafer effects are observed as best focus shifts between structures or tilt (distortion) of the Bossung shapes. Even though we were not able (yet) to determine whether these M3D-induced focus shift limit the OPW of our particular logic test vehicle (due to currently missing after-litho Bossung data), it is clear that at least the magnitude of the observed focus-shifts is large enough to potentially do so (see section 4.4).
- Resist 3D effects[11-12] (R3D): Differences in resist profiles (e.g. between different structures or through PW) can affect the actual litho-etch bias, as also reported in Reference 11. In our investigation, we did conclude that the limiter #1 tip-to-line structure is hypothetically R3D sensitive (see section 4.1). This interpretation was inspired

by the observation of a PW asymmetry (i.e. deviation at one defocus side) between two structures that had received a different OPC. In the absence of experimental resist profiles for these exact structures we cannot really prove this hypothesis, but we think it is the most likely explanation of the PW asymmetry. Accounting for resist profile contributions into the calibration of a compact resist model (for full-chip application) represents the actual challenge that EDAs are facing.

- OPC and assist options[13-15]: We included several End-of-Line (EOL) structures in our OPW evaluation, and for the larger EOL gaps, we showed (section 4.2) the importance of the assist-placement in or around the gap. This demonstrates that – if one wants to use rule-based assist placement – the rule would need to specify how to do this.

We found the model-based assist placement cases we tested to be less effective than the (best) rule-based cases, primarily because models for assist placement often seem to 'overestimate' assist printability, resulting in small assist widths or absence of assists altogether. We have however also shown an example where a model-based assist placement tool could potentially be helpful for e.g. validating or improving assist-placement rules generation in a more automatic and faster way.

- CD metrics and tolerances[16-18]: The case of the tip-to-line limiter structure of section 4.3 shows that a careful consideration of which metrics and tolerances should be used for determining the OPW is also essential and needs to reflect the actual requirements of the device, as a non-suitable choice may either lead to a too optimistic or too pessimistic OPW evaluation. In the example we showed, the individual PWs associated with these gaps were in fact improved by the reconsideration of the metrics/tolerances used.

The attentive reader could claim we missed other potential contributors in our M1 patterning study, such as mask errors,[23] residual OPC-model errors,[9] or overlay contributions.[17] Indeed, those topics were not covered in our investigation but of course are also potential contributors indeed. For example, Reference 17 reported on the same 20nm Logic node test vehicle, in which a new measurement methodology based on contour metrology was developed to quantify line-end pattern shapes and pattern placement errors. This contour-metrology method should provide useful information (pattern placement errors and line-end shapes), and could potentially be integrated in the work that was presented in this paper.

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Industry Briefs

2013: A Year in Review — Semiconductor Equipment and Materials Market and Outlook

Lara Chamness

2013 was a record year in terms of semiconductor device revenues; the industry finally exceeded the long elusive $300 billion mark, registering almost 5 percent growth according to the SIA. While 2013 was a growth year for the chip industry, it was the second consecutive year of declining revenues for both semiconductor equipment and materials.

Worldwide sales of semiconductor manufacturing equipment totaled $31.6 billion in 2013, representing a year-over-year decrease of 14 percent and spending on par with 2005 levels. 2013 saw contractions in all major categories, Wafer Processing equipment contracted 11 percent, while Assembly and Packaging and Test equipment contracted 26 and 24 percent, respectively. The Other Front-end segment (Other Front End includes Wafer Manufacturing, Mask/Reticle, and Fab Facilities equipment) contracted 34 percent.

Analysts predict mid- to high single-digit growth for the semiconductor device market for 2014. Initial data for silicon shipments and semiconductor equipment are proving to be encouraging. Given growth expectations for the device market, it is projected that the semiconductor materials market will increase 2 percent this year. Given two consecutive years of double-digit decline, the outlook for semiconductor equipment is much more optimistic with current expectations positive with spending potentially growing 20 percent or more.

SEMI Reports 2013 Semiconductor Photomask Sales of $3.1B

Mask sales are forecasted to reach $3.3B in 2015. After contracting 3% in 2012, the photomask market increased 1% in 2013. It is expected to grow 3% sequentially over the next two years. Key drivers continue to be advanced technology feature sizes (<45 nm) and increased manufacturing in Asia-Pacific. Taiwan remains the largest photomask regional market for the fourth year in a row and is expected to be the largest for the duration of the forecast. Revenues of $3.1B place photomasks at 14% of the total wafer fabrication materials market, behind silicon and semiconductor gases. By comparison, photomasks represented 18 percent of the total wafer fabrication materials in 2003.

Another trend highlighted in the report is the emerging importance of captive mask shops. Aided by intense capital expenditures in 2011 and 2012 and a weakening Yen in 2013, they gained market share at merchant suppliers' expense, with captive mask suppliers accounting for 49 percent of the total photomask market last year, up from 42 percent in 2012. Captive mask shops represented 31 percent of the photomask market in 2003.

Intel Reveals Financial Black Hole Called Mobile

Peter Clark

Intel reports net income of $1.9B on sales revenue of $12.8B in the quarter in 2013. Sales came in at the mid-point of guidance reflecting a 7.7% sequential decline and an 1.5% increase compared with Q1'13. However, income was down 4.8% year-on-year. Intel reveals that while the PC business remains responsible for more than half of Intel's sales revenue and continues to be highly profitable, it continues to shrink. It also reveals that mobile and communications group made a loss of $3.15B in 2013 on sales of $1.375B.

"In the first quarter we saw solid growth in the data center […] and we shipped 5 million tablet processors, making strong progress on our goal of 40 million tablets for 2014," said Intel CEO Brian Krzanich. "Additionally, we demonstrated our further commitment to grow in the enterprise with a strategic technology and business collaboration with Cloudera, we introduced our second-generation LTE platform with CAT6 […] and we shipped our first Quark products for the Internet of Things."

In the first quarter of 2014, PC Client Group made of profit of $2.8 billion on sales revenue of $7.9 billion, down 1 percent year-over-year. The Data Center Group made profit of $1.3 billion on revenue of $3.1 billion that was up 11 percent year-over-year. The newly-formed Internet of Things Group made a profit of $123 million on sales of $482 million, up 32 percent year-over-year.

Join the premier professional organization for mask makers and mask users!

About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

Individual Membership Benefits include:

- Subscription to BACUS News (monthly)
- Eligibility to hold office on BACUS Steering Committee

www.spie.org/bacushome

Corporate Membership Benefits include:

- 3-10 Voting Members in the SPIE General Membership, depending on tier level
- Subscription to BACUS News (monthly)
- One online SPIE Journal Subscription
- Listed as a Corporate Member in the BACUS Monthly Newsletter

www.spie.org/bacushome

Calendar

2014

SPIE Photomask Technology

Co-located with
SPIE Scanning Microscopies

16-18 September 2014
Monterey Marriott and
Monterey Conference Center
Monterey, California, USA
www.spie.org/pm

SPIE Scanning Microscopies

Co-located with
SPIE Photomask Technology

16-18 September 2014
Monterey Marriott and
Monterey Conference Center
Monterey, California, USA
www.spie.org/sg

2015

SPIE Advanced Lithography
22-26 February 2015
San Jose Convention Center
and San Jose Marriott
San Jose, California, USA
www.spie.org/al

SPIE is the international society for optics and photonics, a not-for-profit organization founded in 1955 to advance light-based technologies. The Society serves nearly 225,000 constituents from approximately 150 countries, offering conferences, continuing education, books, journals, and a digital library in support of interdisciplinary information exchange, professional growth, and patent precedent. SPIE provided over $3.2 million in support of education and outreach programs in 2013.

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You are invited to submit events of interest for this calendar. Please send to lindad@spie.org; alternatively, email or fax to SPIE.