PHOTOMASK

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Invited Paper - AL13

The impact of 14-nm photomask uncertainties on computational lithography solutions

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ABSTRACT

Computational lithography solutions rely upon accurate process models to faithfully represent the imaging system output for a defined set of process and design inputs. These models, which must balance accuracy demands with simulation runtime boundary conditions, rely upon the accurate representation of multiple parameters associated with the scanner and the photomask. While certain system input variables, such as scanner numerical aperture, can be empirically tuned to wafer CD data over a small range around the presumed set point, it can be dangerous to do so since CD errors can alias across multiple input variables.

Therefore, many input variables for simulation are based upon designed or recipe-requested values or independent measurements. It is known, however, that certain measurement methodologies, while precise, can have significant inaccuracies. Additionally, there are known errors associated with the representation of certain system parameters. With shrinking total CD control budgets, appropriate accounting for all sources of error becomes more important, and the cumulative consequence of input errors to the computational lithography model can become significant. In this work, we examine with a simulation sensitivity study, the impact of errors in the representation of photomask properties including CD bias, corner rounding, refractive index, thickness, and sidewall angle. The factors that are most critical to be accurately represented in the model are cataloged. CD Bias values are based on state of

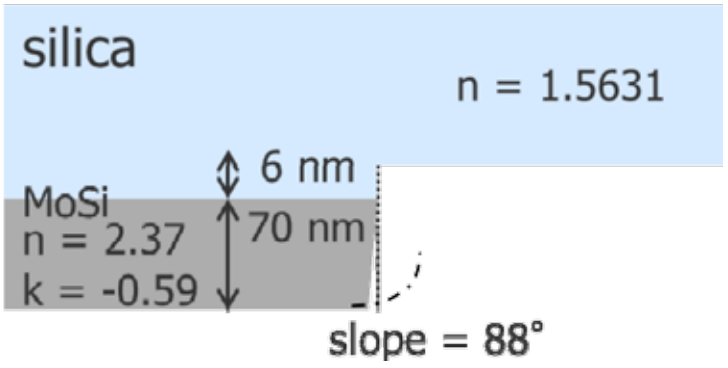

Figure 1. Schematic diagram of attenuated PSM mask stack representation in simulator. Baseline assumptions as shown result in 5.8% transmission and 179.6 degree phase.

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EDITORIAL

Intaglio

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The family of printing and printmaking techniques in which the image is incised into the surface and the incised line or sunken area holds the ink.

Some History

A recent exhibit at the de Young Museum in San Francisco had a generous selection of etchings by Rembrandt. What does this have to do with mask making? Just as the Rubylith® process gave way to the e-beam patterning and etching, so did the printmaking technique of engraving give way to etching. It was simpler. Remember as we try to figure out the method to make that single digit nanometer defect free mask, we are carrying on in the tradition of Rembrandt.

Some Future

Extreme ultraviolet (EUV) lithography has missed the initial stages of the 10nm logic and 1xnm NAND flash nodes.

Chipmakers hope to insert EUV by the latter stages of 10nm or by 7nm, but vendors are not counting on EUV in the near term and are preparing their back-up plans. Barring a breakthrough with EUV or other technology, IC makers will likely use today's 193nm immersion with multiple patterning at 14nm, 10nm and perhaps beyond.

Chipmakers are keeping their options open for good reason—extending optical comes with a penalty. The shift from single patterning at 28nm to multiple patterning at 20nm is projected to increase lithography costs by up to 56%, according to Barclays Capital. Consequently, the shrinking strategy riding on the overall cost-per-transistor curve is in danger of slowing or derailing.

Lithographers, who seem to achieve miracles when the chips are scaled down, are determined to stay on Moore's Law. The ability to stay on the critical cost-per-transistor curve puts enormous pressure on the lithographic supply chain, which includes the EDA houses, materials suppliers, mask shops, and tool vendors. Lithographers also may resort to some new patterning tricks. The wild card is directed self-assembly (DSA), an alternative lithography technology that makes use of block copolymers to enable fine pitches.

NGL woes

The thinking is that optical lithography would run out of gas, prompting the need for a next-generation lithography (NGL). EUV emerged as the leading NGL candidate. The other NGLs, maskless and nanoimprint, are also in the hunt.

Some are targeting EUV for mass production in 2014, but the industry isn't taking any chances and will extend 193nm immersion—at a price.

Lithography steps and costs will soar at 14nm and beyond. In response, chipmakers already are prepared for the dreaded multiple patterning era.

Another technology, DSA, potentially could extend 193nm lithography beyond 10nm. As before, the challenges for DSA are defects and the lack of a design infrastructure. The new gap for DSA is non-destructive metrology as a means to inspect the morphologies in the patterns.

DSA materials providers have said DSA would be ready at 10nm, but there are signs the technology may get pushed out.

Some solutions

Until NGL is ready, chipmakers are stuck. Customers are even looking at extending immersion beyond 10nm. To keep up with the increase in multiple patterning steps, ASML and Nikon are shipping faster scanners.

Besides lithography scanners, there is an urgent need for new and faster e-beams

(continues on page 10)

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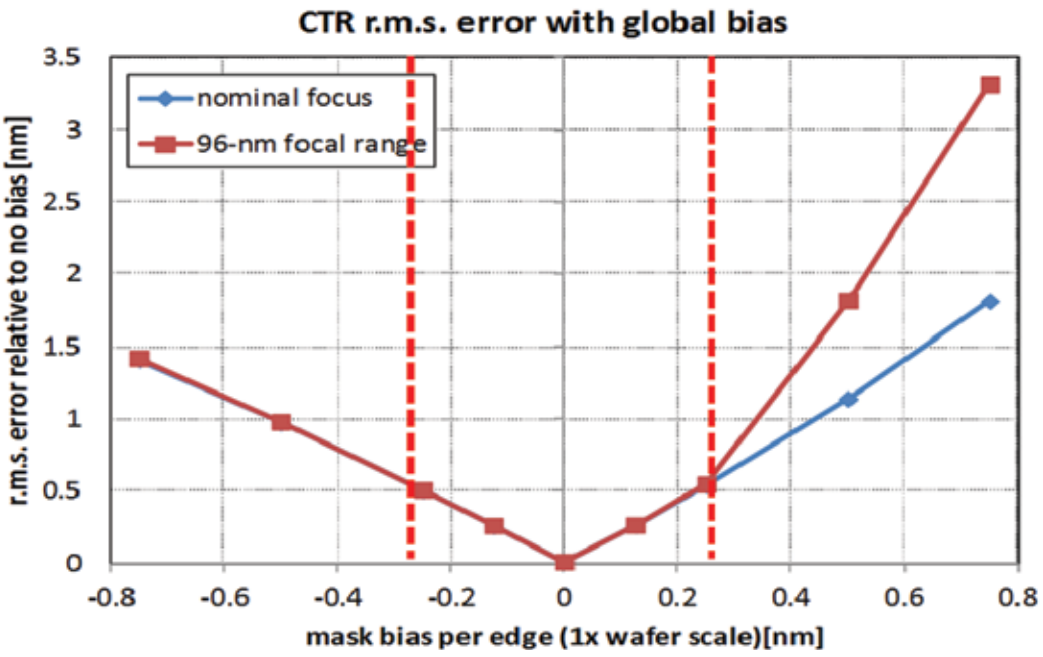

Figure 2. CTR RMS error relative to no bias for global mask bias as shown. The ITRS specification corresponds to 0.25 nm per mask edge.

Table 1. 2012 ITRS Mask specifications for CD, transmission, and phase control.

	Specification
Mean CD Error	2.0 nm
CD Linearity	4.0 nm
L/S CDU	1.5 nm 3σ
CH CDU	0.8 nm 3σ
attPSM Mean transmission	4%
attPSM transmission uniformity	3%
attPSM Mean phase	3 degrees
attPSM phase uniformity	3 degrees

the art mask manufacturing data and other variables changes are speculated, highlighting the need for improved metrology and awareness.

INTRODUCTION

Models for OPC and post-OPC verification describe the entire patterning process, including mask, optics, resist, and etch, as a set of mostly separately characterized modules. These modules are represented by a variety of parameters, some of which are supplied as user known input values, and others are empirically tuned during the calibration process. The tuning is typically done by iteratively varying parameter values, and minimizing the errors between the model prediction and experimentally determined photoresist or postetch critical dimensions (CD) determined from a CD-SEM tool.

The parameters associated with the calibration of the mask, optical, resist and etch processes can be sorted into three classes. There are parameters associated with software options for altering the approximations used in the model, such as the nature of the mask representation, the number of optical kernels, or optical diameter, and the form of the resist or etch model. A second class of parameters are those associated with physical phenomena, where direct measurement is not done, but rather the model contains mathematical proxies for the parameters. These parameters are most often associated with the complex photoresist bake, develop, and etch chemical kinetics. A final class of calibration options includes directly measurable or known as designed-in values. These for the most part are associated with the mask and optical system and would include mask film stack thickness and refractive indices, wavelength, numerical aperture (NA), illumination profile, and wafer and resist film stack optical constants. It is extremely important to note, however, that there can be inaccuracies associated with these known or measured parameters, and the

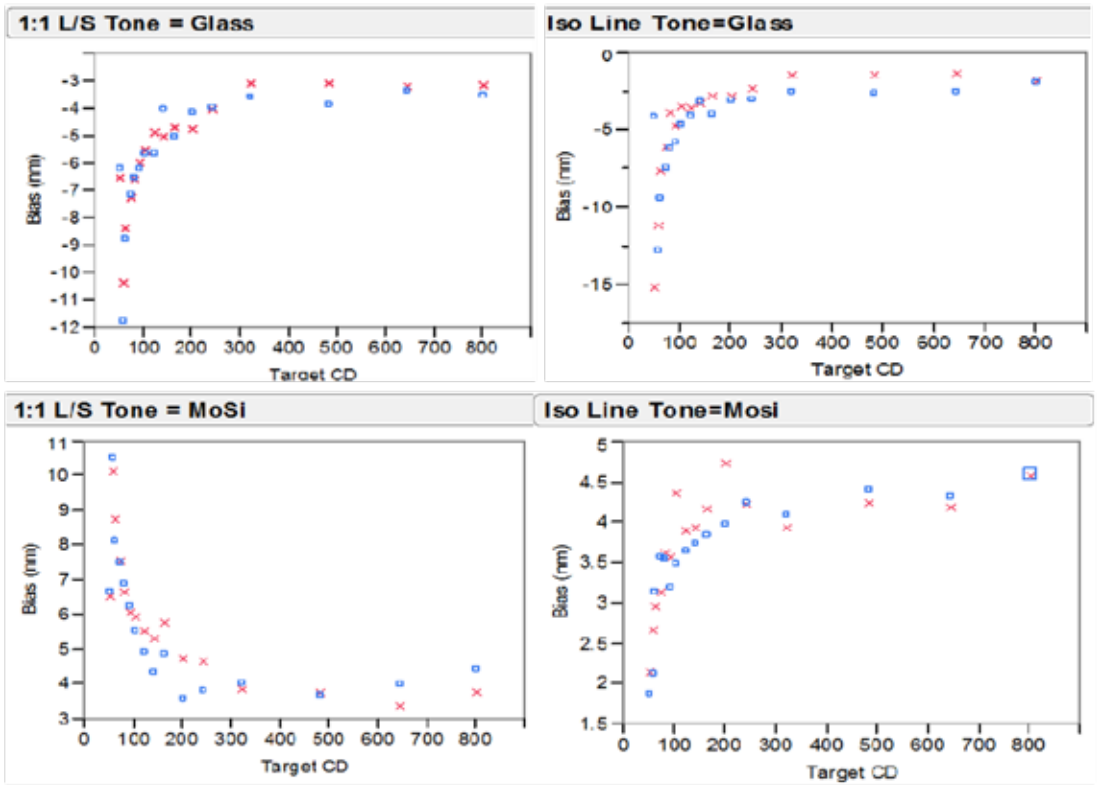

Figure 3. Mask CD bias (actual-target) 4X for four different pattern types and both horizontal and vertical orientations.

impact of errors or uncertainties associated with the physical mask on 14 nm OPC models is part of the focus of this paper.

Historically, OPC models have been calibrated based upon an assumed exact two dimensional match of the physical test mask and the test pattern layouts representing those patterns. However it is known that systematic proximity effects such as corner rounding and isolated-to-dense bias are manifested in the mask patterning process. Because the mask manufacturing process is usually invariant for the life of the wafer technology, it has been acceptable in the past to ignore these distortions and effectively lump the systematic mask proximity effects into the grey box resist process model. This implies, however, that any substantial change to the mask process will require the OPC model to be recalibrated. More significantly, the OPC model incorrectly ascribes mask behavior to the photoresist model, which will necessarily limit the predictive capability of the model to some extent. Recent work on mask process proximity modeling is enabling a departure from this paradigm.[1-2] This work involves calibrating a mask process model (MP) based on mask CD or contour measurements, then referencing the MP model to describe the mask input to the wafer OPC calibration flow. More than a 50% reduction in mask CD variability can be realized with this approach, and the impact on wafer OPC model accuracy will be explored in this work.

The attempted introduction of alternating phase shift masking (PSM) technology into manufacturing as early as the 350-nm node for I-Line lithography[3] and 130-nm node for KrF lithography[4] raised awareness of the impact of mask topography on wafer lithography. Ultimately this aggressive PSM approach was replaced with more manufacturable solutions, including attenuated-PSM, which eliminated etched quartz in favor of a thin, partially absorbing layer. The Kirchhoff, or flat mask approximation, has been employed extensively, where it is assumed that the mask is sufficiently thin that the diffracted light can be computed by means of scalar or vector diffraction theory. This is in contrast to rigorous 3D electromagnetic field (EMF) simulation, which accounts explicitly for the topography and refractive indices of the mask materials, and solves Maxwell's equations in 3D, a highly computation-intensive operation not suitable for full-chip scale. There are a variety of different approximation methods that have been offered to enable a reduction of this 3D EMF system to simpler 1D or 2D representations.[5-7] Comparison to full rigorous simulation shows an advantage in accuracy by accounting for 3D mask effects versus the Kirchhoff mask.

Recently, even thinner absorbing layers such as Opaque MoSi on Glass (OMOG) have been reported, which further reduce the mask 3D contribution to wafer CD variation, thus rendering the continued use of the Kirchhoff approximation a reasonable trade-off for 28-nm technology node8-9. But for 20-nm node and below it is increasingly necessary to account for the 3D effect.

The return of negative tone develop for 20/14-nm nodes has driven a migration back to 6% attenuated PSM for hole/space layers. For imaging mask transparent spaces to print wafer spaces with positive-tone systems, OMOG was demonstrated in many cases to deliver improved process window over attPSM at 45 to 28-nm technologies. For imaging mask

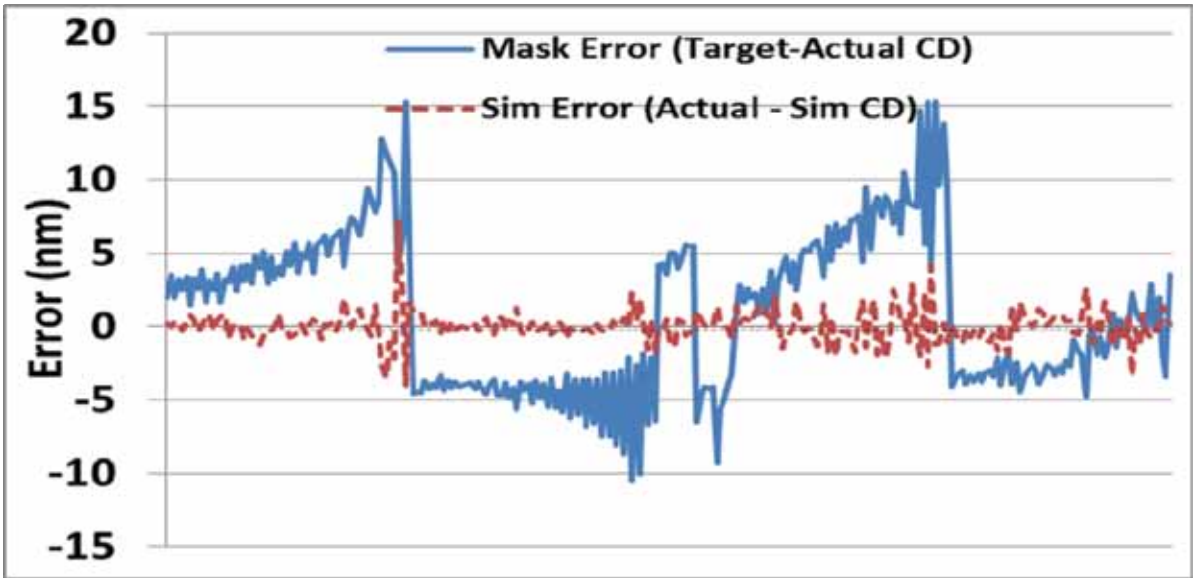

Figure 4. Mask CD error (4X) versus target and residual mask process simulation error.

absorbing lines to print wafer spaces with negative-tone develop, attPSM has an advantage in some cases.[10] Since the attPSM is approximately 40% thicker than OMOG, this will increase the contribution from mask 3D EMF effects, and will drive further adoption of 3DEMF mask full-chip computational models.

This paper examines the impact of uncertainties associated with 3D and 2D representations of the photomask, and it is shown that inaccuracies in the representation of photomask one and two-dimensional CDs can lead to significant errors in the accuracy of the wafer image CDs, computed using the constant threshold resist (CTR) model. Real mask bias data from a state of the art mask manufacturing facility are representation of three-dimensional mask topography can account for relatively large errors in wafer CTR model accuracy.

EXPERIMENTAL

The simulation methodology that was applied in this study is based upon Calibre™ simulation for an ensemble of test patterns featuring variable size and pitch for lines and spaces, as described below. A constant threshold resist (CTR) model was generated using a given set of image simulation parameters and used as a baseline. Then those simulated data were modified such that a single model parameter was altered to determine the sensitivity of that factor. The error in this simulation relative to the baseline is reported as RMS error.[11] All simulations utilized 50 optical kernels and used the 3D EMF mask model with oblique illumination.

The baseline mask for simulation was attenuated PSM with MoSi absorber. It is understood that such a blank substrate may in fact manifest higher CD bias errors than the thin OMOG blank, but was studied due to the likelihood of this mask type being used for 14-nm metal and via layers. The baseline mask, shown in Figure 1, provided 5.8% transmission and 179.6 degrees of phase shifting.

The wafer OPC model testcase was for a 14-nm metal layer negative tone develop (NTD) process, and was comprised of 657 test patterns, with layout CD ranging from 38 to 180 nm, and SRAFs down to 22 nm (1X). It is recognized that true 14-nm layouts will likely have even smaller sub-resolution assist feature (SRAF) dimensions. The test patterns were both 1D and 2D, both horizontal and vertical orientation, and featured mask absorber lines (which are metal spaces on wafer for NTD) and transparent spaces. Defocus was varied from nominal by +/-18nm, +/- 32 nm, +/- 48 nm for a total range of 96 nm. Thus a total of 4598 simulations were conducted for each model condition.

Mask CD measurements were made on thin OMOG masks, for both positive and negative toned chemically-amplified photoresist processes. For bright field masks, the nCAR mask patterning process is used predominantly and pCAR process mostly for dark field masks. A total of 262 mask patterns were measured, comprising lines and spaces in both horizontal and vertical orientation and both 1D and 2D geometries. The target drawn dimensions ranged from 50-800 nm (4X). CD metrology was conducted with a state of the art Advantest CD SEM. Four repeat measurements were averaged to represent the mean for each feature. Feature types included 1:1 dense lines, dense contacts, isolated contacts, isolated lines, through pitch contacts, and through pitch lines.

RESULTS

1. Photomask XY CD errors

There are two different types of errors related to the representation of the photomask that can manifest inaccuracies in OPC models: 1) CD and shape differences between as-designed and actual test patterns used in calibration, and 2) approximations in the model and user input parameters relative to 3D electromagnetic field (EMF) effects. The 2012 ITRS roadmap[12] provides optical photomask specifications for 2014 (~ 14 nm) as shown in Table 1.

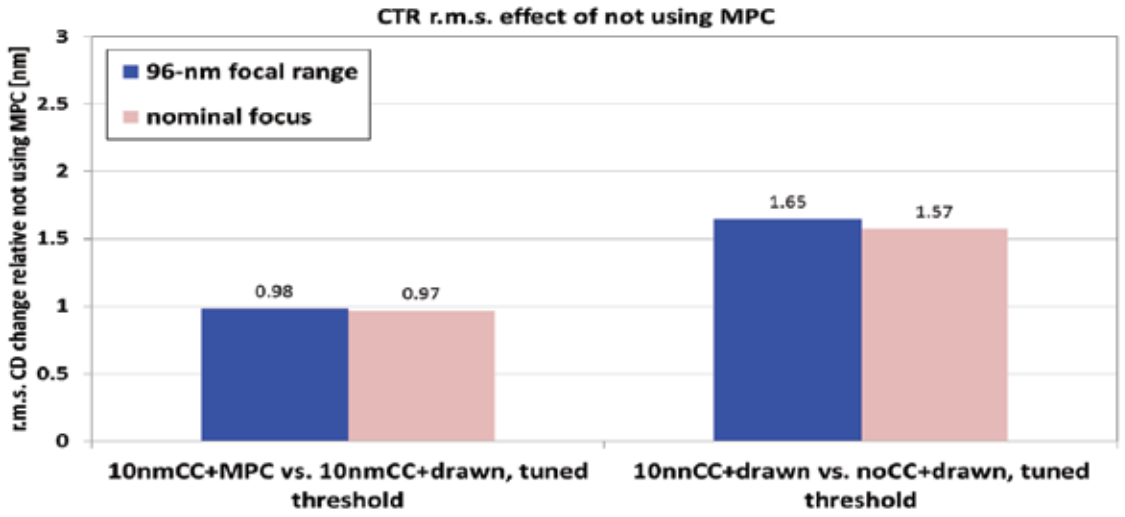

Figure 5. Comparison of CTR RMS improvement available (left) through the use of mask process simulation versus target layout and (right) through the use of 10 nm mask corner rounding applied in wafer simulation.

1.1. Photomask CD errors

Historically, OPC model calibration is based upon simulations of test patterns represented as drawn in the target GDS layout, even though it is known that this is not a completely accurate representation of the real mask. Errors arising from the actual mask being different from the design target have typically been absorbed into the photoresist model, and since systematic mask errors such as proximity bias or corner rounding are fixed for a given mask manufacturing process, this approximation has largely been considered "safe". We investigated the available improvement to the CTR model fitness associated with direct accounting for these errors. utilized to represent the magnitude of the mask CD effect. In addition, uncertainties associated with the

1.1.1. Mean to Target (MTT) Errors

Mean to target errors occur randomly in photomask manufacturing. The operating paradigm has always been that as long as a mask is within a MTT specification, the wafer fab can use exposure dose to adjust for this error with little to no penalty. This is still largely true, but with the extremely high and gaugedependent mask error enhancement factor (MEEF) values in low k_1 lithography, there is an increasing penalty associated with global MTT errors. Figure 2 shows the RMS error relative to a perfect no bias mask, after dose/threshold correction. The current ITRS specification for MTT errors are 2.0 nm (4X) or 0.5 nm at wafer scale, or 0.25 nm per mask edge. It can be seen that such MTT errors result in approximately 0.5 nm CTR RMS error relative to the perfectly on target mask.

For any given wafer OPC calibration test mask, measurements can reveal the MTT error, and in principle, this error can be accounted for in the OPC model. The challenge comes in applying such a model to a production chip mask, where it is possible that the MTT error could be of opposite sign as the calibration test mask, in which case more harm than good could be accomplished. However, for a given production chip mask, once it is manufactured, the MTT is known, and a verification model that comprehends this MTT error could be used to more accurately predict wafer behavior.

1.1.2. Proximity and Linearity Errors: Mask Proximity Model

A second class of mask errors reflects the fact that the photomask manufacturing process, like the wafer patterning process, manifests systematic proximity and linearity effects. So even if a given mask is exactly on target for the average CD across multiple feature types and locations, there can by systematic variations in mask CD versus pitch or target dimension. For this study, actual mask measurement data provided the basis for calibrating a mask proximity model, which was then used to alter the test pattern layout in order to more accurately represent a typical 14-nm photomask. The mask measurements resulted in a mean to target deviation of -0.99 nm, and a standard deviation of 5.26 nm (4X). It is noted that the features included both dense, through pitch, and isolated lines and spaces as well as dense, through pitch, and isolated contacts and mesas. For actual production masks, there would not typically be such a variety of feature types, and the CD uniformity for a given feature is tighter. For an individual feature type, however, there is a strong nonlinearity in bias as the target dimensions drop below 200 nm, as illustrated in Figure 3.

A mask proximity model calibration results, optimized using 262 features, are show in in Figure 4. Plotted are the mask bias values (target – measured CD) and the simulation errors (measured – simulated CD). It can be seen that the mask proximity model faithfully predicts the actual mask CD to within 1.1 nm RMS error (4X). Therefore, with bias-to-target errors of 5.35 nm RMS, it would be expected that conducting wafer OPC model calibrations by referencing the post MP model representation of the mask would yield a significant improvement in results over assuming the mask is perfectly on target. Indeed, Figure 5 shows the strong benefit in improved CTR RMS fitness of using a MP model to represent the actual mask manifestation of the test patterns.

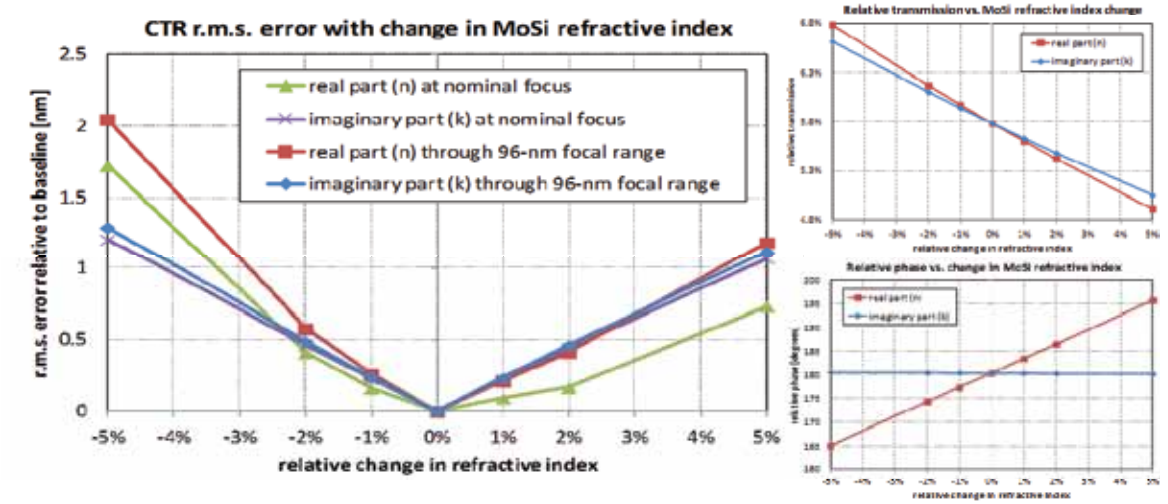

Figure 6. Impact of changing the MoSi real and imaginary refractive indices on CTR RMS error at nominal condition and through focus. At right are shown the corresponding normal incidence transmission (top) and phase (bottom) results for each case.

1.2. Corner Rounding Errors

It is well known that due to the finite resolution of the mask writing process, the physical mask edges are not sharp corners, but are rounded with a characteristic corner rounding that can be regarded as systematic for a given process. For two-dimensional features such as contact holes, this rounding can have a substantial impact on wafer patterning. Convex and concave corner rounding can be empirically tuned during OPC model calibration, and yields corner rounding values of approximately 10-15 nm, which is consistent with direct mask SEM corner rounding measurements. Figure 5 shows the improvement in model fitness for the 14 nm metal testcase layer by assuming a sharp corner versus using the optimized corner rounding. More than 1.5 nm CTR RMS improvement can be realized by assuming corner rounding consistent with the mask SEM image.

2. Photomask 3D EMF Model

Rapid full chip 3D EMF mask model simulation is accomplished by making approximations to the rigorous finite difference time domain (FDTD) solution. The EMF signals are generated based upon the user defined representation of the mask stack, which requires input of the real and imaginary indices of refraction, and thickness of the various layers comprising the mask. In addition, the user indicates the sidewall angles and corner topography details. The interesting question is how wafer OPC modeling engineers access accurate parameters to feed into the simulation tool.

2.1. Mask Blank refractive index and thickness

The first parameter investigated was MoSi absorber refractive index. Both the real and imaginary components were independently altered through +/- 5% of the baseline values. A deviation of 2% in n or k from baseline results in approximately 0.4% transmission difference and 5 degrees of phase difference. For the 14-nm metal OPC model, this drives a CTR RMS difference to approximately 0.5 nm, as shown in Figure 6.

Next the impact of MoSi thickness was studied. The MoSi absorber film thickness was altered from the nominal 70 nm by +/- 5%. This resulted in linear transmission and phase differences as shown in Figure 7.

In this case, a 2% thickness deviation gives rise to 0.3 nm RMS difference at nominal focus and 0.4 nm RMS difference through defocus.

It is well known that quartz overetch is used to target the desired 180-degree phase shift between the MoSi absorber and the silica features. The overetch depth was varied from 0 to 12 nm (6 nm baseline) resulting in a range of phase values from 174 to 187 degrees. The impact of phase only versus phase and transmission changes can be seen in comparing Figures 7 and 8.

2.2. Patterned mask sidewall angle and corner rounding

Finally, the impact of mask absorber sidewall angle and top corner rounding was examined. The RMS CD difference response to slope is quite pronounced, a full 1.0 nm per degree at nominal focus and more at defocus for steeper angles than the 88 degree baseline. (See Figure 9). Stack rounding corner radius of 17 nm gives rise to a similar 1.0 nm RMS CD difference.

DISCUSSION

Shrinking target dimensions and CD control budgets require that all sources of error be thoroughly understood and mitigated. There have been steady improvements in both mask CD control and OPC model accuracy that have contributed to enabling manufacturing down to 20 nm node design rules. Model accuracy is dependent upon a proper representation of the photomask in the simulator, and there are many sources of potential uncertainty in such a representation. The most significant factor from this analysis appears to be the one that has long been known to be a vulnerability in wafer OPC modeling methodology: systematic mask XY critical dimensions biases. It is true that ignoring such effects and leaving it to the resist model to compensate has been an accepted approach for many generations of technology, but for 14 nm it

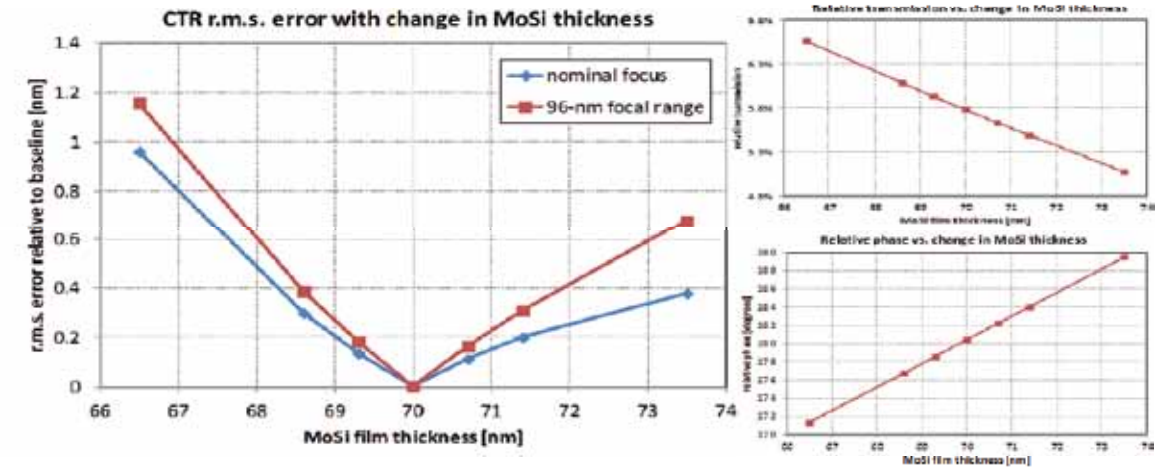

Figure 7. Impact of changing the MoSi thickness on CTR RMS error at nominal condition and through focus. At right are shown the corresponding normal incidence transmission (top) and phase (bottom) results for each case.

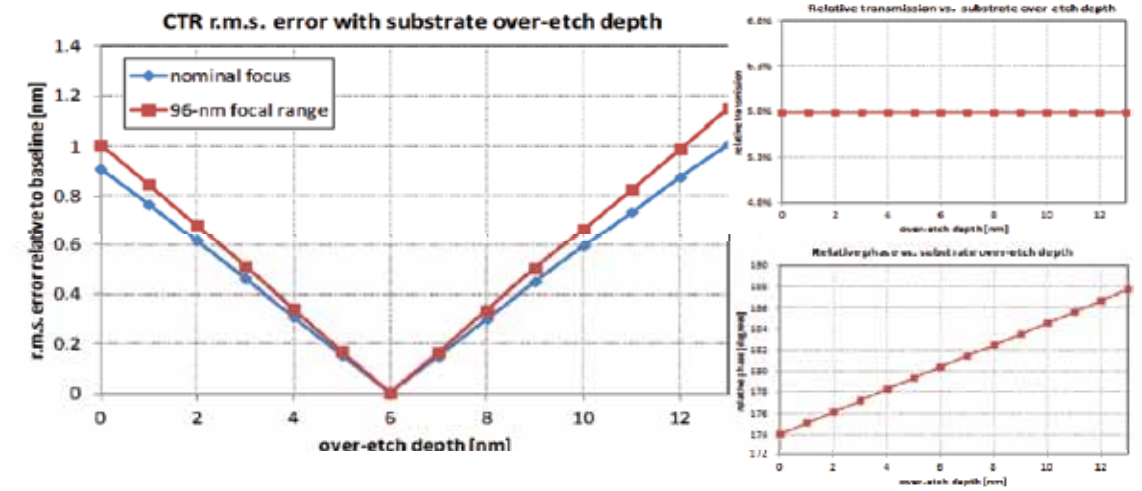

Figure 8. Impact of changing the quartz overetch on CTR RMS error at nominal condition and through focus. At right are shown the corresponding normal incidence transmission (top) and phase (bottom) results for each case.

is prudent to appropriately capture the mask error for optimum model predictability.

Accounting for systematic mask corner rounding can be easily accomplished in the OPC simulator, and doing so results in over 1.5 nm of CTR RMS error improvement versus assuming the mask has sharp corners. Further work is required to understand whether a global corner rounding bias applied to all corners is appropriate or whether feature dependent corner rounding biases can deliver even further improvement in the optical CTR model fitness.

Systematic proximity and nonlinearity CD bias on the mask can be very accurately modeled and by representing the mask with the modeled contour instead of the input GDS layout, up to 1.0nm improvement in CTR accuracy for wafer data can be realized. Mask Proximity Modeling should be utilized for 14-nm model calibration, either through correction at the mask shop or through awareness during wafer OPC model calibration.

Finally, a third type of mask XY error can only be considered "quasi-systematic". Global mean to target errors are generally well controlled during mask manufacturing, but for 14 nm, up to 0.50-nm (1x) CD mean errors are allowed. Given the feature dependence and in some cases extremely high MEEF (>4), such errors are not adequately accounted for by simply changing model threshold, akin to in-fab exposure dose adjustment. While it is true that for any given mask in production, the bias cannot be known a priori, for the specific test mask on which wafer OPC calibration is conducted, the bias is knowable from mask measurements and can be corroborated during empirical tuning of the wafer OPC model. By so doing, approximately 0.5 nm of improvement in wafer CTR RMS error can be realized.

Beyond XY CD biases on mask, it has been important since 20-nm technology node to consider mask 3D electromagnetic field effects in the wafer OPC model. The thin mask (TMA) or Kirchhoff approximation can leave more than 1 nm RMS of

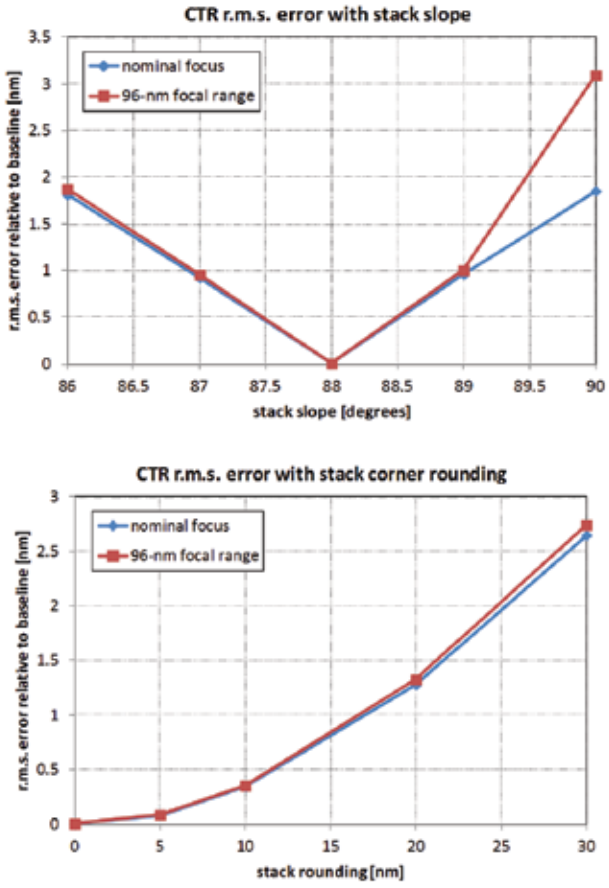

Figure 9. Impact of changing the MoSi slope (left) and corner rounding (right) on CTR RMS error at nominal condition and through focus.

nominal focus CD error and much higher errors for defocus conditions.

In order to create a 3D EMF mask model, it is necessary to provide information associated with the physical and optical properties of the photomask. This is directly analogous to the type of information that is needed by the simulator to model the optics: wavelength, numerical aperture, magnification, illumination profile, wafer film stack, etc. Many such parameters are knowable as design values, but others derive from various metrology techniques, such as spectroscopic ellipsometry. In the case of photomask modeling, it is observed that there are large ranges amongst users for the input values for refractive index, thickness, and sidewall angle for "industry standard" attenuated MoSi PSM. It is certainly possible that specific mask manufacturing processes can alter parameters such as sidewall angle or corner rounding, but this observation may also highlight uncertainties associated with photomask metrology methods.

In addition to the above issue, it is important to assess whether the current ITRS roadmap mask specifications are in fact sufficient to deliver the requisite wafer CD accuracy for 14-nm technology.

Combining the MTT and range specifications, the effective total range of possible transmission values for a nominally 5.8% transmission mask would be 5.40-6.21%. Similarly, the effective total range of possible phase for a nominally 180 degree mask would be 174-186 degrees. Each of these correspond to approximately 0.5 nm CD RMS error, with resulting CD error ranges of approximately 5 nm at nominal focus and over 10 nm at defocus. It is important to emphasize that these errors cannot be fixed by adjusting dose in the fab. It may be necessary to tighten these specifications, and in addition, to ensure improved accuracy in the determination of mask transmission, phase, thickness, and sidewall angle so that the OPC mask models can in turn be more accurate.

CONCLUSION

The 14 nm node will be characterized by extremely aggressive CD control targets, and with the traditionally assumed allocation of 50% of that budget for the photomask, approximately 2 nm of reticle scale CD control will be required. Photomask CD control has largely been specified in terms of mean-totarget, CD uniformity, and linearity errors. The latter have typically received the least attention, but at 14 nm, the MEEF for some features will approach or exceed 4, such that a mask with 4 nm

of nonlinearity can manifest approximately 4 nm errors at wafer scale, which is a very large error relative to the OPC model accuracy targets. In practice, the nonlinearity when going all the way down to SRAF dimensions can greatly exceed 4 nm. It is imperative to account for such errors appropriately and not merely absorb them into the photoresist black box model.

One approach for dealing with these systematic errors is to eliminate them at the mask manufacturing facility through the use of mask proximity models and correction. Alternatively, the mask process models may be referenced to create a virtual mask for use when calibrating wafer OPC models, and we have shown how such an approach can lead to significant improvements in wafer OPC model accuracy. Similarly, the systematic corner rounding present on masks can be simulated and enables a very large improvement in wafer model accuracy.

As important as two-dimensional mask CD specifications are, three-dimensional considerations are increasingly vital as 14-nm processes utilize attenuated PSM masks, and wafer OPC models incorporate 3D EMF simulation. There are several mask processing related parameters including absorber sidewall slope and corner rounding, as well as quartz overetch that can have a significant impact on wafer CD results. In addition, the absolute accuracy of the absorber thickness and refractive indices is a key to dictating the effective phase and transmission used in the simulator, which in turn has a strong influence on the wafer CD simulation results. Misrepresentation of the actual values in the simulator will lead directly to OPC optical/mask model errors that the resist model will attempt to compensate. Improvements in metrology methods are therefore necessary to confirm the accuracy of such measurements.

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EDITORIAL

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in photomask production. Mask making itself is quickly turning into a fine and precise art (remember Rembrandt).

Some Perspective

The Fast Food Theory (shamelessly stolen from Medium and reprinted here)

A trick to try with co-workers when trying to decide where to eat for lunch and no one has any ideas. Recommend fast food.

An interesting thing happens. Everyone unanimously agrees that we can't possibly go fast food, and better lunch suggestions emerge. Magic!

It's as if we've broken the ice with the worst possible idea, and now that the discussion has started, people suddenly get very creative. Call it the Fast Food Theory: people are inspired to come up with good ideas to ward off bad ones.

Nothing catalyzes people like a pending disaster.

There's no defined process for all creative solutions, but all creative endeavors share one thing: the second step is easier than the first. It takes a crazy kind of courage, of focus; of foolhardy perseverance to quiet all those doubts long enough to move forward.

Sketch a few shapes, then label them. Say, "This is probably crazy, but what if we.…" and try to make your sketch fit the problem you're trying to solve. The moment you put the stuff on the board, something incredible will happen. The room will see your ideas, will offer their own, will revise your thinking, and you'll have made progress.

That's how it's done.

Industry Briefs

TSMC Plots System Super Chips -

By **Colin Johnson,** EETimes

Taipei, Taiwan — The world's leading semiconductor foundry, TSMC, detailed its plans to dominate the "system super-chip" market. According to TSMC's VP, Jack Sun, "If anybody pushes Moore's Law to extremes, TSMC will be there too, but that is not all we do. We also have specialized technologies such as embedded flash, high-voltage, power transistors, MEMS and image sensors. And as we move monolithic CMOS on to more advanced nodes, all these other technologies can not be moved along with it — that's where our interposers and 3-D technologies will enable integration in a system super-chip packages."

TSMC revealed its roadmap for monolithic CMOS, starting with advanced planar SoCs at the 20-nanometer in 2013, using double-patterning without direct coloring by virtue of its novel method of avoiding G-rule violations. TSMC will follow up with FinFETs at the 16-nm node by 2014. Next TSMC plans to transfer its FinFETs to the 10-nm node by 2015 to 2016 for a 35 percent speed gain, using either direct-write multiple e-beams or extreme-ultra-violet (EUV), which it is developing with ASML.

"We have already demonstrated EUV with our preproduction tools, and our early production tools are now being installed. The availability of the light-source is the main obstacle, along the mask color code and operating in a vacuum system, and there is always a steep learning curve for any new lithography," said Sun. Closer to the manufacturing floor is e-beam lithography, which TSMC has been perfecting with Mapper Lithography, using multiple beams for direct-write in novel patterns that avoid hot spots while maintaining the high-throughput necessary to make it commercially feasible.

Yet more experimental that e-beam and EUV are new techniques and materials to TSMC hopes to perfect at the 7-to-5 nanometer node in time to put it ahead of the pack. At these advanced nodes the transistors channels will have to be made either of silicon nanowires or possibly from III-V materials, such as indium arsenide (InAs) deposited on a silicon substrate. TSMC is holding its cards near its vest, but claims to see a clear path to 5-nanometer operating at voltages as low as 0.5 volts in as little as 10 years.

Japan Fair Trade Commission Clears ASML Acquisition of Cymer

VELDHOVEN, the Netherlands/SAN DIEGO, United States, 2 May 2013 – ASML Holding NV (ASML) and Cymer, Inc. (Nasdaq: CYMI) announced that the Japan Fair Trade Commission (JFTC) has cleared the previously announced merger between Cymer and affiliates of ASML.

Clearance of the merger has previously been granted by the U.S. Department of Justice, the U.S. Committee on Foreign Investment in the United States (CFIUS), as well as the Taiwanese, German and Israeli antitrust authorities. Furthermore, Cymer stockholders have approved the merger agreement.

As already indicated in the deal announcement of 17 October 2012, ASML will manage Cymer as an independent business unit where it concerns commercial hardware sales and services activities, and Cymer will continue to supply sources to and engage in R&D activities with all lithography tool manufacturers on fair, reasonable and non-discriminatory commercial terms. Furthermore, ASML reiterates it will continue to let its scanner customers choose their preferred light source, and its scanners will continue to interface with light sources from all manufacturers.

Global Semiconductor Sales Outplace Last Year Through Q1 of 2013

The Semiconductor Industry Association (SIA), representing U.S. leadership in semiconductor manufacturing and design, announced that worldwide sales of semiconductors reached $23.48 billion for the month of March 2013, an increase of 1.1 percent from the previous month when sales were $23.23 billion. Global sales for March 2013 were 0.9 percent higher than the March 2012 total of $23.28 billion, and total sales through the first quarter of 2013 were 0.9 percent higher than sales from the first quarter of 2012. All monthly sales numbers represent a three-month moving average.

"Through the first quarter of 2013, the global semiconductor industry has seen modest but consistent growth compared to last year," said Brian Toohey, president and CEO, Semiconductor Industry Association. "Sales have increased across most end product categories, with memory showing the strongest growth. With recent indications that companies could be set to replenish inventories, we are hopeful that growth will continue in the months ahead. Regionally, the Americas slipped slightly in March after a strong start to the year, but Asia Pacific and Europe have seen impressive growth."

Join the premier professional organization for mask makers and mask users!

About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

Individual Membership Benefits include:

- Subscription to BACUS News (monthly)
- Complimentary Subscription *Semiconductor International* magazine
- Eligibility to hold office on BACUS Steering Committee

www.spie.org/bacushome

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- Three Voting Members in the SPIE General Membership
- Subscription to BACUS News (monthly)
- One online SPIE Journal Subscription
- Listed as a Corporate Member in the BACUS Monthly Newsletter

www.spie.org/bacushome

Calendar

2013

SPIE Photomask Technology

10-12 September 2013
Monterey Marriott and
Monterey Conference Center
Monterey, California, USA
www.spie.org/pm

Submit late abstracts directly to Pat Wight, patw@spie.org, for consideration by conference chairs.

2014

SPIE Advanced Lithography

23-27 February 2014
San Jose Convention Center
and San Jose Marriott
San Jose, California, USA
www.spie.org/al

SPIE is the international society for optics and photonics, a not-for-profit organization founded in 1955 to advance light-based technologies. The Society serves nearly 225,000 constituents from approximately 150 countries, offering conferences, continuing education, books, journals, and a digital library in support of interdisciplinary information exchange, professional growth, and patent precedent. SPIE provided over $3.2 million in support of education and outreach programs in 2012.

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You are invited to submit events of interest for this calendar. Please send to lindad@spie.org; alternatively, email or fax to SPIE.