PHOTOMASK

BACUS—The international technical group of SPIE dedicated to the advancement of photomask technology.

BACUS NEWS

JUNE 2012
VOLUME 28, ISSUE 6

Best Paper Award of MOEMS-MEMS 2012
(Authors generously donated the award funds to the BACUS Scholarship Fund.)

Programmed resist sidewall profiles using sub-resolution binary grayscale masks for Si-photonics applications

Ofir Gan, Assia Barkai, Harel Frish, Micron Semiconductor Israel Ltd P.O.Box 1320 Kiryat-Gat 82109, Israel

Paul Allen and Peter Buck, Toppan Photomasks, Inc., 1500 NW Bethany Blvd., Beaverton, Oregon USA 97006

Brid Connolly, Toppan Photomasks Germany, Raehnitzer Allee 9, Dresden Germany 01309

Massimiliano Pindo, Toppan Photomasks France, Rousset, 118 Avenue Francis Perrin, Rousset France 13106

ABSTRACT

In this paper we present a 45-degree mirror created for optical applications utilizing CMOS high-volume manufacturing processes with a gray-scale lithography technique. The process that is presented here was done by creating a 3D pattern in the photoresist and then by transferring the photoresist profile to the Si/SiO_2 substrate by specific dry etch processing. We discuss the optimization of the half-tone pattern to achieve the desired resist profile. We achieved smooth sidewalls with various sidewall angles and show that different 3D angles and profiles can be achieved and processed simultaneously.

Introduction

Recently there is a large interest in silicon optical component processing, which is based on fabrication technologies originating from the mature processes developed

Continues on page 3.

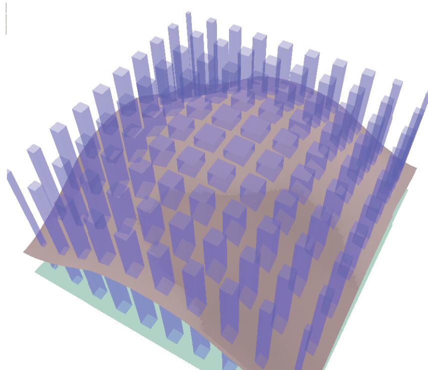


Figure I. Sub-resolution half-tone pattern showing resulting resist surface after development.

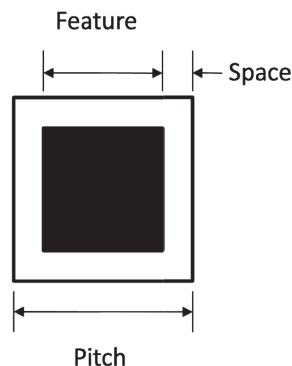


Figure II. Sub-resolution half-tone cell.

TAKE A LOOK INSIDE:

INDUSTRY BRIEFS
—see page 14

CALENDAR
For a list of meetings
—see page 15

Editorial

"Innovation distinguishes between a leader and a follower." — Steve Jobs

Larry Zurbrick, Agilent Technologies

Innovation is the driver in the semiconductor and mask making industries. It never ceases and never ceases to amaze me. Many of past BACUS News editorials and articles have acknowledged the innovativeness of those in our industry, whether they are mask makers, material suppliers, software suppliers or equipment manufacturers. In each segment, innovation is a way of life. What was leading edge yesterday is the workhorse today and will be obsolete tomorrow as newer technologies come to the forefront. What was perceived as impossible or very difficult yesterday is now commonplace in the industry. This is common across all aspects of our high-tech industry, from basic raw materials to the final consumer product.

It is interesting to see how innovation continually pushes the red brick wall out another node in the ITRS Roadmap. The connection to my day to day work relates to overlay registration. The division of Agilent Technologies I work in produces laser interferometer systems that find their way into stage positioning systems. When I first became a mask maker the step and repeat camera and optical pattern generator were reaching their zenith. Each was controlled by a Hewlett-Packard laser interferometer system with a resolution 0.158 um. Fast forward to today and resolution of Agilent interferometer systems is 0.15 nm, a 1000X increase. (Note that Agilent Technologies was spun out of Hewlett-Packard in 1999.) Along the way, a number of "discoveries" were made that appeared to limit the accuracy of laser interferometer systems and each were addressed through an innovation. Looking forward from today to meeting the position measurement and overlay accuracy roadmap for the sub-10 nm node whether the lithography of choice be EUV, multiple patterning, nano-imprint or something else, the error budget numbers allotted to the position measurement system are incredibly tiny. Typically the error budget allotted to the position metrology system is one-tenth the overlay tolerance. In the case of the 10 nm node and assuming the ITRS Optical Mask Requirement image placement spec of 1.2 nm, 0.12 nm would be allotted to the stage positioning metrology system. Assuming that there are 10 statistically independent error budget items related to the interferometer system, this would mean that each budgeted item would get allotted approximately 0.04 nm. To put this in perspective, this is approximately the theoretical atomic radius of the neon atom used in the interferometer system's HeNe laser. (As an aside for all you chrome users, the theoretical atomic radius of a chromium atom is 0.166 nm, larger than the current resolution of the interferometer system.) The innovations to get there are already being discussed and planned. I look forward to Agilent continuing to help its customers move bricks in the wall forward a node at a time.

BACUS N • E • W • S

BACUS News is published monthly by SPIE for BACUS, the international technical group of SPIE dedicated to the advancement of photomask technology.

Managing Editor/Graphics Linda DeLano
Advertising Lara Miles
BACUS Technical Group Manager Pat Wight

■ **2012 BACUS Steering Committee** ■

President
Wolfgang Staud, *Applied Materials, Inc.*

Vice-President
John Whittey, *KLA-Tencor MIE Div.*

Secretary
Artur Balasinski, *Cypress Semiconductor Corp.*

Newsletter Editor
Artur Balasinski, *Cypress Semiconductor Corp.*

2012 Annual Photomask Conference Chairs
Frank E. Abboud, *Intel Corp.*
Thomas B. Faure, *IBM Corp.*

International Chair
Naoya Hayashi, *Dai Nippon Printing Co., Ltd.*

Education Chair
Artur Balasinski, *Cypress Semiconductor Corp.*

Members at Large
Paul W. Ackmann, *GLOBALFOUNDRIES Inc.*
Michael D. Archuletta, *RAVE LLC*
Uwe Behringer, *UBC Microelectronics*
Peter D. Buck, *Toppan Photomasks, Inc.*
Brian Cha, *Samsung*
Kevin Cummings, *ASML US, Inc.*
Glenn R. Dickey, *Shin-Etsu MicroSi, Inc.*
Thomas B. Faure, *IBM Corp.*
Brian J. Grenon, *Grenon Consulting*
Jon Haines, *Micron Technology Inc.*
Mark T. Jee, *HOYA Corp, USA*
Bryan S. Kasprowicz, *Photronics, Inc.*
Oliver Kienzle, *Carl Zeiss SMS GmbH*
Wilhelm Maurer, *Infineon Technologies AG*
M. Warren Montgomery, *The College of Nanoscale Science and Engineering (CNSE)*
Abbas Rastegar, *SEMATECH North*
Emmanuel Rausa, *Plasma-Therm LLC.*
Douglas J. Resnick, *Molecular Imprints, Inc.*
Steffen F. Schulze, *Mentor Graphics Corp.*
Jacek K. Tyminski, *Nikon Precision Inc.*
Larry S. Zurbrick, *Agilent Technologies, Inc.*

SPIE

P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 360 676 3290
Fax: +1 360 647 1445
SPIE.org
help@spie.org

©2012

All rights reserved.

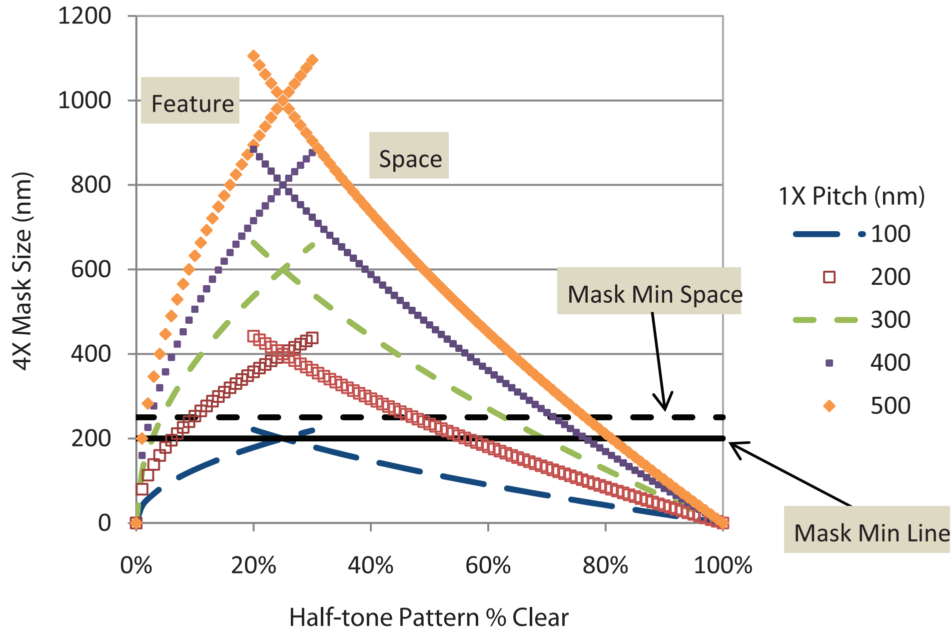


Figure III. Feature size requirements to achieve % clear values close to zero and 100% as a function of half-tone pitch and the limitations of mask manufacturing.

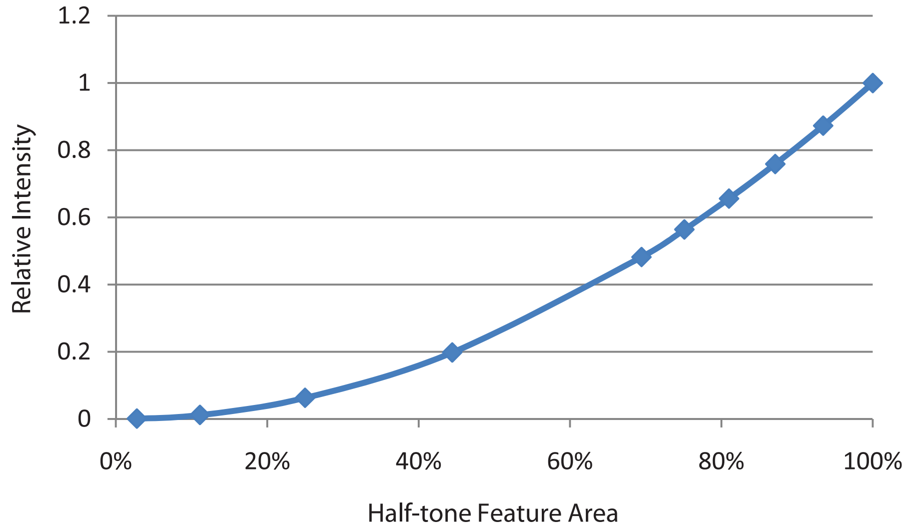


Figure IV. Relative transmitted intensity for an optical lithography tool with λ = 365 nm, NA = 0.5, & σ = 0.68. Due to finite resolution the transmitted intensity is not linear with % clear area for small feature sizes.

for silicon integrated circuit fabrication. However, common IC fabrication processes can achieve only a limited number of etched sidewall profiles: vertical sidewalls through dry anisotropic etching; angled sidewalls dependent on the crystallographic orientation of the substrate through wet anisotropic etching;[1] or undercut profiles through dry/wet isotropic etching. Conversely, there is an ever-increasing interest in a high-volume fabrication technique that can realize gradient height profiles in silicon. Such a technique is required in silicon photonics for various applications, such as: optical mirrors for light redirection;[2,3] gradual transition of the optical mode for fiber coupling.[4]

Forty-five degree mirrors are used routinely in silicon photonics in order to reflect the guided mode light either upwards or downwards through the substrate. This approach is particularly attractive since at 45° the incident light undergoes total internal reflection (TIR) at the SiO_2/Si-air interface.

A technique using half-tone lithography has proven to be a useful batch process to create gradient height structures. This method is a one-level lithography process enabling the development of 3D profiles in a photoresist masking layer, which can then be transferred to the silicon substrate. The half-tone photomask is manufactured using conventional

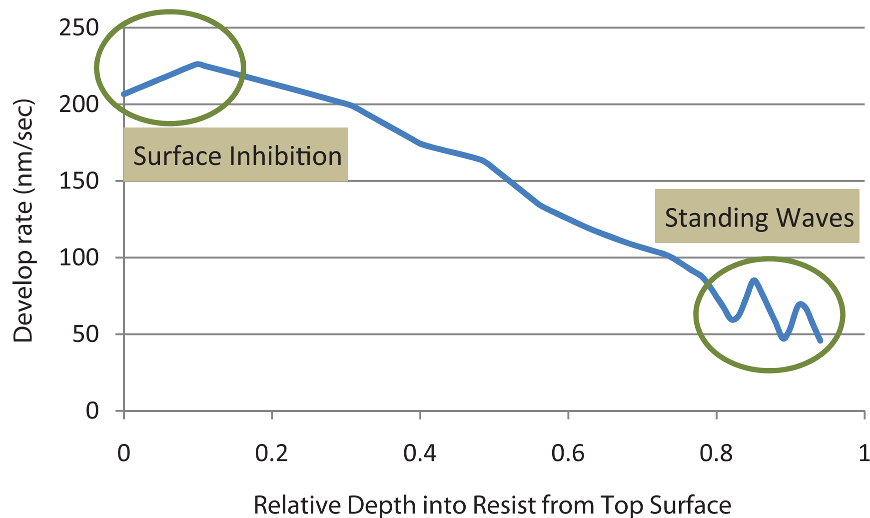


Figure V. A plot of develop rate as a function of relative depth into the resist shows surface inhibition and standing wave effects.

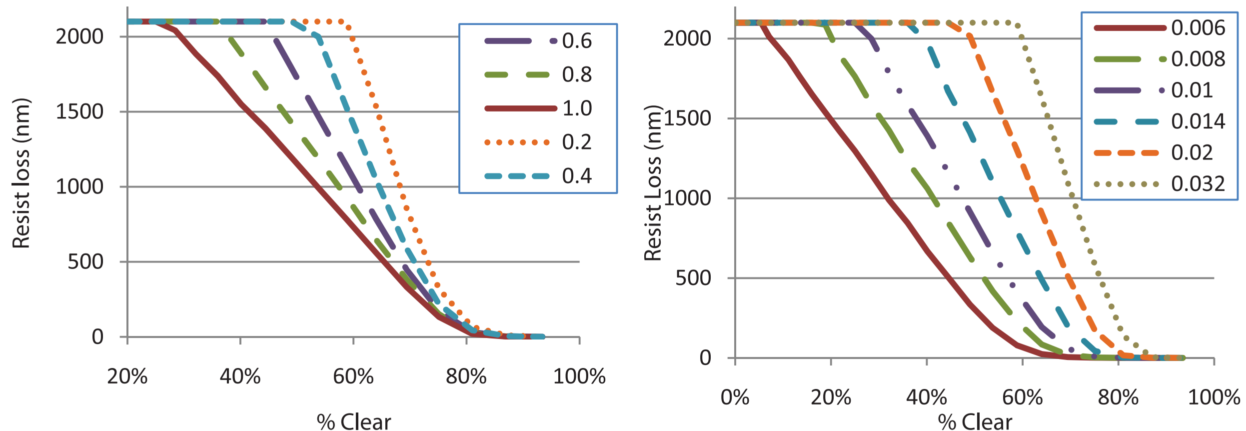


Figure VI. Influence of Dill "A" (left) and Dill "C" (right) on the resist loss characteristic curve for a 2-μm coating of resist, using a clear-field half-tone pattern simulated with Prolith™.

chrome-onglass materials and manufacturing methods but utilizes variable density arrays of sub-resolution patterns to create a transmittance gradient. The mask feature dimensional characteristics need to be chosen to meet mask manufacturing requirements. The effective transmittance must be matched to the wafer lithography photoresist response to achieve the desired sidewall profile.

Similar sidewall profiles can be achieved by other methods such as tuning of the resist slope with hard-baking using standard binary photomasks[5] or directional etching using chemically assisted ion beam etch (CAIBE).[1] These methods are limited by poor process stability and long process times. The gray scale lithography overcomes these limitations and has a unique capability of forming different 3D angles and profiles simultaneously. Therefore it was chosen in this case.

Approach

Imaging photoresist (resist) involves altering the dissolution rate of the resist as a function of absorbed exposure. In a positive resist the dissolution rate increases as a function of absorbed exposure (the "latent image"). As the resist is developed, the exposed regions of resist dissolve at different rates relative to the absorbed exposure dose. The absorbed exposure varies with depth into the resist film as a function of the resist transparency; thus, the top of the resist film receives more exposure than the bottom. The absorbed exposure also varies with position across the edge of an exposed region because of the finite contrast of the aerial image used to expose the resist. The combination of finite aerial image contrast, a finite dissolution contrast and an exposure absorption gradient throughout the thickness of the resist film causes the developed image to be wider at the top of the resist than at the bottom, naturally producing a sloped resist sidewall profile. The top of the resist film

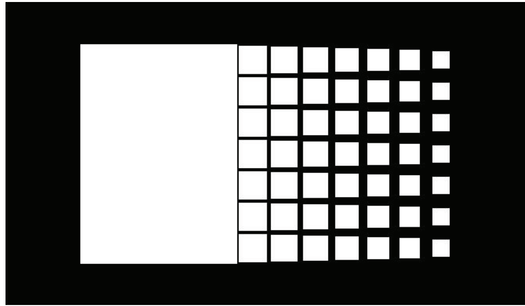


Figure VII. Typical mask for 45° slope solution.

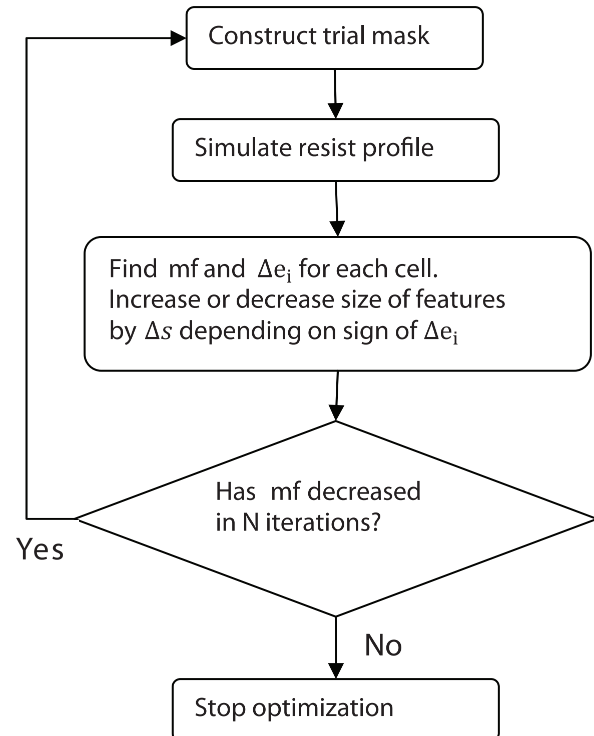


Figure VIII. Refined algorithm for optimizing halftone cells.

receives a longer develop time than the bottom of the resist film. Because of the finite dissolution contrast, the developed feature edge occurs at a different absorbed exposure value at the top of the resist than at the bottom. The design of resists used for IC manufacturing strives to produce vertical resist sidewalls by making the resist as transparent as possible to reduce the absorbed exposure gradient throughout the thickness of the resist film and by making the dissolution contrast as high as possible to deal with a finite aerial image contrast. Totally transparent resists are insensitive to exposure. To solve this apparent conflict (non-transparency is required for exposure to occur, but transparency is required for constant vertical absorbed exposure gradients) the DNQ-novolak resist systems used for *i*-line lithography take advantage of a bleaching phenomenon, where the resist is non-transparent before exposure but turns transparent after exposure. As exposure occurs from the top of the resist to the bottom, the exposed resist turns transparent allowing the underlying resist to be exposed at nearly the same dose throughout the resist film thickness.[6] Photoresists for 248-nm and 193-nm lithography use chemical amplification to allow for very low levels of initial exposure absorption in a transparent resist.[7]

The method we have chosen to produce programmed resist sidewall slopes in resists designed for vertical sidewalls is to create an exposure dose profile tuned to the absorption and dissolution characteristics of the photoresist to control resist dissolution such that the desired resist edge profile is achieved. This requires solving two problems: determining the required exposure dose profile and producing that dose profile using a photomask. We will tackle the latter problem first, since the computational methodology developed to solve the former problem depends on our photomask strategy.

Mask Strategy

Chrome-on-glass (COG) photomasks for IC manufacturing are intended to transmit a binary image to the photoresist in a wafer exposure tool. The photomask is typically composed of a transparent fused silica substrate coated with a thin chromium oxynitride film (Cr_xO_yN). The chrome layer is formulated to produce an optical density of >3 at the exposure wavelength and to have physical characteristics favorable to manufacturability and durability in use.[8] One method to use COG masks to deliver an exposure gradient is to partially etch the chrome film to produce regions of lower optical density. Since optical density is linear with thickness, if the mask absorber film were uniform with depth it would be a simple matter to calculate the required absorber thickness to achieve the desired transparency. However, the composition of the Cr_xO_yN film changes with thickness to achieve acceptable adhesion to the substrate, to have favorable etch properties, and to have low reflectance at the surface. This makes it difficult to predict the required thickness for a given transparency. This is compounded by an etch rate that varies with depth due to the changing composition. Finally, this method requires multiple coat/expose/develop/etch cycles to produce each level of transparency desired.

Another method to produce transmittance gradients involves the use of alternate mask materials that change transparency as a function of exposure dose during mask fabrication.[9] The material is only sensitive to high-energy electron exposure and not to typical wafer exposure wavelengths, so it is possible to generate the transmittance gradients with 50-keV electron beam exposure tools and still use these masks in wafer fabrication. However the exposure dose to generate halftone masks using these materials is several orders of magnitude greater than typical production photomask lithography tools are able to produce and, as with the previous example, each level of transparency requires a separate exposure step although with this material there is no processing to worry about.

The method we have chosen utilizes conventional COG mask material and conventional mask lithography and

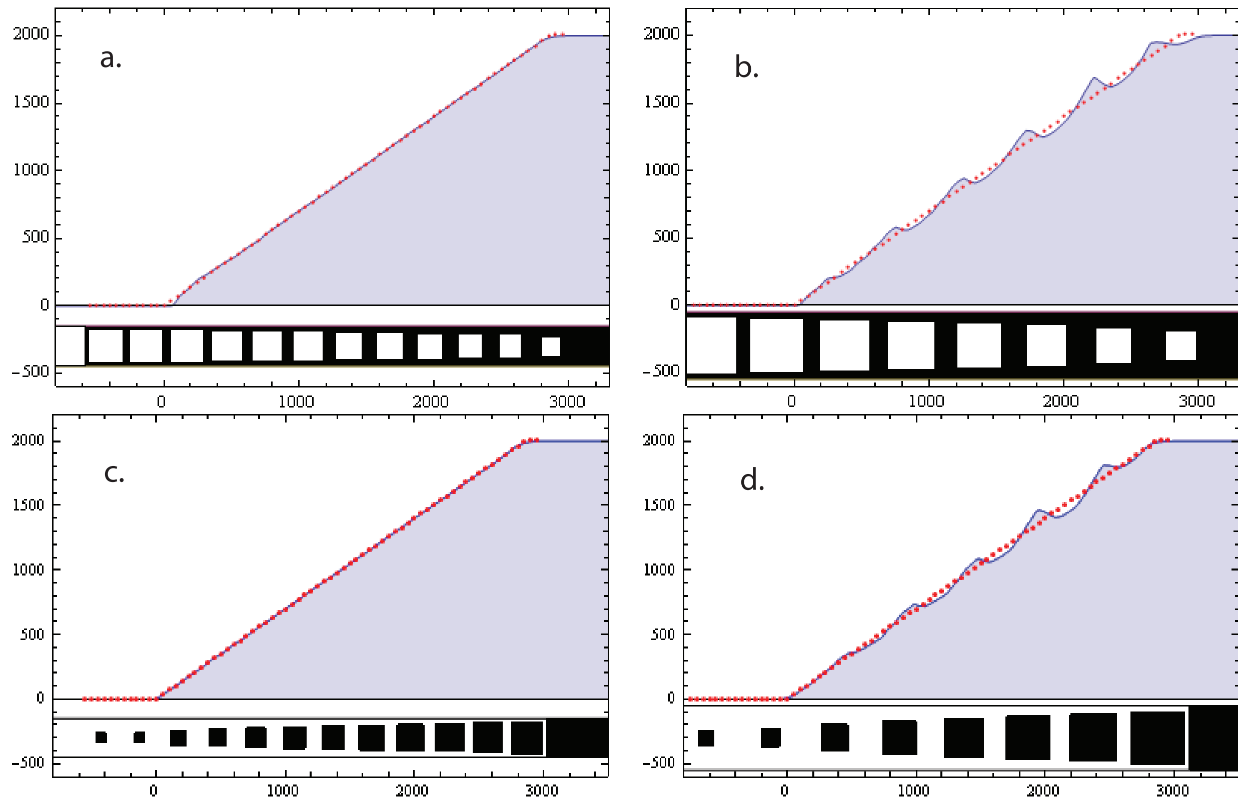


Figure IX. Four optimizations in 2 micron thickness resist and target slope angle of 35 deg. a.) 300 nm cell pitch with contacts, b.) 500 nm cell pitch with contacts, c.) 300 nm cell pitch with posts, d.) 500 nm cell pitch with posts. Horizontal and vertical axes are in nanometers.

processing. To produce varying transmittance we use sub-resolution half-tone patterns composed of arrays of features of a size below the resolution limit of the wafer lithography tool by varying either the size of features on a fixed pitch or by varying the pitch of a fixed size feature the effective transmittance of the mask can be altered. An example of a sub-resolution half-tone pattern super-imposed on the two-dimensional resist surface that results is shown in figure I. The basic half-ton pattern cell is shown in Figure II.

Since there is no difference from conventional COG mask manufacturing this method is conducive to high volume manufacturing from the mask cost perspective. As with any circuit design, however, some attention needs to be paid to mask manufacturing limits to select a mask manufacturing process that has the best cost/performance trade-offs. Two areas that are specific to gray scale masks using this methodology that must be dealt with are minimum feature size and figure count. Figure-count affects mask write time and therefore mask cost, so minimizing figure count helps minimize mask cost. Figure count is determined by the half-tone pitch — the smaller the pitch the greater the number of figures. The optimum pitch from the figure count perspective is the largest pitch that produces smooth resist surfaces. Minimum feature size affects write tool selection. Generally, mask write cost increases as mask minimum feature size decreases, so keeping mask minimum feature size as large as possible helps control mask costs.

The effective mask transmittance is proportional to the ratio of the feature area to the pitch area. If we consider a Clearfield pattern, when the transmittance is high the feature size is a very small opaque square. When transmittance is low, the dark square is almost equal to the pitch leaving a very small clear gap. The mask resolution limits the ability to create transmittances close to zero or 100% especially with small half-tone pitch values. To some extent the resist contrast limits the minimum and maximum transmittance values required. Higher contrast resists show little or no response to low exposure doses and the maximum develop rate is reached at doses well before those represented by 100% transmittance if the exposure dose is chosen carefully. Co-optimizing the half-tone strategy with the selected resist and the exposure dose is therefore necessary to achieve optimum results.

The maximum half-tone pitch that will produce smooth resist surfaces can be estimated by the Rayleigh resolution equation:

$$\text{half-pitch} = k_1 \frac{\lambda}{NA} \quad (1)$$

If we set k_1 to 0.25, generally considered to be the limit of resolution for conventional lithography, for typical *i*-line lithography with λ = 365 nm and NA = 0.5 this yields a pitch equal to the wavelength. This should be considered a good starting point but empirical evaluation of pitches in

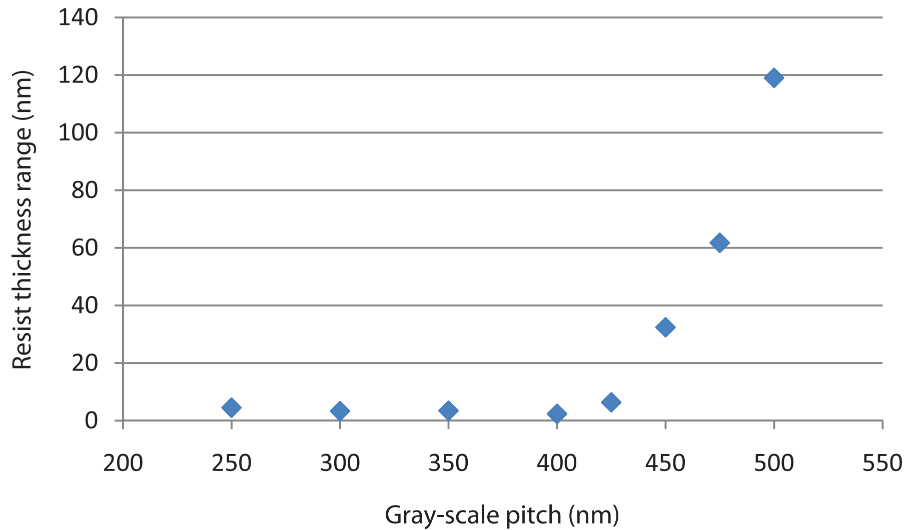


Figure X. Simulated resist surface roughness expressed as the remaining resist thickness range for half-thickness developed resist exposed with a 50% clear half-tone pattern at various half-tone pitches.

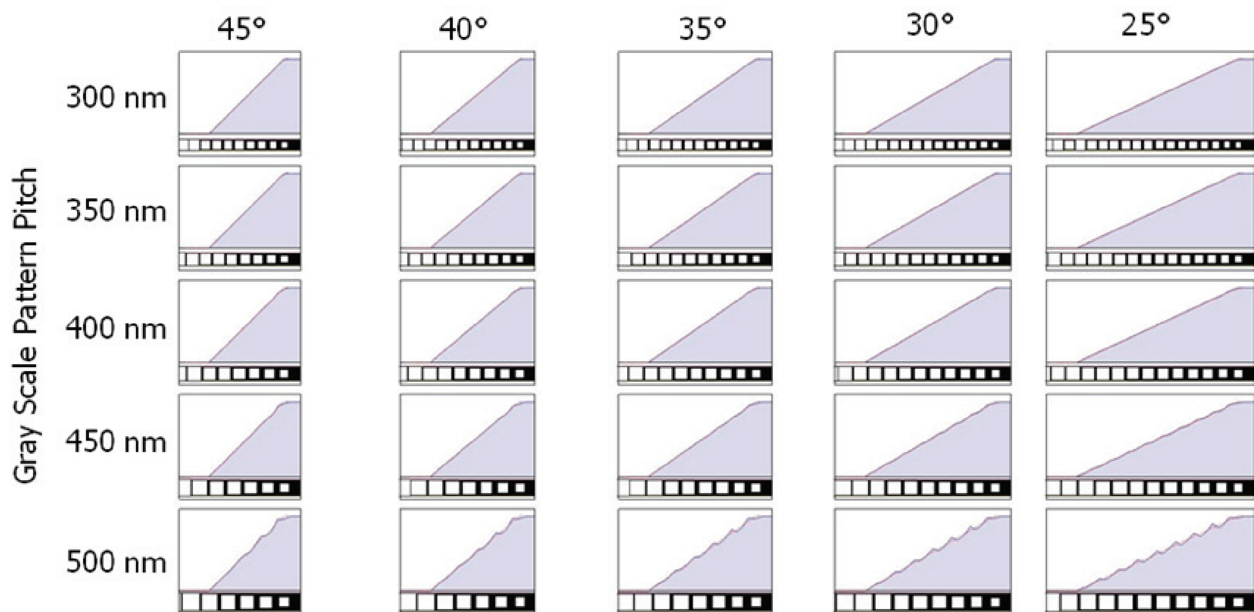


Figure XI. Simulated resist sidewalls with target angles of 25° to 45° at half-tone pitches from 300 nm to 500 nm.

this range is necessary to take into account resist effects.

Determining the required dose profile

The required half-tone feature size to generate a desired resist thickness is dependent on the optical transfer function of the imaging system and the resist response to exposure. The imaging system acts as a low-pass bandwidth filter making the effective transmittance of small features different than that of large features.

The resist response to exposure is not linear. There are inhibition effects that cause the resist dissolution rate to differ at the top surface of the resist compared to the same exposure below the surface. The bulk develop rate increases quickly at a threshold exposure on purpose to provide high develop contrast and therefore vertical resist sidewalls. The develop rate decreases with depth into the resist as a function of resist absorption. Standing wave effects can become apparent near the interface between the resist and the substrate. To account for these effects lithography simulation is used to determine the required half-tone sub-resolution pattern necessary to produce the desired resist sidewall profile.

Litho model calibration

The accuracy of the resist sidewall angle and the straightness of the sidewall depend on the accuracy of the lithography model used to determine the half-tone pattern. Often resist models are available for the specific resists

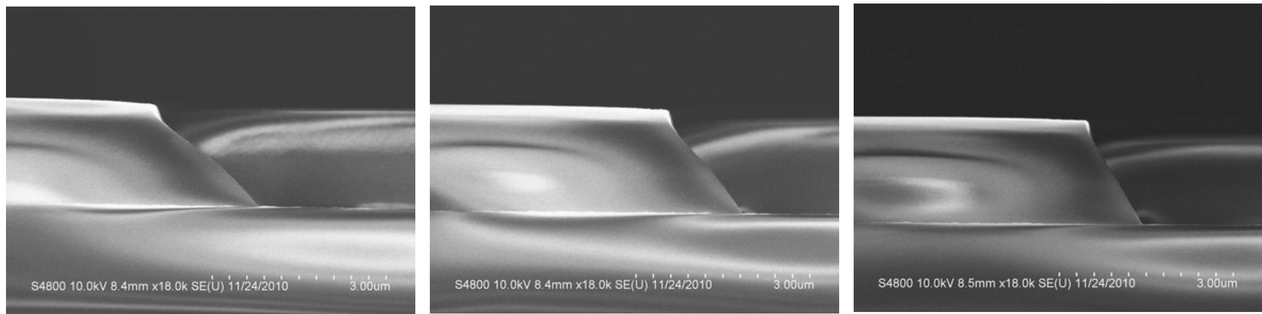


Figure XII. SEM images of resist sidewall profiles with target sidewall angles of 25° (left), 35° (center) and 45° (right) in an initial resist coating thickness of 2 μm. Half-tone pitch to produce the sloped sidewalls is 300 nm. Exposure time is 124 mJ/cm².

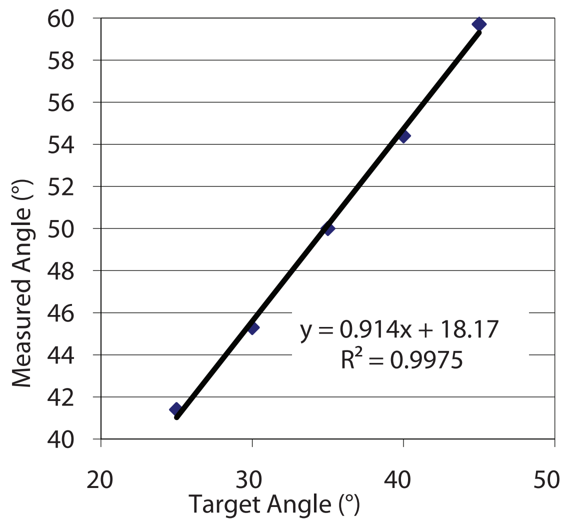


Figure XIII. Correlation of measured to target resist sidewall angle for 300-nm half-tone pitch and 124 mJ/cm² exposure dose.

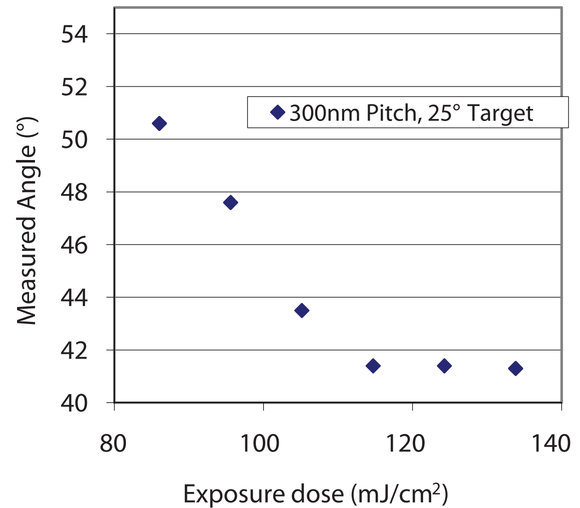


Figure XIV. Measured resist sidewall angle changes with exposure dose but becomes constant at ≥115 mJ/cm².

being used but the process conditions used to generate the model may not be the same or they may be unknown. For this reason we found it necessary to calibrate the resist model specifically to the actual process being used. Ideally we could measure the develop rate curve shown in Figure V and change model parameters to match that curve. This is typically done using specialized develop rate monitor (DRM) tools that measure the resist loss as a function of exposure dose and develop time in situ during resist development. We adopted the "poor man's DRM" method of measuring resist loss as a function of dose after development. We vary dose by using half-tone patterns with different feature sizes on a constant pitch to change the effective transmittance of the mask. By systematically varying each resist parameter and simulating the resist loss as a function of half-tone feature size we were able to determine which simulation parameters were relevant to resist sidewall slope.

We found that the Dill "A", Dill "C", Mth, n, and exposure dose parameters had an effect on the shape of the characteristic curve while Dill "B", PEB time, PEB temperature, resist thickness, relative surface rate, and inhibition depth had little or no effect. Using actual measurements of resist loss as a function of half-tone pattern size we were able to use the Prolith™ AutoTune™ tool to co-optimize relevant model parameters to achieve a match between the model and the actual process.

Automation

The goal of this development project was to produce linear sloped resist regions over a range of angles for two resist thicknesses. For the 2-μm resist thickness, solutions were sought for slopes from 25° to 45° using halftone cell pitches of 300 to 500 nm (wafer scale dimensions). For the 5-μm resist thickness, solutions were sought for slopes from 6° to 14° using cell pitches from 300 to 500 nm. Halftone patterns with both square openings in opaque cells and square opaque regions in clear cells were explored. The width of the pattern was chosen to be large enough so that the resist thickness would be a constant in the middle of the features in the direction orthogonal to the slope direction. In practice this meant using patterns 7 cells high. Fig. VII shows a typical pattern for the 45 deg slope mask using clear openings rather than opaque regions or posts.

For any given cell pitch, the optimization problem becomes one of finding the correct size of the contacts along

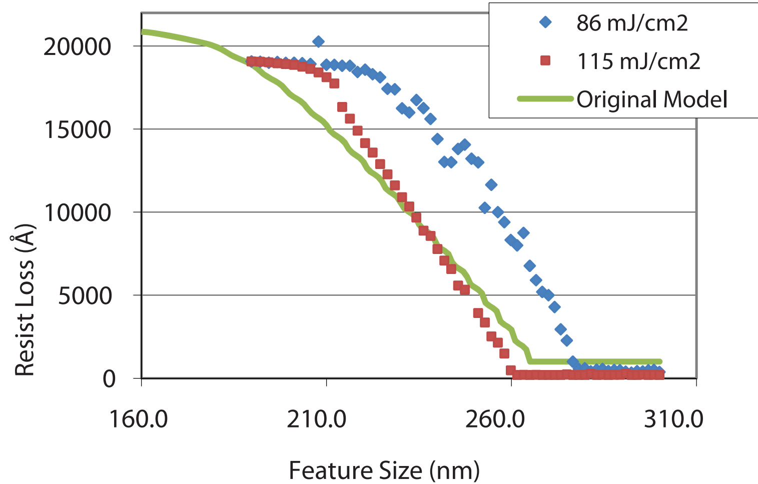


Figure XV. Resist loss characteristic curve showing measured resist loss data from two exposure doses for a clear-field half-tone pattern with a 300-nm half-tone pitch. Simulated results from the model used to generate the half-tone edge slope patterns are also shown.

	Calibrated	Original
Dill "A"	0.49	0.74
Dill "C"	0.0101	0.0126
Relative Surface Rate	0.089	0.3
Inhibition Depth	196.8	0.29

Figure XVI. Significant model parameters affecting model calibration and their values before and after calibration.

the slope such that the simulation of the wafer exposure and resist development produces a linear resist profile of the correct angle. In principle, this problem can be approached manually by calibrating resist loss vs. contact (or post) size for large regions using either empirical data or wafer lithography simulations, and then choosing the size of contact that produces the desired resist thickness at the relevant coordinate. However this approach can neither account for the lithographic contribution from neighboring pixels or the non-linear resist effects from lateral development and surface inhibition effects. This leads to time consuming multiple iterations to find an accurate solution.

This sort of problem is ideally suited to computer automation. It is a multiple variable, constrained global optimization problem. The feature sizes in the halftone array are the variables which must be in a size range governed by the manufacturing limitations of the mask fabrication process and the size of the cell. The merit function to be minimized is a metric of the departure of the simulated resist profile to the target profile. The procedure to be automated is as follows: 1) construct the mask to be evaluated; 2) run a lithography simulation to find the resist profile; 3) calculate merit function based on difference between calculated profile and target; 4) adjust the halftone array to reduce the error; 5) repeat. For our work, we used Prolith™ to model the resist exposure and development, and Mathematica™ for program control of Prolith™ through its .NET interface, to construct the mask, and to calculate the merit function.

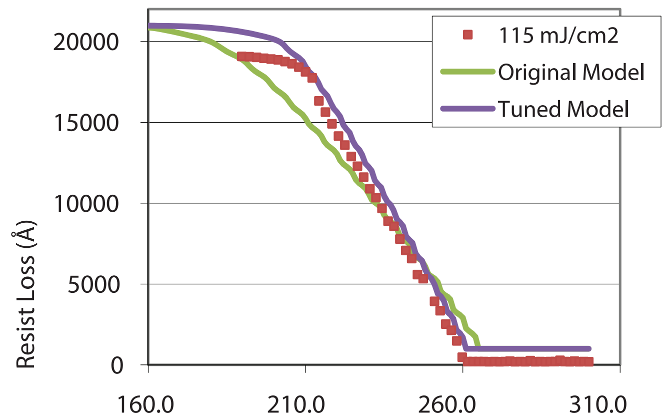


Figure XVII. Comparison of resist loss characteristic curve for measured data, the original model, and the calibrated model.

The merit function was initially chosen as the sum of squares of the differences between simulated and target resist thicknesses using one measurement location per halftone cell. Then one cell was changed at a time and the resist profile recalculated. However this proved too inefficient as many iterations are required for each cell and there are many cells, especially for the shallower slopes. An attempt was made to use the global minimization routines built into Mathematica but these were frustrated by local minima from small differences in the simulated resist profiles and by slow convergence. In the end, a custom algorithm was constructed that used a global merit function *mf*, and a separate error function, e_i for each halftone cell. These are given by the formulas below.

$$mf = \sum_j \left(r(x_j) - \hat{r}(x_j)\right)^2 \quad 2$$

$$e_i = \sum_j e^{-k(x_i - x_j)^2} \left(r(x_j) - r(x_j)\right)^2$$

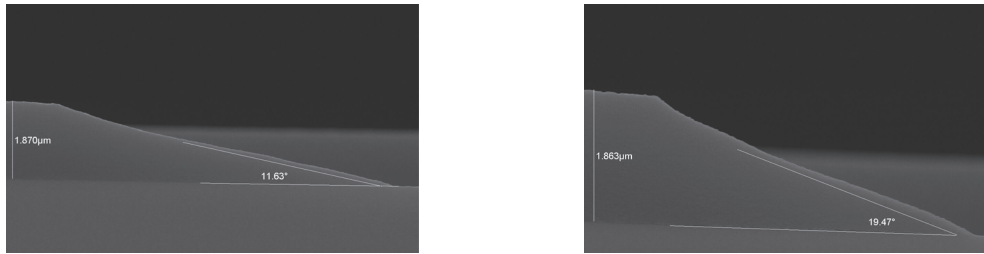


Figure XVIII. Resist edge profiles for target angles of 25° (left) and 30° (right) using the calibrated model.

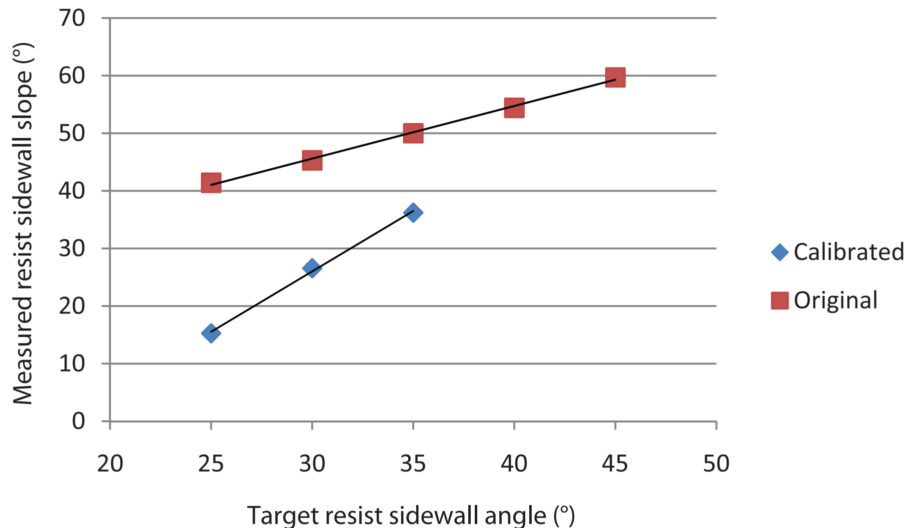


Figure XIX. Comparison of model predictability before and after model calibration.

Here the iterator *i* designates a particular cell, *j* designates a particular measurement point for resist thickness sampling, $r(x_j)$ and $\hat{r}(x_j)$ are the simulated and target resist thicknesses at location x_j, and k is an interaction length constant that determines the range of interaction of a cell. The summation is over all resist thickness measurement points along the row of the array. The exponential weighting reflects the diminishing contribution of cells as they fall outside the optical interaction range. By constructing a separate error function for each cell, the feature size within each cell can be adjusted between each iteration, and convergence significantly sped up. The algorithm is then described by Fig. VIII, where Δe_i is the change in error from the last iteration. The value of N was typically set to 10. The optimizations were run in two phases, first with a step size, Δs, of 0.5 nm and followed by a run at 0.1 nm.

Fig. IX shows the results of four optimizations for 35° slopes in 2 µm of resist. The dots are the target resist thickness at that position. The solid color represents the remaining resist after develop. The optimized halftone features from one of the array rows are drawn at the bottom of each graph to the scale of the axes coordinates. Fig. IX-a shows the result for contacts on a cell pitch of 300 nm; Fig. IX-b shows the same optimization for a cell pitch of 500 nm. Fig IX-c and –d repeat the exercise for features of the opposite tone. The 300-nm pitch solutions produce a good match to the target; the 500-nm pitch is within the spatial bandwidth of the optics and the individual cells start to resolve resulting in a wavy appearance of the slope. The algorithm has proven to be quite robust over a range of 2 to 5 µm of resist thicknesses, a range of 6° to 45° of resist slope and the use of both tones of cells. The accuracy is limited primarily by the calibration of the resist model used in the simulation. In this work we explored creating linear resist gradients exclusively, but the algorithm has clear extension to 2D non-linear surfaces, such as lenslets as well.

Experimental

Our primary goal was to produce resist sidewall angles of 45° in a 2-µm resist coating. Also included in the project was the desire to produce extremely shallow angles of ~10° in a 5-µm resist coating. The general steps we followed to achieve this were:

- Use a generic lithographic model to predict the optimum half-tone pitch
- Create half-tone test patterns using the generic lithographic model
- Generate a test photomask with calibration patterns necessary to calibrate a resist model

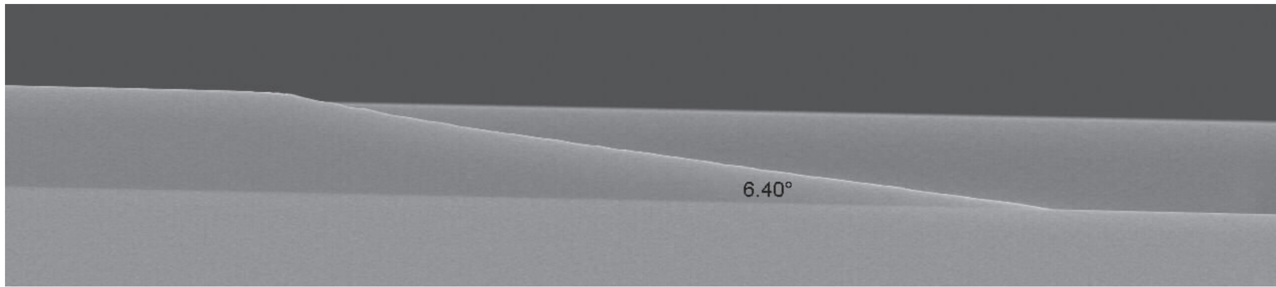


Figure XX. Resist edge profile with measured slope of 6.4° degrees with a 6° target.

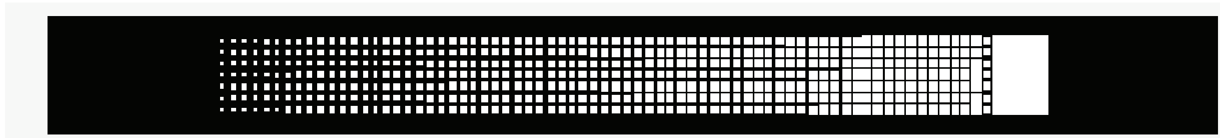


Figure XXI. Half-tone mask pattern used to create resist image shown in figure XX.

- Print wafers and measure resist loss as a function of half-tone % clear area
- Evaluate resist sidewall profiles from first-generation half-tone test patterns
- Calibrate a resist model
- Generate final half-tone patterns
- Apply to product data

The Prolith™ lithography simulator was used to set up a model of the process including the optics, substrate films, and photoresist coating and development. The resist model was chosen from those supplied with the simulator to best match the actual resist. Using a parametric 2-dimensional contact array test pattern we measured the resist surface roughness by simulating a 50% clear half-tone pattern at a range of half-tone pitches. The exposure dose was selected to cause the resist to be developed about halfway through the 2-μm initial thickness. The results are shown in figure X. Surface roughness is minimized at pitches ≥400 nm. With the chosen illuminator conditions of $\lambda = 365$ nm, NA = 0.5, $\sigma = 0.68$ the k_1 value (see equation I) is 0.27, confirming our initial estimate.

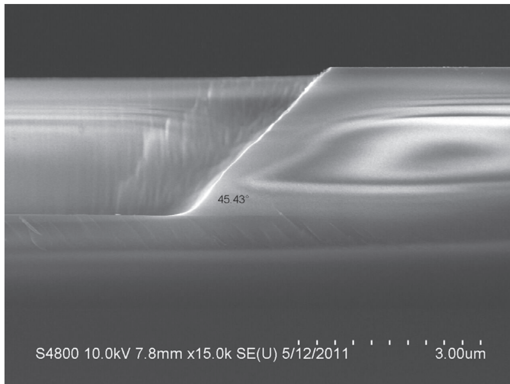
Having determined the range of half-tone pitches most likely to provide a smooth resist surface we then created two test patterns. The first test pattern, intended to measure the resist loss characteristic curve to calibrate the resist model, consisted of 200-μm square regions of half-tone pattern with % clear values from zero to 100% in 1% increments with half-tone pitches of 200 nm to 600 nm in 50-nm increments. This test pattern was printed on a photomask in both normal, or dark-field (clear half-tone features on an opaque background) and reverse, or clear-field tones (opaque halftone features on a clear background). Wafers coated with both 2-μm and 5-μm coatings of TOK THMR-ip5668 were exposed with this mask and resist thickness loss measurements were made. The second test pattern consisted of line patterns with half-tone patterns applied to the line-ends to produce resist sidewall angles of 25° to 45° in the 2-μm resist and from 6° to 14° in the 5-μm coating. The gray-scaling was applied using the automation methods described earlier in this document. In this document we will focus on the 2-μm resist results with occasional reference to the 5-μm results when relevant.

While the initial assessment of the maximum pitch that results in acceptable surface roughness suggested that half-tone pitches as large as 400 nm are acceptable, which is also supported by observing simulated results of edge slope test patterns (figure XI), surface roughness does not tell the entire story. During the optimization of the half-tone patterns to produce the edge-slope test patterns it became apparent that the half-tone pitch also affects the ability to control the edge slope at the top and bottom of the resist. This was confirmed with observations of SEM images of resist and to maximize the opportunities for success we arbitrarily selected the 300-nm pitch for the remainder of the project.

Initial sidewall results were promising. Resist sidewalls (again focusing on the 300-nm half-tone pitch) were fairly straight with sharp transition to the substrate. The sidewall straightness extends for most of the resist thickness, with some change in slope at the very top surface of the resist. Some curvature of the sidewall is evident for the shallowest target edge slopes.

We observed a linear relationship between measured and target sidewall angles but we did not accurately predict the target sidewall angle. The slope of the relationship is 0.914 and the offset is 18.2°. The exposure dose is expected to influence sidewall angle based on our model parameter sensitivity analysis (figure VI). We examined resist sidewall angle as a function of exposure dose (figure XIII) and observed that at low doses the resist sidewall angle is indeed sensitive to exposure dose but at an exposure time of 115 mJ/cm^2 and above the resist sidewall angle becomes constant (figure XIV). This implies better process control at higher doses.

Measurements of resist loss as a function of half-tone



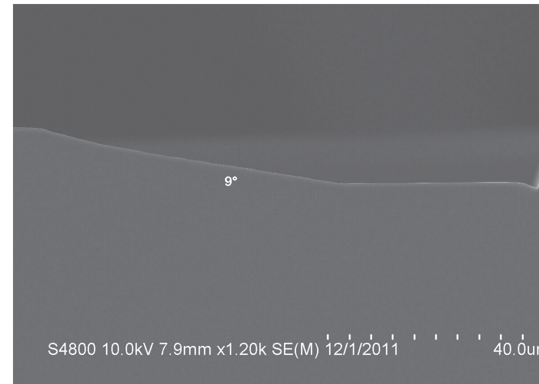


Figure XXII. SEM cross section images of SiO_2 profile(left) and of Si profile (right) using sloped photoresist followed by dry etch process on a full 8-inch wafer.

feature size were compared with simulation to test how well the generic resist model matched the actual process. Figure XV shows results from two exposure times compared to simulated results. The test pattern used is a clear-field half-tone pattern with a 300-nm half-tone pitch. Data from the lower exposure time exhibits noise and is in the range of exposure dose where sidewall angle changes rapidly with dose. Data from the higher exposure time has low noise and is a better match to the simulated results, however the slope is different and the response for small feature sizes (high intensity for a clear-field pattern) is significantly different.

To resolve the differences between predicted and measured results we calibrated the resist model by co-optimizing resist parameters to match the measured resist loss characteristic curve for the 115 mJ/cm^2 exposure dose using the Prolith™ AutoTune™ tool. As predicted by our original model parameter sensitivity tests the Dill "A" and Dill "C" parameters had significant impact on model accuracy. We did not expect relative surface rate or inhibition depth to have a significant impact on the model but in fact both did and the change in value from the original to the calibrated model was large.

After model calibration the slope and response at low intensity matches measured data much more closely.

New half-tone test patterns were generated using the calibrated resist model and a new test mask was generated to evaluate the change in resist model. Improvement in the resist edge straightness was observed. Figure XVIII shows resist edge profiles for target angles of 25° (left) and 30° (right) using the calibrated model. The predictability of the resist sidewall angle changed but is still not accurate. The linearity remains acceptable but the change in the model caused the slope to more than double. Still, for the range of angles of interest this is still a better result than the original model. Figure XVI shows the change in edge slope angle predictability of the new model.

Interestingly, the prediction of very shallow angles in thicker resist is better using the same calibrated model. Figure XVIX shows a resist edge slope measuring 6.4°. The target angle was 6°. Similar predictability was achieved with target angles up to 14°. The half-tone mask pattern used to create the angled resist profile is shown in figure XX.

In order to form a required angle in the substrate, different parameters should be considered:

- Photoresist slope angle
- Dry etch chemistry
- Photoresist:substrate achievable selectivity

Figure XXII (left) shows a 45º slope in SiO_2. The SiO_2 dry etch process was done on a TEL Unity 2 200-mm tool using C_xF_y/O_2 based chemistry. Since the tool was limited to 1:1.8 Photoresist:SiO_2 selectivity, a 26º resist slope angle was required.

Figure XXII (right) shows a 9º slope in silicon. The silicon dry etch process was done on a Hitachi M511AE 200-mm tool using Cl_2/O_2 chemistry. With a photoresist:Si selectivity of 1:2, a 4º resist slope was required. For 200-mm wafers the cross wafer non-uniformity was ±0.5º for photoresist profiles and ±1º for SiO_2 and silicon profiles.

Discussion

One of the challenges that must be overcome to enable wide-spread use of half-tone gray-scale techniques in production is the application of the half-tone pattern to design data. For simple patterns it is possible to manually "cut and paste" an optimized half-tone pattern to design elements where sloped resist profiles are desired. For more complex patterns and to address certain two-dimensional shapes, and to deal with interactions between closely spaced patterns an automated approach is desirable. One method we have found promising is the use of a Design Rule Check (DRC) tool. DRC tools like Mentor Graphics Calibre DRC have evolved to be powerful geometric processing engines that can be used to transform design data using rules that select, alter, create, and delete design data. By writing rules that select edges where sloped resist profiles are desired and using the DRC tool box to create the half-tone patterns at these edges it is possible to fully automate the generation of half-tone gray-scale patterns for arbitrary patterns. This allows data for gray-scale masks

to be prepared in the same data processing flow used for standard masks.

More work is necessary to fully understand resist model calibration. The "poor-mans DRM" method we used could be improved by using multiple develop steps to fully capture the resist development behavior.

We also found some evidence that the substrate materials were affecting prediction of sidewall slope, suggesting that we need to pay more attention to calibration of substrate thickness and refractive index as part of model calibration.

Conclusions

We have demonstrated the feasibility of manufacturing programmed sloped resist sidewalls using half-tone gray-scale masks created on standard COG mask material. We have described the concepts used to calibrate a resist model, to optimize the half-tone pattern size characteristics, and to generate the gray-scale pattern using automation combined with resist simulation. We have shown how these half-tone gray-scale patterns can be used to transfer resist edge slopes to SiO_2 and silicon substrates.

References

[1] N. Izhaky, M. T. Morse, S. Koehl, O. Cohen, D. Rubin, A. Barkai, G. Sarid, R. Cohen, and M. J. Paniccia, "Development of CMOSCompatible Integrated Silicon Photonics Devices," *J. Sel. Topics Quantum Electron,* VOL. 12, NO. 6, 1688-1698, (2006).

[2] P. Cheben, B. Lamontagne, E. Post, S. Janz, D.-X. Xu, and A. Delage, "Out-of-Plane Total Internal Reflection Coupling Mirrors in Silicon-on-Insulator Ridge Waveguides," Group IV Photonics, 2006. 3rd IEEE International Conference on , vol., no., pp.146-148

[3] Fengtao Wang, Fuhan Liu, and A. Adibi, "45 Degree polymer micro-mirror integration for board-level three-dimensional optical interconnects," Electronic Components and Technology Conference, 1842-1845, (2009).

[4] Chun-Wei Liao, Yao-Tsu Yang, Sheng-Wen Huang, and M.-C.M. Lee, "Fiber-Core-Matched Three-Dimensional Adiabatic Tapered Couplers for Integrated Photonic Devices," *Journal of Lightwave Technology,* vol.29, no.5, 770-774, (2011).

[5] S. C. Saha, H. Sagberg, E. Poppe, G. U. Jensen, T. A. Fjeldly, and T. Saether, "Tuning of resist slope with hard-baking parameters and release methods of extra hard photoresist for RF MEMS switches", *Journal of Sensors and Actuators A,* 143,452?461, (2008).

[6] R. Dammel, "Diazonapthoquinone-based Resists", *SPIE Optical Engineering Press*, Bellingham, (1993).

[7] P. Rai-Choudhury, "Handbook of Microlithography, Micromachining, and Microfabrication Volume I: Microlithography", *SPIE Optical Engineering Press,* Bellingham, 330-345, (1997).

[8] J. R. Smith, P. Graat, D. A. Bonnell, and R. H. French, "Relation between Local Composition, Chemical Environment and Phase Shift Behavior in Cr-Based Oxycarbonitride Thin Films", *MRS Proceedings,* (2001).

[9] Walter Daschner, Pin Long, Robert Stein, Chuck Wu, and S. H. Lee, "General aspheric refractive micro-optics fabricated by optical lithography using a high energy beam sensitive glass gray-level mask", *J. Vac. Sci. Technol.* B 14(6), 3730-3733, (1996).

N • E • W • S

Sponsorship Opportunities

Sign up now for the best sponsorship opportunities

Photomask 2012 —
Contact: Lara Miles, Tel: +1 360 676 3290; laram@spie.org

Advanced Lithography 2013 —
Contact: Teresa Roles-Meier, Tel: +1 360 676 3290; teresar@spie.org

Advertise in the BACUS News!

The BACUS Newsletter is the premier publication serving the photomask industry. For information on how to advertise, contact:

Lara Miles
Tel: +1 360 676 3290
laram@spie.org

BACUS Corporate Members

FUJIFILM Electronic Materials U.S.A., Inc.
Gudeng Precision Industrial Co., Ltd.
HamaTech APE GmbH & Co. KG
Hitachi High Technologies America, Inc.
Ibss Group, Inc.
JEOL USA Inc.
KLA-Tencor Corp.
Max Levy Autograph, Inc.
Mentor Graphics Corp.
Mentor Graphics Corp.
Molecular Imprints, Inc.
Plasma-Therm LLC
Raytheon ELCAN Optical Technologies
XYALIS

Industry Briefs

Photomask Market to Grow 7% in 2012, SEMI Says

by **Dylan McGrath,** EETimes

The worldwide semiconductor photomask market is expected to be worth $3.35 billion in 2012, up 7 percent from 2011, according to the fab tool vendor trade group SEMI. It is expected to set a new record high this year for the third consecutive year, followed by the growth by another 4 percent next year and an additional 3 percent in 2014, SEMI said.

Growth in the semiconductor photomask market is being driven by migration to advanced technology feature sizes (less than 65 nm) and increased manufacturing in Asia-Pacific. Taiwan became the largest photomask regional market, surpassing Japan in 2010, and is expected to remain the largest market for the duration of the forecast, SEMI said. The mask market is becoming increasingly capital intensive. 2011 was a record year for mask/reticle making equipment, with sales growing 36 percent year-over-year from the previous record year of 2010 to reach $1.11 billion. As the capital intensiveness of the photomask industry increases, captive mask shops are increasing their market share of the total mask market, now representing 40 percent of the market, up from 30 percent in 2006, SEMI said.

Microsoft Joins Micron Memory Cube Effort

by **Rick Merritt,** EETimes

Microsoft became the seventh core member of the Hybrid Memory Cube Consortium led by Micron and Samsung, a sign of the broad technical implications for the concept of 3-D memory chip stacks. Microsoft's participation signals the potential of the Memory Cube to drive changes in the traditional memory hierarchy and systems software for computers and networks. Micron has proposed a Cube of stacked memory die that includes a logic layer to optimize the placement of and access to memory, potentially handling functions carried out by memory controllers typically integrated in server and network processors today.

"The compilers and the whole system stack can be optimized [because] we can put additional functions out in our logic layer," said Mike Black, senior manager of business development for the Hybrid Memory Cube at Micron. "Having the logic layer manage some of your memory lets you localize data movement patterns that traditionally would be in systems memory or elsewhere," he said.

The Cube "represents a major step forward in the direction of increasing memory bandwidth and performance, while decreasing the energy and latency for moving data between the memory arrays and the processor cores," said KD Hallman, general manager of Microsoft's strategic software/silicon architectures group, speaking in a press statement. "Harvesting this solution for various future systems could lead to better and/or novel experiences," she added.

Major Semiconductor Makers Order EUV Lithography Metrology Tool from Carl Zeiss

Carl Zeiss Semiconductor Metrology Systems (SMS) Division won orders for its extreme ultraviolet lithography (EUVL) actinic aerial image metrology system, AIMS EUV, from 2 of the 4 members of SEMATECH's EMI partnership (GLOBALFOUNDRIES, Intel, Samsung Electronics, TSMC). The tool allows semiconductor makers to review defects in advanced masks needed for EUVL.

The remaining 2 EMI members are expected to place orders in accordance with their agreed-upon slot assignments, noted Dr. Oliver Kienzle, managing director of Carl Zeiss SMS. Carl Zeiss SMS developed the AIMS EUV tool in cooperation with the scanner optics department of Carl Zeiss SMT, Lithography Optics (LIT), and external partners.

Kienzle notes that the metrology tool wins "confirm the relevance of EUV technology for the industry." Metrology tools for EUVL are an industry need that could benefit from governments' support, asserted Dan Armbrust, president & CEO of SEMATECH, at the SEMI Industry Strategy Symposium (ISS) 2011. The AIMS EUV platform enables development and manufacturing of defect-free EUVL masks supporting the 22nm half-pitch (hp) technology node, with extendibility to 16nm hp. A first production-ready platform is scheduled for delivery in Q3 2014.

Micron Wins Exclusive Right with 200 Bln Yen Offer - Source

by **Maki Shiraki**

- SK Hynix dropped out of bidding race
- Elpida seeking buyer after filing for bankruptcy

Micron Technology won the right to negotiate exclusively to buy Elpida Memory Inc after offering more than 200 billion yen ($2.5 billion) for the failed Japanese chipmaker, according to a source with direct knowledge of the deal that would more than double the U.S. company's global market share. By acquiring Elpida, Micron would boost its market share to 25 percent, surpassing South Korea's SK Hynix and becoming the second-biggest maker of DRAM memory chips used in personal computers, according to U.S. technology research firm IHS iSuppli. Samsung Electronics is the largest.

"The most important thing is, after this deal you end up with three major players in DRAM, which makes it a more rational market, with more rational capital decision-making and probably more stability from a pricing standpoint," Warden said. A growing preference for tablets has dampened demand for memory chips used in PCs, and growing costs to implement new technology has added to pressure faced by dynamic random-access memory (DRAM) makers.

Join the premier professional organization for mask makers and mask users!

About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

Individual Membership Benefits include:

- Subscription to BACUS News (monthly)
- Complimentary Subscription *Semiconductor International* magazine
- Eligibility to hold office on BACUS Steering Committee

spie.org/bacushome

Corporate Membership Benefits include:

- Three Voting Members in the SPIE General Membership
- Subscription to BACUS News (monthly)
- One online SPIE Journal Subscription
- Listed as a Corporate Member in the BACUS Monthly Newsletter

spie.org/bacushome

Calendar

2012

SPIE Photomask Technology

11-13 September 2012
Monterey Marriott and
Monterey Conference Center
Monterey, California, USA
spie.org/pm

Late abstract submissions may be considered by the Chairs. Please send to Pat Wight at patw@spie.org.

2013

Advanced Lithography

24-28 February 2013
San Jose Convention Center and
San Jose Marriott
San Jose, California, USA
spie.org/al

SPIE is the international society for optics and photonics, a not-for-profit organization founded in 1955 to advance light-based technologies. The Society serves nearly 225,000 constituents from approximately 150 countries, offering conferences, continuing education, books, journals, and a digital library in support of interdisciplinary information exchange, professional growth, and patent precedent. SPIE provided over $2.5 million in support of education and outreach programs in 2011.

International Headquarters
P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 360 676 3290
Fax: +1 360 647 1445
help@spie.org • SPIE.org

Shipping Address
1000 20th St., Bellingham, WA 98225-6705 USA

SPIE Europe
2 Alexandra Gate, Ffordd Pengam, Cardiff,
CF24 2SA, UK
Tel: +44 29 2089 4747
Fax: +44 29 2089 4750
spieeurope@spieeurope.org • www.spieeurope.org

You are invited to submit events of interest for this calendar. Please send to lindad@spie.org; alternatively, email or fax to SPIE.