PHOTOMASK

BACUS—The international technical group of SPIE dedicated to the advancement of photomask technology.

BACUS NEWS
JUNE 2011
VOLUME 27, ISSUE 6

Paper 7970-8

Progress in Mask Replication using Jet and Flash Imprint Lithography

Kosta S. Selinidis, Cynthia B. Brooks, Gary F. Doyle, Laura Brown, Chris Jones, Joseph Imhof, Dwayne L. LaBrake, Douglas J. Resnick, and **S. V. Sreenivasan,** Molecular Imprints, Inc, 1807-C West Braker Lane, Austin, TX 78758 USA

Abstract

The Jet and Flash Imprint Lithography (J-FIL™) process uses drop dispensing of UV curable resists to assist high resolution patterning for subsequent dry etch pattern transfer. The technology is actively being used to develop solutions for memory markets including Flash memory and patterned media for hard disk drives. It is anticipated that the lifetime of a single template (for patterned media) or mask (for semiconductor) will be on the order of 10^4 – 10^5 imprints. This suggests that tens of thousands of templates/masks will be required to satisfy the needs of a manufacturing environment. Electron-beam patterning is too slow to feasibly deliver these volumes, but instead can provide a high quality "master" mask which can be replicated many times with an imprint lithography tool. This strategy has the capability to produce the required supply of "working" templates/masks. In this paper, we review the development of the mask form factor, imprint replication tools and processes specifically for semiconductor applications.

The requirements needed for semiconductors dictate the need for a well defined form factor for both master and replica masks which is also compatible with the existing mask infrastructure established for the 6025 semi standard, 6" x 6" x 0.25" photomasks. Complying with this standard provides the necessary tooling needed for mask fabrication processes, cleaning, metrology, and inspection. The replica form factor has additional features specific to imprinting such as a pre-patterned mesa. A Perfecta™ MR5000 mask replication tool has been developed specifically to pattern replica masks from an e-beam written master. The system specifications include a throughput of four replicas per hour with an added image placement component of 5nm, 3sigma

Continues on page 3.

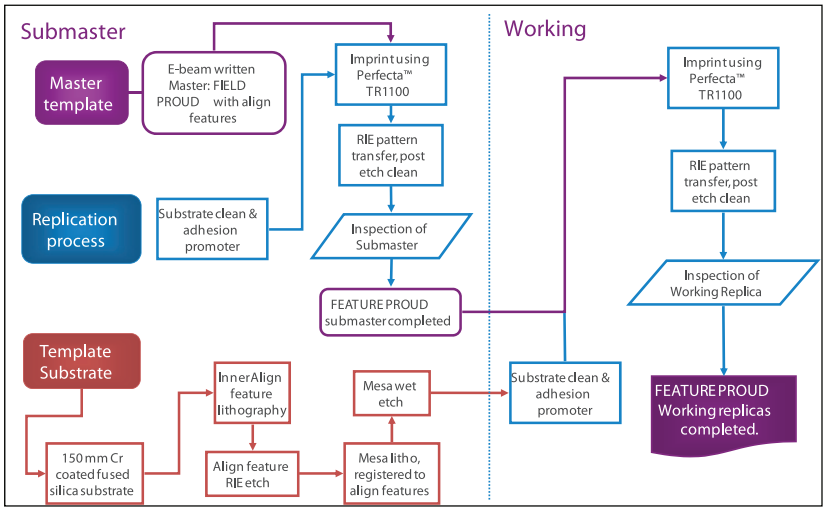


Figure 1. Process flow for creating both submaster and working replica templates for patterned media.

TAKE A LOOK INSIDE:

SPIE

EDITORIAL

The 7-year (p)itch

Artur Balasinski, Cypress Semiconductor Corp.

Some forecasts about the semiconductor industry seem to make more sense than others. Compare these: (1) The number of devices on a chip would double every 2 years [yes, Moore's law], (2) Total IC market value would exceed the Total goods market value [a joke at one of the SPIE sessions], and (3) The end of the roadmap is 7 years away [borrowed from Marilyn M. movie -? - e.g. at EUV workshop in 2009]. One may say, because of (1), we would have (2), if it were not for (3). I heard prediction (3) last month again, coming from a big foundry, so I keep asking myself, is it for real this time or are we really going into a crazy future with more ICs than all manufactured goods, ICs including?

One way to answer this is to look at the roadmap in question, i.e., the ITRS. It includes a spreadsheet with the dates out all the way to 2024, so it doubles the 7-year (p)itch, except there is not a single non-red field past the year 2017, meaning we have no clue what to do. This sounds ominous but at least the time axis is there and we should be used to a lot of red fields anyway. I tried to do a quick check, but the ITRS did not let me go any further back than to 2009. Back then, the Roadmap featured a dedicated chapter on mask making with the benchmark 22 nm process. Mask was recognized as challenge, especially that "the mask industry has experienced numerous consolidations and partnerships" [we know that] and "the mask specifications have increased more quickly than the half-pitch designated by the roadmap, driven by the MPU gate line width (post-etch) and the greater mask error enhancement factor (MEEF) associated with low k1 lithography. The need for 2X patterns on the mask (sub-resolution enhancement) for double patterning demands mask registration specifications that far outpace the half-pitch in the roadmap." So far, no mention about the EUV or any other preferred technology, but importantly, progressive defect formation has already been recognized a greater problem with deposits on masks after many wafers are exposed, meaning perhaps that there is future for bigger mask fields (demanding fewer exposures). This has caused a scary, 13X increase in the reworking of masks at 193 nm compared to the 248 nm technology. Mask damage from electrostatic discharge (ESD) is expected to be more problematic when CDs become smaller and more critical, in addition to electric field migration (EFM) shown to change CD sizes. One may sum up, this picture has been accurate back in 2009 as it is accurate right now. Think "product cycletime increase."

In contrast, the latest, 2010 ITRS edition does not seem to care about masks all that much, perhaps because it goes down to predicting CDs of 16 nm, a 50% area reduction in a year, far more aggressive than dictated by the forecast (1). This spurs so many "difficult challenges" to the NGL due to the incomprehensible, non-incremental improvements, despite "vast technology options," that the mask related issues blend in. In the order of difficulty, defect free masks, source brightness, and optimal resist system are considered the three keys to the 16 nm EUV, followed closely by the higher than ever NA for the exposure with higher incidence angles to require thinner absorber thicknesses and flare mitigation. Come to SPIE/BACUS Photomask Symposium in September to discuss all that!

But the ITRS roadmap also seems to reconcile the apparent conflicts among the forecasts (1), (2), and (3), by saying that, "by the end of the next decade it will be necessary to augment the capabilities of the CMOS process by introducing multiple new devices to realize properties beyond the CMOS including heterogeneous integration either at the chip level or at the package level." So we may conclude that, (1) we will continue the doubling up, (2) we will grow the market value beyond the wildest dreams, and (3) the technology roadmap may deviate from the beaten track, but so what. Let's come back in 7 years and check it out.

BACUS

N • E • W • S

BACUS News is published monthly by SPIE for BACUS, the international technical group of SPIE dedicated to the advancement of photomask technology.

Managing Editor/Graphics Linda DeLano
Advertising Teresa Roles-Meier
BACUS Technical Group Manager Pat Wight

SPIE

P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 360 676 3290 or +1 888 504 8171
Fax: +1 360 647 1445
SPIE.org
customerservice@spie.org

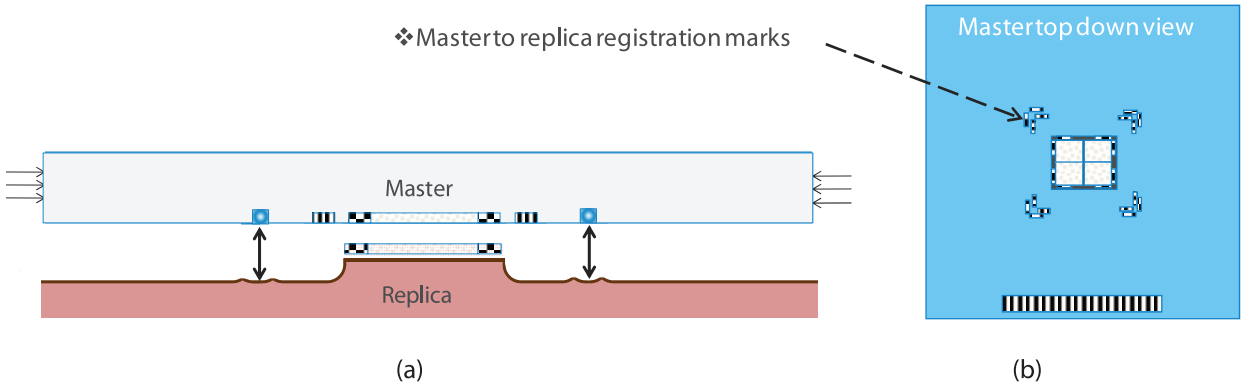


Figure 2. a) A schematic of the process used to align the master mask to the replica mask blank. Registration marks outside of the active field aid in the alignment of the field to the mesa on the replica. b) Schematic illustration of the patterned master mask.

MR5000 Specifications

- Throughput: 4 replicas/hr
- Substrate size: 6″x6″x0.25″ (6025)
- Nominal Field size:33x26 mm
- RTLU: < 4 nm, 3 σ
- Added CDU < 1 nm, 3 σ
- Add image placement: ≤5 nm 3 σ
- Environment: ISO class 2

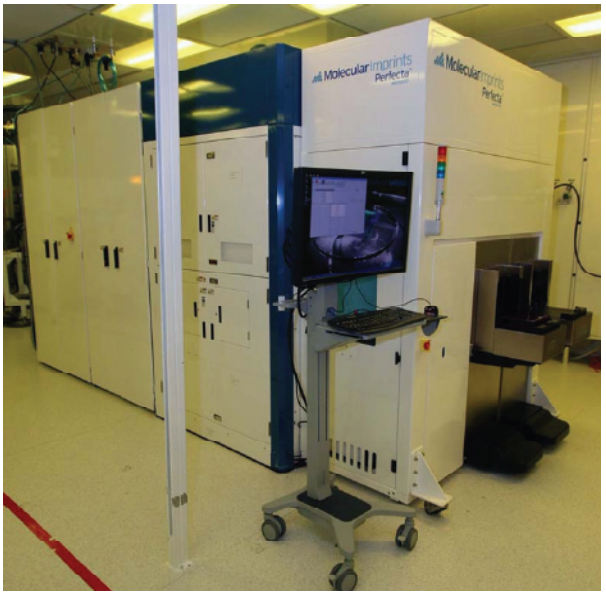


Figure 3. The MR5000 mask replication tool and a list of tool specifications.

and a critical dimension uniformity error of less than 1nm, 3sigma. A new process has been developed to fabricate replicas with high contrast alignment marks so that designs for imprint can fit within current device layouts and maximize the usable printed area on the wafer. Initial performance results of this marks are comparable to the baseline fused silica align marks.

1. Introduction

The Jet and Flash Imprint Lithography (J-FIL™) process uses drop dispensing of UV curable resists to assist high resolution patterning for subsequent dry etch pattern transfer. The technology is actively being used to develop solutions for memory markets including Flash memory and patterned media for hard disk drives. It is anticipated that the lifetime of a single template (for patterned media) or mask (for semiconductor) will be on the order of 10^4 – 10^5 imprints. This suggests that tens of thousands of templates/masks will be required to satisfy the needs of a manufacturing environment. Electron-beam patterning is too slow to feasibly deliver these volumes, but instead can provide a high quality “master” mask which can be replicated many times with an imprint lithography tool.

Previous work on patterned media for hard drives has demonstrated the feasibility of replicating templates for both discrete track recording and bit patterned media. A typical process flow is shown in Figure 1. Replication of the master was conducted using a Perfecta 1100TR system. The TR1100 uses Molecular Imprint’s Jet and Flash™ Imprint Lithography (J-FIL™) technology. The system platform is based on three previous generations of Imprio tools and was specifically designed to produce templates meeting the requirements for patterned media disk imprinting systems. The TR1100 system capabilities include micron level alignment, template automation, and the ability to handle 150mm fused silica substrates. The system can produce approximately ten templates per hour, more than two orders of magnitude more productive than today’s leading edge e-beam template writers.

For the case of the semiconductor market, a variety of feature types must be resolved, although for most memory applications, the dominant feature set consists of 1:1 line/space patterns for critical front-end layers, particularly Flash.

In the case of Flash memory, the most aggressive production

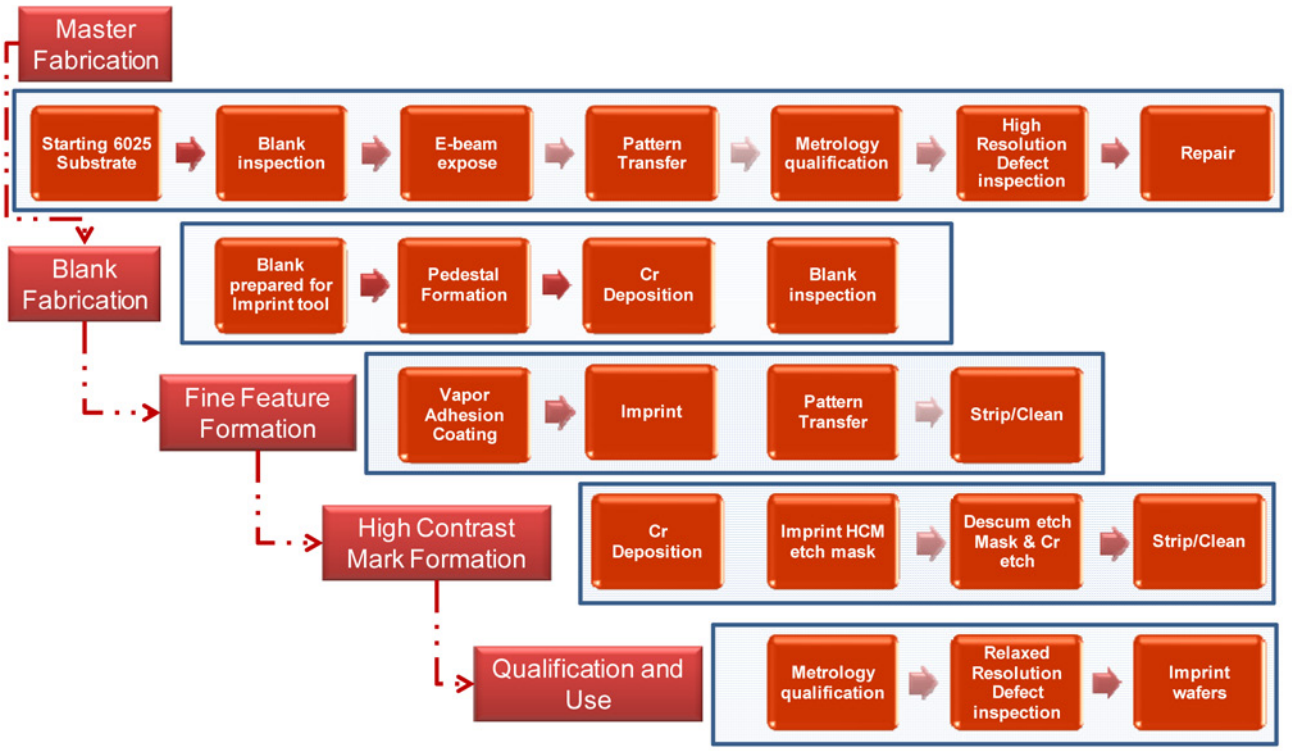


Figure 4. Replica process flow, including steps for master fabrication, replica blank formation, fine feature patterning, high contrast mark definition and replica mask qualification and use.

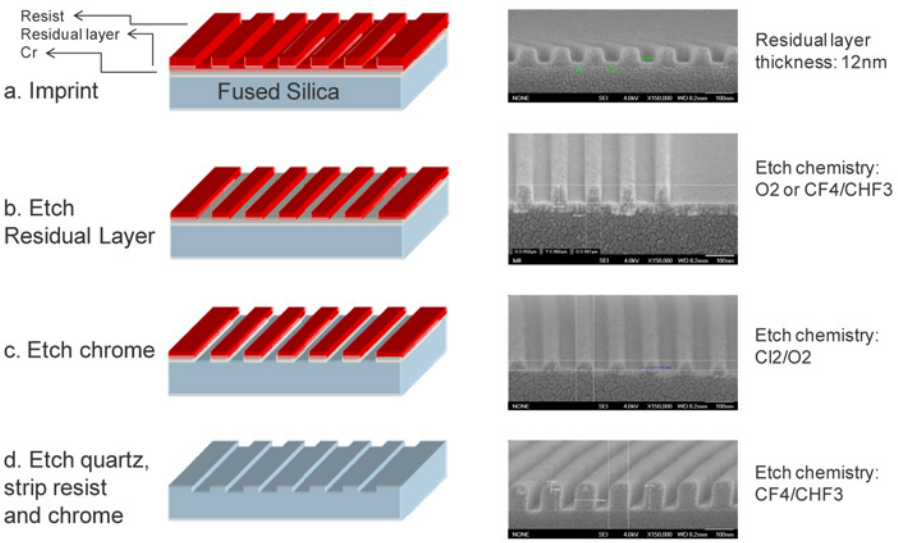


Figure 5. Key processing steps necessary for replica pattern transfer.

designs are now pushing to half pitches of 25nm. For such designs, mask critical dimension uniformity (CDU) must be less than 10 percent of the minimum device half pitch, mask image placement must be below 5nm and defectivity of the mask is required to be less than 1 defect/cm^2. In this paper, we review the development of the mask form factor, the imprint tool, the imprint process and pattern transfer specifically for semiconductor replica masks.

The requirements needed for semiconductors dictate the need for a well defined form factor for both master and replica masks which is also compatible with the existing mask infrastructure established for the 6025 semi standard, 6" x 6" x 0.25" photomasks. Complying with this standard provides the necessary tooling needed for mask fabrication processes, cleaning, metrology, and inspection. The replica form factor has additional features specific to imprinting such as a pre-patterned mesa. A Perfecta™ MR5000 mask replication tool has been developed specifically to pattern replica masks from an e-beam written master. The system specifications include a throughput of four replicas per hour with an added image placement component of 5nm, 3sigma and a critical dimension uniformity error of less than 1nm, 3sigma. A new process has been developed to fabricate replicas with high contrast alignment marks so that designs for imprint can fit within current device layouts and maximize the usable printed area on the wafer. Initial performance results of this marks are comparable to the baseline fused silica align marks.

2. Mask Details

a. Mask form factor

The 6025 master mask form factor allows mask shops to use the identical tooling currently used for resist coating, writing, patterning pattern transfer, metrology, inspection and repair. Unlike standard photomasks which required the majority of the mask surface to achieve a 4x reduction, imprint replication pattern transfers exactly and thus only requires very middle of the mask for device features. The additional space around the periphery of the device patterns

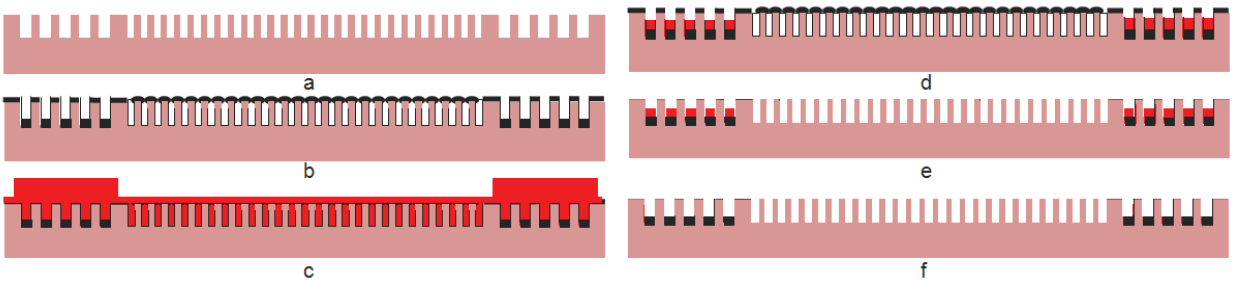


Figure 6. High contrast mark process flow: a) patterned replica mask b) Thin chromium deposition c) Imprint step to isolate the alignment features d) Resist etchback e) Chromium wet etch f) Resist strip.

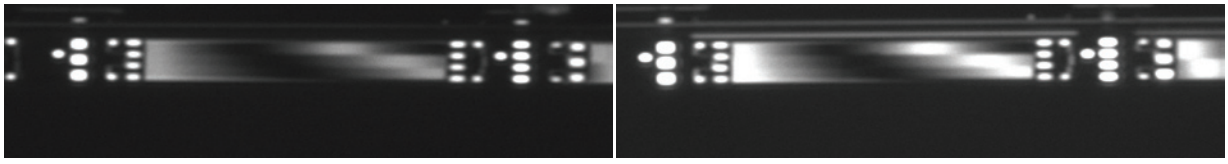


Figure 7. Moiré signal intensity using a thin (10nm) and thick (30nm) chromium layer.

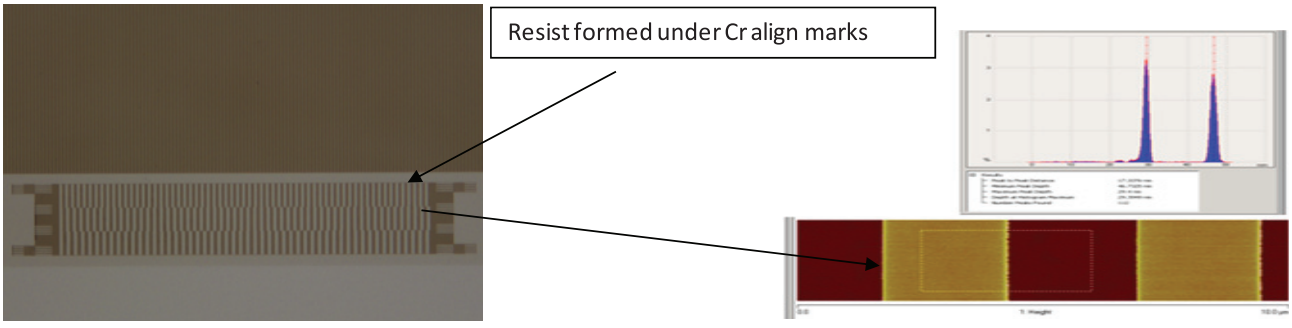


Figure 8. Resist pattern on a silicon wafer demonstrating pattern under the chromium material in selected areas.

is used for registration marks in order to align the pattern to the mesa on the replica mask blank.

The replica mask also has a 6025 form factor, but additionally includes a raised pedestal or mesa. This mesa later becomes the patterned area of the replica mask. This design was chosen specifically to eliminate the defects added to the mask by forming the mesa after the pattern transfer of the fine features on the mesa. As a result, we can take advantage of the imprint blank infrastructure that has already demonstrated an imprint mask blank defectivity of only 0.04/cm^2.[8]

b. Mask replication tooling

In December 2010, the first mask replication tool specifically for the CMOS market, the MR5000, was shipped to Dai Nippon Printing. The tool accepts a standard 6025 mask form factor and prints a nominal field size of 26mm x 33mm. Residual layer thickness uniformity (RLTU) and the added critical dimension uniformity error are 4nm and 1nm, 3sigma, respectively. The added image placement error is specified at 5nm, 3 sigma and the tool operates within an ISO Class 2 environment. A photograph of the MR5000 and a list of tool specifications are shown in Figure 3.

Details of the master mask process have been previously published.[9,10] Prior to imprinting the replica blank, an adhesion layer is applied. The adhesion layer provides preferential bonding between the replica blank and the imprint resist which is critical for maintaining low defectivity during the imprint process. Properties of this VALMat layer have been discussed in detail in previous publications.[11,12] Briefly, VALMat was specifically designed to have low molecular weight and high vapor pressure at room temperature. This is a preferred method for coating, since vapor deposition processes can achieve excellent uniformity and low defectivity across the mesa of the replica blank.

Adjustment of magnification is done within the imprint tool by registering the master to a reference. This extra step provides additional flexibility to better meet customer overlay requirements. After the resist image is imprinted on to the replica blank, pattern transfer is accomplished by plasma etching in series the remaining resist residual layer, the chromium hard mask, and underlying fused silica. A schematic and SEM images illustrate the process, as shown in Figure 5.

The final steps in the process include a high contrast mark (HCM) fabrication sequence and metrology and inspection. Inspection has been discussed in previous publications.[13,14] Details of the HCM steps are reviewed in Section 3.

3. Replication Results

a. High contrast align mark formation

MII uses a Moiré alignment scheme to align the mask to patterns on the wafer. Typically the mask pattern contains a periodic line/space structure and the wafer substrate has a corresponding checkerboard pattern. The interaction between these mask and wafer features scatter light in such a way that results in an optical image providing sub nanometer resolution alignment information.

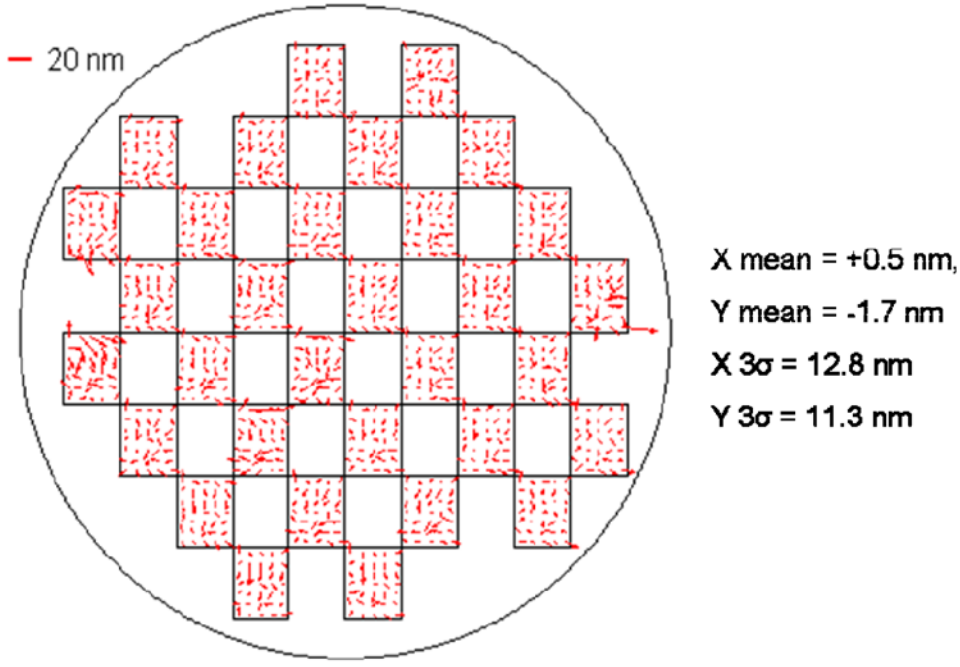
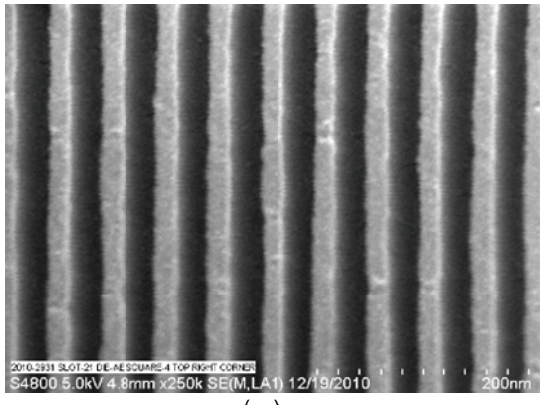


Figure 9. Mix and match overlay achieved using a HCM imprint mask.



(a)

CDU 3σ	Imprint1 (nm)	Imprint2 (nm)	Master (nm)
28nm	1.9	1.9	1.9
24nm	1.8	1.8	1.3

(b)

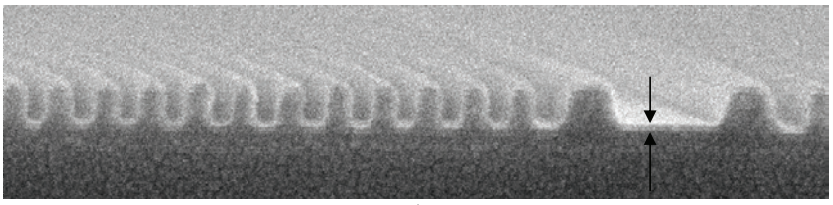
Figure 10. a) Example of imprinted 24nm half pitch lines using the MR5000 tool. b) 3sigma error comparison between the master mask and two replica masks.

The original Moiré align mark design included a moated area to separate the imprint resist in the patterned area from the align mark.[15] This was necessary because the imprint fluid has a very similar index of refraction to the fused silica. As a result, features in the mask would become invisible when in contact with the resist fluid and thus the moiré align technique would not function properly. By creating an air gap (with an index of refraction of 1.00), the mark was easily viewed. While acceptable for research and development, the approach has two drawbacks: 1) the moated area takes up valuable real estate on the field which can no longer be patterned, and 2) The moated area is subject to contamination from the nearby deposited resist drops, which may affect alignment signal strength after printing several wafers.[16]

The moat has been eliminated by depositing a thin (~15nm) layer of chromium in the base of the trenches of the Moiré mark on the replica mask. The chromium film provides contrast when the liquid resist fills the Moiré relief images, thereby enabling a high intensity interferometric signal. While many different materials are possible for use with a HCM scheme, chromium has been selected for its compatibility with both standard photomask processing and imprint processing. The method for fabricating the HCM is shown in Figure 6. After patterning of the fine features,

Chromium is deposited across the field. An imprint step is then used to apply uniform layer of resist across the field while preferentially protecting the alignment mark locations. This step is important because typical resist planarization methods such as spin-on techniques do not work uniformly over large mesa edges. A resist etch-back step exposes the chromium in all areas except the align marks, then chromium is selectively removed and the remaining resist is then stripped away. Two examples of Moiré signals are shown in Figure 7. Both thin (10nm) and thick (30nm) chromium layers were tested, and both signal intensities were found to be greater than the baseline Moiré signal observed in air.

Although chromium is a good material for producing a Moiré signal with high contrast, there was an initial concern that this material might interfere with resist curing. If the resist inside the



a)

	RLT Mean	RLT 3 σ
Field to Field	10.6nm	1.6nm
With-in Field	10.3nm	1.5nm

b)

Figure 11. a) Imprint cross section showing both the feature cross section and the residual resist layer. b) Within field and field-to-field RLT and RLTU.

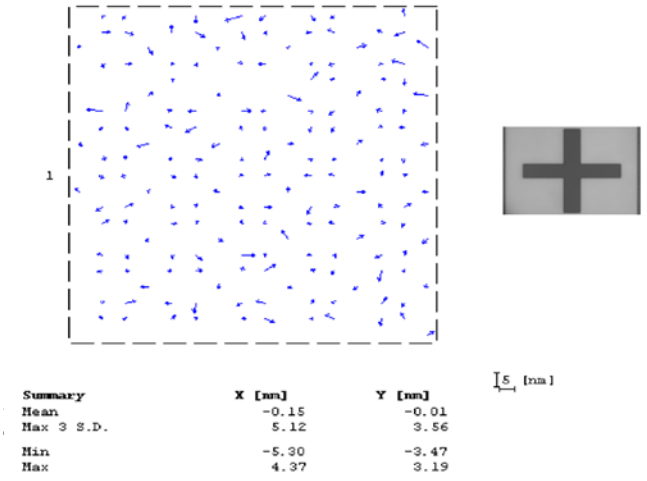


Figure 12. Image placement vector plot showing the added image placement error contribution resulting from the mask replica process after imprinting. The mark used to measure the displacement vectors with an IPRO1 are shown to the right of the vector plot.

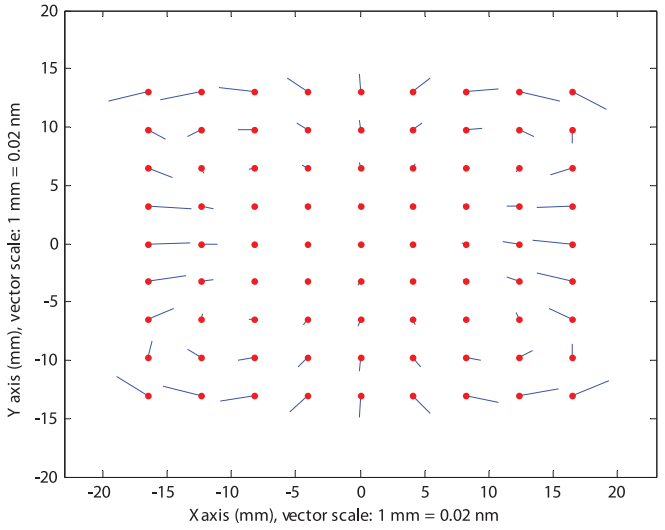


Figure 13. Induced distortion per ppm applied magnification correction. Maximum error vectors in x and y are 0.07nm and 0.04nm, respectively.

align mark does not cure properly, it could become a potential contamination source. An experiment was run with four different Moiré mark conditions: No chromium, 10nm, 15nm, and 30nm chromium thicknesses. In all cases, resist under the align marks properly cured with the target exposure dose of 100 mJ/cm^2. Some resist thickness loss was observed for the 30nm Cr thickness at exposure doses below 80mJ/cm^2. This is an extreme case and is not required for good results. Thicknesses around 15nm showed optimal contrast with no adverse effects from chromium shadowing as compared to the no chromium condition.

Alignment and overlay were tested by placing a mask with high contrast marks on an Imprio 500 and aligning to a silicon wafer patterned with 193nm scanner. The results are shown below. Three sigma mix-and-match errors were 2.8nm in x and 11.3nm in y, less than the 15nm overlay specification on the tool. It should be noted that the imprint mask used for this test had image placement errors of approximately 10nm, indicating that better mix and match results should be obtained by using an imprint mask with smaller image placement errors.

b. Imprint characterization

Initial data has been collected to evaluate the performance of the MR5000. First tests include critical dimension uniformity (CDU), residual layer thickness uniformity and image placement error contributions.

CDU was tested by measuring 24nm and 28nm dense lines at thirty different locations on both the master and replica mask and comparing the 3sigma variations for each data set. The results are shown below in Figure 10. The 28nm features show no difference in variation. The master and replica differ by 0.5nm for the 24nm lines. The error differences are within the gauge capability of the SEM, and consistent with previous work that documents that little or no additional variation occurs as a result of imprinting.[17]

Residual layer thickness (RLT) and residual layer thickness uniformity (RLTU) tool specifications are <15nm and <4nm, 3sigma, respectively. Two ask fields were imprinted and data was collected by cross sectioning the sample in five locations and measuring RLT fifteen times for each cleave, for a total of 45 measurements. In this experiment, RLT was targeted at 10nm. The measured RLT within field was 10.3nm. The field to field variation was 10.6nm. The RLTU was 1.5nm and 1.6nm, respectively. An example of a

resist cross section and a summary chart of the RLT data is shown in Figure 11.

Image placement errors were evaluated by measuring both a master mask and an imprinted mask and comparing the image placement vectors. Measurements were made on a Leica IPRO1. Gauge error on this tool is estimated at 3-4nm. The added image placement error vector plot is shown in Figure 12. The added contributions to image placement are 5.12nm in x and 3.56nm in y. The added error contributions will need to eventually be reduced to approximately 2nm in order to meet the requirements of the ITRS roadmap. It should be noted that modeling indicates that the error contribution from compressing the mask is not more than 0.07nm per ppm of applied magnification correction (See Figure 13.). Additional experiments and modeling will be required to identify the key contributors and drive image placement down to acceptable levels.

c. Replica mask pattern transfer

In order to study pattern transfer, a master mask was fabricated by DNP. The field size was 26 x 32mm, and contained critical dimensions of 28, 32 and 48nm. For this work, fluorine-based chemistry was used to etch the residual layer. Pattern transfer examples of all three feature sizes are shown in Figure 14. Figure 14a shows the imprints from the master. Figure 14b shows cross-sections of the same features on the replica mask. Note the near vertical profile obtained for all three line sizes. A cursory study of etch depth uniformity looks promising. A targeted 60nm fused silica etch resulted in an etch depth of 60.5nm, with a 3 sigma variation of only 2.5nm.18 A more detailed study of both etch depth uniformity and CDU after etch will be the subject of future studies.

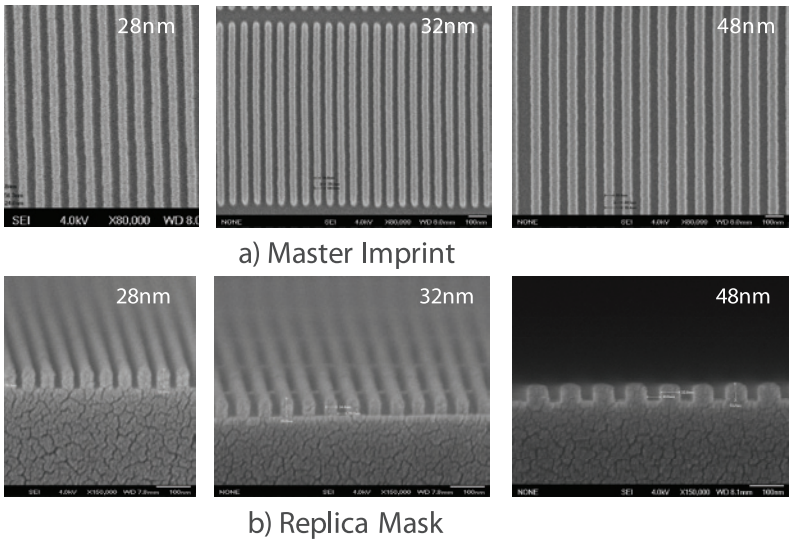


Figure 14. Pattern transfer of a semiconductor replica mask. a) Imprints of the master onto the mesa of the replica substrate. b) The same features etched into the replica mask.

4. Conclusions

A first look has been taken at the replication of semiconductor masks. A semiconductor mask specific replication tool, the MR5000, has been fabricated and shipped to DNP in late December. The initial data is promising. A high contrast mark process has been developed in order to maximize wafer pattern area and insure longevity during field to field alignment. Critical dimension uniformity and residual layer thickness uniformity are performing well within tool specifications. An initial study of image placement error, resulted in added displacement vectors of 5.12nm in x and 3.56nm in y. Further work will be required to drive down image placement errors in order to meet the ITRS roadmap for imprint masks. Finally, pattern transfer of an imprint mask has been demonstrated. Additional work will be required to optimize the pattern transfer process. The final subject to address is defectivity. Previous imprinting tests on wafer imprint tools indicates that particle adders of 0.1 per wafers pass can be obtained. A careful inspection of the replica blank in addition to low particle adders will be necessary to meet the aggressive defect targets necessary for replica mask fabrication. Resolution after pattern transfer of 28nm has been confirmed. The early results on both etch depth and CD uniformity are promising but more extensive work is required to characterize the pattern transfer process.

5. Acknowledgments

The authors would like to thank Masaaki Kurihara, Shiho Sasaki, Koji Ichimura and Naoya Hayashi from Dai Nippon Printing for their excellent imprint mask fabrication work.

6. References

1. M. Colburn, S. Johnson, M. Stewart, S. Damle, T. Bailey, B. Choi, M. Wedlake, T. Michaelson, S. V. Sreenivasan, J. Ekerdt, and C. G. Willson, **Proc. SPIE, Emerging Lithographic Technologies III, 379** (1999).
2. M. Colburn, T. Bailey, B. J. Choi, J. G. Ekerdt, S. V. Sreenivasan, **Solid State Technology, 67,** June 2001.
3. T. C. Bailey, D. J. Resnick, D. Mancini, K. J. Nordquist, W. J. Dauksher, E. Ainley, A. Talin, K. Gehoski, J. H. Baker, B. J. Choi, S. Johnson, M. Colburn, S. V. Sreenivasan, J. G. Ekerdt, and C. G. Willson, **Microelectronic Engineering 61-62** (2002) 461-467.
4. R. S. Sasaki, T. Hiraka, J. Mizuochi, A. Fujii, Y. Sakai, T. Sutou, S. Yusa, K. Kuriyama, M. Sakaki, Y. Morikawa, H. Mohri, N. Hayashi, **Proc. SPIE Vol. 7122,** 71223P (2008).
5. S.V. Sreenivasan, P. Schumaker, B. Mokaberi-Nezhad, J. Choi, J. Perez, V. Truskett, F. Xu, X, Lu, presented at the SPIE Advanced Lithography Symposium, Conference 7271, 2009.
6. K. Selenidis, J. Maltabes, I. McMackin, J. Perez, W. Martin, D. J. Resnick, S.V. Sreenivasan, **Proc. SPIE Vol. 6730,** 67300F-1, 2007.
7. I. McMackin, J. Choi, P. Schumaker, V. Nguyen, F. Xu, E. Thompson, D. Babbs, S. V. Sreenivasan, M. Watts, and N. Schumaker, **Proc. SPIE 5374,** 222 (2004).
8. L. Singh, K. Luo, Z. Ye, F. Xu, G. Haase, D. Curran, D. LaBrake, D. Resnick, S.V. Sreenivasan, **Proc. SPIE 7970** (2011).
9. S. Sasaki, T. Hiraka, J. Mizuochi, Y. Sakai, S. Yusa, Y. Morikawa, H. Mohri Naoya Hayashi, **Proc. SPIE 7470,** 74700J (2009).
10. T. Hiraka, J. Mizuochi, Y. Nakanishi, S. Yusa, S. Sasaki, Y. Morikawa, H. Mohri, Naoya Hayashi, **Proc. SPIE 7379,** 73792S (2009).
11. G. M. Schmid, C. Brooks, Z. Ye, S. Johnson, D. LaBrake, S. V. Sreenivasan, and D. J. Resnick, **Proc. SPIE 7488,** 748820 (2009).
12. Z. Ye, R. Ramos, C. B. Brooks, P. Hellebrekers, S. Carden, D. LaBrake, **SPIE 7637**, 76371A (2010).
13. D. J. Resnick, G. Haase, L. Singh, D. Curran, G. M. Schmid, K. Luo, C. Brooks, K. Selinidis, J. Fretwell, S. V. Sreenivasan, **Proc. SPIE 7637,** 76370R (2010).
14. K. Selinidis, E. Thompson, S. V. Sreenivasan, D. J. Resnick, M. Pritschow, J. Butschke, M. Irmscher, H. Sailer, Harald Dobberstein, **Proc. SPIE 7379,** 73790N (2009).
15. Ian McMackin, Philip Schumaker, Daniel Babbs, Jin Choi, Wenli Collison, S. V. Sreenivasan, Norman E. Schumaker, Michael P. C. Watts, and Ronald D. Voisin, **Proc. SPIE 5037,** 178 (2003)
16. M. Malloy and L. C. Litt, **Proc. SPIE 7637,** 763706 (2010)
17. G. M. Schmid, N. Khusnatdinov, C. B. Brooks, D. LaBrake, E. Thompson, Douglas J. Resnick, **Proc. SPIE 7028,** 70280A (2008).
18. C. Brooks, K. Selinidis, G. Doyle, L. Brown, D. LaBrake, D. J. Resnick, S. V. Sreenivasan, **Proc. SPIE 7823,** 78230O (2010).

Industry Briefs

IMEC has announced two breakthroughs in its EUV mask its defectivity assessment

April 18, 2011

For about two years IMEC has been using a combination of 3 inspection techniques for the evaluation of the defectivity level of state-of-the-art reticle; mask blank inspection, non-actinic patterned mask inspection and wafer inspection. This approach was leveraging the full wafer print capability of the ASML EUV Alpha Demonstration Tool (a.k.a. ADT). It has delivered some evidence that blank inspection, used by EUV mask blank vendors, does not satisfactorily detect all blank related defects that result in a printed defect on the wafer. IMEC has been able to visualize examples of multilayer (ML) defects that were previously undetectable. It is know that a printed-pit ML-defect on the order of a few nanometers can induce high distortion in the upper part of an EUV mask.[1] ML-defects that are missed by the 'state-of-the-art' blank inspection tools can be detected utilizing actinic microscopy or by leveraging EUV scanners to print the mask defect.

Next, there is a need to mitigate the ML-defects. The second breakthrough was a project, working with Zeiss SMS, to generated experimental proof for defect compensation based on the ebeam MeRiT® repair technology. It is not easy to repair ML-defects, but by adjusting the absorber pattern anticipating their presence has been shown to minimizing the change in printed feature.
[1] http://www.nanowerk.com/news/newsid=21050.php

EUV Mask Cleaning Presents Economic Challenges

By **David Lammer,** March 25, 2011

EUV lithography is forcing a closer relationship between metrology and mask cleaning. Mask makers will have to develop new techniques for dealing with particles on the EUV mask blanks and patterned EUV masks, speakers pointed out at the SEMATECH sponsored- Surface Preparation and Cleaning Conference (SPCC) in Austin, Texas. Beyond the daunting technical challenges, vendors are raising return-on-investment questions. Because so few semiconductor vendors are likely to use EUV masks, the capital required to develop the cleaning methods and equipment may not pay off, several participants said during the meeting, attended by about 150 people over two days.

In spite of all the dollars being invested on EUV infrastructure, cost of learning continues to increase as early adopters struggle to buy mask blanks and patterned mask metrology tool. A Sematech mask cleaning engineer indicated that the Sematech R&D EUV mask cleaning group sometimes gets "leftover" mask blanks for testing, with sources including Sematech's own member companies. But it is difficult to get more than a few of them, at any given time and they are used up quickly.

The small number of mask vendors and the high tooling costs of inspection equipment have necessitated a consortia style funding approach. As a result, Sematech now leads an EUV Mask Infrastructure (EMI) consortium, formed to develop EUV mask inspection tools. Sematech is moving to 15nm half pitch (HP) and 8 nm HP process technology R&D.

One goal of the EMI consortium is to develop an AIMS mask review tool. The EMI consortium also will develop inspection tools that can be used for both blank substrates and patterned EUV masks. The EMI team will likely focus new tooling to deliver actinic (13.5nm wavelength) solutions at the 16nm node and beyond, beginning in 2013.

[2] http://semimd.com/blog/2011/03/25/euv-mask-cleaning-presents-economic-challenges/

Join the premier professional organization for mask makers and mask users!

About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

Individual Membership Benefits include:

- Subscription to BACUS News (monthly)
- Complimentary Subscription *Semiconductor International* magazine
- Eligibility to hold office on BACUS Steering Committee

spie.org/bacushome

Corporate Membership Benefits include:

- Three Voting Members in the SPIE General Membership
- Subscription to BACUS News (monthly)
- One online SPIE Journal Subscription
- Listed as a Corporate Member in the BACUS Monthly Newsletter

spie.org/bacushome

Calendar

2011

SPIE Photomask Technology

19-22 September 2011
Monterey Marriott
and Monterey Conference Center
Monterey, California, USA
spie.org/pm

2012

Advanced Lithography

12-16 February 2012
San Jose Convention Center and San Jose Marriott
San Jose, California, USA
spie.org/alcall

Submit your Abstracts Now!

You are invited to submit events of interest for this calendar. Please send to lindad@spie.org; alternatively, email or fax to SPIE.

SPIE is an international society advancing light-based technologies.

SPIE

International Headquarters
P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 888 504 8171 or +1 360 676 3290
Fax: +1 360 647 1445
customerservice@spie.org • SPIE.org

Shipping Address
1000 20th St., Bellingham, WA 98225-6705 USA

SPIE Europe

2 Alexandra Gate, Ffordd Pengam, Cardiff,
CF24 2SA, UK
Tel: +44 29 2089 4747
Fax: +44 29 2089 4750
spieeurope@spieeurope.org • www.spieeurope.org