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2017 Advanced Lithography

Application of actinic mask review system for the preparation of HVM EUV lithography with defect free mask

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ABSTRACT

We introduce an extreme ultraviolet lithography (EUVL) mask defect review system (EMDRS) which has been developing in SAMSUNG. It applies a stand-alone high harmonic generation (HHG) EUV source as well as simple EUV optics consisting of a folding mirror and a zoneplate. The EMDRS has been continuously updated and utilized for various applications regarding defect printability in EUVL. One of the main roles of the EMDRS is to verify either mask repair or mask defect avoidance (MDA) by actinic reviews of defect images before and after the process. Using the MDA, small phase defects could be hidden below absorber patterns, but it is very challenging in case of layouts with high density patterns. The EMDRS clearly verify the success of the MDA while conventional SEM could not detect the images. In addition, we emulate images of the sub-resolution assist features (SRAFs) by the EMDRS and compared them with the wafer exposure results.

1. Introduction

Recently, readiness of the EUVL infrastructure for the high volume manufacturing (HVM) has been accelerated[1]. EUV source availability, the first showstopper against EUVL HVM, has been dramatically increased and close to the targets for HVM insertion. Mask defectivity, another focus area for the HVM, has also been concerned. Due to the difference in mask and optics appropriate for the wavelength between EUV and ArF lithography, specialized metrology tools are required in EUVL. However, current DUV and e-beam inspection tools are easy to miss the printable phase defects in EUV mask since the lights of corresponding wavelengths cannot penetrate multilayers (MLs)[2,3]. Therefore, the actinic review system is essential to provide defect free EUV masks.

Since actinic inspection tools for EUVL masks are not ready, DUV or e-beam inspections are prevalent solutions. However, images using DUV or e-beam are sometimes far from the aerial images of scanner. Thus, if a defect is repaired, there is no way to verify the result during the mask fabrications. In addition, the AIMSTM EUV is still being developed and a HVM tool is not available[4]. Hence, EMDRS in SAMSUNG is supposed to be the first and unique mask defect review

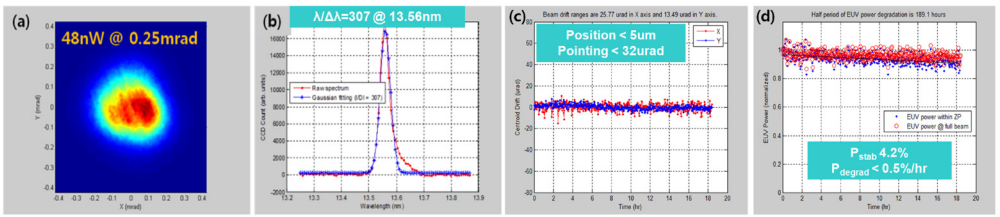

Figure 1. (a) EUV source power and divergence was measured by EUV CCD. (b) Spectrum of the 59th harmonic shows spectral purity more than 300 (c) Position and pointing stability (d) power stability.

BACUS NEWS

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VOLUME 33, ISSUE 7

TAKE A LOOK INSIDE:

INDUSTRY BRIEFS
—see page 9

CALENDAR
For a list of meetings
—see page 10

SPIE.

10145-21

EDITORIAL

EUVL vs. NIL: Why aren't we done yet?

Artur Balasinski, Cypress Semiconductor Corp.

With some surprise, I was reading a recent report from the panel session of 2017 Photomask Japan (PMJ): Who is Closer to Goal, EUVL or NIL? For years now, the momentum and press releases indicated that the general election for the sub-10 nm litho technology is over (and the winner is EUVL, in case you are wondering). As with any election, one may like or not like the result, but it is over now. Yet, it now seems that either the industry is doing better than expected, trying to develop two exceedingly expensive patterning techniques to sustain the unsustainable Moore's law, or, some people are losing their minds, thinking that the votes should be counted all over again. So, which way is it?

PMJ report on Panel Discussion, "Race for Volume Production", presented how the EUV team gave the device maker, the exposure equipment maker, and the mask maker perspective. Jim Wiley from ASML claimed that EUVL has progressed over 30 years from NGL to HVM insertion. 14 NXE systems are installed and > 800,000 wafers exposed at several customer sites. The NXE:3400B scanner exposed 104 WPH at 148 W and the productivity roadmap towards > 125 WPH is in place, enabling 7nm and 5nm nodes. NXE pellicles films could be produced without printing defects. Erik Hosler from GF continued on, about the EUVL Cycle time advantage. The number of critical mask steps for optical lithography are 30 and only 10 for EUVL. For yield and quality, at GF there is less variation in electrical parameter and tighter process control, so process complexity is greatly reduced.

From the NIL team, Naoya Hayashi from DNP reported that the achieved resolution of NIL templates is < 20nm in L/S and holes. Compared to NIL, EUVL needs complex mask, scanner and dedicated infrastructures. NIL is simple but needs 1X nm feature and defect control. The printing size was shrunk by a factor of a million over 100 years.

Tatsuhiko Higashiki from Toshiba pointed out that the device architectures are shifting from 2D to 3D. He argued that the requirements for Non-volatile memory devices are changing from higher resolution to process cost reduction due to higher productivity, manufacturing yield and reliability. Therefore, in order to reduce investment in lithography, NIL technology has aggressively been developed with Canon and DNP.

The audience voted a total of three times, which team was dominant. Although the rule was that only the last vote decides the team's victory or defeat, two votes early in the race directed the merits of the middle stage and raised the discussion for final voting. NIL took a lead in the first vote but twice, including the final voting, EUV gained 65 votes against 55 votes for NIL. Bryan Kasprowicz from Photronics, concluded: "Both technologies still need work but EUV is the clear leader".

While this outcome was hardly a surprise, it is interesting to note that over the last 10-15 years, neither side was able to knock the opponent out, and certainly not for the lack of trying. The question remains, is this type of competition valuable? Shouldn't the effort be focused to deliver only one solution? The answer seems to be a resounding "NO". All the players continue the struggle at their own cost, hoping to get ahead, and who knows, maybe come up with some breakthroughs. This shows that maskmaking business should still have many good years ahead.

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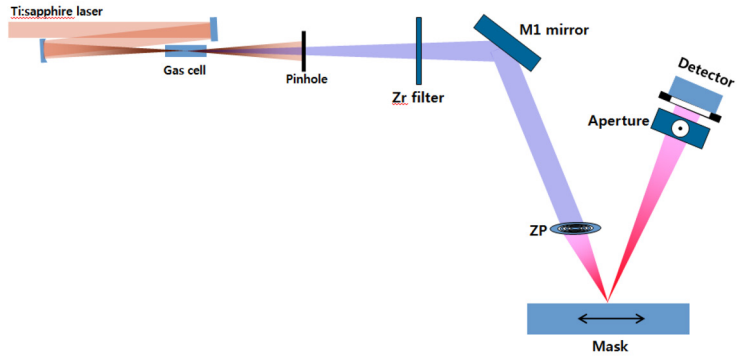

Figure 2. System configuration of EMDRS.

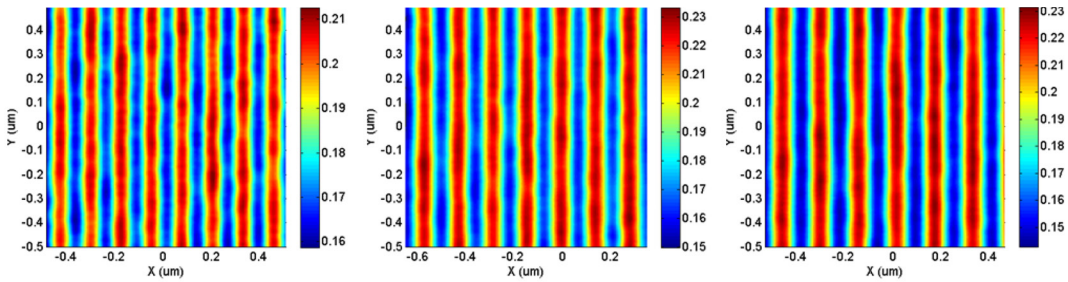

Figure 3. Aerial images of L/S patterns taken by EMDRS with 16nm, 18nm, and 20nm HP (1x).

tool installed in the mask shop[5] to provide a defect free mask to wafer fab. Here, we introduce our recent works regarding practical applications with our improved aerial imaging system in EMDRS.

2. EUV mask defect review system (EMDRS)

We previously introduced a prototype EMDRS which had been developed in SAMSUNG[5,6]. The EMDRS has been continuously updated and used in various EUV related studies. It consists of a stand-alone coherence EUV source and a simple EUV optics including scanning stages, a zoneplate lens, and an X-ray detector. The scanning based imaging system in the EMDRS provides aerial images. Firstly, the source generates 13.5nm wavelength of EUV light which is delivered to multilayer (ML) mirror and focused at the EUV mask through the zoneplate. Secondly, while the PZT stage scans the mask in X and Y directions, the each point intensity is detected at the X-ray detector and converted to the electrical signals. Thirdly, the signal is digitized at the analog-to-digital converter and sent to the imaging processing unit. Lastly, aerial images are reconstructed during the mask scans and those processes are repeated until the scan ends.

EUV source is one of the most important parts in actinic systems. Current EUV sources for scanners in semiconductor manufacturing fab are either discharge-produced plasma (DPP) or laser-produced plasma (LPP) type. Although both DPP and LPP type sources show high brightness and good stability through the continuous improvement of source technology, they are still complex and require high cost of ownership (CoO). Instead, we accordingly chose a HHG EUV source considering its intrinsic properties such as excellent spatial coherence, compactness, and stability[7,8]. Moreover, it exhibits high photon flux in low divergence with efficiency and cost effectiveness for the applications[9].

Figure 1 shows power and divergence of the HHG EUV source which is good enough to adopt in the actinic defect review system. The high power femto-second laser is focused into a gas cell and generates 48nW EUV power with the divergence of 0.25 mrad. Small beam divergence increases the collecting efficiency of EUV photons which is determined by the zoneplate diameter. The EUV source has spectral purity ($\lambda/\Delta\lambda$) of 307 as shown in Figure 1b. Since the zoneplate is a kind of diffractive optics, narrow beam bandwidth was required to minimize chromatic aberrations. As shown in Figure 1c and 1d, the position and pointing stability are 5 μm (3σ) and 32 μrad (3σ), respectively, and EUV power stability with 1 kHz repetition rate is 4.2% (3σ). These outputs are important to guarantee the image quality as well as the long term measurement repeatability.

Figure 2 illustrates system configuration of the EMDRS. Interaction between intense femtosecond (fs) IR laser and gaseous medium generates EUV lights. Then, coherent EUV lights pass through the pin-hole while most of IR lasers are primarily blocked by the pin-hole and then also removed by the Zr filter. The rectilinear EUV lights are redirected by the M1 mirror and form a diffraction-limited spot (82nm) on the mask by a zoneplate (ZP) lens. The M1 mirror consists of 52 bi-layers of Mo/Si of which thickness is 0.8 and 9.62nm in each layer. It is designed to satisfy both high reflectivity and narrow bandwidth under the circumstance of 13.56nm of wavelength and 42 degrees of angle of incidence. As a result, the tilted M1 mirror reflects EUV lights with narrow bandwidth centered at 13.56nm and the peak reflectivity of 65%.

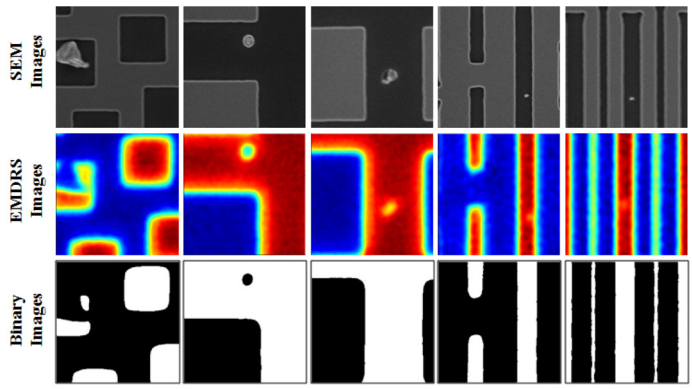

Figure 4. Various defects on EUV mask. Some are critical so they can be printed on wafer and some are not.

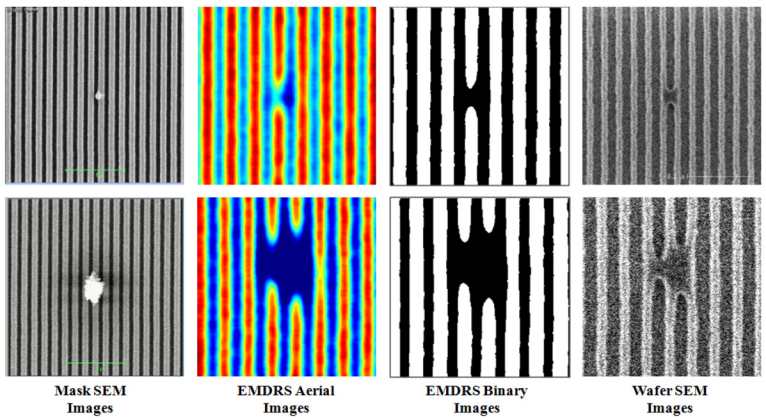

Figure 5. Comparison of mask SEM images, EMDRS aerial images, EMDRS binary images, and wafer SEM images. The EMDRS binary images show the same results with the wafer prints

Then only 59th harmonic component could propagate to ZP while the neighboring orders could not. The ZP focuses EUV lights onto EUV mask surface with incidence angle of 6 degrees and diffracted beams from the mask are detected by a photodiode. To emulate EUV scanner, NXE3300, the numerical aperture (NA) and sigma in EMDRS are designed to 0.33 (wafer scale) and 0.9, respectively.

Aerial images are attained by scanning of the mask with the focused beam during continuous movement of the two Piezoelectric Transducer (PZT) stages in x and y directions. Figure 3 shows aerial images of 16nm, 18nm, and 20nm HP (1x) 1:1 line and space (L/S) patterns obtained by the EMDRS. Clear dense L/S aerial images are shown down to 16nm HP (1x) node. The pixel size is 10nm and the field-of-view (FOV) is 1μm x 1μm in these images. The pixel size and FOV could be variable depending on defect size, throughput, and image resolution.

3. Applications

3.1. Defect review

After the patterning process of a mask, pattern inspection is required to find printable defects and repair them. Some defects on the masks are fatal to wafer production yield, and thus it is essential to confirm if the defects are printable or not on the wafers prior to the mask flow to wafer FAB. In case of printable defects on critical areas, they have to be repaired and then verify their non-printability after the repair. Figure 4 compares SEM and EMDRS images of several defects on the EUV masks. Those are typical process defects created during the mask manufacturing. All defects in the SEM images are clearly noticeable while EMDRS images are differentiated from the SEM images. Some defects in the EMDRS images look very clear and others do not. To verify whether they are critical or not, the binary coded images from the EMDRS set by threshold intensity of target CD are shown in the third row. The white and black colors correspond to the clear and opaque areas, respectively, on the mask patterns in the binary images. According to the binary images, we can estimate that not all defects on the EUV mask are printed on the wafers.

Figure 5 compares defect images on the L/S patterns in the mask SEM, EMDRS (full scale aerial images), EMDRS (binary images at target threshold), and wafer SEM. As shown in the figure, EMDRS binary images and wafer SEM show the same results which are one bridge (first row) and two bridges (second row). Hence, we can estimate wafer printing results of mask defects prior to the wafer exposures by applying EMDRS analysis.

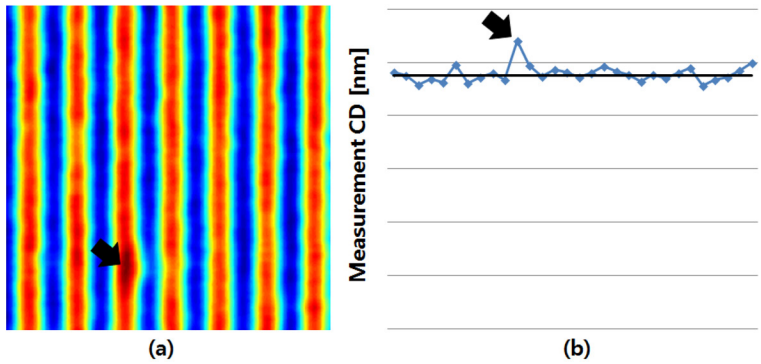

Figure 6. CD measurement results; (a) an aerial image in 1.3μm x 1.3μm of FOV of dense L/S patterns with a defect (b) All CD results with 200nm slice width.

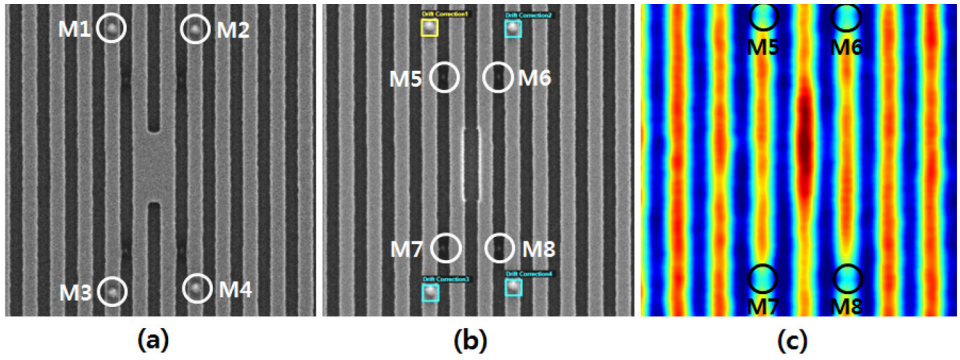

Figure 7. Comparison of (a) before and (b) after repair in SEM images and (c) EMDRS review after the repair. The EMDRS image shows clear difference between the normal and repaired patterns.

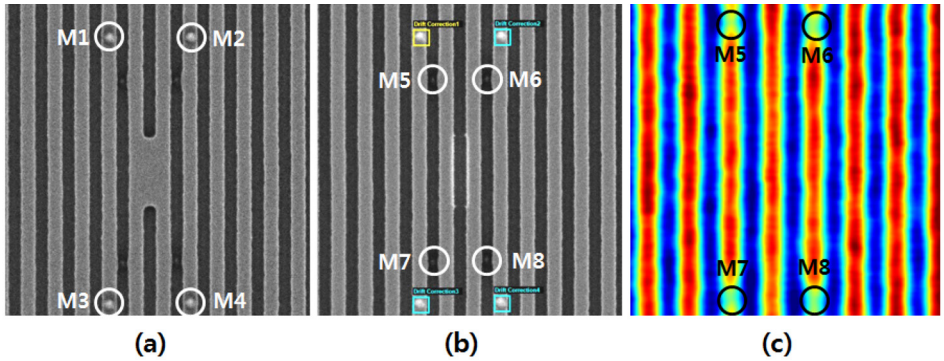

Figure 8. Comparison of (a) before and (b) after repair in SEM images and (c) EMDRS review after the repair. The EMDRS image shows no difference between the normal and repaired patterns.

3.2. CD measurements

In mask fabrications, defect inspection should be followed by defect review process to judge the existence and influence of the detected defects. For the quantitative analysis with the EMDRS, CDs in clean areas are compared with those in the defect positions. Figure 6 shows a typical example of L/S patterns in 7nm node which includes a noticeable defect. All CDs in the images are measured and averaged with 200nm slice width in a 1μm x 1μm area, so 30 CDs are obtained. The arrow in Figure 6a corresponds to the defect location and its CD is larger than the target CD by 13.5% as shown in Figure 6b.

3.3 Repair verification

Providing defect-free masks to wafer fabs is one of the most important roles in mask shops, and thus all of printable defects on the critical areas should be eliminated prior to the mask shipments[10,11]. In general, all defects caught by an inspection tool should be checked by a defect review system, before and after

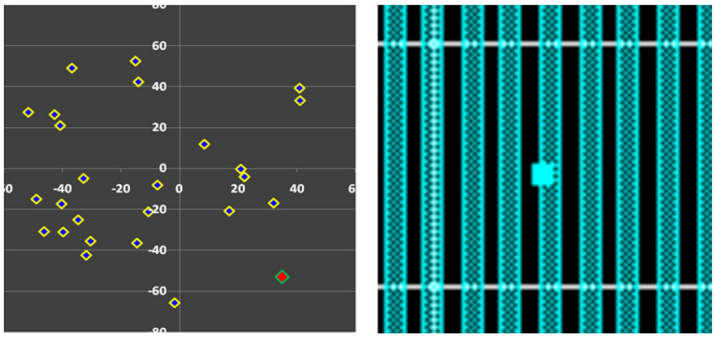

Figure 9. (a) Blank defect inspection map of an EUVL mask and (b) MDA calculation image of a selected ML defect which is not covered by absorber patterns.

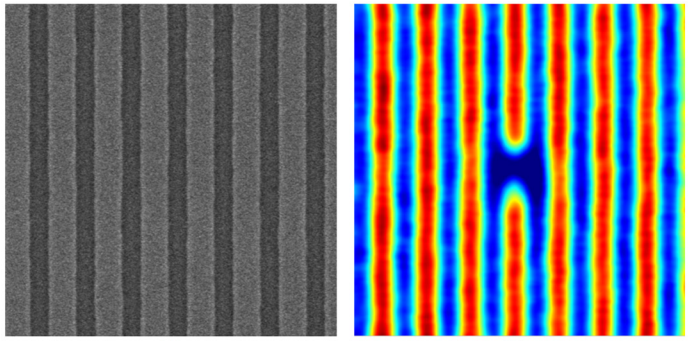

Figure 10. (a) SEM and (b) EMDRS images of the selected ML defect which is not covered by absorber patterns after the MDA.

the repair process, if they are printable. The review system also measures success or failure for the defect repair process. If it is practicable, application of the actinic review system is the most desirable for the defect review. However, there are no commercial actinic review systems installed at mask shop in the world and only a pre-production tool of the AIMSTM EUV is available on the supplier's site. Thus, the results of the EMDRS presented below are meaningful as a pioneer for the actinic defect review of the EUVL masks.

Figure 7 and Figure 8 show two typical applications of the EMDRS. A programmed defect mask (PDM) which includes defects with 2μm height on dense L/S patterns is utilized. Figure 7a and Figure 8a show SEM images of the programmed defects before the E-beam repair. M1 to M4 marks are indicators on the absorber patterns for e-beam repair alignments. During the e-beam repair, we engrave additional marks, M5~M8 shown in Figure 7b and Figure 8b, on the ML for the alignments for the EMDRS and post SEM reviews. According to the SEM images, both defects in Figure 7a and Figure 8a are clearly removed and hardly distinguishable as shown in Figure 7b and Figure 8b. However, there are clear distinctions between the EMDRS images after the repair in Figure 7c and Figure 8c. The CD difference (Δ CD) between the repaired and normal areas is only 2.9% in Figure 8c, while that of Figure 7c is 18.6%. Based on these data, we can conclude that the EMDRS is a powerful defect review tool for the EUVL mask since it can detect printable defects which are not visible with the SEM.

3.4. Mask defect avoidance (MDA)

There are two defect types in the EUV masks; one is amplitude (pattern) defect and the other is phase (ML) defect. Unlike the amplitude defects, phase defects are more troublesome since they are normally non-repairable and sometimes hard to be detectable during the mask process. The phase defects include pit defects, which come from scratches occurred during the substrate polishing process, and bump defects caused by particles on the substrate as well as in the MLs. They lead to phase errors during wafer exposures and result in pattern defects on the wafer[12]. Thus, to keep cleanliness in substrate polishing and ML deposition is primarily important to mitigate the phase defects. Otherwise, additional leading-edge techniques, which make the phase defects not printable, such as mask defect avoidance (MDA) and proximity repair process, are required[13,14].

The MDA is a technique to relocate phase defects to non-printable areas, such as under the absorber patterns in the device layout, based on the information of the defects from the blank inspection. Thus, alignment through the fiducial mark (FM) between blank defects coordinates and e-beam writing is the key process for the precise control of the MDA. In the range of a few dozen, small phase defects could be mitigated by rotating or shifting mask layouts during the ebeam writing. Due to the dramatic improvement of the ML defect level in recent years, EUVL mask with zero printable defects become available if the MDA is applied. However, accuracy errors in defect size, defect position, and e-beam align-

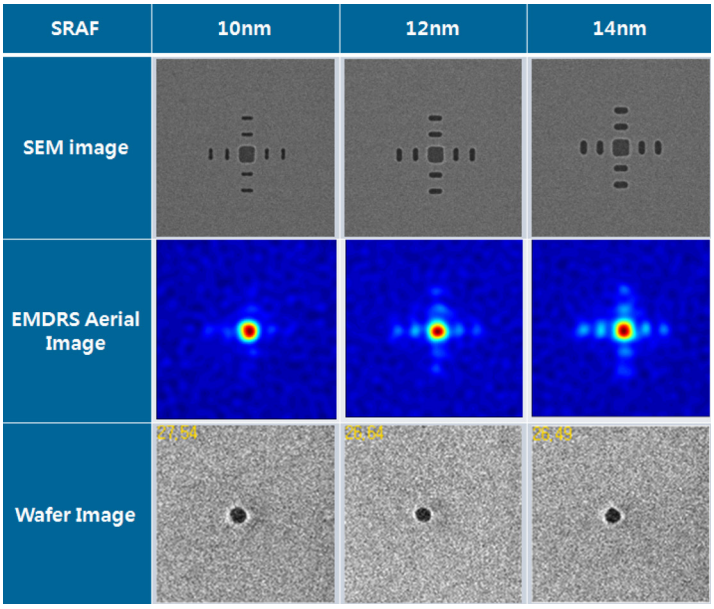

Figure 11. Mask SEM, EMDRS, and wafer SEM images of an isolated contact pattern with SRAFs. The SRAF widths are split by 10nm, 12nm, and 14nm and the main CD of the contact is 26nm in wafer scale (1x).

ment can be added during the MDA and may result in the failure of the MDA. Therefore, similarly with the repair process, success of the MDA should be verified with a defect review tool, although all ML defects are covered by the absorber patterns. As discussed previously, since it is impossible to detect all phase defects with inspection tools using DUV or e-beam, the EMDRS can be the only tool for this purpose during the mask process. According to the EMDRS results, we can make a decision whether to proceed with the proximity repair and sometimes we may scrap the mask due to the non-repairable phase defects.

Figure 9a shows a blank defect inspection map is taken by Teron Phasur system. MDA is applied to this blank prior to the e-beam writing and 25 ML defects out of total 26 defects are concealed under the absorber patterns. The exceptional defect point corresponds to the dot with red color in the map and its calculated image of the location on the patterns after the MDA is shown in Figure 9b. As shown in the figure, this ML defect is partially covered by the absorber patterns and ~1/3 of the total size is exposed on the open ML areas.

Figure 10 shows SEM and EMDRS images of the phase defect which is not covered by the absorber patterns in Figure 9b. Although the MDA software displays that the ML defect is partially covered by the absorber pattern, the SEM image in Figure 10a does not leave any evidence of the defect. However, when we look at the EMDRS image on the same point, a bridge defect is clearly observed as shown in Figure 10b. This is a typical case why we need an actinic review of defects in the EUVL mask. Up to now, there have been no satisfactory solutions to predict printability of ML defects on the wafers prior to the wafer exposures. Therefore, estimation of the wafer printability using the EMDRS could be a practical defect review solution in terms of cost and time.

3.5. Aerial images with SRAFs

Current optical masks in ArF for high-end devices adopt sub-resolution assist features (SRAFs) to enhance lithographic printing resolution. Similarly, we can also improve the printing resolution in EUVL, which is restricted by the 13.5nm wavelength and 0.33 NA, by applying the SRAFs [15]. In addition, application of the SRAFs has an effect to save cost and time by reducing exposure energy, especially for the contact arrays. Figure 11 shows mask SEM, EMDRS, and wafer SEM images of a contact pattern with SRAFs of different widths. The main CD of the isolated contact is 26nm in wafer scale (1x) and widths of the SRAFs are split by 10nm, 12nm, and 14nm. We can see that the SRAF widths affect the aerial images of the EMDRS. As a result, the EMDRS can emulate CD variations depending on target thresholds and SRAFs size. In addition to the defect verification, it is another active application area to be extended for the EMDRS which can emulate wafer exposure results in advance of the actual printings.

4. Conclusion

The EUV mask defect review system (EMDRS) adopting a scanning-type EUV microscope using a coherent and aberration-free EUV source and zoneplate optics has been developed. In the EMDRS, 82nm FWHM beam is focused onto the EUV mask and aerial images are acquired by scanning the stages. Several applications of EMDRS such as defect review, CD measurement, repair verification, MDA, and SRAF review are discussed. Since the EMDRS aerial images and actual wafer SEM images are well matched, the EMDRS provides confident verification results regarding defect printing before and after the repair and MDA. The EMDRS also emulates wafer printing results of the isolated contacts depending on SRAF sizes. In the further, we plan to reduce CD repeatability errors come from the EUV source in the EMDRS by improving the photon efficiency of the optics. These works would result in less shot noise, better source stability, and increase of the throughput in the EMDRS.

5. Acknowledgements

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Industry Briefs To Come

Long-Term IoT Semiconductor Forecast Reduced

SolidState Technology

IC Insights scaled back its total semiconductor sales forecast for system functions related to the Internet of Things in 2020 by about $920 million, mostly because of lower revenue projections for connected cities applications (such as smart electric meters and infrastructure supported by government budgets). The updated forecast still shows total 2017 sales of IoT semiconductors rising about 16.2% to $21.3 billion (with final revenues in 2016 being slightly lowered to $18.3 billion from the previous estimate of $18.4 billion), but the expected compound annual growth rate between 2015 and 2020 has been reduced to 14.9% versus the CAGR of 15.6% in the projection from December 2016. Total semiconductor sales for IoT system functions are now expected to reach $31.1 billion in 2020 versus the previous projection of $32.0 billion.

Meanwhile, the IoT semiconductor market for wearable systems is expected to show a CAGR of 17.1% (versus 18.8% in the previous projection). The lower growth projection in chip sales for connected cities systems is a result of anticipated belt tightening in government spending around the world and the slowing of smart meter installations now that the initial wave of deployments has ended in many countries. Slower growth in semiconductor sales for wearable systems is primarily related to IC Insights' reduced forecast for smartwatch shipments through 2020.

The updated outlook nudges up semiconductor growth in the industrial Internet category to a CAGR of 24.1% (compared to 24.0% in the December 2016 forecast) and slightly lowers the annual rate of increase in connected homes and connected vehicles to CAGRs of 21.3% and 32.9%, respectively (from 22.7% and 33.1% in the original 2017 report).

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Intel Contributes High-Level Pattern Analysis Language to Si2

SolidState Technology

Silicon Integration Initiative Inc. (Si2), a research and development joint venture, announced the contribution of a new integrated circuit programming language developed by Intel Corporation for the 2D pattern analysis of sub-20nm mask layouts.

The new language, called OPAL (Open Pattern Analysis for Layout), is a declarative language for geometric pattern matching. "It's a high-level, modeling language that can describe layout patterns of any complexity," according to Jake Buurma, an Si2 senior fellow. "OPAL provides an essential set of geometric expressions that can find specific patterns that detract from yield and it can find the robust patterns that improve first-pass yield over normal manufacturing variances."

For example, in sub-20nm processes, wires used for interconnect have an ideal pitch for the mask to chip image transfer during lithography, Buurma explained. "But these wires also have a prohibited pitch where the image transfer is poor since lithography cannot faithfully reproduce certain 2D patterns. The OPAL language searches for the layout patterns of both yield detractors and yield enhancers and then back annotates markers onto those patterns that will have an impact on manufacturing yield. OpenAccess has always had the ability to store mask layout constraints in its C++ database, but the actual checking of those constraints required an expert to program an exact sequence of steps into a design rule checking engine. But as a high-level, declarative language, OPAL can model complex 2D patterns by just describing a specific pattern with a few geometric expressions."

Si2 will host the OPAL project and launch an OPAL Working Group to evaluate and entertain proposals for an industry roadmap on how to best utilize the newly contributed technology from Intel.

http://electroiq.com/

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About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

Individual Membership Benefits include:

- Subscription to BACUS News (monthly)
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Calendar

2017

SPIE Photomask Technology and SPIE International Conference on Extreme Ultraviolet Lithography 2017
11-14 September 2017
Monterey, California, USA
www.spie.org/puv

The 33rd European Mask and Lithography Conference EMLC 2017
27-29 June 2017
Hilton Hotel
Dresden, Germany

2018

SPIE Advanced Lithography
25 February-1 March 2018
San Jose Marriott and
San Jose Convention Center
San Jose, California, USA
www.spie.org/al

Photomask Japan 2018
18-20 April 2018
Pacific Yokohama
Yokohama, Japan

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