PHOTOMASK

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Model based correction of placement error in EBL and its verification

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ABSTRACT

In maskmaking, the main source of error contributing to placement error is charging. DISPLACE software corrects the placement error for any layout, based on a physical model. The charge of a photomask and multiple discharge mechanisms are simulated to find the charge distribution over the mask. The beam deflection is calculated for each location on the mask, creating data for the placement correction. The software considers the mask layout, EBL system setup, resist, and writing order, as well as other factors such as fogging and proximity effects correction. The output of the software is the data for placement correction. One important step is the calibration of physical model. A test layout on a single calibration mask was used for calibration. The extracted model parameters were used to verify the correction. As an ultimate test for the correction, a sophisticated layout was used for the verification that was very different from the calibration mask. The placement correction results were predicted by DISPLACE. A good correlation of the measured and predicted values of the correction confirmed the high accuracy of the charging placement error correction.

1. Introduction

The placement error is one of the most important factors in semiconductor manufacturing. The maskmaking industry imposes challenging requirements for the placement error. The reason for this was outlined by Dr. J. Chen of nVidia: his results show a logarithmic increase of the failure rate in a chip at a linear misalignment between the VIA and metal layer, see Figure 1. At the 20

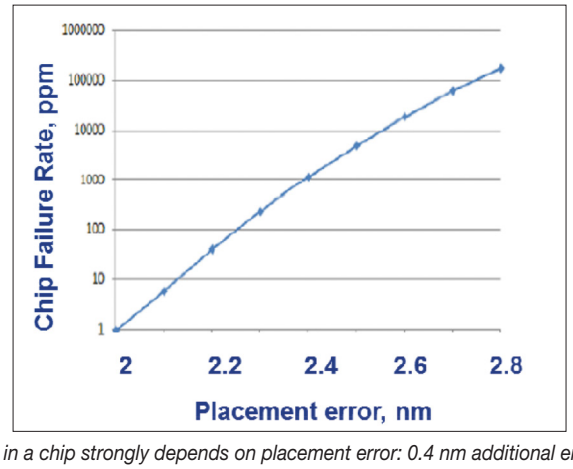

Figure 1. Failure rate in a chip strongly depends on placement error: 0.4 nm additional error causes 1000 times higher failure rate[1]; courtesy of J. Chen, nVidia.

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EDITORIAL

Full-scale Curvilinear ILT OPC on Photomask Manufacturing – Are We Ready?

By **Peter D. Buck,** Mentor Graphics Corp.

Inverse Lithography Technology (ILT) was introduced in 2006 as a novel OPC approach to improving lithography process window. The "organic" curvilinear shapes this produced further distanced the intuitive visual recognition of the target design in the OPC output. The seemingly random arrangements of "blobs" of pattern data, sometimes interconnected with tendrils so fine they defied reasoning as to their lithographic value, made it virtually impossible to visually comprehend the design intent. Mask manufacturability was quickly identified as a significant limiter to practical deployment. Neither single-beam raster ebeam lithography tools nor vector-shaped beam (VSB) writers could handle the data volumes and/or shape complexity to produce masks with reasonable write times. Limits on inspection, particularly die-to-database, metrology, and repair all proved too daunting to enable this new technology. Methods to simplify through Manhattanization with varying degrees of complexity reduction showed that the value of ILT was significantly reduced when complexity reduction intersected with practical mask manufacturability. ILT OPC did find a home, though. Today, ILT OPC is used as a local repair process for OPC hotspot regions, where the repair regions are few enough and small enough to minimize the impact on overall write time. MRC rules are enforced to render the output manufacturable, typically through Manhattanization with edge lengths set to be a compromise between mask manufacturability and value for process window expansion. Single beam raster ebeam mask writers are now retired from advance mask manufacturing, but VSB writers have advanced considerably and are capable of shot write rates high enough to accommodate the additional complexity of a localized ILT OPC approach. ILT OPC is still generally considered to be too computationally expensive to use on full layouts and even the most advanced VSB mask writers cannot handle the shot volume of even a Manhattanized full layout ILT approach. However, the computational cost of full-layout ILT OPC relative to its perceived value is lowering. It is not uncommon to use thousands of CPU-cores in distributed OPC applications in clusters of 10s of thousands of CPU-cores, which suggests that the computational capacity required is available. The introduction of multi-beam raster mask writers is expected to reduce the write time cost of raw ILT mask data compared to VSB writers, possibly soon making full-layout ILT OPC a reality. Since the write time of raster writers is generally a function of write area with little influence of data complexity (at least up to some limit), curvilinear ILT OPC may be enabled while the value of low data volumes may be reduced – in effect, the cost difference between high and low complexity mask layouts will be reduced.

Is the time for curvilinear, full-layout ILT OPC approaching? Answers may be available at the annual SPIE BACUS Symposium, to be held September 12-14, 2016 in San Jose, California. Papers updating progress on multi-beam mask writers, the expected application space of multi-beam writers, and the use of ILT OPC will be presented. This year's Panel Discussion focuses on the Impact of Full-scale Curvilinear ILT OPC on Photomask Manufacturing. Panelists representing IC manufacturers, and the mask technology domains of mask data preparation, lithography, inspection, repair, repair validation, and metrology will present their views on the readiness of the industry to support ILT OPC.

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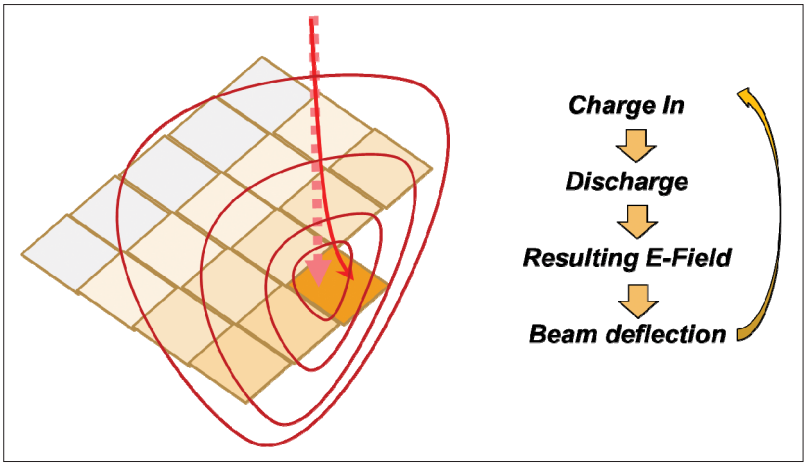

Figure 2. DISPLACE software provides a full physics simulation at each cell of the mask. Charge and discharge result in an electrical field inside the resist and outside the mask; the field deflects the electron beam from the desired location, creating placement error.

nm technology node, for each 0.1 nm increase in placement error, the failure rate increased in almost an order of magnitude. This result was later confirmed by K. Standiford of Global Foundries[2].

Most of the photomask placement error, or registration, comes from resist charging. When the mask is being written by electron beam lithography (EBL), the resist is getting charged; this charge creates an electrical field, which deflects the electron beam from the intended point of landing.

There are currently three methods to correct the placement error: applying charge dissipation layer (CDL)[3], software correction based on fitting by NuFlare Technology[4,5], and model based software correction by aBeam[6,7]. The CDL is a simple method and good progress has been made in the materials used for CDL in recent years. However, additional defects are unavoidable: the resolution and line edge roughness degrade, and the process signature is being changed. In addition, it was found that the charging error is reduced by CDL, but not eliminated. These drawbacks together with additional process steps and cost increase limit the application of CDL. The charging effect correction (CEC) by NuFlare based on polynomial fitting of a calibration mask shows improvement for some types of masks. However, its success was limited [8,9]. At Photomask Technology 2015, TSMC reported that CDL does not suppress placement error down to the specification and that CEC does not work up to expectations[10].

Model based correction that is of high enough quality and calibrated well is free from these problems. The model, however, should be comprehensive, as there are numerous factors contributing to the placement error. The DISPLACE software utilizes a physical model to predict the placement correction map for any layout. When the correction map is known, it can be accepted by any modern EBL system; no mask data modification is needed.

In this paper, we describe the model based mask placement correction, its calibration, and the results of the experimental verification. The verification was done using a complex mask layout that was very different from the calibration mask. The results of the prediction correspond very well to the experimental results.

2. Model Based Placement Correction

2.1. Software based charging correction

Compared to CDL, software based correction is beneficial because it does not induce additional defects and it do not impact the process signature or any other aspect of the regular maskmaking.

A simple method was adopted in CEC by NuFlare. A calibration mask was written, and the placement error was fit by a polynomial function. Good fitting results were achieved and the results of this fitting were used for correction. While correcting the same mask that was used for the calibration shows almost perfect results, the correction of other mask layouts may meet challenges. There is no reason why the correction data on one mask will work on any other layout. This is why the correction displayed improvement on some masks, little or no improvement on others, and even worse error after correction on other masks[8,9].

The physics based correction done by the DISPLACE software showed good results, see[6,7]. The charging effect is dynamic; it depends on the layout, writing order, exposure dose, beam voltage and current, and other factors. The simulation takes much more effort than polynomial fitting of calibration mask, but it brings significant benefits: any layout can be corrected with a similar confidence. If the error map can be predicted, then the placement error can be corrected. The correction can be done by:

a) Direct input of the placement error map into the EBL system: the system deflects corresponding areas during the writing, and in this way, compensates for the placement error induced by charging.

All modern EBL systems have this capability to accept correction maps, if the map is known.

b) Modifying the mask layout by taking into account the correction map. This modified layout can be written on any system, including old systems. The layout modification may need approval of the mask ordering party, in the same way as adding bias to the mask layout prior to writing.

2.2. Physical model of charging correction

The DISPLACE model was further upgraded. The physics causing placement error in maskmaking is complex. In the simulation, the mask is divided into a simulation mesh; the full simulation is done at each mesh cell of the mask. The schematic is shown in Figure 2. The total charge distribution over the mask at any moment of writing creates an electrostatic field; this field deflects the electron beam, creating a positional error.

The physical model utilized in the DISPLACE software considers:

- Charge up by the primary beam
- Charge dissipation, multiple mechanisms

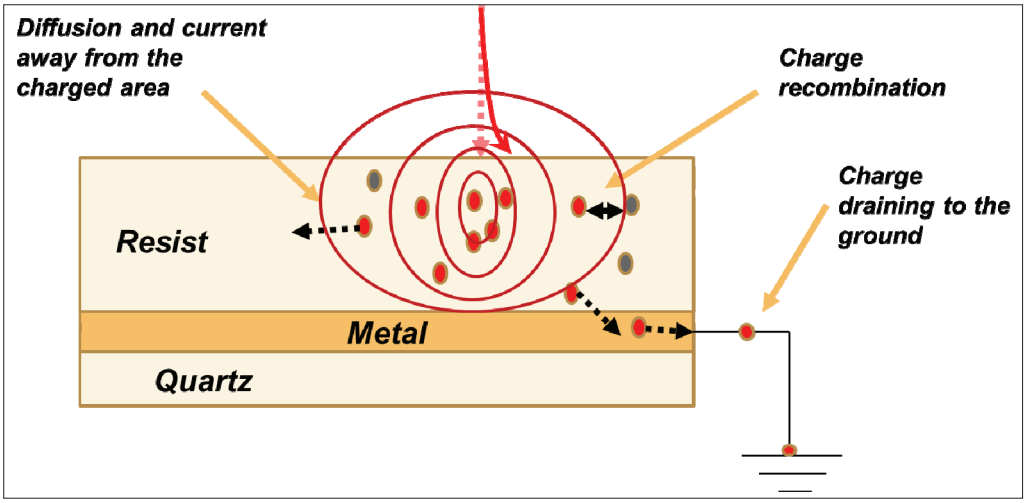

Figure 3. Charging up and discharge involve multiple mechanisms that result in a distribution of the electrical field inside and outside the mask; the field deflects e-beam producing placement error.

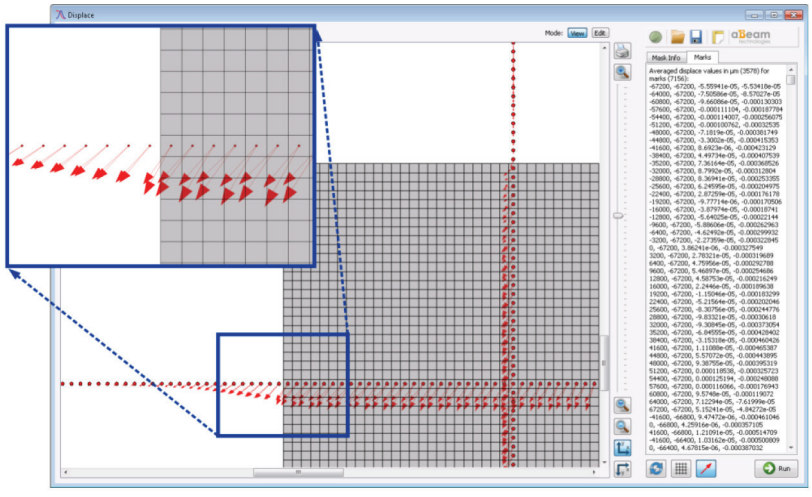

Figure 4. Graphical user interface of the DISPLACE software is easy to use and mostly intuitive. Results of the placement error are shown by arrows in the requested areas, separately for each pass.

- Fogging effect: both charging and dose modification due to fogging
- Proximity effects correction; dose modification
- System parameters such as voltage, current density, and working distance
- Order of exposure
- Timing of writing
- Resist sensitivity
- Modification of resist properties by e-beam
- Mask layout or pattern density map

This complexity of the model is necessary to achieve good results for placement correction.

2.3. Models of resist charge and discharge

During mask writing, the primary electron beam creates positive and negative charges in the resist. In addition, backscattered electrons modify the charge distribution while travelling in the resist. Backscattering electrons also scatter from the bottom of objective lens, creating fogging electrons that add charging over a long range area. These effects result in an electrical field inside the resist and over the resist. The fogging and its effect on placement error were described in[6], where the Monte Carlo software was used for extensive simulations of fogging and an experimental verification of the placement correction accuracy was done using an EBL system.

The discharge is one of the main effects in placement correction; it is time dependent. Multiple mechanisms of discharge are considered in 3D; see Figure 3. In a simplified way they are:

- Electrons and holes travel in the resist under the electrical field distributed inside the resist.
- Electrons drain to the ground
- Electrons and holes recombine
- Modification of resist by electron beam exposure is considered

This charge up and discharge produces complex distributions of positive and negative charge over the mask. The electrical field deflects the electron beam; the amplitude and direction of the deflection is found according to the Poisson equation.

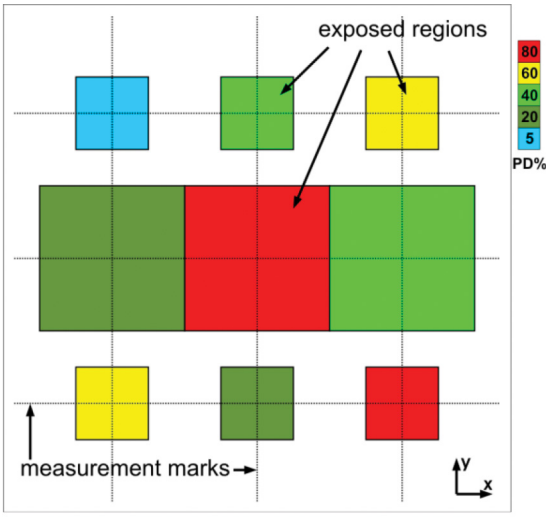

Figure 5. The verification mask layout was developed by Jeol. It is very different from the calibration mask and involves areas with variable pattern densities from 8% to 80%, and with varying sizes and surroundings.

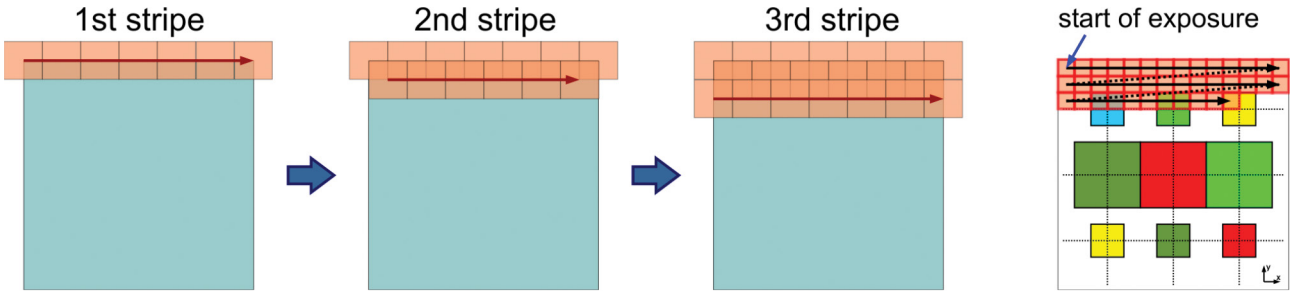

Figure 6. The exposure was done in two passes, with the second pass overlapping the first pass by one half of the stripe width.

3. The Displace Software to Correct Placement Error

The DISPLACE software utilizes the physical model described above. The parameters used as input to the software are:

- Pattern layout: it can be the actual layout or a pattern density map
- Resist parameters: sensitivity and thickness
- System parameters, such as beam voltage, current density, working distance, etc.
- Writing strategy, including number of passes, their direction, stripe width
- Parameters of the model, taken from the calibration

The operator of an EBL system usually knows all these input parameters. The software uses this information to find the necessary details of the mask writing and simulate the charging during the writing. The placement error is simulated for each mesh cell in the sequence shown in Figure 2. The simulation time is proportional to the number of mesh cells and normally takes a few hours per mask. The typical number of cells used is 400x400, 800x800 or more.

The output of the software is the predicted charging distortion map. This map can goes directly into an EBL system for placement correction.

The software utilizes a user-friendly graphical user interface. The interface is easy to use and is mostly intuitive. It is displayed in Figure 4. The arrows represent the magnitude and direction of the simulated placement error in each requested mesh sell. Moreover, the placement error is simulated separately for each pass; the correction can use an averaged value of displacements, or it can use distortion maps to correct each pass separately, further improving the correction accuracy.

4. Model Calibration and Verification

The calibration procedure uses a single mask. The provided calibration layout should be exposed and the placement error should be measured. Based on the measurement results, parameters for the physical model are extracted. The calibration is good for one combination of resist and EBL system. Recalibration using a single mask is needed for every new resist and new type of EBL system.

The model calibration and verification of the software were done using 50 kV variably shaped beam Jeol maskmaking system, JBX-3200MV. The system is used to fabricate masks down to 22/20 nm nodes. A positive tone resist was used for model calibration and verification. The sensitivity was 14 uC/cm2 per pass in a two pass exposure. After the calibration mask was written, an IPRO system was used to measure the placement error on the mask. Using the placement error on the calibration mask, parameters of physical model were extracted.

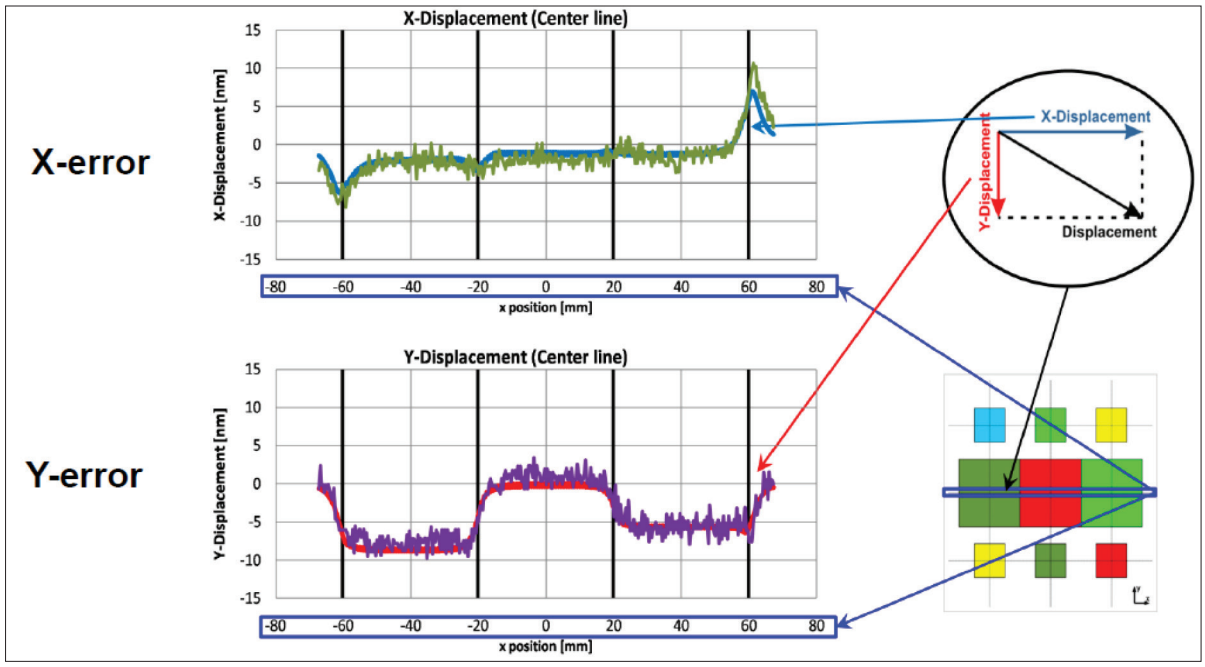

Figure 8. The placement error in a verification mask over the middle horizontal line is shown for the x and y components of the placement error. Smooth lines are the results predicted by Displace, and the noisy lines are the measured results.

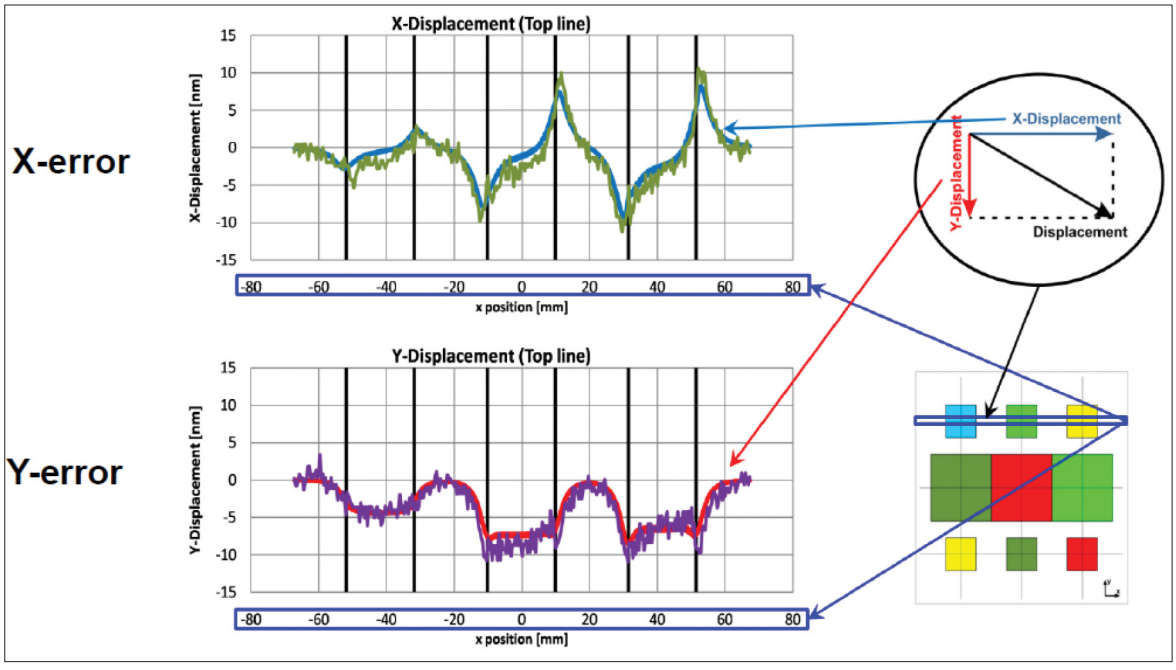

Figure 9. The placement error in a verification mask over the top horizontal line for the x and y components of the placement error are shown. The maximum placement error in the x direction without correction ranges from -10 nm to +10 nm.

For the verification, a mask layout was developed by Jeol. The layout was very different from the calibration mask. It presents the most complex case for the correction, as it involves areas with variable pattern densities from 8% to 80% and with varying sizes and surroundings, from standalone areas to areas directly connected to each other. The verification mask layout is shown in Figure 5.

The exposure of the mask was done in two passes, each pass in the horizontal direction in the Forward-Forward mode, with the second pass overlapping the first pass by one half of the stripe width, see Figure 6.

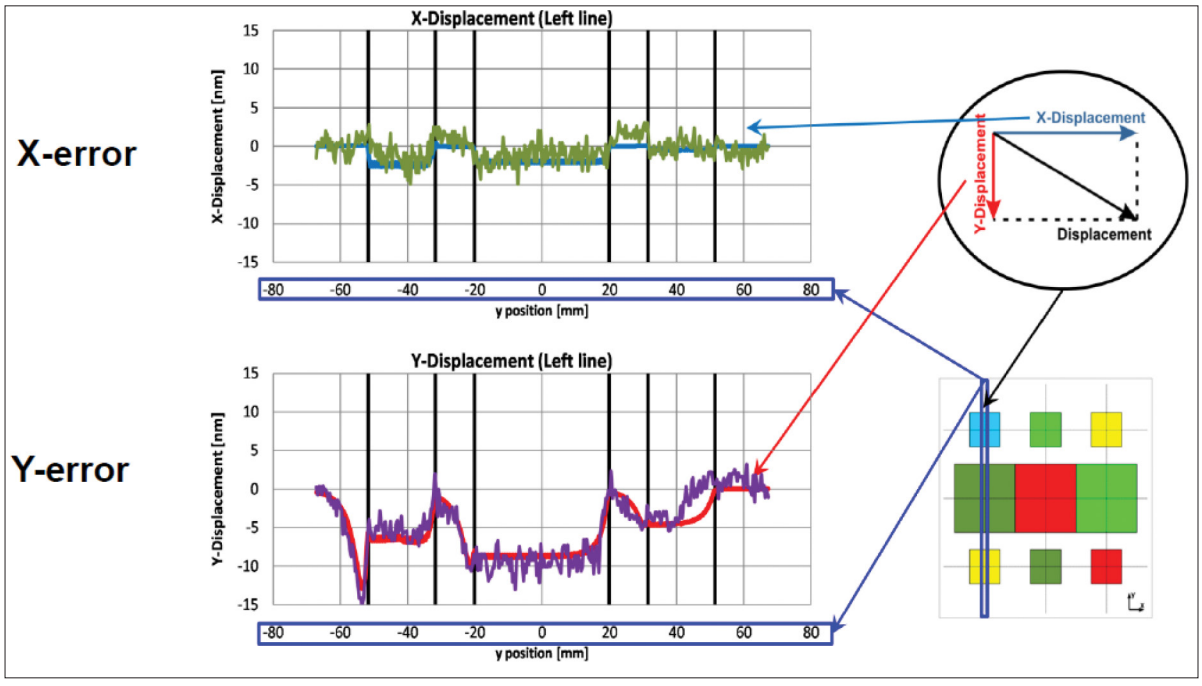

Figure 10. The placement error in a verification mask over the left vertical line for the x and y components of the placement error. The maximum placement error in the y direction without correction ranges from 0 nm to -15 nm.

5. Results of the Verification

The charging placement error was predicted for the verification mask using model parameters derived from the calibration mask. The results are presented in the following graphs, along with the experimental data. Figure 6 displays the placement error measured in the experiment (lines with visible noise) and predicted by DISPLACE (smooth lines) over the middle horizontal line of the mask. The placement error is a vector; it is presented as two components in the x and y directions.

The results of the placement correction for the top horizontal line over the mask is displayed in Figure 9; the results for the left vertical line over the mask is shown in Figure 10.

Note that the signatures of the placement error in the x and y directions differ considerably and depend on the history of the writing. The X-error changes direction over the mask, while the y-error has negative values. The maximum placement error in the x direction without correction ranges from -10 nm to +10 nm and in ydirection from 0 to -15 nm.

A good correlation of the predicted results and the experimental data was found.

6. Conclusion

Improving the placement error in maskmaking is extremely important as it directly affects the fault rate of the fabricated chips, especially in the 20 nm node and below An additional 0.4 nm placement error may increase the fault rate by a thousand times.

The model of the charging placement correction in the DISPLACE software was further improved. The correction is based on an extensive physical model. The calibration of the model was performed using data from a single calibration mask. The verification of the correction accuracy was done using a complex layout suggested by Jeol. Placement errors were predicted for the verification mask by the DISPLACE software and measured.

A good correlation of the predicted and the experimental data was confirmed.

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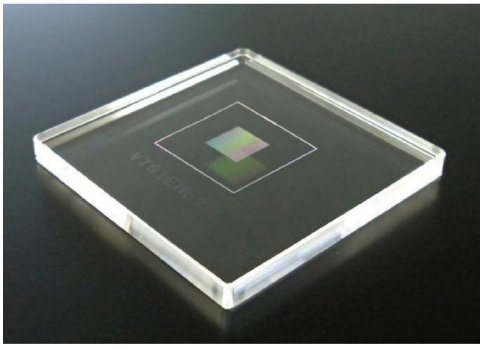
Industry Briefs

Toshiba taps new tech to make flash memory cheaply

By **Nikkei Asian Review,** June 3, 2016



A nanoimprint mold made by Dai Nippon Printing.

TOKYO — Toshiba will adopt new technology to significantly lower production costs of NAND flash memory, one of the restructuring company's core businesses. Researching nanoimprint lithography (NIL) technology together with Dai Nippon Printing and Canon, Toshiba plans to allocate part of the 860 billion yen ($7.9 billion) over three years on the business toward setting up flash memory production lines that utilize NIL.

Production will begin in 2017 in Yokkaichi, a city in Mie Prefecture. Toshiba will then shift to mass production at a new building set to go into operation there in 2018.

Typically, expensive equipment such as special light sources and high-precision lenses are used to form circuits on silicon. NIL presses a template on the wafer like a stamp, and costs related to that production stage will likely plummet by roughly two-thirds. For the entire flash memory fabrication process, Toshiba sees costs falling by approximately 10%.

Moore on his Law and More

By **Rick Merritt,** EETIMES, May 24, 2016

In a video interview from his home in Hawaii, Gordon Moore shared his views on the future of technology including the future of his landmark prediction that has fueled the semiconductor industry since 1965. He also showed at 87 the humble engineer can still laugh at himself. "It would not surprise me at all if we come to end of scaling in this coming decade, but I'm impressed by engineers who keep overcoming what looks like insurmountable barriers," he said in a video shown at the Imec Technology Forum. But when asked about predicting the future he said, "I'm not very good at it. I missed the PC and the importance of the Internet and a lot of things I don't even know about. Predicting major innovations is a tough job. I'll leave that to someone else." Imec chief executive Luc Van den Hove travelled to Hawaii to interview Moore as part of presenting him with a lifetime achievement award. He called Moore's law "a prediction with unprecedented impact…the heartbeat of a global semiconductor industry." Moore also responded to a few just-for-fun questions in the video, showing his wry humor and engineer's mind. Asked if he would prefer a new smartphone or book, Moore said he'd prefer a non-fiction book "to introduce me to a technology area I wasn't very conversant in." Asked if he would prefer to live with no email or no phone he said, "No phone. I do [live without one] already. I carry a phone but it's a send-only phone. I only turn it on when I want to make a call. You can play phone tag, but you don't have email tag," he quipped. Would he prefer to be a deep sea diver or astronaut? "A diver. Astronauts gets committed for a long period of a very boring life," he joked. Finally, does the father of Moore's law prefer beer or chocolate, the Belgium CEO asked. A voting audience was almost evenly split. The correct answer: chocolate. "It's becoming more difficult to scale transistors and we do not automatically get the advantages we used to get in previous generations, but I believe we have solutions to continue Moore's legacy a couple more decades," said Van den Hove whose research institute has been helping push chip technology forward for many years. Engineers need to embrace a smorgasbord of technologies beyond chip scaling, he said. Tomorrow's transistors will morph from today's finFETs to horizontal, then vertical nanowires. "This will keep us busy for 10 years and bring us to at least 3nm," Van den Hoven said. As transitions between nodes slow, engineers will apply the kind of 3-D designs, he predicted. Long term logic stacks with through silicon vias and on-chip optics will emerge. In the medium term, "we are convinced extreme ultraviolet lithography will be essential, and from what I've seen in the last 12 months I'm very convinced EUV will enter manufacturing," he said of the lithography Imec has helped pioneer.

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Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

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