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Best Student Paper - AL14

Production of EUV Mask Blanks with Low Killer Defects

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ABSTRACT

For full commercialization, extreme ultraviolet lithography (EUVL) technology requires the availability of EUV mask blanks that are free of defects. This remains one of the main impediments to the implementation of EUV at the 22 nm node and beyond. Consensus is building that a few small defects can be mitigated during mask patterning, but defects over 100 nm (SiO_2 equivalent) in size are considered potential "killer" defects or defects large enough that the mask blank would not be usable. The current defect performance of the ion beam sputter deposition (IBD) tool will be discussed and the progress achieved to date in the reduction of large size defects will be summarized, including a description of the main sources of defects and their composition.

This paper will discuss the main sources of >100 nm defects in the IBD tool and a path forward for eliminating ~70% of the large defects found during multilayer deposition (i.e., stainless steel and aluminum oxide particles).

1. Introduction

For full commercialization, extreme ultraviolet lithography (EUVL) technology requires the availability of EUV mask blanks that are free of defects. This remains one of the main impediments to the implementation of EUV at the 22 nm node and beyond. Industry progress towards achieving a consistent defect yield and zero defect EUV blank has been elusive. This prompted SEMATECH to concentrate its efforts on identifying the major sources of defects in the deposition tool, implementing mitigation techniques, and demonstrating an EUV mask blank deposition process with a low defect density. The masks for EUVL are, in essence, a Bragg reflector composed of a multilayer periodic structure consisting of molybdenum (Mo)

Figure 1. a) Schematic of Deposition Chamber Showing Position of Mask, Target, and Ion Source; b) Process Module at SEMATECH Showing Different Components.

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EDITORIAL

Another Mask Maker Vacation?

Larry Zurbrick, Agilent Technologies, Inc.

My current involvement with mask making is on the equipment side of the business as a subsystem supplier of position measurement systems. Agilent Technologies[1] is a manufacturer of interferometry lasers, optics and electronics which traces its roots back to Hewlett Packard before being spun out of HP in November 1999.

I recently met with a few customers of our interferometry products for the purpose of aligning our technology roadmaps. The basis of discussion for roadmap alignment was the position measurement error budget. From a high level perspective the assumptions are straightforward. One applies the Gage Maker's Rule to the overlay requirement as the starting point, meaning, one assumes that the position measurement capability needs to be one-tenth of the total overlay error. From there, one lists out the error budget contributors and assigns a portion of the error budget to each. An underlying assumption is that the error contributors are not correlated and add in quadrature. Since one-tenth of a few nanometers overlay requirement is a fraction of a nanometer and the number of error contributors range from ten to fourteen terms depending on system design, error budgets are calculated in picometers to avoid the increasing number of leading zeroes after the decimal point.

As a starting point for updating the position measurement error budget roadmap in preparation for these meetings, I referred to the ITRS 2013 Edition of the Litho Tables which was published a few weeks prior to the scheduled customer meetings (in April 2014.) There were a number of interesting differences noted with respect to both the 2011 Edition and to the historical trends of previous Edition updates. The first was an acknowledgement that the microprocessor/ASIC metal 1 half pitch had stalled in the period from 2010 to 2013 at 40 nm. The second was a change in the DRAM metal 1 node cycle from 3 years to 4 years. The third was a change in of the Flash minimum half pitch bottoming out at 8 nm in the 2011 Edition to 12 nm in the 2013 Edition. Historically, the ITRS Roadmap used to show a three year node cycle, which pulled a node in one year. The 2013 Edition was released on a two year cycle, which essentially accelerated the nodes to a two year cycle. What was going on here!? Perhaps it's the roadmap accounting for reality. From the optical mask requirements standpoint, it appears that mask makers had a two year requirements vacation since the 2013 requirements in the 2013 Edition were the same as the 2011 requirements in the 2011 Edition! Secondly, the one year slowdown in node timing suggests that we may be living in interesting times; that is, the industry is indeed reaching maturity. What does this mean for the mask making industry? It's probably not the same thing as the first mask makers' vacation in the 1980's where masks became a commodity for a number of years. Although half pitch and minimum feature size will not shrink for 193 nm based masks and multiple patterning, overlay will still need to improve to follow the minimum pitch on the wafer. The same is true for overlay requirements in the case of EUV masks. Therefore, continued investment in mask making material, process and equipment technology will be required. In order for the mask making industry to keep ahead of the curve, or least to stay on the curve, the exchange of ideas and developments in the industry needs a venue. This was the one of the original concepts behind the formation of BACUS long ago. As such, today's Photomask Technology conference is an ideal venue to exchange the latest information of what's happening in our industry. See you in September!

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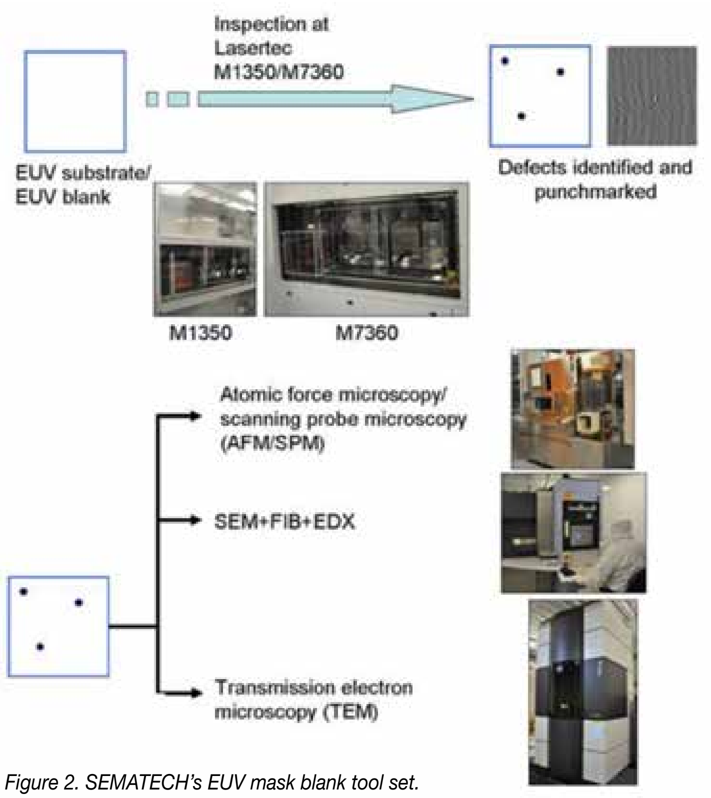


Figure 2. SEMATECH's EUV mask blank tool set.

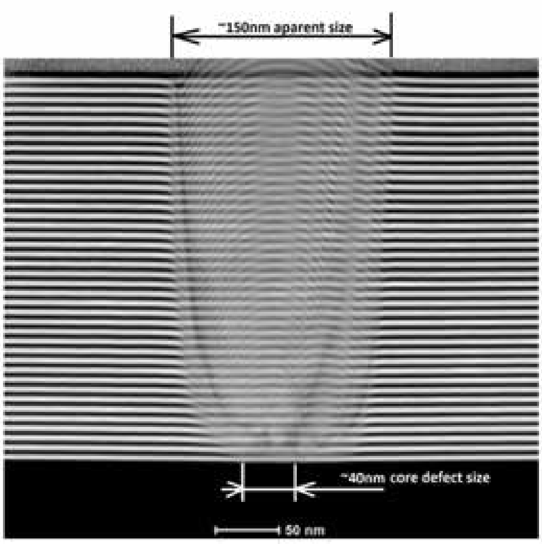
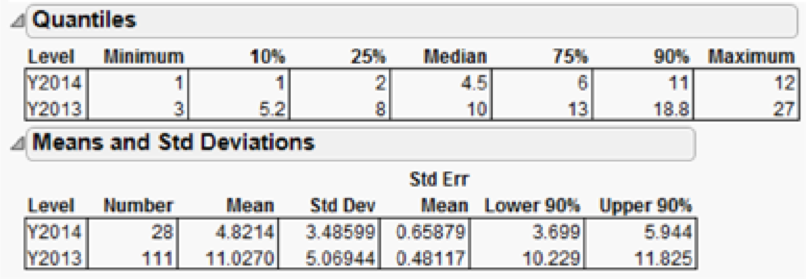


Figure 3. TEM image of substrate defect with core size below the inspection resolution.

Table 1. Distribution of >100 nm particle adders for M19 and M20.



Quantiles

Level	Minimum	10%	25%	Median	75%	90%	Maximum
Y2014	1	1	2	4.5	6	11	12
Y2013	3	5.2	8	10	13	18.8	27

Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean	Lower 90%	Upper 90%
Y2014	28	4.8214	3.48599	0.65879	3.699	5.944
Y2013	111	11.0270	5.06944	0.48117	10.229	11.825

and silicon (Si), a capping layer, and a patterned absorber layer formed on a 6-inch quartz substrate. At SEMATECH, EUV mask blanks have a multilayer structure with a capping layer but without an absorber mask pattern. The main focus for this paper will be on the progress made in the reduction of mask blank defects larger than 100 nm (SiO_2 equivalent). The current defect performance of the ion beam sputter deposition (IBD) tool will be discussed, including a description of the main sources of defects and their composition. The defects can originate on the substrate, during multilayer deposition, or during processing and handling.

1.1 Veeco Low Defect Density Deposition Tools

Veeco Instruments' Nexus low defect density (LDD) tools are used to deposit the Mo/Si multilayer films. Each LDD tool consists of two loadlocks with standard mechanical interface (SMIF) units, an aligner, a transfer module, and the deposition system as shown in Figure 1a and Figure 1b. The deposition module consists of an ion source with Si, Mo, and ruthenium (Ru) water-cooled targets and an electrostatic chuck (ESC) to hold the mask substrates. The ion source uses inductively coupled radio frequency (RF) to create the argon (Ar) plasma inside the source. The Ar ions are extracted through holes in three grids to produce a low-divergence ion beam with a typical energy of 600 V at a current of 300 mA. The grids are dished so that each beamlet overlaps the center of the target, resulting in an erosion spot on the target center ~3 inches in diameter. The Ar supplied to the chamber produces a background pressure of 0.14 mTorr; the base pressure of the system is ~1E-08 Torr. The target turret contains up to four 12-inch diameter targets. The chamber walls are lined with stainless steel shields which

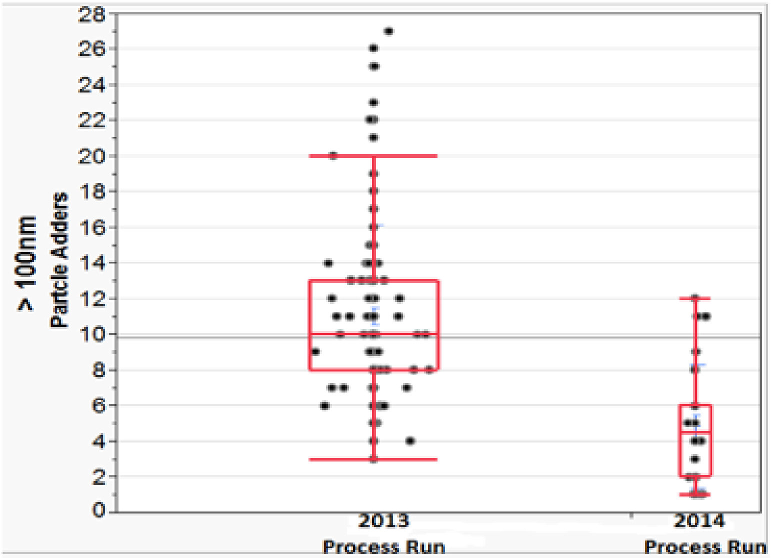


Figure 4. Particle adders for M19 and M20.

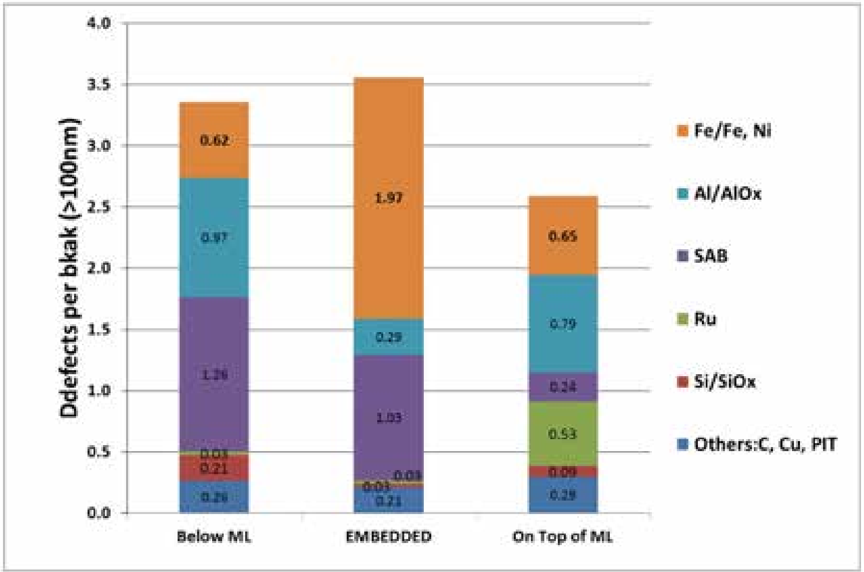


Figure 5. Failure analysis data from M19.

were roughened using an aluminum oxide grid blast process. The surface texture must be rough enough to hold the coating successfully, but clean enough that it does not add defects to the process.

1.2 SEMATECH Suite of EUVL Mask Tools

SEMATECH has a complete set of EUV mask blank tools installed in the Mask Blank Development Center (MBDC), as shown in Figure 2. To find substrate or mask blank defects, SEMATECH uses a Lasertec M1350 inspection tool with a resolution down to ~65 nm, and a Lasertec M7360 with a resolution down to ~50 nm. Defects can be further analyzed using atomic force microscopy (AFM), focused ion beam/scanning electron microscopy with energy dispersive spectroscopy (FIB/SEM+EDS), and transmission electron microscopy (TEM).

SEMATECH follows a standard process flow which can be divided in two parts: before deposition processes and after deposition processes. Before deposition, the process flow focuses on substrate preparation and quality and includes industry-standard substrate cleaning (SP_1, $H_2SO_4+H_2O_2$), substrate inspection, and quality screening. After multilayer deposition on the Veeco Nexus IBD tool, the process flow is geared towards determining the deposition-added defects and composition analyses of the defects. Specifically, the freshly-produced mask blanks are inspected on the M1350, a

Figure 6. Aligner and several backside defect maps showing the signature of the aligner failure.

defect adder is generated and split in two size categories to be submitted for failure analyses. Defects above 100 nm to 150nm are sent for SEM+EDS analyses; smaller defects are sent for TEM analyses.

This paper will focus and report on large defects (>100 nm SiO2 SEVD equivalent). From experiments performed at SEMATECH, we found that most large defects are deposition- and/or process-generated defects. We also found that more than half of the defects between 70–100 nm are, in fact, substrate decorated defects. This defect decoration effect has been previously published and is well understood. In Figure 3 we provide an example (TEM image) of a substrate defect with a core size below the inspection resolution. This defect, after multilayer deposition, is decorated more than 3X its core size. This is an extreme example—the majority of defects decorate much less. The 100 nm defect size "cutoff" is arbitrary, but we find it to more accurately reflect the deposition tool performance.

2. Results

2.1 M19 and M20 Process Runs

M19 and M20 are process runs performed at the end of 2013 and the beginning of 2014, respectively, in SEMATECH's "PM1" Nexus tool. M19 was stopped when defect levels increased after a few hundred blanks had been coated. M20 is still early in its run and we are reporting on preliminary data here.

Before each process run, the shields were removed, the ion source was rebuilt, the targets were replaced (if required), the chamber was cleaned, and the shields were replaced. After this maintenance process was completed and the chamber requalified, then one hundred mask blanks were produced to assess the cleanliness of the maintenance procedure and tool.

Figure 4 shows defect data for M19 and M20, while Table 1 gives descriptive statistics for the data. M19 achieved a median of 10 added defects >100 nm per blank. This is comparable to our previous best defect level which had a median of 11 added defects. The initial M20 data looks even better with a median of five added defects >100 nm per blank. The remainder of this paper will describe the observations and tool changes made to achieve this improvement.

2.2 M19 Failure Analysis

Failure analysis was performed on 34 blanks during M19. All defects >100 nm, based on the M1350 inspection, were looked at and 323 defects were located. Failure analysis provided the EDS-measured composition of the defect core, an image of the defect shape, and the location of the defect vertically—under, in, or on the mask multilayer. Figure 5 shows the failure analysis data for M19. The data show a large defect component consisting of stainless defects (containing Fe, Ni-) that were primarily in the multilayer. The data also contain a large "same as background" (SAB) component below and in the multilayer. SAB means the EDX signal from the defect core was indistinguishable from the background signal near the defect, normally Mo/Si. The third major component was an AlOx signature primarily below and above the multilayer.

2.3 AlOx Defects from the Aligner

Several experiments were performed between M19 and M20 to identify the root cause of the AlOx defects seen in M19. As the defects were predominantly located below and on the multilayer, handling defects were suspected. The experiments quickly focused on the mask aligner in the robotic transfer chamber. Figure 6 shows a top-down view of the aligner and adder maps of backside substrate inspection resulting from

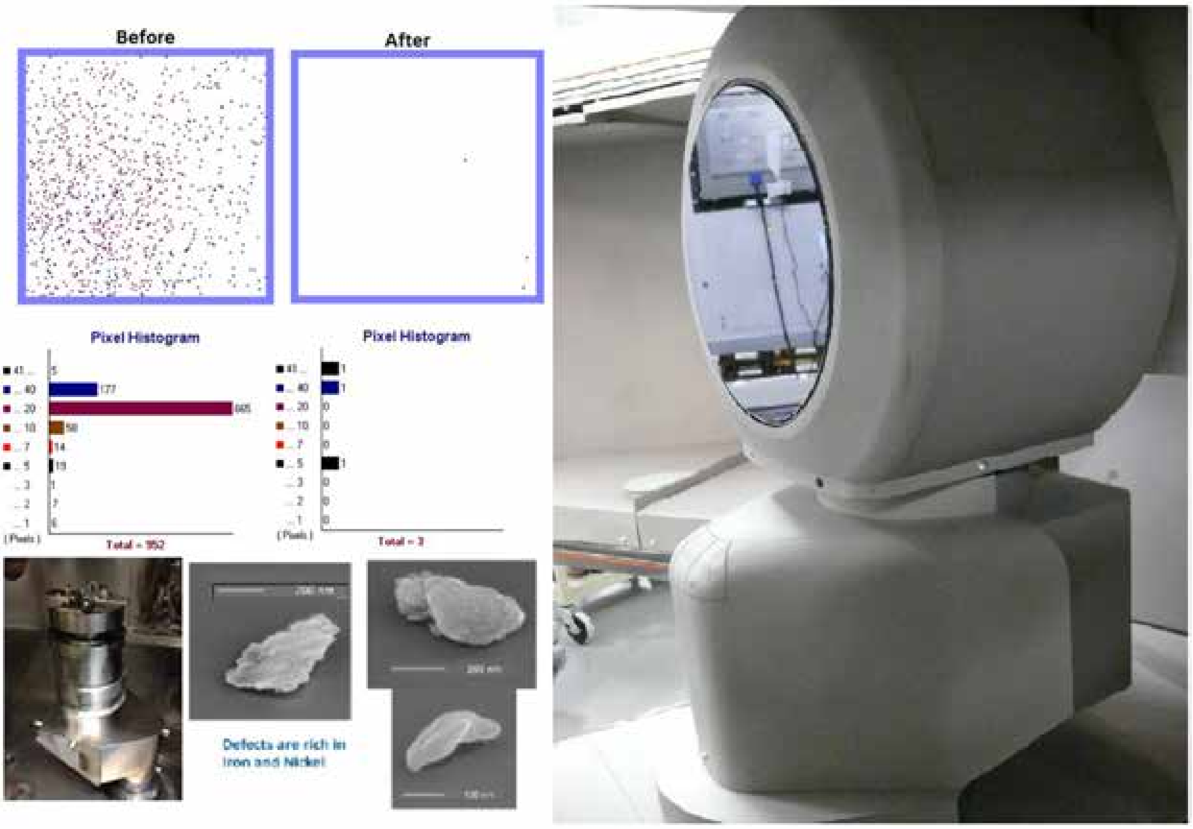


Figure 7. Defect data and pictures related to the target turret defect source.

performing several aligner experiments. The aligner was statistically identified as the defect source using multiple cycle experiments (the average top surface substrate defect level was 2 per pass with no clear spatial pattern). Once the problem was identified, it was discovered that the back side of the mask saw many more defects, in a clear pattern on the mask. Figure 6. Several defect maps of typical backside defect patterns from the failing aligner are also shown in Figure 6.

2.4 Stainless Steel Defects from the Target Turret

Based on the M19 defect distribution, it seemed most likely that the stainless steel defects were coming from the deposition chamber during deposition. Using aggressive multiple cycle tests, the defects were traced to the target turret. The ferrofluidic feedthrough for target indexing was replaced and the target turret was re-adjusted. Figure 7 shows the assembled/disassembled target turret, and the defect maps for identical experiments performed before and after the target turret feedthrough replacement. Replacing the feedthrough greatly reduced the defects on the mask. The defects seen before the replacement were indeed stainless steel in composition.

2.5 Y-axis Feedthrough Defects

During identification of the target turret defects, another defect source was discovered in the mask fixture. After several partitioning experiments, we found that the mask fixture y-axis motion was adding defects. The y-axis ferrofluidic feedthrough was replaced with a new model and the defect source was eliminated. Figure 8 shows an image of the feedthrough that was removed. A large discolored region is visible which we feel is a further indication of feedthrough failure. Figure 8 also shows defect data from identical experiments performed before and after the feedthrough replacement. The clear signature of defects clustered around the top edge of the mask disappeared after the feedthrough was replaced.

2.6 M20 Results

After these changes were made to the deposition tool (aligner, target index and mask y-axis feedthroughs), another process run was begun. Figure 4 shows the preliminary large defect adder data from M20 compared to M19. The median defect count was reduced from 10 to 5 added defects >100 nm (SiO_2 equivalent). Not only was the total defect number significantly reduced, but the defect composition was significantly different between M19 and M20, as would be expected since we had attacked the major defect sources in the interim. Figure 9 shows the failure analysis data for M20. Between M19 and M20, stainless steel defects were reduced from 3.24 to 0.125 per mask blank. Alumina defects were reduced from 2.05 to 0.50 per mask blank.

Early in the M20 run, we found that one to three Ru defects were added to the multilayer blanks produced. This was approximately a 4X increase of Ru-type defects compared to M19. During the second part of M20 we changed our process—leaving mask blanks Si-capped instead of Ru-capped—and the Ru defects disappeared. The speculated cause of the Ru defects is either the age of the Ru target and/or surface nodule

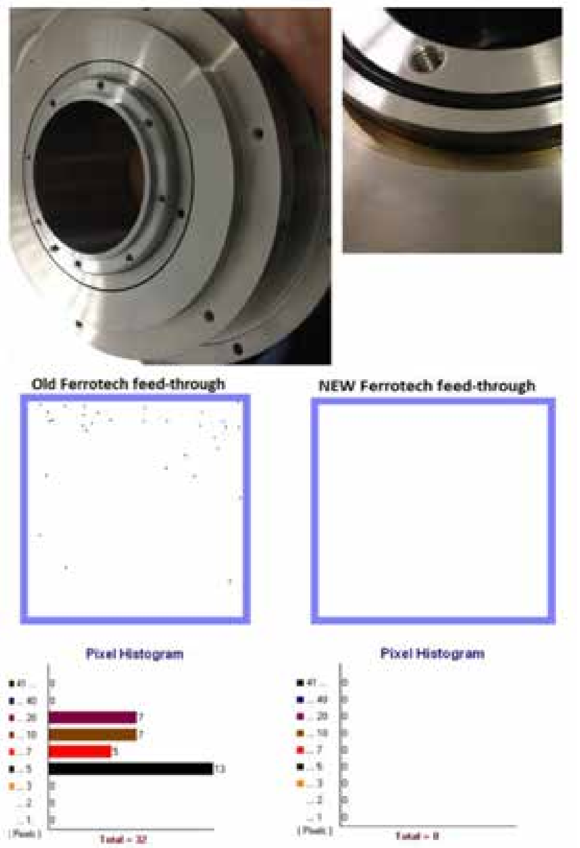


Figure 8. Image of the y-axis ferro-fluidic feedthrough showing discoloration, and defect data from identical tests performed before and after the feedthrough was removed.

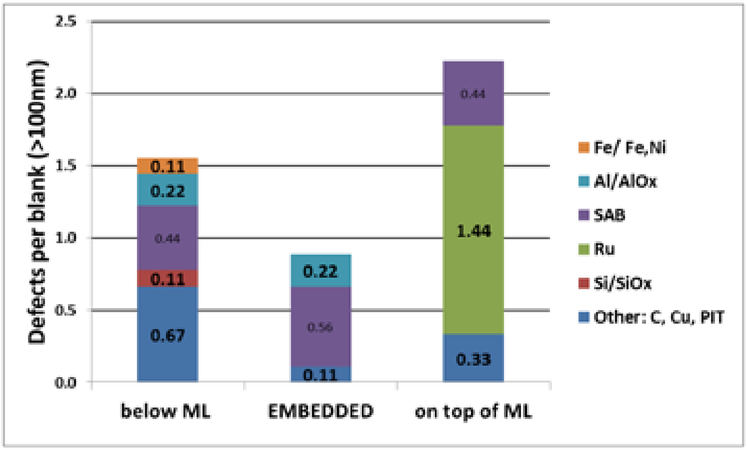


Figure 9. Preliminary failure analysis data for M20.

formation. This will be investigated during the next scheduled maintenance.

3. Conclusions

The current mask blank specification for defectivity is zero defects above 80 nm and 10 defects or less at the inspection sensitivity between 50–80 nm. SEMATECH has achieved its best defect performance during the current process run, lowering large (>100 nm) mask blank defect adders by a factor of 2, from 10 defects per blank down to less than 5 per mask blank. The 50% percent defect reduction was accomplished by fully utilizing the MBDC tool set to determine where the defects were coming from and then attacking the major defect sources. Two poorly performing feedthroughs were replaced and one component, the aligner, was bypassed. The target indexing feedthrough was found to be adding 34 stainless steel type defects per mask blank. By bypassing the aligner, we further eliminated 80% of the AlOx type defects. As a result of these actions, the defect level seen at the beginning of the current process run (M20) is the lowest we have ever seen. The defect Pareto has also changed significantly with the reduction in stainless steel and alumina defects in the latest data.

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Industry Briefs

SEMATECH Achieves Breakthrough Defect Reduction in EUV Mask Blanks

SEMATECH announced reaching a significant milestone in reducing tool-generated defects from the multi-layer deposition of mask blanks for extreme ultraviolet (EUV) lithography, a significant step toward readiness for high-volume manufacturing (HVM).

Following a four-year effort to improve deposition tool hardware, process parameters and substrate cleaning techniques, technologists at SEMATECH have, for the first time, deposited EUV multilayers with zero defects per mask at 100nm sensitivity (SiO2 equivalent), on a 40 bi-layer Si/Mo film stack and measured over the entire mask blank quality area of 132×132 mm2. Eliminating these large “killer” defects is essential for the use of EUV in early product development.

In addition, by subtracting out incoming substrate defects, SEMATECH has demonstrated that the multilayer deposition process itself can achieve zero defects down to 50nm sensitivity. Coupled with novel improvements to the mask substrate cleaning to remove incoming defects, this represents the capability to both extend EUV to future nodes by eliminating smaller “killer” defects, and as a step to reducing smaller defects (which can be mitigated) to a level where improved yield and mask cost make EUV more cost-effective for HVM.

According to Kevin Cummings, SEMATECH’s Lithography manager, SEMATECH’s programs continue to produce the results that our members and the industry need to show that EUV lithography is manufacturable, such as mask blank defect reduction, more efficient deposition and cleaning, effective reticle handling.

Imec Launches R&D Tool Hub

Mark LaPedus

To help fab tool vendors, Imec has launched a new R&D hub, with ASML and Lam as the first members. The semiconductor industry is entering yet another inflection point. Consumers want faster mobile systems with more functions. So, chipmakers are under pressure to deliver new low-power chips that are smaller and faster. The problem is that IC design and chip manufacturing costs continue to escalate. These costs, in turn, are fueling an ongoing shakeout in the chip and fab tool industries, leaving only a few chipmakers and fab tool vendors which can afford to play at the leading edge.

“Fewer companies need to address more challenges,” said Luc Van den hove, president and chief executive officer of Imec, during a keynote address at the Imec Technology Forum (ITF2014) in Brussels, Belgium. The trends are especially challenging for fab tool vendors. IC equipment vendors must continue to spend more in R&D to address the leading edge. But yet there are fewer and fewer customers for vendors.

To help fab tool vendors, Imec has launched what it calls a “suppliers hub” program aiming to offer an open R&D platform and enable chip suppliers and tool makers to collaborate more deeply and in an earlier stage in the process. Suppliers joining Imec’s supplier hub have the ability to assess their tools on product stacks, develop process control and hardware/software options, and integrate new materials.

Imec has been working with fab tool vendors and materials suppliers for decades. The new suppliers hub increases the level of collaboration. In fact, ASML Holding has been one of the early participants of the suppliers hub. ASML and Imec recently launched an advanced patterning center, which formed the basis of the suppliers hub.

EUV Nudges Toward 10nm

Rick Merrit

BRUSSELS — The latest extreme ultraviolet (EUV) lithography systems are making about 28 wafers/hour or 100 wafers/day with a 40 W light source in pilot tests. The progress is significant but falls far short of a production target of up to 200 wafers/hour for the systems upon which ride many of the hopes of the semiconductor industry.

ASML chief technology officer Martin Van den Brink reported the results achieved over the last three months, raising hopes for a handful of EUV proponents at the annual Imec Technology Forum here. The systems could be available in 2016, in time for the 10 nm node, but it’s a nail biter at best, given the many challenges ahead. “Over time I am convinced we will get to 100-200 wafers/hour with higher numerical aperature — that will give us another 10 years” of new chipmaking capabilities, Van den Brink said.

Initially, ASML hopes to stabilize the systems for commercial production at about 85 wafers/hour for work at 10 or 7 nm nodes. Ultimately it hopes to deliver systems producing 100 to 200 wafers/hour with a higher numerical aperture, better resists, and an improved light source, slashing costs as much as six-fold for the 5 nm node.

Despite the optimism, based on ASML’s work on future immersion tools that could handle work from 10 nm to 5 nm nodes, one can predict that, if such tools are used at 10 nm, the amount of multi-patterning they require could push chipmakers far off the curve of Moore’s Law, said Kurt Ronse, Imec’s lithography expert. Immersion tools may require 18 masks at 10 nm and 27 masks at 7 nm, driving up costs 35% and 21% or more, respectively, an “unsustainable” level. By contrast, a hybrid process would use eight immersion and six EUV masks, keeping cost increases for the 7 nm node to about 7%.

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About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

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