PHOTOMASK

BACUS—The international technical group of SPIE dedicated to the advancement of photomask technology.

July 2013
Volume 29, Issue 7

Invited Paper

Consideration for High-Numerical Aperture EUV Lithography

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ABSTRACT

With numerical apertures > 0.4 there will be broad ranges of angles of incidence of light on masks for EUV systems with 4x lens reduction, leading to several undesirable consequences with current MoSi multilayers and tantalum-based absorbers, An option for reducing the range of incident angles is to increase the lens reduction, but this entails small field sizes with standard 6” mask for factors or necessitates the use of larger masks sizes. Small fields lead to a need for stitching or accepting substantially reduced throughput – a problem for a technology already challenged with respect to cost-of-ownership. The implementation of larger mask formats is straightforward but requires considerable investments in new tools for mask making. New absorbers may provide a solution for high-NA EUV lithography at 4 lens reduction, but much R&D is required to demonstrate that this approach will work.

1. Introduction

High-numerical aperture EUV lithography involves larger chief ray angles for light incident on masks as well as a larger range of angles about the chief ray than occurs with small numerical apertures. The ipact of these larger angles can be seen in Fig. 1, which shows pattern placement errors due to mask 3D effects for half-pitch size features across a range of pitches for EUV lithography with NA = 0.45 and a lens reduction of 4x. Such non-telecentricity-induced placement errors are on top of the conventional edge shifts due to linewidth variation resulting from imperfect control of focus and dose, as well as line-edge roughness.

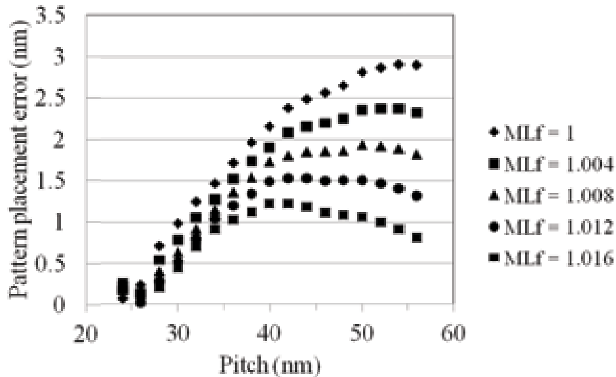

Figure 1. Simulated pattern placement errors (resulting from mask 3D effects) of equal lines and spaces through 100 nm focus range, over a range of pitches, for exposures on a 0.45 NA EUV exposure tool with 4x lens reduction using quadrupole illumination (σ_{inner}=0.55,σ_{outer}=0.84). MLf is the multilayer expansion factor and represents the thicknesses of the Mo Si layers divided by their nominal thicknesses. Mo/Si intermixing is assumed for all cases, but constant for all cases.

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Editorial

ASMC Minutes

Jacek Tyminski, NIKON Precision Inc

The 23rd, IEEE/SEMI Advanced Semiconductor Manufacturing Conference, ASMC, took place in Saratoga Springs, NY 14-16 May, 2013. Traditionally the conference is a forum to review a wide range of semiconductor manufacturing topics. This year's edition was attended by over 300 representatives from GLOBALFOUNDRIES, IBM, Intel, Toshiba, TSMC, Micron, Infineon, Applied Materials, ASML, KLA-Tencor, and representatives of other IC makers, as well as tool and material suppliers, and members of academia. Among the participants, GLOBALFOUNDRIES had by far the strongest representation, most likely because of the proximity of one of GLOBALFOUNDRIES fabs.

The single-track conference included 15 oral sessions with sixty presentations plus a poster session with 20 posters. The sessions focused on a wide range of manufacturing topics such as advanced patterning, design for manufacturing, 3D and through-silicon vias (TSV), metrology, defect Inspection, yield enhancement, advanced equipment, processes, and materials and factory optimization. The conference three keynotes, two tutorials and a panel discussion addressed key issues at the intersection of technology and business.

Subramani Kengeri, Vice President, Advanced Technology Architecture at GLOBALFOUNDRIES, pointed out that the technology costs do not keep up with Moore's Law, with double patterning being the key cost driver. Kengeri pointed out that return on investment is also diminished by the increased development costs of the new designs. The cost is going to escalate through 14 nm design node. The complexity of industry ecosystem increases the time between development and high-volume manufacturing of the new technologies. Design process productivity becomes a major factor for new technology development, driving demands for IC design tools.

Vivek Singh, Intel Fellow, pointed out that computational lithography provides a cost effective means to explore new technology options. The gap between device CDs and the imaging wavelength is bridged by computational lithography and design-process co-optimization. Moving forward, the expectation is that 14-nm and 10-nm node devices will be manufactured with immersion ArF double-patterning (iArF DP), while the EUV will be used in pilot lines. However, iArF extensions will require source-mask co-optimization (SMO), involving inverse lithography technology (ILT). Currently, the key ILT challenge is scaling the masks solutions to the chip full field size. Singh stressed that ILT is non-intuitive, i.e. mask layouts do not resemble the target patterns. Also, ILT solutions are strongly dependent on the illuminator design, requiring a link between SMO and ILT.

Tim Hendry, Vice President, Technology and Manufacturing Group, Intel Corporation, discussed materials challenges in high volume manufacturing (HVM). He pointed out that the new technologies introduced to HVM put new demands on quality control of the old and new materials used in IC manufacture. However, the material supply chains are complex, and, to meet the material requirements, the quality control culture must be embedded in the entire supply chain. All of this can lead to increased material costs. Intel proactively engages with the suppliers at the materials production flow design level to control the costs of the materials.

The conference also included a panel discussion, "450mm Wafers – Supersize Me!" moderated by Paul Farrar, Director of Global 450 mm Consortium, G450C. Its members included State University of New York College of Nanoscale Science and Engineering, GLOBALFOUNDRIES, IBM, Intel and TSMC. The current staff

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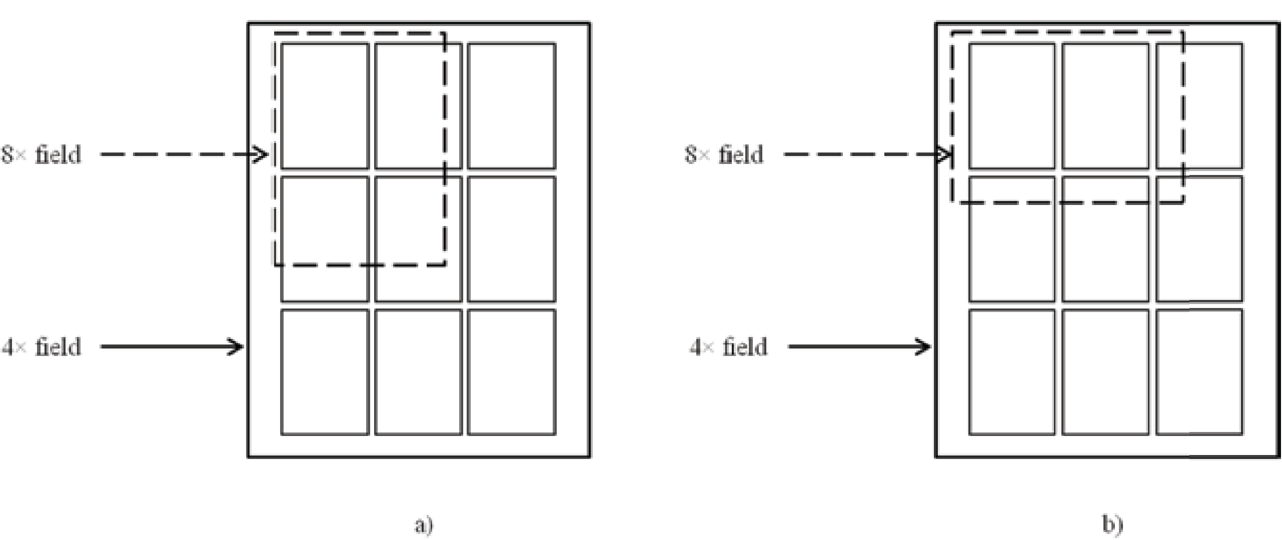

Figure 2. 3x3 arrays of dies in 4x and 8x reticle fields. a) the 4x and 8x fields are scanned in the same direction; b) the 4x and 8x fields are scanned in perpendicular directions.

The magnitude of these errors can be reduced by modifying the multi-layer space,[1] but at the expense of significantly reduced mask reflectivity and system throughput.

A number of options have been proposed to mitigate the problems associated with larger chief ray angles, such as an increase in lens reduction and modifications of the mask multilayers and absorbers. In this paper, the implications of these proposals will be assessed, largely from the viewpoint of a foundry, i.e., a company that fabricates a large variety of integrated circuites – primarily – and makes a large number of masks.

2. Larger Lens Reduction

2.1 Illustration of the problem

The challenges associated with larger lens reduction can be understood by contemplating a specific hypothetical situation. Consider a technology in which the EUV layers are exposed using lenses with 8x reduction and masks are standard 6 inch format, while optical layers are exposed using conventional 4x lenses and 6 inch masks. Suppose the die to be fabricated has an area of 7 mm x 10 mm on the wafer. In this case, a 3x3 array of dies fills a 4x reticle field. As can be seen in Fig. 2, there are a number of options for exposing some layers with exposure tools with 8x lens reduction and other layers with 4x lens reduction and the same 6 inch mask form factor:

1. No stitching
2. Stitching along in the vertical dirction
3. Stitching in the horizontal direction
4. Stitching in both directions.

2.2 No Stitching

From a design, layout, and process perspective, no stitching is simplest. For the example shown in Fig. 2a), an 8x system would result in a single die reticle, necessitating die-to-database mask defect inspection. The amount of unique scribe area is ~ 1/9 that the full field, limiting the area for process monitors that can be placed on the wafer. Moreover, nine times more exposures will be required than for 4x systems. The issue of throughput will be discussed later in this section.

The situation depicted in Fig. 2a) results in an interesting overlay control problem. One can expect that the 8x layers will be the critical layers, and it would be typical in situations in which 4x and 8x systems are mixed that the overlay of concern due to multiple field sizes is that of less critical layers to the most critical ones. In the scenario under consideration in this section, that means the primary overlay challenge is that of getting the larger 4x layers to overlay the smaller 8x layers. The overlay problem involved with optimizing overlay of the larger field to the small field has been considered previously when the grids of the smaller and larger fields are fully commensurate.[2] This is the case that arises from Fig. 2a), but the configuration depicted in Fig. 2b) is a new situation. This can be seen in Fig. 3. In this situation, 8x exposures #1 and #3 lie completely within 4x exposure fields, but exposure #2 straddles two 4x fields. When all three rows of the 4x field are taken into account there are 9 distinct situations for 8x fields laying within 4x fields. This greatly increases the complexity of mix-and-match of non-critical layers to critical layers. While it is probable that the smaller 8x field will result in easier overlay control between critical layers, there would likely be a degradation in overlay for non-critical layers.

If it is necessary to align 8x fields to 4x fields, then nine process control loops are needed for controlling overlay. The need for this can be appreciated by considering a simple overlay error, one of isotropic field magnification for the 4x fields. In circumstances where the 4x and 8x fields are scanned in the same direction, the problem of incommensurate fields can still arise, as shown in Fig. 4.

2.3 Stitching

The problems associated with incommensurate fields described in the prior sub-section could reduced in difficulty by the use of stitching, so that the 8x and 4x grids are commensurate, but this involves a different set of problems, perhaps even more difficult to solve. A geometry crossing a stitching boundary is illustrated in Fig. 5. For geometries that cross boundaries between the parts of the stitched fields, critical dimension and overlay errors lead to distortion of features that

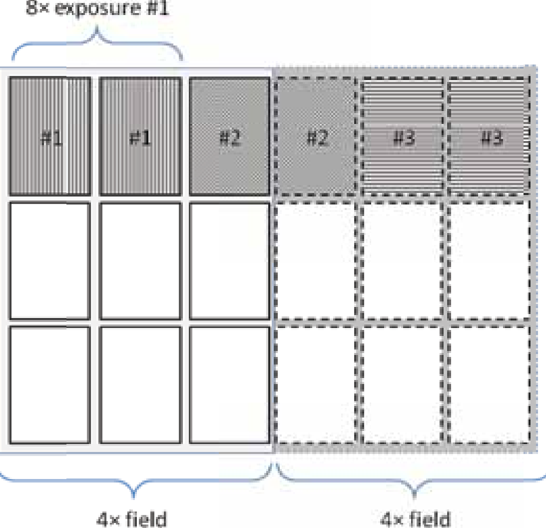

Figure 3. Configuration for overlay between 4x and 8x reticle fields.

are not as intended by design. Because all parts of the stitched fields can be exposed without removing the wafer from the chuck of the scanner, critical dimension control and overlay control can be expected to be better than the typical lot-to-lot variation seen in manufacturing, but will still be extremely difficult to have the level of control needed for critical features to cross stitching borders. Performance-dependent features, such as gates and fins, or reliability-dependent features such as metal lines, should not be stitched. Such restrictions would be very difficult to manage for products produced in foundries. For a foundry which is expected to make wafers for a large number of designs, stitching represents a significant challenge. Restricting critical features so that they cannot cross stitching boundaries might be considered for a small number of standard products, but will likely not be well received by foundry customers.

Stitching across boundaries that are perpendicular to the scan has the advantage that the exposures on both sides of the stitch boundary will be exposed with the same part of the lens. Hence the features on the two sides of the boundary will be subject to the same lens aberrations. For stitching along the other direction, the features exposed on the two sides of the boundary will be subject to aberrations on opposite sides of the lens slit.

Stitching would be particularly difficult for EUV lithography, where there is often some residual reflectance from the absorber of a few percent. One proposed solution for avoiding overexposure at the edges of fields due to the light reflected from the absorbers of neighboring fields is to etch away the multilayer around the exposure field. Such a “black border” reduces this problem when there are scribe lines between adjacent exposures but is probably lacking the acuity needed for stitching fine features. Alternatively, a double-absorber stack could be adopted, as used frequently for optical attenuated phase-shifting masks. Software could also be used to compensate for reflections from absorbers, but would greatly complicate mask data preparation.

2.4 Throughput

Regardless of which 8x~ scenario is adopted, throughput will be reduced substantially. With a smaller field, the EUV light can be concentrated in a smaller area, resulting in ~2x~ higher light intensity at the wafer plane. As long as EUV tools are throughput-limited because of light intensity, this reduces the impact of needing to expose more fields with 8x~ than with 4x~ lens reduction. However, it doesn’t reduce the problem entirely. If we consider the situation depicted in Fig. 2b), 4.5 times more fields need to be exposed with 8x~ lens reduction than with 4x~, while the light intensity improvement only provides ~2x~ relief. However, the 8x~ exposure field is only 14 mm in the scan direction, while the 4x~ field is scanned 30 mm. This might appear to recover another factor of 30/14 ≈ 2.1x~ in throughput, but it isn’t quite so. Because the actual length of the scan needs to be the field length plus the height of the slit, there is greater loss of relative efficiency for smaller fields. This can be seen as follows. Suppose the effective slit height (slit height plus curvature) is 5 mm. Then the 4x~ field must be scanned 35 mm, while the 8x~ field must be scanned 19 mm. The actual gain in throughput due to the smaller field in the scan direction for the 8x~ system is somewhat less: 35/19 ≈ 1.8x~.

In equation form, the exposure time for a scanner is given by:

$$t_{exp} = \frac{S}{I}\left(\frac{H_F + H}{H}\right) \quad (1)$$

where I is the average light intensity, S is the resist sensitivity, H_F is the scan length and H is the effective slit height. The impact can be appreciated as follows. A simple equation for estimating scanner throughput is

$$\text{Throughput (wafers per hour)} = \frac{3600}{t_{OH} + N(t_{exp} + t_{step})} \quad (2)$$

where t_{OH} is the overhead time per wafer, which primarily involves the time to exchange wafers, t_{exp} is the amount of time when resist is being exposed in a single field, and t_{step} is the time between the end of one exposure and the start of another. All times are measured in seconds, and N is the number of fields being exposed. If we use some typical values for these

Table 1. Throughtput for 4x and 8x scenarios, assuming that the light intensity for 8x systems is twice that of 4x systems. A small reduction in t_{step} is estimated due to the smaller field.

	4× scenario	8× scenario	8× scenario with throughput enhancements
t_{OH} (secs)	5	5	2.5
t_{step} (secs)	0.12	0.10	0.05
t_{exp} (secs)	0.10	0.027	0.027
N	120	540	540
H_F (mm)	30	14	14
H (mm)	5	5	5
Throughput (wph)	115	49	82

Table 2. Tools required for making masks.

Infrastructure	Mask shop	Wafer fab
Substrate fabrication	Beam writer	Defect inspection tools
Multilayer/absorber deposition	Resist coat	Mask cleaners
Defect inspection	Defect inspection	Stockers
Reticle carriers & pods	Defect repair	Automated mask handling
Cleaning tools	Cleaning tools	Reticle carriers & pods
Flatness measurement	Etchers	Reticle pod cleaner
Reflectometers	AIMS	
	CD/profile measurement	
	Registration measurement	

parameters (Table 1), then the calculated throughput for the 4x~ lens reduction situation is 115 wafers per hour (wph), while the throughput is less than half of that for the 8x~ situation. For a technology that already needs cost-of ownership improvement, this is not attractive. It can be seen that cutting the overhead time and stepping times in half still leads to much lower throughput than with 4x~ systems.

The issues associated with larger lens reduction were exemplified through a specific example. Clearly the impact on productivity is dependent on die size and aspect ratio, but regardless, larger lens reduction for EUV lithography results in a number of throughput and technical challenges. The specific example of 8x~ lens reduction was discussed. It does have the potential advantage of providing commensurate 8x~/4x~ layouts, but this would entail stitching or substantial losses in throughput. Lens reductions other than 8x~ can be considered, and the specific example of 6x~ is discussed in the next section.

3. Larger format masks

A large mask format (230 mm) was considered many years ago[4] but has never been used in large scale integrated circuit manufacturing. This larger format was developed in anticipation of extremely large DRAM die sizes that never materialized, and without motivation, the 230 mm format was shelved. With larger lens reduction under consideration for high-NA EUV lithography, it is natural to revisit this larger format.

Listed in Table 2 are the tools that are needed for making masks. Adoption of larger masks will require versions of each of these tools (of which there are a considerable number) capable for 230 mm masks. For many of these tools, such as defect inspection, reflectometry and CD measurement, nearly all of the changes from tools capable of handling 6 inch masks will not involve the most critical aspects of the tools' capabilities, but the substrate handling will need to be modified to accommodate the larger sized substrate. For other tools, particularly those related to substrate fabricationand multilayer deposition, substantial development will likely be required due to the critical requirements for substrates and blanks.

A larger lens reduction does make a few things easier for mask making. Larger feature sizes on the mask reduces the need for improved mask-patterning resolution and increases the minimum size at which defects print, making mask inspection easier. No improvement is seen in the minimum height at which phase defects will print, but larger lens reduction will lead to an increase in the lateral dimensions at which phase defects will print, easing mask blank defect inspection requirements. A decrease in the chief ray angle can obviate, or at least reduce in magnitude, the need for improved mask flatness for meeting overlay requirements

From the perspective of wafer process control, larger lens reduction accompanied by a large mask format is attractive. Mask defect and overlay issues are reduced in difficulty. Reduction of the EUV mask defect problem is of particular concern to wafer processing, given the current lack of an EUV pellicle. From a mask making perspective the technical concerns are

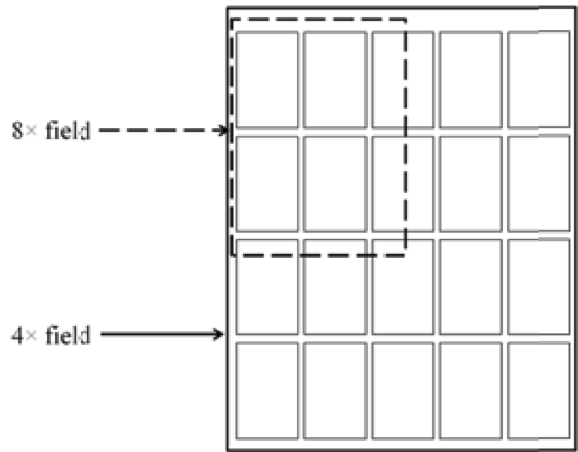

Figure 4. 4x5 array of dies in 4x and 8x reticle fields.

stitching boundary

Figure 5. Feature crossing a stiching boundary.

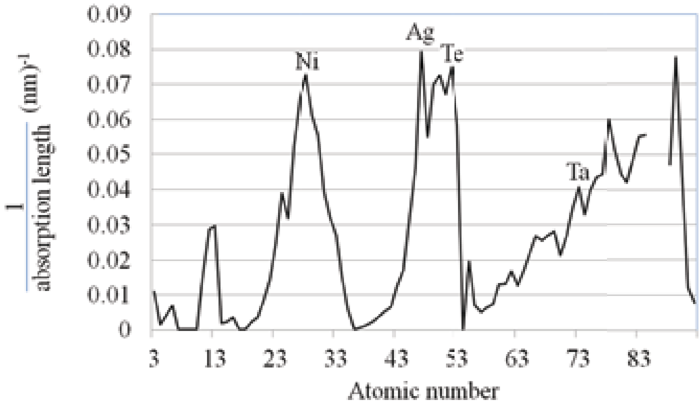

Figure 6. Absorptivity for 13.5 nm wavelength light, across the periodic talbe.[5] There are several elements with substantially reater absorptivity than tantalum.

expected to be tractable, assuming all of the necessary equipment and materials will be commercially available. There will be the usual challenges associated with increased substrate size, such as achieving good linewidth uniformity and registration, but these parameters will be reduced in criticality to some degree by the higher lens reduction. Looking at 230 mm substrate reticle manufacturing as added capacity, the financial considerations are also likely to be acceptable for foundry mask makers.

The major consideration for larger format EUV masks is whether or not the required tools and materials will indeed be produced commercially. The limited market for mask tools requires that utilization of larger format EUV masks is something that all users of high-NA EUV tools will adopt. This is clearly a topic that requires further discussion within the semiconductor industry.

4. Options at 4x lens reduction

Given the challenges associated with higher lens reduction it is worth continuing to see if there are aceptale solutions with 4x lens reduction, particularly when these solutions are compared to the alternatives The problems associated with large chief ray angles result from three-dimensional effects at the mask, and they are most significant with wafer defocus. This suggests that two changes could improve performance with 4x lens reduction:

1. Mask absorbers with greater absorptivity.
2. Better scanner focus control.

Below is a figure showing the absorption coefficients of various elemental solids at a wavelength of 13.5 nm. There are several elements, such as nickel and silver, which have much higher absorptivity than tantalum, a metal often used in the absorbers of EUV masks. This suggests it would be useful to investigate whether metals such as Ni or Ag, or compounds made with these metals, could satisfy other requirements for mask absorbers, such as the ability to be plasma-etched and durability during cleans.

If we improve focus control, the situation can also be improved. For example, if we consider the pattern placement errors of Fig. 1 but improved focus control to 60 nm range, the placement errors can be reduced considerably, as show in Fig. 6. The challenges associated with improving scanner focus control and improving wafer flatness after chemical-mechanical polishing might be met more easily than attempting snitching or introducing a new format for EUV mask substrates.

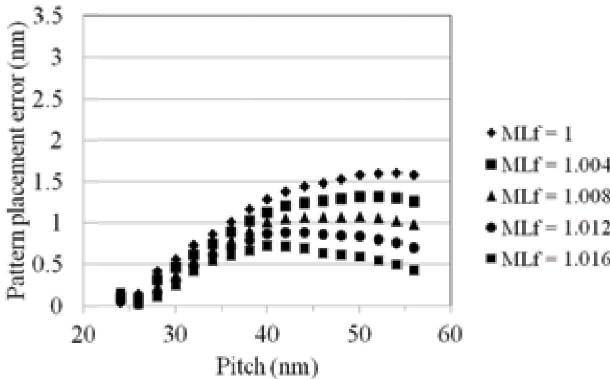

Figure 7. Pattern placement errors for the same conditions as the date in Fig. 1, except for 60 nm focus ange instead of 100 nm.

5. Summary

The proposal to introduce 1/2-field or 1/4-field imaging with larger lens reduction will reduce throughput substantially, which will likely lead to unacceptable cost-of-ownership for high-NA EUV lithography. A lens reduction of 6x~ along with 230 mm masks can simultaneously provide relief from the problems associated with larger chief ray angles at the mask while avoiding the throughput limitations of a smaller field, assuming that a suitable lens can be designed and built. However, this would require a new generation of tools for mask making. Evident opportunities for extending 4x~ lens reduction should be pursued.

6. References

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Editorial

(continued from page 2)

of 60 will grow to 150, with 60 engineers from the member companies, to continue to work on tool and process guidelines, and compliance standards.

The panelists, Kirk Hasserjian, Corporate Vice President, Applied Materials; Brian Trafas, Chief Marketing Officer, KLA-Tencor; Mark Fissel, Vice President of 450 mm Program, Lam Research Corporation; and John Lin, Director of 450mm Project, TSMC, made the following points:

Kirk Hasserjian: The lesson from 300 mm is that building the IC manufacturing ecosystem piecemeal is very costly. Various elements of the 450 mm ecosystem have to be ready simultaneously.

Brian Trafas: To succeed in 450 mm, collaboration is a must even between competitors. Productivity requirements of patterning tools for 450 mm HVM call for tool technology innovation. R&D tools are needed 5 to 7 years before HVM.

Mark Fissel: The big challenge is to continue to invest in 300 mm technology for the next 3 nodes and at the same time to invest in 450 mm tools. 450 mm HVM will require a new generation of wafer handling, saturated with automation.

John Lin: The benefits of design shrink are diminishing. The two key motivators for 450 mm are: the expectation that it will restore the value of the IC manufacturing, and that it is going to be "greener" than 300 nm.

The unifying message from the conference is that the industry is continuing its dual focus on new technology development and introduction, and HVM cost control. The next big goal is to find cost effective way to proliferate iArF DP imaging, followed by the introduction of 450 mm tools. Along the way, 3D IC designs supported by TSV will be key facilitators of device integration.

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Industry Briefs

New Intel CEO Krzanich Takes Reins of Core Product Groups, Management Shakeup, New Devices Division Launched

By **Neil McAllister,** San Francisco, May 21, 2013

Newly minted Intel CEO Brian Krzanich has hit the ground running with a sweeping reorganization to see the launch of a new mobile devices division. “As your CEO I am committed to making quick, informed decisions,” Krzanich said in an email. “I am committed to being bolder, moving faster, and accepting that this means changes will be made knowing that we will listen, learn and then make adjustments in order to keep pace with a rapidly changing industry.”

Ring of Fire Poses Risk to Semiconductor Manufacturing

By **Adrienne Downey,** May 9, 2013

The trend over the past several years has been one of consolidation of hundreds of semiconductor fabs, spread all over the world into several main manufacturing centers in the Asia/Pacific region, the United States, and Europe. Unfortunately for the industry, many of these fabs are located in areas prone to earthquakes. Some locations are also at an added risk of damage from tsunamis generated by earthquakes. The “Ring of Fire”, an area of high seismic activity that extends from southeast of Australia north along the Pacific coast of Asia, crosses south of Alaska, and then continues south along the Pacific coast the Americas, is involved in 90% of the world’s earthquakes. Another 5-6% of the world’s earthquakes occur along the Alpide Belt, which starts along the west coast of Indonesia, continues across the Himalayas, through the Mediterranean, and out into the Atlantic.

The northeast coast of Japan is a prime example; in March 2011, the region suffered a massive 9.0 magnitude earthquake and tsunami that killed 15,883 people, injured over 6,000, and left almost 2,700 still missing. The disaster also caused seven meltdowns at the Fukushima Daiichi nuclear power plant. The plant is still running on makeshift equipment and recently suffered a power outage that left fuel storage pools without cooling water. Almost 130,000 buildings were completely leveled, and over a million others sustained some sort of damage. The amount of devastation was astounding, but the Japanese have done an amazing job of clearing away debris and recovering in the two years since.

Current and Future Defectivity Issues for Equipment Components and Materials

By **Vibhu Jindal,** SEMATECH, May 1, 2013

Changes in the semiconductor equipment and material ecosystem, new materials and process integration for sub-20nm node manufacturing, next generation lithography requirements, and progression to the 450mm wafer size require stringent performance specifications be met in a timely manner. The ecosystem is currently facing huge investment gaps where R&D costs are exponentially increasing due to the costly infrastructure necessary to deliver the solutions. This puts tremendous pressure on the component-level supply chain due to continuously changing technology requirements and slow adoption cycles which in turn result in sluggish recovery of high non-recurrent engineering costs.

Industry requirements for some processes, such as EUV lithography, require zero defects above 50nm in size, since these are considered killer defects, and only a few defects can be tolerated between 20nm and 50nm. The defect requirements for other applications are less stringent, though the trends are driving towards less than 10 particles at continuously smaller sizes. The reduction of particles at such small sizes is producing extreme challenges for original equipment manufacturers (OEMs) as they must tightly control the performance of every component within the equipment, in addition to reducing process defects. The component suppliers face additional challenges as they not only have to meet the stringent performance specifications but also must improve performance based on continuously changing process latitudes and chemistries of end users.

One of the biggest challenges with such small defects is inspection and metrology. State-of-the-art inspection tools can find defects down to 25nm on wafers and masks. Inspection tools capable of detecting smaller sizes are not available. Inspection and failure analysis tools that are capable of detecting defect sources below 50nm are enormously costly, which causes a large infrastructure gap for suppliers working in component and material development. Lacking that infrastructure, it is very difficult for many OEMs and subsystem, component and material suppliers to reduce defect sources and improve defect performance.

Additionally, as defect reduction requirements go down to such small sizes, interdisciplinary knowledge is required to understand the defect generation process and later devise removal or mitigation techniques. Therefore, research and learning at such small defect sizes can take longer which increases development time of components and materials. This delay, in turn, affects yield ramps.

Join the premier professional organization for mask makers and mask users!

About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

Individual Membership Benefits include:

- Subscription to BACUS News (monthly)
- Complimentary Subscription *Semiconductor International* magazine
- Eligibility to hold office on BACUS Steering Committee

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Corporate Membership Benefits include:

- Three Voting Members in the SPIE General Membership
- Subscription to BACUS News (monthly)
- One online SPIE Journal Subscription
- Listed as a Corporate Member in the BACUS Monthly Newsletter

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Calendar

2013

SPIE Photomask Technology

10-12 September 2013
Monterey Marriott and
Monterey Conference Center
Monterey, California, USA
www.spie.org/pm

Submit late abstracts directly to Pat Wight, patw@spie.org, for consideration by conference chairs.

2014

SPIE Advanced Lithography

23-27 February 2014
San Jose Convention Center
and San Jose Marriott
San Jose, California, USA
www.spie.org/al

SPIE is the international society for optics and photonics, a not-for-profit organization founded in 1955 to advance light-based technologies. The Society serves nearly 225,000 constituents from approximately 150 countries, offering conferences, continuing education, books, journals, and a digital library in support of interdisciplinary information exchange, professional growth, and patent precedent. SPIE provided over $3.2 million in support of education and outreach programs in 2012.

SPIE

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You are invited to submit events of interest for this calendar. Please send to lindad@spie.org; alternatively, email or fax to SPIE.