PHOTOMASK

BACUS—The international technical group of SPIE dedicated to the advancement of photomask technology.

BACUS N • E • W • S

July 2011
Volume 27, Issue 7

Invited Paper 7985-4

NGL Masks: Development Status and Issue

Naoya Hayashi, Electronic Device Operations, Dai Nippon Printing Co., Ltd., 2-2-1, Fukuoka, Fujimino-shi, Saitama, 356-8507, Japan; **Tsukasa Abe, Yuichi Inazuki, Tadahiko Takikawa, and Hiroshi Mohri,** Electronic Device Lab, Electronic Device Operations, Dai Nippon Printing Co., Ltd., 2-2-1, Fukuoka, Fujimino-shi, Saitama, 356-8507, Japan; **Takeya Shimomura,** Electronic Device Labs, DNP Corporation USA, 3235 Kifer Road, Suite 100, Santa Clara, CA 95051

ABSTRACT

Semiconductor lithography candidates toward 2xnm node and beyond include wide variety of options, such as extension of 193i, EUVL, NIL, and ML2. Most of those candidates, except ML2, need critical mask feature to realize effective high volume manufacturing. In this presentation, EUVL mask technology update and future issues will be presented.

1. Introduction

There are several lithography candidates for 22/20 nm technology node, as Next Generation Lithography (NGL). Each candidate has some complexity and risk in mask fabrication and lithography process as shown in Table-1. Optical extension of current 193 immersion lithography needs multiple patterning with very complex mask pattern features. Extreme Ultra-violet Lithography (EUVL) is a candidate of NGL with very shorter wavelength of 13.5nm light source and single patterning step, with less complex pattern features. NIL templates have 1X patterns and are requiredmanufacturing process with higher resolution compared to that of the 4X photomasks for optical extension and EUVL. Mask Less Lithography (ML2) does not need ordinary masks, but has very slow throughput for manufacturing.

Continues on page 3.

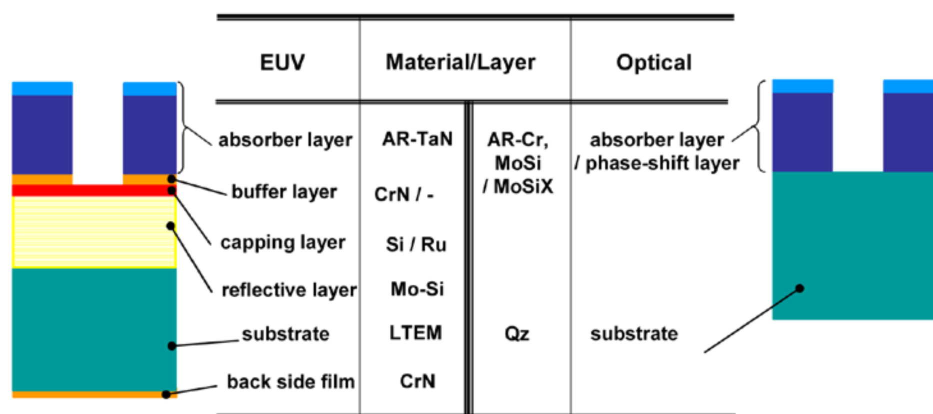

Figure 1. Comparison of mask substrate structures.

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EDITORIAL

Industry Veterans Weigh in on EUV

Bryan Kasprowicz, Photronics, Inc.

Earlier this year, we held annual BACUS panel discussion at the SPIE Advanced Lithography Symposium. The theme for this discussion was "How to afford the infrastructure to support EUV and can masks be made at an affordable price?" We had several industry veterans share their thoughts.

Harry Levinson of GLOBALFOUNDRIES justified the EUV investment by comparing wafer cost to that for optical lithography, at throughputs of 125 and 200 WPH, respectively, highlighting the importance of mask cost amortized as wafer cost per chip, decreasing with higher wafer volume. Sean Doyle of Intel Capital and Andy Wall of Hoya discussed EUV investment strategy. Mr. Doyle focused on the mask market paradigms, how the key elements of productivity are related to the technology, customers and suppliers. He then offered a response, how to advance EUV through consortia and collaboration routes but also highlighted an opportunity for "mutualization" where there may be multi-party agreements or direct equity investments to foster market pull through demand alignment. Mr. Wall compared the current EUV blanks business environment to that of optical blanks and showed the significant investment (a 6:1 ratio over return) is required to support the current limited volume. He then suggested a simple outlay recovery model should the investments be made. Accordingly, the blanks company makes the investment required to deliver the blanks and recovers these investments through blank sales.

Brian Haas of KLA-Tencor presented their reticle inspection roadmap strategy down to the 11nm HP/8nm Logic nodes leveraging existing models and hinting at the development of an actinic platform. He went on to propose that broader EUV adoption will be based on the scanner throughput, assuming of course the mask manufacturing infrastructure is available. He suggested that an 80 WPH minimum is required to ensure affordability with double of that number necessary to allow full merchant mask manufacturer participation.

Naoya Hayashi of Dai Nippon Printing and Chris Progler of Photronics were of like mind that the EUV Mask Infrastructure will be expensive with limited opportunity to realize any returns within a reasonable period of time without commitments from the captive mask facilities. Hayashi-san suggested that joint ventures between the captives and the merchants as well as between the merchants may be necessary to aggregate enough mask volume to ease the burden of the capital investment. While Mr. Progler noted that due to the high costs and redundancy for business continuity, a merchant solution would benefit the industry in terms of competition, cost sharing and development. However, they concluded that the end user must realize these benefits and be willing to accept the costs of the technology, perhaps a new paradigm for the mask industry.

Lastly, John Warlaumont of Sematech highlighted some of the commercialization aspects of the EUV mask infrastructure (EMI). Given that there are a few IDM's that currently have EUV on their roadmap, the amount of investment required by them is significantly higher. This poses an infrastructure funding problem, especially for masks. In order to find a solution, Sematech launched the EMI and proposed funding models that are being well received. Mr. Warlaumont concluded that still, not everyone will be amenable to these models due to the technology innovation and cost.

Since this Advanced Lithography panel discussion, several more EUV systems have been installed, with more coming, and advanced learning is in the early stages. This demonstrates the seriousness of the interest in implementing this technology across all areas – memory and logic, foundry and IDM. Now the questions are, would there be enough IC demand for these advanced nodes requiring EUV, and when?

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BACUS News is published monthly by SPIE for BACUS, the international technical group of SPIE dedicated to the advancement of photomask technology.

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Tel: +1 360 676 3290 or +1 888 504 8171
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Table 1. Complexity and risk of NGLs.

		Optical Extension	EUV	Nanoimprint	Maskless Lithography
Patterning & Mask Production	Mask materials	Optimization and Standardization	Very complex substrate stacks	Standard Qz substrate	No mask used
	Data Prep	Very complex data with SMO/ILT/DPL	Minimum data prep for flare correction	No OPC needed	Compatibility with Optical litho
	Pattern Generation	Massive shot counts/writing time	Flat data exposure needed	1x resolution	1x resolution and Throughput
	Processes	CD and defect control	Damage free process/Cleaning	Defect control	Compatibility with Optical litho
	Inspection & Metrology	Very complex feature and spec.	Actinic inspection & metrology	Inspection and repair	Resolution & Data base inspection
Lithography	Throughput	Multiple exposure	Source, resist, mask life	Step & repeat time	Massive parallel beams needed
	Mask cost	Multiple complex masks needed	High substrate and QA cost	Replication usable	No mask used
	Readiness	Ready now	Pilot in 2011?	Tool/Feasibility needed	Tool availability

EUVL has been recognized as a preferred candidate for NGL with single exposure, relatively simple mask pattern feature, and 4X mask magnification as current optical lithography. On the other hands, EUV mask substrate has quite complex multi layer stacked feature as shown in Figure-1, and will be required very critical defect and flatness control. We have been evaluating both optical and electron beam (EB) inspection systems for EUVL mask[1,2]. In this paper, mask development status for EUVL are updated in mask qualities compared with ITRS requirements[3], and also in mask cleaning and defect inspection technologies.

2. Experiment

Blank substrates of EUVL mask for evaluation are provided by HOYA with Si- and Ru-Capping structures on the mirror layers with TaN based absorber layer on the top. Mask fabrication was done with 50KeV VSB mask writer, JBX-3040 and EBM-7000 using CAR and Non-CAR processes. For measurement tools, we used "LWM9000" (Advantest) CD-SEM, "LMS IPRO" (KLA-Tencor) image placement measurement tool.

DUV optical mask inspection system "NPI-6000EUValpha" (NuFlare), and Mask EBI system "eXploreTM 5200" of Hermes Microvision, Inc., were used as EUV mask pattern defect inspection tool.

3. Results and Discussion

3-1. Mask pattern qualities

Figure-2 shows the absorber pattern resolution of EUV mask written by EBM-7000. We confirmed the resolution of 40nm, 70nm, 60nm, and 50nm on isolated space, isolated line, lines & spaces, and dense hole array, respectively. Those results satisfied ITRS requirement of 78nm at 2013 [3].

The results of absorber pattern CD (Critical Dimension) uniformity across the EUV mask is shown in Figure-3. It shows 3.6nm and 3.5nm in 3-sigma on isolated space and space of lines & space patterns respectively. Those results were close to ITRS requirement of 3.0nm at 2013.

The line width roughness of EUV mask using chemical amplitude resist (CAR) and non-CAR on 128nm line and space design feature and 88nm one written by EBM-7000 system is shown in Figure-4. With non-CAR, line width roughness of both 128nm and 88nm were about 3nm and satisfied the ITRS requirements. On the other hand, general CAR needs further improvement for 88nm, which equivalent to 22nm HP node.

3-2. EUV mask cleaning

Figure-5 shows EUV specific mask cleaning issues. There will be some damage in the capping layer, which consists of Ru or Si, during mask cleaning cycle in the FAB to remove the particle and contamination. Due to no-pellicle applied on EUV mask, more frequently cleaning will be needed.

The results of reflectivity change after mask cleaning by general SPM and SC1 cleaning method on Ru capping structure is shown in Figure-6. Initial several cleaning cycle may remove Ru-oxide on the surface and change the reflectivity uniformity signature. Additional cleaning will not affect on further reflectivity change because of sufficient durability of Ru capping layer.

On the other hand, Figure-7 shows the results of same on Si capping structure. General cleaning method may cause continuous damage, which thinning the Si capping layer, along with the cleaning.

We need appropriate cleaning method which may not cause damage on any capping layer and also absorber layer.

3-2. Defect inspection methods and evaluation results

Figure-8 shows the printability evaluation results and defect type on EUVL mask. We found that some defect on EUVL mask could not be seen with current mask inspection tool, but be printed on wafer. So called "Phase defect" will exist in multi layer, and will be printed on wafer with even very small height, less than 2nm, on the surface. Inspection tool vendors have been trying to capture the defect with optical source tool and EB tool[2,4,5,6]. However,

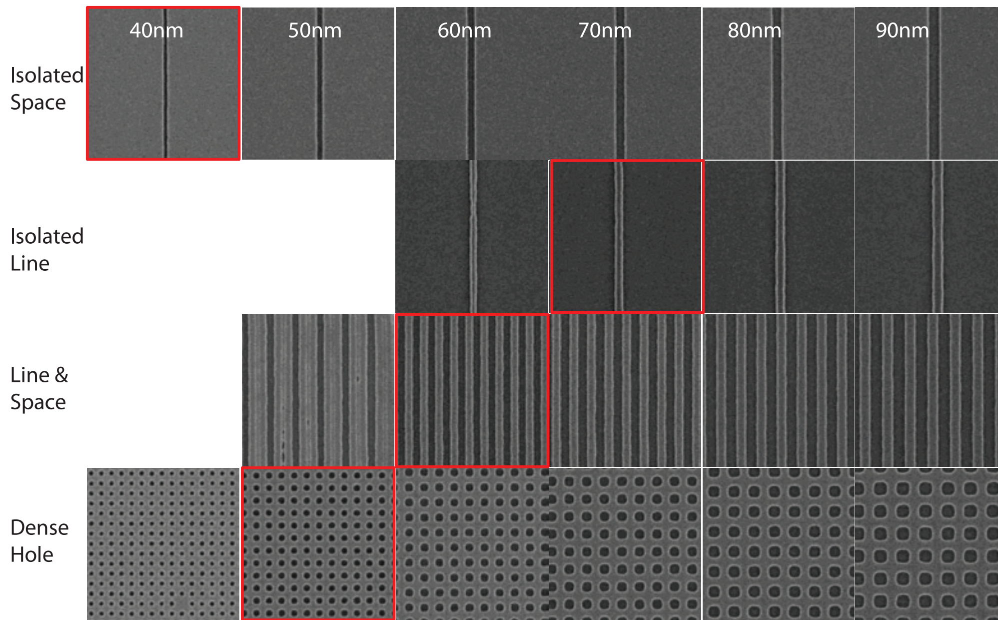

Figure 2. Patterning performance of EUVL mask.

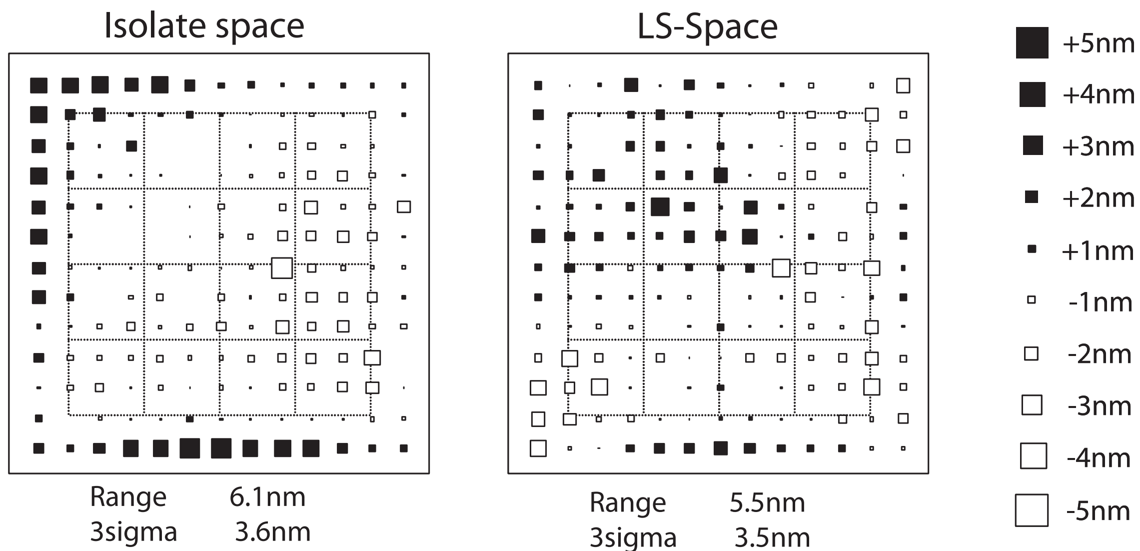

Figure 3. CD uniformity of absorber pattern.

we think that we need actinic, with EUV light source, blank defect inspection tool to capture the "Phase defect" at the stage of EUV mask blank manufacturing.

The general inspection methods for optical mask and EUV mask are shown in Figure-9. Current existent mask inspection system with DUV light source was designed using both transmitted light and reflected light to capture various types of defects on the optical mask. On the other hand, EUV mask substrate does not have the capability to transmit the DUV light, which limited the capability and sensitivity of inspection system for EUV mask. The inspection system with electron beam (EB) source has been considering to be applied for EUV mask by using reflected secondary electron to capture the defect with better resolution. However, the throughput of EB inspection system is very slow due to very small pixel size for inspection.

Figure-10 shows the inspection results of designed defect EUV mask by DUV optical source inspection tool, NPI-6000EUValpha with 199nm wavelength light source and polarized illumination. We

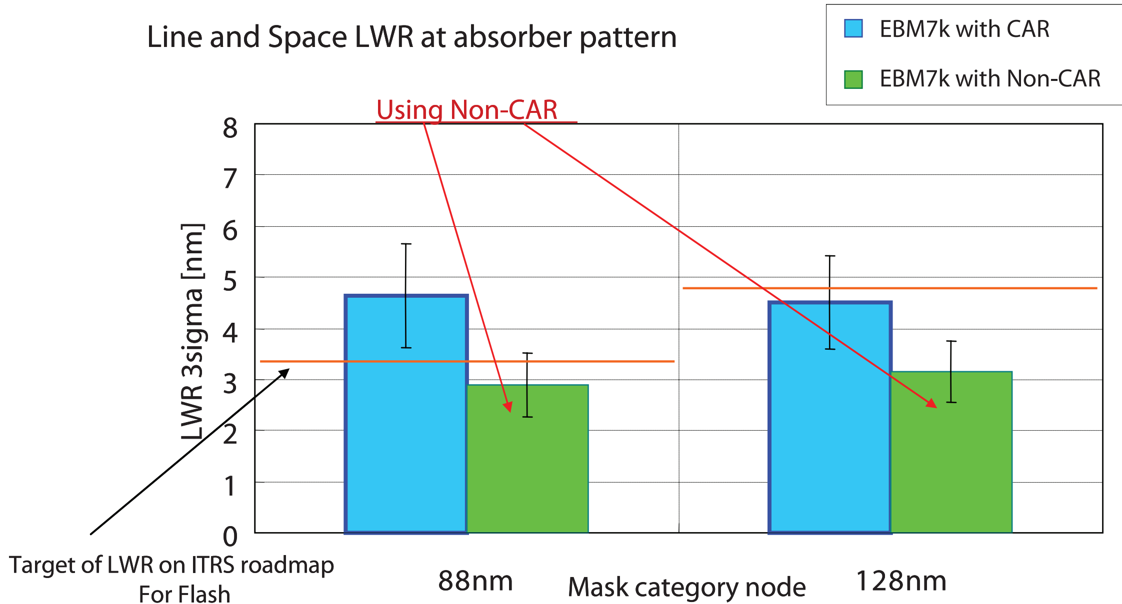

Figure 4. LWR evaluation results on EUVL mask.

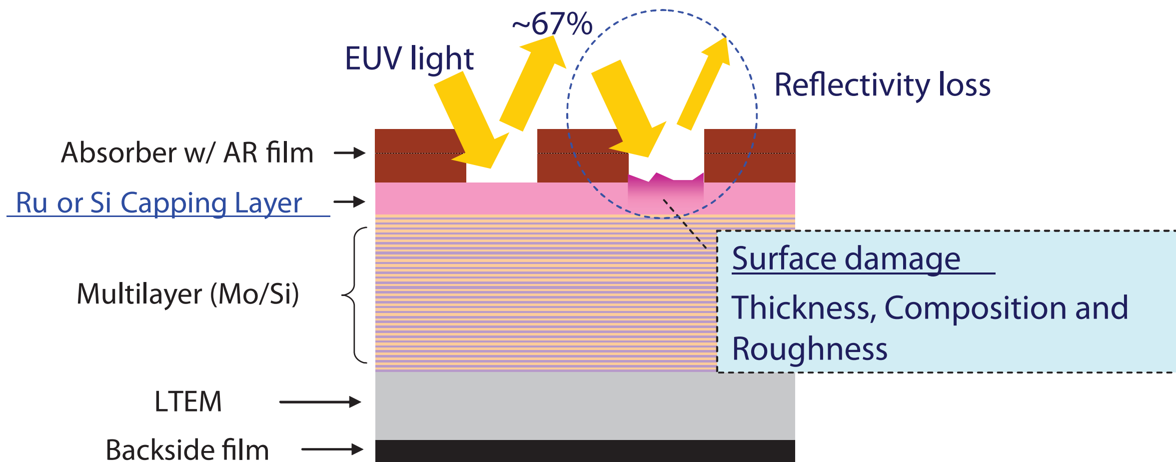

Figure 5. EUV mask cleaning damage.

found that low reflective absorber layer and polarized illumination will enhance the contrast of the image, and improve the defect inspection sensitivity. The results showed that the sensitivity satisfied the requirement for 27nm HP features [7].

The evaluation result of EB inspection tool, eXplore 5200, on the designed defect EUV mask with 22nm lines and spaces is shown in Figure 11. The result showed the capability of capturing 25nm defect size, which reaches ITRS 32nm HP requirement.

Both inspection methods still need further improvement to reach to the 22nm HP requirement with enough stability and reasonable inspection cycle time.

4. Summary

We have been developing EUVL mask using and modifying current photomask manufacturing technology. The qualities of EUVL mask have been achieving the requirement of 32nm HP generation at 2013.

We still need further study and development for EUVL mask cleaning, and defect inspection method to guaranty the printability and yield on wafer.

5. Acknowledgment

The authors would like to thank Selete for optical defect inspection tool evaluation and Hermes Microvision, Inc. for EB tool evaluation.

We also express our thanks to DNP members involved in this work

6. REFFERENCE

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Ru cap EUV reflectivity damage

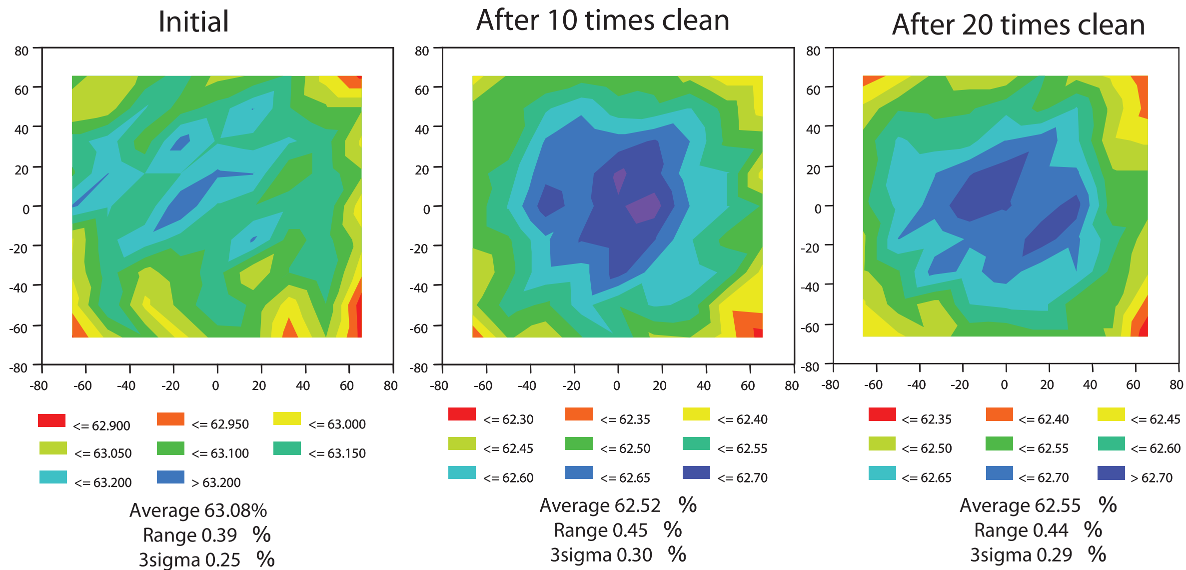

Figure 6. Cleaning damage evaluation (Ru Capping).

Si cap EUV reflectivity damage

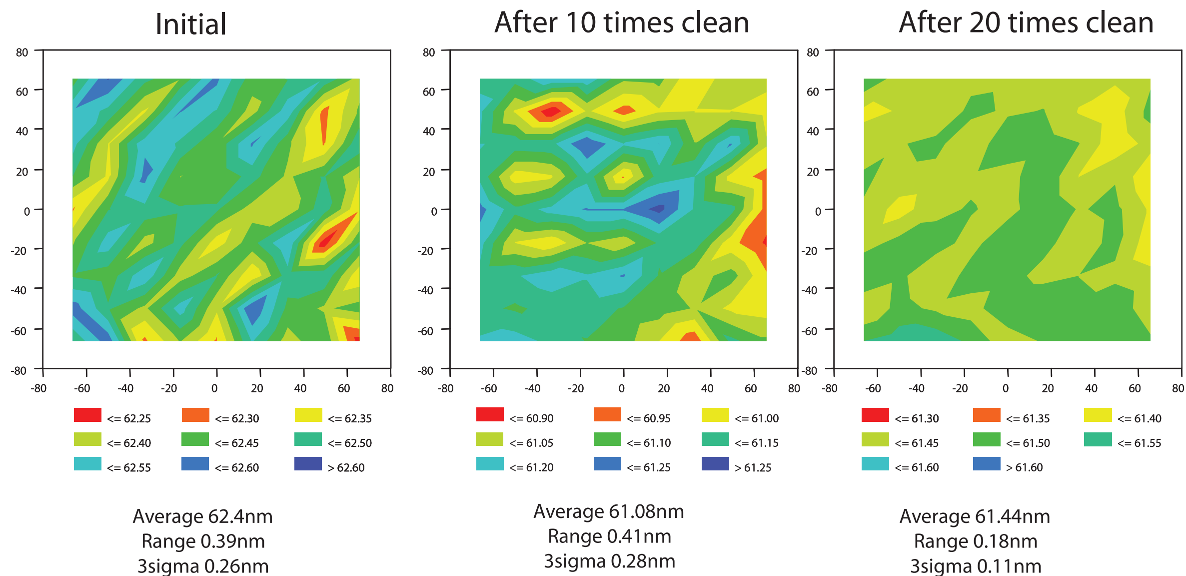

Figure 7. Cleaning damage evaluation (Si Capping).

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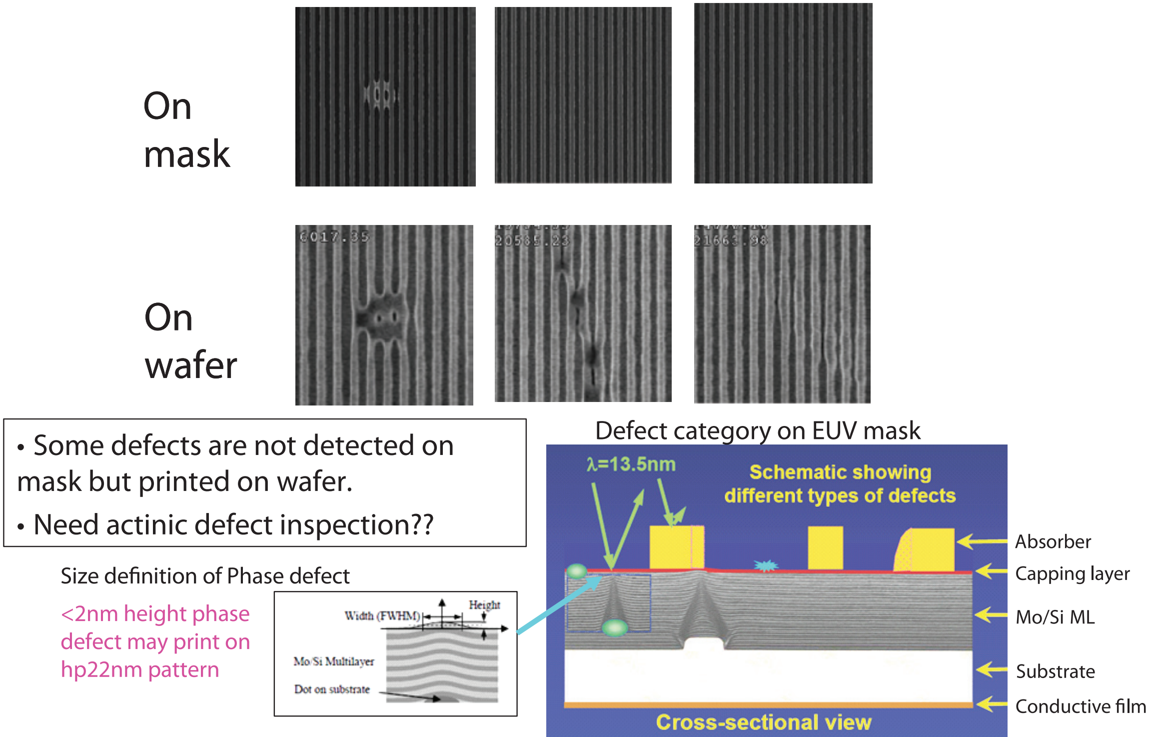


Figure 8. Defect printability.

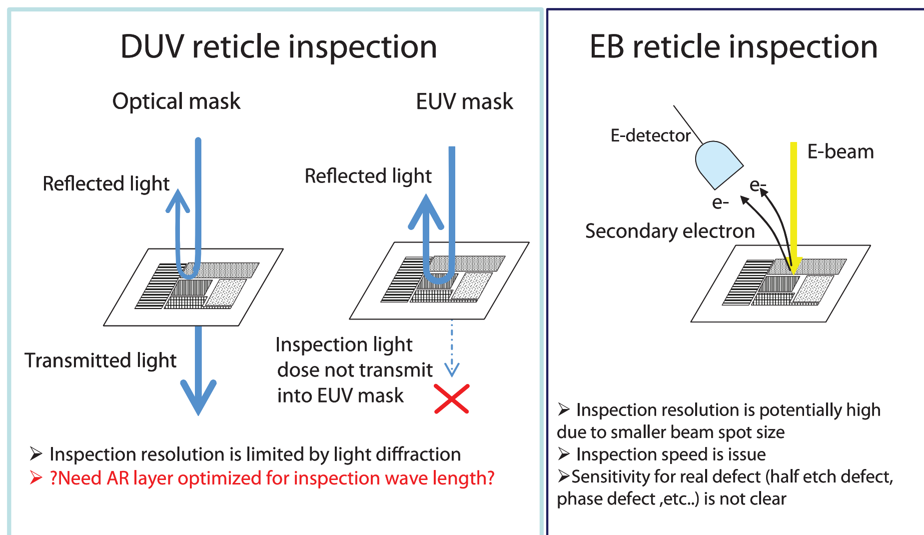
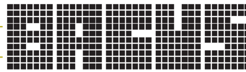


Figure 9. Mask inspection methods.



Inspection sensitivities @hp108nm

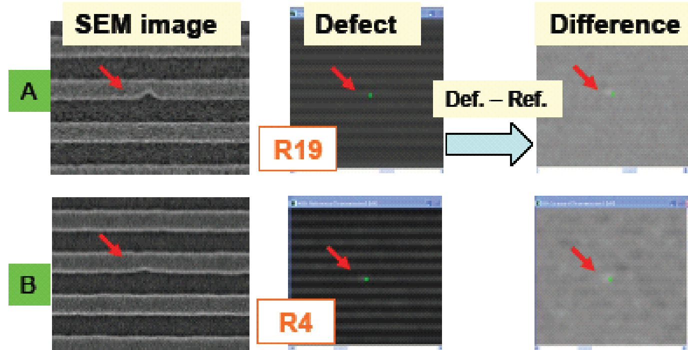
D-D, 5 runs

Defect type	Mask	Illumination	Defect size [nm] (Square root of area) 80	75	70	65	60	55	50	45	40	35	30	25	20	15	10	5
Edge extension	R19	C-pol.																
		P-pol.																
	R4	C-pol.																
		P-pol.																
Edge intrusion	R19	C-pol.																
		P-pol.																
	R4	C-pol.																
		P-pol.																

A

B

10% CD error (Calculated)



・Image contrast was poor but defect signal appears strongly.

・Small edge intrusion defect was captured as clear defect.

Figure 10. Optical tool inspection result on 27nm L&S.

Type / No.	0 Size	1 Size	2 Size	3 Size	4 Size	5 Size	6 Size	7 Size	8 Size	9 Size
0										
1									2	
2									4	
3									6	
4							21		7	
5			13				22		11	
6			31		15		33		11	
7			34		22		39		15	4
8			44		26		45		16	6
9			67	26	33		47	20	17	7
10			71	28	41	17	60	24	19	10
11			72	38	44	19	63	34	22	12
12			76	43	48	20	70	39	26	14
13			78	48	53	25	78	45	26	16
14	70	21	81	56	62	32	90	50	30	19
15	73	26	82	59	63	33	96	62	31	19
16	76	30	84	67	70	33	100	88	34	23
17	77	59	84	67	80	41	105	100	37	24
18	80	64	87	70	84	61	107	103	37	28
19	86	69	90	72	88	68	112	110	93	31
20	87	73	93	76	91	73	116	116	93	33
21	91	76	93	76	91	74	117	121	93	36
22	98	81	93	81	94	78	123	124	93	38
23	96	81	97	83	95	84	126	128	93	42
24	99	85	98	87	100	87	126	131	93	42
25	99	86	100	88	102	88	128	131	93	44
26	99	88	101	93	102	91	131	134	93	93
27	102	91	101	91	99	91	133	137	93	93
28	101	94	102	96	99	95	133	139	93	93
29	104	96	104	96	106	98	135	142	93	93
30	104	100	102	100	105	98	139	144	93	93

No (visible) defect
Not clealy resolved
Break or Bridge

25nm defect size
(ITRS 32nm HP)

Not detected
Detected by EBI

hp88nm on mask

20nm pixel size inspection

Figure 11. EB tool inspection result on 22nm L&S.

Industry Briefs

CEA-Leti Annual Review: Update on maskless litho work

By **Hughes Metras,** U.S. Development, Leti
June 28, 2011

Multi e-beam lithography, a maskless technology, is a recognized alternative to EUV on the International Technology Roadmap for Semiconductors for the 22nm node and below. But the technology must first overcome throughput, data handling and other challenges, Leti lithography program manager Serge Tedesco told Leti's 13th Annual Review in Grenoble, France. Leti, MAPPER Technology, and others partners launched the Imagine program in 2009 to assess the capabilities of multi e-beam technology against the needs of end users on a 300mm pilot line. The Imagine program's members include software, tool, materials suppliers, and chipmakers: Mentor Graphics, Aselta, Synopsis, SOKUDO, Nissan Chemical, Tokyo Electron, JSR, Dow EM, and MAPPER.

Tedesco said MAPPER will have a system with 13,000 parallel e-beams capable of producing 10 wafers/hour in 2013-14, to establish multi-beam technology infrastructure and demonstrate tool capability in terms of resolution, throughput, overlay, and stitching. By eliminating the need for photomasks, multi e-beam lithography would cut millions of dollars from the cost of manufacturing chips, and would open the doors for more designs and innovation.

Lithography cost-of-ownership considerations

By **David K. Lam,** Multibeam Corporation
June 27, 2011

The semiconductor industry is facing major cost challenges in patterning advanced ICs in high volumes. A cost analysis by Burn Lin of TSMC, in 2009, projected the cost of lithography at the 22nm node, for optical, extreme ultraviolet (EUV) and multiple electron beams (MEB), at a throughput of 100 wafers/hour and excluding costs of EUV masks, infrastructure and power usage, etc., to be comparable.

Reality check #1. The EUV throughput of ASML's most recent EUV system, being installed at imec in May 2011, is 5-6wph, still considered a substantial improvement from previous versions, thanks to higher EUV source power, but almost 20X slower than the 100wph used in Lin's calculation. Lin also assumed that an EUV tool would cost 25% more than an 193i tool. Given 193i's current price tag of $50 million, this formula puts EUV tool price at $62.5 million. However, G. Dan Hutcheson of VLSI Research projected in November 2010 EUV tool cost to be $125 million. This is 2X Lin's 2009 projection and 2.5X today's cost of a 193i tool. Nevertheless, EUV is making progress. A 5X boost in EUV source power, for example, could potentially increase throughput to 25-30wph for the $125 million tool price.

Reality check #2. Mask infrastructure for EUV is still in development. SEMATECH in 2007 estimated that the average critical layer mask for EUV would cost $300,000 and pattern 5000 wafers. This adds $60 per layer. There remain unresolved issues in EUV infrastructure including mask blanks, mask making, defect inspection, and defect compensation — a requirement unique to EUV. On the other hand, complementary lithography, uses two lithography technologies to complement each other for better patterning at lower cost. Multibeam Corporation is developing CEBL for patterning critical layers for advanced logic and system-on-a-chip (SoC). CEBL focuses on cutting poly and metal lines as well as contact and via holes, while optically patterning all other layers. One version of CEBL is optimized for cutting applications and requires no masks.

Electron-beam lithography (EBL) tool price is tied to throughput. The desired 100wph for about €50 million (roughly $71.4 million) puts pressure on EBL developers to increase throughput and reduce tool cost. EBL is too slow for high-volume manufacturing if used to pattern all layers. CEBL may play a limited yet crucial role: patterning only critical layers, with low feature density of ~5%. The scalable architecture delivers high throughout to complement and extend optical lithography. In addition, support infrastructure for CEBL is available today, thus eliminating major investments in new infrastructure.

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