PHOTOMASK

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Photronics Award for Best Student Oral

Effects of the illumination NA on EUV mask inspection with coherent diffraction imaging

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ABSTRACT

RESCAN is a coherent diffraction imaging based APMI microscope prototype. A complex image of the EUV reticle is reconstructed from diffraction patterns collected on a CCD detector. With the next upgrade of the tool, the resolution will be enhanced from the current 34 nm down to 20 nm on mask. Also the illumination NA value will change from the current range of 0.002 to 0.02 to a value of 0.035. Here, we study how a change of the illumination NA affects the EUV mask inspection in simulation. We observe a better image quality, lower object error and higher defect sensitivity with increasing illumination NA.

1. Introduction

RESCAN (reflective-mode EUV mask scanning lensless microscope) is an APMI microscope prototype developed at the Paul Scherrer Institut. It is based on a coherent diffraction imaging¹ technique called ptychography,^{2,3} where the reticle is scanned with spatially-confined, coherent EUV illumination in overlapping positions. On a CCD detector in the far-field, the diffraction patterns for each scan position are collected. The (complex) image of the reticle is reconstructed from the intensity data by using a phase-retrieval algorithm.

The current RESCAN tool (the optical layout is depicted in fig. 1 (a)), has a resolution of 34 nm on mask. The EUV beam is focused onto the sample with an angle of incidence of 6° and the illumination numerical aperture (NA) value ranges from 0.002 to 0.02.4 An upgrade of the tool is under construction: an image of the new design is shown in fig. 1 (b). The two mirror system will be replaced by a Fourier synthesis illuminator, which will enhance the resolution on mask down to 20 nm.⁵ A visible light microscope will facilitate the navigation on the sample. Furthermore, the illumination NA changes to a larger value of 0.035.

In this paper, we study in simulation how a change in the illumination NA influences the EUV mask inspection with coherent diffraction imaging.

2. Illumination NA Simulation

In this study, we are performing defect inspection on simulated data sets with illumination NA values ranging from NAillum = 0:005 to NAillum = 0:050. The lowest NA value corresponds to the typical illumination NA of the current RESCAN setup, the range is chosen to cover the illumination NA for the RESCAN upgrade (NAillum = 0:035). As our current RESCAN tool is limited to a maximum illumination NA of 0.02, we study the influence of the illumination NA on EUV mask inspection in simulation only.

The EUV mask sample is generated from a mask design file with programmed absorber defects, varying

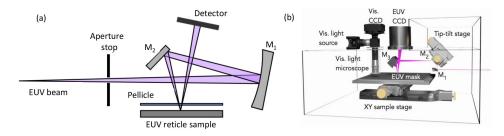


Figure 1. (a) Schematic of the current RESCAN setup. (b) Rendering of the upgraded RESCAN setup, with a Fourier synthesis illuminator.



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EDITORIAL

The European Mask and Lithography **Conference (EMLC) Survives Difficult Times**

Uwe Behringer, UBC Microelectronics, Germany

The European Mask and Lithography Conference (EMLC) has been a fixed part of the VDE-GMM (Verband der Elektrotechnik - Gesellschaft Mikroelektronik, Mikrosystemund Feinwerktechnik) conference program for many years. Considering the role of the semiconductor industry as a key technology for almost all application topics of our life today, this connection is only logical. In the context of the global semiconductor industry, Europe is of paramount importance for this market, not so much in the field of circuit manufacturing, but definitely as a location for leading equipment manufacturers.

First organized in 1984 as the "Mask Technology for Microelectronic Devices" conference, its organizers have been committed to scientific and technical exchange on the latest topics related to the manufacture & application of masks for optical lithography. Since 2004, the conference has been a forum for the discussion of all lithography relevant topics, which was manifested not least in the changed name of the conference - "European Mask and Lithography Conference - EMLC," with its main location in Dresden, Germany.

The format of the conference, which provides ample opportunity for direct exchange between colleagues from applied research and industry, has been regarded as very valuable by the conference participants for many years.

As in the new name of the conference there is the word "European," the members of the EMLC program committee together with VDE decided to organize the conference with changing venues within Europe. Outside of Dresden, the EMLC was organized three times in Grenoble, France with support of CEA/LETI and ST, one time in Eindhoven in The Netherlands supported by ASML, and now is set up for June 2021 in Leuven, Belgium, supported by the renowned IMEC (Interuniversity Microelectronics Center) and ASML.

EMLC 2021, the 36th edition of EMLC, originally planned for June 2020 in Leuven (Belgium), like the majority of face-to-face events this year, had to be postponed by one year. The organizers now hope that the conference can be held face-to-face again in Leuven, 21-23 June 2021. With Leuven, the headquarters of IMEC, as the venue of the conference, the best conditions are offered for an exchange on the latest developments in the semiconductor industry. The time-honored halls of KU Leuven provide the perfect setting.

From the point of view of the program committee, the course for an interesting conference is already set. The vast majority of the authors who had confirmed their participation for 2020 will also be represented in the 2021 program.

First of all, the three Keynote speeches are to be mentioned here: Professor Dr. Luc Van Den Hove, President & CEO of IMEC, Dr. Frank E. Abboud from Intel (Vice President, Technology and Manufacturing Group, General Manager of Intel Mask) and Professor Dr. Jos P.H. Benschop from ASML (Senior Vice President Technology). This is an ideal introduction to the main topics of the conference.

In addition, there will be 12 invited presentations covering current issues in mask making, optical and EUV lithography, process technology, layout data preparation and latest research results in the field of quantum computing. The final technical program will be complemented by regular submissions until the official submission deadline for abstracts on Friday, April 9th, 2021

The format of Tutorials, well-proven at its previous editions, is also planned for 2021. The organizers were able to enlist Dr. Peter De Bisschop of IMEC, Dr. Roger Verberk of TNO and Professor Dr. Takeo Watanabe of the University of Hyogo as Tutors.

A technical - commercial exhibition will be included as well. All interested companies are cordially invited.

Depending on the pandemic situation in Belgium in June 2021, the program committee already started discussing as a fall back version to hold the conference as a virtual event.

In a digital version of the EMLC 2021, the conference will be daily split in two time slots. This would allow live Keynote, Invited and Tutorial presentations with attendance from America, the Asian Hemisphere and Europe. All other presentations (oral and poster) would be pre-recorded and thus made available to registered EMLC 2021 participants.

Further details can be found on the conference website https://www.emlc-conference.com/en

Uwe Behringer for the last 28 years has been head of the EMLC Program Committee and the EMLC Conference Chair. He is a member of the BACUS and Photomask Japan Steering Committees, In 2019, Uwe Behringer of UBC Microelectronics received the BACUS/SPIE Lifetime Achievement Award in recognition of his promotion and support of the phot industry over many decades through his efforts to plan and organize The European Mask and Lithography Conference and his unflagging contribution to the Photomask Technology and Photomask Japan conference.



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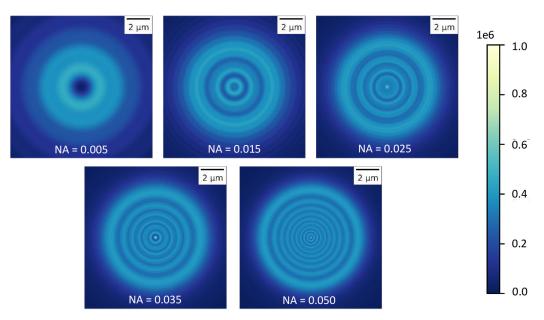


Figure 2. Simulated illumination magnitudes without noise on the object plane. From left to right and top to bottom increasing illumination NA.

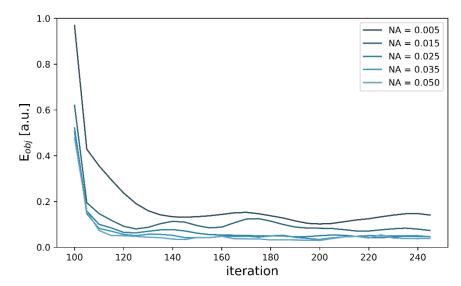


Figure 3. Object error for the illumination NAs.

in size from 200 nm to 20 nm. We assume the sample to be binary, and add a phase shift to the absorber layer, that corresponds to 70 nm TaBN under 6° angle of incidence at a wavelength of 13.5 nm. The complex illumination function (also called probe) is simulated matching the characteristics of the current RESCAN setup (fig. 1 (a)). It is generated as an image of the beam shaping aperture on the reticle, with a wavelength of 13.5 nm (EUV). The illumination NA is determined by the aperture stop diameter and by its distance from the sample. The EUV reticle is moved through focus to maintain a constant probe diameter of 10 μm on object for all data sets. Images of the probe magnitudes are shown in fig. 2.

To generate the diffraction patterns, the probe function is multiplied with the object region, that corresponds to the current scan position. The product corresponds to the exit wave and is propagated to the detector in the far-field, using a Fourier transform and an appropriate

phase term.6 The squared absolute value of the propagated exit wave gives the noise-free diffraction pattern. To get the full ptychographic data set, This procedure is repeated for all scan positions. The average detector count per data set is scaled according to real RESCAN data. We add Poisson noise to each diffraction pattern. The sample is scanned in a circular pattern with a step size of 1 μm to avoid regular grid pathology. 7

3. EUV Reticle Image Reconstruction

We reconstruct a (complex) image of the EUV mask for each illumination function using the difference map algorithm. The algorithm is run for 250 iterations, while updating the probe function from the 100th iteration on. The initial object is generated following a random uniform distribution of values between zero and one, the initial probes are the complex illumination functions as simulated.

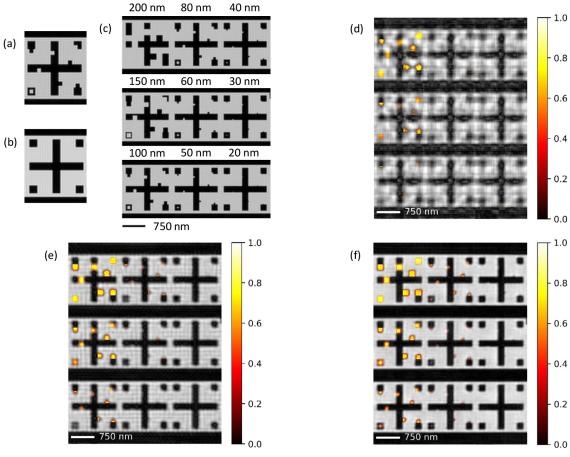


Figure 4. Defect maps for three different illumination NAs. (a) Schematic of a sample area with defects and (b) the respective reference from the database. (c) Layout of the sample design with defect sizes ranging from 200 nm to 20 nm. (d) Shows the defect map overlaid on the reconstructed image magnitude for an illumination NA of 0.005, (e) for an illumination NA of 0.025, and (f) from an illumination NA of 0.050, from a die-to-database comparison.

To compare the reconstructions quantitatively, we introduced the object error⁸

$$E_{obj} = \frac{\sum_{r} \sum_{i,j} ||O_{ij}^{ref}| - |\hat{O}_{ij}||^2}{\sum_{r} \sum_{i,j} 1},$$
 (1)

The absolute value of the reconstructed object Ô is compared at each iteration to a reference object Oref from the sample layout. The error is normalized to the total number of pixels. The object error for all NAs is shown in fig. 3. After the probe update starts, at the 100th iteration, the error is decaying fast to a steady level for all the illumination NAs. Fluctuations around that level, best visible for the lower NA curves, are inherent to the difference map algorithm, that typically reaches a steady state close to the optimal solution.7 To find the optimal image reconstruction, one can average the solutions of the last few iterations, or run for more iterations with another algorithm (for example from the PIE-family⁹) that is known to converge more likely to the global minimum. We observe a larger object error for the two smallest NAs, and a smaller object error for the largest three illumination NAs. The lowest error is observed for the largest NA (NAillum = 0:050). From fig. 3, we observe a trend for a lower object error and hence a more accurate reconstruction of the sample, with larger illumination NA.

4. Defect Detection

The simulated EUV mask contains an area with planned defects ranging in size from 200 nm to 20 nm. A schematic of the region is shown in fig. 4 (c). Each of the nine crosses contains line intrusions and extrusions, one

corner defect and one pin-dot defect with respective size. The critical dimension of the sample is 200 nm. To detect the defects, we perform a die-to-database comparison for each of the reconstructed mask images.⁴ A die with defects, depicted in fig. 4 (a), is compared to the defect free reference shown in 4 (b).

In fig. 4 (d), (e), and (f), the defect maps for three different illumination NA values (NAillum = 0:005, NAillum = 0:025, and NAillum = 0:050) are shown overlaid with the reconstructed EUV mask image magnitudes. From a first look, we observe a better image quality for the larger illumination NA reconstructions. The features are better resolved and the pattern is well visible for the largest illumination NA in fig. 4 (f). Considering all three defect maps, we see that more defects are detected down to smaller defect sizes for a larger illumination NA. It is important to note that this is a simulation study. For real RESCAN data we demonstrated defect detection down to 50 by 50 nm² with an illumination NA of $0.002.^4\,$

To look more closely on the influence of the illumination NA on EUV mask inspection with coherent diffraction imaging, we listed the detected defect signals for different illumination NA and defect size in a table for each defect type. The tables for line intrusions (left) and extrusions (right) are shown in fig. 5. For both line defect types, smaller defects are detected with increasing illumination NA. Please note, that the defect signals in the table are not corrected for false positives.

In fig. 6 the same tables for corner and pin-dot defects are shown. For all defect types, we observe a higher defect sensitivity with larger illumination NA.



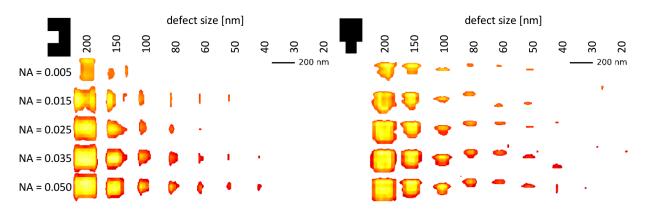


Figure 5. Table containing the detected defect signals for the different illumination NAs with changing defect size. On the left, a table with line intrusion defects is shown, while on the right, a table with line extrusion defects is shown.

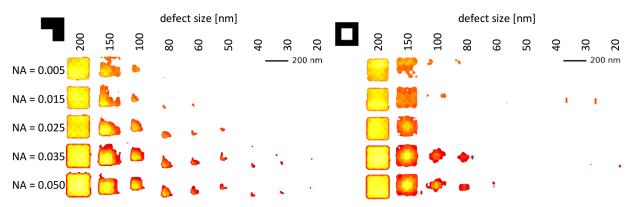


Figure 6. Left: Table showing the corner defect signals for different NAs and changing defect size. On the right, the same table with pin-dot defects is shown.

5. Conclusions and Outlook

In this paper, we studied the effects of the illumination NA on EUV reticle inspection with coherent diffraction imaging. We first simulated ptychographic data sets for several illumination functions with illumination NA values ranging from NAillum = 0:005 to NAillum = 0:050, and reconstructed the (complex) EUV mask image using the difference map algorithm.

We observed that larger illumination NA values yield lower object errors. The reconstructed image quality is better for a larger illumination NA and the pattern is better resolved. We furthermore observe a higher defect sensitivity with larger illumination NA values. More and smaller defects are detected in a die-to-database comparison for the large illumination NA data sets.

We expect that with the RESCAN upgrade to a Fourier synthesis illuminator and an increased illumination NA, we will enhance the resolution to 20 nm on mask and get a higher defect sensitivity.

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Industry Briefs

■ Fortune - Using Pandemic Recovery Funds, Europe Moves to **Build Up its Semiconductor Industry**

By David Meyer

Half the countries in the European Union, including Germany and France, are joining forces to develop semiconductors for use in self-driving cars, data centers, A.I., and supercomputers.

Europe already has a sizable semiconductor industry with particular strengths in areas such as smart cards and sensors, but it's still small compared with those in the U.S., South Korea, and Taiwan: European companies hold just a tenth of the \$530 billion global semiconductor market.

In their joint statement, the EU countries warned the components "determine the characteristics of the products into which they are embedded—including security, privacy, energy performance, and safety—shaping how Europe's green and digital transition will unfold."

"Europe has all it takes to diversify and reduce critical dependencies, while remaining open," said Thierry Breton, the EU's internal market commissioner. "We will therefore need to set ambitious plans, from design of chips to advanced manufacturing progressing towards 2nm nodes, with the aim of differentiating and leading on our most important value chains."

https://fortune.com/2020/12/07/eu-semiconductor-push-using-pandemic-recovery-funds/

■ North Phoenix Land Auctioned Wednesday Will Become **Massive International Semiconductor Factory**

By Jen Fifield, Arizona Republic

Taiwan Semiconductor Manufacturing Co. is buying a large tract of undeveloped state land in north Phoenix to build its multibillion-dollar semiconductor factory. The company's \$89 million bid was the only bid the state received at an auction on Wednesday for 1, 129 acres of undeveloped land off Interstate 17 between Loop 303 and Carefree Highway. The bidding started at \$89 million. The auction made public the exact location for the advanced chip factory, which the company has kept quiet since May, when city and state officials announced it was coming.

TSMC commitment to spend \$12 billion building its factory, which will open by 2024 and employ 1,600 workers, in Phoenix has been lauded as a huge economic win for the city.

https://www.azcentral.com/story/news/local/phoenix/2020/12/09/taiwan-semiconductormanufacturing-pay-89-million-north-phoenix-land/6499660002/

■ The New York Times - Amazon and Apple Are Powering a Shift Away From Intel's Chips

Bv Don Clark

Amazon's cloud computing business and Apple's Macs are increasingly using the companies' homegrown chips. For close to a decade, supporters of the chip technology that powers mobile phones vowed to shake up the market for computers. For the most part, they made little headway.

Now that finally seems to be changing, in a potential power shift over the direction of the computer industry.

The change is being driven by Apple and Amazon who are cutting their dependence on the Intel chip technology that has long controlled most personal computers and larger server systems. Instead, the companies are increasingly leaning on homegrown chips that were designed using technology that Arm, a British company, licenses for smartphones and other consumer products.

Apple fired a salvo last month when it introduced Mac computers that for the first time used its own Arm-based chips. In June, Amazon's cloud computing business started marketing a new computing service based on its own Arm-based chips, telling customers that the service was both faster and cheaper by one-fifth than its Intel-based offerings.

The actions by Apple and Amazon are causing ripple effects across the \$400 billion semiconductor industry. Their moves suggest that key decisions in chips may increasingly shift from silicon suppliers, where the power had long resided, to chip users with the resources to make their own components. For computer users, the moves may result in more technology choices, snappier computing speeds and lower costs.

https://www.nytimes.com/2020/12/01/technology/amazon-apple-chips-intel-arm.html



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Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

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