

# PHOTOMASK

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## Mask Data Processing in the Era of Multibeam Writers

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### Abstract

Mask writers' architectures have evolved through the years in response to ever tightening requirements for better resolution, tighter feature placement, improved CD control, and tolerable write time. The unprecedented extension of optical lithography and the myriad of Resolution Enhancement Techniques have tasked current mask writers with ever increasing shot count and higher dose, and therefore, increasing write time. Once again, we see the need for a transition to a new type of mask writer based on massively parallel architecture. These platforms offer a step function improvement in both dose and the ability to process massive amounts of data. The higher dose and almost unlimited appetite for edge corrections open new windows of opportunity to further push the envelope. These architectures are also naturally capable of producing curvilinear shapes, making the need to approximate a curve with multiple Manhattan shapes unnecessary.

This paper will look into the requirements and considerations for mask processing to take advantage of the new multibeam architectures.

### 1. Introduction

The ability to print features on the wafer that are more than 10x smaller than the size of the imaging wavelength was only made possible by using Resolution Enhancement Techniques (RET)<sup>1</sup>. In RET the pattern data is altered with decorations for Optical Proximity Correction (OPC). RET has been extended to use Phase Shift Mask (PSM) and more recently Computational Lithography or Inverse Lithography (ILT)<sup>2,3</sup>. Keeping up with Moore's law<sup>4</sup> of integrated circuit scaling, this trend is likely to continue for the upcoming 10 and 7nm nodes, resulting in an unprecedented increase in the number of vertices needed to describe a figure. The result is a proportional increase in pattern file size and complexity. Many efforts are placed on data compaction and hierarchy to maintain a manageable mask pattern data file size, including the preservation of polygon descriptors and references to repeated cells. However, the pattern data for each layer of mask making goes through a data processing step post RET tape-out that prepares the pattern file for the mask processing tools (Writing, Inspection, and Metrology, etc.). This step is referred to as Mask Data Preparation (MDP), or Data Fracture. In such a step, pattern file polygons are fractured into primarily Manhattan shapes and in some cases, are sorted and/or organized in a format most suitable for the processing tool. Figure 1 shows a typical ratio of tape out files sized to a fractured file size. In addition, it shows our estimate for the tape out and fractured file sizes for the 14 and the 10nm nodes.

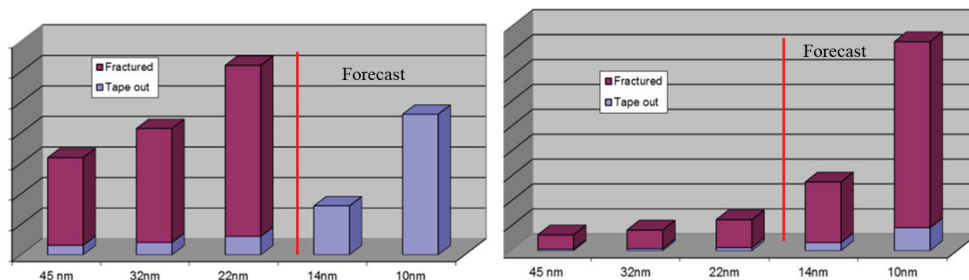


Figure 1. Tape out file size vs. fractured file size per node for the complete mask set.

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# EDITORIAL

## The World Is Not Flat or Square

Paul C. Allen, **Toppa Photomasks, Inc.**

Mainstream semiconductor lithography has primarily concerned itself with the reproduction of two-level Manhattan features into photoresist. Edges are usually oriented in the x or y direction and the ideal transition is as sharp as possible between full resist thickness and no resist. The mask industry and the tools that support it have grown up in this paradigm for so long that these constraints have become second nature to our thought processes. Yes, GDSII supports polygons and OASIS supports polygons and even circles, but OASIS.MASK does not allow polygons or circles. Some vector scan e-beam machines have 45 degree apertures but most angled lines must be composed of stair steps. Curved features must be represented as polygons with many vertices resulting in an explosion of shots when fractured for pattern generation. None of the EDA or simulation tools handle curved edges in any way other than with straight edge approximations. Finally, no mask data formats exist to convey the design intent of the 3D topological features that are produced by gray-scale lithography.

An increasing number of applications are surfacing that could benefit from a more exact approach to pattern description, computation, and generation. Here are a few:

- **ILT** Inverse Lithography Technology naturally produces curved regions. Simulations have demonstrated larger process windows with more exact reproduction of the ILT mask.
- **Silicon devices** There are some specialized silicon processes that require well controlled ramps on the edges of features, currently created by gray-scale lithography.
- **Photonics** Photonics used to be a niche application dedicated to long-haul data communication. Now it is migrating into the data center, handling connections between racks and within racks with data speeds on the way to 1 Tb/sec. The resolution needed to implement Si photonics is not particularly challenging by today's standards due to the 1300 nm wavelength typically used, however, CD control can be important due to the evanescent wave coupling between some waveguide structures. Arrayed wave guide devices require accurate waveguide lengths and smooth curves. Grid snapping and segmentation can lead to reduced device performance. In addition, there are applications that have ramped and curved features in the waveguide structures, which require gray-scale lithography to fabricate.
- **Micro-optics** Small lenslets, mirrors and gratings have been created using custom gray-scale lithography for applications such as microdisplays.
- **MEMs** Complicated micro-mechanical structures typically have several layers of patterning that can benefit from control of z-axis topography with gray-scale lithography. Applications include accelerometers and digital micro-mirror devices.
- **Biological structures** Silicon devices that interact with biological structures often require 3D surface profiles produced with gray-scale lithography. An example of this is a bed-of-nails structure formed by an array of cones.

In the case of curvilinear structures, approximation through the use of linear segments can perhaps get the job done for a while longer. The approximation can always be improved through the use of smaller segments and a finer grid at the cost of more geometries and computation. Gray-scale patterning is a bit different. It is similar to OPC in that the design information is modified to create a mask pattern that, when lithographically imaged by limited bandwidth optics, produces features close to the design intent. In the case of OPC, the feature edges are of primary importance; in the case of gray-scale lithography, the entirety of the exposed region is important. What is missing from the gray-scale lithography applications is the means to express the design intent that is also compatible with mask data infrastructure. This leaves the practitioner with the job of creating his own mathematical description and cobbling together scripts to run the existing two dimensional software tools.

I expect, as some of these applications become more mainstream, tools and formats will evolve to handle curved and 3D features more easily. Then we can escape the constraints of the two-level, Manhattan world.



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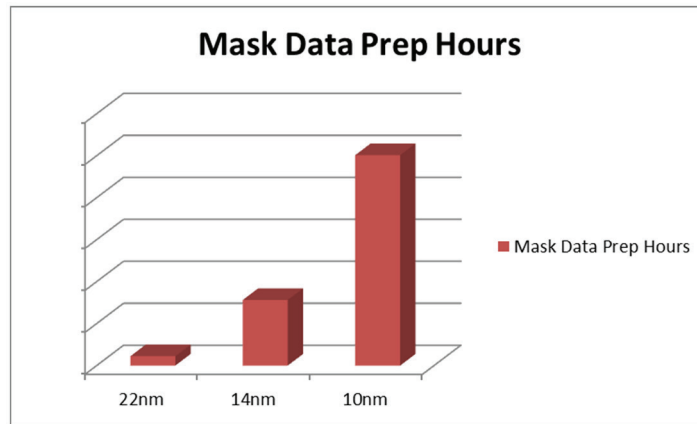


Figure 2. Relative increase in compute hours needed per mask set at mask fracture step per node for a mask set.

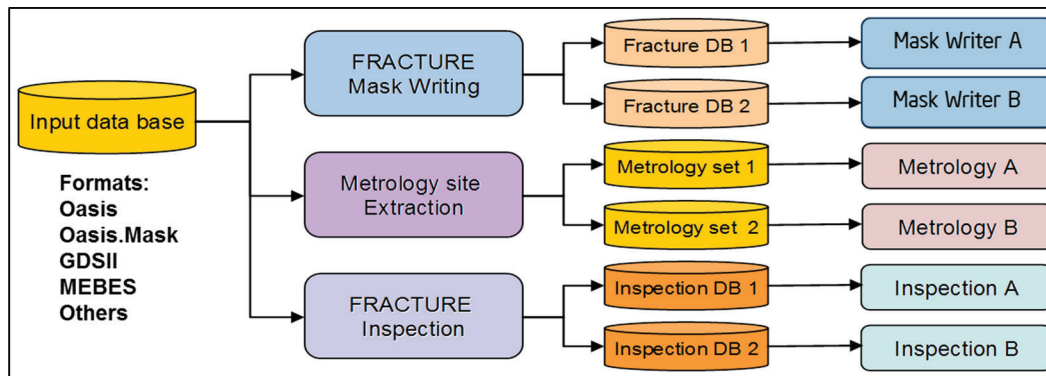


Figure 3. Typical Data Processing Flow.

There is a proportional increase in data processing power needed at data fracture. This increase is driven by the file size explosion, a product of the volume and complexity of the pattern figures. These complexities are due to the added decorations introduced at RET. However, there is an increased demand for processing power due to additional processing at the data fracture step, which has become essential in ensuring the proper mask patterning. As the mask requirements are becoming more stringent for the 10 and 7nm nodes [appendix A], additional mask error correction techniques like Mask Process Correction MPC<sup>5</sup> are now needed to correct for CD linearity and feature fidelity. These mask error corrections applied at the data fracture step (post tape-out) are closely related to the mask processing and therefore are ideally done at that step of the data flow. Figure 2 shows our predicted relative increase in compute power needed for the 14 and 10nm node mask sets.

The Data Fracture step is also required to prepare pattern files needed for the various processing tools in the mask shop. These tools require a machine specific format that is unique and at times proprietary for that tool set. Such varieties in required output format increase the overall mask set data size and also the required compute time. Efforts have been in place to incorporate a common format, Open Artwork System Interchange Standard (OASIS.MASK),<sup>6</sup> since 2006. However, the adoption has been slow, primarily due to the fact that downstream treatment of the data is still required to fit the unique needs of the processing tools. Figure 3 shows a

typical data fracture flow indicating the need for multiple unique output files which are required for the various processing tools.<sup>7</sup>

An ideal flow was shown in Zaatri (2010)<sup>7</sup> proposing the use of a common format to replace the multiple unique tool formats. The adoption of OASIS.MASK has not occurred across all platforms. In many cases the need to process the data for an individual tool specific format was not eliminated for practical reasons. The processing tools are designed to be efficient, and the toolspecific format is designed to adapt to that particular architecture.

## 2. Impact of Multiple Patterning

One key effective enabler of Optical Lithography extension into the sub 32nm regime has been Multiple Patterning<sup>8,9,10,11</sup>. In its simplest form, double patterning, two masks are used to print the lines on a single wafer layer. This is accomplished by exposing two masks with larger pitches but interleaving the patterns, resulting in the patterning of half the single mask pitch<sup>9</sup> on the wafer. There have been many variants of such techniques including the use of cut masks to make contacts and trenches<sup>10</sup> and the use of multiple masks (up to 8)<sup>10</sup> to make one layer on the wafer. The side benefit of this technique on mask making is that the single layer increased wafer complexity and scaling from node to node did not translate to a proportional complexity on the associated single mask. Previous predictions for the single layer write time for sub 32nm nodes have shown a potential mask write time of multiple days. In reality, the worst case layer mask has been a

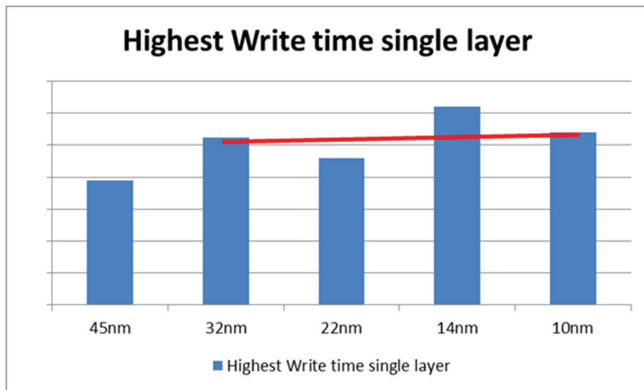


Figure 4. Maximum write time mask within a mask set per node.

constant node to node, as shown in figure 4 below.

This plateau in the worst mask write time was offset by a large increase in the total mask count required per set. Figure 5 shows actual number of critical masks required per node up to the 10nm node and a prediction of the number of critical masks needed at the 7 and 5nm nodes respectively.

In addition to the increased number of mask layers needed by Multiple Patterning, mask to mask overlay requirements<sup>11</sup> have also tightened, creating a significant disproportion to other lithography specification. This forced many layers to go into the E-beam writer not only for better resolution and Critical Dimension Control (CDU), but also to maintain a tight registration and overlay performance. These layers in previous nodes would have traditionally been written on the laser writers. However, laser pattern generators have not kept up with the technological advancement needs as laser pattern generators equipment development ended at around the 32nm node. Figure 6 shows the percentage of layers that are allocated to the E-beam within a mask set.

In Lee et al. 2010<sup>12</sup>, the single vs multiple patterning impact on the worst case layer was compared. In that study, it was concluded that the worst layer shot count in a multiple patterning scheme is 1/3 of that for single patterning. However, this may not have taken into account the loss of efficiency when splitting the single wafer layer into multiple masks. In our study, we simulated what would the shot count be without the loss of efficiency. In figure 7, we show the total shot count for all mask layers that comprise the single wafer layer vs the worst mask shot count. We then compare that to the simulated shot count if double patterning had not been used. The results show an increasing ratio at smaller nodes and further demonstrates a 2.5 ~ 3x reduction in the worst case mask shot count.

Multiple patterning may have saved the mask industry from layers that would require multiple days of write time; however it created a new problem of total number of hours needed to write the full mask set. In addition to the write time metrics for critical layers, the total numbers of days to deliver a complete mask set is a new additional metric that must be considered. This new metric of how many E-beam mask writer tools per mask set per week is something with which the mask industry is not familiar. To continue with the same architecture of writers, the same methodology for describing the pattern files, and aggressive RET, would require approximately 10 times as many beams at the 5nm node as at the 32nm node in order to maintain the same level of lead time in delivering a mask set to the customers. Figure 8 shows a graphical representation of that prediction.

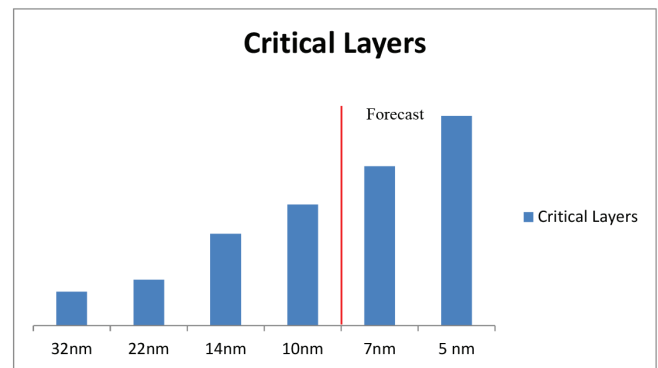


Figure 5. Number of critical mask layers within a mask set per node.

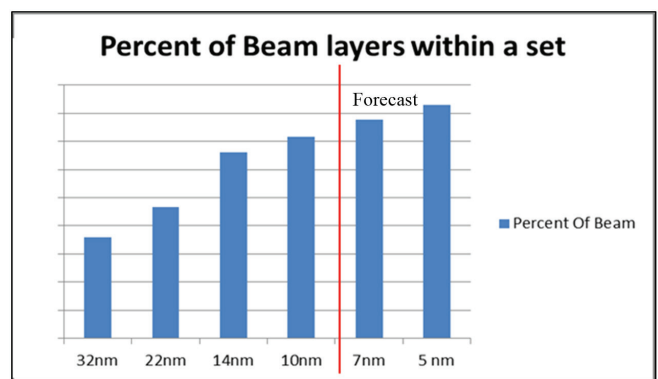


Figure 6. Percent of layers allocated to the E-beam writer within a mask set.

### 3. Data Formats Historical Perspective and What Changed

The basic building block for describing design geometries has not changed in years since the inception of the first mask writer about 45 years ago. In this section we will make a case for change. The new multibeam writer architectures are not optimized for Manhattan based data format. Due to historical reasons, unnecessary fracture steps are being inserted in the flow, compromising accuracy and imposing unnecessary limitations.

As shown in figure 9, in the early sixties, the mask layout layer was drawn by hand on Mylar sheets then imaged using optical reduction into emulsion glass substrates. Free hand drawing was later replaced with Rubylith cutting using coordinatograph tools which provided an X/Y draftinglike table to assist humans in creating the patterns. In the early seventies, automated optical pattern generator tools became widely used to replace Rubylith cutting. The tools had an X/Y stage and an optical aperture. Some of the pioneers were David Mann Machine division of GCA in Burlington, MA, and Electromask in Van Nuys, CA. Both the Mann and Electromask pattern generator (PG) had a data format consisting of rectangular shapes with a rotation from 0 to 90 degrees. AT&T Bell Labs<sup>13</sup> researchers were experimenting with both optical and electron beam mask writers that could print arbitrary shapes. Although the laser system was prototyped first, the decision was made to use an electron beam as an imaging source to overcome the resolution limitation of the laser and the optical mask sketching tool. Both the electron beam mask writer and the data format, MEBES<sup>14,15</sup> were commercialized by ETEC Systems and quickly

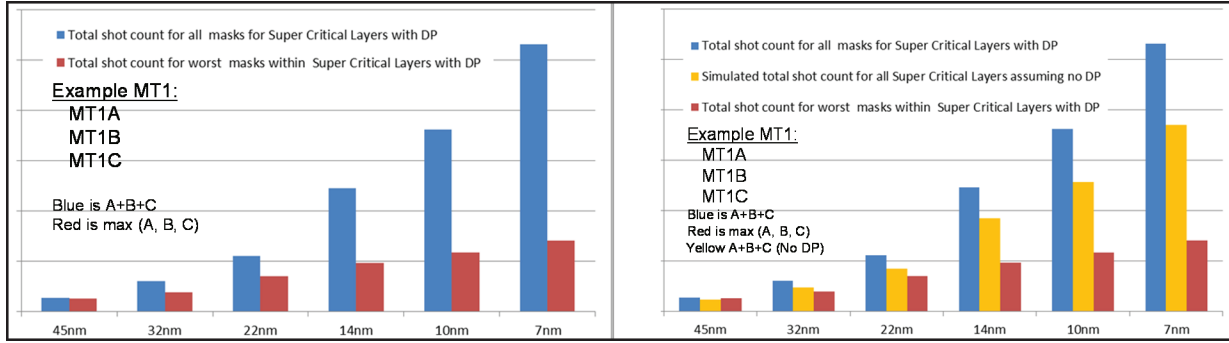


Figure 7. Shot count of single wafer layer using multiple patterning vs single patterning per node.

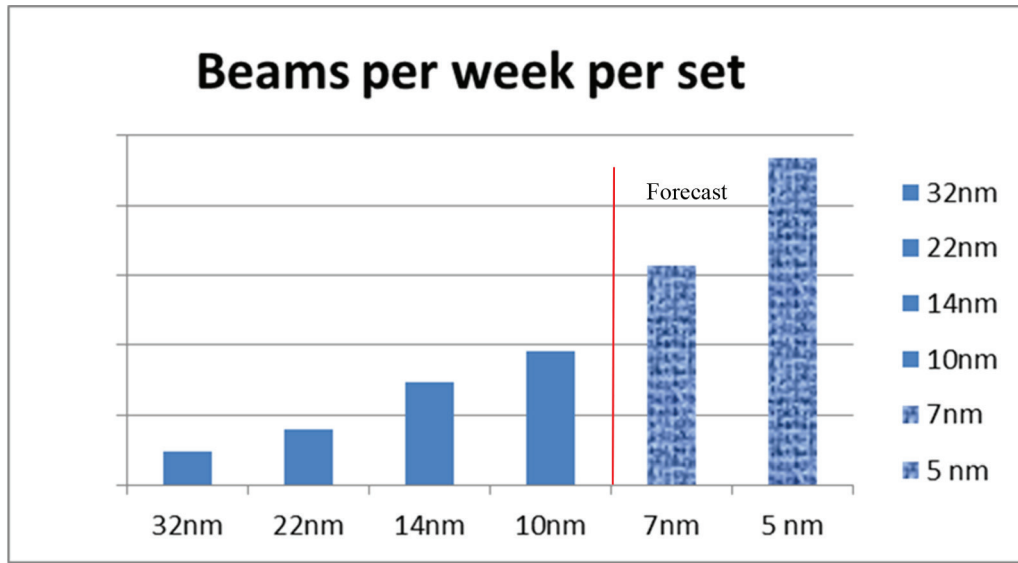


Figure 8. E-beams per week per mask set needed per week per node.

became the industry standard in the early eighties.

On the IC design side, Calma Company provided the CAD software for chip designers, which included a Layout Interface Data format, GDS. Once the design was completed and passed the verification step, it needed to be sliced into multiple layers, each containing the layout required for the associated mask layer. Although a number of companies had internal CAD capabilities to perform the design, verification and layout separation, the Calma GDS pattern format became the de facto standard by the mid-eighties. A conversion step to a machine-proprietary format like Mask Writer, Mask Inspection, and Mask Metrology was, and is, still required.

During the eighties and nineties, both GDS and MEBES continued to be the standards for the industry; GDSII at the IC design end and MEBES at the equipment interface side. A number of tool specific formats were in use to match the equipment makers' needs, such as those for EL3/IBM, JEOL, Hitachi, HP, Toshiba, Micronic, Ateq, and KLA-Tencor. Further, Transcription Enterprises (now Synopsys) introduced Cref and Cflat, an intermediate format used in converting GDSII into the multiple required outputs, including MEBES for writers, KLA-Tencor for inspection, and JEOL and Hitachi for alternate mask writers. In the year 2000 and beyond, the VSBx format was introduced by Toshiba (now Nuflare)

as a tool specific format for the Toshiba/Nuflare mask writer. All these formats utilize Manhattan and triangles as the primitive for evolutionary reasons. Most significantly, the tools' architectures themselves were well suited well for such primitives.

Manhattan representation was an effective form of data compaction as long as the feature imaged was significantly larger than the basic primitive. In figure 10, we show a number of examples where effective compaction can be achieved using Manhattan primitives. For example, in a single beam raster tool, 48 dots can be described by only few bytes. Similarly, in a single beam Vector Shaped beam, a number of shots can be fitted within one large trapezoid. In laser writers or tools that adopt multipass writing strategies, a large number of pixels can be fitted in one trapezoid. Common problems, such as edge fidelity due to grid snapping errors, raster algorithm approximation of odd angles, and slivers and stair case approximation of angled lines, were tolerable as long as the feature of interest on the mask was much larger than such error.

On the design side, a new layout interchange format for ICs was introduced and adopted as a SEMI standard in 2002 and 2006. The new OASIS format was to replace GDSII by allowing more efficient compaction and maintain the polygon primitives. OASIS is now widely used and has proven to deliver on the promise of reduced file size, increased resolution, and efficient data processing.

<p><b>~1960</b></p> <p><u>hand drawn lines</u></p> <p>On Red Mylar</p> <p>10x reduction optical projection</p> <p>2 in mask</p> <p>Curvilinear was OK</p>	<p><b>1965~1975</b></p> <p>First MASK writer "David Mann PG"</p> <p>X,Y aperture</p> <p>Optical projection</p> <p>X,Y and rotation</p> <p>First data format "Mann PG"</p> <p>Only Manhattan</p>	<p><b>~1971</b></p> <p><u>Calma Stream</u></p> <p>GDSI</p> <p>Layout design Format</p> <p>Allows Hierarchy</p> <p>Polygon Description</p>	<p><b>1975</b></p> <p><u>MEBES</u></p> <p>MEBES Data Format</p> <p>Tool Specific format</p> <p>Flat data, sorted in stripes</p> <p>Four basic primitives</p>	<p><b>1980's</b></p> <p><u>MEBES, Jeol, Cref, Leica, Hitachi, IBM, HP, Toshiba, Micronic, Ateq ...etc</u></p> <p>Tool Specific format</p> <p>basic primitives</p>	<p><b>2002, 06</b></p> <p><u>Oasis (02)</u></p> <p>GDSII improvements</p> <p><u>Oasis.Mask (06)</u></p> <p>basic primitives</p> <p>No Polygon description</p>
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Figure 9. Time line of Mask Pattern Data Formats.

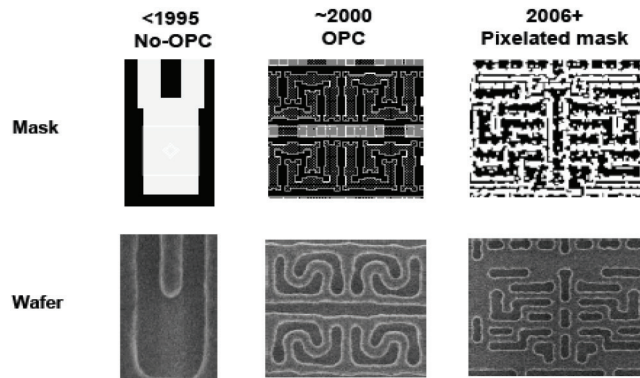


Figure 9. Increase of mask complexity required to meet patterning needs since 1995.

One obvious question remains: Why could the equipment makers not take OASIS directly? OASIS is a high level format with unlimited nested hierarchy. A feature can be defined as a polygon, a group of polygons or even a higher level function like a memory cell. The data is organized by functions with little consideration to sequence in position. Almost all mask equipment has an X/Y stage and the pattern is written, inspected or measured in a sequential order. As a minimum, a reordering of the features to be printed is required, as is a flattening step to discover all instances of a feature. In order to perform the sorting per location, the hierarchy must be flattened to see exact locations of features. This results in a processing time in the order of hours. It is economically prohibitive to have a very expensive machine with a stage, vacuum, laser or e-beam source sitting partially idle awaiting its pattern preparation computers to finish the sorting of the OASIS pattern file.

OASIS.MASK was introduced in 2006, and was more suitable for tools, as it had limited hierarchy, and was intended to be a universal format to alleviate the need for the multiple tool specific formats. In doing so, however, the basic fundamental primitive

was set to Manhattan and triangle shapes. In GDSII and OASIS, polygon representation is allowed, providing a basis for curvilinear representation. However, as data conversion takes place into OASIS.Mask, the polygon representation is lost and geometries are reset to Manhattan and triangles.

#### 4. OPC/ILT Impact on Shot Count

It is well known that mask complexity is increasing from node to node to meet wafer patterning challenges<sup>16,17</sup>. Figure 11 highlights the evolution of mask design<sup>18</sup>. One of the driving forces is the improvement of wafer print accuracy. The purpose of the mask is to generate wafer level images with minimum deviation from the target shape with sufficient process latitude. The OPC modelling step iterates between mask shapes and simulated wafer images until a suitable result is produced<sup>19</sup>. As shown in figure 11, the result of this is a target mask contour which the mask making process is tasked with producing.

Currently, the target mask shapes are approximated by Manhattan polygons, as shown in the top flow in figure 12. Single beam Variable Shape Beam (VSB) tools can only expose rectangular

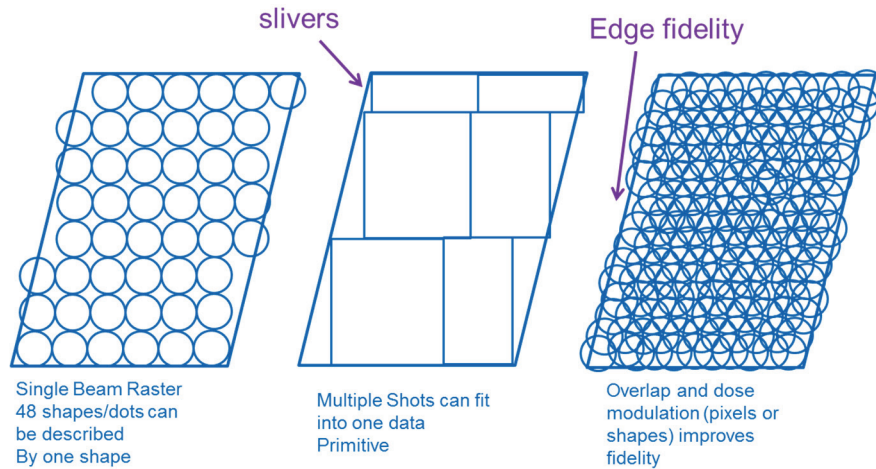


Figure 10. Data Compaction Examples for various mask Writing tools.

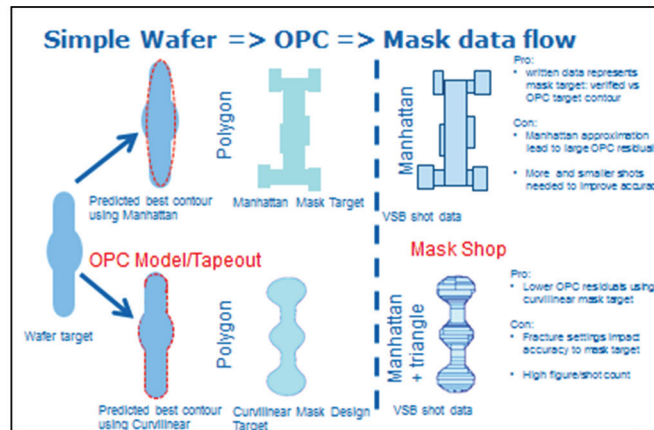


Figure 10. A comparison of Manhattan (top) and polygon flows (bottom) from OPC to VSB mask data.

and triangular shots. The incoming polygon data is fractured into individual figures, which the writer converts into shots. As discussed in the literature<sup>20</sup>, Moore’s Law results in an increase in the number of features per unit area and therefore an increase in the total shot count. Straight scaling results in a 2x increase; however, more aggressive OPC scaling will cause a larger than 2x increase.

The restriction of using Manhattan shapes limits the ability to hit the wafer target<sup>21</sup>. Recently, inverse lithography technology (ILT) has been deployed. The ILT process outputs mask target shapes that are more closely approximated by curvilinear shapes<sup>22</sup>. The current flows include a step to approximate the curved target shapes with Manhattan geometries<sup>21,23</sup>. However, this requires extra computational steps and further creates a tradeoff between lithographic quality and mask complexity. One option to improve the accuracy would be to use curvilinear figures to represent the mask target shape. By removing the edge placement restrictions inherent to the Manhattan representation, the mask target shapes will have additional degrees of freedom and should result in better model accuracy and wafer prints. Schematically, this is indicated in figure 13b in the lower flow.

The conversion of curvilinear polygons to VSB compatible shots produces new errors which need to be considered. This option is shown in the lower flow in figure 12 and in figure 13a-b. As dis-

cussed in the next section, it is possible to reduce these errors but at the cost of higher shot counts.

### 5. Fracture Error Impact on Mask Fidelity

If the incoming data is Manhattan, the edges produced by the VSB shots exactly match the original mask target data, as shown in the top flow of figure 12. In the case of the curvilinear data, this is not possible. The fracture of curvilinear polygons into Manhattan shapes produces approximation errors, since the edges have to be approximated using rectangular and 45 degree triangle shots on VSB tools.

As shown in figures 12 and 13a-b, the fracture step required to prepare VSB exposure data introduces deviations between the written and the design edges for features at arbitrary angles. Since this error is introduced after OPC, it is not comprehended by the OPC model. This introduces a risk of poor wafer print performance and may require an additional modelling check post-fracture. This is a difficult requirement as the step is late in the flow. This is one reason why some EDA companies do Manhattan simplifications at the OPC step.

These approximations also degrade the mask CD performance. Figure 13c demonstrates this, with the LER of angled lines printed using a VSB tool being higher than a straight line. The horizontal axis measures the maximum deviation between the written data

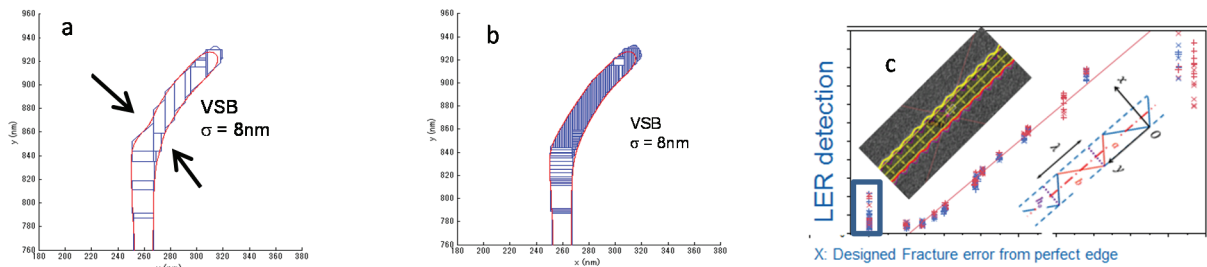


Figure 11. A comparison of (a) coarse and (b) fine fracture settings on VSB data if the input shape was polygon. Solid curves are simulated exposure contours with  $\sigma = 8\text{nm}$ . (c) Experimental data of approximating an angle edge by polygons is shown. The approximation error gets larger from right to left. The printed line image is compared to the original design and the LER is extracted. As the deviation error  $X$  is reduced, the LER signal falls below the background LER of straight lines (enclosed in the box).

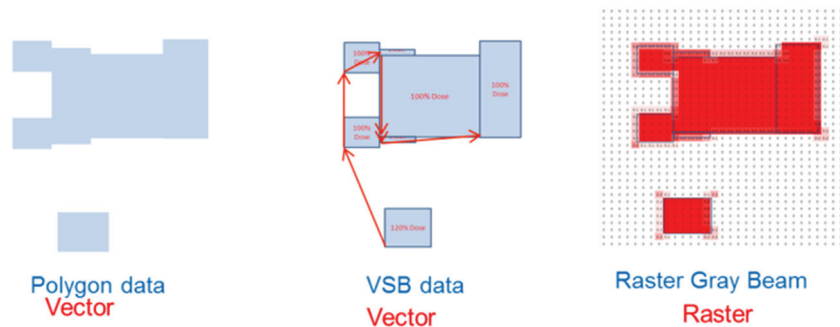


Figure 12. Illustration of how PEC requires different areas of the original polygon data to be exposed with different doses.

and the original edge. As the deviations get smaller, the LER signal is indistinguishable from the straight line background. This is accomplished by using finer rectangles/triangles during the fracture step, as shown in figure 13b.

The approximation errors will not be detectable by using suitable fracture settings. However, the cost of using finer fracture settings is higher shot counts and longer writes. The user will need to manage the tradeoff between accuracy and shot count. For the past half-decade, several companies have proposed using overlapping shots to print curvilinear features using VSB tools<sup>24,25,26</sup>. These approaches require complex modeling to produce the shots.

Ideally, one would prefer to deliver polygon data to the mask writer and have the writer print with no error and no impact to write time. This is not possible with VSB tools. Recently new generations of multibeam mask writers are being developed<sup>27,28</sup>. These tools use a raster write strategy which renders the mask image with pixels and not shots. The write time depends on the pixel delivery rate and exposure area. If the datapath has sufficient bandwidth, the pixel delivery rate is not impacted by incoming data complexity (i.e., number of vertices). Additionally, the print strategy results in equal fidelity of Manhattan and arbitrary angle edges. These tools are ideally suited to handle curvilinear polygon data<sup>29</sup>.

There is one limitation preventing the preservation of polygon data through the write step for multibeam tools. This limitation arises from the proximity effect correction (PEC), which varies the dose on a per figure basis. Since VSB tools expose and adjust dose per shot, the PEC capability is built into the fracture data flow, Figure 14. Multibeam tools will also require some level of fracturing so that features can be tagged to receive different dose. The vendors appear to be reusing elements of the VSB fracture tools and flows by approximating curvilinear polygons with rectangles

and trapezoids. This, again, introduces errors which need to be managed via fracture settings.

In order to take full advantage of multibeam mask writers, we are proposing a new data format to be created. One new feature would be the inclusion of new figure types with continuous curvilinear edges. These may be extensions to circles and curve commands, both of which were allowed in previous formats. The second change would be to create a curvilinear fractured format to enable PEC corrections, as shown in figure 15. This will require the cooperation between EDA vendors, writer manufacturers and customers.

## 6. Simulator

In order to facilitate a new data format that can take full advantage of a multibeam mask writer, we have been developing an in-house multibeam writing simulator. This simulator is designed to emulate actual writing modes of multibeam writers based on publicly available information in the literature<sup>26,30</sup>. One of the key features of this simulator is its capability of loading pattern data as generic polygons, which are not allowed in OASIS.MASK but are in OASIS. As the simulator emulates rasterized writing using 5nm grid and 20nm square beam, the first step of simulation is creating a dose assignment map with a 5nm grid for a given polygon structure. This step is straightforward, as schematically shown in Figure 16.

When an input polygon is overlapped with the 5nm writing grid, the doses assigned to each grid can be calculated to be 1 for the grids within a polygon that is smaller than original polygon by a fixed size, and 0 for the grids outside of another polygon that is larger than the original polygon by the same fixed size; and fractional values between 0 and 1 to the grids in between. A detailed algorithm of computing fractional doses can be more sophisticated to improve the accuracy of edge locations. However, the key



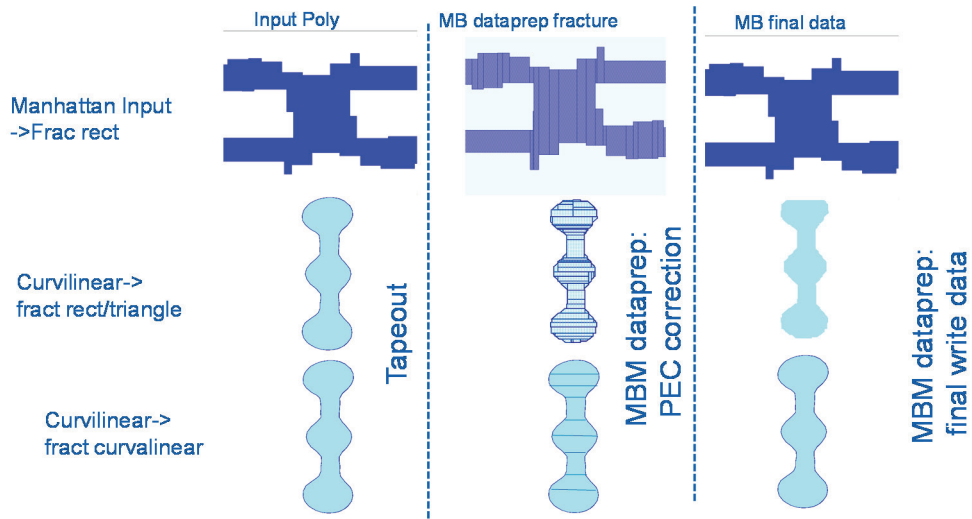


Figure 13. Comparison of the current and ideal mask data flow.

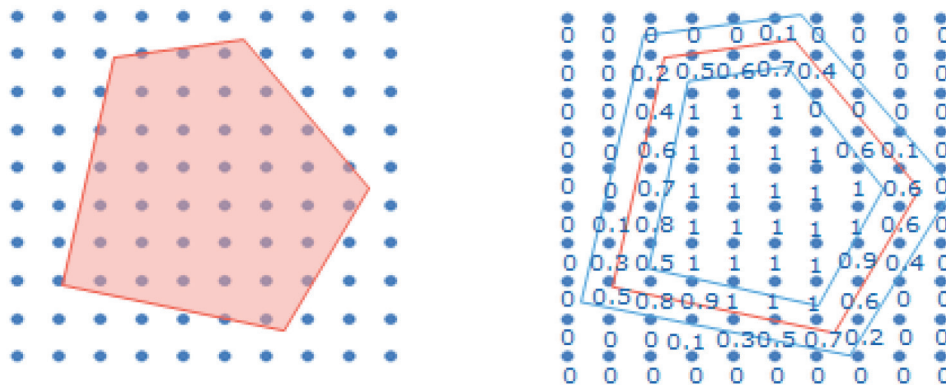


Figure 14. Schematic illustrations of rasterized dose assignment in multibeam simulator.

point is the simulator does not need to fracture the polygon into smaller figures. This is why a polygon is better suited as a data input structure for a raster beam machine with much smaller data size, especially polygons which represent curvilinear structures.

In actuality, when fractured trapezoid data is the input, the first step is to synthesize the fractured trapezoids into a polygon to effectively run this rasterization algorithm. Therefore, there is no fundamental need for the incoming data to be fractured into trapezoids. Rather loading polygons, even if they need to be cut into smaller sizes if the polygon extent is too large, is the most efficient way of running the next step of multibeam writer simulator.

The normalized dose is modulated as needed for PEC or fogging correction followed by digitizing into 241 levels<sup>31</sup>. These can ultimately be represented by 0-15 levels for each grid by a simple matrix computation to emulate 4 bit intensity data. Aerial image calculation is essentially the same as overlapped VSB simulation, where only a 20nm square beam is assigned with 16 level doses.

The dose modulation for PEC in this simulator is simply implemented by directly specifying backscattered electron dose from users. Dose modulation follows to compensate for the backscattered electron dose, similar to the way CDs at a threshold are the same. The computation of dose modulation values, for a given pattern data in a self-consistent fashion, should be possible

for coarsely gridded sections, such as 640nm, by following a methodology explained in the literature<sup>32</sup>. However, computation implementation is beyond the scope of this handy simulator. The important point is that dose modulation-based online PEC could be possible after the rasterization of polygon data using the known methodology. While offline PEC, with sizing-based correction, might utilize OASIS.MASK trapezoid data, online PEC will not necessitate any trapezoid fracturing of original polygon data. This further supports use of polygon in the intermediate data format in multibeam writers.

Figure 17 shows the CAD tool view of OASIS data of an ILT pattern, as well as its aerial image simulation results, through use of the simulator explained in this paper. The simulation used a 20nm square beam and a 5nm grid (quad mode) with 5nm sigma process blur (kernel FWHM = 11.8nm), following a rasterization of the input polygon data and digitizing into 241 levels. It is well demonstrated that the polygon worked as input data for multibeam writing simulation, and hence is a candidate indicative of the new data format for intermediate mask writing data for multibeam mask writers with significantly reduced data volume compared with OASIS.MASK.

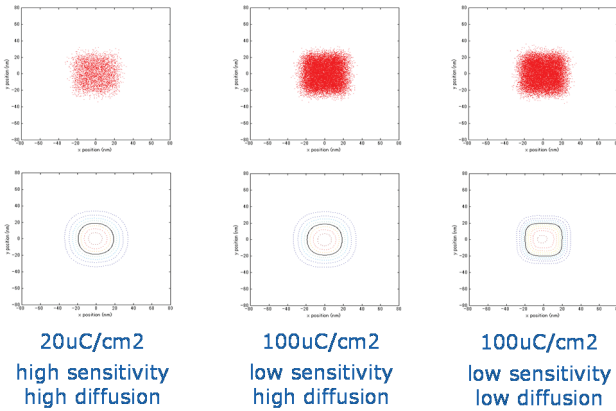


Figure 15. Isolated Hole: Monte Carlo Simulation for various dose and diffusion combination.

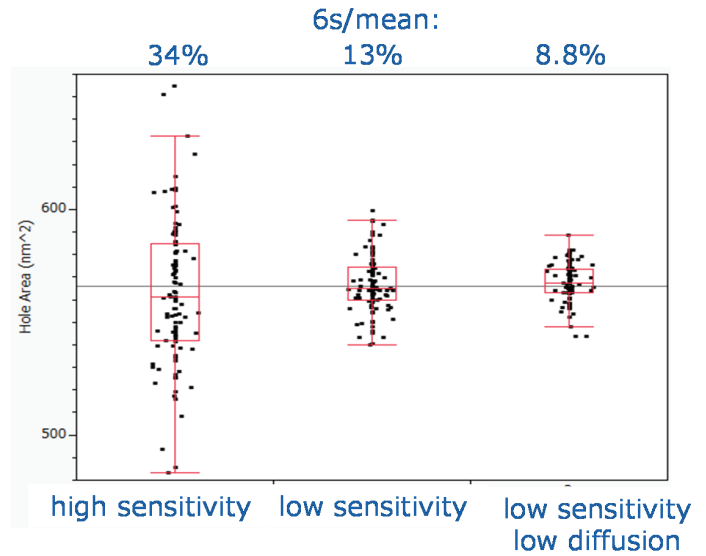


Figure 16. Hole Area Variation Simulation.

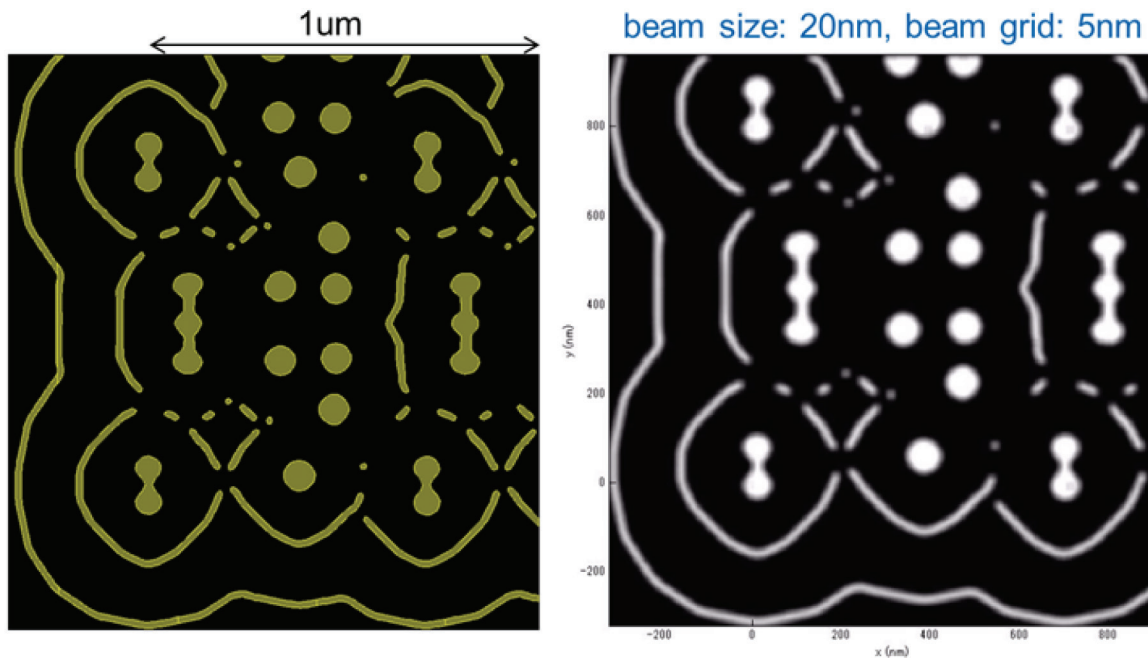


Figure 17. Pattern review of ILT data in CAD tool (left), and grey scale aerial image simulation using multibeam writer (right).

### 7. High Dose Resist and Process Results

In Jamieson (2011)<sup>33</sup>, it was shown that a lower sensitivity resist is necessary to meet future node requirements. With that in mind, we developed a simulator based on the Monte Carlo model<sup>34</sup> taking into account the electron trajectory in the resist and the beam blur from the exposure system, along with the diffusion characteristics of the resist. The simulator calculates the acid density profile from which we determine the contour at threshold. Figure 18 shows the results from various simulations of an isolated hole.

In figure 19, we show the resulting 6-sigma results of the hole area from a 100 time repeated simulation to quantify the variability. In this simulation, the tape size of the hole for the low sensitivity and low diffusion resist was shrunk so that the average area of

each hole is equalized with the other two cases even at different corner rounding and to make the comparison neutral to the finally delineated area. More specifically, 32 x 32nm, 32 x 32nm, and 27.2 x 27.2nm tape hole sizes are selected for high sensitivity and high diffusion resist, low sensitivity and high diffusion resist, and low sensitivity and low diffusion resist, respectively. This change results in a smaller electron count for the low sensitivity and low diffusion resist than that for the low sensitivity and high diffusion resist by about 28%. Despite the decreased number of electrons, clearly a low sensitivity and low diffusion resist produces the best results.

In 2012 we presented a paper at SPIE<sup>19</sup> in which we made a case for the need for a Multibeam Writer to meet the demand of the future nodes. We presented an impartial view of the available

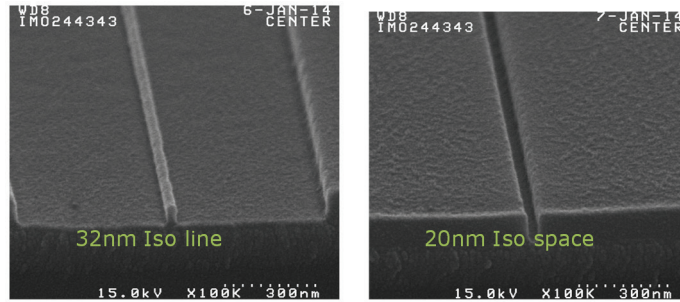


Figure 17. Resist cross sections of 100uC/cm<sup>2</sup> printed on IMS tool.

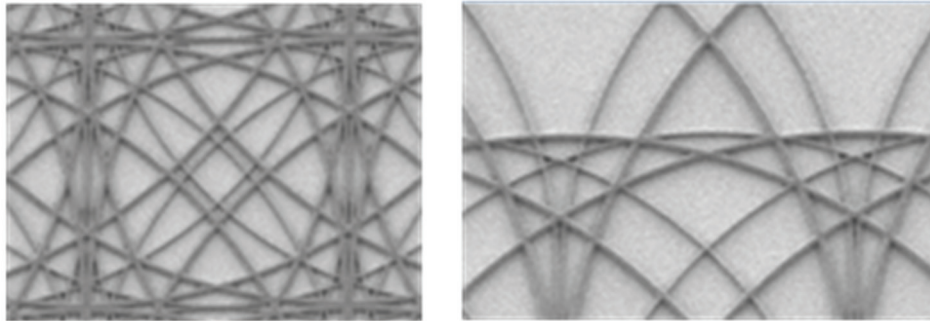


Figure 18. Top down SEM images of curvilinear patterns printed on IMS tool on negative tone resist. Images are courtesy of Photronics, Inc.

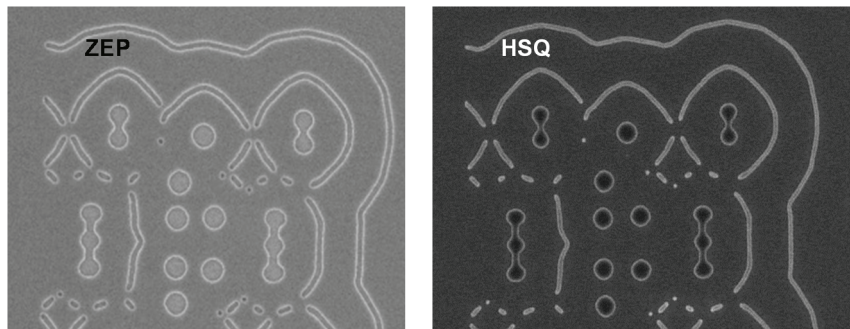


Figure 19. Mock ILT pattern printed on IMS tool. Images are courtesy of Dai Nippon Printing Co., Ltd.

architectures. We continue to be impartial and welcome technological breakthroughs to advance the technology.

Recently, a multibeam mask writer, being developed by IMS, has become mature enough to print test masks. The tool uses a raster based writer strategy and E-Beam dose modulation<sup>35</sup>. It is capable of delivering sufficient dose to enable the use of slow resist at reasonable write time. Figure 20 shows cross sections of a ~100uC/cm<sup>2</sup> resist on a plate printed on the IMS proof of concept tool (POC). The line and space resolution are 32nm/20nm, respectively, which meet the 7nm ITRS<sup>11</sup> node targets. Figure 21 shows SEM images of curvilinear features printed on the same tool on an NCAR resist. There was no throughput impact printing these arbitrary angle patterns and there are no detectable artifacts of rendering the arbitrary angle lines. Another example of printing curvilinear features is shown in Figure 22, which is a mock ILT pattern. This design is composed of polygons with a relatively coarse distribution of vertex points defining the edges. The tool has sufficient resolution to resolve discrete changes in

angle inherent to the design.

## 8. Summary and Conclusion

The extension of optical lithography has impacted the mask industry in two key areas: the enormous increase in the complexity of shapes that represent an IC single layer design for patterning purposes and the increase in the number of masks needed for single wafer layer patterning. Both are driving the mask set data volume explosion, increased data processing time and much increased mask set write time. Without a technological breakthrough, the number of writers needed at the 5nm node level would reach approximately 10 times that at the 32nm just to maintain the same mask set delivery lead time. Much progress has been made in the area of multibeam writers, promising improved write times by utilizing Massively Parallel Architecture, E-beam dose modulation, and novel writing strategies. All are aimed at not only reducing write time, but also keeping up with the future node resolution requirements by providing more than an order of magnitude higher dose.

These factors open the door for low sensitivity and low diffusion resists that were not previously considered.

The data format is at the core of the writer. With time, the industry migrated towards Manhattan and triangle figures as the fundamental primitives to describe the IC design. These primitives have not changed for more than 45 years. During the VSB era, such primitives were natural multiples of the VSB tool aperture repertoire. Furthermore, prior to OPC/ILT, the design geometries were much larger than the aperture repertoire. Thus, the format provided an efficient form of compaction. However, the advent of OPC/ILT has created the need for finer jogs and decorations. The design geometries are now approaching the tool aperture size and the compaction benefit is diminished. This is more prevalent when trying to describe a curvilinear shape by many small Manhattans and triangles.

The multibeam writers fundamentally are raster tools and are built to deal with massive amounts of data including curvilinear shapes. Due to the existing data processing infrastructure and historical reasons, complicated designs which start as polygons are being forced to fit into Manhattans and trapezoids in order to be compatible with today's data formats. They subsequently are converted into polygons inside the multibeam writer as part of the rasterization step. Accuracy is lost in the conversion process, not to mention the additional time wasted with the unnecessary conversion steps.

In this paper, we demonstrated through simulation the direct rasterization of polygons and curvilinear shapes is doable. We further have shown simulation and initial results of the effects of high dose and the use of low sensitivity resists.

In conclusion, we recommended an industry wide effort to create a new data format which allows the polygon representation to be carried into the multibeam writer without the need for intermediate steps of converting to Manhattan shapes. We also proposed ideas for such a format to overcome potential limitations when using polygons for PEC correction.

## 9. Acknowledgements

The authors would like to acknowledge the contributions of Drs. Bassam Shamoun, Yulia Korobko, Reid Juday and Bin Liu of Intel Mask Operation for their diligent work in experimental data. We also would like to acknowledge Jim Wiley of ASML for the invaluable insight and historical perspective on the origins of data format and the mask industry.

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## Appendix A

### 7 nm Node Requirements

Area	Challenge	Scale Factor	Scaled ITRS Reqt	Areas of Focus
Data volume single layer	More ILT More layers	~2x	~6 TB	Write Tools EDA tool/Data format (for efficiency/TPT)
Mask sub-res min feature	LER vs defect size	~.7x	~30nm	Blanks Materials (resist, charge dissipation) Process stability Reg enhancements
CDU 3s dense lines	Capability scaling	.7x	.6-.9nm	
CD ATT	Capability scaling	.7x	.9-1.3nm	
Image Placement	Capability scaling	<.7x	1.3-1.8nm	Inspection Repair capability
Defect size	More ILT More layers	.7x	10-14nm	



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# Industry Briefs

## ■ TSMC to Use EUV for 7nm, Says ASML

Alan Patterson, EETimes

12/8/2014

HSINCHU, Taiwan — ASML NV, Europe's largest maker of chip-production equipment, says that Taiwan Semiconductor Manufacturing Co. (TSMC) plans to buy two extreme ultraviolet (EUV) scanners next year to extend the boundaries of its process technology, potentially to 7 nanometers.

"The EUV scanners are for 10 nanometers," said ASML executive vice president Frits van Hout in an interview on the sidelines of a TSMC event on Dec. 4. "They're going to use them to prepare for production in 7 nanometers."

TSMC spokesperson Elizabeth Sun declined to comment.

The shift toward EUV may signal a switch in the conventional wisdom on the next generation of lithography equipment. The earlier expectation was for chipmakers to use traditional immersion lithography for production of 10 nm chips instead of the long-delayed EUV systems.

ASML said on November 24 that TSMC has ordered two NXE:3350B EUV systems for delivery in 2015 with the intention to use the systems in production. In addition, ASML said two NXE:3300B systems already delivered to TSMC would be upgraded to NXE:3350B performance.

## ■ Cypress Bids \$4B For Spansion

Rick Merritt, EETimes

12/1/2014

SAN JOSE, Calif. — In another sign of the consolidating chip industry, Cypress Semiconductor Corp. hopes to merge with Spansion in an all-stock deal valued at \$4 billion. The deal would create an expanded embedded chip vendor with \$2 billion in annual revenues, half in mainly NOR flash and SRAM memory with the rest split between microcontrollers and analog parts.

T.J. Rodgers will remain as chief executive of the merged company under the Cypress name. Although Cypress is the slightly smaller of the two firms, it has had consistent profits while Spansion has been crawling its way into the black, in part due to the decline of its core NOR flash business.

The combined companies will not have enough heft to break into the world's top 20 chip vendors which these days requires nearly twice as much in revenues. However they claim they will be the world's fourth or fifth largest supplier of chips to car makers. They will rank eighth in automotive microcontrollers and ninth in the overall MCU market.

## ■ IC design houses gearing up for 64-bit smartphone boom

Cage Chao; Steve Shen, DIGITIMES

December 2014

With Android phone makers pushing for migration to 64 bit architecture, chip suppliers including Qualcomm and MediaTek are set to introduce new quad- and 8-core 64-bit solutions in the first half of 2015, according to industry sources.

Sources at China-based handset ODMs also revealed that 64-bit 8-core CPUs are likely to become standard specifications for the mid-range to high-end smartphones in 2015, while 64-bit quad-core processors will be the mainstream specifications for the entry-level to mid-range models, said the sources.

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