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EUV mask defect mitigation through pattern placement

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ABSTRACT

One of the challenges of EUVL is to bring EUV mask blank defect levels to zero. With uncertainty on when defect free masks may be routinely available, we explore a possibility for effectively using defective EUV mask blanks in production with a defect avoidance strategy. The key idea is to position the pattern/layout on the blank where the defects do not impact the final wafer image. Assuming that layout designs contain some non-critical areas in which defects can be safely positioned, it may be possible to align these regions with a given, small set of defect positions mapped from an imperfect mask blank.

Using a few representative assortment of current-node, full-chip layout patterns we run multiple trials against real blank defect maps with various defect counts successfully. Our goal is to assess the probabilities that defect avoidance will work as a function of mask blank defect count, and by lithography layer.

1. Introduction

While similar to conventional optical lithography in many respects, Extreme Ultraviolet Lithography (EUVL) impacts many supporting infrastructure technologies beyond the exposure tool itself. In addition to the disruptive changes in exposure tool technologies—reflective optics, exotic light sources, vacuum environment—infrastructural technologies impacted include needed new resist and etch processes, new mask materials, new mask blank and finished mask inspection tools, mask handling in the absence of pellicle, and so on. Challenges in all of these supporting areas must
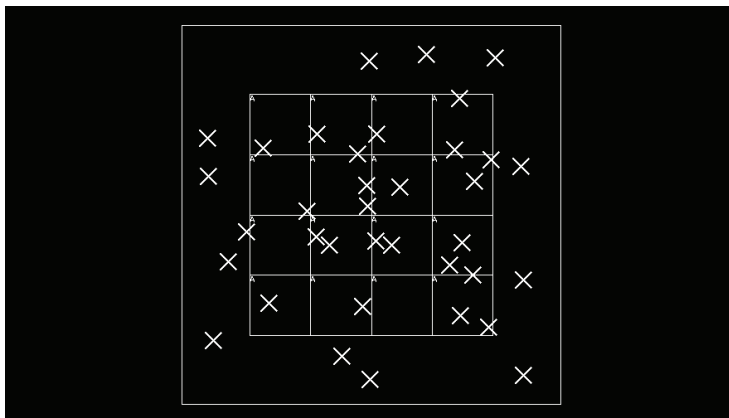
Figure 1. Example mask blank (outer square) with defects (X's) and an arrayed mask layout pattern (inner rectangle grid).

TAKE A LOOK INSIDE:

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SPIE

EDITORIAL

"To the Cloud"

Wolf Staud, Applied Materials

By the time most of you will get to read this, we are well on our way into 2011, so first of all, on behalf of the Executive Office, the Steering Committee, and the Symposium Program Committee, it is my pleasure to wish you all a HAPPY NEW YEAR! May the New Year be even more prosperous and successful than the past.

It is also my pleasure to introduce to you this year's BACUS officers: Artur Balasinski- Secretary, Larry Zurbrick-Vice President, and myself, Wolf Staud- President. As elected officers it is our responsibility to ….

Let's look back for a moment: In the year 2000 I was fortunate enough to live in Manhattan on a company assignment. A year where America was richer than ever before. Dot.com was in full swing, Wall Street was making money hand over fist, and the City was booming. I remember looking inside the Del Frisco Steakhouse on an early Friday afternoon, and the bar and restaurant was overcrowded with successful young brokers and entrepreneurs, sipping Martinis, and having lavish business dinners.

A week ago I was back in New York for two days, and to my greatest surprise – the picture did not look a whole lot different: bars and restaurants full, department stores crowded with holiday shoppers, company bonuses are back, and so are company holiday parties in almost all venues at night. It appears that the economy is on an uptick, and that the much quoted 'confidence' of the consumer is back – or at least on the rise. Much of that was mirrored in our industry this year. A banner year! With growth of 31% to a landmark revenue of $300.3B. Most companies showed record profits, huge increases in revenue YoY, and 2010 was being compared to the only three other years (1988, 1995 and 2000) when revenue growth had been >30% in any one year. Semiconductor revenue grew $71.9 B in 2010 — the largest single dollar increase for the semiconductor industry in any one year.

So what will 2011, or the next decade bring? We read of signs of overcapacity, of high inventories, all the usual signs and announcements ringing in a cyclical contraction. But all forecast so far remain optimistic, while some companies have slowed hiring or even frozen some of their reqs. One of the most inspiring talks that some of us witnessed this year was by Kiyoshi Kobayashi, CEO of the Semiconductor Division of Toshiba Corporation, in his keynote at the Kobe EUV Lithography Symposium in October. He took the audience 'to the cloud' – taking a look at the technology innovations coming with and necessary for the much heralded cloud computing. Cloud computing is all the rage, and most certainly the 'phrase du jour'. According to Kobayashi's presentation, we are already on a track of an ever widening gap between memory capacity we can produce, and what is actually needed by the many, many millions more that are joining the web every year from now on. 35 Zeta-byte is what he described as the need. But most of all was the requirement for replacing HDD media with Flash SSD. Not for speed or capacity reasons, but - for environmental impact. A switch to SS memory in the WW cloud computing farms will alleviate the need for the equivalent of 75 nuclear power plants, much in line with their three important environment-related themes: "Greening of Process", "Greening of Product" and "Greening by Technology".

We see our industry changing. We see our industry adopting. We see it 'greening'.

Most of all: we see it growing! Have a great new year.

Figure 2. With space defining absorber (a darkfield mask) the layout pattern can be rotated and repositioned so that both defects fall into "harmless" areas, as shown in the right hand image.

be resolved before practical high volume EUV production is real.[1]

One of the most significant infrastructural changes brought on by EUVL is the change from optical transmission masks to the reflective masks needed for EUVL. To maximize reflection at 13.5nm wavelength, the mask blanks contain a Bragg reflector constructed from a stack of 40 to 50 Mo-Si alternating layers. Each of these 4-5 dozen component layers, (in addition to other material layers such as Ru cap layer, TaN absorber layer, CrN conductive layer), is a discrete processing step with a cumulative opportunity for adding defects.

Early EUV mask blanks contained thousands of defects. With first generation mask-blank inspection methods limited to detecting 80nm defect size the trend of detectable defects showed steady progress, with defect counts dropping to hundreds by 2007. However, improving blank inspection capabilities reveal an increasing number of previously undetected but relevant defects. Increasing the detection to 50nm from 80nm raised the defect count by more than an order of magnitude.[2] The relevant defect levels on EUV blanks will remain unknown until EUV blank inspection tools are capable of resolving them. In spite of steady progress in EUV blank manufacturing technology, it is quite possible that EUV blanks will not achieve zero defectivity by the time they are needed for production.

If EUV mask blank defects are not resolved by EUV high-volume production then some method will be required to deal with defective mask blanks. The complex multilevel structure of the blanks may make mask blank repair, certainly below the top mask blank layer, all but impossible. An alternative approach is to render the defects harmless by shifting the mask layout on the blank so that all defects occur where they cannot impact the resulting image on the wafer image. We call this "defect avoidance."

2. Experiment

Our experiment is to test the defect avoidance method to a set of mask layouts constructed from real circuit designs applied to a set of ten defect maps measured from actual EUV mask blanks. Seven mask layouts were derived from an assortment of lithography-layer designs shrunk to 11-22nm node dimensions. To maximize filling the EUV exposure field (26mm X 33mm) relatively small circuit layouts were arrayed edge-to-edge, with no intervening frame space between array instances. For this experiment the dispositional area was confined to be under the mask absorber layer, which corresponds to either the defined feature or space

of the mask layout, depending on the process tone. The dispositional area also includes the region outside of the arrayed mask layout, where defects do no harm. The measured defect maps were converted to layout patterns with rectangles corresponding to the location and X and Y dimensions of the measured defects for each mask blank. An acceptable alignment of a mask layout with a mask blank takes place when all of the defects land entirely within dispositional features or regions.

For these trials, the freedom to locate acceptable alignments was limited to shifting the mask layout pattern within a range of +/- 200 µm in X and Y, in each of four orientations: 0, 90, 180, 270 degrees. For each trial, a layout representing the dispositional area for a mask layout and a second layout containing the defect features for a mask blank were compared over the degrees of freedom. The seven mask layouts were tested against the 10 defective mask blanks for a total of 70 trials.

Synopsys' CATS mask data preparation tool was used to find the alignment within the acceptable range that matches the defect map to the disposition locations. A minimally acceptable match is detected wherever all defects are enclosed. In some cases, several minimally acceptable locations are found, from which the location that provides the largest enclosure margin can be identified. For proof of concept, when one or more acceptable alignments are found for a current orientation, no further orientations are tested.

The computations were executed in distributed mode, involving up to 64cpus, with a maximum runtime of 146 minutes. All design data was encoded in OASIS data files placed in an extended jobdeck.

3. Results and Observations

Table 1 summarizes the results of our 70 trials. For each trial 'NA' indicates that no alignment was found within the +/- 200µm range in X and Y in any of the four orientations. 0 indicates an alignment found on the first orientation, 90 indicates that an alignment was found on the second orientation but not in the preceding orientation, and so on.

The total number of defects on each blank is tabulated in row 2, the largest dimension of the biggest defect on row 3.

The last two rows show data for two early runs used to develop the methodology with designs larger than 22nm (and these rows of data are not included in our summary statistics).

Taken together, a defect avoidance strategy with these 10 mask blanks and the 7 mask layouts provides many alternative effective
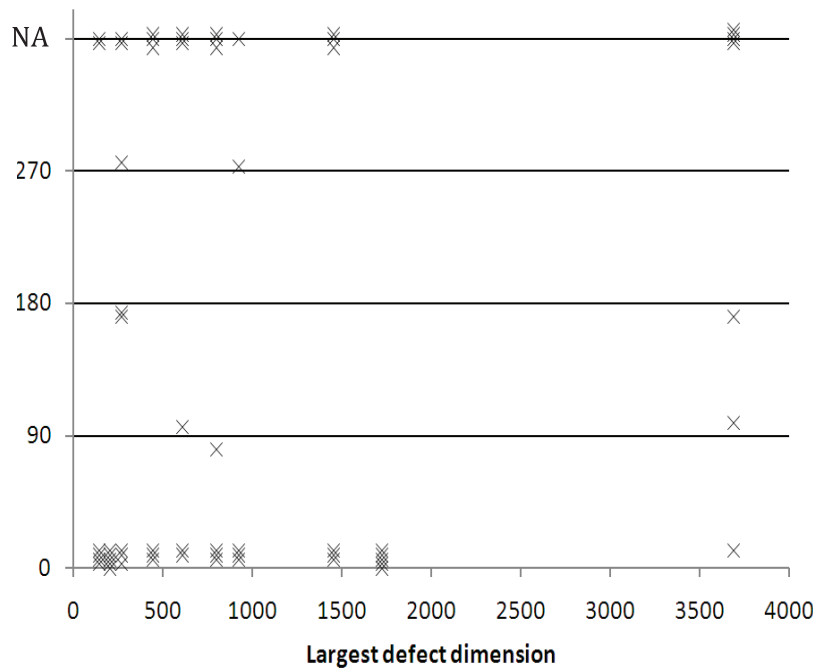
Figure 3. Alignment success vs. maximum defect size.

pairings among them—all these designs have at least 2 blanks on which they can be realized, and every blank is usable on 3 or more designs. Blank 8 was the hardest to deploy, where pairing with 4 layouts was not possible. Design C was the hardest to fit on a blank, where pairing with 8 blanks was not possible. If we randomly had just one of these mask blanks on hand, and tried to fit it to one layout picked at random, we would have had a 70% chance (49 successes out of 70 trials) of getting a usable combination. This suggests for a production environment, a reserve of some number of mask blanks must be kept on hand at all times to ensure high probability of pairing it to the next design in the door.

The +/- 200µm limit on translation degrees of freedom was chosen for experimental expediency. Wherever the mask layout is smaller than the available exposure field the translation range can be increased to position the layout anywhere within the exposure field, which will increase the probabilities of a successful alignment. To first order, if the probability, p, of finding a fit within a 400 x 400 range is, say 30%, for a particular defective mask blank and pattern, doubling the range in both axes to 800x800 quadruples the number of possible alignment locations thus increasing the probability to $1-(1-p)4$; thus in this example increasing the chance for successful alignment from 30% to 76%.

Increasing the dispositional area in the mask layout is another opportunity to further increase the probability for successful alignments to avoid defects. With real mask layouts the frame space between die placements could be declared "safe" for defects (depending on user requirements) and included in the dispositional area. Similarly, regions containing non-critical features, such as dummy fill patterns, could be added to the dispositional area, as well as additional areas declared by design to be immune to the presence of defects.

As seen in figure 3 there is some correlation between defect size and difficulty in finding an alignment. However this data suggests that some layout pattern types contain a sufficient number of large disposition areas in which to safely align a mask blank

with an enormous defect. A fit was not possible with Layout "C" on 80% of the mask blanks, but a suitable alignment was made with a blank containing a relatively large defect.

In some additional testing that was done with our customer on their actual designs, we were able to find solutions for most of the layers attempted. However, we found some difficulties in a dense polysilicon layer that included filler and dummy features. We believe that if the mask defects were allowed to fall within the filler feature regions (outside of absorber pattern) the prospects for finding a fit would improve, however, this experiment has not been done as of yet.

4. Conclusions and Future Directions

Allowing for the relatively small sample of mask blanks, and the fact that most of the mask layouts used in this study were concocted from designs for less advanced nodes by way of shrinking them, the prospect for using defect avoidance methodology to make use of defective masks looks promising. With current levels of mask defectivity, a mask shop must plan on maintaining a reserve of some number of mask blanks to maximize its chance of finding a blank to pair with each new design. With the data collected in this study the chance of finding a useful pairing with one blank is 70% (49/70). Based on this number the probability of getting an effective pairing with one of N mask blanks is $P = 1 – (0.3)N$. Thus to achieve a 99% probability of pairing to the next (unknown) design of any type we would need to have at least 4 mask blanks on hand. Recall that one design (C) could be paired with only 20% of the blanks. To insure 99% probability to fit this "worst case" design 21 mask blanks would be needed on hand (0.821 = 0.0092 = probability of not finding a fit). Risk is further mitigated by choosing the "worst mask" wherever possible—that is to use the mask with the most or largest defects as early as possible—thus leaving the better masks for the next (unknown) layout.

One factor that may lower the apparent effectiveness of this method is that current EUV mask and mask blank inspection tools

Table 1. Summary of defect avoidance trials.

	Blank 1	Blank 2	Blank 3	Blank 4	Blank 5	Blank 6	Blank 7	Blank 8	Blank 9	Blank 10
Total Defects	10	23	31	33	36	40	43	47	53	55
Largest Defect (nm)	206	1726	800	1456	926	446	610	3690	270	146
Design A	0°	0°	NA	NA	0°	NA	0°	0°	180°	0°
Design B	0°	0°	0°	0°	0°	0°	NA	NA	NA	NA
Design C	0°	0°	NA	NA	NA	NA	NA	NA	NA	NA
Design D	0°	0°	NA	NA	270°	NA	NA	NA	0°	0°
Design E	0°	0°	0°	0°	0°	0°	90°	NA	270°	0°
Design F	0°	0°	0°	0°	0°	0°	0°	90°	0°	0°
Design G	0°	0°	0°	0°	0°	0°	0°	0°	0°	0°
Pipecleaner 1	0°	0°	0°	0°	0°	0°	0°	0°	0°	0°
Pipecleaner 2	0°	0°	90°	0°	0°	0°	0°	180°	180°	0°

do not use AIMS-based inspection (with actinic illumination).[3] It may turn out that the actual number of critical defects is substantially larger than what is currently possible to detect[4] by indirect optical, SEM, and AFM methods, and the probabilities of pairing the blanks to designs may therefore go down.

To enable a practical defect avoidance method the mask blank inspection tools must be able to accurately locate defects on the blank. This means that the mask blanks must embody fiducial marks on which to reference defect locations. Similarly, mask writing tools must align the circuit layout with respect to these alignments marks. The accumulated alignment tolerance between the inspection tool and the mask writing tool must be accounted in defect avoidance, most likely by enlarging the effective area of the defects.

An obvious next step is to empirically validate the effectiveness of defect avoidance by fabricating an EUV mask and measuring the performance on printed silicon. Depending on actual results and the expected trend in defect reduction, design-driven methods to expand the defect dispositional area on each layout design may help improve the practical application of defect avoidance.

5. Acknowledgements

6. References

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Industry Briefs

■ As the year turns, let's take a look at what our 'experts' see in the Crystal Ball:

C. J. Muse, analyst, Barclays Capital gives predictions based on his several written eports from which these predictions have been derived:

Upturn coming "We see consensus moving from flat to closer to plus 5-10 per cent. Specifically, we see flash spending growing ~36 per cent year-over-year to $9.8 billion, logic spending up 4 per cent year-over-year to $11.6 billion, foundry spending up ~4 per cent to 13.9 billion, and DRAM spending down ~12 per cent to $10.7 billion."

2012 is going to be good '2012' (is) still early, but initial read is positive. We are hesitant to jump on the 'super cycle' bandwagon, but we clearly think it is reasonable to suggest that 2011 is not a peak year for capex, we suggest $31 billion WFE vs. prior peak of $36 billion. Here we point to technological advances driving increased capital intensity and emerging market demand enabling silicon content to continue to grind higher. And bigger picture, we view the macro backdrop as a positive factor heading into 2011 and beyond.

Gartner Inc. recently forecast 2011 expenditure on fab tools by major chipmakers to stay high despite a slight slip in the spending across semiconductor industry following vigorous investments in 2010.

With an estimated spending of US$9.2 billion, Samsung is forecast to be the No.1 tool investor in 2011, far leading the estimated US$5.7 billion and US$5 billion for Taiwan Semiconductor Manufacturing Co. (TSMC) and Intel, respectively.

GlobalFoundries is estimated to spend US$3.2 billion on tools in 2011, followed by Hynix Semiconductor`s US$2.7 billion, Micron Technology`s US$1.9 billion, Toshiba Semiconductor`s US$1.9 billion, United Microelectronics Corp.'s (UMC`s) 1.8 billion, Inotera Memories' US$1.6 billion and Sandisk`s US$1.4 billion.

Of the top 10 spenders, six are memory-chip makers, three are silicon foundries and only Intel is an integrated device manufacturer (IDM).

Gartner estimated global expenditures on fab tools will dip 5% worldwide, to a total US$51.1 billion in 2011, from 2010`s US$53.9 billion.

Year of NAND—NAND benefits from the fact that two vendors control ~75 % of the market, Samsung (40%) and Toshiba/Sandisk (33%). In 2011, Capex spending on NAND is likely to exceed capex spending on DRAM, for the 1st time.

Apple effect—the (growth of the) 2010 tablet market will have a lot to do with the supply/demand balance. AMAT said there would need to be a 200 kwspm wafer start fab to support expected demand. Apple's demand is expected to at least double YoY in 2011—most likely to triple, driven by the fact all the Macbooks are now SSD base

Samsung: Leader, follower. The move to 2x-nm—all the vendors are moving to various forms of 2x-nm: Samsung at 27-nm, Micron at 25-nm, Toshiba at 24-nm and Hynix at 26-nm. Samsung is no doubt a production and profitability leader, and is now able to make NAND chips at 3x-nm and 2x-nm nodes. It will be at the 27-nm node in 2011, bringing down costs by 35 % vs 3x-nm node. Samsung expects that 3x-nm & below will be at 80 % by the end of 2010.

Korean DRAM duopoly—unlike in NAND, a tier system does exist but there is a danger that it becomes a Korean duopoly. At present, only Samsung and Hynix are Tier 1 vendors with the most profitable technology. Micron, Nanya, Inotera (finances, technology slightly lagging) are probably Tier 2. Elpida, Powerchip, Rexchip (technology, money both lagging but attempting to make a grand leap forward) are Tier 3. Samsung also cornered the market on the ASML's NXT litho tools required to do 30-nm DRAMs due to overlay requirements. The WW DRAM bit grew ~ 50 % vs Samsung's growth of 70%.

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About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

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Calendar

2011

❈ **SPIE Advanced Lithography**

27 February-4 March
San Jose Marriott and
San Jose Convention Center
San Jose, California, USA
spie.org/al

Late submissions will be considered by conference chairs.

❈ **SPIE Photomask Technology**

19-22 September 2011
Monterey Marriott
and Monterey Conference Center
Monterey, California USA

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You are invited to submit events of interest for this calendar. Please send to lindad@spie.org; alternatively, email or fax to SPIE.

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