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Novel MRC algorithms using GPGPU

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Abstract

GPGPU (General Purpose Graphic Processor Unit) has been attracting many engineers and scientists who develop their own software for massive numerical computation. With hundreds of core-processors and tens of thousands of threads operating concurrently, GPGPU programs can run significantly fast if their software architecture is well optimized. The basic program model used in GPGPU is SIMD (Single Instruction Multiple Data stream), and one must adapt his programming model to SIMD. However, conditional branching is fundamentally not allowed in SIMD and this limitation is quite challenging to apply GPGPU to photomask related software such as MDP or MRC.

In this paper unique methods are proposed to utilize GPU for MRC operation. We explain novel algorithms of mask layout verification by GPGPU.

1. Introduction

Using GPU (Graphic Processor Unit) for general computation is referred to as GPGPU (General Purpose computing on GPU). Recently many studies have been reported that try to speedup the massive scientific calculation by GPGPU. Since the speed increase of GPUs has been overwhelming that of CPUs as shown in Fig.1,[1] more application

Continues on page 3.

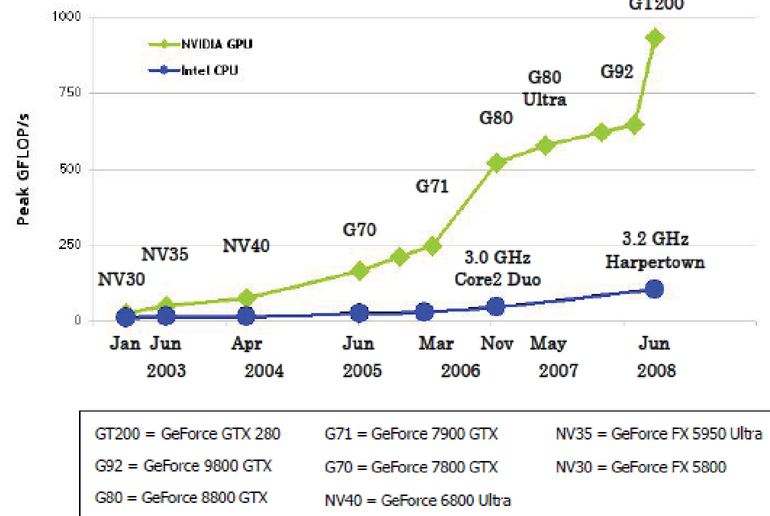

Figure 1. Peak GFLOP/s of CPU and GPU.

TAKE A LOOK INSIDE:

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Editorial

How Many Conferences Are Too Many For Photomask Making and is Adequate Value Being Delivered?

John Whittey, KLA-Tencor MIE Division

It seems as though every year the subject comes up whether we have too many conferences for the Photomask community. EMLC, BACUS, PMJ, SPIE Lithography mask session, and Sematech sponsored meetings on EUV/Lithography are the primary ones that keep popping up. My peers question the frequency of conferences, locations, timing, and support/sponsorship. It seems (at least according to some) that the various industry organizations, and even at times within a single organization, are working at cross purposes. The other topic that goes along with these discussions is the need for growth, how to make the conferences bigger. As I listen to the arguments go round and round, I question the validity and forces driving the discussions. It seems as though perspective is one of the driving factors of this discussion; whose viewpoint or organization is being defended.

My opinion is: "Let the market decide." Semicon is an event that is a good market driven example of value. In recent years a number of large semiconductor industry companies have drastically cut or withdrawn sponsorship and participation with Semicon. Many others have dramatically changed their approach to how they participate. Semicon is viewed by many companies now as a venue, not to introduce new products or find new customers, but rather as an event for targeting specific key customers with specific messaging. Semicon (in general) is not the same as it was twenty years ago, it has transformed from what it once was to cover a broader industry spectrum.

The purpose of the Semicon example is to show that when BACUS, EMLC, PMJ, SPIE Lithography's mask session, and Sematech events occur, and when they cease to provide value, people will no longer attend. Exhibitor's attendance at photomask events has been steadily falling (with the possible exception of PMJ) primarily due to the photomask industry maturing, and as a result of consolidation both from the mask shop side and equipment supplier side. Again, exhibitors recognize that the photomask venues are no longer a place to reach new customers, but rather a place to target messaging for specific customers. For many, the value in exhibiting is no longer worth resources required and hence, lack of participation.

I don't think there is a right or wrong answer here. I also don't believe growth should be the ultimate driver. The question that we should be asking is: "Is there enough value to the industry to warrant the efforts and resources being put forth to hold these specific conferences?" If not, then the choice facing the specific conference in question is either to adapt and/or transform to provide needed value or perish. Ultimately the market (through attendance and sponsorship) will decide if adequate value is being delivered.

"Let the market decide."

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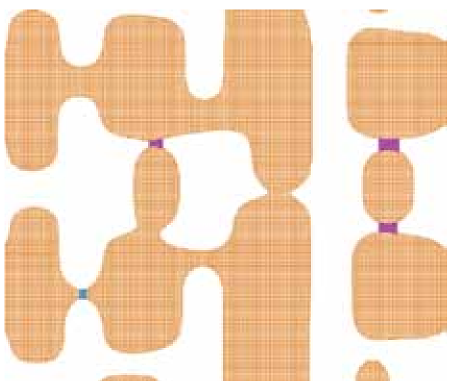


Figure 2. MRC errors by simulation based GPU method

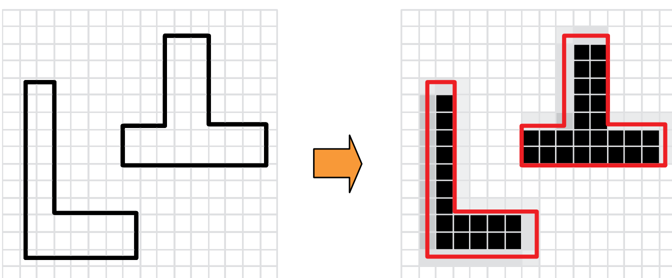


Figure 3. Gray pixel method.

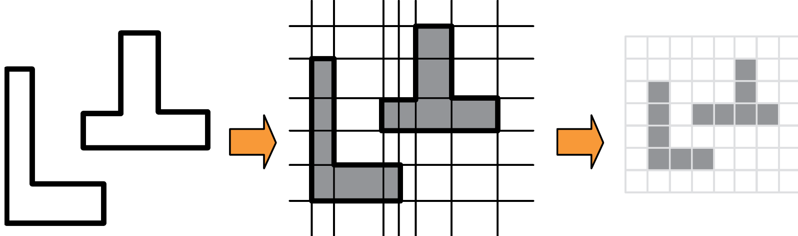


Figure 4. Normalized bitmap method.

of GPGPU is expected to solve massive computational problems.

Originally, GPU used to be used only for graphic processing and it was difficult to write efficient program codes to utilize the GPUs for general computation. However, CUDA, which is an excellent program development environment provided by Nvidia, has enabled easier access to the computational power of GPU. Thus, remarkable results have been achieved in the field such as numerical simulation.[2]

However, not many of significant commercial success has not been done in the photomask industry so far because of the difficulty to apply the programming model suitable for GPU architecture. Typically, program flows are controlled by conditional branching (if-else-then statements) and loop instructions, but they are virtually prohibited in GPGPU programming. Programs need to be described in SIMD (Single Instruction Multiple Data) model for GPGPU application. The concept of SIMD is quite opposite to many modern programming methods and all the fundamental algorithms have to be totally modified to meet the requirements of SIMD.

This paper tries to modify the basic MRC algorithm to SIMD-based one so that the computational ability of GPUs can be used for mask data processing.

2. Background

Increased complexity of mask data has brought explosion of mask data volume, which leads to the longer hours of mask data processing. On the other hand, the power consumption of computers has became one of the major issues because distributed cluster environment consisting of numerous Linux machines consumes greater electricity than ever as the number of Linux machines reaches up to hundreds.

AIST (Advanced Industrial Science and Technology) and SIINT (SII NanoTechnology) have been working on the joint development project for faster and 'greener' methods of mask data verification aiming at the computational lithography era. Since 2010, we have been developing and evaluating novel MRC algorithms to achieve faster calculation and lower power consumption. Fig.2 is an example of our presentation in the previous year,[3][4] which was generated by the simulation-based MRC algorithm on GPUs. In this case, 25x calculation performance and 17x power consumption reduction was achieved.

The basic method of the simulation-based MRC is as follows:

- First, electron beam energy accumulation and distribution is calculated by GPU
- Then, the energy intensity map is sent to CPU
- Contour images are generated in CPU and the spaces between contours are measured

The calculation of energy distribution is a time consuming job if processed in CPUs, but its process can be divided in parallel relatively easily. Therefore, the program can be described in SIMD model without great difficulties.

However, the target of this paper is more practical and the authentic MRC algorithms have to be rewritten to make it suitable for the SIMD concept. Breakthrough technologies are needed to describe MRC codes in SIMD form because MRC codes are full of if-then-else statements and loops that must not exist in SIMD.

3. Algorithm

3.1 Selection of basic algorithm

GPU was originally used as image processor and it should be still good at handling pixel records. Therefore, in this paper we try to convert the mask layout data to pixel records so that we can make the most use of processing power of GPUs. Two methods are available for pixel-based MRC, gray pixel method and normalized bitmap method.

[Gray pixel method]

As shown in Fig.3, in the gray pixel method, the uniform grids are set and all the pixels have values varying from 0 to 1.0. Pixels covered by patterns perfectly are expressed as 1.0, and pixels perfectly outside of the patterns are 0.0. This method is quite straightforward and simple, but accuracy needs to be sacrificed to some extent. If accuracy of 1nm level is needed, the grid must be set at 1nm, but the size of the intermediate pixel records will explode and it is not realistic.

[Normalized bitmap method]

Normalized bitmap method splits the layout with lines called slits. Slits are generated at each vertex of mask patterns and rectangular areas surrounded by slits are bitmap elements (See Fig.4). Since the elements are expressed as binary, no deterioration of accuracy will be observed.

Table 1. MRC rules.

Name of rule	Check target
Space check	Space between edges
Vertex distance check	Space between corners
Singular check	Detection of singularities
Notch check	Detection of small extrusions or intrusions
Dot check	Detection of small dots
Hole check	Detection of small holes
Jog check	Detection of small jogs
Step check	Detection of continuous jogs
Line-and-space rule check	Space between line heads inside of uniform line and space field

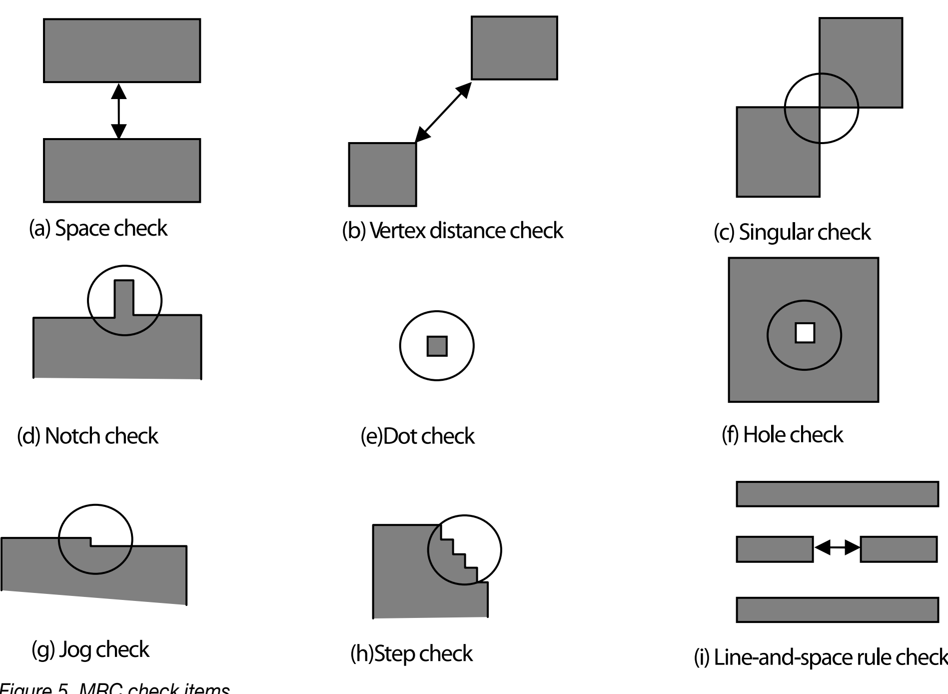


Figure 5. MRC check items.

As an intrinsic requirement of MRC, accuracy must not be sacrificed because all the mask data is expressed in integer. Therefore, we have decided to choose the normalized bitmap method as a basic algorithm of GPU based MRC.

3.2 MRC rules

Fig.5 illustrates the typical MRC rules that are used practically.

3.3 Definitions

In this paper, templates are used to search for the target patterns from the whole layout. Definition of the templates is expressed as follows:

Problem size = (X , Y) : X and Y are pixel count of the templates in horizontal and vertical direction, respectively.

H (N) : Width of the Nth pixel in the template

W (N) : Height of the Nth pixel in the template

Fig.6 is a example of the definition of the template with the problem size of (3,2).

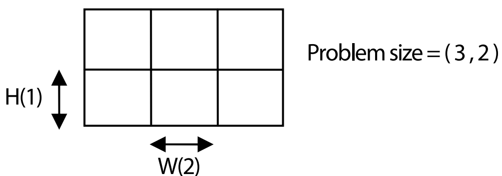


Figure 6. Definition of the template.

3.4 Algorithms

Algorithm for each rule check defined in section 3.2 is shown in the following:

[Space check]

Problem size = (3 , 1)

Searches for the bit array (101) from the layout, and detects the places where W(2) is smaller than the specified value.

There are derivatives of directions.

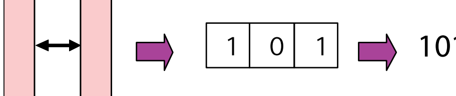


Figure 7. Space check.

[Vertex distance check]

Problem size = (3 , 3)

Searches for the bit array (100000001) from the layout, and detects the places where $\sqrt{W(2)^2 + H(2)^2}$ is smaller than the specified value.

There are derivatives of directions.

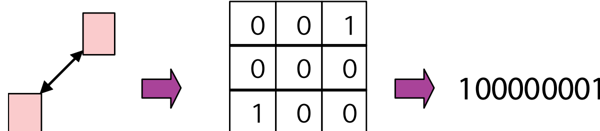


Figure 8. Vertex distance check.

[Singular check]

Problem size = (2 , 2)

Searches for the bit array (1001) or (0110) from the layout.

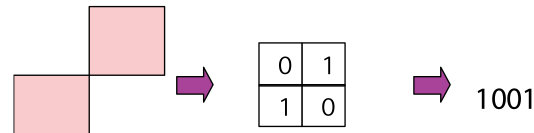


Figure 9. Singular check.

[Notch check]

Problem size = (3 , 3)

Searches for the bit array (111010000) from the layout, and detects the places where W(2) and H(2) are smaller than the specified values.

There are derivatives of directions and intrusions/extrusions

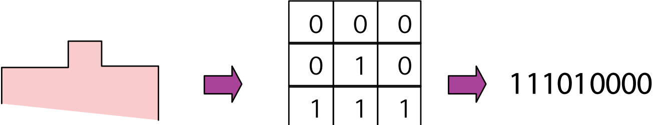


Figure 10. Notch check.

[Dot check]

Problem size = (3 , 3)

Searches for the bit array (000010000) from the layout, and detects the places where W(2) and H(2) are smaller than the specified values.

There are derivatives of holes and dots.

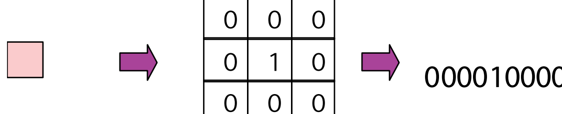


Figure 11. Dot check.

[Jog check]

Problem size = (2, 3)

Searches for the bit array (111000) from the layout, and detects the places where H(2) is smaller than the specified value.

There are derivatives of directions.

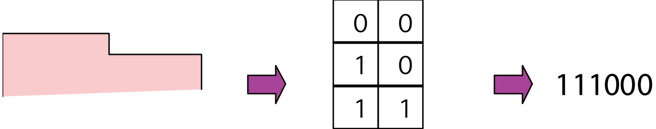


Figure 12. Jog check.

[Step check]

Problem size = (4, 4)

Searches for the bit array (111011001000000) from the layout, and detects the places where H(1), H(2), H(3) and W(2),

W(3) are smaller than the specified values.

There are derivatives of directions and number of the steps.

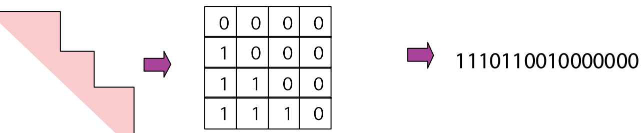


Figure 13. Step check.

[Line-and-space rule check]

Problem size = (3, 5)

Searches for the bit array (111000101000111) from the layout, and detects the places where W(3) is smaller than the specified value.

There are derivatives of directions.

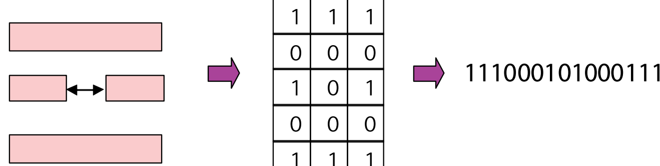


Figure 14. Line-and-Space check.

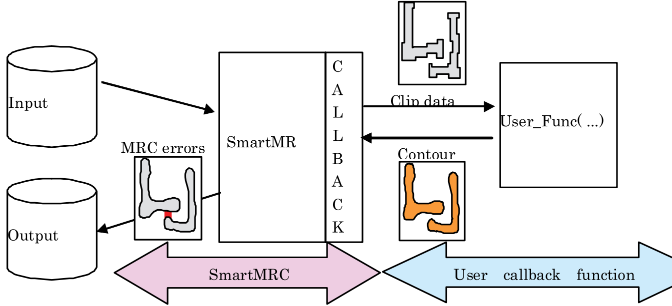


Figure 15. API function of SmartMRC.

4. Program Architecture

4.1 SmartMRC API

We use the API (Application Program Interface) function of SmartMRC as the fundamental framework of the software development and evaluation. SmartMRC is a commercial MRC software product provided by SII NanoTechology Inc. By using the API function of SmartMRC, programmers can access to the mask layout data easily without knowing the details of the mask data format. As shown in Fig.15, SmartMRC reads in the input file, clip the small area and send it to the function defined by the user called User_Func( ). The user defined function receives the clipped data, processes the data and sends the result back to SmartMRC if necessary.

As illustrated Fig.16, the API function of SmartMRC can utilize the distributed or parallel processing to boost the calculation performance. In this case, 8 slaves use each core in parallel and GPU can be used from each slave equally.

4.2 Program Architecture

Fig.17 illustrates the basic program architecture of the software developed in this paper.

(1) Callback function

The callback function is an entry point from SmartMRC API. This function is called per each sub-mesh and clipped pattern data is sent to this function. Programmers develop the software under this parent function.

(2) Bitmap management

The bitmap management function generates the bitmap from the input layout and sends it to GPU. Since the data transfer speed between CPU and GPU is the most crucial part, the greatest care must be paid to optimize this part.

(3) MRC engine

The MRC engine runs MRC operation using GPU. The main role of GPU is a template search by bit pattern matching and CPU judges the results returned from GPU one by one.

(4) Input/output control

When errors are detected, polygons to show the error flags need to be generated.

(5) Parameter / rule recognition

Information about parameters or rules given by the user has to be conveyed to the API programs. User_Func( ) accesses this kind of information by reading a configuration file specified by API.

4.3 GPU interface

In the programming with GPU devices of Nvidia, the CPUs are manipulated by the controlling structure called CUDA. The program codes that run on GPU are described in the interface routines named kernel functions and they are called through the CUDA runtime library (libcurart.so). Generally, GPU program codes consist of the codes that run on CPU and those that run on GPU, and each part is translated into object code by “nvcc” complier.

CUDA library files have to be linked as share-object in order to use SmartMRC API. Therefore, as implementation of the MRC software we link the CUDA codes as share-object to the main body of the program. This can be possible by adding the parameter “-shared –Xcompiler -fPIC” to the nvcc command. In addition, CUDA runtime library “libcudart.so.2” is needed when the programs run.

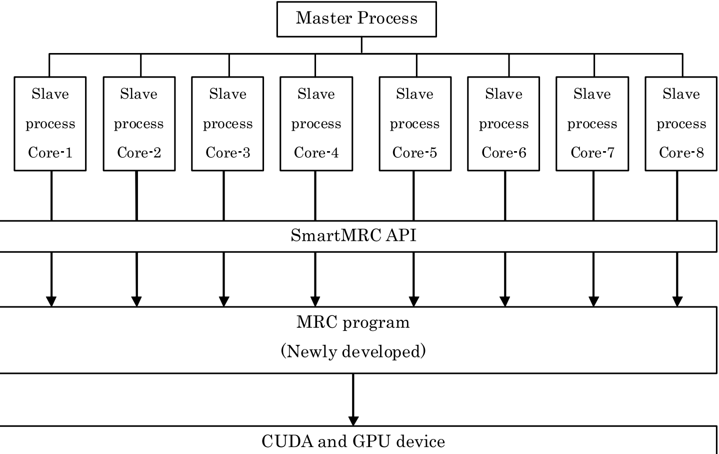


Figure 16. Parallel processing by SmartMRC.

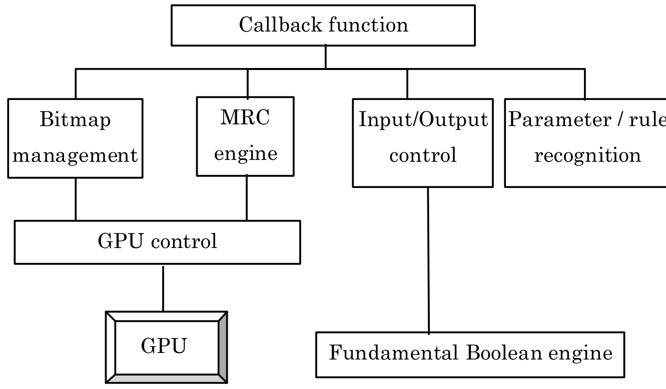


Figure 17. Program architecture.

5. Experimental results

5.1 Environment

The environment used for the evaluation proposed in this paper is as follows:

Table 2 shows the details of GPU used in the evaluation. This information can be retrieved by deviceQuery command.

CPU : Intel® Xeon® CPU E5607 @ 2.27GHz
2CPU × 4 Cores
GPU : Tesla C2050 / C2070
14 Multiprocessors × 32 CUDA Cores / MP= 448 CUDA Cores
Global-memory : 2,817,982,464 bytes
GPU Clock-speed : 1.15GHz
Constant-memory : 65,536 bytes
Shared-memory per block : 49,152 bytes
Register count per block : 32,768
INPUT
File type : OASIS (gzipped)
Volume : 403,885,772 byte
: 708,433,466 byte (After gunzip)
Zone : 5.8 mm x 5.8 mm

Table 2. Result of deviceQuery command.

Device 0: "Tesla C2050 / C2070"	
CUDA Driver Version / Runtime Version	4.0 / 4.0
CUDA Capability Major/Minor version number:	2.0
Total amount of global memory:	2687 MBytes (2817982464 bytes)
(14) Multiprocessors x (32) CUDA Cores/MP:	448 CUDA Cores
GPU Clock Speed:	1.15 GHz
Memory Clock rate:	1500.00 Mhz
Memory Bus Width:	384-bit
L2 Cache Size:	786432 bytes
Max Texture Dimension Size (x,y,z)	1D=(65536), 2D=(65536,65535), 3D=(2048,2048,2048)
Max Layered Texture Size (dim) x layers	1D=(16384) x 2048, 2D=(16384,16384) x 2048
Total amount of constant memory:	65536 bytes
Total amount of shared memory per block:	49152 bytes
Total number of registers available per block:	32768
Warp size:	32
Maximum number of threads per block:	1024
Maximum sizes of each dimension of a block:	1024 x 1024 x 64
Maximum sizes of each dimension of a grid:	65535 x 65535 x 65535
Maximum memory pitch:	2147483647 bytes
Texture alignment:	512 bytes

Table 3. Performance comparison of CPU-based and GPU-based method.

Method	CPU-based	GPU-based	improvement ratio
Dot check	607 s	94 s	X 6.5
Space check	491 s	100 s	X 4.9
Singular check	742 s	92 s	X 8.1

5.2 Experimental result

Table 3 shows the results of the performance comparison between GPU-based and CPU-base method. It has been proven that the GPU-based method proposed in this paper is 5 to 8 times faster than the conventional CPU-based method. Regarding the power consumption, approximately 40 percent of reduction was observed in total. Fig.18 shows the examples of the detected errors by space check and hole check.

5.3 Considerations

It has been proven that the GPU-based MRC method works approximately 5 to 8 times faster than the conventional CPU-based method from the evaluation results. However, we have to overcome the two challenges in order to user this method for real complicated mask data: existence of slant angle edges and generation of redundant slits by complicated layout.

[Existence of slant angle edges]

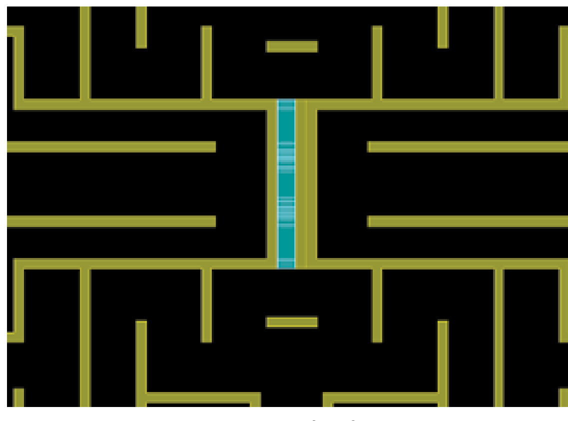
The bitmap expression can describe Manhattan layout without losing the accuracy, but it always has to sacrifice the accuracy to describe slant edges. It is required to use higher resolution to describe slant shapes more accurately, but it leads to the explosion of bitmap volume. In addition, approximated bitmap can harm the performance of the pattern search operation by GPU, and space check in slant direction is very difficult in this method. Although such kinds of any angled shapes are not common in LSI mask layout, we need to overcome this issue.

[Generation of redundant slits by complicated mask layout]

In the evaluation of this paper, relatively simple layout has been used, but in the actual mask there are numerous complex shapes as the output of RET operation. Especially, the employment of holistic computational lithography has generated very complicated patterns such as SRAFs. In this method, the input of significantly complex layout can cause unnecessarily redundant slits in the bitmap. This phenomenon can affect the calculation speed, but optimization of sub-mesh size may relax the deterioration of performance.

6. Conclusion

AIST and SIINT have been working on the project to develop the GPU technologies for faster and greener MRC to meet the verification requirements of aggressive computational lithography. In this paper, we have made a new proposal of MRC algorithm that uses GPU by layout bitmap generation. Through the evaluation we have proven that this method can work efficiently and x times faster than the conventional CPU method. We have also brought up two measure difficulties to apply the proposed method to real mask data processing and suggested possible solutions.



(a) Space check

(b) Hole check

Figure 18. Detected errors.

We will continuously try to utilize the promising computation device, GPU, for further seek of faster and greener methods to solve the problem related to computational lithography.

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Industry Briefs

ASML Brion Rolls Mask Optimization Tool

by **EETimes**

ASML Brion has introduced the Tachyon Flexible Mask Optimization (Tachyon FMO) tool to enable seamless use of multiple optical proximity correction (OPC) techniques in a single mask tapeout and to allow advanced and computationally intensive OPC in those local areas where they can be most beneficial. The use of different OPC techniques tailored to localized imaging challenges can reduce the tapeout cycle time to just one-third the time of alternative technologies, while maintaining the desired level of imaging performance. Brion has also developed a solution that detects and manipulates hotspots and can cleanly reinsert the corrected hotspots into the full chip design without introducing new defects due to the proximity effects of neighboring patterns. STMicroelectronics (ST) has been evaluating Tachyon FMO for its 2x nm node development, focusing on the hotspot repair application. ST has demonstrated dramatic reductions in defects in the contact layer by using Tachyon MB-SRAF along with Tachyon FMO, while ensuring that no new defects were introduced by the repair method itself.

Gudeng Precision Designs EUVL Pod with VICTREX for Low Contamination

by **Solid-State Technology**

To maintain a contamination-free environment, Gudeng has designed a new EUV dual-pod with the inner pod made from metal and the outer pod made with VICTREX PEEK-ESD 101. VICTREX PEEK-ESD 101, for all of the photomask contact components and the housings, is a good EUV pod base material because of its high surface hardness, low particle generation, high purity, and tight ESD tolerance. Contamination levels can be effectively reduced and the resistance to wear significantly increased compared to materials currently in use.

EVG620HBL Mask Alignment System

by **Photonics**

EV Group (EVG) has announced the EVG620HBL Gen II, the second generation fully automated mask alignment system for volume manufacturing of extremely bright light-emitting diodes (HB-LEDs). Introduced one year after the launch of the first-generation EVG620HBL, the Gen II is tailored to address HB-LED customer-specific needs and the ongoing demand to reduce the total cost of ownership. EVG has also signed a joint development and licensing agreement with lithography company Eulitha AG, integrating Eulitha's PHABLE mask-based UV photolithography technology with EVG's automated mask aligner product platform. Combining Eulitha's full-field exposure technology with EVG's mask alignment platform reportedly allows cost-effective, automated fabrication of photonic nanostructures over large areas and supports the production of energy efficient LEDs, as well as solar cells and liquid crystal displays (LCDs).

IBM Technology for 14nm FinFETs

by **Semiconductor Manufacturing and Design**

IBM and its Common Platform alliance partners, GLOBALFOUNDRIES and Samsung, hope that commercially feasible EUV lithography will be available some time during the 14 nm node, if not at the beginning. The Common Platform companies are hoping many of the challenges in commercializing EUVL will be overcome through its various research links, including those with the EUV Center of Excellence now under construction in Albany, New York.

Join the premier professional organization for mask makers and mask users!

About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

Individual Membership Benefits include:

- Subscription to BACUS News (monthly)
- Complimentary Subscription *Semiconductor International* magazine
- Eligibility to hold office on BACUS Steering Committee

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Corporate Membership Benefits include:

- Three Voting Members in the SPIE General Membership
- Subscription to BACUS News (monthly)
- One online SPIE Journal Subscription
- Listed as a Corporate Member in the BACUS Monthly Newsletter

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Calendar

2012

SPIE Photomask Technology

11-13 September 2012
Monterey Marriott and
Monterey Conference Center
Monterey, California, USA
spie.org/pm

Late abstract submissions may be considered by the Chairs. Please send to Pat Wight at patw@spie.org.

2013

SPIE Advanced Lithography

24-28 February 2013
San Jose Convention Center and
San Jose Marriott
San Jose, California, USA
spie.org/al

SPIE is the international society for optics and photonics, a not-for-profit organization founded in 1955 to advance light-based technologies. The Society serves nearly 225,000 constituents from approximately 150 countries, offering conferences, continuing education, books, journals, and a digital library in support of interdisciplinary information exchange, professional growth, and patent precedent. SPIE provided over $2.5 million in support of education and outreach programs in 2011.

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You are invited to submit events of interest for this calendar. Please send to lindad@spie.org; alternatively, email or fax to SPIE.