PHOTOMASK

BACUS—The international technical group of SPIE dedicated to the advancement of photomask technology.

SPIE Photomask Technology + EUV Lithography
2nd Place Winner - Zeiss Award for Talent in the Industry

iN5 EUV Single Expose Patterning Evaluation for Via Layers

Argho Das, IMEC, Kapeldreef 75, 3001 Leuven, Belgium; Hochschule Furtwangen University (HFU), Robert-Gerwig-Platz 1, 78120 Furtwangen, Germany

Victor Blanco, Sayantan Das, Sandip Halder, and Mircea Dusa, IMEC, Kapeldreef 75, 3001 Leuven, Belgium

Nicola Kissoon, ASML Technology Development Center, Kapeldreef 75, 3001 Leuven, Belgium

ABSTRACT

The continuous need to shrink dimensions using EUV lithography has posed challenges and opportunities for patterning materials and processes. Scaling BEOL interconnect structured is a key element to performance improvement of functional devices. In this paper, we investigate the impact of various factors on the patterning of EUV single exposure vias, to find effective strategies to shrink critical dimension (CD) with improved critical dimension uniformity (CDU), local critical dimension uniformity (LCDU) and decrease in defectivity. This work is based on patterning a system on chip (SoC) random logic via layer at minimum horizontal interconnect wire pitch of 28nm, which is the limit of single exposure interconnect with 0.33 NA EUV tools. This design uses aggressive CPP/Mx gear ratio of 3/2 which is equivalent to 38nm to 34nm pitch orthogonal via arrays, thus, examining the impact of the primary patterning parameter and illumination source co-optimized with OPC treatment of rectangular vias. The via patterns are transferred to bottom dielectrics to study the evolution of LCDU and defectivity through etch.

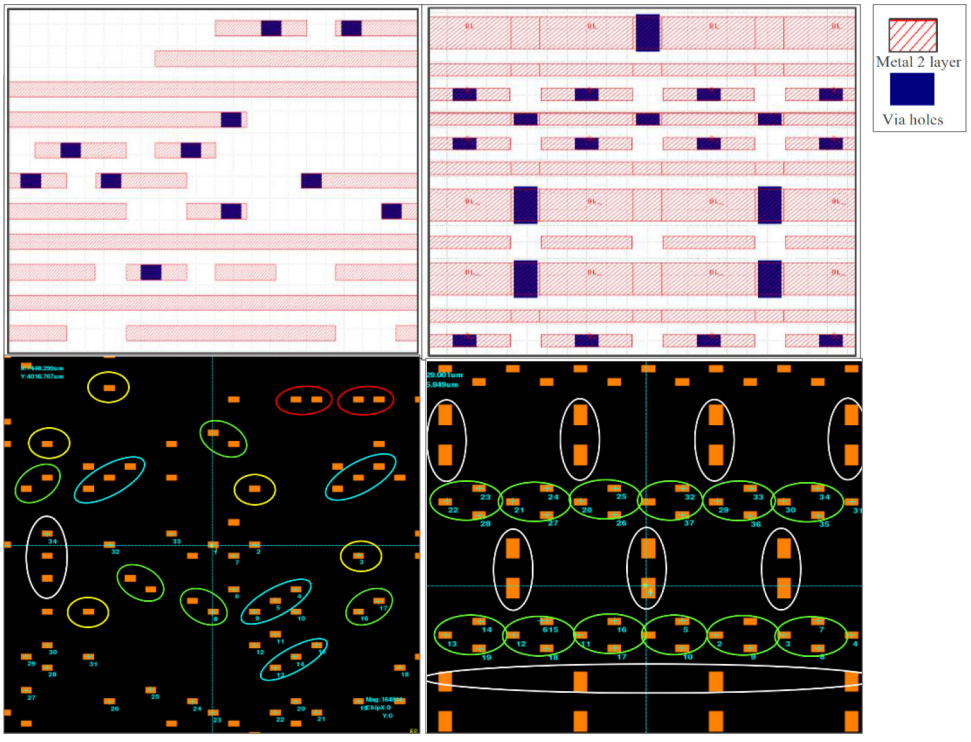


Figure 1. Random logic structures (left) and SRAM memory structures (right) – via & metal layers.

BACUS NEWS

FEBRUARY 2022
VOLUME 38, ISSUE 2

TAKE A LOOK INSIDE:

SPIE.

11854-23

EDITORIAL

Looking forward, full steam ahead

Romain Lallement, IBM

When I joined the semiconductor industry more than a decade ago as lithography process engineer, my day-to-day job was elusive to my family beyond the final goal of chip making. It will not come as a surprise to anyone if I say it is still the case, but they are now aware of how prevalent our work is to society. For a long time, semiconductor devices were quietly being introduced to our pockets, homes, cars, warehouses until suddenly there were not enough of them. One of the ripple effects of the pandemic is an increased thirst for computing, automation, and data to make us ever more interconnected. What makes me hopeful and even excited is the amount of innovation that we see across our ecosystem to fill the gap and go beyond.

Gate All Around (GAA) technology has been embraced by integrated device manufacturers (IDM) and foundries. The transition from FinFET to NanoSheet will continue to push device scaling and improve power consumption for the next nodes.

Artificial Intelligence (AI) is moving down the stack from pure software application to dedicated hardware. Novel architectures and materials in memory computing will significantly advance model training and inference. Bringing memory closer to the processor core will alleviate the Von Neumann bottleneck, speeding up computing and the overall chip power consumption.

Quantum computing is being pursued by large companies and start-ups alike. It has the potential to shift the paradigm, making prohibitive computing problems of the past within the realm of possibility today.

What does this all mean for the mask industry? I believe none of the technologies listed above will replace the other. They will coexist and complement each other to create systems that are far more powerful than the individual units. In other words, the overall integrated circuit (IC) portfolio will grow in volume and variety. Mask making is already adapting to it. The first straightforward evolution is the increased capacity. Aging tool replacement will hopefully offer efficiency benefits. The leading edge is not shy of innovations either. The EUV community is on the lookout for what comes after the Ta-based mask stack and exploring EUV phase shifting masks. The MultiBeam writer improves the raw performance metric and opens the door for curvilinear design, leading to open discussions on design file format.

It is indeed an exciting time as every aspect of the mask community is evolving and enabling the next revolutions in compute. The renewed interest is the icing on the cake to attract more talent.

BACUS

N • E • W • S

BACUS News is published monthly by SPIE for *BACUS*, the international technical group of SPIE dedicated to the advancement of photomask technology.

Managing Editor/Graphics Linda DeLano
SPIE Sales Representative, Exhibitions, and Sponsorships Melissa Valum
BACUS Technical Group Manager Tim Lamkins

SPIE.

P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 360 676 3290
Fax: +1 360 647 1445
SPIE.org
help@spie.org

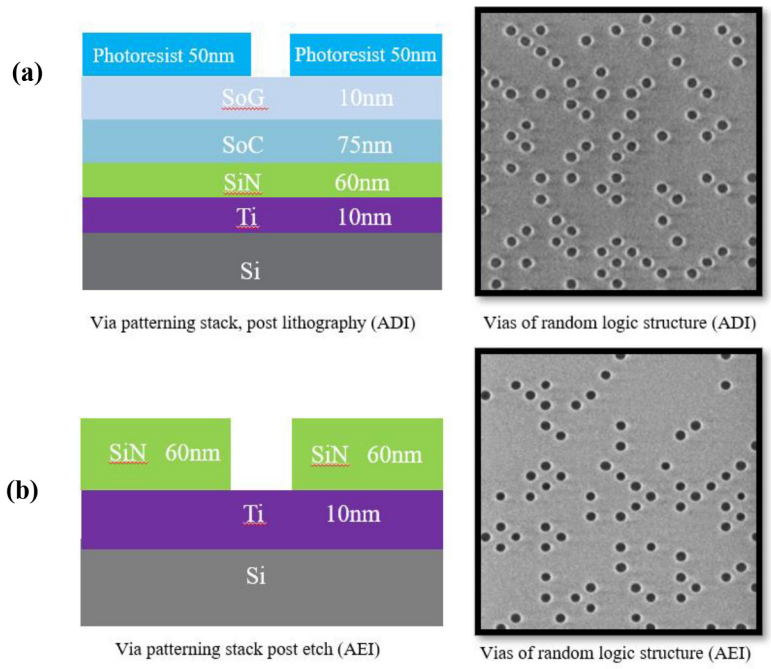


Figure 2. (a) Via patterning stack after lithography and vias of random logic structure-ADI (b) Via patterning stack after SiN etch and vias of random logic structure-AEI.

1. Introduction

The limits of EUV single exposure, for such aggressive design rules to print non-arrayed randomly distributed via holes, poses a patterning challenge due to the stochastic effects present in EUV imaging combined with small vias CDs. In this work, the patterning transfer of via holes in SRAM and random logic structures post lithography were evaluated from an ARM clip with metal 2 pitches ranging from 24 nm to 30 nm. The isolated vias instances which have been highlighted in yellow in Fig.1, is 5 times in Field of View (FoV); the vertical cluster of vias at 2 times of the minimum pitch which has been highlighted in white, is 1 time in FoV; the diagonal clusters at minimum design, center-to-center has been highlighted in blue and is 4 times in the FoV; the horizontal doublets as highlighted in red is 2 times in FoV; the diagonal doublets as highlighted in green is 5 times in FoV; large rectangular vertical holes as highlighted in white is 11 times in the FoV; triangular triplets as highlighted in green is 12 times in FoV as shown in Figure (1). An optimal and advanced chemically amplified resist (CAR) and patterning stack was selected and etch optimization was performed on TEL etch tool to shrink after development inspection (ADI) CD to final design CD. Figure 2(a) illustrates the stack details post EUV lithography exposure. A continuous titanium layer at the bottom of the stack is used to enable voltage contrast (VC) metrology and defectivity investigation post etch. The printing and pattern transfer capabilities at ADI and after etch inspection (AEI) were investigated. Initial process window and CD evaluation was done using Hitachi critical dimension scanning electron microscope and contouring methods.

Patterned mask used with a reduction ratio of 4:1. In the reduction of structure sizes, single patterning in place of multi patterning has been used. Figure 2(b) illustrates the stack details post etch and illustrates the printing of the random logic via holes on silicon nitride hard mask. The minimum center-to-center dimension of the random logic structures was around 48 nm and around 50 nm in SRAM structures. The current focus is on further shrinkage of critical dimensions to meet the design CD target of less than 20 nm.

2. Experimental

EUV lithography was first used in high volume production at the 7 nm node. Its application includes contact and via layers; and due to dense pattern density characteristics of single-exposure EUV imaging, defectivity probability increases. Dimensional & defect inspection metrology (via failures), massive data collection, statistical analysis with CDSEM and e-beam data post lithography and etch has been done. Figure (3) illustrates random Logic place and route and SRAM via holes respectively that have been designed for patterning the SoC device layers.

2.1 EUV Exposure

The exposure process was carried out on a ASML NXE3400 full field EUV scanner in the 300 mm cleanroom with an illumination that has been customized and by a mask vehicle with optical proximity corrections (OPC). OPC was applied on the via structures, but no bias was applied. When aligning the wafers, phase grating alignment has been used to detect targets. An UV-based level sensor contributed towards reducing the wafer film stack variation to the process-dependent height variations. Patterning with a CAR photoresist was done using the nitride stack as described in figure (2), focusing mainly on pitch 28 nm with further exploration of pitches 30 nm, 26 nm, and 24 nm. The resist was coated on stacked wafers with an underlayer of spin-on-glass (SOG) thickness of 10 nm.

2.2 Photoresist Screening

The first Focus Energy Matrix (FEM) wafers had been exposed to ascertain the best dose-focus conditions for future wafers exposure. Optimum process windows were generated along with graphs for Bossung curve and observe the quality of printing of the vias at certain dose, focus and CD conditions. Resist screening was done based on the process window analysis at an optimum dose to size and we were already able to capture a process window for our target pitch of 28 nm with the desired photoresist based on the current FEM-lithography conditions. In figure (4), a process window overlap (in black region) was generated between the process windows of pitches 26nm (in orange), 28nm (in blue), 30 nm (in green) to check for the optimum dose and focus conditions that were necessary for printing on the wafers across all the aforesaid pitches for Logic and SRAM structures. A process window overlap along with pitch 24 nm (in yellow) was not derived because at a lower pitch, a higher dose to size ratio is being necessary for good printing whereas for the remaining pitches, optimum dose-focus conditions could be already determined for exposure. A stack comprising of silicon nitride was selected for lithography and etch processes' development.

2.3 Methodology

In this work, back-end-of-line processes involving metal and via layers

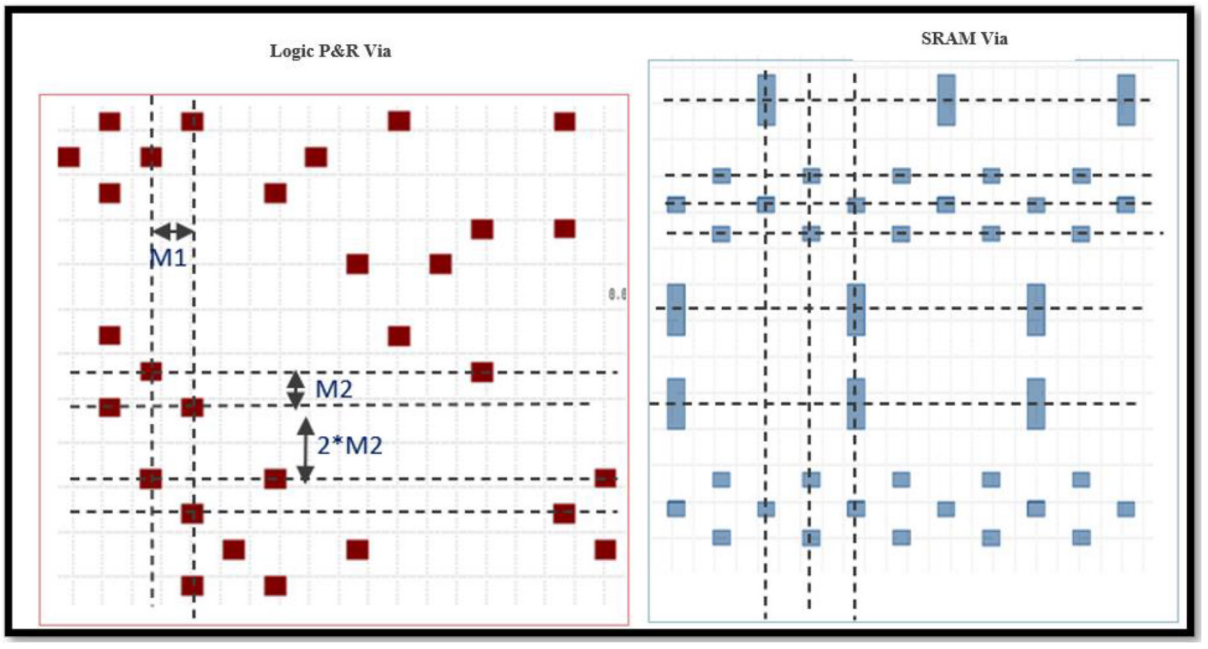


Figure 3. Random Logic Place & Route (P&R) Via structures, SRAM via structures, Metal 1 (M1) and Metal 2 (M2) layers.

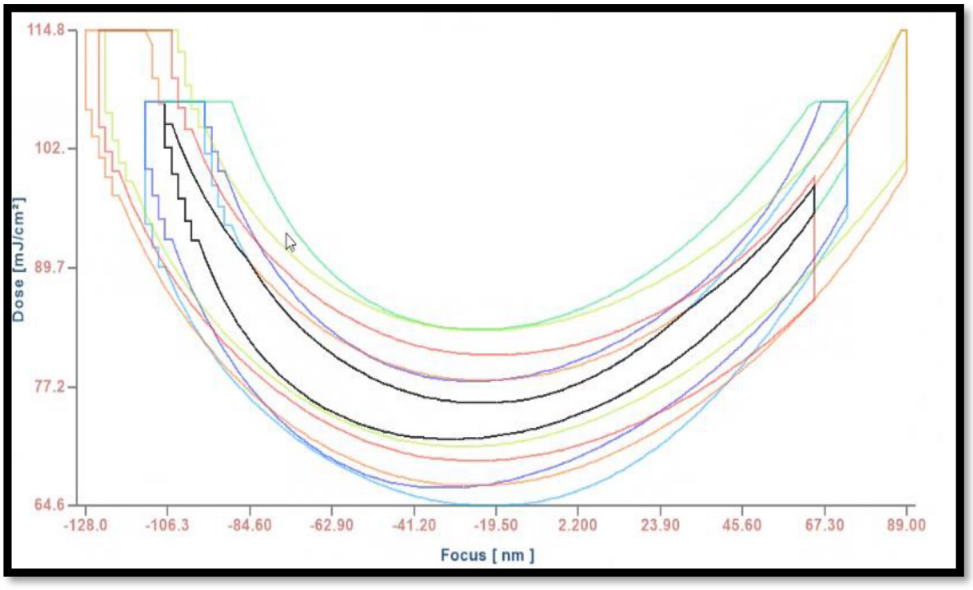


Figure 4. Process windows overlap for determining optimum dose-focus conditions for SRAM and Logic structures.

were evaluated to assess 0.33 NA EUV single patterning limits. Wafer maps were generated to analyze the die-to-die fingerprints to understand the characteristics of printing such as local CD uniformity and CD uniformity on the dies post-lithography (ADI) and additionally, a center-to-edge fingerprint in case of after etch inspection (AEI) enabling viable observations for both Logic and SRAM structures on pitch 28 nm as shown in Figure (5).

Small and slot vias in SRAM structures show center to edge fingerprint post-etch CDSEM inspection and random logic vias post-etch CDSEM inspection also show considerable fingerprint. Through several etch design of experiment (DoE), large statistical data were collected from CDSEM inspection initially focusing on all pitches but concluding with our major focus on Pitch 28 nm module. Furthermore, e-beam inspection was done with eP5, large FoV SEM tool for large statistical data collection.

3. Results and Discussions

3.1 Etch DoE & Critical Dimension Scanning Electron Microscopy

The critical dimension is one the most critical variable in lithography which is the minimum distance measured within the boundaries of a via edges. The CD defines the width or height of a via, depending on the

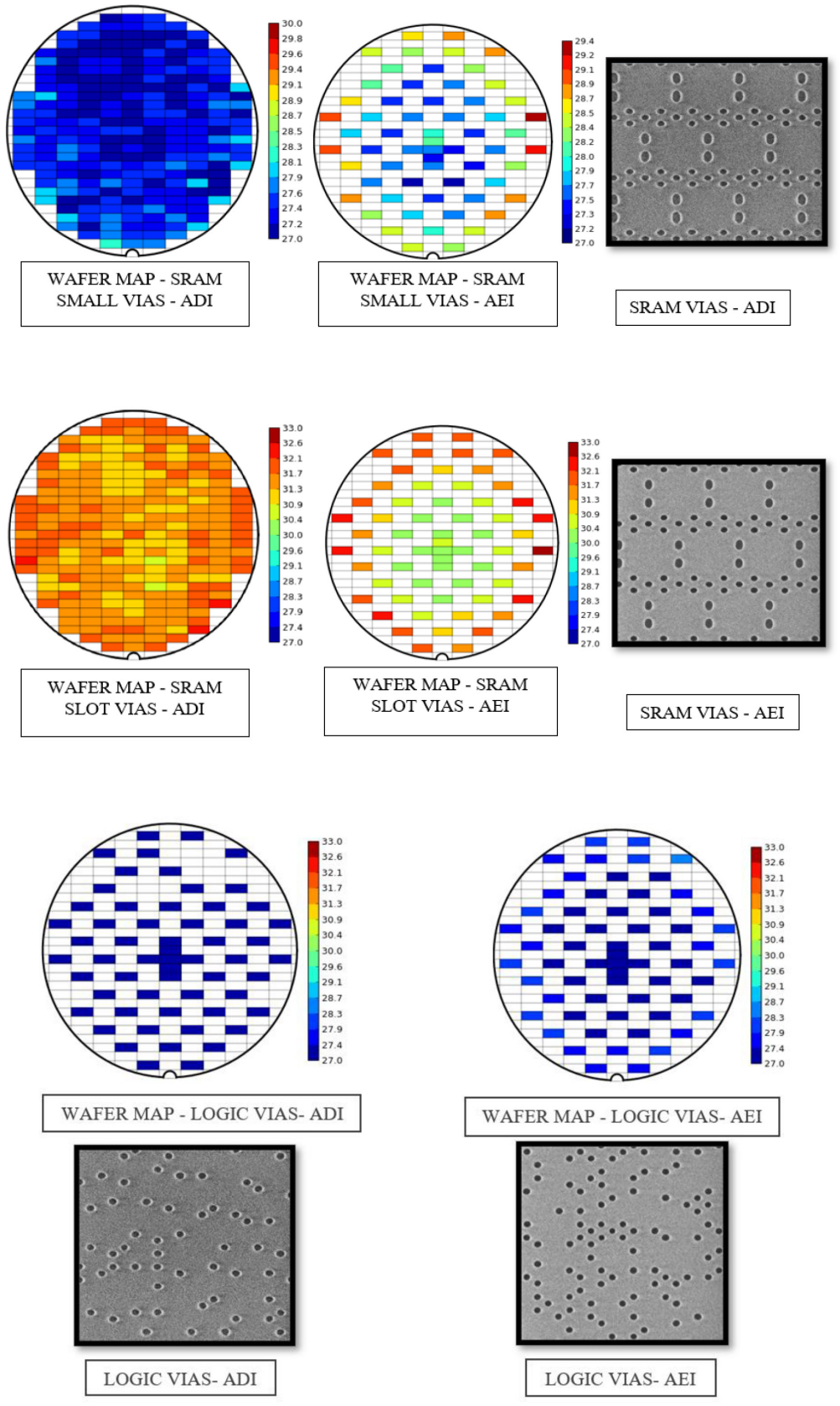


Figure 5. Post lithography (ADI) and post etch (AEI) wafer maps and via printings for SRAM and Logic structures at pitch 28 nm.

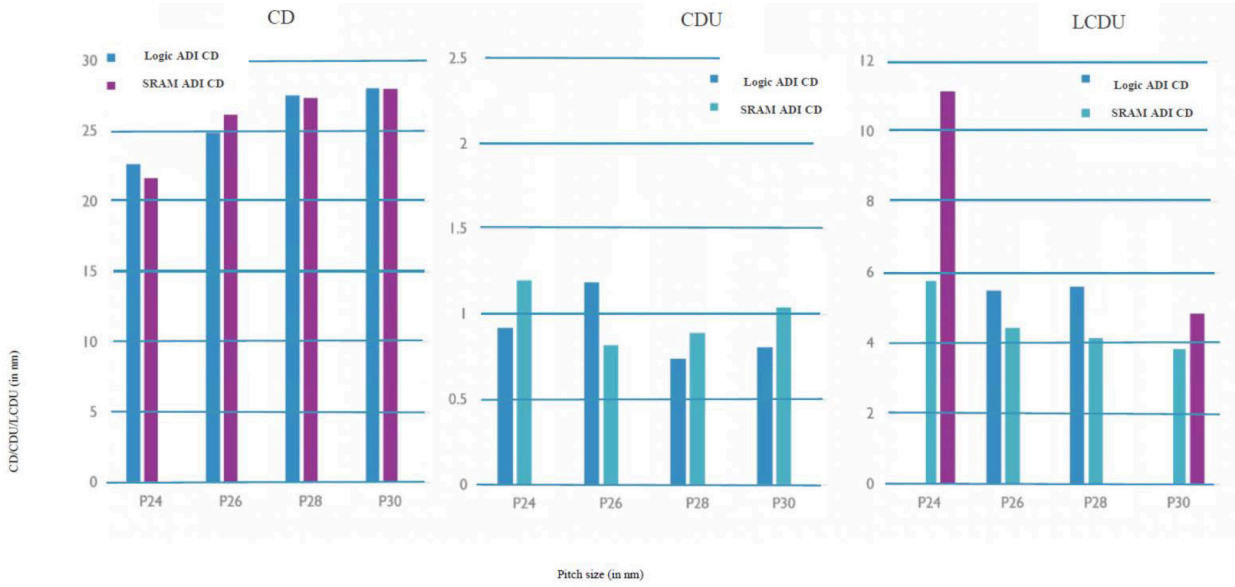


Figure 6. Post lithography (ADI) CD, CDU, LCDU trend for SRAM and Logic structures through pitches.

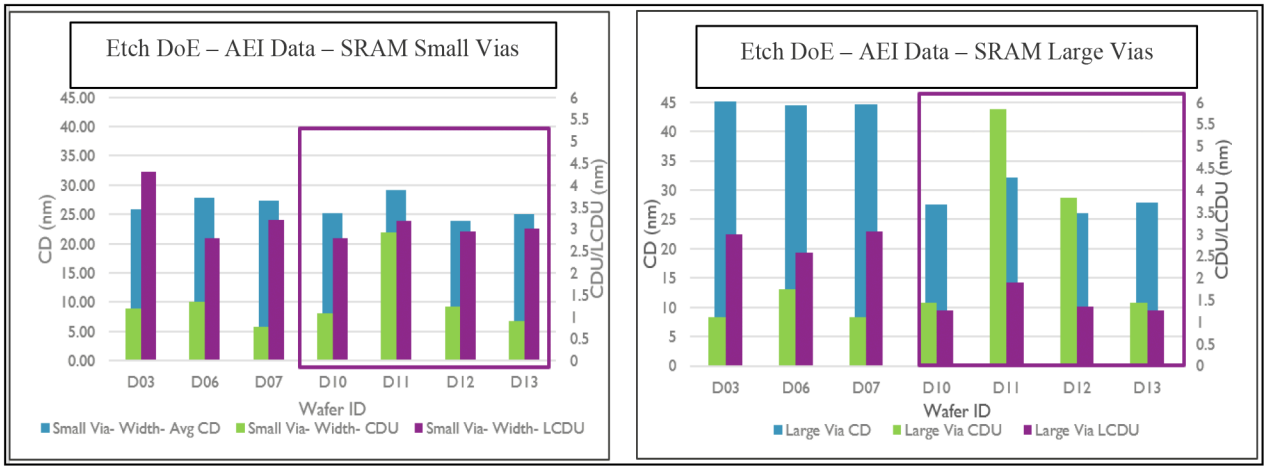


Figure 7. Post etch DoE (AEI) CD, CDU, LCDU trend for SRAM small and slot vias studied separately (pitch 28nm).

measurement direction along x-direction or y-direction respectively. The CDU determines the deviation of the CD per die from the wafer's average CD. The LCDU is the deviation of the CD of each via within a SEM FoV from the average die CD. Both CDU and LCDU are statistical calculations that refer to data within three standard deviations (3-sigma) from the mean CD value.

In figure (6), on SRAM and logic structures, we achieved an average ADI CD, on pitch 28 nm of around 27 nm, on pitch 24 nm of around 21nm, on pitch 26 nm of around 26 nm or lesser, on pitch 30 nm of around 28 nm. The next challenge lies in shrinkage of CD post etch to less than 20 nm. In the meantime, AEI CDU and LCDU should be less than 1.5 nm and 5 nm respectively. Etch DoEs were done on TEL etch tool, with several iterations and optimization with split in SOG thicknesses, etch deposition and trim steps, different gas chemistries, spin-on- carbon (SOC) and silicon Nitride etch time, silicon nitride over-etch and descum among others. Every iteration was followed by thorough CDSEM inspection on random Logic and SRAM vias initially, however, keeping in mind the complexity of the SRAM structures over logic vias; both small and slot vias were measured within the same FoV for the SRAM modules, concluding metrology was focused on pitch size 28 nm SRAM module. CD and defectivity were also simultaneously monitored with large FoV e-beam inspection on eP5 tool.

Certain CD shrinkage has been observed on SRAM slot vias after etching on CD measured on wafers D10-D13 to around 30nm compared to around 40nm on D03, D06 and D07 as shown in figure (7). Further DoE at specific etch steps and stack has helped to reduce LCDU to below 5 nm and CDU to less than 1.5 nm. Optimized Etch DoEs makes it possible to reduce CD after etching. On pitch 28nm SRAM module, post etch has enabled small via CD ~ 14.48nm with slot via CD ~ 19.55nm.

3.2 Voltage Contrast Metrology & E-beam inspection with HMI eP5 metrology

While the physical inspection can reveal via holes anomalies on top layer (at resist level ADI or hard mask AEI), the Voltage Contrast (VC) metrology helps to check the bottom of the via layer. When Ruthenium is filled into the vias on wafers post etch, VC metrology shows if the bottom of the vias is open or not as illustrated in figure (9). Physical voltage contrast defect inspection is also possible because of the titanium layer at the

BACUS NEWS

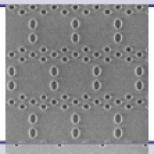
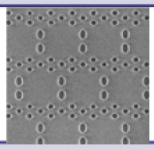
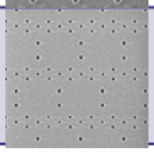
Wafer ID	D09	D20
SoG	10 nm (with etch DoE – 1)	10 nm (with etch DoE – 2)
Via Print (post lithography)		
Via Print (post etch)		
Post lithography CD	Small Vias – 27.18 nm Slot Vias – 31.39 nm	Small Vias – nm Slot Vias – nm
Post etch CD	Small Vias – 14.48 nm Slot Vias – 19.55 nm	Small Vias – nm Slot Vias – nm

Figure 8. Post etch DoE (AEI) data for SRAM small and slot/large vias at pitch 28 nm demonstrating etch shrink to our target below 20 nm.

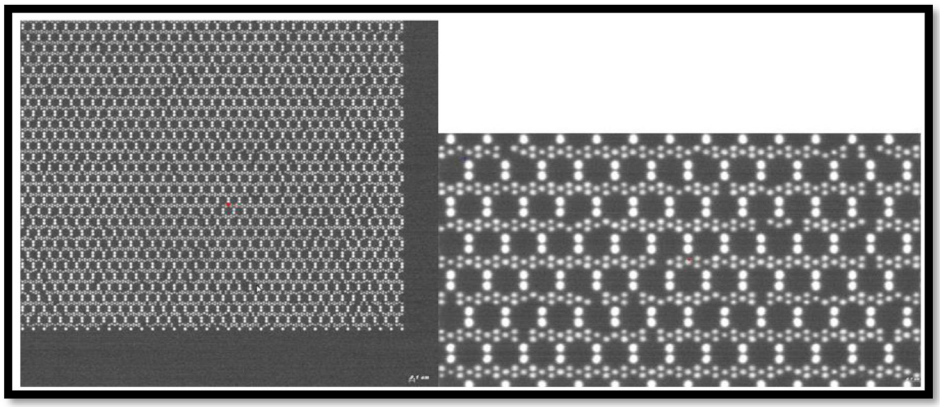


Figure 9. VC inspection metrology enabling detection of very small vias at pitch 24 nm.

bottom of the stack.

HMI-eP5 tool enabled us to collect large field of view images of 8μm x 8μm with default image condition settings. Over 7000 vias per die were measured on the logic clip. It was confirmed that SRAM vias are open validating the etch optimization. Large scale data collected with eP5 included CD measurements that could be used to retrieve parameters like CD, LCDU, defectivity, height, width, small vs slot vias, CoG shift in X-direction, CoG shift in Y-direction, area in single file in a relatively short inspection time. As shown in figure (10), on aligning GDS to image obtained from eP5, it is easy to find merged vias visually at the region of aggressive design.

Further analysis of eP5 data by plotting quantile plots has enabled us to look for any via CD within the distribution. From figure (11), at the bottom tail of the quantile plot, very small vias can be seen with the smallest CDs. The plot also shows that small vias and slot via width were properly measured. In figure (12) and (13), for SRAM and Logic vias respectively, learning is achieved through the pitches in terms of CD shrinkage with the different Etch DoEs due to large number of vias measured and data collected with eP5 inspection.

4. Conclusion

Random logic and SRAM vias are studied for metal 2 to metal 1 layers. Experimental results demonstrated AEI CD of less than 20nm on design target of Pitch 28 nm for both small and slot vias. AEI CD of around 15 nm & LCDU less than 5 nm was achieved with a combination of optimum SoG thickness and specific etch DoEs. E-beam inspection enabled larger FoV data collection on SRAM and Logic vias. From both pitch 28 nm and pitch 26 nm, SRAM and logic structures images collected from e-beam shows high probability of smaller vias in the normal quantile tail. A larger FoV enabled initial assessment of via missing after metallization using VC measurement and to check the bottom of the vias.

5. Acknowledgement

We would like to extend our gratitude for the contribution of the Etch Team of Tokyo Electron Limited (TEL) in Leuven, Belgium.

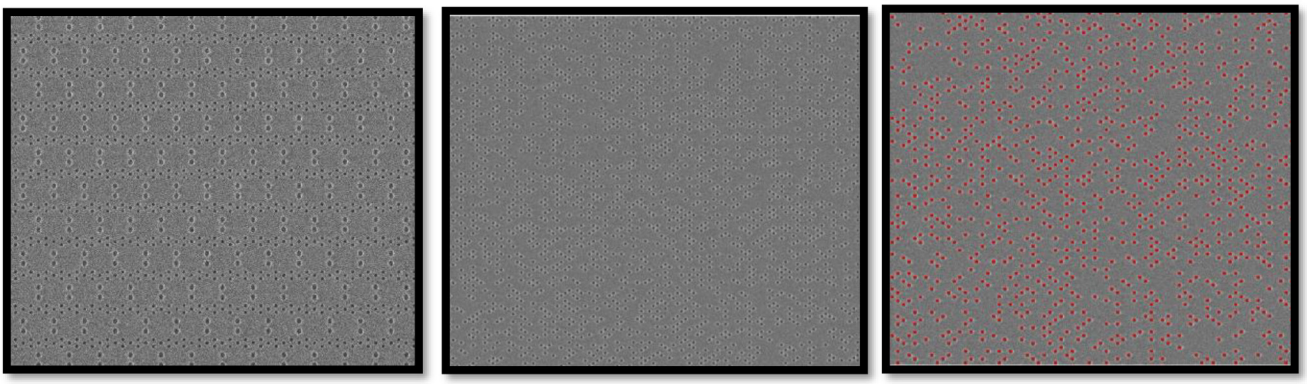


Figure 10. (Left & Center) Small area from a large FoV on SRAM and logic clip; (Right) Image collected post eP5 inspection shows GDS aligned to image.

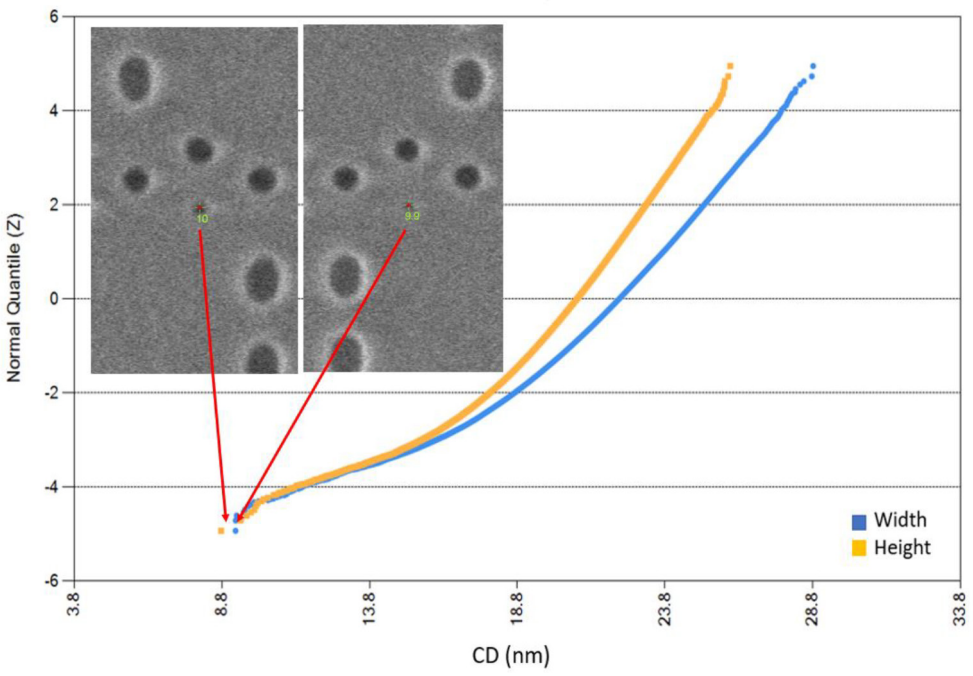


Figure 11. Quantile plot showing small via on distribution lower tail location with high probability of via closure defect (dimension measured in x-direction on via).

6. Reference

[1] Simulation investigation of enabling technologies for EUV single exposure of Via holes patterns in 3nm logic technology, W. Gao, et al, doi.org/10.1117/12.2552888.

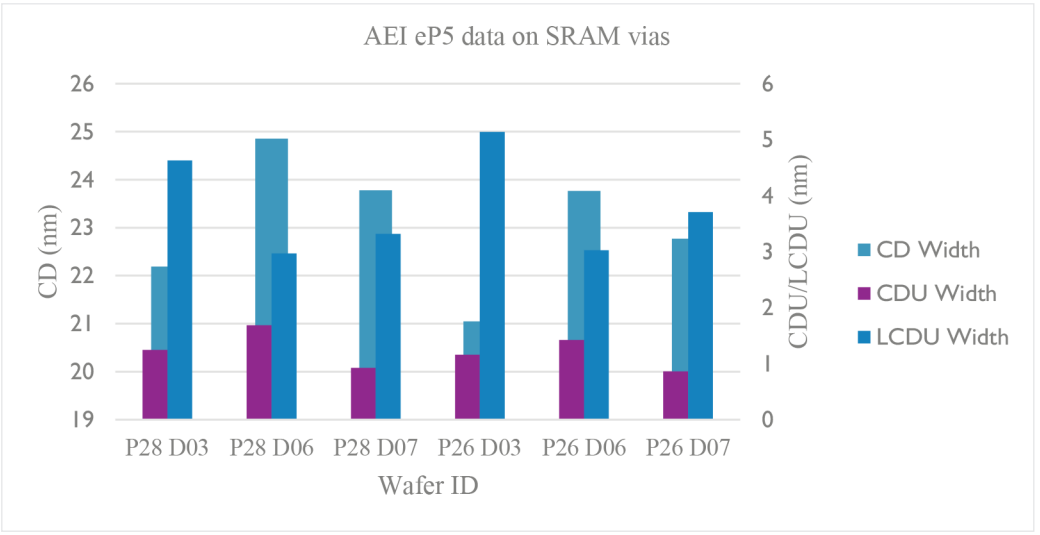


Figure 12. Post Etch (AEI) CD, CDU, LCDU data collected on two pitches from eP5 inspection on SRAM vias.

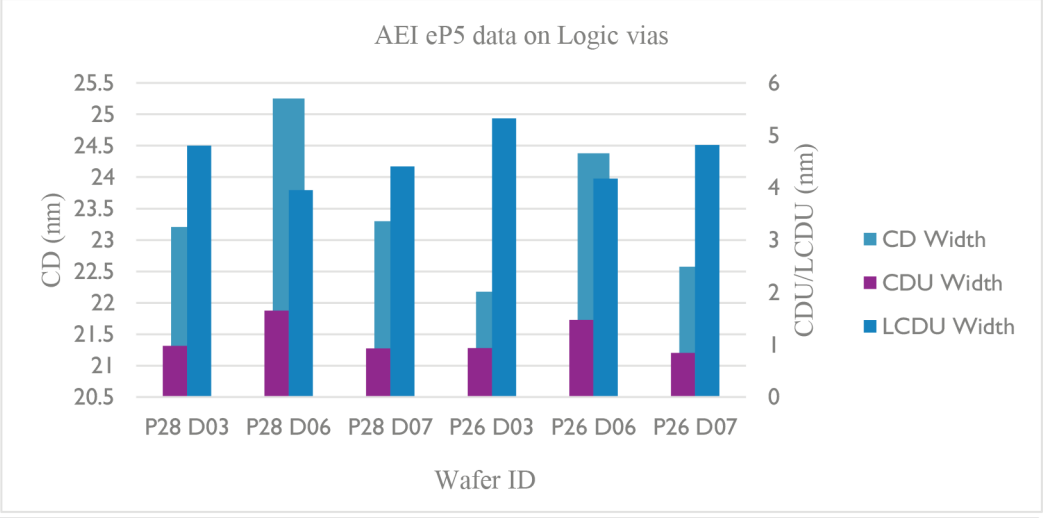


Figure 13. Post Etch (AEI) CD, CDU, LCDU data collected on two pitches from eP5 inspection on Logic vias.

Industry Briefs

Hitachi Launches E-beam Inspection System for EUV 3nm and 5nm Processes

David Manners

Hitachi High-Tech Corporation today announced the Development of its Electron Beam Area Inspection System. The device manufacturers are beginning to utilise EUV in the mass production of 5nm node devices and the development of 3nm node devices. GS1000 is an advanced conventional Electron Beam Inspection system. It is a fusion of a high-performance electron optical system and a high-speed, large-capacity data processing system, which provides solutions to the challenges that arise when introducing EUV lithography to semiconductor device mass-production.

https://www.electronicsweekly.com/news/business/hitachi-launches-euv-2021-12/

Intel Mum on Ohio Fab Project

Alan Patterson

Intel Corp. remains tight-lipped in response to a report that it will build a $20 billion fab in Ohio. The largest U.S. chip maker has chosen a site in Licking County, just east of the state capitol of Columbus. The proposed fab would directly employ 3,000 workers, helping to create an ecosystem of material and equipment suppliers.

"We will decline to comment on this," William Moss, Intel's senior director for corporate communications, said in an email reply to our query about the report. Intel launched two new chip projects last year in Chandler, Ariz., to provide additional capacity for its foundry customers. The $20 billion initiative is the largest private-sector investment in Arizona history.

Late last year, Samsung selected a Texas site for its latest fab project, which will cost $17 billion. That facility will extend capacity at an existing Samsung fab in nearby Austin. TSMC said it will spend as much as $44 billion in 2022 to maintain its manufacturing edge over foundry rivals such as Samsung and Intel. Taiwan-based TSMC is currently building a 5-nm fab in the Phoenix area. That process node is already in production in Taiwan. TSMC will be the world's first to start production of 3-nm chips in late 2022. The new 5-nm TSMC fab in Arizona, announced in 2020, will start production in 2024.

Responding to technology supply chain disruptions, proposed federal incentives are designed to attract new U.S. foundry investments. The $52 billion CHIPS for America Act approved by the U.S. Senate is aimed at reviving the domestic industry over the next decade. The bill must still be approved by the House.

https://www.eetimes.com/intel-mum-on-ohio-fab-project/#

Reliability Concerns Shift Left Into Chip Design

Ann Steffora Mutschler

Demand for lower defect rates and higher yields is increasing, in part because chips are now being used for safety- and mission-critical applications, and in part because it's a way of offsetting rising design and manufacturing costs. What's changed is the new emphasis on solving these problems in the initial design. In the past, defectivity and yield were considered problems for the fab. Restrictive design rules (RDRs) were implemented to ensure chips were designed in ways that could be successfully manufactured. But several things have fundamentally changed since then:

RDRs add too much margin into designs, particularly at advanced nodes. That negatively impacts performance, power and area.

More chips are being customized for specific applications, utilizing advanced packaging, different kinds of processors and memories, and unique architectures that have not been produced in volume in the past.

Longer life expectancy for chips in some applications mean that latent defects can require costly recalls. As a result, design teams are starting to include sensors in designs to determine how a chip is behaving until its anticipated end of life.

A chip used in the drive train of an automobile, for example, has entirely different stresses and expectations than one produced for an IoT consumer device. Design teams need to understand how these chips will behave over time, from environmental and use conditions, to aging, electro-thermal, stress, and variation effects.

https://semiengineering.com/reliability-concerns-shift-left-into-chip-design/

Join the premier professional organization for mask makers and mask users!

About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

Individual Membership Benefits include:

- Subscription to BACUS News (monthly)
- Eligibility to hold office on BACUS Steering Committee

spie.org/bacushome

Corporate Membership Benefits include:

- 3-10 Voting Members in the SPIE General Membership, depending on tier level
- Subscription to BACUS News (monthly)
- One online SPIE Journal Subscription
- Listed as a Corporate Member in the BACUS Monthly Newsletter

spie.org/bacushome

CALENDAR

2022

SPIE Advanced Lithography + Patterning
27 February-3 March 2022
San Jose Convention Center
San Jose, California, USA
www.spie.org/al

Photomask Japan
26-28 April 2022
Digital Forum
www.photomask-japan.org

EMLC 2022
20-23 June
Leuven, Belgium
https://www.emlc-conference.com/

SPIE Photomask Technology + Extreme Ultraviolet Lithography
25-29 September 2022
Monterey, California, USA
www.spie.org/puv

SPIE, the international society for optics and photonics, brings engineers, scientists, students, and business professionals together to advance light-based science and technology. The Society, founded in 1955, connects and engages with our global constituency through industry-leading conferences and exhibitions; publications of conference proceedings, books, and journals in the SPIE Digital Library; and career-building opportunities. Over the past five years, SPIE has contributed more than $22 million to the international optics community through our advocacy and support, including scholarships, educational resources, travel grants, endowed gifts, and public-policy development. www.spie.org.

SPIE.
International Headquarters
P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 360 676 3290
Fax: +1 360 647 1445
help@spie.org • spie.org

Shipping Address
1000 20th St., Bellingham, WA 98225-6705 USA

SPIE.EUROPE
2 Alexandra Gate, Ffordd Pengam, Cardiff,
CF24 2SA, UK
Tel: +44 29 2089 4747
Fax: +44 29 2089 4750
info@spieeurope.org • spieeurope.org

You are invited to submit events of interest for this calendar. Please send to lindad@spie.org.