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PM16 Best Paper-Second Place

Analyzing EUV Mask Costs

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ABSTRACT

The introduction of Extreme Ultraviolet Lithography (EUV) as a replacement for multiple patterning is based on improvements of cycle time, yield, and cost. Earlier cost studies have assumed a simple assumption that EUV masks (being more complex with the multilayer coated blank) are not more than three times as expensive as advanced ArFi (ArF immersion) masks. EUV masks are expected to be more expensive during the ramp of the technology because of the added cost of the complex mask blank, the use of EUV specific mask tools, and a ramp of yield learning relative to the more mature technologies. This study concludes that, within a range of scenarios, the hypothesis that EUV mask costs are not more than three times that of advanced ArFi masks is valid and conservative.

1. Introduction

Extreme Ultraviolet (EUV) lithography has the opportunity to displace multiple patterning in advanced semiconductor production with significant benefits in improved cycle time, faster yield ramp, reduced complexity, and reduced cost.^[1-3] This is dependent on several factors including tool throughput which has been studied extensively,^[ref] and on usage costs including materials. Although EUV mask cost has been previously investigated,^[4-6] this was in a time comparing EUV to much different optical lithography conditions.

In this study, we investigate EUV mask costs during a ramp of introducing EUV into high volume manufacturing (HVM) with increasing volume and yield rates. The mask blank costs are modeled with a simple defect density model, and coupled to a mask cost model based on capital depreciation, material usage, and yields similar to the SEMATECH cost models.^[7] Since any mask cost is dependent on the complexity of the mask which varies by device level, mask tone, and field size, we ratio the cost of EUV masks to the equivalent ArFi mask cost to

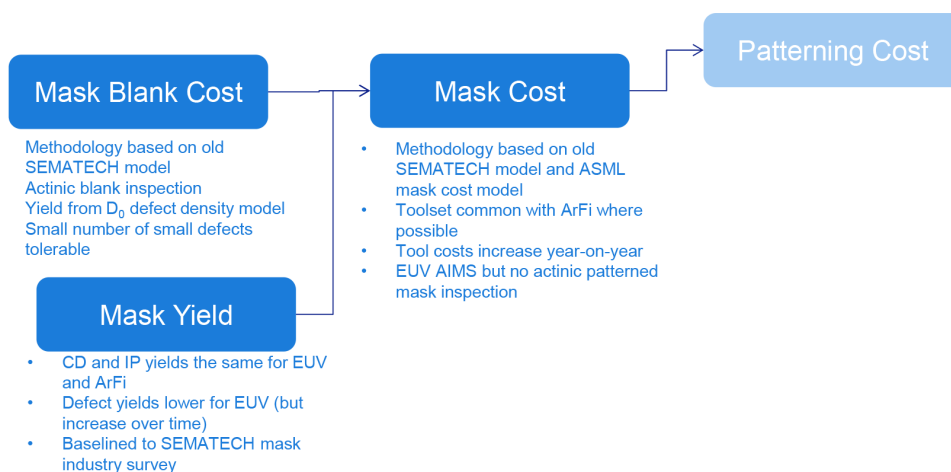


Figure 1. Integrated mask cost model.

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TAKE A LOOK
INSIDE:

INDUSTRY BRIEFS
— see page 8

CALENDAR
For a list of meetings
— see page 9

SPIE.

9985-27

Are the days of separate mask processes and optical proximity correction flows at an end?

D.N. Dunn, IBM Research

For several technology nodes, development has proceeded assuming that mask process limitations can be captured in a simple set of mask rule constraints (MRC). These constraints are typically implemented as a short list of inequalities that govern the minimum space, minimum width, and corner-to-corner separations that optical proximity correction (OPC) algorithms must respect to ensure mask shapes can be manufactured.

As development has proceeded for 7 nm and beyond, it has become clear that mask processes are not necessarily well characterized by rules based constraints, but may require more sophisticated bias models to truly represent the full range of allowable shapes generated by OPC. These bias models have been historically developed in mask houses in the form of mask process correction (MPC) models and typically applied to shapes post-OPC. The need for these types of models is particularly acute for EUV levels where feature dimensions stress process limits of mask processes. In some cases, mask process limitations might drive concessions from upstream unit processes to relax dimensional requirements for key design constructs to enable predictable wafer patterning outcomes.

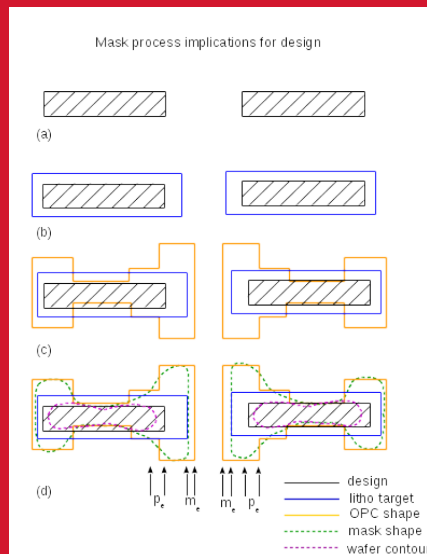
From a high level, it is tempting to treat mask process limitations as yet another complexity challenge, but we believe that this situation is a unique opportunity to incorporate mask process models throughout the entire physical design flow. What, specifically, do we mean by capturing mask processes throughout the physical design flow? To answer this question, we need to explain one possible development flow.

For several nodes, IBM and partners have been exploring a design arc methodology to explore viable technology node architectures. A design arc is a minimum set of constructs and rules required to design representative content which is then evaluated on wafer. The definition of a design arc is typically done by design technology co-optimization (DTCO) teams made up of representatives from design, computational patterning, patterning process, unit process, integration, and device engineers. Target constructs are evaluated through a series of computational patterning simulations, process emulation, and previous node experience to identify the minimum set of ground rules that enable meaningful wafer exploration of architecture choices.

An important part of this process is initial exploration of design constructs with lithography simulations. These simulations incorporate model or rules based retargeting to account for the impact of downstream unit process biases on the ultimate lithography target. Process variability simulations are then carried out using the biased lithography target to identify supportable design constructs and, more importantly, those constructs that cannot be supported with current unit process bias assumptions.

For example, shown in Figures 1a through 1d is a typical tip-to-tip construct of importance in design arc definition. In Figure 1a, a key bar like tip-to-tip construct is proposed in black cross-hatch. In order to transfer this pattern to wafer on target, down-stream unit process biases are

Figure 1: Steps considered in a DTCO flow incorporating mask process awareness. (a) Drawn bars in tip-to-tip configuration. (b) Lithographic target in blue incorporating biases from downstream processes. This target represents the litho target required to pattern bars on wafer. (c) Idealized OPC shapes to print bars at target dimensions. (d) Actual mask shape in green and resulting final wafer contour in magenta.



Continues on page 7

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Table 1. The seven variables chosen for the analysis.

Blank cost +50% -20%
Mask yield +10% -10%
Inspection tool cost +50% -25%
AIMS tool cost +20% -20%
Write time +80% -15%
Inspection time +100% -33%
Number masks / week +/- 20%

	EUV unique
Resist coater	
Blank inspection	<input checked="" type="checkbox"/>
Write (-beam)	
Laser writer	
Resist bake+developer	
Absorber RIE	<input checked="" type="checkbox"/>
Resist strip	
CD SEM	
Image placement	
Clean	
AIMS	<input checked="" type="checkbox"/>
Defect inspection	
Defect repair	
AIMS	<input checked="" type="checkbox"/>
Black border write	
Black border etch	<input checked="" type="checkbox"/>
Final clean	
Final inspection	
Pellicle mount	<input checked="" type="checkbox"/>

Figure 2. Mask patterning flow from the mask cost model with the EUV unique tools identified.

normalize these factors. In this study, the key EUV mask cost drivers are varied in a fractional factorial analysis to provide a set of mask cost ratios. The conclusion is that the largest driver of the ratio is the volume of EUV masks produced which drives the utilization of EUV specific mask tools.

2. Cost Modeling Methodology

2.1 Integrated Model

Mask cost modeling methods have been covered previously by an extensive study from SEMATECH.^[7] However, these studies were completed 10+ years ago and the costs and assumptions used are no longer valid and we update those in this study. The mask blank, mask yield, and fabricated mask cost models were linked in this study so various sensitivity studies could be compared, Figure 1. In a future study, this output will be linked to the total patterning cost model.

The calculation model used in this paper uses a method similar to the SEMATECH studies – a process flow for the mask (or mask blank) is generated and associated with the process and metrology/inspection tool costs and throughput. The cost per step is calculated from the equipment depreciation and productivity. The volume of mask (or mask blank) shipments per week can drive additional process and metrology/inspection tools as calculated from the tool utilization. The number of mask starts per week is adjusted by the yield to reach the required mask shipments per week.

The mask blank model calculates yield based on a D0 defect density model using a Gamma distribution for yield.^[8] Actinic

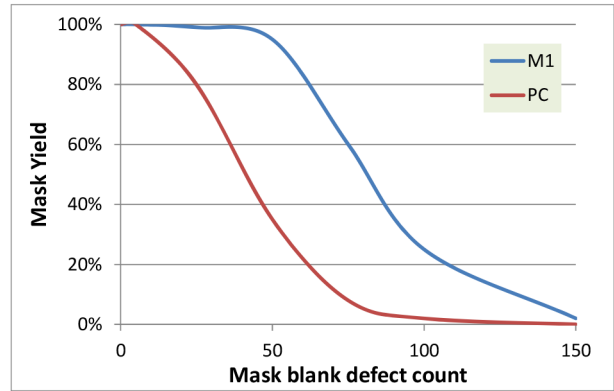


Figure 3. Mask yield versus mask blank defect count using pattern shift defect avoidance for a gate (PC) and metal (M1) device layers. This is a parametrized version from the original data from ref [15].

blank inspection in the blank shop is assumed to be required with only an optical inspection at the mask patterning site. Patterned mask yields were separated into CD, image placement, and defect yields. The EUV mask process flow has a few unique tools and steps (Figure 2) with all other steps held common with ArFi mask production.

2.2 Statistical Analysis

With the goal of testing the ratio of EUV to ArFi mask costs, a statistical test methodology was adopted around the key variables. The operational space of assumptions was calculated using a fractional factorial model^[9] and then regression modeled to provide ANOVA output for the significant factors. A 2⁽⁷⁻³⁾ fractional factorial with power 4 was used around the 7 key variables, Table 1. This test has resolution for two factor analysis as several of the variables are correlated.

3. Input Assumptions

Several input parameters are critical to the end patterned mask cost so were analyzed in some detail in the following sections. Tool costs and process times were estimated, and the more critical factors analyzed in the sensitivity testing in section 5.

3.1 Mask blank defect levels

The critical driving factor for mask blank yields is the defect density during the multilayer deposition step. Recent reports from Hoya^[10] and SEMATECH^[11-12] indicate defect densities ~0.01/cm² can be achieved today. This was assumed as the starting point and year-on-year defect density improvements were assumed.

However, the blank defect target does not have to be zero to make a usable mask. Several studies have discussed using pattern shift^[13] or pattern compensation^[14] to avoid mask blank defects. Small defects (<100nm) in a small number can be avoided with no large defects allowed. This improves the yield of usable mask blanks. This study assumed that 10 defects per blank were tolerable. Several studies have investigated the defect density tolerable with actual semiconductor designs.^[15] Figure 3 shows a parametrized model from the results from^[15] for mask yield versus defect density for two different device levels (gate and metal) as fit to a simple logistics regression.

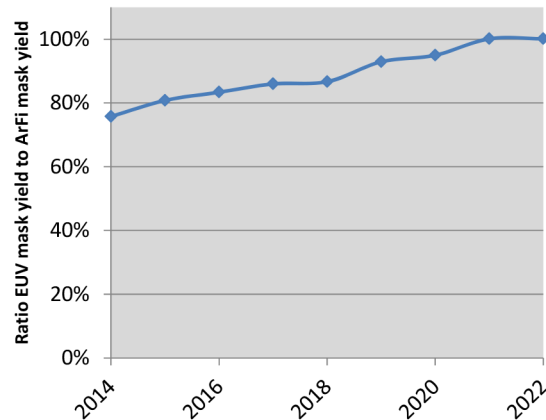


Figure 4. Ratio of patterned mask yields (EUV to ArFi).

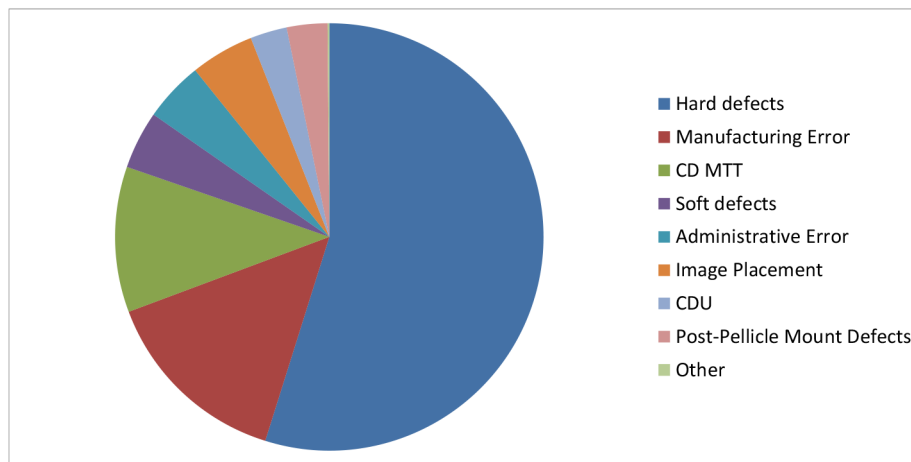


Figure 5. Distribution of yield losses for mask fabrication. Original data from Ref [16].

3.2 Patterned Mask Yields

For the comparison of EUV masks to advanced ArFi masks, the assumption was made that the CD and IP yields would be the same. Previous studies included the assumption that EUV mask CD yield would be higher due to lower MEEF^[7], and IP yield might be lower of ArFi masks due to the need to match signatures in multiple patterning; however these were not included here except in the sensitivity analysis. The EUV masks were given a lower defect yield that decreased as EUV volumes increased to manufacturing levels. Figure 4 shows the ratio of EUV mask to ArFi mask yield over the length of the study.

The SEMATECH 2013 Mask Industry Survey^[16] results were used as the starting point for the patterned mask yields. Both the rate of yield improvement for advanced nodes, and the distribution of CD, IP, and defect yields were extracted from the survey. Figure 5 shows the distribution of defect types from the SEMATECH survey accumulated over an ~10 year range. Approximately 59% of the yield losses are from defects (hard and soft), ~7% from CD losses (uniformity and mean-to-target), and ~5% for image placement yield.

4. Mask Cost Results

4.1 Impact of shipment volume

An important conclusion from the early modeling is the critical importance of mask shipment volume to EUV mask price. With several expensive EUV-specific tools required, if volume is low then the tool utilization is low and tool depreciation is amortized across a small volume of masks. The volume of EUV masks required was assumed to increase through ramp and into high volume manufacturing. If mask shipments were <5-7 masks per week, then depreciation from underloaded EUV-specific tools is the largest driver of EUV mask costs, Figure 6.

4.2 EUV to Advanced ArFi mask cost results

For comparison of EUV to multiple patterning ArFi, as many variables as possible were held constant in the baseline case. The factors that improve the EUV cost over the introduction into manufacturing are the finished EUV mask volume per week (as noted in the prior section) and the EUV mask yield. For this study, the ArFi line was assumed to be at high utilization. Figure 7 shows the ratio of the finished mask costs. The blue line is for

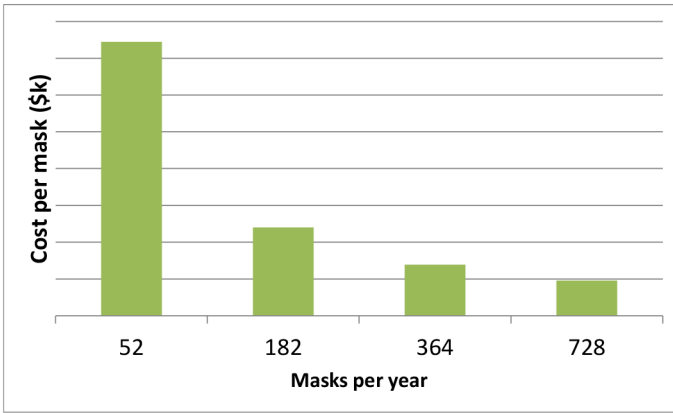


Figure 6. Cost per yielded EUV mask varying only the volume of shipped completed masks. Low production volumes (~1/week) result in high mask costs from depreciating the EUV specific tools across a small production base.

a mask fab dedicated to EUV (so all tools are at low utilization in the pre-volume ramp phase). The red line is for an ArFi mask fab running at high utilization with a few EUV specific tools that are running at a utilization reflecting the volume of only the EUV masks. From the graph, there is a cross-over of the 3:1 ratio either the year before reaching HVM volumes (HVM-1) for the dedicated line, and earlier for EUV specific tools in the existing mask fab.

5. Discussion and Sensitivity Analysis

5.1 Regression model output and parameter sensitivity

The previous section covers the base case of the analysis. However, it is clear that several of the input factors are not easy to predict such that a sensitivity analysis can help provide guidance as to the required accuracy of these parameters to provide guidance on the model results, as well as statistically test across a factor space. The factors varied in the analysis are shown in Table 1.

Figure 8 shows the results of the regression analysis using the scenario during HVM ramp (HVM-1) as two-level plots across the six of the key factors. Figure 9 shows the results of the importance of the variables as ranked from the statistical output (the t-statistic). It should be noted that each of these variables is statistically significant in the analysis, which is expected since a preliminary screening was conducted to identify the most critical factors. Also to be noted is that there are some two-factor correlations in the model (inspection cost and inspection time, for example) which are not graphically shown here.

From Figures 8 and 9, we can conclude that blank cost and the volume of finished masks shipped per time are the most critical variables during the HVM ramp phase. The other factors (inspection cost, inspection time, write time, mask yield, and AIMS cost) are statistically important but with a weight that is less than half of the two primary variables.

5.2 Hypothesis testing

With a regression model, it is possible to model mask costs across a range of the factor space to test where the 3:1 mask cost ratio assumption is a valid hypothesis. Figure 10 shows the output of the regression model across a sample space.

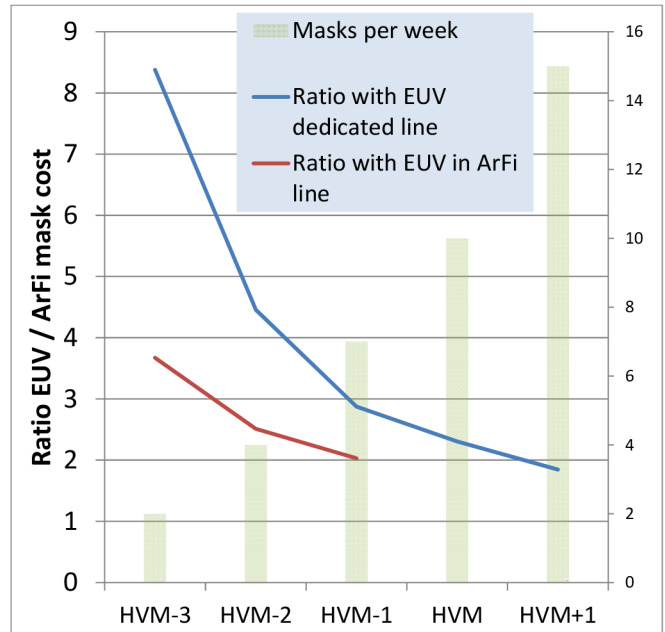


Figure 7. Ratio of the cost of a completed EUV mask to that of an advanced ArFi mask at the same node from this analysis. Horizontal axis is years before and after HVM. Right hand scale and bars indicate the weekly mask ships used in the model.

For each replicate, the mask cost ratio is plotted in increasing cost ratio. The left graph of Figure 10 is centered on the HVM-1 scenario during volume ramp. 78% of the scenarios are below the 3:1 assumption ratio (and the others only slightly higher). The right graph shows the equivalent plot at HVM (higher EUV mask volume and slightly higher EUV mask yield) where all of these scenarios fall below the 3:1 ratio.

Hence we can conclude that across the range of input assumptions tested, the 3:1 ratio of EUV mask costs to advanced ArFi mask costs is valid. It should also be noted that during HVM, more than 40% of the cases fall below a 2:1 ratio. So as volumes increase during HVM, it is possible that an EUV replacement for double patterning scenario could also meet a 2:1 mask cost ratio. However, that scenario has not been statistically tested yet.

This methodology allows for testing of mask costs under a variety of scenarios. However, using the fractional factorial and regression model does not allow for “experimental error” which makes developing confidence intervals difficult. We are exploring variations on this method using simulation with random variates as a next step in the analysis.

6. Conclusion

EUV is being introduced into manufacturing because of benefits in cost, cycle time, yield, process complexity, and others. Currently it is targeted as a replacement for triple patterning, where the total patterning cost ratio is favorable. In this analysis we tested the mask component of that analysis with the hypothesis that EUV mask cost is not more than three times that of a leading edge ArFi mask. Given increasing EUV mask volumes during a manufacturing ramp, the hypothesis is true with the key factor being the number of EUV masks produced and the associated utilization of the EUV specific mask tools. As volumes

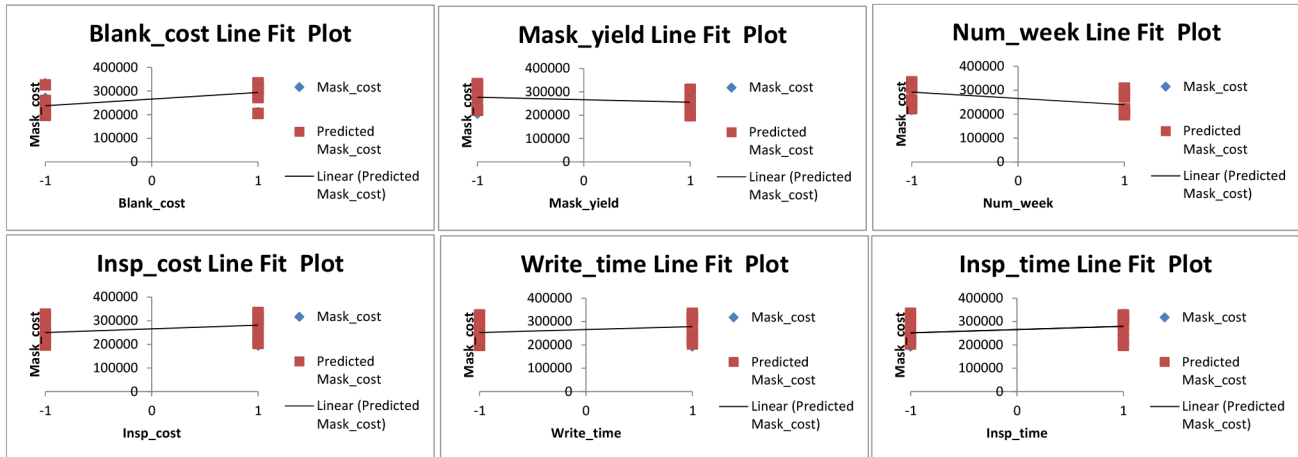


Figure 8. Two level plots for each of the prime factors from the regression analysis for the year before HVM (HVM-1). At low and high levels, the range of yielded mask cost are indicated by the distribution of the red squares. Note that AIMS cost two level plot is not included as it is smaller than the others.

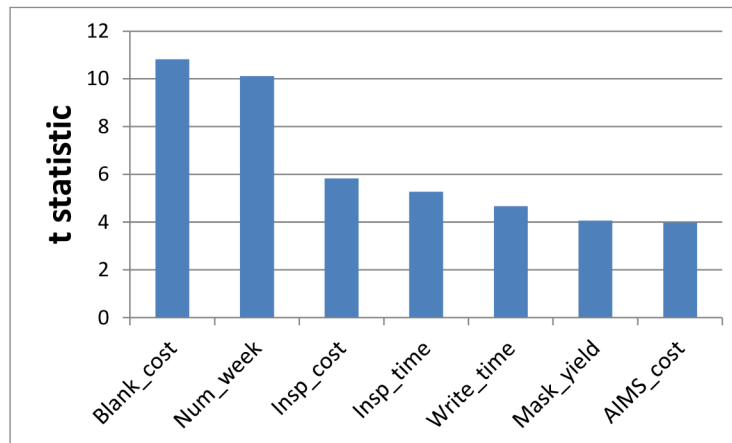


Figure 9. Relative weight of importance of each factor from the regression analysis.

increase, the analysis shows it is possible that EUV masks can even meet a 2:1 cost ratio although that needs further analysis. Hence the conclusion is that given an HVM ramp of EUV, EUV mask costs should match the assumptions associated with multiple patterning.

7. Acknowledgements

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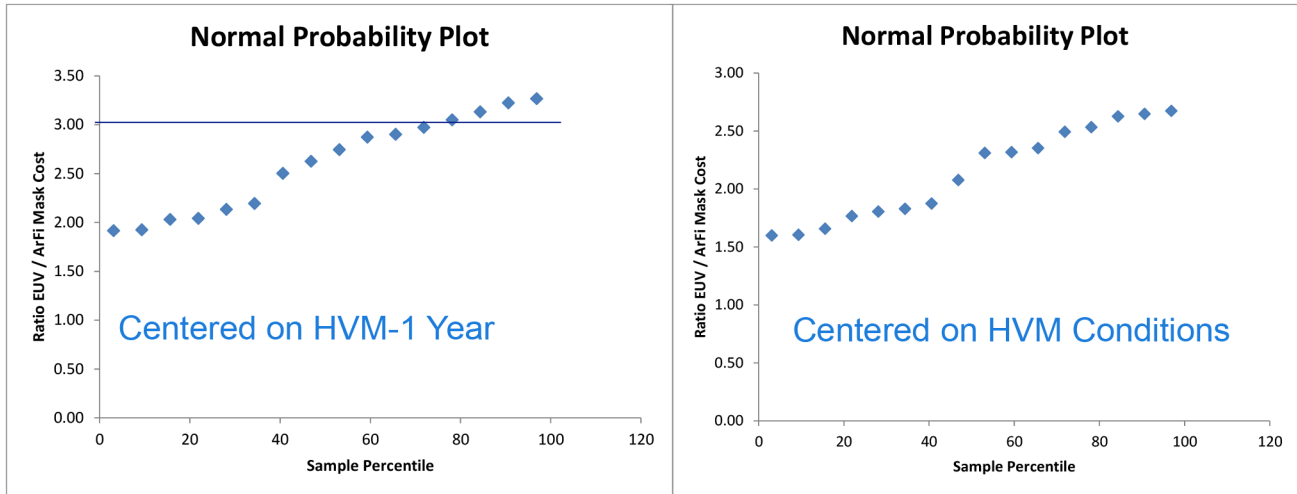


Figure 10. The ratio of finished EUV mask cost to advanced ArFi mask cost at the same node plotted against the results of the regression analysis through the sample space. (Left) for the year before HVM (HVM-1), 78% of the scenarios give a ratio $< 3:1$. (Right) for the first year of HVM, all of the scenarios give a ratio $< 3:1$.

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EDITORIAL

Continued from page 2

taken into account to generate a lithography target drawn in blue in Figure 1b. This feature represents the lithography target that must be printed on wafer to deliver the drawn feature on wafer. Typically, engineers would then take this lithography target, use it in a model based OPC flow to generate the shapes shown in orange in Figure 1c. Process variability contours would then be generated from this idealized mask shape and analyzed to determine whether this bar configuration can be supported.

Wafer reality is impacted significantly by biases not contemplated in steps 1a through 1c. If DTCO teams terminate their analyses at step 1c, they miss significant impacts to their design decisions imparted by mask process capability. For example, a schematic representation of an actual mask shape is shown by the dotted green contours in Figure 1c. There are clearly differences between the actual mask shape and the idealized OPC shape in orange. One aspect of these differences can be represented by the difference in line end dimensions between the idealized OPC shape and the actual mask shape in Figure 1d. The difference between idealized mask shapes and actual mask patterns represented by me leads to wafer level pattern errors represented by pe that are not captured by process variability simulations using idealized OPC shapes.

Clearly, typical DTCO simulation flows are missing a significant source of error in their analyses of potential design constructs. Furthermore, these errors are propagated through the entire computational patterning flow during data preparation of development masks and product masks.

While it is tempting to treat these errors as yet another source of complexity and uncertainty, we believe that these differences should be viewed as opportunities. In particular, we have a tan-

gible opportunity to develop more realistic design space definitions and mask data preparation flows if we incorporate mask process awareness into DTCO processes and mask data preparation flows. Mask process models can be applied to post-OPC shapes to generate more realistic mask shapes for construct analysis similar to what is shown in Figure 1d. In this case, a more accurate assessment of which bar construct configurations can be supported is achievable. In addition, more accurate guidance can be given to unit process owners and mask process owners required to achieve technology node goals.

A second opportunity is to carry mask process bias models forward through OPC recipe development to generate mask shapes that represent as closely as possible shapes delivered by current mask processes. This practice will provide continuity from early design arc definition through product level OPC development, thereby providing a more accurate design to wafer flow computational patterning flow.

While it is easy to recognize an opportunity as valuable, it is far more difficult to implement flows that fully leverage these opportunities. There is still a lot of work to be done to generate bias models with necessary run-time efficiency and accuracy to make mask process aware simulation and OPC flows a reality. There are also business culture issues that will likely have to be overcome to incorporate mask house engineering teams into more traditional DTCO and computational patterning teams. We anticipate that these challenges are well worth embracing because the pay-off for developing these flows will be more accurate ground rule definitions, faster times to market, and fewer wafer resources required to address unanticipated deviations from target on wafer.



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Industry Briefs

■ Third Quarter 2016 Worldwide Semiconductor Equipment Billings Reach \$11B, Reports SEMI

Solid State Technology, December 2016

SEMI, the global industry association representing more than 2,000 companies in the electronics manufacturing supply chain, today reported that worldwide semiconductor manufacturing equipment billings reached US\$11.0 billion in the third quarter of 2016. The billings figure is 5 percent higher than the second quarter of 2016 and 14 percent higher than the same quarter a year ago. The data is gathered jointly with the Semiconductor Equipment Association of Japan (SEAJ) from over 95 global equipment companies that provide data on a monthly basis.

Worldwide semiconductor equipment bookings were \$11.3 billion in the third quarter of 2016. The figure is 30 percent higher than the same quarter a year ago and 5 percent lower than the bookings figure for the second quarter of 2016.

<http://electroiq.com/blog/2016/12/third-quarter-2016-worldwide-semiconductor-equipment-billings-reach-11b-reports-semi/>

■ IEDM Highlights: TSMC, IBM Detail 7-nm Work, Upbeat on EUV Lithography

Rick Merritt, *EETimes*

Like presents under a Christmas tree, separate papers on 7-nm process technology from TSMC and IBM energized a packed ballroom on the first day of the International Electron Devices Meeting (IEDM). They showed results nudging forward both Moore's law and extreme ultraviolet lithography (EUV).

TSMC reported the smallest 6T SRAM to date in a process that it aims to put into risk production by April. IBM described the smallest FinFET made to date in a research device made with EUV. Conference organizers highlighted the papers in October as late-news headliners for the event. Nevertheless, both companies surprised some attendees with more upbeat results than expected.

IBM showed FinFETs with contacted poly pitch of 44/48 nm, a metallization pitch of 36 nm, and a fin pitch of 27 nm. One device included a source-to-drain contact opening of about 10 nm and a gate length of about 15 nm. TSMC described a 256-Mbit SRAM test chip with the cell density of 0.027 mm² with full read/write capabilities down to 0.5 V. The node should provide up to a 40% speed gain, a 65% power reduction, and a 3.3x routed gate density increase compared to TSMC's 16FF+ process now in volume production, said Michael Shien-Yang Wu, a senior director of N7 development at TSMC.

Although it was not part of his formal paper, Wu also commented on work using the 7-nm process to validate EUV. The next generation lithography provided "comparable patterning fidelity" and "comparable yield" to the conventional immersion steppers it will use in the commercial 7-nm process next year.

The EUV systems from ASML are still in a pre-production release. TSMC already announced its plans to start using EUV in its 5-nm node. But Wu declined to give details of how the 7-nm process compares to its 10-nm node or nodes from rivals such as Samsung. He also declined to give aspect ratios of his 7-nm FinFETs, details about a "novel strain technology" the node uses or figures for yields of a test chip that included a GPU and ARM Cortex A-72 core, except that they were in "double digits."

Wu did say TSMC had reached 50% yields on its 7nm SRAM. That suggests it is on a path to have volume manufacturing in the process by late 2017, Kanter said.

http://www.eetimes.com/document.asp?doc_id=1330940

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About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

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2017

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SPIE Advanced Lithography
 26 February-2 March 2017
 San Jose Marriott and
 San Jose Convention Center
 San Jose, California, USA
www.spie.org/al
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SPIE Photomask Technology and SPIE International Conference on Extreme Ultraviolet Lithography 2017
 11-14 September 2017
 Monterey, California, USA
- 
The 24th Symposium on Photomask and NGL Mask Technology
 5-7 April 2017
 Pacifico Yokohama
 Yokohama, Japan
- 
The 33rd European Mask and Lithography Conference EMLC 2017
 27-29 June 2017
 Hilton Hotel
 Dresden, Germany

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