PHOTOMASK

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Alternative material to mitigate chrome degradation on high volume ArF layers

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ABSTRACT

One of the objectives of a robust optical proximity correction (OPC) model is to simulate the process variation including 3D mask effects or mask models for different mask blanks. Assuming that the data of different reticle blanks is the same, the wafer data should be a close match for the same OPC model. In order to enhance the robustness of the OPC model, the 3D mask effects need to be reduced. A test of this would be to ensure a close match of the so called fingerprints of different reticle blanks at the wafer level. Features for fingerprint test patterns include "critical dimension through pitch" (CDTP), "inverse CDTP", and "linearity patterns" and critical dimension (CD) difference of disposition structures. In this manuscript the proximity matching of implant layers on chrome on glass (COG) and advance binary reticle blanks will be demonstrated. We will also investigate the influence of reticle blank material including reticle process on isolated and dense features upon the proximity matching for 28 nm high volumes ArF layers such as implant and 2X metal layers. The OPC model verification has been done successfully for both bare wafer and full field wafer for implant layers. There is comparable OPC model for advanced binary and COG reticle. Moreover, the wafer critical dimension uniformity (CDU) results show that advance binary has much better wafer CDU then COG. In spite of higher reticle cost when switching

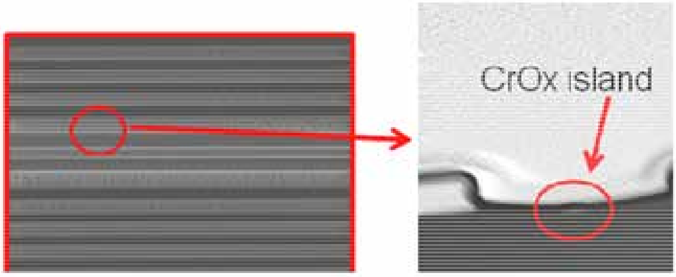

Figure 1. Top-down (left) and cross section (right) SEM micrograph illustration of CrOx island formation in the clear reticle area.

TAKE A LOOK INSIDE:

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EDITORIAL

What if there is no window?

Artur Balasinski, Cypress Semiconductor

In the spring of 2005, I made a bet with Ken Rygler that in 10 years, my Company would take commercial advantage of an EUV machine. Just like many of us, I am now getting increasingly more frustrated that I can lose that bet. With only 2 years to go, the opportunities for a commercial use of EUV in mainstream IC manufacturing are still uncertain. True, there are systems set up as proof-of-concept but from there to making the EUV a game-changer, there is a long way. I keep recalling the Concorde syndrome, discussed at the SPIE in the early 2000's, how that white elephant took off the ground on life support just to come to the bitter end sooner that we hoped for. When it flew, it was a real head-turner, the product it delivered was a traveler's dream, and everything was wonderful, except for the price tag.

In the recent years, there has been a follow-up to this story, which may be of interest to us. Arguably, development of high-tech, capital intensive industries follows similar paths, even if they are in the different phases of their lifetimes. The airline industry has sailed through an ocean of red ink, only recently to emerge with much higher hopes. A huge consolidation took place (true also for the IC makers but not yet to such extent) and two main trends emerged, both related to air travel becoming a low-cost commodity. The aircraft makers and the airlines alike had to forget the quest for speed: they settled for the subsonic. Gone is the quest for comfort – out with the elegance, in with the sardine class. In addition, travel protocols are getting more nightmarish by day. The list of "no's" is suffocating: no pardon for being late, no free food, no liquids in the carry-ons, no operator-assisted booking. This invites two questions: would the general public accept the horrors of future travel or would they rather switch to virtual reality or telepresence? We already google places we can't go to. Aircraft makers have high hopes and bulging order portfolios, but with the travel quality falling on its face, would people follow?

And interestingly for us, are the IC makers going to become as mean to their customers, as the airlines are, quoting design rule restrictions and new process risks, to improve profit margins? Our backs are almost against the wall as far as the scalability goes. At the recent edition of the IEDM, the perhaps inevitable discussion took place, how long the industry could continue scaling. We are "running out of numbers," was a response to a question regarding what was after 7nm. "We're running out of atoms." ML2 and DSA were deemed cost effective and complementary solutions, to extend 193i lithography to the end of the roadmap! The end of the roadmap? Although the ITRS looks out to 2026, one should hope that means the end of the conventional scaling. Memory industry transition from planar to 3D scaling and emerging memory devices into manufacturing over the next decade will drive several unique challenges. We are facing a new paradigm where advancements in materials science, equipment, and control methodologies are critical for scaling cadence. This, again, is not dissimilar to the efforts of aircraft makers, to make the flying equipment lighter using carbon-based composites.

With all this, hopes remain high for EUV – the urgent need for it was confirmed at the IEDM. Only, it was not going to happen for 10nm and the delay has already caused most companies to look earnestly for alternatives.

I recently witnessed a conversation between a manager and a group of engineers. The manager said, "So you are looking for a window, that is great, very commendable. But what if there is no window?" The response was, "Well, then, we have to reengineer the whole thing". If I lose my bet with Ken, would it mean that the window for EUV does not exist?

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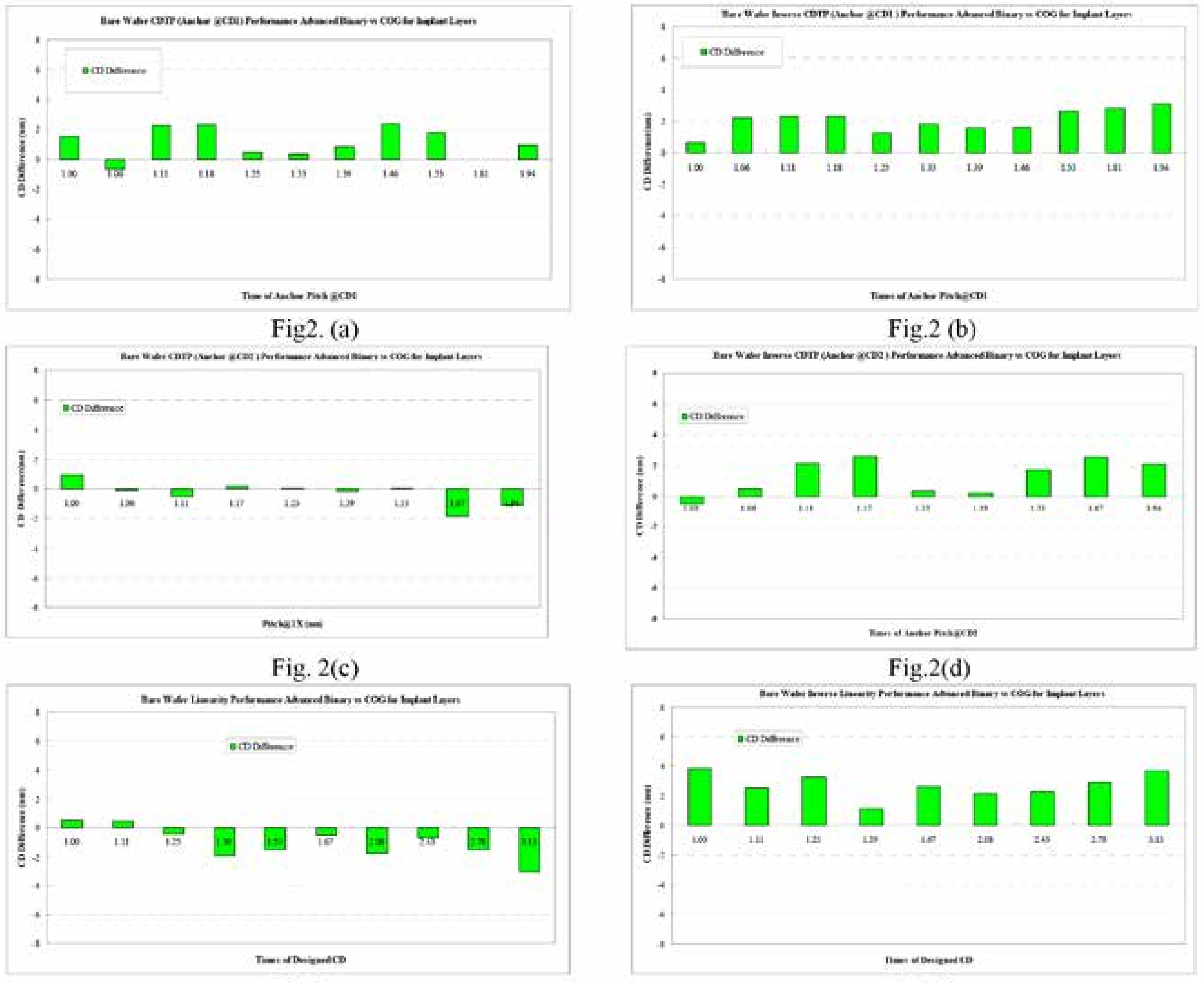

Fig2. (a) Fig.2 (b) Fig. 2(c) Fig.2(d) Fig.2(e) Fig.2(f)

Figure 2. Process matching verification based on bare wafer for advanced binary vs COG (a) CDTP CD difference at CD one; (b) inverse CDTP CD difference at CD one; (c) CDTP CD difference at CD two; (d) inverse CDTP CD difference at CD two;(e) linearity CD difference; (f) inverse CDTP CD difference.

over to advanced binary, there is a considerable cost reduction for the wafer fab which includes a 39% savings in total reticle cost as well as cost reduction due to minimal line holds (LH), wafer reworks and scraps due to Chrome degradation.

1. Introduction

A competitive foundry environment ultimately requires stringent yield loss mechanism control and continuous reduction of reticle-related manufacturing costs. Chrome on glass (COG) reticles have well-known degradation issues, resulting from photo-chemical deposition of the light-absorbing film during photolithography exposures, electrostatic discharge, and electric field-induced metal migration.[1] All those effects result in a dynamic drift of resist printability on a wafer, increasing defect generation and yield degradation risks. Although the drift is detectable by reticle defect inspection, it remains hardly quantifiable. To ascertain the lifetime of a COG reticle usage, a systematical monitoring via wafer level measurements of in-die disposition structure is required, which increases overall cost and cycle time. Taking into account that there is a relatively big number of COG reticles for each product tapeout, more effective methodology or material change is needed in the nearest future. With recent developments of sulphate-free cleaning process, stringent environment controls at the mask house and litho, improved pellicle materials, the formation of

Table 1. Writer and mask process for COG and advanced binary (ArF implant layers).

Blank	Writer	Mask Process
COG	Laser	COG
Advanced Binary	EBM	Advanced Binary

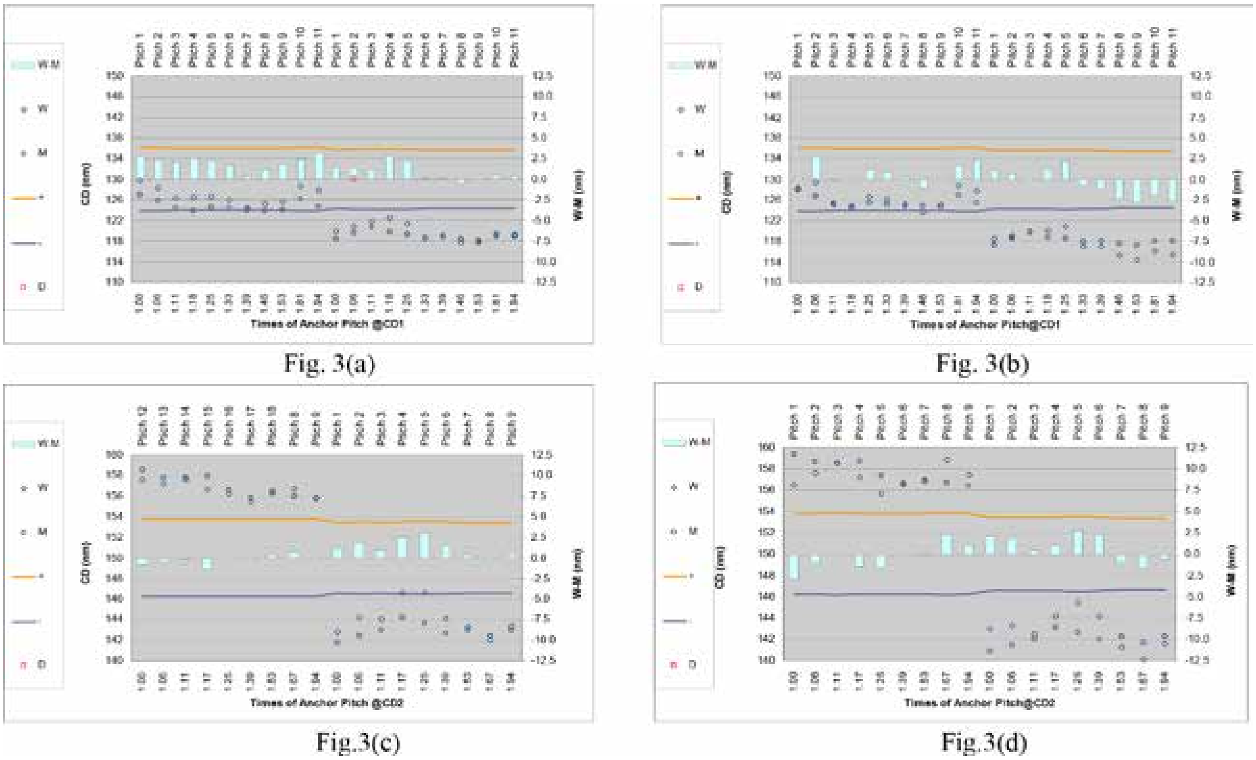

Fig. 3(a) Fig. 3(b) Fig.3(c) Fig.3(d)

Figure 3. CDTP and inverse CDTP OPC verification based on bare wafer for COG and advance binary(a) COG OPC OPC model verification at CD one; (b) advance binary OPC mode verification at CD one; (c) COG OPC model verification at CD two; (d) advance binary OPC mode verification at CD two.

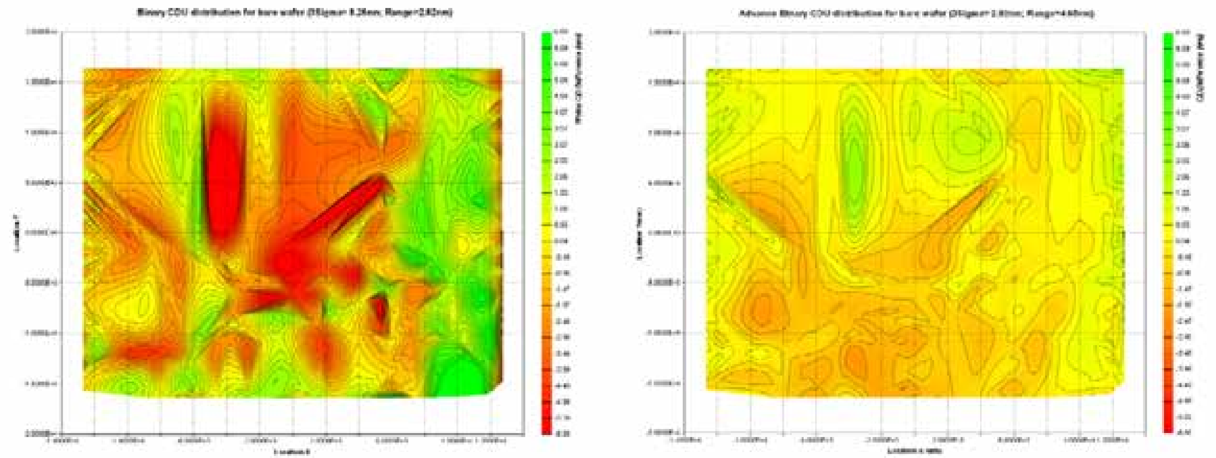

Figure 4. CDU distribution based on bare wafer for COG and advanced binary (ArF implant layer).

haze crystals has significantly reduced.[2] An upgrade of reticle process towards advanced binary reticles is the direct solution of problems discussed above. Advanced binary reticle process does not show similar mechanisms and trends and has been successfully utilized for 1X and 1.3X metal layers in foundry manufacturing environment.

The main challenge of mask making process upgrade within foundry manufacturing environment lies in wafer-level pattern matching for small-size features. A mismatch may appear due to 3D mask effects and across field uniformity distortion arising from different reticle substrate stack and writing process. The first concern may be addressed by an Optical Proximity Correction (OPC) model, which is able to simulate the process variation including 3D mask effects or mask models for differ-

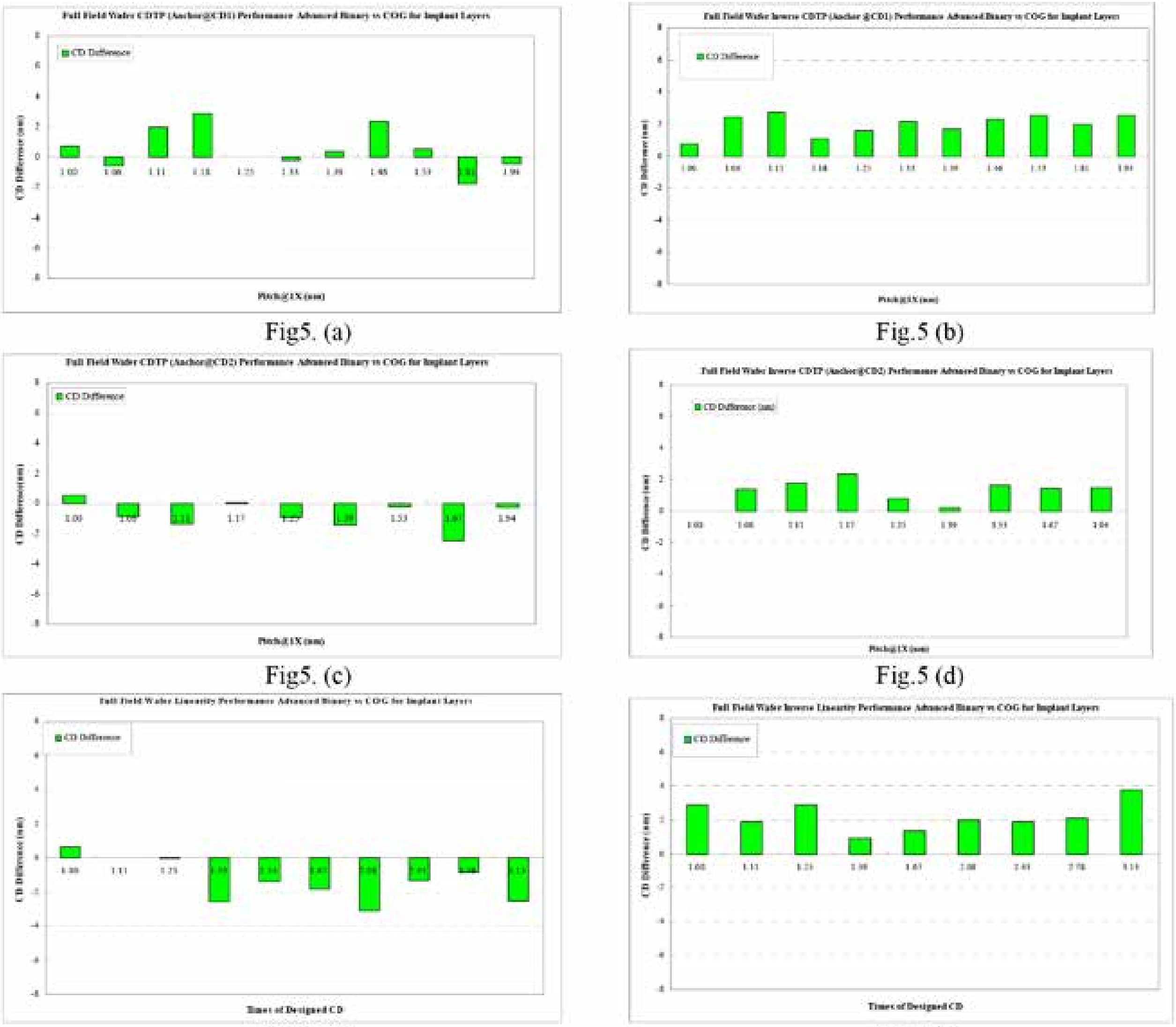

Fig5. (a)

Fig.5 (b)

Fig5. (c)

Fig.5 (d)

Fig5. (e)

Fig.5 (f)

Figure 5. Process matching verification based on full field wafer for advance binary vs COG (a) CDTP CD difference at CD one; (b) inverse CDTP CD difference at CD one; (c) CDTP CD difference at CD two; (d) inverse CDTP CD difference at CD two;(e) linearity CD difference; (f) inverse CDTP CD difference.

ent mask blanks.3 In order to enhance the robustness of the OPC model, the 3D mask effects need to be reduced. On the other hand, a strict level of CDU matching enables cost-saving extensibility of the new mask process for next generations of technology.[4] Therefore, to systematically quantify the process change, optical proximity correction (OPC) and across field CD uniformity (CDU) wafer level verifications are required. Assuming that the data of different reticle blanks is the same, the wafer data should be a close match for the same OPC model.

In this manuscript we demonstrate the robustness of the new reticle process based on foundry pattern matching criteria of implant layers on COG and advance binary reticle blanks. OPC model verification has been done for both bare and fully integrated wafer. The OPC model performance is comparable for advanced binary and COG reticles. We show the influence of reticle blank material including reticle process on isolated and dense features upon the proximity matching for 28nm implant layers. Moreover, CDU results show that advance binary has much better wafer CDU then COG. The results of the investigation of the 3D mask effects including the influence of the reticle writer, as the proximity matching will be affected by the 3D mask even if the same writer is used. In spite of higher reticle cost when switching over to advanced binary process, there is a considerable long term cost reduction for foundry operations which is estimated to 39% savings in total reticle cost.

2. Experimental results and discussions

The physical appearance of reticle chrome degradation for COG is as depicted in Figure 1. Electro-field migration of the CrOx from the top and sidewall of the structures leads to the

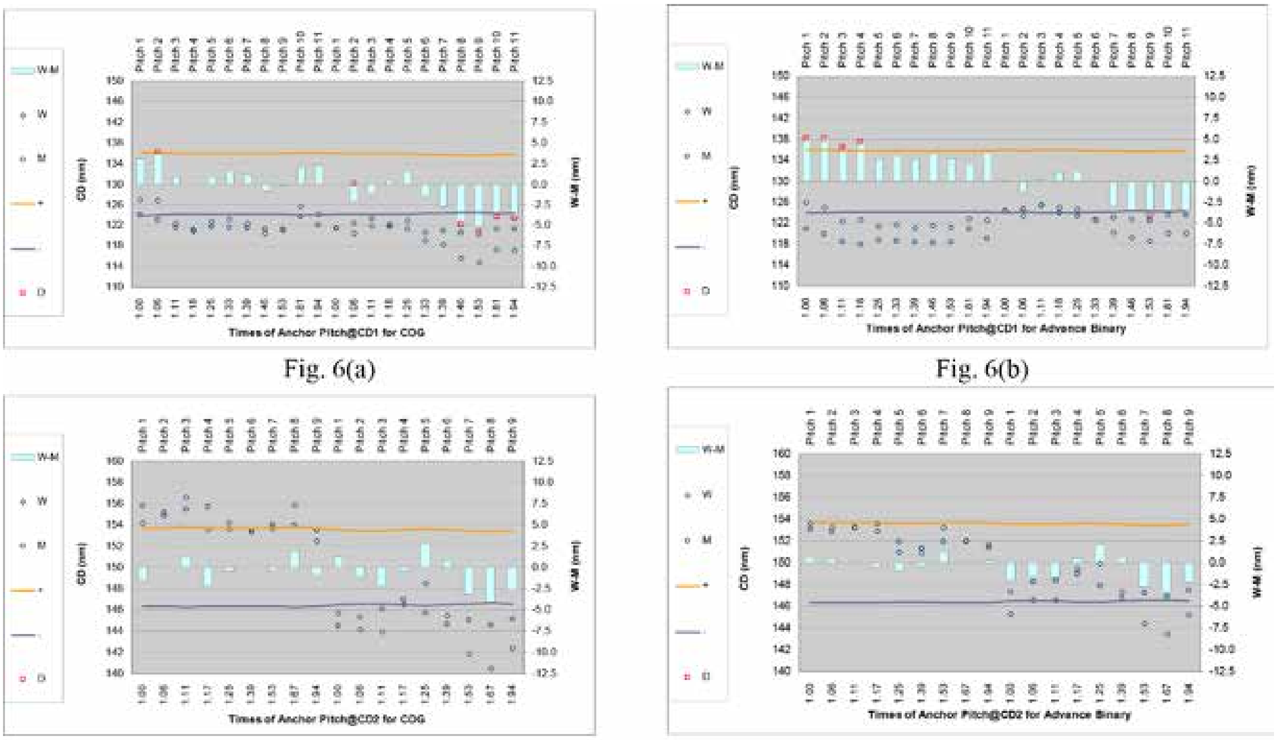

Fig. 6(a)

Fig. 6(b)

Fig. 6(c)

Fig. 6(d)

Figure 6. CDTP and inverse CDTP OPC verification based on full field wafer for COG and advance binary(a) COG OPC model verification at CD one; (b) advance binary mode verification at CD one; (c) COG OPC model verification at CD two; (d) advance binary mode verification at CD two.

formation of the footing at the sidewall and eventually to the formation of CrOx islands in the clear or trench.

In order to obtain the wafer-level CD difference between reticle blanks, COG and advanced binary mask process were evaluated for high-volume manufacturing implant layers. In-house designed features for fingerprint test patterns include “critical dimension through pitch” (CDTP), “inverse CDTP”, “linearity patterns” and CD difference of disposition structures. An automated design-based CDSEM tool metrology platform has been used for data collection.[5] The details of mask process between COG and advanced binary for ArF implant layer are described in Table 1.

Fig. 2 (a) and (b) show the CDTP and inverse CDTP performance for advanced binary and COG based on bare wafer CD which is anchored at CD one. The results indicate that the COG and advanced binary match very well when anchored at CD one. The point-to-point CD difference is ~2nm. Fig.2 (c) and (d) demonstrate the CDTP and inverse CDTP matching between COG and advanced binary based on anchor CD two. The values of CD two is about 20nm bigger than anchor CD one. It clearly illustrates that COG and advanced binary have better CDTP and inverse CDTP at larger anchor CD due to the proximity matching of laser writer and electronic beam (EBM) writer. The linearity and inverse linearity process match results are demonstrated in Fig. 2(e) and (f). It illustrates that COG and advanced binary match well. The point-to-point CD difference is ~ 2.5nm.

The CDTP and inverse CDTP OPC verification for COG and advanced binary for different anchor CD is displayed in Fig. 3. Figs. 3 (a) and (b) illustrate that both COG and advanced binary match well to OPC model simulation results at anchor CD one. The CD difference between wafer measurement and simulation data is almost within 2.5 nm for both COG and advanced binary. Figs. 3 (c) and (d) display the CDTP and inverse CDTP OPC verification for anchor CD two. It can be seen that the CDTP and inverse CDTP matching results are comparable for COG and advanced binary at anchor CD two.

Table 2. Writer and mask process for COG and advanced binary (ArF 2X metal layers).

Blank	Writer	Mask Process
COG	EBM	COG
Advanced Binary	EBM	Advanced Binary

The distribution of the CD-difference of special dispositioning structures is also an important criterion to assess the variation of the intra-field CD across the entire wafer. In Fig. 4 the distribution of the CD-differences of dedicated dispositioning intra-field structures across the wafer is displayed. It can be seen that advanced binary has much better performance than COG. Fig. 5 (a), (b), (c) and (d) demonstrate the CDTP and inverse CDTP performance at different anchor CD for both COG and advanced binary based on fully integrated wafer CD. The point-to-point CD difference is ~ 2.0 nm compared with

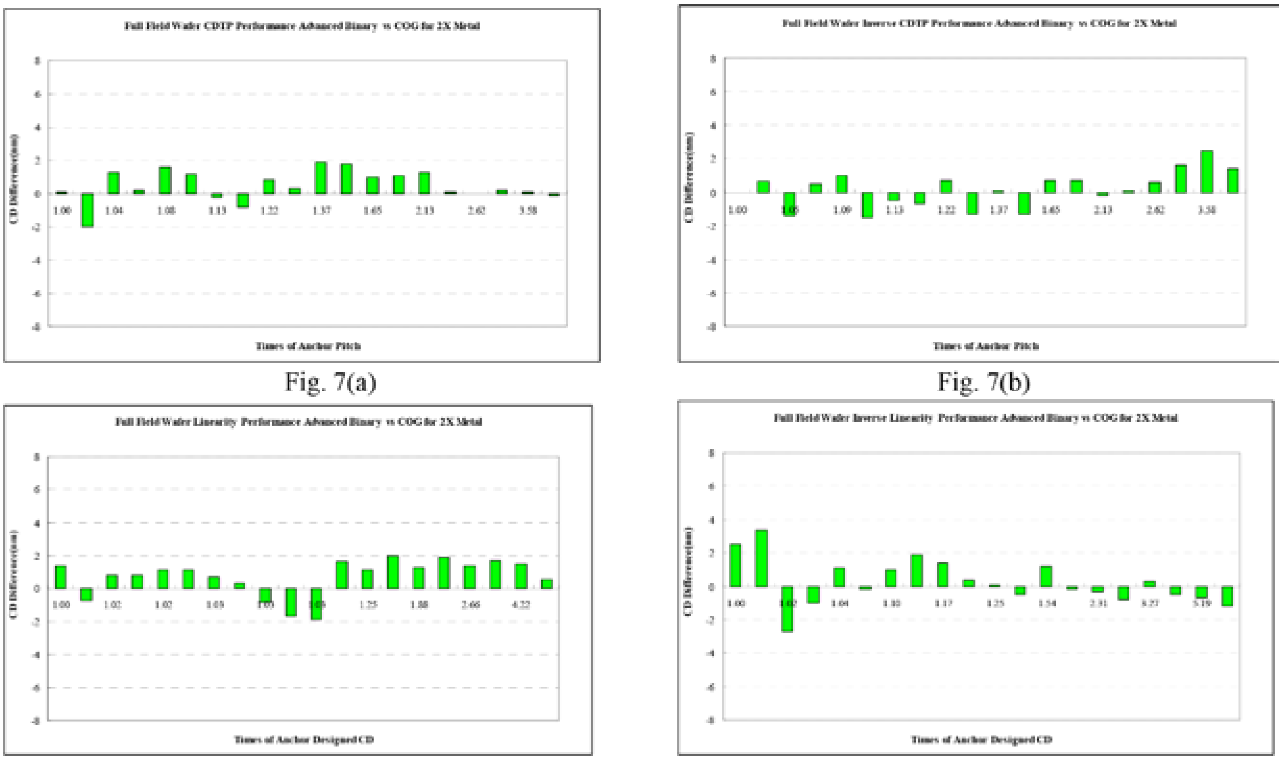

Fig. 7(a)

Fig. 7(b)

Fig. 7(c)

Fig. 7(d)

Figure 7. Process matching verification based on full field wafer for advance binary vs COG using same EBM writer (a) CDTP CD difference; (b) inverse CDTP CD difference; (c) linearity CD difference; (d) inverse CDTP CD difference.

COG and advanced binary for both anchor CD one and two. As anchor CD two is about 20nm larger than anchor CD one, it shows advanced binary has a better match to COG at the higher anchor CD. This is due to the better proximity matching between the EBM and tha laser writer at larger CD. Fig. 5(e) and (f) illustrate the linearity and inverse linearity matching based on full field wafer. The point-to-point CD difference between COD and advanced binary is ~2.5 nm. Compared with the bare wafer and fully integrated wafer matching results between COG and advanced binary, it demonstrates that the wafer topography has slightly better tolerance for the process match of COG and advanced binary.

The CDTP and inverse CDTP OPC verification for COG and advanced binary for difference anchor CDs is illustrated in Fig. 6. Figs. 3 (a) and (b) illustrate that both COG and advanced binary match well to OPC model simulation results at anchor CD one for full field wafer CD. The CD difference between wafer measurement and simulation data is almost within 2.5 nm for both COG and advanced binary. Figs. 6 (c) and (d) display the CDTP and inverse CDTP OPC verification for anchor CD two. It can be seen that the CDTP and inverse CDTP matching results are comparable for COG and advanced binary at anchor CD two. It also shows that the wafer CD results match better in anchor CD two for both advance binary and COG.

Table 1 demonstrates the different writers for COG and advanced binary for ArF implant layer, the same writer for COG and advanced binary is shown in table 2 for ArF 2X metal layers.

Fig. 7(a) and (b) demonstrate the CDTP and inverse CDTP performance of 2x metal layer matching between COG and advanced binary. The CD-difference is within 2.0 nm based on full field wafer. Figs. 7 (c) and (d) demonstrate the line and space linearity performance for advanced binary matching to the COG. It can be seen that advanced binary matches well to COG with a point-to-point CD difference of within 2.0nm.

Fig. 8 displays the full field wafer CD difference distribution of several dispositioning structures. It can be seen that advanced binary has a better distribution of CD difference-values (with a 3sigma-value equal to 1.20 nm and a range equal to 1.71 nm which is about 55 % better than COG.

3. Conclusions

The goal of this study was to systematically investigate the alternative reticle material to mitigate chrome degradation on high volume manufacturing ArF layers. The influence of blank material and reticle process on isolated and dense features upon the proximity matching for 28nm high volumes ArF layers has also been investigated. The OPC model verification has been done successfully for both bare wafer and full flow wafer for implant layers. The results show that there is comparable OPC model for advanced binary and COG reticle based on both bare silicon wafer and fully integrated wafer. Moreover, the bare wafer-level CDU results clearly demonstrate that advance binary has much better wafer CDU than COG. In spite of higher reticle cost when switching over to advanced binary, there is a comparable processing match and OPC verification for both implant layers and 2X metal layers. The fully integrated wafer

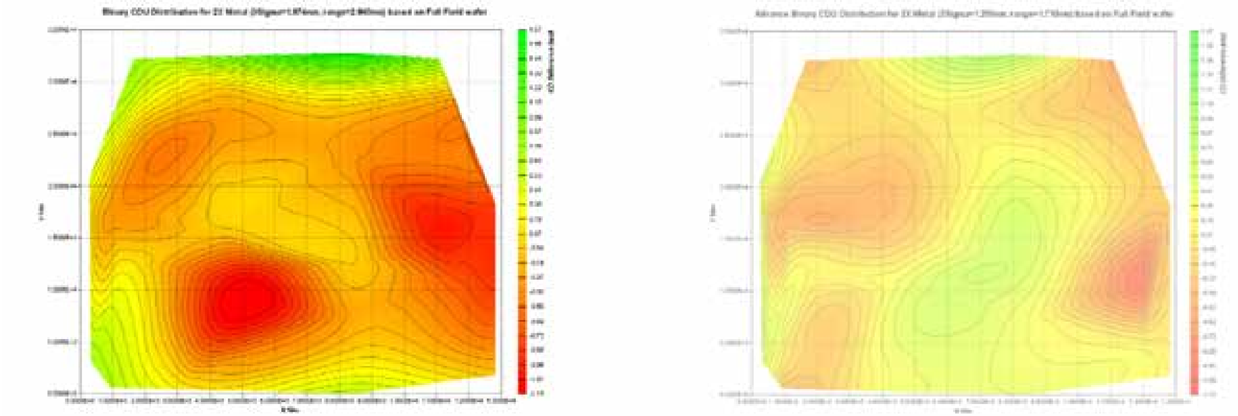

Figure 8. Across field CDU distribution collected from fully integrated wafer for COG and advance binary (2X metal layer).

CDU results of 2X metal layer indicate an improvement of about 55% in CDU when shifted to advanced binary.

4. Acknowledgments

We would like to express our deep appreciation to GLOBALFOUNDRIES metrology and one integration teams (K. Kurth, P. Javorka) who swiftly enabled wafer logistics and quick automated data collection / recipe troubleshootings.

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Industry Briefs

■ North American Semi Equipment Industry Posts November 2013 Book-to-Bill of 1.11

North America-based manufacturers of semiconductor equipment posted in November 2013 $1.24 billion in orders worldwide (three-month average basis) and a book-to-bill ratio of 1.11, according to the SEMI/EMDS Report. The bookings are 10.1% higher than $1.12 billion for October 2013 of, and 72.3% higher than $718.6 million for November 2012. The billings are 4.0% higher than for October 2013 at $1.07 billion, and 22.4% higher than for November 2012 at $910.1 million. The continuing rise in equipment bookings points to year-end order activity substantially stronger compared to one year ago, according to Denny McGuirk, president and CEO of SEMI. This trend supports the current outlook showing a rebound in equipment spending for 2014.

■ Avago to Buy LSI for $6.6 Billion to Focus on Storage Chips

By **Sruthi Ramakrishnan**

Avago Technologies said it would buy LSI Corp for $6.6 billion in one of the semiconductor industry's largest deals in 2013, as it turns to the fast-growing storage chip market to counter volatility in its main wireless business. Avago's shares rose as much as 11 percent to an all-time high of $50.55 on Nasdaq, while LSI jumped 39 percent to $10.99, below the $11.15-per-share cash offer. The combined company will have about $5 billion in annual revenue. Avago's customers include Apple Inc, Samsung Electronics Co Ltd, LG Electronics Inc and Huawei Technologies Co Ltd.

The wireless business' share of Avago's revenues will fall by half to 25 percent, to help help reduce exposure to that sector's volatility, which is only expected to increase, Chief Executive Officer Hock Tan said on a conference call.

Silver Lake Partners will help fund the acquisition with a $1 billion investment in the form of a seven-year convertible note. Avago said the remaining funding for the acquisition would come from a $4.6 billion term loan from a group of banks and $1 billion of cash in hand. The deal would immediately add to free cash flow and earnings per share, excluding one-off costs. It forecast savings of $200 million in the 12 months ending November 1, 2015, the first full fiscal year after the transaction closes.

■ Globalfoundries Adjusts Global Workforce

By **Josephine Lien** and **Jessie Shen**

Globalfoundries is adjusting its global workforce, including an up to 3% reduction, to optimize its cost structure and strengthen the company's competitive positioning. The job cuts will involve mainly non-technical support staff. About 400 employees were to be laid off by the end of 2013.

Globalfoundries has been taking an aggressive approach to expanding its presence in the semiconductor foundry space, including establishing a regional office in Shanghai in September 2013 to better serve its IC design customers in China. The company unseated United Microelectronics as the world's second-largest pure-play IC foundry in 2012, also making a large investment in developing 14nm FinFET technology under the IBM Common Platform Alliance. The company is also building an R&D facility at its Fab 8 campus in New York at the cost of nearly US$2 Billion. Globalfoundries' capex for 2013 is estimated at around US$4.5 billion. The foundry has spent more than US$10 billion to support its expansion over the past three years.

■ SK Hynix Plans New Chip Factory Next Year for Mobile

By **Jungah Lee**

SK Hynix Inc., the world's second-largest maker of memory chips, plans to build a new factory in South Korea to meet the growing demand for mobile devices. The company plans to invest 4 trillion won ($3.8 billion) in 2014 on the plant, maintenance and technology upgrades at existing facilities. Construction of the new factory will begin in 2014, with production of DRAM chips starting in 2015.

SK Hynix, a supplier to Apple Inc. and Sony Corp., is seeking to tap higher prices and surging semiconductor demand for smartphones and tablet computers with advanced features. The company had 28.5% of the market for DRAM chips in the third quarter of 2013, compared with Samsung Electronics Co. 37.1%, and Micron Technology Inc. controling 26.2% of the market.

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Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

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