PHOTOMASK

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Impact of EUV photomask line edge roughness on wafer prints

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ABSTRACT

The line-edge roughness (LER) of a photomask image has a measurable impact on the corresponding printed wafer LER. This impact increases as wafer exposures move from 193nm DUV to 13.5nm EUV wavelengths since the imaging tool is a low-pass filter with EUV passing more spatial frequencies. Even the high frequency mask LER may impact the wafer image by lowering its image log-slope (ILS). Studying the magnitude and frequency content of mask LER is a first step to reducing the wafer LER. The next step is to determine which components of mask line roughness actually contribute to the wafer line roughness. Order is imposed on this study by fabricating programmed LER patterns on an EUV mask to introduce controlled variations in LER spatial frequency and magnitude. More specifically, line-width roughness

(LWR), LER and power spectral density (PSD) are extracted from 64nm and 90nm (1X) pitch lines on a programmed LER EUV photomask. The same mask is then exposed on the ASML EUV Alpha Demo Tool (ADT) at best focus and dose. Three chemically amplified EUV photoresists are evaluated using the programmed LER photomask through
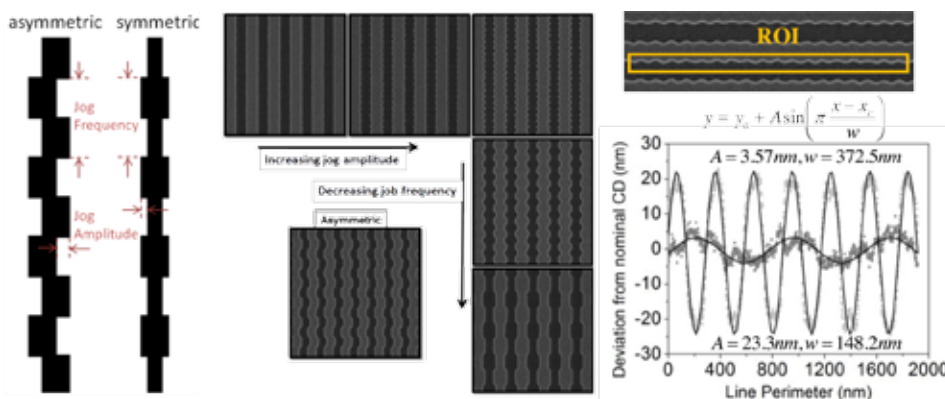
Figure 1. (left) Schematic of symmetric and asymmetric programmed LER. Jog pitch and jog width nomenclature defined. (middle) SEM micrographs of photomasks with programmed LER. (right) Region of interest (ROI) for raw line data extraction. Two programmed LER lines fit to a Sine function of for the extraction of actual jog width and jog pitch.

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EDITORIAL

BACUS Scholarships:
Are we bridging the gap?

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February is the month when we start our annual cycle of candidate selection for scholarships. Following the introductory meeting, the selection process would identify the few best and brightest among the hundreds of applicants, many of them with outstanding academic credentials, impeccable references, and great abilities. As a member of the Selection Committee, I am often having difficulties to contrast this enormous human potential with the prospects that lie ahead, based on what we, the industry veterans, are readying for the Candidates. It is easy to award the monetary prize, but much less easy to fulfill the promise that goes with it, in terms of the employment prospects, the academic guidance, and the overall hope of good life that would be enabled due to the direction the awardee takes as a result of the shining success.

There are several levels of issues I am wondering about when reviewing the applications. Some of them have easy (not necessarily pleasing) answers, some do not. Why has the NCG (New College Graduates) hiring slowed to the point that those who graduate have to seek extension of their university-based support to survive? Here, the answer is "easy": because the industry can make a penny by cost reduction, and adding to the payroll is not a solution to improve the bottom line. It may be a way to improve the top line, some time in the future, but the number of companies willing to bet on the young blood is not large enough. Not too long in the past, those who risked ended up under water.

Another key issue for BACUS community is a gap between the student's expertise and the subject matter discipline we are dealing with. The gap between university training and the realities of the Photomask world has always been substantial, but these days, it seems bigger than ever. I do not have an "easy" answer to this one, but having to guess, which of the esoteric theses on the theory of light would be a better background to advance the mask and lithography business, is challenging. Here, I rely on the scrutiny of academic credentials, something I can put a ruler to. I do it in the hope that the brightest minds would find their ways to shape up the world to their satisfaction, no matter in how bad a shape the previous generation would leave it.

Let's come back to the title question: Are we bridging the gap? The gap between the expectations of the Committee and those of the Candidates, the gap between the education and the industry, between the job market and the NCG enthusiasm. Surely that is something we should address by updating our agenda, by looking into what the universities have to offer, by thinking more about the mainstream customer than about the niche problems with poor market response. And more about the innovation than cost reduction. It is interesting to note how many challenges we are trying to solve to bring the EUV lithography to bear some fruit, yet not much help is coming from the Academia, perhaps due to the enormous cost of the hardware the universities would need to bear. Maybe it is our community barking at the wrong tree after 50 years of Moore? Who knows. At the very least, we should take any opportunity to work together, and then both the job market and the expertise would come together too.

Table 1. (left) Designed jog width and jog pitch for programmed LER patters for 64nm pitch line/space. (right) Measured jog width and jog pitch. Grey areas are locations that did not resolve on mask and will be omitted in the anlaysis.

| DESIGN											MEASURED										
Jog Pitch 4X (nm)	Jog Width 4x (nm)										Jog Pitch 4X (nm)	Jog Width 4x (nm)									
1000	2	3	4	5	6	8	10	15	20	40	1005±41	2.30	4.57	5.54	6.22	8.23	10.49	12.30	20.40	25.18	50.60
750	2	3	4	5	6	8	10	15	20	40	743.47±8.7			7.14	7.02	4.48	9.71	11.69	18.82	24.46	48.55
500	2	3	4	5	6	8	10	15	20	40	495.53±4.7	2.43	3.69	4.98	4.59	7.07	11.27	12.17	18.59	23.56	49.50
300	2	3	4	5	6	8	10	15	20	40	298.41±2.9	2.64	4.06		4.17	7.45	7.79	10.52	17.06	22.58	46.53
200	2	3	4	5	6	8	10	15	20	40	197.49±2.1	3.13		3.57	5.05	5.30	8.19	9.54	15.33	20.99	44.13
100	2	3	4	5	6	8	10	15	20	40	98.81±0.4			2.82	3.57	3.92	5.32	6.64	8.98	11.97	28.69
80	2	3	4	5	6	8	10	15	20	40	79.22±0.3				2.11	1.94	3.19	4.48	6.57	8.73	18.28
60	2	3	4	5	6	8	10	15	20	40	59.29±0.1							2.04	3.10	4.28	9.21
40	2	3	4	5	6	8	10	15	20	40											
20	2	3	4	5	6	8	10	15	20	40											
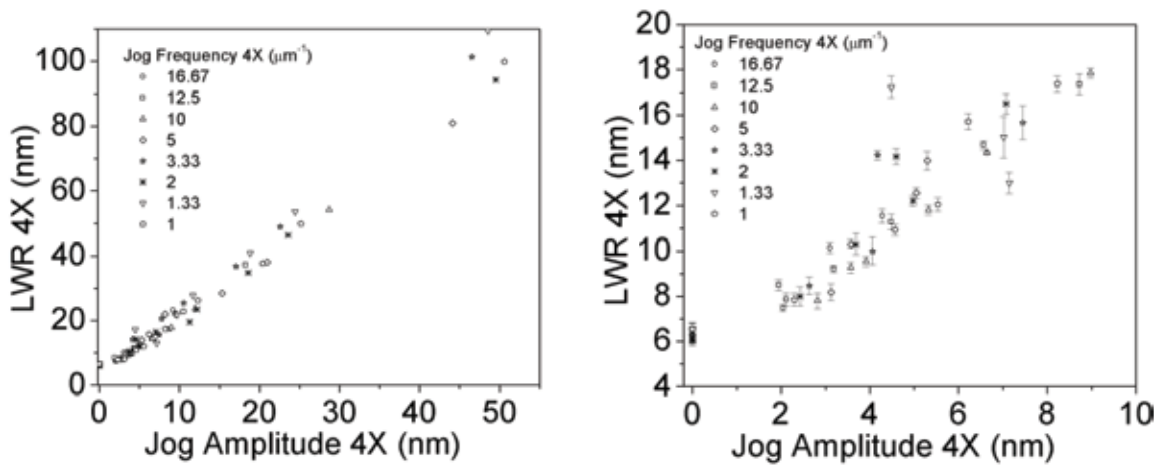
Figure 2. (left) Mask level 128nm HP symmetric programmed LWR measurments correlated to measured jog pitch and jog width from Table 1. (right) Zoomed in including error considerations.

PSD and LWR comparisons and the highest performance resist is used for a comprehensive LER transfer analysis. Wafer LWR is extracted from 64nm and 90nm pitch lines and correlated back to the base mask patterns revealing an empirical LWR transfer function (LTF). Finally, the study is extended to 45nm (1X) pitch lines by deploying a pupil filter on the ADT to explore the effect on LWR as the feature sizes shrink.

1. Introduction

The march towards single digit nanometer nodes requires not only novel device designs but also new lithography advances. The transitions from 193nm DUV to 13.5nm EUV lithography is a necessary step in the coming years to allow the continued scaling of high performance logic devices. With a decrease in feature size, deviations from their nominal critical dimension (CD) will start to have an impact on device reliability and performance. Previous studies on transistor performance have shown that as the magnitude of line edge roughness (LER) increases on the gate, device performance suffers as a result.[1,2] Despite the success that has been seen in reducing LER in resist, there is a continued push to for lower LER that is dominated by

the industry's move towards smaller, more efficient and complex chip designs.

This paper will address some of the factors that contribute to the LER in wafer resist with a focus on contributions from the EUV photomask LER. Section 2 begins with an extensive study on a programmed LER photomask that details the intentional LER variations etched into the absorber. Section 3 describes the use of this mask to screen three EUV photoresists to select the current state-of-the-art resist for this study. In section 4, a quantitative way of relating mask induced LWR to wafer LWR is introduced and an empirical LWR Transfer Function (LTF) is derived for 45nm, 64nm, and 90nm 1X pitch line/space, expanding on previous understandings and simulations.[3,4,5] Lastly, section 5 gives a simulation of mask LWR impact on wafer for future lithography systems and concluding thoughts in section 6. It must be noted that this study will not take into account the mask surface roughness induced LER, only absorber level LER. However, there have been extensive studies regarding surface roughness, as detailed in the references.[6,7] Speckle from the source is also neglected in this study since the source does not have temporal coherence.
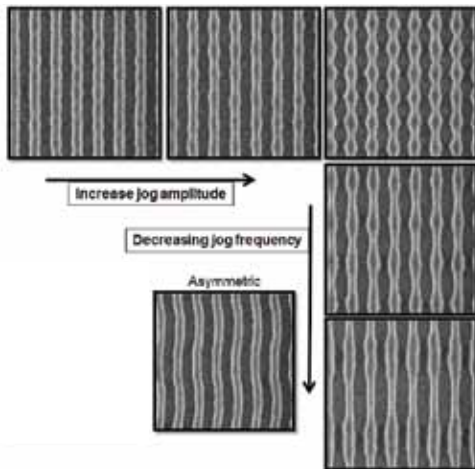
Figure 3. Wafer prints showing the transfer of programmed mask line roughness for various jog amplitude and jog frequency.

Figure 4. LWR comparison between Resist A, B and C at different jog pitch.

2. Programmed Ler Photomask

The EUV photomask was fabricated using a standard 40 layer Mo/Si stack on quartz. LER with varying magnitude and frequency is programmed into 90nm, 128nm, 180nm (4X) half pitch line/space. Figure 1 (left) shows the nomenclature of the programmed LER, illustrating jog amplitude and jog frequency as defined for the symmetric and asymmetric case.

SEM imaging using an Adventest LWM 9045 was used for mask micrographs at 75kx (Figure 1, middle).

Each site on mask is measured using SuMMIT v.10 to extract the raw line data. A sine function is used to fit the raw data and the measured mask jog amplitude and jog frequency is extracted so exact mask features can be quoted when referencing the corresponding wafer prints. Figure 1 (right) is an example of the raw line data and its corresponding fit values. Table 1 shows an example comparison between design and measured programmed LER feature size for 64nm 1X pitch. Small jog pitch and jog amplitudes are not resolved on mask, indicated by the greyed boxes. This signifies a resolution limitation on current ebeam mask writers, which can be noted for further study.

LWR analysis done using SuMMIT v10 follows the same approach by A. Zweber et. al.[8] Results for 128nm (4X) half pitch line/space are shown in Figure 2. It can be noted that LWR increases linearly with jog amplitude, as expected, while LWR stays statistically constant with increasing jog frequency (LWR is frequency independent). When the mask is printed, the projection optics of the lithography system acts as a low-pass filter and attenuates the impact of mask level LER. Frequency filtering can be designated by an f_{min} and f_{max}, in which frequencies above f_{max} should be completely filtered out by the illumination system and frequencies below f_{min} should completely transfer onto the wafer. The intermediate frequencies represent a region of partial frequency transfer. The remainder of this study will deal with extraction of an empirical transfer function to understand, beyond the formula, how mask level LER will impact the wafer.
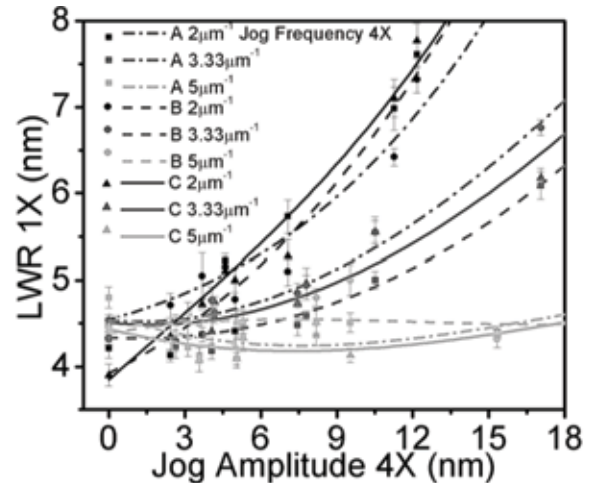
3. Wafer Prints and Analysis

Wafers are printed to explore the impact and transferability of mask level LER. The ASML EUV Alpha Demo Tool (ADT) at Albany NanoTech is the lithography system used for wafer prints. SEM micrographs of the patterned wafers in resist were recorded on the Hitachi CG4000 CD-SEM at 300kx. Before beginning to explore the effects of absorber induced LER on wafer prints, an understanding of the illumination system and resists should be considered. Depending on the resist that is chosen, the transfer function will vary slightly since not all resists are made equal.

One must take note of the varied performance of different chemically amplified photoresist as this will impact wafer prints and the transferability results. This varied performance is understood as the tradeoff between resolution, LER and sensitivity (RLS tradeoff).[9] An evaluation on the various resist is necessary to fully represent the transferability of mask features. Resists that are favorable to LER and resolution will be chosen for subsequent studies. High resolution resists will most honestly represent the features that transfer from mask to wafer while resist with high LER scores will show the best performance for LER optimization.

The illumination system should also be considered for understanding LER transferability. Depending on the lithography tool, the transfer function will depend on the illumination optics, which acts as a high-pass filter. Mask level LER is filtered through the illumination system, defined by an f_{max} and f_{min}, as shown in Equation 1. Considering the ADT illumination settings, mask level LER frequencies above $f_{max}=6.94\mu m^{-1}$ should be completely filtered out while mask level LER frequencies below $f_{min}=2.31\mu m^{-1}$ should completely transfer onto the wafer. The frequencies between $6.94\mu m^{-1}$ and $2.31\mu m^{-1}$ represent a region of partial LER transfer. First, the resist that will represent the
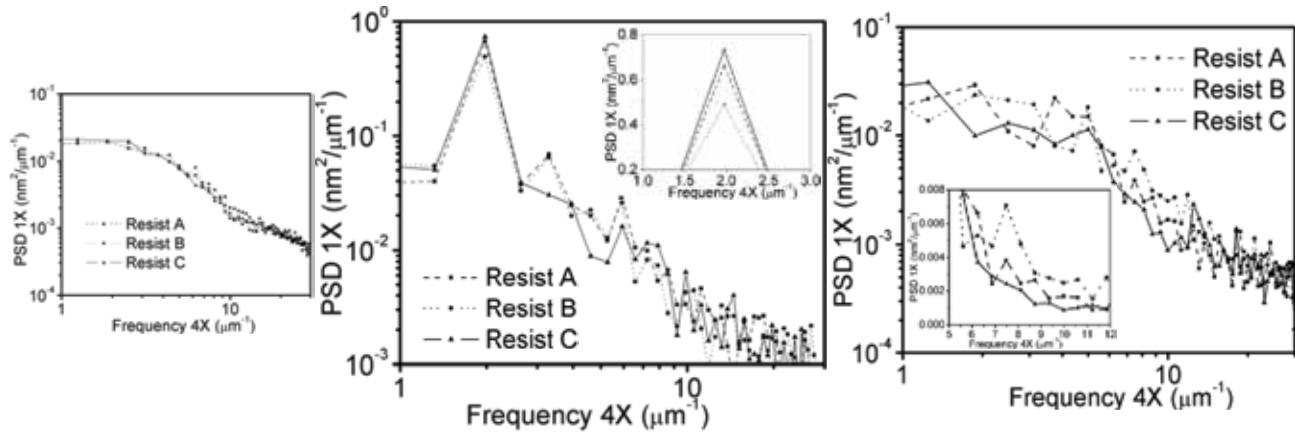
Figure 5. (left) Reference power spectrual density for three resists (middle) Power spectral density comparison of resist A, B and C at 2μm⁻¹ jog frequency and 11.3nm jog amplitude. (right) Power spectral desnity comparison of resist A, B and C at 5μm⁻¹ jog frequency at 9.5nm jog amplitude.

most state-of-the-art EUV chemically amplified resist will first be established.

Three state-of-the-art EUV photoresist, labeled as Resist A, B and C, are explored to establish the optimal resist that will most honestly represent the transferability of mask features. The nominal dose and focus were established for these resists through finding the center dose and best focus dies that matches to expected CD dimensions. Wafer SEM (Figure 3) analysis were done on Terminal PC Offline CD Measurement Software 6.1 to select the optimum die for each resist evaluated.

$$f_{max} = \frac{NA*(1+\sigma_{out})}{\lambda} = 27.78 \mu m^{-1}(1X) = 6.94 \mu m^{-1}(4X)$$

$$f_{min} = \frac{NA*(1-\sigma_{out})}{\lambda} = 9.26 \mu m^{-1}(1X) = 2.31 \mu m^{-1}(4X)$$

Equation 1. Theoretical cutoff frequency for the illumination system. fmax and fmin represents LER frequencies on mask that should either fully transfer ($f_{LER}<f_{min}$), partially transfer ($f_{min}<f_{LER}<f_{max}$), or no transfer ($f_{LER}>f_{max}$) to wafer.

Resist A, B, and C are evaluated by studying the PSD and LWR at three programmed LER frequencies: 2μm⁻¹, 3.33μm⁻¹ and 5μm⁻¹ (4X). Figure 4 represents the LWR as measured on wafer for the three resists at different jog amplitudes and jog frequencies. A 2μm⁻¹ mask LER frequency should completely transfer to wafer (Equation 1) while there is only partial transfer for the 3.33μm⁻¹ and 5μm⁻¹ frequencies. This trend is seen for all three resists (Figure 4). At a fixed jog amplitude, the LWR decreases with increase jog frequency—this represents the line roughness filtering from the ADT.

Concentrating solely at the 2μm⁻¹ frequencies for the three resists, Resist C shows the lowest LER at zero jog amplitude (reference) but the LWR increases beyond Resist A and B at higher jog amplitude. From a resolution, LER, sensitivity (RLS) tradeoff standpoint, the resist with the lowest LWR at reference is the resist with the best LER performance (Resist C). As the jog amplitude increases at this frequency, it is

expected that the LER is completely transferred from mask to wafer. Resist C (solid line) has consistently higher LWR compared with Resist A and B at larger jog amplitudes. We can expect relatively higher LWR from the resist that has the highest resolution at 2μm⁻¹ since the jog amplitude is completely transferred to the wafer. To verify this, the resist that has the highest increase in power spectral density (PSD) at the set programmed frequency when compared to the reference should represent the resist with the best resolution—this is due to the most honest representation of frequency transfer. The higher PSD peak at 2μm⁻¹ for Resist C compared with Resist A and B (Figure 5, middle) can be attributed to the higher resolution performance from Resist C. Also, this can be correlated back to Figure 3, which indicates that the consistently higher LWR for Resist C is due to the higher PSD at 2μm⁻¹—Resist C has the best resolution performance out of the three wafer resists.

High spatial frequencies on the other hand have diffraction orders that are not collected by the pupil thus will not be transferred into the resist. The resist with the lowest PSD and LWR at nontransferable or barely-transferable frequencies represent the resist with best LER performance. Across the board, lower LWR for Resist C (solid line) at 5μm⁻¹ represents the better performance LWR resist. The PSD at 5μm⁻¹ strongly shows an overall lower PSD and thus suppression of mask level LER—Resist C has the best LER performance out of the three wafer resists.

4. Mask to Wafer: Transfer Properties
LWR is extracted from 128nm (4x) half pitch (HP) features on wafer using SuMMIT v.10 analysis on wafer SEM micrographs. The wafer LWR values are then correlated back to the mask location that was used to create the wafer print. Figure 6 (left) shows the frequency dependence of the mask line roughness on wafer LWR. The linear correlation of mask LWR vs jog frequency (Figure 2) is broken by the lithography system—higher frequencies on the mask are filtered out while lower frequencies are transferred. Solid lines represent mask line roughness frequencies that
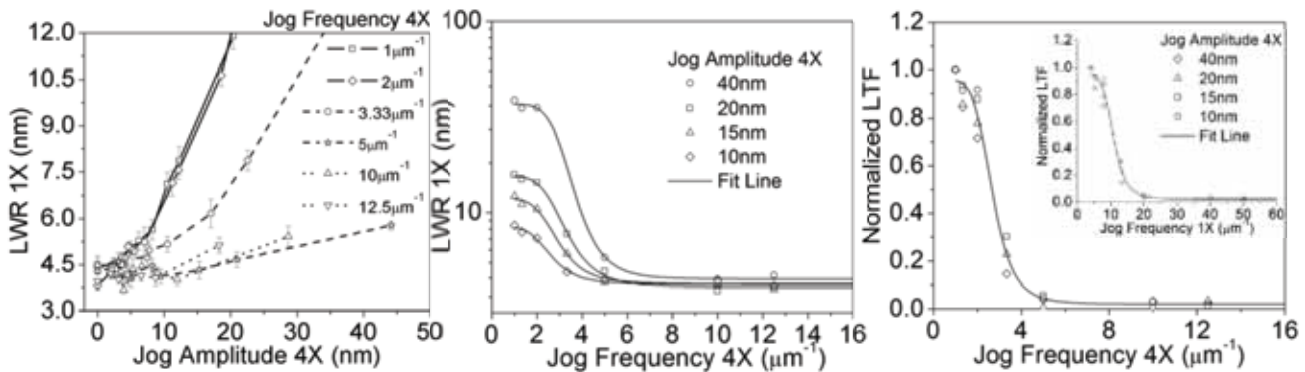
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Figure 6. (left) Impact of varying mask LER frequencies on wafer prints as a function of mask LER amplitude. (middle) LWR as a function of jog frequency. (right) Transfer function for 128nm HP line/space on mask. Inset shows the LTF as a function of 1X jog frequency.
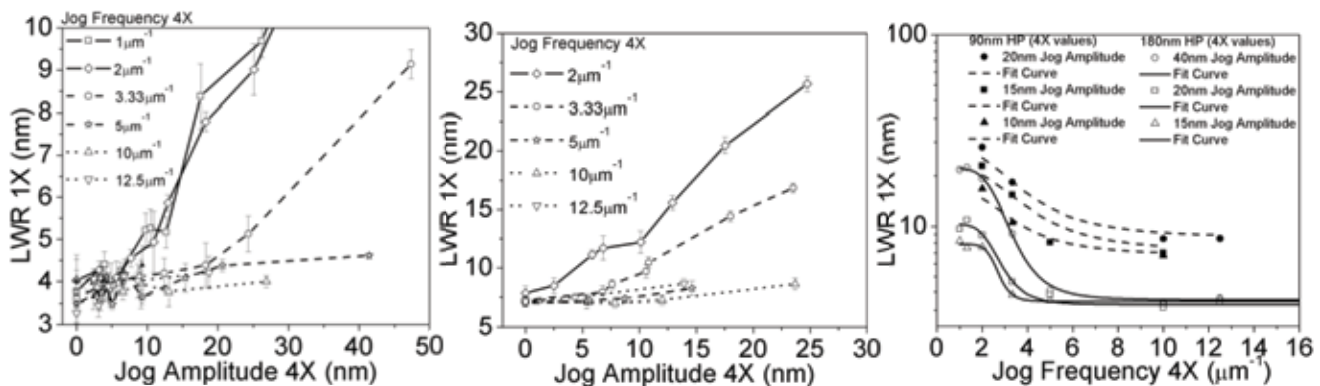

Figure 7. (left) Wafer level LWR as a function of mask jog amplitude and varying mask LER frequency for 180nm HP 4X. (middle) A top-hat σ=0.5 pupil filter extends the study to 90nm HP 4X. Baseline LWR increases due to a feature size shrink enabled by the pupil filter. (right) LWR as a function of jog frequency for the two pitches.

should transfer completely from mask to wafer. Dashed lines represent frequencies that are between f_{max}=6.97μm^{-1} and f_{min}=2.94μm^{-1}, thus should only partially transfer. Dotted lines represent frequencies that should be completely filtered by the illumination optics. This expected trend is seen, however it can be noted that even at frequencies >f_{max}, large jog amplitudes will still impact wafer LER—this can be seen as the reduction of the image-log slope (ILS) from the effects of shadowing. Figure 6 (middle) represents the LWR dependence on programmed jog frequency. The larger the amplitude, the sooner the LWR begins to impact wafer and the saturation LWR is also larger. However, when the LWR is normalized, the relative LWR impact on wafer falls together, revealing an empirical transfer function for the ADT (Figure 6, right). This normalized LWR is independent of jog amplitudes, representing the pure frequency impact of mask level LER on wafer. From this result, it can be concluded that mask line roughness frequencies above 6μm^{-1} (4x) do not have a major impact on wafer for this illumination and resist system.

Similar to the 128nm (4X) HP case, the study can be expanded to 180nm HP where a similar trend can be seen

(Figure 7, left). Moving towards a smaller feature size, use of a blocking filter in the pupil plane of the projection optics extends this study to 90nm HP (Figure 7, middle), where the filter has been optimized for this particular feature.[10] Baseline LWR increases due to a feature size shrink enabled by the pupil filter. When plotting the LER frequency dependence of both 90nm HP and 180nm HP line/space, the shift of the baseline LWR for the pupil filter exposure becomes apparent (Figure 7, right). Similar to the 128nm HP, an increase in jog amplitude, the saturation LWR at low frequency becomes larger.

Normalizing the LWR reveals the impact of mask level line roughness beyond the baseline LWR. The 128nm HP LWR Transfer Function (LTF) is similar to the 180nm HP LTF while the transfer function for the 90nm HP is shifted to the right (Figure 8). The similarity between the 128nm and 180nm HP LTF represents the line/space pitch independence of mask LWR tranfer to wafer. However, when a pupil filter is used to print 22.5nm 1X HP lines on wafer, there is a shift in the transfer function. This is likely because the filter, by blocking low frequency rays, causes the imaging to result from a larger ratio of higher vs. lower diffraction orders.
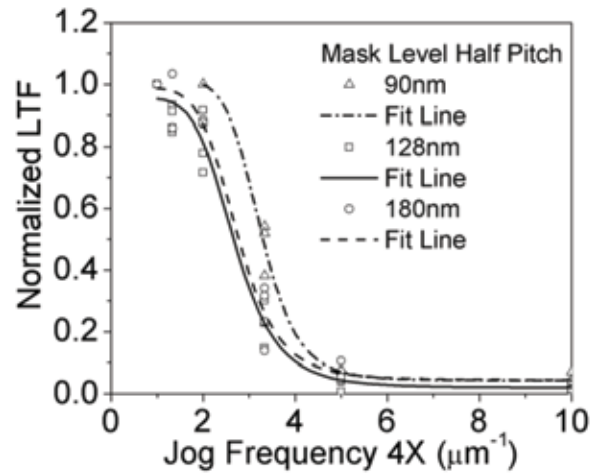
Figure 8. The relative impact on wafer becomes independent of mask level LER amplitude. This reveals an empirical LWR transfer function for the ADT with and without a pupil filter.
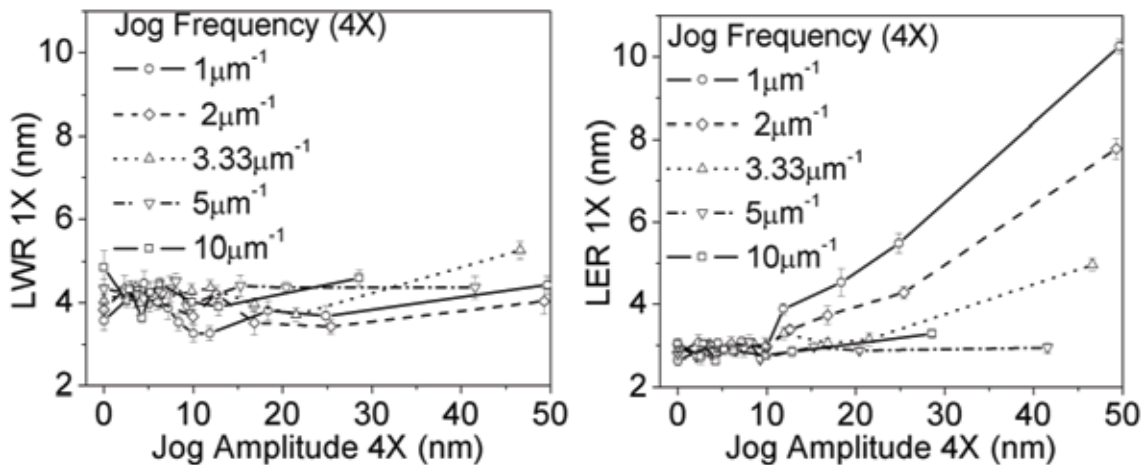

Figure 9. 128nm HP 4X lines with programmed asummetric LER. Asymmetric line variations on mask does not impact wafer LWR. This is due to the constant line width that is transferred onto the wafer. However, an identical look at the LER reveals the full impact on wafer.

This enables the printing of smaller features, however it simultaneously resolves higher frequency mask roughness. In summary, the transfer function is independent of jog amplitude and line/space pitch. Freqeuncies above 6µm^{-1} on mask will begin to impact the LWR on wafer. Deploying a pupil filter to print 22nm HP 1X lines shifts the LTF to the right, representing a greater influence of high frequency mask line roughness on wafer LWR.

A further study on 128nm HP 4X lines with programmed asymmetric LER shows the need to also consider both mask LER and LWR (Figure 9). In this case, the wafer LWR is constant throughout jog frequency and jog amplitude. This is due to the constant line width that is transferred from an asymetric programmed LER mask feature to wafer. However, the wafer LER shows the expected increase in LER as a function jog amplitude. Thus, an understanding of mask LER in conjunction with mask LWR is necerssary to reveal the full influence of mask line roughness on wafer.

5. Simulations

In consideration for next generation EUV lithography systems, two different illumination optics are simulated to understand when the onset of LER transfer will being for future tools. Figure 10 shows a simulation that looks at two different metrology points (MP1 and MP2) which vary in CD while measuring the image log slope as a function of LER pitch. At a certain frequency, the measured ILS becomes different for the two different metrology points. This can be seen as the onset of LER transfer from mask to wafer. For NA=0.25, the point at which the ILS bifurcate is around
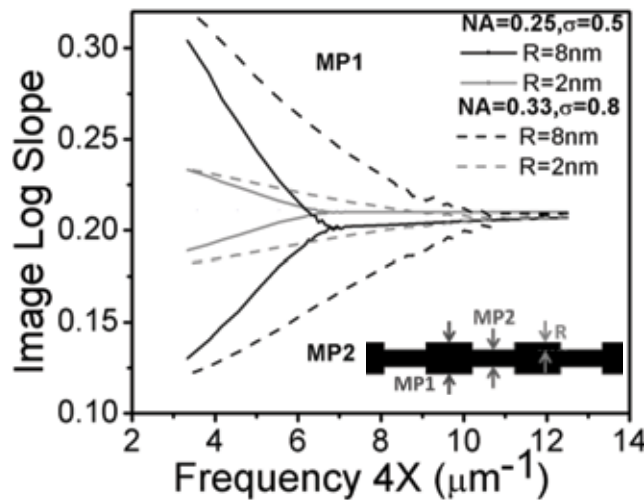
Figure 10. ILS as a function of LER frequency as simulatued using two tool and illumination settings.

$6\text{-}7\mu m^{-1}$. In contrast, for NA=0.33, the bifurcation begins at a higher frequency ($\sim 11\mu m^{-1}$). As the industry moves to higher NA/σ systems, the minimum achievable resolution also increases along with the ability to capture higher frequency patterns. To ensure that the mask line roughness does not impact wafer, a continued study on LER transfer for future lithography system is needed.

6. Summary

The correlation between mask LWR and wafer LWR is explored. The increasing complexity of advanced lithography systems directs the mask maker to not only consider the photomask but also the lithography tool and wafer resist for a complete understanding of mask impact and transferability to wafer. The study begins by looking at an EUV photomask with programmed line roughness. The measured LWR on mask is independent of jog frequency and increases linearly with increasing jog amplitude. The lithography system and wafer resists are now taken into account for a comprehensive understanding of line roughness transfer. Wafer resist evaluation is performed using the same programmed LER photomask through PSD and LWR comparisons. Three chemically amplified EUV photoresists were screened and one was chosen to represent the state-of-the-art, to be used for this study. LWR is extracted from the printed wafers for 32nm and 45nm HP (1X) for varying jog frequencies and jog amplitudes. A direct mask to printed wafer analysis shows that mask line roughness with frequencies above $6\mu m^{-1}$ do not have a major impact on wafer—this result is independent of line pitch and LER amplitude. Using a pupil filter, the study is extended to 22.5nm HP (1X), revealing increased sensitivity to higher frequency mask level LER. An empirical LWR Transfer Function is extracted for 22.5nm, 32nm, and 45nm HP (1X) line/space, showing the impact of mask level line roughness on wafer prints. Finally, simulation is used to understand future lithography systems. With an increase in NA and sigma, LER transferability is expected to occur at higher frequencies - this should be taken into consideration for future EUV photomask fabrication.
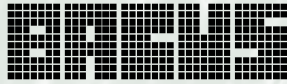
6. Acknowledgments

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Industry Briefs

■ Fabless Firms Outperform IDMs in 2012, says IC Insights

Digitimes

Combined sales generated by fabless IC companies worldwide increased 6% in 2012, while those by IDMs decreased 4% year on year, according to an IC Insights report. Overall revenues generated by the global semiconductor market saw a 2% decline in 2012. Fabless IC companies have outperformed IDMs every year since 1999, except for 2010, when IDMs as a group enjoyed a sales rise of 34% while fabless firms had growth of 29%. Fabless IC companies represented 27.1% of the global semiconductor market in 2012, reaching their highest level in history, IC Insights said.

In 1999-2012, fabless firms' revenues have been growing at a 16% CAGR, while IDMs have grown a modest 5%, IC Insights indicated. IC Insights forecast that in 2017, fabless IC companies will have 'at least' 33% of the global semiconductor market. More companies are expected to become fabless over the next five years, such as IDT, LSI Logic, Agere and AMD, IC Insights said.

■ TSMC December Sales Down 16%

Jessie Shen, DIGITIMES

December sales at Taiwan Semiconductor Manufacturing Company (TSMC) declined by 16% sequentially, the lowest level in nine months. TSMC has announced consolidated revenues of NT$37.11 billion (US$1.28 billion) for December 2012, down 16.1% on month but up 18.8% on year. Consolidated sales for the fourth quarter of the year totaled NT$131.31 billion, down about 7% sequentially but coming slightly above the company's guidance of NT$129-131 billion.

TSMC chairman and CEO Morris Chang previously predicted that the company would report revenue dips sequentially for the fourth quarter of 2012 and first-quarter 2013. However, sales would rebound to growth following two quarters of decreases, Chang said. TSMC's consolidated revenues climbed to an all-time high of NT$506.25 billion in 2012, up 18.5% on year. Chang forecast in late-2012 that TSMC would enjoy another sales growth of 15-20% in 2013.

■ Samsung Expects Another Quarter of Record Profits

Digitimes

Samsung announced its financial guidance for Q4'12, with operating profits set to hit a new record high for a fifth consecutive quarter. Samsung estimates Q4 operating profits at between KRW8.6T (US$8.1B) and KRW9T, compared with the KRW8.12T reported for Q3. Samsung credited revenue growth for Q3'12 to increased sales of handheld phones and stronger demand for display panels.

■ Globalfoundries Hints at $10-billion Fab Location

Peter Clarke, EETimes

Foundry chip maker Globalfoundries Inc. is planning to invest $10 billion in a next-generation wafer fab possibly next to its existing Fab 8 in upstate New York, according to local reports quoting CEO Ajit Manocha. He also said that the previously announced creation of a $2-billion R&D center next to Globalfoundries' Fab 8 in Malta, New York, will bring the company closer to investing $10 billion in a next-generation wafer fab, the reports said.

The recently-announced $2-billion Technology Development Center (TDC) at Globalfoundries campus in upstate New York, is intended to support manufacturing process node transition and R&D around interconnect and packaging for the 3-D stacking of chips, advanced mask-making and the use of extreme ultraviolet lithography. Construction is expected to start early in 2013 and be completed late in 2014. The spending will bring the total capital investment at the Fab 8 campus to more than $8 billion and direct employment up to about 3,000 people.

■ Tablet Sales to Outpace Notebooks

Dylan McGrath, EETimes

More than 240 million tablet PCs are expected to ship in 2013, easily exceeding the 207 million notebook PCs projected to ship during the year, according to market research firm NPD Group DisplaySearch (Santa Clara, Calif.). The tablet shipments are projected to grow 64 percent in 2013 compared to 2012, DisplaySearch said. By 2017, the firm expects that the number of tablets sold will exceed the number of notebooks sold by nearly three to one.

DisplaySearch also predicts that in 2013 a new class of smaller tablets with screen sizes of 7 to 8 inches will account for about 45 percent of the tablet market, roughly 108 million units. Tablets with screen sizes of about 10 inches will account for about 17 percent of the market, or about 41 million units, according to the firm.

China, which in 2012 was the second largest tablet market in the world, is expected in 2013 to account for about 27 percent of the tablet market, or 65 million units. North America is expected to remain the No. 1 tablet market in the world, accounting for about 35 percent of the market or 85 million units in 2013, DisplaySearch said.

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Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

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Calendar

2013

❋ **SPIE Advanced Lithography**

24-28 February 2013
San Jose Convention Center and
San Jose Marriott
San Jose, California, USA
www.spie.org/al

❋ **SPIE Photomask Technology**

10-12 September 2013
Monterey Marriott and
Monterey Conference Center
Monterey, California, USA
www.spie.org/pm

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You are invited to submit events of interest for this calendar. Please send to lindad@spie.org; alternatively, email or fax to SPIE.