PHOTOMASK

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First Place
Best Poster Award

Mask Process Correction (MPC) modeling and its application to EUV mask for Electron beam mask writer, EBM-7000

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ABSTRACT

In electron beam writing on EUV mask, it has been reported that CD linearity does not show simple signatures as observed with conventional COG (Cr on Glass) masks because they are caused by scattered electrons form EUV mask itself which comprises stacked heavy metals and thick multi-layers. To resolve this issue, Mask Process Correction (MPC) will be ideally applicable. Every pattern is reshaped in MPC. Therefore, the number of shots would not increase and writing time will be kept within reasonable range. In this paper, MPC is extended to modeling for correction of CD linearity errors on EUV mask. And its effectiveness is verified with simulations and experiments through actual writing test.
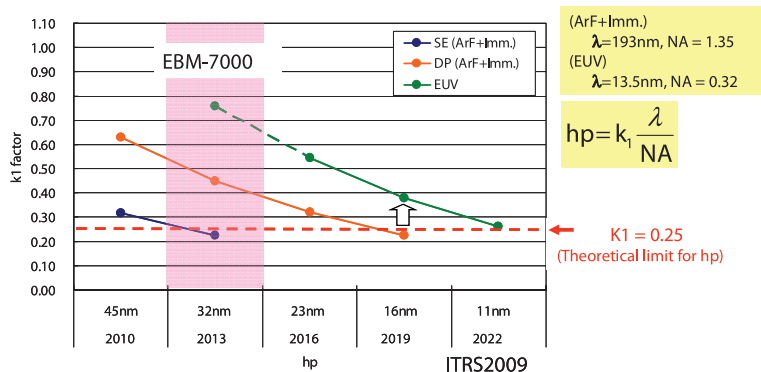
$hp = k_1 \dfrac{\lambda}{NA}$

(ArF+Imm.) λ=193nm, NA = 1.35
(EUV) λ=13.5nm, NA = 0.32

K1 = 0.25 (Theoretical limit for hp)

Figure 1. Lithograph outlook in near future.

TAKE A LOOK INSIDE:

SPIE

EDITORIAL

ML2 Funding – Where are the Users?

Peter D. Buck, Toppan Photomasks, Inc.

The Mask-less Lithography special session at the recent Photomask Symposium in Monterey, CA, while perhaps an ironic focus for a conference dedicated to photomask technology, provided yet another opportunity to ponder the economic forces that drive technology development in the integrated circuit lithography industry. Replete with the prerequisite historical talks about the past golden age of mask-less lithography at IBM, the snail's pace progress of the various tool development programs, the as yet unanswerable questions about shot noise limitations, and the manufacturing scenarios narrowly defined to meet the limitations of each specific tool, the most interesting and perhaps most crucial point in the session was when Bert Jan Kampherbeek of MAPPER was asked how much MAPPER had spent so far and how much more was required to bring a manufacturing tool to market. The context of the question was the lament that if only a small fraction of the money spent on EUV were to be spent on ML2 it would be possible to catch up with the ITRS roadmap and be a mainstream lithography solution. Bert Jan remarked that they had already spent around 100M€. Discussion ensued and it was suggested another 300-400M€ would be needed to complete the job. I thought about this for awhile, then reread the paper I presented with Franklin Kalk and Charlie Biechler at the 2007 Photomask Symposium entitled "A Maskmaker's Perspective on Maskless Lithography" in which we presented a use model along with an economic model that defined the investment limit to produce a tool to serve that market. Our use model was ASIC prototyping. Please read the paper for the details, but our conclusion was that the industry only had about $100M to spend to serve this use model and that it was unlikely that a manufacturing tool would be available before at least 2010. It is now the end of 2010, the $100M has been spent and still no tool exists.

Ponder the difference between EUV and ML2 and one characteristic stands out – EUV has a very well-defined use model while ML2 does not. EUV is focused on economic production of DRAM, and it is DRAM manufacturers who have demonstrated the most interest in EUV. Over time, as EUV introduction has been delayed, microprocessor manufacturers have also become more interested but DRAM is still the driving force. ML2, on the other hand, has many proposed use models: low volume manufacturing, lower cost prototyping to enable design innovation, contact layer printing, part of a double patterning strategy and others. Some of these proposed use models already have alternate solutions: low volume manufacturing is available through shuttle runs and multi-project masks, for example. While masks may contribute to prototyping costs, the cost of design and design verification cannot be ignored as major cost drivers. In addition the bulk of design still happens at technology nodes from 130 nm and above where mask and wafer manufacturing prices are already low.

Lloyd Litt, speaking for SEMATECH, proposed a ML2 funding consortium. I wonder if the first task should be to validate the proposed ML2 use models. This would focus ML2 development on real industry needs as well as identify who would benefit from (and therefore should pay for) ML2.
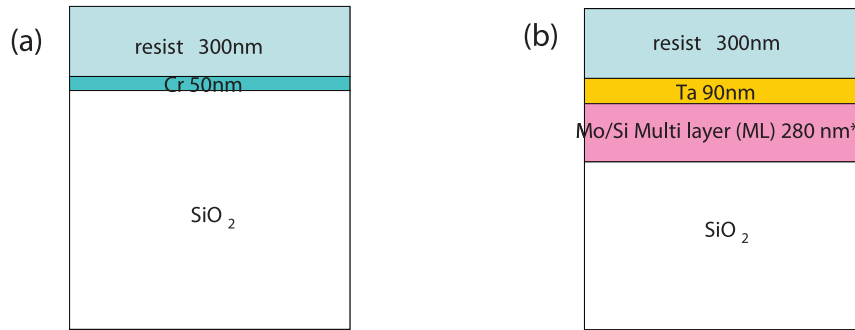
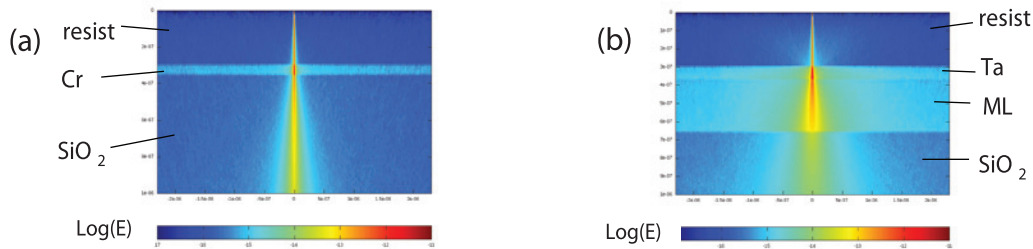Figure 2. Substrate setups (a) COG and (b) EUV for Monte Carlo simulation

Figure 3. Monte Carlo simulation results, deposited energy distributions as 2D contour map for (a) COG and (b) EUV.

Table 1. Linearity and sub-resolution requirement in ITRS2009

	Year	2013	2016	2019	2022
	DRAM hp [nm]	32	23	16	11
Optical	Sub-resolution [nm]	56	40	28	20
	Linearity [nm]	5.1	3.6	2.5	1.8
EUV	Sub-resolution [nm]	78	55	39	28
	Linearity [nm]	4.8	3.4	2.4	1.7

1. Introduction

1.1 Background

Semiconductor scaling is continuously pursued to fabricate lower power and higher performance devices. One of the lithography technologies strongly following this trend is EUV to take advantage of its short wavelength, although EUV lithography still has such issues as light source, defect free blanks and defect inspection to be overcome to be used for production. In parallel with the efforts of resolving these issues, it is to be noted that the difficulties in patterning with minute feature sizes like hp 23nm/16nm are getting significantly important, requiring extremely high accuracy.

CD linearity of EUV mask, written by electron beam mask writer, does not have simple signatures like the conventional COG (Cr on Glass) masks do. Such a symptom is caused by scattered electrons form EUV mask itself which comprises stacked heavy metals and thick multilayers.[1]

EB mask writer, EBM-7000[2], has certain functions to compensate for pattern/CD errors incurred by proximity effect, fogging effect and loading effect with dose modulation. It is assumed that those effects have several dozen um to a few mm in their impact length. On the contrary, range of scattered electrons of EUV mask is a few um or less. Therefore, even if those functions are applied to suppress errors of CD linearity on EUV mask, accurate correction will not be achieved within allowable time because of in-adequate calculation grid sizes. They should be 1/100 -1/10 smaller for EUV

mask. Also, every pattern should be divided into small shot sizes to fit the gird sizes to which respective dose settings are assigned to meet high accuracy. Then, the number of shots will increase substantially to cause the writing time so long.

To overcome this issue, Mask Process Correction (MPC) will be ideally applicable. This technology was already presented for correction of CD non-linearity on COG mask.[3][4][5] Every pattern is reshaped for correction in MPC. Thus, it is expected that the number of shots would not increase maintaining the writing time within the reasonable range. In this paper, MPC is extended and applied to modeling to correct CD linearity errors on EUV mask. And its effectiveness is verified by simulations and experiments through actual writing test. These results will be reported.

1.2 Linearity target for EUV lithography

Figure 1 shows required k1 factors for respective hp generations in optical/EUV lithography. The k1 factor is now getting close to a virtual limit of 0.25 for resolving pre-hp 32nm generation pattern (1:1 L/S pattern) with single exposure (SE) of ArF (193 nm wave length). Then, double pattering (DP)[6] is becoming one of the most promising candidates to cope with the current situation. But even with DP technique, k1 factor less than 0.25 will be required in hp16nm or beyond. It does mean that DP is not applicable in those generations. Therefore, EUV lithography is expected to overcome the situation.

Figure 2 shows linearity and sub-resolution requirements for mask in the International Technology Roadmap for Semiconductors (ITRS) 2009.[7] Linearity is defined as maximum deviation between mask "Mean-to-Target" for a range of features of the same tone and different design sizes. This includes features that are equal to the smallest sub-resolution assist mask feature and up to three times the minimum wafer half-pitch multiplied by the magnification. According to descriptions, linearity accuracy of 2.4nm is required for the range of CD size of 39nm to 192nm for hp16nm generation on EUV. But patterns smaller than 70nm (especially, LS patterns) are not resolved well to be measured with CD-SEM because of resist collapse, process blur, etc., therefore, 70nm~1200nm patterns are studied in this paper.
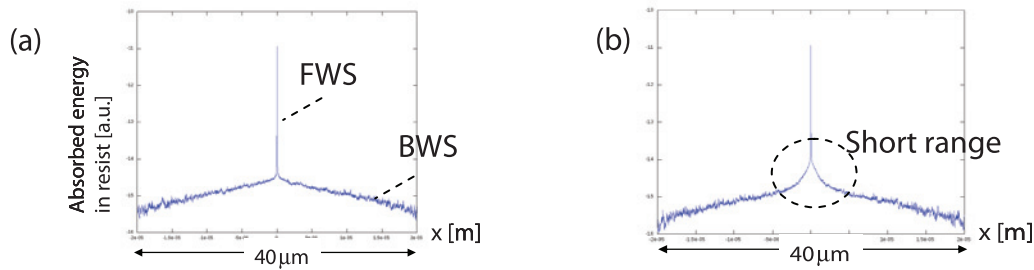
(a)

(b)

Figure 4. Absorbed energy profiles in resist (PSF) for (a)COG and (b) EUV.
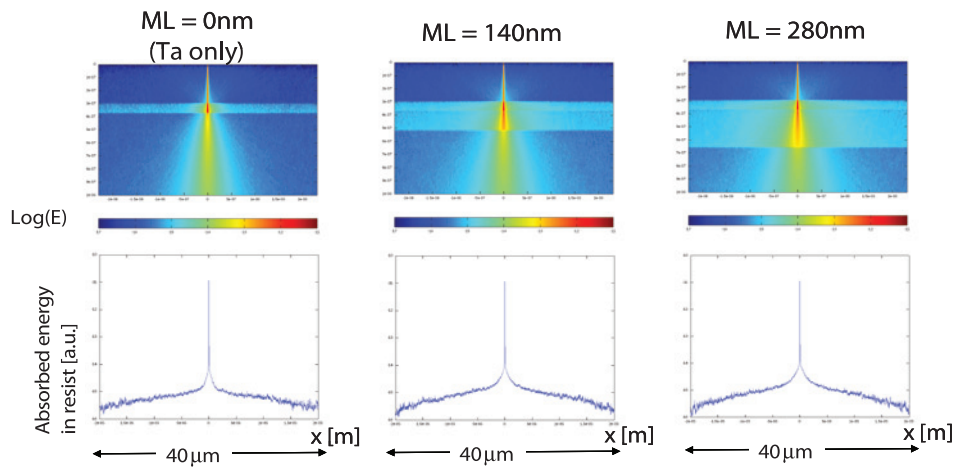
ML = 0nm
(Ta only)

ML = 140nm

ML = 280nm

Figure 5. Deposited energy distributions as2D contour map and PSF for various ML thicknesses.

2. EUV Short Range Effect in EB Write

2.1 Monte Carlo simulation

EUV substrate consists of heavy metals like Ta and Mo. Backscattering of electrons seems to be fairly larger than Cr on Glass (COG) or Halt-tone (HT) substrates. And it may incur unexpected influence to Proximity effect correction (PEC). In this regard, point spread function (PSF) in EUV is estimated with Monte Carlo simulation. PSF of normal COG is also calculated for comparison. Set-ups of substrates are shown in Figure 2 (a) COG and (b) EUV.[8][9] A traditional/classical, continuous energy slow down model was used in simulation. Figure 3 (a) and (b) show simulation results of both COG and EUV as 2D contour maps of deposited energy in substrates. Wider spread profile with much higher intensity is observed in EUV substrate, especially, in Ta layer and Mo/Si multilayer. Absorbed energy in resist area which is defined as PSF is also estimated. It is obtained with accumulation of the energy along z-direction in resist area. This absorbed energy profile in resist actually determines pattern sizes and shapes. In COG substrate, forward scattering (FWS) and backward scattering (BWS) distributions are observed, and generally defined with double Gaussians as shown in Figure 4 (a). FWS and BWS radius are about 10nm and 10µm respectively. On the other hands, short range scattering is observed in EUV substrate, in addition to double Gaussians like COG case. Its radius is about 1µm. This is shown in Figure 4 (b).

2.2 Multi layer dependency of short range scattering

Monte Carlo simulations are additionally conducted for various thicknesses of Mo/Si multi-layers (ML) to investigate characteristics of short range scattering. Figure 5 shows the results for ML thickness, 0nm (Ta layer only, no ML), 140nm (half) and 280nm (normal). 2D contour map and PSF are shown. Short range scattering increases with thickness of multilayer. And another important point is that short range scattering is already observed in only Ta layer without ML.

Quantitative comparisons of PSFs for EUV with several ML thicknesses and COG are estimated. The profiles in radial component are shown in Figure 6 (a). Obviously, short range scatterings are only observed for EUV and the intensity increases with ML thickness. The profiles of short range scattering are well fit with A*exp(-x/σ) functions.[1] Then, their radius σ and short range energy ratio A were estimated as shown in Figure 6 (b). The short range energy ratio is normalized with ML thickness of 0 nm. The radius is about 0.28µm for EUV without ML, it is increased linearly and then reaches about 0.39 µm for normal EUV with 280nm ML thickness. The short range energy ratio is about 2 ?large in normal EUV, compared to the one without ML.

2.3 Dose margin & linearity

EUV short range scattering induces degradation of EB dose margin. Figure 7 shows the comparison of dose margins between COG and EUV. The dose margin is defined as derivative of CD
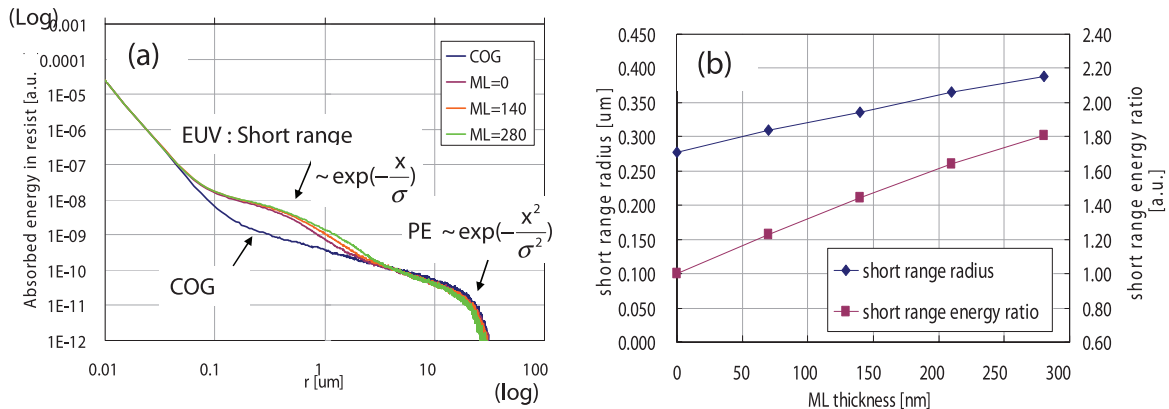
Figure 6 (a) Absorbed energy profiles in resist (PSF) for COG and EUV with various multilayer thicknesses, (b) Short range/short range energy ratio dependency with EUV ML thickness
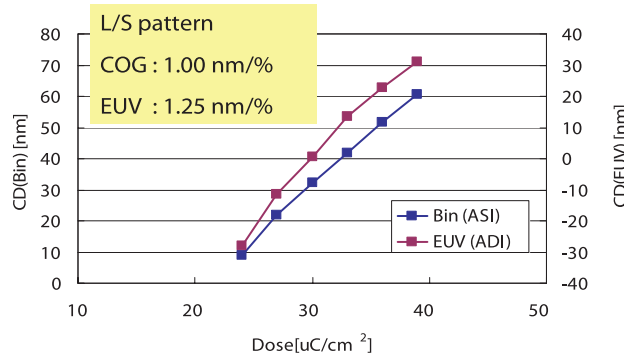

Figure 7 Dose margin comparison between COG and EUV.

with exposure dose. The dose margin is about 25% worse for EUV masks than COG because of short range scattering effect.

Figure 8 shows linearity of (a)Half tone (HT) and (b) EUV. HT linearity was evaluated after resist stripping process (ASI)(PMJ2010). EUV linearity was done after development process (ADI) because etching process is currently not well defined. EB writer evaluation pattern which is known as through-pitch pattern was used (Please see sec.3-2). Both process/dose conditions were adjusted to iso-focal which dose not induce CD error in defocusing. This is carried out with LS patterns (50 % pattern density) which have 350nm designed CD size. The signatures of linearity are different for respective substrates. HT case has comparably normal signature of linearity. CD errors increases in negative direction along with designed CD sizes, meaning measured CDs get narrower. PEC error is small and less than 1nm. CD errors of EUV are spread among local patterns/densities in the region of designed CD size less than 0.5μm which is close to the short range scattering radius. This implies short range scattering effect for EUV linearity. But generally, short range scattering should induce much degradation of linearity, i.e., CD error should be larger in negative direction. The actual linearity of EUV looks opposite. (Linearity of EUV was checked in ASI once. Then, the signature is mostly same as the one shown in ADI, although ASI evaluation is still to be conducted.) This means that the linearity signature is not well described only with short range scattering.

Figure 9 shows linearity signature changes with PEB temperatures. This evaluation was done with COG at ASI. LS patterns

which have designed CD sizes of 100nm-650nm are measured under two conditions of PEB temperatures, 110°C and 120°C. (EUV PEB temperature is set between 110 and 120.) As shown in the figure, linearity signatures change with PEB temperatures. Thus, process or resist characteristics should be taken into account to well understand linearity. It does mean that linearity is not only defined with absorbed energy profile in resist but also process conditions.

For these complexities, empirical MPC model which parametrically correct such linearity is quite efficient.

3. EUV Mask Process Correction (MPC)

3.1 MPC evaluation flow
Figure 10 shows the evaluation flow of Mask Process Correction. MPC gauge patterns were first written and measured in 1st step. EBM-7000[2] was used for EB write. In 2nd step, model calibration was done on Tachyon (Brion technology) which is the computer system including many processing units. After this, patterns are corrected with MPC+ system/software on Tachyon. The MPC+ model pixel size was 32nm in 4x scale to target the line width larger than 70nm. The original GDS data and the corrected GDS data by MPC+ were fractured, converted to VSB12 using a 0.1nm address unit and was input to EBM-7000. MPC gauge patterns and EB writer evaluation pattern are used for the correction.

This evaluation is carried out on resist measurement because etching process is currently not well defined. In this paper, residual errors which are defined as "measured data – modeling data" are
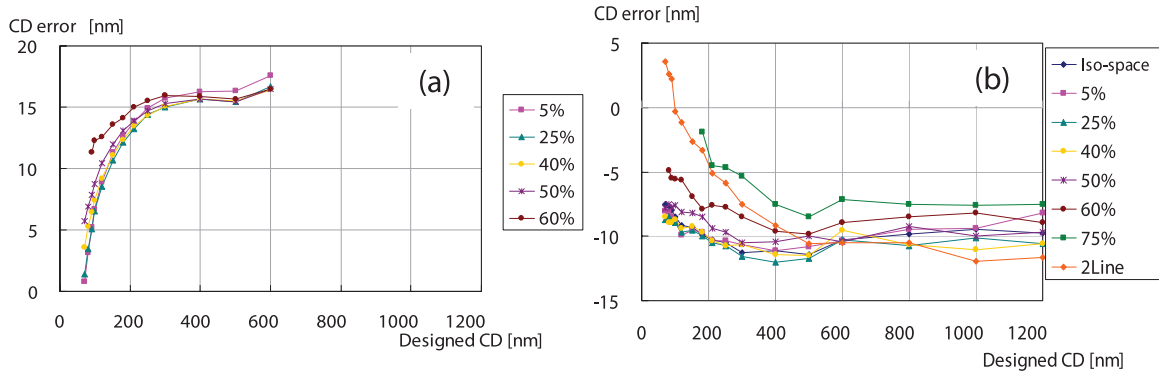
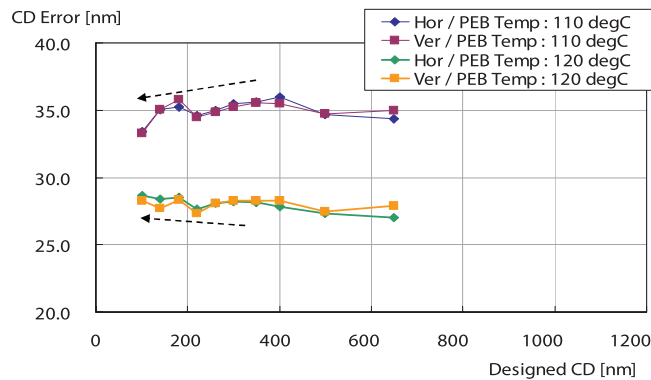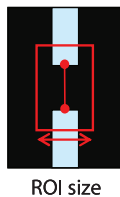Figure 8.Linearity of through-pitch pattern for (a) Half tone and (b) EUV

Figure 9.Linearity changes with PEB temperatures

Table 2.CD-SEM measurement conditions

ROI size

No.	Chip Name		Pattern Type	ROI Size	Measurement Number for Averaging	Comment
1	Test chip	Linearity	1D	1.5um	5	Used for model calibration and evaluation
2		Through Pitch	1D	1.5um	5	
3		Butting	2D	0.1um	5	
4	Mask writer evaluation chip		1D	1.5um	5	Used for MPC+ evaluation only

estimated to check the modeling accuracy. The 3rd step evaluation including writes of patterns corrected with MPC + was abbreviated.

3.2 MPC gauge pattern & EB writer evaluation pattern

Figure 11 (a) shows a layout used for this evaluation. There are MPC gauge patterns, EB writer evaluation pattern and PEC check patterns. PEC check patterns are used to see if proximity effect correction is accurately done with isolatedspace, LS patterns and 2Line patters which have a fixed designed CD size of 400nm. MPC gauge patterns shown in Figure 11 (b), (c) and (d) are used for model calibration on MPC+. These are not only 1D patterns including various CD sizes, Clear CD, Dark CD and different pitches to vary pattern densities but also 2D pattern (Butting) to add some influences of pattern edge morphology. EB writer evaluation patterns are shown in Figure 12. It consists of well known through-pitch patterns, isolated space and 2line patterns.

3.3 Measurement condition

To achieve an accurate evaluation, the metrology technique is significantly essential. The CD-SEM, KLA LWM9000, was used. Its measurement repeatability is smaller than 0.5nm and the number of scan lines is 4096 in each field of view (FOV). The Region of Interest (ROI) size is 1.5um. The Field of View (FOV) is 1.75um at magnification of 75,000 (70 - 1200nm design width). An ROI of 0.1um was used only for butting (2D) patterns, because it is hard to assure multiple ROI in 2D pattern. Measurement conditions are also summarized in Table 2.

3.4 MPC modeling results

MPC+ modeling results are shown in Figure 13. Blue lines indicate original measurement data and red lines are MPC modeling data. Additional density terms for modeling new e-beam effects from EUV mask substrate are applied, compared to HT/COG model.[3] With these terms, MPC+ model well captures the EUV mask linear-
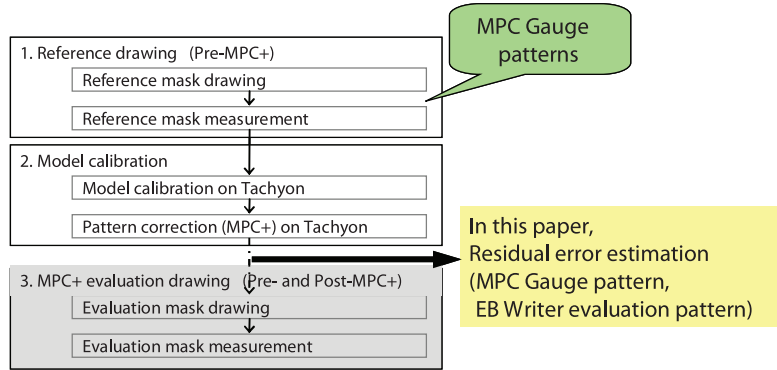
Figure 10.MPC evaluation flow.

L1 = 70nm - 1200nm

P1 = 60nm - 400nm

P2 = 60nm – 1200nm
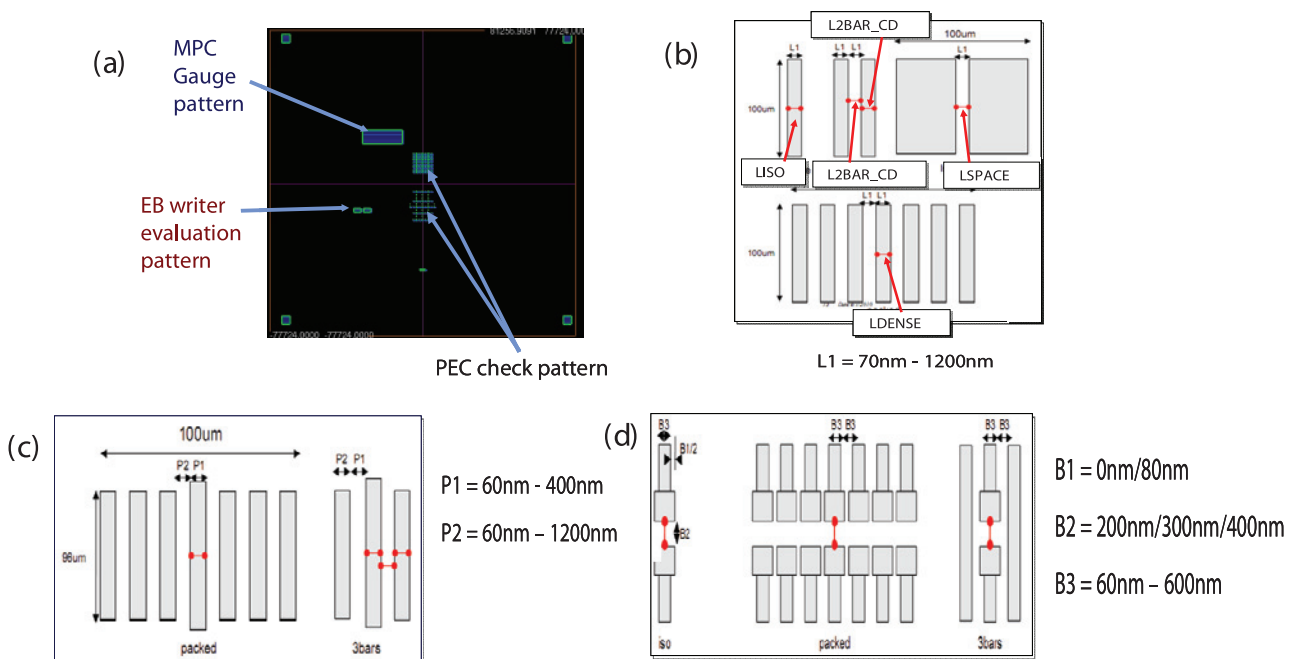
B1 = 0nm/80nm

B2 = 200nm/300nm/400nm

B3 = 60nm – 600nm

Figure 11.MPC evaluation patterns, (a) layout, (b),(c) MPC gauge patterns (1D) and (d) MPC gauge pattern (2D)
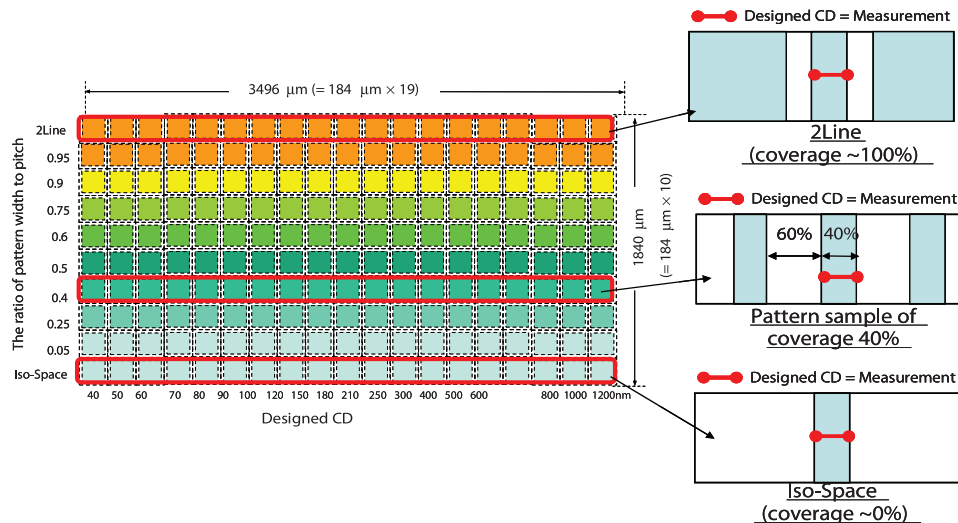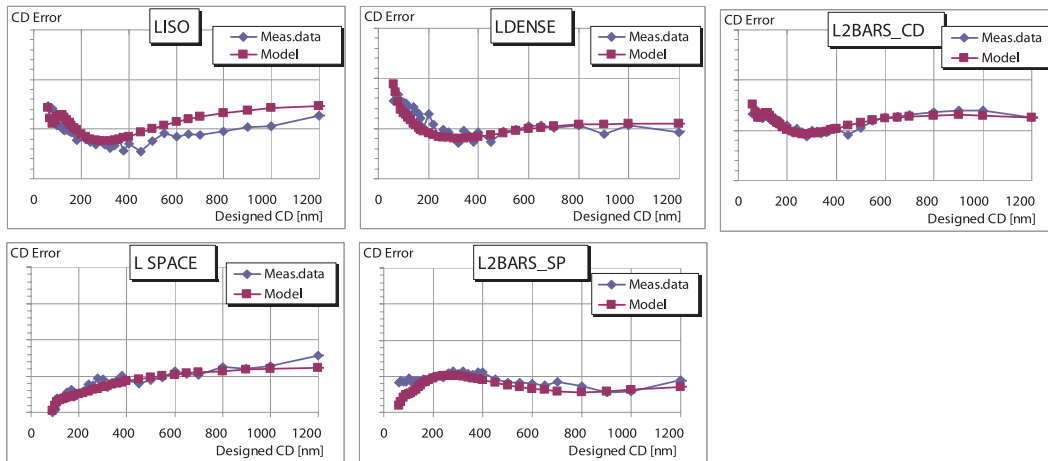

Figure 12.EB writer evaluation pattern
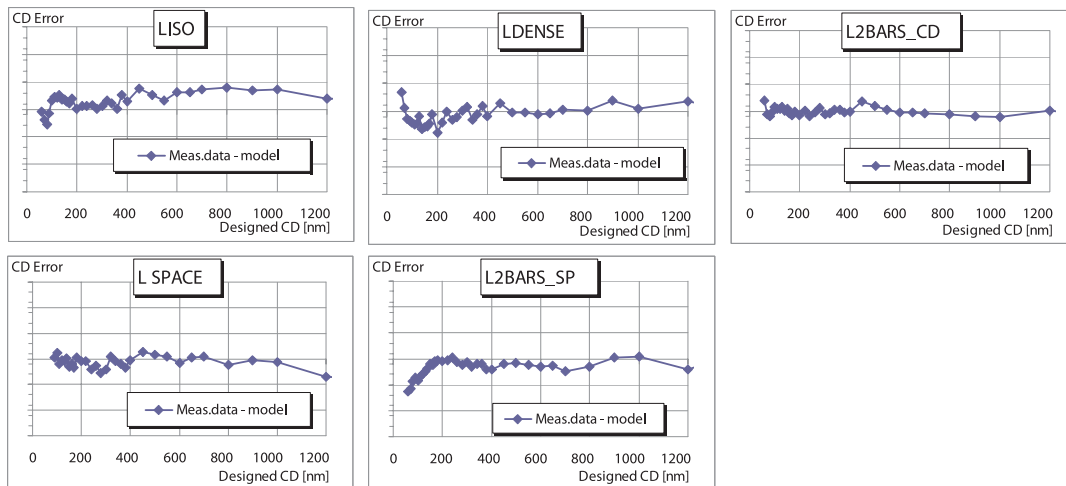
Figure 13.MPC+ modeling results for MPC gauge pattern

Figure 14.MPC+ residual error, "Measurement data – modeling data"

ity trend. MPC+ residual errors which are defined as "Measurement data – MPC Modeling data" are shown in Figure 14. CD error range is reduced by 62% after MPC+ @ 70nm-1200nm. Figure 15 shows linearity data of EB write evaluation pattern without MPC+ (a) and with MPC+ (b). CD error range is reduced by 51% after MPC+ @ 70nm-1200nm. Also, CD differences among local densities are reduced.

3.5 MPC calculation time

The runtime for full mask MPC+ on a Tachyon 3.0 system was benchmarked at 29.6 hours. It is about 3 times of runtime for HT/COG masks[3], due to smaller feature size, smaller pixel size and additional density terms. Further speed up of EUV MPC+ for production is expected through software optimization and hardware upgrades.

4. Summary

Absorbed energy profiles in resist which is defined as point spread function are estimated with Monte Carlo simulation for COG and EUV substrate. Only EUV shows short range scattering of a few µm or less. Dose margin is degraded about 25%, compared to COG. Linearity shows some unexpected signatures which are not observed in HT. This is not well explained with short range scattering only. Probably, process/resist characteristics should be taken into account to qualitatively explain them. Thus, empirical MPC model which parametrically correct such linearity is quite efficient.

MPC is applied to EUV linearity and its correction accuracy was discussed. CD errors of EUV linearity was 62% reduced for MPC gauge patterns @70nm-1200nm, and 50% reduced for EB writer evaluation patterns @70nm-1200nm.

But this is still unsatisfactory for ITRS2009 EUV linearity requirement of 2.4nm for hp16nm, 2019. Further study/improvement of the modeling is needed. Process/resist improvement is also required to resolve smaller CD patterns to evaluate actual sub-resolutions of 39nm or less.
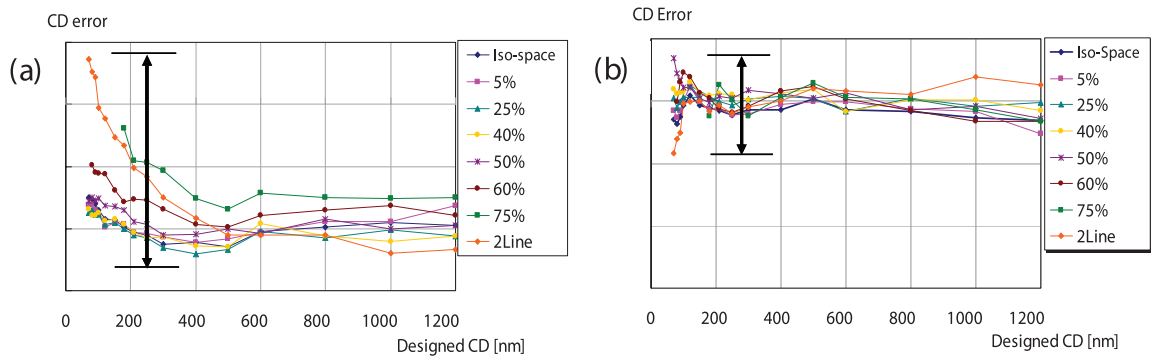
5. Acknowledgments

Figure 15. MPC+ results for EB writer evaluation patterns, (a) Measurement data and (b) "Measurement data – modeling data"

6. References

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Industry Briefs

■ Wafer Production in Recovery Mode

By **Semicon Europe 2010,** Dresden

The worldwide semiconductor industry, reflecting the expected demand for electronic goods and components in the next cycle in 2011, is set to grow sales 28% this year, according to the Head of the global industry producers' association. But that's still 11% lower than production in 2007, suggesting a graded recovery is underway. Speaking at Europe's top semiconductor trade show in Dresden, Stanley Myers, President of Semiconductor Equipment and Materials International (SEMI) said: "2010 is set to be a remarkable year for sales and shipments. Growth of some devices will be 28% [up], perhaps even more." (hktdc.com)

■ Intel Opens Billion-Dollar Factory in Vietnam

Intel's new billion-dollar factory, which opened in late October has a clean room the size of five-plus football fields, rises up from former rice paddies like a Wal-Mart on steroids. "On behalf of Intel's 85,000 employees, I would like to say, 'Hello Vietnam,'" company CEO Paul Otellini told an auditorium packed with enthusiastic government officials, employees and other dignitaries during a ceremony that featured a dragon dance and women in ao dais, traditional Vietnamese gowns. The Santa Clara chip giant's arrival in the Southeast Asian country put it "on the map for high-tech investment and helped the country attract significant investments from several leading global technology firms, including Foxconn and Compal," he added. At full capacity, Vietnam's first semiconductor factory, which produces chipsets for mobile devices and laptops, will double Intel's assembly and testing capabilities. The complex has the ability to produce microprocessors in the future. (EE Times)

■ Advanced Reticle Etch for 22 nm

By **Solid State Technology,** September 2010

Applied Materials launched its new Applied Centura Tetra X Advanced Reticle Etch system capable of etching photomasks needed for challenging device layers at 22nm and beyond. The Tetra X breaks the 2nm critical dimension uniformity (CDU) barrier across all feature sizes. "Next-generation lithography techniques place tremendous demands on the mask where accuracy of the pattern is crucial," said Ajay Kumar, VP and GM of Applied. Mask and TSV1 Etch product division. "The Tetra X system delivers the technology necessary to achieve this accuracy, enabling chipmakers to optimize lithography process capability for their highest performing memory and logic chips. This system has been qualified for 22nm production at a leading mask shop." The Tetra X system uniformity performance enables enhanced lithography resolution for demanding double-patterning and source-mask optimization (SMO) techniques by delivering highly uniform, linear etch across all features sizes and pattern densities while maintaining virtually zero defectivity. The Tetra X system employs a wide range of system enhancements, including proprietary, real-time process monitoring technology to enable the next-generation hard mask, opaque molybdenum silicon oxynitride ($MoSi2$), and quartz etch processes used to fabricate advanced binary and phase shift photomasks

European Mask and Lithography Conference 2011 (EMLC) program has been set and will be held from January 18-19, 2011 in Dresden Germany. More information can be found at http://conference.vde.com/emlc/Pages/Homepage.aspx

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About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

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Calendar

2011

SPIE Advanced Lithography

27 February-4 March
San Jose Marriott and
San Jose Convention Center
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Late submissions will be considered by conference chairs.

SPIE Photomask Technology

19-22 September 2011
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