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Impressions of our past

EDITORIAL

Impressions of our past

Paris Spinelli, Micron Technology

Albrecht Dürer was a 16th century Renaissance artist who had established mastery of woodcuts by his early twenties. He found fame, financial success, and freedom from the patronage system after completing a series of woodcuts based on the Book of Revelation. It was this fame which allowed him to focus on engraving. After his successful woodcut series, Dürer's works were in high demand and great efforts were undertaken to preserve the original engraved plates, and to keep them in a state where impressions could continue to be made. The similarities between the preservation of engraved plates during Dürer's day and the challenges we face in improving photomask lifetime by haze reduction are fascinating.

Dürer's etching plates were made of copper. Ink would be coated on to the plate, then wiped off so only the ink in the grooves remained. This would then be pressed onto paper to produce the image. Residual ink would remain in the grooves and require cleaning via a targeted wash depending on the ink: oil based for oil inks and water based for water inks. This process is paralleled today by specialized mask cleans, which prevent crystal haze formation by removing sulfate residue left on the surface of the mask during processing. While these crystals are much smaller than the residual ink left, they cause yield fallout if they were left without mitigation. Sulfate removal cleans also require specific targeting based on haze composition and formation mechanisms.

Storage of engraved plates between uses impacts conservation of the plates which still survive today. Engraved plates are stored in low-acid paper in low humidity and often coated with petroleum jelly. These efforts serve to prevent oxidation and degradation of the copper so the plates can continue to be used for prints. In the mask world, pellicles are similarly used to prevent haze formation on the surface of reticles. Material selection for pellicles continues to be an important consideration to maximize reticle lifetime. Some technologies take this even further by applying protective capping layers onto photomask surfaces preempting the formation of haze between features, making cleaning much simpler and more effective.

As etching plates were repeatedly used, the quality of definition decreased. Since copper is malleable, the edges of the channels cut into the plate would begin to blur and flatten out, this would decrease resolution of the lines and degrade the image which took days to carve. To preserve the fidelity of this image, printers would occasionally 'recarve' areas of the plate which had degraded. Techniques such as Rhazer to provide in fab removal are used to eliminate in fab haze from reticles. Repell and reclean facilities are also used to return reticles to a usable state through surface cleans.

As technology advances in photomask manufacturing, I will continue to be fascinated by the similarities between ourselves and our predecessors. If we find parallels so abundant now, what old challenges will we face as nano-imprint technology advances, and what solutions we can carve out for the continuation of our art?

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FEATURED ARTICLE

A study of ILT-based curvilinear SRAF with a constant width

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Abstract

SRAF plays a critical role in mask synthesis. It is a fundamental component of masks, for Manhattan or curvilinear masks, and for DUV or EUV masks. ILT is one of the technologies that can produce high-quality curvilinear, model-based SRAF. With this technology, the actual shapes of curvilinear assist features are naturally obtained by thresholding an optimized ILT mask that is represented as an image grid, ending up with freeform shapes. In this case, the ILT mask is formed through iterations of an optimization process. The shapes and widths of the freeform SRAF vary from location to location. Such SRAF is expected to deliver a wafer performance close to the optimum defined by the objective function. Nevertheless, the ILT-based curvilinear SRAF is an emerging technology, still on its way to full adoption in production. Therefore, this report focuses on the ILT SRAF obtained differently — constant width SRAF. Constant width SRAF is a more suitable starting point in addressing many practical concerns such as MRC compliance, SRAF printing avoidance, tile boundary stitching friendliness, run-time robustness, and data volume control.

The SRAF in this study is characterized by skeletons, each of which is in turn given by the coordinates of ordered "critical" points. These critical points mainly consist of local minima of the gradient map of the objective function. Here the gradient map, roughly speaking, is the partial derivative of the ILT objective function with respect to the transmission values of a grid-represented mask. We will show that the shapes of such constant width SRAF closely match that of the freeform SRAF obtained by thresholding the iterated ILT mask, up to their locations and connectivity, and maintaining the EPE convergence and simulated wafer performance compatible with its freeform counterpart.

Introduction

With Moore's law exploration, the lithographic process has dramatically evolved. Optical proximity correction (OPC) is widely and necessarily used to improve the pattern printability and the process window. Rule-based OPC as the first-generation correction technology can no longer satisfy the resolution requirements, as the pattern sizes continuously shrink. Then the model-based approach becomes the primary correction technology to deal with complicated and smaller designs. It is worth noting that the physical-empirical joint model, built with the real design on a particular process, makes model-based OPC possible, because the lithography model enables us to calculate and predict the physical results of the pattern transformation from the complicated shapes on a mask to the contours of the printed image on the wafer. An accurate model can also help check and predict the match of the simulated wafer contours to the required wafer target and predict the process window. At about the same time as OPC notion and practice were introduced to the industry, a resolution enhancement technologies (RET) technique, scattering bar, also known as sub-resolution assist features (SRAF) was adopted too. Nowadays, applying both SRAF insertion and OPC correction on the main patterns has become a common practice in the production of mask synthesis to improve the printing ability and pattern fidelity. Not much later than the adoption of OPC and SRAF technologies, if not around the same time, a rigorous mathematical concept for curvilinear mask generation, inverse lithography technology (ILT) was introduced, c.f.,[1-4] and the references therein. As the IC manufacturing technology node keeps shrinking, curvilinear masks and inverse lithography technology (ILT) are getting on fast tracks towards production adoption, and are promising to become the next generation of mask correction technology after rule-based OPC and model-based OPC, c.f.,[1,2].

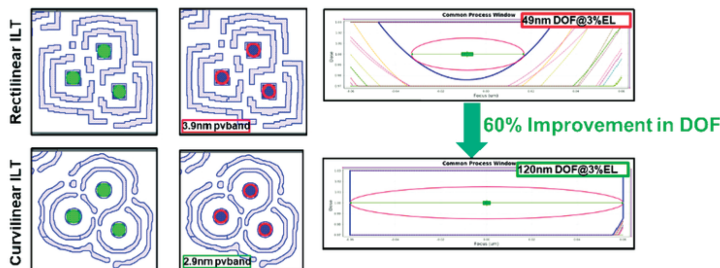

Figure 1. *The curvilinear ILT improves the cDOF by 60% over the rectilinear OPC on the most advanced EUV hole designs.*

Cases have been seen and reported, where ILT provides acceptable solutions to challenges of traditional OPC, and where curvilinear ILT masks could produce better process windows compared with rectilinear OPC, shown in Figure 1. However, there are also some important issues that have to be addressed before adoption for volume production. For instance, the simulation runtime of ILT, which could be tens or even hundreds of times of OPC, significantly limits the full-chip ILT adoption. It only was used for weak point tuning. Another question one may ask is how to maintain pattern fidelity of mask shapes during mask writing, especially for the tiny thin SRAF shapes and when using variable-shaped beam (VSB) writers. Moreover, for mask synthesis, the complicated curvilinear mask shapes generated by ILT may make the mask rule check (MRC) hard to comply. However, ILT is still a popular developing direction for its unique power in delivering high wafer performance and larger process windows[1,2].

Curvilinear SRAF is an essential component of the ILT technology in the application, as it grows through iterations of optimization governed by objective functions. As we know, larger SRAF typically provides more benefit to the main features but increases the risk of SRAF printing. In general, we must consider multiple parameters when calculating SRAF locations and shapes, such as the shape of the main pattern, the offset of the assist feature from the main feature, the distance between two assist features, and the width and length of the assist feature. In the optimization process, the SRAF growth and placement have to proceed with consideration of both performance and SRAF printing. In ILT, SRAF print avoidance can be factored into the optimization process. Freeform SRAF will then be formed as a result of the optimization[3,4].

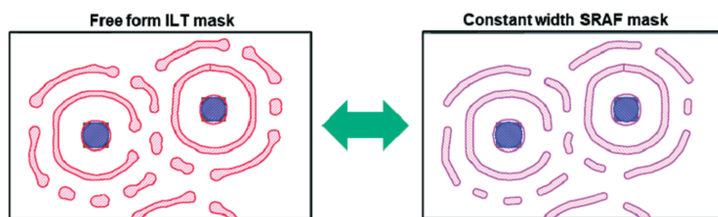

Figure 2. *The free-formed ILT mask (left) vs. curvilinear cwSRAF (right).*

However, freeform SRAF may have shapes that are more challenging to mask writing and inspection as well as to MRC clean-up, like T/Y junctions, cross shapes, sharp turns, and too-small features. To address the MRC challenges for free-formed curvilinear masks, we take a reasonable and practical starting point, that is, constant width SRAF or cwSRAF in short, shown in Figure 2. With cwSRAF, the user could control directly and precisely in the recipe the width, curvature, and minimal area of SRAF. Thus, there are chances that cwSRAF can largely save the run time for MRC clean-up. Even though cwSRAF provides interesting benefits to us, we need to study the risks of its discounting the full power and benefits that ILT can deliver for wafer performance otherwise. The amount of the discount depends on the design, model, and MRC rules.

In this paper, we present a study on the curvilinear cwSRAF based on ILT solutions, especially on the MRC compliance with some practical concerns in mind. The SRAF in the study is characterized by skeletons, each of which is in turn given by the coordinates of ordered "critical" points. These critical points mainly consist of local minima of the gradient map, which roughly speaking is the partial derivatives of the ILT objective function with respect to the transmission values of a grid-represented mask. In this work we will focus on comparing curvilinear cwSRAF vs. the curvilinear freeform ILT SRAF, based on their EPE convergence, mask geometrical characteristics, such as minimal width, minimal space, minimal area, Y/T/cross junction counts and wafer performances indicators, such as cDOF, PVband, NILS, circularity and extra print counts. We will show that the shapes of such cwSRAF closely match that of the freeform SRAF obtained by thresholding the iterated ILT mask, up to their locations and connectivity.

Curvilinear ILT flow

Curvilinear ILT generates optimal mask shapes by formulating and solving an optimization problem through multiple stages of iterations. The stages include pixelated mask evolution, mask optimization defined by objective functions of both wafer performance indicators and mask geometrical characters, and simultaneous or stagewise optimizations of SRAF insertion and/or SRAF/main features co-optimizations. In practice, curvilinear ILT is carried out in terms of an objective function that is constructed in the recipe and by combining task-emphasized modules. In the flow as shown in Figure 3, the lithography target is brought to the ILT objective function or traditional OPC for initialization. The result is then passed to the steps that control the MRC SRAF quality and the wafer results, which include SRAF generation and co-optimization of SRAF and main feature towards the MRC objectives to output the free-formed masks. Finally, the output masks will be sent to the final touch-up OPC to achieve the EPE convergence to the spec with less runtime cost.

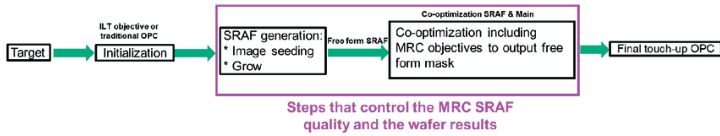

Figure 3. *The curvilinear ILT working flow.*

Challenges to MRC clean up for curvilinear SRAF

For the curvilinear SRAFS, min_width, min_space, min_area and min_curvature are examples of basic MRC checks for every mask. Due to the complexity of curvilinear SRAF shapes, the MRC cleaning is not a straightforward job. The MRC concerns should be addressed in multiple stages of ILT process. For example, in the SRAF generation stage, the regularizer and filter techniques could be used in construction of objective functions for SRAF growing optimization. For the imaged based MRC cleaning, the cleanup could be enhanced through optimization iterations and construction of objective functions that are lithographical and MRC-aware. Figure 4 shows the results of such an example. For the geometry-based cleanup, polygon operations and Boolean operations are applied on SRAFs after their shapes are formed.

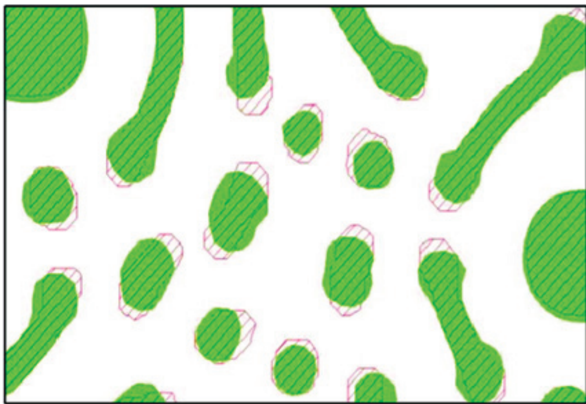

Figure 4. *Image-based MRC clean-up, red shapes are before cleaning, and the solid green shapes are after cleaning.*

To quantify the difficulty level of generating MRC-clean SRAF, we define a parameter ρ, which presents the "pitch ratio". The formula of ρ is shown in formula 1. We noticed that the difficulty level is correlated to a pitch ratio of MRC to the model.

where
$$\rho := \frac{MRC\ min\,width + MRC\ min\,space}{model\ pitch}$$

$$model\ pitch := \frac{wavelength\ \lambda}{NA\ (1 + patial\ coherence\ \sigma)}$$

The correlation trend could be summarized as follows: the difficulty increases as the ratio ρ increases. For instance, when $\rho < 1$, the SRAF can be made more lithographical during growing, extraction, and clean-up. However, when $\rho > 1$, then the optimal lithographical locations of SRAF may have to be compromised for MRC clean-up; but it is still possible to get acceptable wafer simulation performance while making the MRC clean. As for cwSRAF, the MRC min_space compliance can be addressed through the pitch control, while other MRC rule compliance, such as min_width, min_area, and min_ curvature can be handled more easily.

Curvilinear cwSRAF experimental results

The approach of our study

The experimental test case we used is an EUV hole layer in the most advanced design. We will show the results of quantitative simulation on-wafer validation, which include different SRAF styles of curvilinear free-formed ILT and cwSRAF, process conditions of dose, focus and mask bias, different MRC resolutions, and different MRC-to-model pitch ratio (ρ). The metrics to present the experimental results consist of 3 parts: (1) mask geometrical characteristics of SRAF, which include min_width, min_space, min_area, and count of T/Y/cross junctions, (2) the convergence presented by EPE, and (3) the wafer performances indicators of cDOF, NILS, PVband, extra printing, and circularity. Circularity is defined as the ratio of the wafer contour's curvature by the curve_target's curvature. Thus, closer to 100 percent is better. The EPE and PVband results are normalized by the target CD at the measurement location. All the MRC checks, min_width, min_space, and min_area, are normalized by the corresponding MRC spec as well, thus >= 1 means MRC clean.

In this study we compared three different simulation flows, which are called CLILT, FF2CW, and Im2CW. The flow chart is shown in figure 5. All flows have the same target and do the same initialization process of main. CLILT stands for curvilinear ILT, which is the baseline flow, including SRAF image generation (seeding and grow), free-formed SRAF extraction, SRAF and main features co-optimization with MRC objective and freeform mask output. FF2CW is the shorthand writing for "freeform SRAF to cwSRAF", which has the same steps until freeform mask output. Then FF2CW will go through the cwSRAF module to extract SRAFs and clean MRC errors. Im2CW stands for image-based cwSRAF extraction, which uses the SRAF image generated in the seeding and the grow step, and then directly extracts and builds cwSRAF. After the SRAF extraction and MRC cleanup, all three flows have a final touch-up OPC step to achieve the EPE convergence to the spec with less runtime cost.

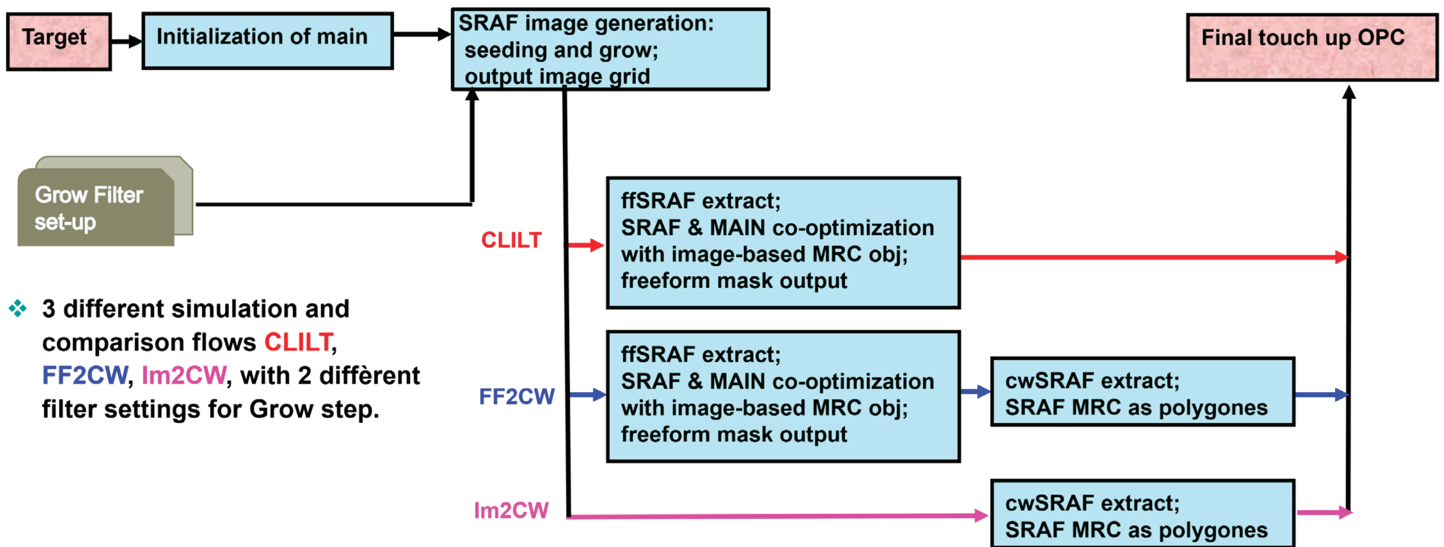

Figure 5. *Flow chart for the three different simulations and comparison flows CLILT, FF2CW, and Im2CW.*

Examples of pitch ratio ρ = 0.95 < 1

Generally speaking, the MRC cleanup of the freeform SRAF can be challenging and runtime-consuming due to the complexity of the curvilinear shapes (skew jogs, T/Y SRAF junctions, …). However, the cwSRAF ensures MRC clean SRAF shapes by construction, as shown in the field of mask geometrical characteristics of Table 1. Indeed, the MRC min_width, mn_area, and min_curvature are user-controlled parameters directly in the recipe while the MRC min_space constraint is addressed indirectly by controlling the MRC pitch through MRC min_width. The challenging part is to have the minimal spacing in spec, which is equivalent to pitch control. For a case where ρ < 1, we have more choices in selecting the filter parameter for the SRAF growth step, and hence make delicate and adaptive pitch control.

The goal of this example is to show we can extract cwSRAF by the Im2CM flow, i.e., directly from the image grid resulting from the image operations of seeding and grow stage, instead of getting the cwSRAF by the FF2CW flow. In order to make a complete comparison, we show here the simulated mask and wafer results of all three flows CLILT, FF2CW and Im2CW. Furthermore, to demonstrate our observation is robust, this 3-way

Table 1. *Wafer performance and mask geometrical characteristics comparison of the CLILT, FF2CW and Im2CW flows.*

Flow	Normalized EPE (a.u)			Wafer performance indicators					Mask geometrical characteristics of SRAF			
	min	max	range	cDOF (nm)	Min NILS (a.u)	Normalized PVBand (a.u)	Circularity (%)	Extra Printing count (a.u)	Normalized min_space (a.u)	Normalized min_width (a.u)	Normalized min_area (a.u)	T/Y/cross count (a.u)
CLILT+Final OPC	-0.0025	0.0075	0.0100	106	1.5	0.0800	99.5	0	0.69	1	1	0
FF2CW+Final OPC	-0.0025	0.0075	0.0100	105	1.5	0.0800	99.5	0	1	1	1	0
Im2CW+Final OPC	-0.0025	0.0075	0.0100	105	1.5	0.0800	99.5	0	1	1	1	0

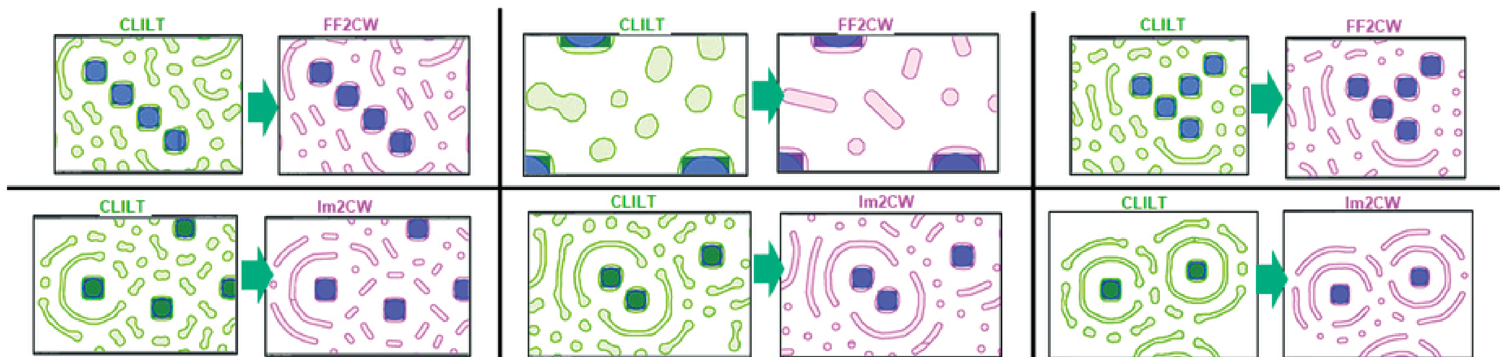

Figure 6. *Mask outputs comparison: CLILT vs. FF2CW and CLIL vs. Im2CW flows.*

Table 2. Wafer performance and mask geometrical characteristics comparison of the CLILT, FF2CW_f and Im2CW_f flows.

Flow	Normalized EPE (a.u)			Wafer performance indicators					Mask geometrical characteristics of SRAF			
	min	max	range	cDOF (nm)	Min NILS (a.u)	Normalized PVBand (a.u)	Circularity (%)	Extra Printing count (a.u)	Normalized min_space (a.u)	Normalized min_width (a.u)	Normalized min_area (a.u)	T/Y/cross count (a.u)
CLILT+Final OPC	-0.0025	0.0025	0.0050	106	1.6	0.0925	99.5	0	0.69	0.056	0.428	0
FF2CW_f+Final OPC	-0.0050	0.0025	0.0075	105	1.5	0.08	99.5	0	1	1	1	0
Im2CW_f+Final OPC	-0.0050	0.0050	0.0100	119	1.5	0.08	99.5	0	1	1	1	0

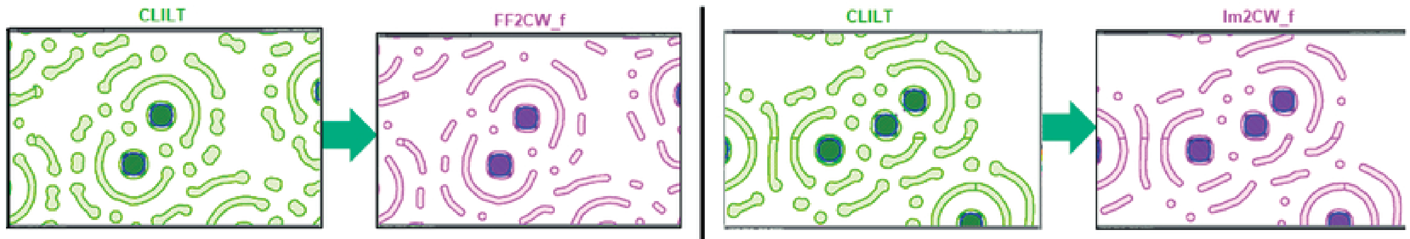

Figure 7. Mask outputs comparison: CLILT vs. FF2CW_f and CLIL vs. Im2CW_f flows.

comparison is even made twice, in 2 separate runs with 2 different filter settings for the grow step. We can observe that with both filter settings, the wafer performance of the freeform SRAF is well preserved in the cwSRAF. This observation is independent of how we extract the cwSRAF, from the freeform SRAF shapes or directly from the seeding-grow image.

Specifically, Table 1 illustrates these results of the first setting of the grow filter parameter, by comparing the mask geometries and the wafer performances of the freeform SRAF (CLILT+Final OPC) and the cwSRAF that is obtained in the FF2CW+Final OPC flow as well as in the Im2CW+Final OPC flow. Moreover, the latter flow has runtime benefit due to the skip of the SRAF-MAIN cooptimization stage, and we will quantify this runtime benefit in section 4.4. The screenshots in Figure 6 shows some mask output of the freeform SRAF (green) as well as their extracted cwSRAF (purple).

Let us next present the results of the same test case but with a different filter setting for the grow step, less forceful in enforcing MRC. We again compare the freeform SRAF to the cwSRAF. Table 2 summarizes the results of the mask geometries and the wafer performances of the freeform SRAF (CLILT+Final OPC) compared to the cwSRAF from the FF2CW flow as well as the cwSRAF from Im2CW, both with this less restrictive filter choice. Be noted that to distinguish the results in Table 1 and Table 2, we used notation FF2CW_f and Im2CW_f for the results in Table 2 in lieu of FF2CW and Im2CW in Table 1.

Table 3. Wafer performance and mask geometrical characteristics comparison: CLILT vs. FF2CW flows for ρ = 1.13 case.

Flow	Normalized EPE (a.u)			Wafer performance indicators					Mask geometrical characteristics of SRAF			
	min	max	range	cDOF (nm)	Min NILS (a.u)	Normalized PVBand (a.u)	Circularity (%)	Extra Printing count (a.u)	Normalized min_space (a.u)	Normalized min_width (a.u)	Normalized min_area (a.u)	T/Y/cross count (a.u)
CLILT	-0.0500	0.0150	0.0650	69	1.4	0.1400	99.5	0	1	1	1	0
CLILT_Final OPC	0.0050	0.0200	0.0250	118	1.5	0.1125	99.5	0	1	1	1	0
FF2CW	-0.0500	0.0150	0.0650	62	1.4	0.0900	99.5	0	1	1	1	0
FF2CW+Final OPC	0.0025	0.0175	0.0200	118	1.5	0.1175	99.5	0	1	1	1	0

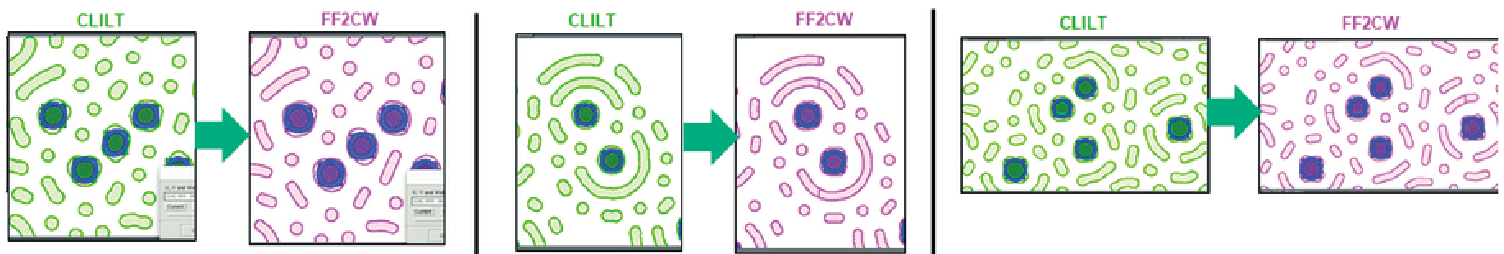

Figure 8. Mask outputs comparison: CLILT vs. FF2CW flows for ρ = 1.13 case.

FEATURED ARTICLE

Example of pitch ratio ρ = 1.13 > 1

When the pitch ratio ρ = 1.13, larger than 1, the MRC pitch is too tight compared to the model pitch. In this case, the lithographical location of the freeform SRAF may have to be compromised for the MRC cleanup. Therefore, the main-SRAF co-optimization stage may be a reasonable step to cwSRAF extraction for such cases. Table 3 shows that even in such tight cases, it is still possible to get acceptable wafer performances. Our trials with Im2CW, namely obtaining cwSRAF directly from the seeding-grow image failed. Therefore, we only show here cwSRAF that are generated in FF2CW flow, which still gives the wafer performances and mask geometrical characteristics comparable to the freeform SRAF of the CLILT. The screenshots in Figure 8 show some mask output of the freeform SRAF (green) as well as the cwSRAF of the FF2CW (purple).

Runtime results

Image based constant width flow is a typical cwSRAF flow in practice. Due to skipping the ILT co-optimization SRAF and main feature stage, the runtime could reduce 45 percent compared with CLILT flow. Figure 9 shows the runtime comparison between CLILT flow and Im2CW flow.

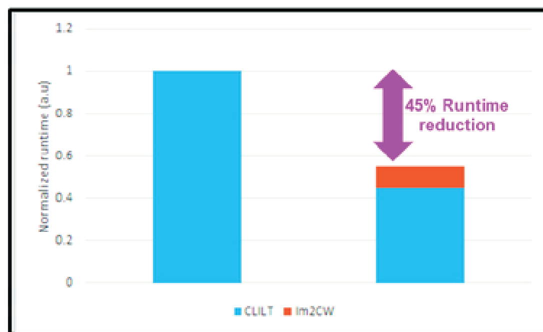

Figure 9. *Im2CW flow provides 45% runtime improvement over the CLILT flow.*

Summary

In this paper, we introduced a notion of "pitch ratio" ρ, which is correlated to the difficulty level of constructing MRC-clean SRAF. The difficulty increases as ρ increases. In all cases we tested, with both freeform and constant width SRAF, the techniques of regularization and filtering for optimization problems and that of MRC aware objective functions can all help enhance MRC in the image operation level and be effective. Specifically, cwSRAF is easier for MRC compliance and more friendly for polygon and Boolean operations in fixing MRC violations than its freeform counterpart is. Furthermore, for cases where ρ <1, we can obtain cwSRAF directly from the seeding-and-grow images, skipping the step of SRAF-main co-optimization. Afterall, in all cases, we noticed that our MRC-clean cwSRAFs can all achieve the EPE convergence and wafer performances to a level similar to what the freeform ones do.

REFERENCES

1. Danping Peng "ILT for HVM: history, present and future", Proc. SPIE PC12051, Optical and EUV Nanolithography XXXV, PC1205106 (13 June 2022).
2. Linyong Pang, "Inverse lithography technology: 30 years from concept to practical, full-chip reality," J. Micro/ Nanopattern. Mats. Metro. 20(3) 030901 (31 August 2021).
3. Sergey Kobelkov, Victoria Roizen, Sergei Rodin, Alexander Tritchkov, JiWan Han, Yuri Granik, "Constraint approaches for some inverse lithography problems with pixel-based mask," Proc. SPIE 10587, Optical Microlithography XXXI, 105870I (20 March 2018).
4. Yuri Granik, "Fast pixel-based mask optimization for inverse lithography," J. Micro/Nanolith. MEMS MOEMS 5(4) 043002 (1 October 2006).

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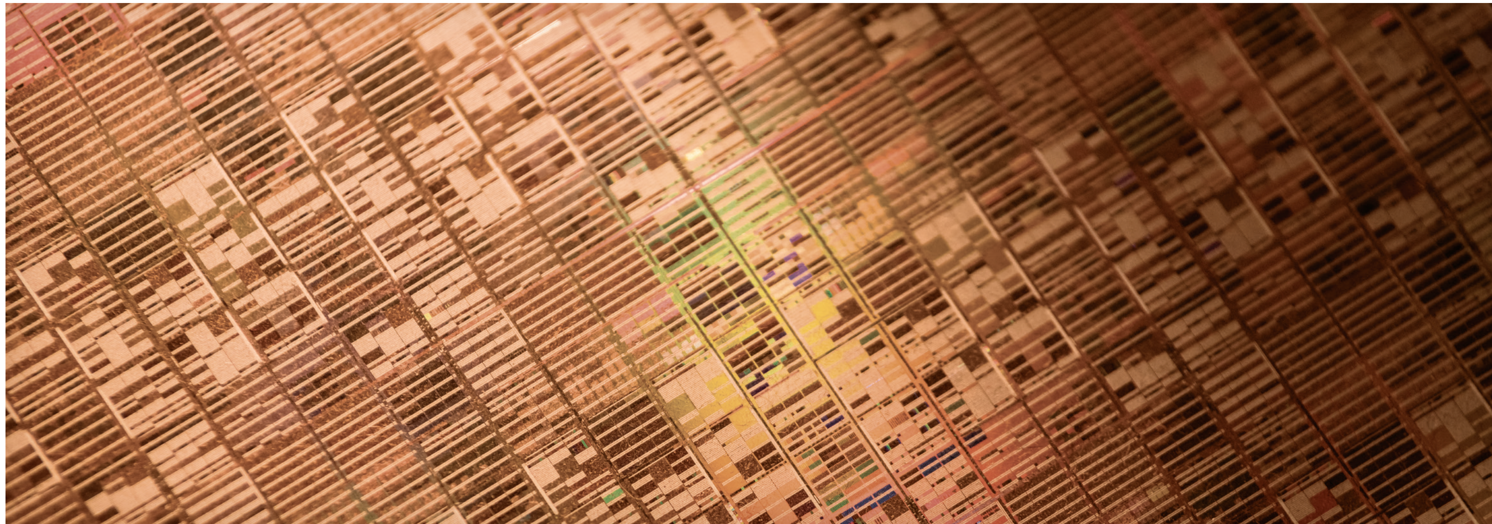

This investment will put us up there with the best in the world

June 23, 2023

A state-of-the-art chip factory is to be built in Magdeburg: The German Federal Government and Intel have signed a declaration of intent to construct a state-of-the-art semiconductor manufacturing plant. This agreement with Intel represents a major success and signals a strong investment in the future.

www.bundesregierung.de/breg-en/news/intel-investment-decision-2199006

Infineon breaks ground for new plant in Dresden

May 2, 2023

Work recently began on a new Infineon semiconductor production facility in Dresden, scheduled to start production in autumn 2026. Among other things, the microchips produced there will be used in the power supply sector in energy-efficient charger components, for example, as well as in small actuators in cars, data centers, and internet applications.

www.infineon.com/cms/en/about-infineon/press/press-releases/2023/INFXX202305-098.html

Taiwan chip industry safe: expert

June 22, 2023

Taiwan does not need to worry about its semiconductor industry moving abroad, and its position as a leader of the sector is set to continue, the head of Europe's largest chip technology research center said.

semiwiki.com/forum/index.php?threads/taiwan-chip-industry-safe-expert.18241/

New technique in error-prone quantum computing makes classical computers sweat

June 14, 2023

Researchers at IBM Quantum in New York and their collaborators at the University of California, Berkeley, and Lawrence Berkeley National Laboratory reported in the journal *Nature* that they pitted a 127-qubit quantum computer against a state-of-the-art supercomputer and, for at least one type of calculation, the quantum computer bested the supercomputer.

news.berkeley.edu/2023/06/14/new-technique-in-error-prone-quantum-computing-makes-classical-computers-sweat/

Infineon: Quantum Partnership

June 26, 2023

Infineon Technologies AG and eleQtron GmbH, a pioneer in quantum computing (QC) based in Siegen, Germany, announced their partnership to jointly develop quantum processing units (QPUs) with ion trap technology for scalable quantum computing. This second partnership of Infineon with a major player in the ion trap field represents the company's first commercial activity in the German quantum computing ecosystem.

silicon-saxony.de/en/infineon-quantum-partnership-infineon-supplies-three-generations-of-quantum-processors-based-on-ion-traps-to-eleqtron/

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About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

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spie.org/bacushome

Key Dates

2023

SPIE Photomask Technology + EUV Lithography
1–5 October 2023
Monterey, California, USA
spie.org/puv

2024

SPIE Advanced Lithography + Patterning
25–29 February 2024
San Jose, California, USA
spie.org/al

Photomask Japan
16–18 April 2024
Yokohama Japan
smartconf.jp

You are invited to submit events of interest for this calendar. Please send to tyb@spie.org.

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