Towards high NA patterning readiness: Materials, processes and etch transfer for P24 Line Space

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ABSTRACT

The goal of this work is to prepare process readiness towards High NA EUV lithography, by using 0.33NA exposures on the NXE3400B scanner. We focus on photoresists, underlayers, and etch processes mitigation of P24nm Line Space patterns. Etch transfer has been validated for Metal Oxide Resist (MOR). Furthermore, we investigate challenges to accelerating Chemically Amplified Resist (CAR) P24nm Line Space processes. Also, here, promising patterning results have been achieved. Thin film metrology-friendly methods like Atomic Force Microscopy (AFM) have been performed to characterize and improve the CAR-based etch processes.

1. Introduction

Insertion of EUV lithography into High Volume Manufacturing (HVM) has now started and enables further scaling of semiconductor devices. To continue pitch reduction in a single exposure, high NA (0.55 NA) EUV lithography is required[1]. Besides the progress needed on scanner systems, optics, and mask infrastructure, we need to improve EUV materials, photoresists, and stack transferability[2] to achieve final resolution targets after etching. These challenging objectives will require full ecosystem development including high resolution resists, new processes availability and advanced etch tools. Additionally, accurate metrology on thin films is needed.

The goal of this work is to assess ecosystem and infrastructure readiness toward high NA EUV lithography by 0.33NA exposures on the NXE3400B scanner at the Imec-ASML Advanced Patterning Center. Wafers are processed in a 300mm fab-like environment.

We focus on resist processes readiness post-litho for 24nm pitch of Line/Space (L/S) patterns. Fading corrections improve dose sensitivity compared to a standard half-leaf dipole source. In fact, the Z6 injec-
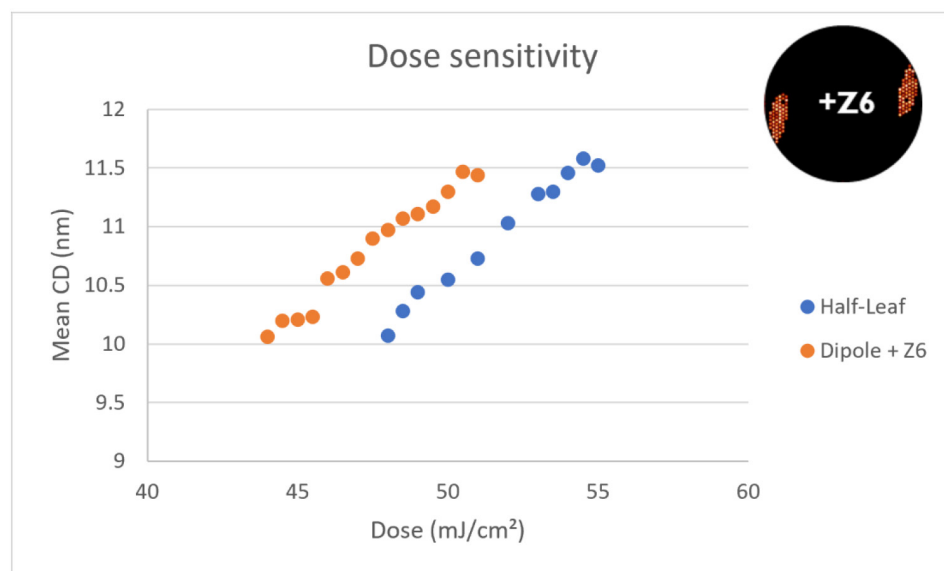
Figure 1. Dose sensitivity curves through sources for P24nm L/S features.

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EDITORIAL

The Catholic University of Leuven, Belgium, hosted the 37th EMLC 2022

Uwe Behringer, UBC Microelectronics, EMLC Conference Chair since 1993

From Monday, June 20th to Thursday, June 23rd, 2022 after the cancellation of the conference in 2020 and a digital conference in 2021, the European Mask and Lithography Conference, EMLC2022 was organized as a face-to-face event.

About 160 attendees listened to 53 presentations starting with a Tutorial Session on Monday afternoon. Peter De Bisschop from imec talked about "Stochastic effects in lithography, the ultimate resolution limit?" These effects manifest themselves in local CD variability (which in the case of a line/space pattern is usually quantified by the "Line Width Roughness," LWR) as well as in local pattering failure (micro bridging in space or randomly missing contact holes). Rogier Verberk from TNO-Netherlands Organization for Applied Scientific Research informed that QuTech (TNO and TU Delft) has agreed to make quantum technology accessible to society and industry via its full-stack prototype: Quantum Inspire.

Most presentations reflected the development of the last 3 years at the forefront of lithography technology. While 3 years ago people were still discussing how EUV lithography would prove itself in semiconductor mass production, this has now become the norm. It was particularly clear in the very first Keynote presentation by Luc van den Hove, President and CEO of imec. In an outlook on the year 2036, he talked about "The endless progression of Moore's law" and explained that we are today at the dawn of the 5th disruptive innovation wave. This emerging 5th deep tech wave builds on the convergence of technologies such as AI, material science, biology, and semiconductors to disrupt virtually every aspect of the world we live in. Semiconductors will be the core of virtually all deep tech innovations thanks to their massive integration power, accessible mass production, and low cost.

But despite the fame of EUV, as of 2022, we have to realize that global non-EUV-based wafer production is in fact higher than that of EUV. This proportion should remain as such for the foreseeable future as stated by Taguhi Yeghoyan from Yole Development. She pointed out that wafer production for More than Moore (MtM) applications is growing with a 5% CAGR and the non-EUV lithography equipment market dedicated to MtM applications exceeds $ 1 B and is expected to reach almost $ 2 B in 2027.

Frank Abboud pointed out in his presentation "Photomask Challenges for Upcoming Technology Nodes" that the continuation of Moore's law in semiconductor manufacturing will benefit from the technological advancement in patterning of ever smaller devices with advanced lithography techniques. One key enabler, he stated, is the innovations in photomasks. EUV mask technologies in materials, tooling, and infrastructure exhibit the most complex and revolutionary changes in the history of the mask industry.

Jos P.H. Benschop from ASML explained that Extreme UltraViolet lithography has come a long way since the pioneering work in the mid-1980s. EUV with 0.33 numerical aperture is currently being used in volume production of logic as well as DRAM IC makers. The next step in the EUV technology will be the 0.55 numerical aperture. Further innovations in a scanner, mask, and resist will further reduce the "k1" factor and enable a continuation of shrinkage well into the next decade.

New for the EMLC: For the first time in its history, the 2022 Program Committee and Carl Zeiss (Zeiss Semiconductor Mask Solution (SMS)) announced the ZEISS Award for Talents in Photomask Industry for the Best Student Presentation. Ms. Canpolat-Schmidt from the Fraunhofer Institute for Electronic Nano Systems (ENAS) at Chemnitz (Germany) received the Award for "Lithographic Performance of Resist ma-N 1402 in an E-beam/i-line Stepper Intra-level Mix and Match Approach."

Two EMLC 2022 Best Presentations were selected: one from Natallia Karlitskaya from Cymer on "Holistic imaging for yield improvements enabled by high availability, and low-environmental impact Cymer ArFi Lightsource," which will be an invited talk at BACUS 2022, and one from Tatiana Kovalevich from imec, Leuven on "Spatial frequency breakdown of CD variation," which will be an invited talk at PMJ 2023.

On June 23rd, 2022 the EMLC 2022 attendees were invited by Kurt Ronse, Advanced Pattering Program Director to imec for an overview of presentations and a window tour of the 300 mm wafer fab facility.

In Summary: The EMLC International Program Committee and many positive comments from Conference Attendees allow us to say: "The EMLC2022 has been a great success."

Please mark your calendar: The EMLC2023 will take place from Monday, June 19th untill Wednesday, June 21st, 2023 at the Hilton Hotel in Dresden, Germany.

BACUS

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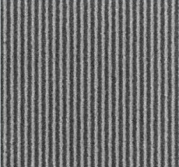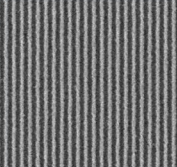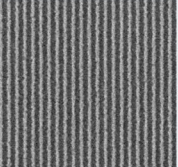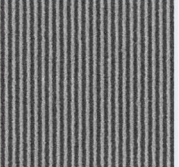**Larry Zurbrick,** *Keysight Technologies, Inc.*

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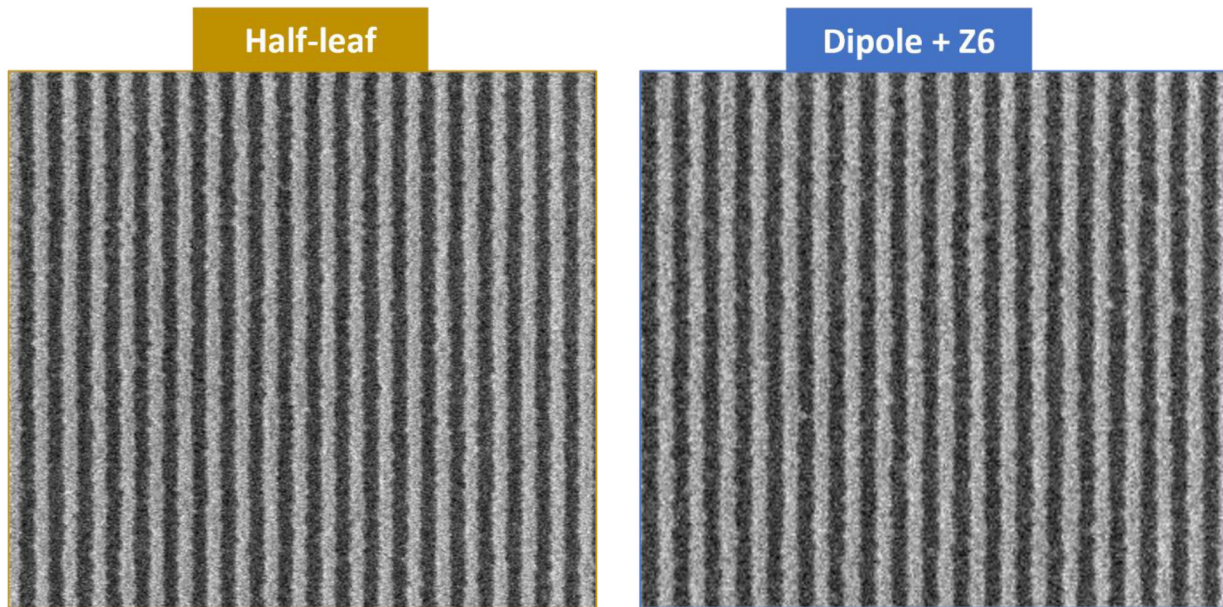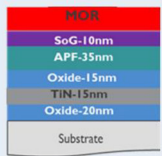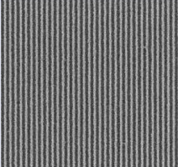
Figure 2. Top-down SEM images of Dense L/S patterns at P24nm and CD on wafer of 11nm.

Table 1. MOR litho process DOE data summary.

MCDII	CONDITION 1	CONDITION 2	CONDITION 3	CONDITION 4	POR
PEB (°C)	PEB2	PEB2	PEB1	PEB2	PEB1
HB (°C)	HB2	HB1	HB2	HB2	HB1
RFTH (nm)	22	22	22	16	22
Smaller CD (nm)	9.8	9.7	9.9	9	10
D2S (mJ/cm²)	44	42	50	45	48
EL (%)	32	28	29.8	32.6	20.3
Substrate	Si+SoG	Si+SoG	Si+SoG	Si+SoG	Si+SoG

tion improves exposure latitude (EL) on wafers by up to 25%, beyond what is predicted by simulation[3]. We investigate new process availability for both Chemically Amplified Resist (CAR) and non-CAR resists with high-resolution performances. Different stacks/materials combinations like Spin-on-Glass (SoG), organic underlayers as well as deposited underlayers have been studied including film thickness variations in the range of 5-10nm.

For Metal Oxide Resist (MOR), process optimization by Post-exposure Bake (PEB) or Hard bake (HB) temperatures and resist film thicknesses variation (16-22nm range) has been carried out. Best process conditions were used to further demonstrate L/S printability down to 10nm CD. First, etch demonstration on an Imec platform stack has been validated using Metal Oxide Resist (MOR). CD capability of 10nm post-litho/post-etch has been achieved after process optimization.

Furthermore, we are exploring challenges to accelerate Chemically Amplified Resist (CAR) processes for P24nm L/S both post-litho and post-etch. First, etch of CAR L/S P24 was done to further improve pattern transferability together with stack materials and thicknesses optimization. To allow for that, thin film metrology-friendly methods like Atomic Force Microscopy (AFM) have been performed to characterize these CARs etch processes. The measurement of resist film thickness after development is a key parameter for a successful etch transfer at tight pitches. This helps to estimate very precisely the photoresist budget and further mitigate etch processes for the thin underlayers and hard-mask materials. On top of that, AFM can help identify L/S defects like breaks that we cannot see on top-down SEM pictures and that can lead to line breaks after etching.

In summary, the work presented here shows the infrastructures current capability towards patterning at high NA EUV lithography. Thanks to optimized photoresists, underlayer materials and etch processes together and metrology enablement, we can explore and optimize patterning capability at tight pitches for L/S patterns.
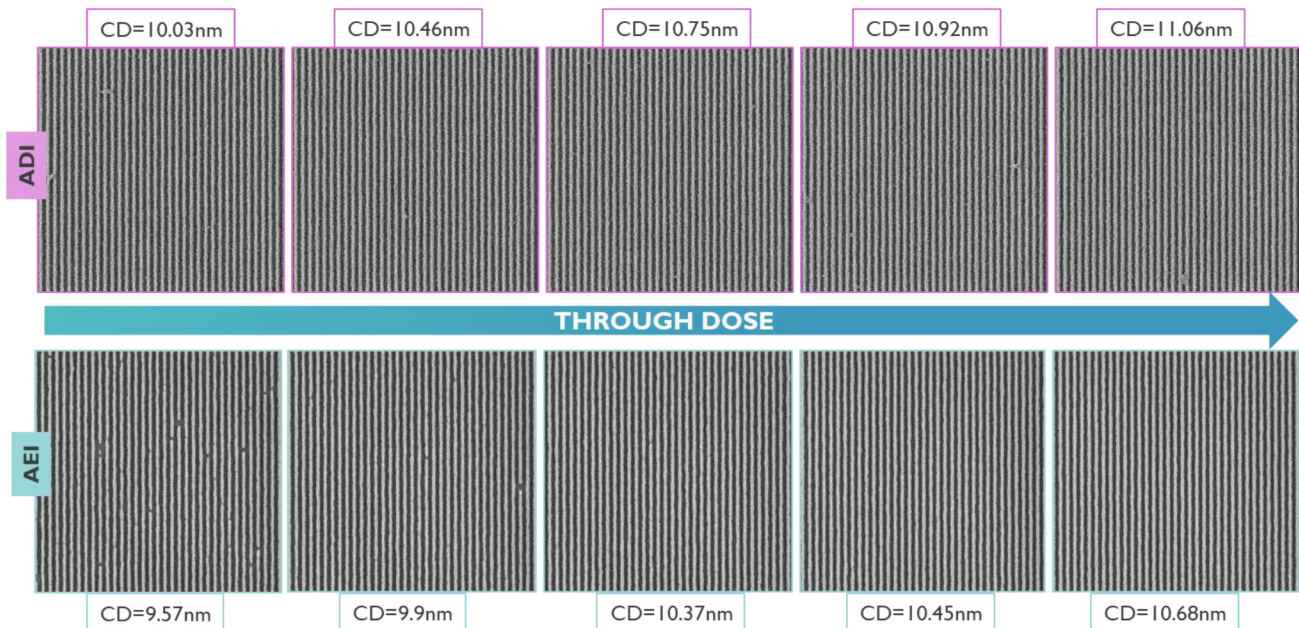
Figure 3. Top-down SEM images of Dense L/S patterns at P24nm after development and after etching on stack wafers & RFTH 22nm

2. P24 Line Space Patterning on Metal Oxide Resist (MOR)

2.1 Illumination conditions

To print the smallest L/S possible, we must optimize the aerial image. At the densest pitch, only two light beams are captured by the lens (2beam imaging). The aerial image is determined by the amplitudes of these two diffraction orders and their relative phase. Balancing the amplitudes optimizes aerial image quality as described by the normalized-image-log-slope (NILS). To reduce NILS loss introduced by the relative phases, we need source optimization. To pattern dense L/S at P24nm, we start from a half-leaf dipole source that allows for a good aerial image. In addition to the half leaf source, we also use a fading corrected source that is optimized for maximum NILS at defocus in the presence of an injected Z6 aberration.

We compare the performance on wafer for these two sources (Half-leaf dipole and dipole + Z6) targeting P24nm L/S patterning. We perform the exposures on 22nm thick MOR layer on top of a 10nm Spin On Glass (SoG). Both sources show good process window with Exposure Latitude >25% and DOF (Depth-of-Focus) of 250-300nm. We notice an increase in Exposure Latitude with the Z6 injected source of about 15% together with an improvement in dose sensitivity of 7%. In Figure 1, we plot Dose sensitivity through source. The observed contrast improvement allows for wider PW after development and hence help for pattern transfer through the full stack. In Figure 2, we show top-down Scanning Electron Microscopy (SEM) images of Dense L/S patterns at P24nm and CD on wafer of 11nm for Half-leaf dipole and dipole + Z6 injected sources, respectively.

Based on this on-wafer validation, all coming experiments use the optimized Z6 injected half-leaf dipole source.

2.2 MOR lithography process DOE data

Once the illumination conditions have been selected, we run a DOE (Design Of Experiments) on Si+SoG by varying multiple parameters such as post-exposure and hard bake temperatures and resist thickness to identify best lithography process conditions for MOR patterning at P24nm.

The results of the DOE are summarized in Table 1 targeting CD on a wafer of 11nm: all conditions are showing very good PW data together with good printing capability. For a standard resist thickness of 22nm, line CD down to 9.7nm could be achieved whereas for 16nm film thickness we could print down to 9nm. These results are very promising and confirm the capability of MOR to cover such tight pitches with a good process window (PW). However, we must mention that high exposure latitude values need to be confirmed after etching.

By varying the PEB1 temperature from POR conditions to PEB2 conditions, we slow down the resist which leads to a dose reduction of 12.5% combined with a slight improvement in exposure latitude.

We have also performed modification in hard bake temperatures. The hard bake is done after the development as final bake step for stabilizing the printed features by hardening the photoresist which may further help for etch process. It ensures complete removal of solvent, improving adhesion in wet etch processes and resistance to plasma and/or RIE etches. In this experiment, we have two different hard bake temperatures of HB1 (standard) and HB2. The hard bake temperature has no or minor impact in dose sensitivity as shown in Table 1. However, it helps widen the process window; the exposure latitude has indeed increased from 14% for PEB2 /HB2 wafers.

Regarding the resist film thickness, we have investigated two thicknesses of 22nm (standard) and 16nm. Based on optimized process conditions for each resist thickness, we performed exposures on 2 wafers and have found no significant improvement in terms of Exposure latitude between the two wafers, nor dose-to-size. The main improvement was seen on pattern resolution, as L/S patterns as small as 9nm could be achieved with resist FTH of 16nm.

Following the lithography process DOE data evaluation, we have decided to keep the two most promising process conditions for further pattern transfer investigation on Metal Oxide Resist: Condition 1 and condition 4 found in Table 1.

2.3 P24nm L/S pattern transfer on Metal Oxide resist

To demonstrate P24 L/S patterns transfer on MOR, we have selected a relevant stack based on Imec pre-platform activity; it consists of 20nm of Oxide layer, 15nm of TiN, 15nm of a second Oxide layer, and 35nm of amorphous carbon, followed by our lithography stack of 10nm SoG and 22 or 16nm MOR photoresist.

To evaluate preliminary etching performances at P24nm, we use our lithography Process of Reference (POR) as indicated earlier in Table 1. By transferring etch process learning from our Imec P28 platform[4], we could successfully transfer the L/S pattern of CD 12nm. Additional etch process tuning was still required to achieve good pattern fidelity. After
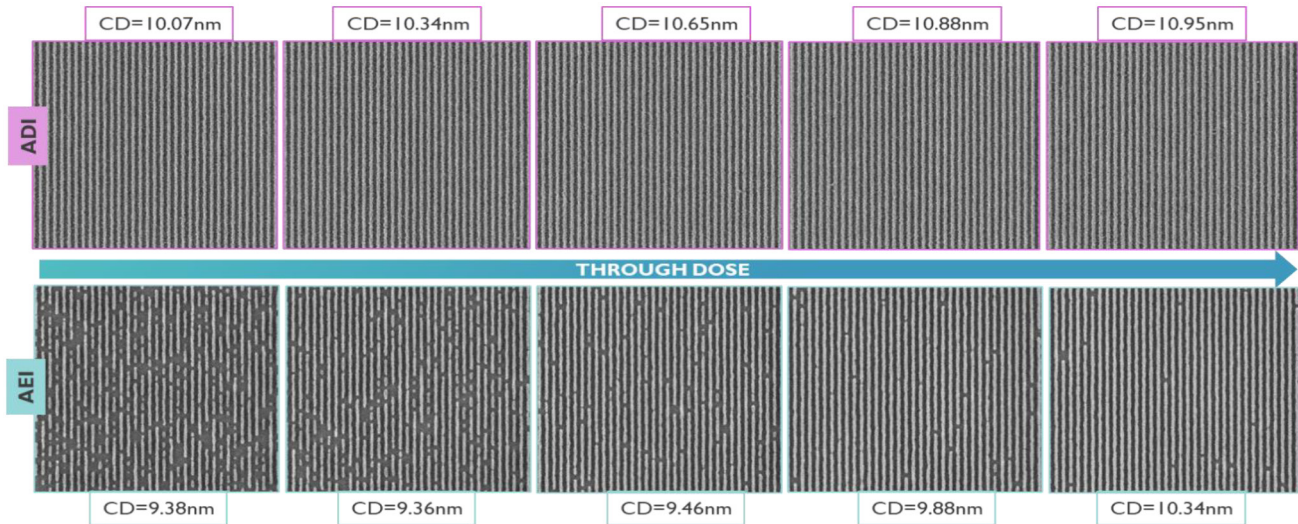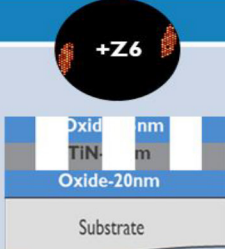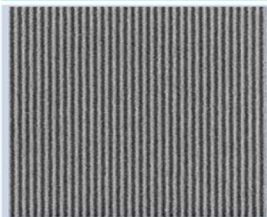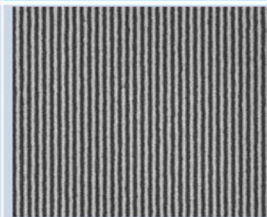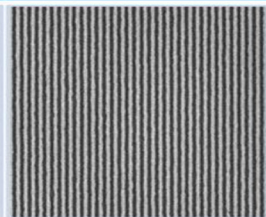
Figure 4. Top-down SEM images of Dense L/S patterns at P24nm after development and after etching on stack wafers & RFTH 16nm

Table 2. MOR process P24 L/S roughness comparison after litho and after etching.

	After Litho	After Etch	
CD (nm)	10.7	10.4	10.9
uLWR (nm)	3.3	2.4	2.3
uLER (nm)	2.4	1.8	1.8
Resist FTH (nm)	22	22	16

development and after etching L/S patterns with CD close to 11nm and unbiased LWR of 2.4nm after etching into TiN/Oxide are obtained. Based on these promising after-etching results, we have transferred the process to the best conditions from our DOE. Exposures are carried out for 2 different resists film thicknesses of 22nm and 16nm as earlier mentioned5.

In Figure 3 we show top-down SEM pictures through a dose of P24nm L/S patterns for MOR film thickness of 22nm on stack wafers after development and after etching. We could achieve L/S printing with no or limited defects from CD 10.4nm AEI.
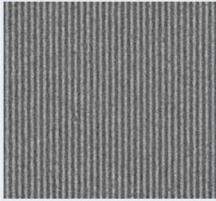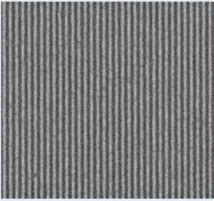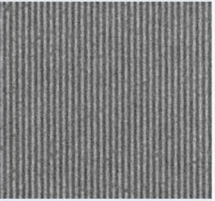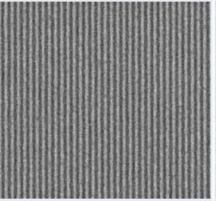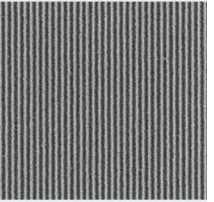
For photoresist film thickness 16nm, despite good lithography performances, the pattern transfer of L/S was not fully achieved. For small L/S CD, we found lots of defects post etch, with many line breaks as shown in Figure 4. The etching process transfer from 22nm resist film thickness to 16 nm thickness will need some tuning to further demonstrate pattern transfer of such thin film. Indeed, the remaining resist film thickness after development, which is known to be close to 8nm for the 16nm resist thickness case, needs to allow for full pattern transfer and is currently under investigation.

2.4 Roughness Comparison

In terms of roughness, we have extracted the unbiased Line Width and Line Edge Roughness (LWR//LER) AEI using Fractilia MetroLER software. For resist film thickness of 22nm, 2.4nm/1.8nm are obtained for LWR/LER and 2.3nm/1.8nm at a film thickness of 16nm. Although CD is smaller for 22nm resist FTH, the roughness data are very comparable as summarized in Table 2. We are however above the specifications for P24 L/S patterning, where LWR/LER unbiased should be below 1.9nm/1.4nm which corresponds to a roughness reduction of around 15-20%. With proper etch process mitigation together with film/stack optimization, some improvement in roughness can be foreseen. But this is however not within the scope of this work. For more accurate resist roughness profiles, the methodology described by Severi et al.[6] would be interesting to consider.

To sum up, we have compared the new AEI data with the one from our POR process. Based on the analysis, roughness data are very comparable for the 3 process conditions and that was also confirmed by PSD plots obtained with Metroler.

Table 3. CAR litho process DOE data summary.

MCD11	CONDITION 1	CONDITION 2	CONDITION 3	CONDITION 4	Best MOR
Top-down SEM					
RFTH (nm)	23	28	28	28	22
Smaller CD (nm)	9.8	10.2	10	10.5	9.8
D2S (mJ/cm²)	58.8	60.7	60.7	62.4	44
Max EL (%)	22.6	22.1	22.1	15.6	32
Substrate	Si+POR UL	Si+POR UL	Si+UL2	Si+UL1	Si+SoG
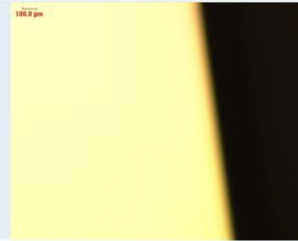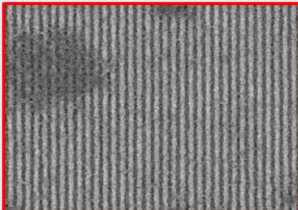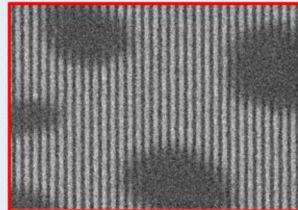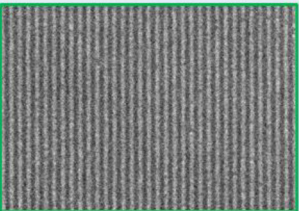
Compatibility	SoG+POR UL	SoG+UL1	SoG+UL2
Post-Coating			
Post-Exposure (P24MCD11LS)			

Figure 5. Post-coating and post-exposure compatibility investigation on CAR stack wafers

3. P24 Line Space Patterning on Chemically Amplified Resist (CAR)

3.1 CAR Lithography process DOE data

To demonstrate successful pattern transfer of sub 5nm node features, many challenges need to be tackled for Chemically Amplified Resist (CAR) processing[7]. The first one is the so-called Resolution LWR/LER Sensitivity (RLS) trade-off. While thin resist film thickness is needed to achieve high resolution, it doesn't help to achieve decent roughness. In addition, good pattern transfer quality of such small features (CD <12nm after development) requires a sufficient etch resist budget. For P24nm L/S patterning one should consider stochastic printing failures such as Line breaks or bridges as well. Therefore, mitigation of stochastic failures and suppression of pattern collapse are the main requirements for a successful P24 L/S pattern transfer.

In our first experiment, we aim to perform a small DOE on lithography performances of our best CAR material candidate to demonstrate the printability of L/S patterns at CD 12nm and below. We have selected two different photoresist thicknesses of 23nm and 28nm. Additionally, we perform Si wafers exposures on three different Organic underlayers (UL) materials to avoid pattern collapse at low CD printing. The data summary is shown in Table 3, with a comparison to our best MOR process data. The illumination conditions are kept the same as in the previous experiments with Metal oxide Resist i.e., a half-leaf dipole source with a Z6 injection.

We found that for the same photoresist changing the film thickness from 28 to 23nm help to have slightly better resolution, but that improvement is counter-balanced by more printing defects and hence a reduced free-failure latitude at 23nm film thickness. From the two new underlayers, UL2 is showing better exposure latitude with respect to POR UL whereas UL1 has lower exposure latitude and slightly higher dose. The top-down SEM images shared in Table 3 show poor contrast of CAR wafers Vs MOR wafer which can be partly explained by the material itself (dissolution rate contrast) but also by the stack used for both exposure types: 5nm organic UL film thickness for CAR wafers and 10nm SoG for MOR wafer.

3.2 CAR lithography performance on a stack

After CAR process verification on Si + UL, we have performed experimental validation of the lithography process onto a representative stack for

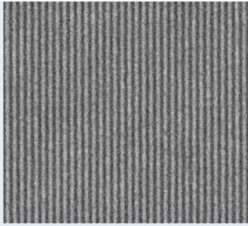**Table 4. CAR lithography performances through photoresists at FTH=23nm.**
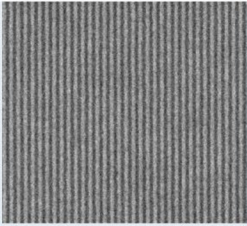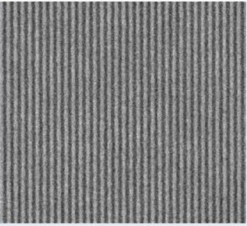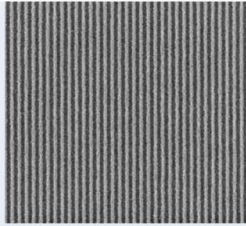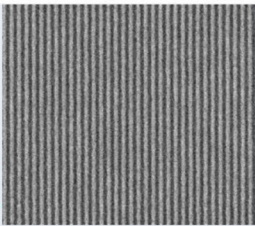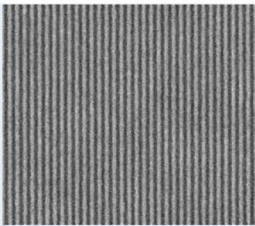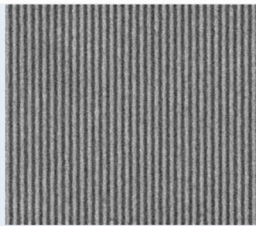
MCDII	POR PR	PRI	PR2	Best MOR
Top-down SEM **Resist FTH 23nm**				
Unb. LWR/LER (nm)	3.4/2.3	3.3/2.2	3.1/2.1	3.3/2.1
Smaller CD (nm)	10	10	10.2	9.8
D2S (mJ/cm²)	61	59	61	44
Max EL (%)	24	19	15.5	32
Substrate	SoG+UL2	SoG+UL2	SoG+UL2	SoG only

Table 5. CAR lithography performances through photoresists at FTH=28nm.

MCDII	POR PR	PRI	PR2
Top-down SEM **Resist FTH 28nm**			
Unb. LWR/LER (nm)	2.8/1.9	2.8/1.9	2.9/2.0
Smaller CD (nm)	10.6	10.2	NA
D2S (mJ/cm²)	63	60	64
Max EL (%)	16	16	11
Substrate	SoG+UL2	SoG+UL2	SoG+UL2

LITHO · UL2 ETCH · SoG ETCH · APF ETCH

CD=11nm

Figure 6. Top-down SEM images through CAR process pattern transfer of L/S P24 features and resist FTH 23nm.
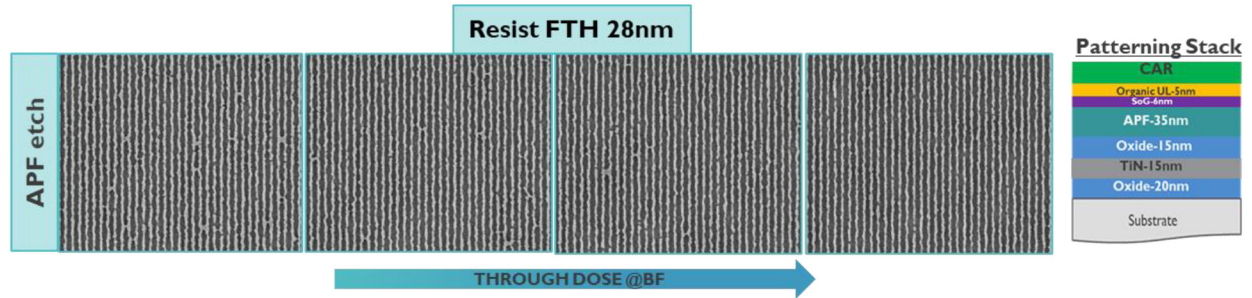
Figure 7. Top-down SEM images of P24 CAR L/S features after APF etch.
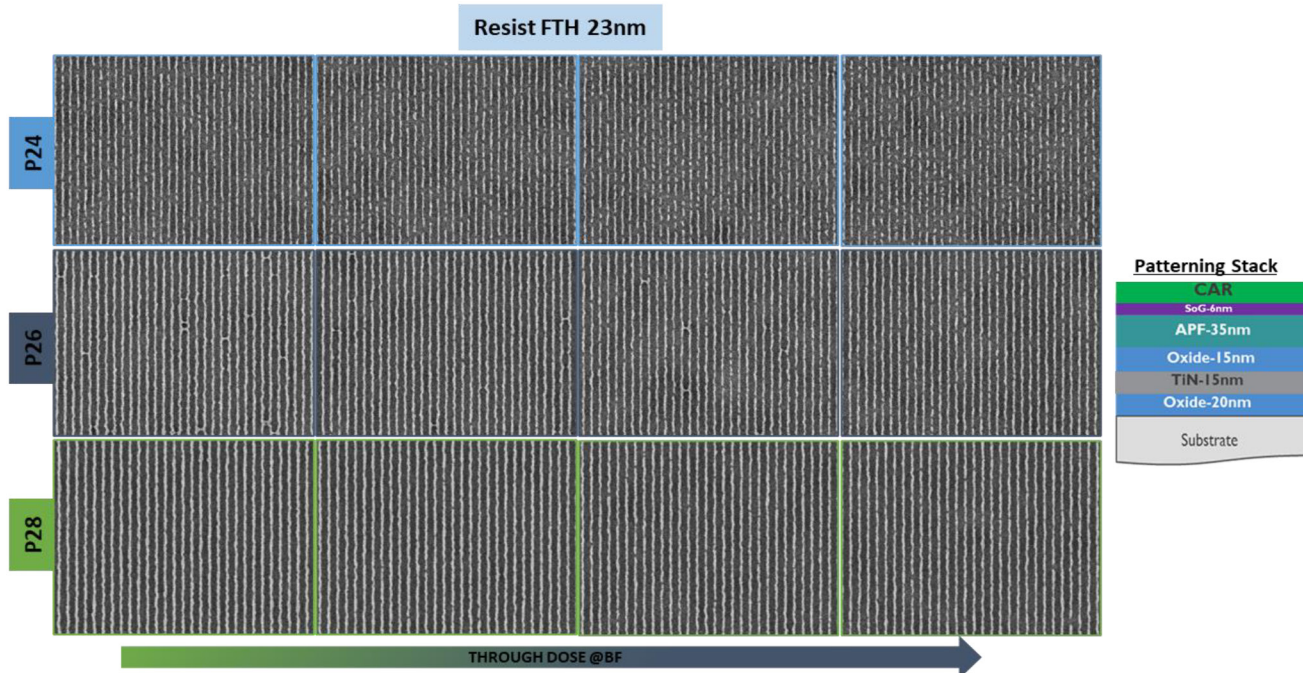
Figure 8. Top-down SEM images through Pitch of CAR L/S features after APF etch.

small L/S features transfer. The chosen stack is very similar to the one demonstrated on MOR patterning; it consists of 20nm of Oxide layer, 15nm of TiN, 15nm of a second Oxide layer, and 35nm of amorphous carbon and SoG. On top of SoG, we use a thin layer of Organic UL to help for adhesion purposes and pattern collapse mitigation. Two different SoG materials have been tested: our POR material (as used in the MOR experiment) and an alternative Si-rich SoG that is stronger and might help for pattern transfer. As explained in [4], silicon hard mask (Si-HM) is one of the key materials used in multilayer lithography for pattern transfe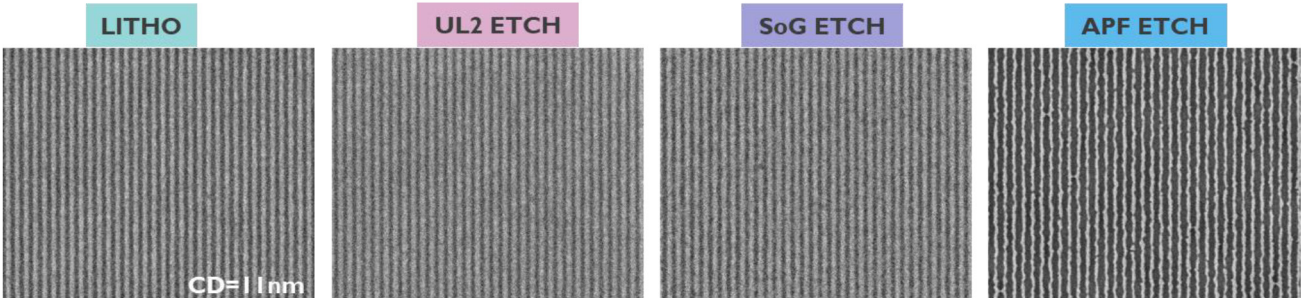r to a substrate using a fluorinated plasma etching process[8], with main challenges in defects control. The previous 3 UL materials are considered in this study as well.

Before performing EUV exposures on the stack wafers, we first handled material compatibility checks to identify or prevent any coating issues. By doing so we noticed that the new organic UL are incompatible with our POR SoG material, and they need to be used in combination with the alternative Si-rich SoG that comes from the same material supplier. In addition, we found that not all 3 ULs are suitable for the mentioned SoG. POR UL and UL1 show coating issues with some flakes on Si wafers that can be seen as big spots/bubbles and were not visible on an optical

microscope but only under an SEM microscope. They lead to L/S defects after printing as shown in Figure 5 with top-down optical microscope clean images and SEM images revealing black spots on L/S features. Indeed, POR UL and UL1 materials are coming from the same platform and the observed issues could be due to their specific composition. This issue is under investigation by the material vendor.

We have decided to pursue the lithography performance evaluations considering only the stack with alternative SoG and UL2 which shows no compatibility issues post-coating or post-exposures. Besides the compatibility, the chosen UL2 platform has been developed to ensure a faster etch rate, hence less photoresist consumption during etching, with respect to our POR material to compensate for thin photoresist thickness. The layer is kept as thin as possible at 5nm and so does the new SoG (film thickness of 6nm). We believe that the new stack combination will allow good CAR lithography performances to print P24 L/S patterns while guaranteeing safe pattern transfer into the underlying layers. A similar stack has been already used in previous experiments to demonstrate pattern transfer at P28 L/S; however, in the mentioned case, the photoresist thickness was 40nm which might be more advantageous for etching budget and successful pattern transfer.
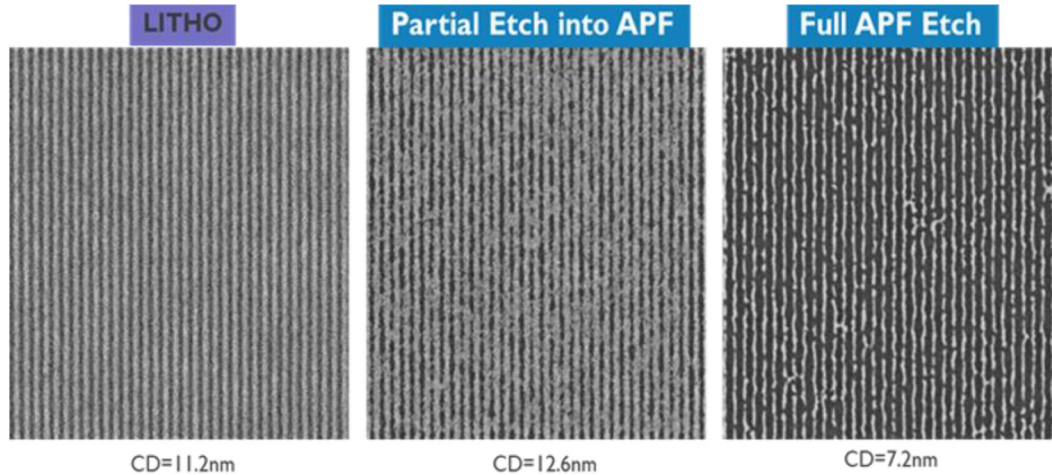
Figure 9. Top-down SEM images of P24 CAR L/S features through APF etch process for resist FTH 23nm.
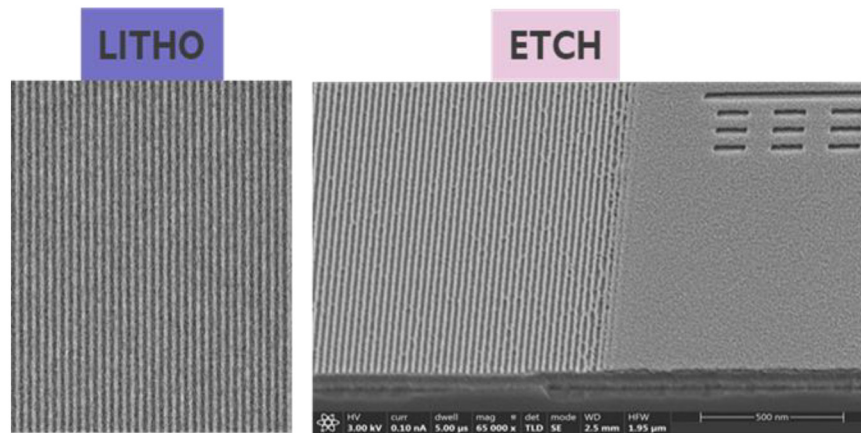

Figure 10. Top-down SEM images of P24 CAR L/S features after litho and X-SEM after APF etch for resist FTH 25nm.

3.3 P24nm L/S pattern transfer investigation on Chemically Amplified resist

As discussed previously, CAR performances are improving towards P24 L/S patterning for future node enablement. To strengthen our experimental plan, we have screened additional CAR materials from the same vendor to evaluate lithography performances and chose the best resist to fulfill the requirements for 12nm features transfer into a stack. Two new resist namely PR1 and PR2 are compared to our POR resist in terms of printability, defects, process window, and roughness post-development. At 23nm resist film thickness, all photoresists are performing the same with maximum exposure latitude of 15 to 24% and dose-to-size of 60mJ/cm^2 (36% higher than for MOR) as shown in table 4. Unbiased roughness is also similar.

By varying the resist film thickness from 23nm to 28nm, we found a very similar resolution for PR1 while exposure latitude slightly dropped for all 3 resists. Unbiased LWR/LER has been improved by 15% as expected for a thicker film as detailed in Table 5.

Starting from these promising lithographic performances, several experiments have been carried out to transfer L/S features into the underlying stacks for a resist film thickness of 23nm. We first performed sequential three steps etch: into 5nm UL2 then etched 6nm of SoG before final transfer into APF. The top-down SEM images of the L/S patterns after

litho and after the three steps are shown in Figure 6. After the organic underlayer etches, the SEM images contrast is too poor and conclusions are difficult to be made at this stage. The selectivity between photoresist and UL is poor and that leads to thinning down the photoresist budget or even having only organic UL remaining as a mask. After SoG etch, the L/S patterns seem opened as per top-down SEM images. After APF etch, we see many bridges on L/S patterns of CD 6-7nm; which indicates that the SoG was not fully opened. As the SoG etch process is too polymerizing, the CD is maintained and this prevents us to see under SEM conditions the real line patterns. We believe that high-density plasmas are too aggressive for this process and stack conditions. In addition, the post-development thickness of the chemically-amplified photoresist appears to be too low for the patterning of this particular stack and has been evaluated in Section 4.

For 28nm photoresist thickness, we applied the same etching process to the wafer and observed better pattern transfer. Indeed, increasing the photoresist thickness hence the PR etch budget is helping to get a more robust process with minimized line breaks as shown in top-down SEM images after APF etch of Figure 7. However, we noticed some bridges may be due to SoG not being fully opened still and L/S features are still thin below 8nm CD. So even with increased PR thickness, it appears that 28nm FTH is not sufficient to open both UL2 and SoG layers.

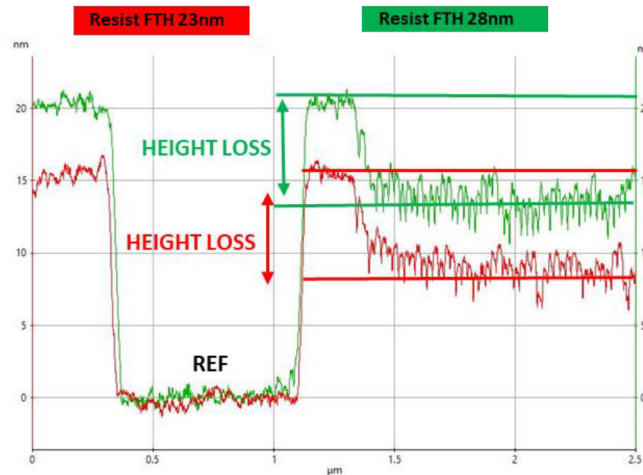Based on previous etching results, we have performed additional ex-

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Figure 11. Post-develop resist step height of P24 CAR L/S patterns for 23nm and 28nm resist FTH.

posures on the same stack but without an organic underlayer to simplify the etch process. At P24nm L/S features can be achieved at a resisting thickness of 23nm without major collapse post-lithography. After stack etching into APF, we observed under SEM the same issues as previously: too thin lines with many line breaks. If removing UL2 simplifies the process, the resist thickness of 23nm doesn't guarantee we have enough PR budget to open the 6nm SoG layer for P24 L/S. Nevertheless, we observed better pattern transferability on the same wafer for P26 & P28 L/S patterns as illustrated in top-down SEM images in Figure 8. We see for P26 L/S features still some breaks and bridges but much fewer defects for P28 L/S patterns, which means that the PR budget is probably pitch dependent: the tighter the pitch, the less photoresist remains after development. That must be confirmed by thin film metrology and will be discussed in Section 4 of this paper. The mechanical resistance of the photoresist lines is crucial here and tighter pitch also means tighter CD in this example, thus higher Aspect Ratio and mechanically weaker lines.

In an additional experiment, after etching UL2, we perform Atomic Layer Etching (ALE) of SoG and a partial 5nmdeep APF etch with a resist thickness of 23nm. After partial APF etch, lines are very rough, and litho/etch CD bias is 1.5nm as described in Figure 9. That can be explained by the polymerization of the SoG etch process which leads to some polymer redeposition around the lines and hence enlarges the CD. Once the full APF stack is etched, we observed, similarly to our POR etch tool, thinned lines of CD 7-8nm with some breaks and bridges. The entire etch challenge appears to be related to the density of species in the plasma and not so much to the ion energy or tool process design (conventional RIE or ALE).

Solving this issue would only be possible if we consider low-density plasma etching combining low RF frequency and low-pressure processes. The challenge coming along with this kind of plasma is the reliability of the plasma to strike as a critical density of electrons needs to be reached to strike and maintain the discharge. The first experimental validation of this process shows improvement in pattern transfer for P24 L/S patterning on APF/SoG stack and photoresist film thickness of 25nm as illustrated in Figure 10. No breaks are observed in L/S features, although still, some bridges are present. We believe that low-density plasmas processes are very promising and may help for further demonstration of P24 CAR L/S pattern transfer into a full stack. However, the main limitation is on hardware capability to allow for such working conditions and will need more investigation.

4. Thin Film Metrology Towards CAR P24 L/S Transfer Demonstration

To further investigate the patterning issues seen for CAR P24 L/S pattern transfer, we would like to evaluate the photoresist budget as precisely as possible. Indeed, it is known that after EUV exposure and development, the remaining photoresist thickness is small, especially when starting with an already thin layer. However, it has not been evaluated. In this work, we have chosen to use the benefits of Atomic Force Microscopy to measure pattern height post-development and get the remaining photoresist thickness of our CAR processes without damaging our wafers for further etching development. Thinner resists allow higher scanning speed and a small aspect ratio gives more accurate measurements.

In this case, we evaluate two CAR samples of 23nm and 28nm POR resist film thickness after coating. After exposure and development, AFM metrology is performed on the 2 wafers; the methodology used has been described in the co-author paper[9] with three main regions of interest: the blanket region which corresponds to the developed part without the density of patterns, the reference region (0nm) and the array region where we have our L/S gratings. For P24 L/S features, we obtained at the central dose and focus a resist remaining thickness of 15nm and 20nm for samples of 23nm and 28nm coated resist thickness respectively. So, after development, 8nm of resistance is already lost as seen in the left part of Figure 11, the blanket region. In addition, we observed in the region of the L/S array (right part of the figure) a height loss of 8nm for both photoresist samples after development, potentially due to the higher acid diffusion in that region where we have the highest pattern density. This post-develop thickness loss needs to be considered for pattern transfer, especially at tight pitches. That means we have a remaining photoresist thickness of 7nm for the 23nm resist sample and 12nm for the 28nm resist sample, which corresponds to our PR budget to etch the 6nm SoG layer + 5 nm of the organic underlayer. The AFM metrology illustrates here how challenging the pattern transfer of our current CAR stack is, when we have poor selectivity between the materials to be etched.

We performed additional AFM measurements on PR1 (cf Table 5) at two thicknesses of 23 and 28nm to evaluate resist height loss through exposure dose at three different pitches of P24, P26 & P28 for comparison. For both samples we observed at P24 L/S an increase of photoresist height loss through dose as shown in Figure 12; the higher the dose the higher the height loss which corresponds to smaller lines CD. In this example, the remaining photoresist thickness after development is 16nm and 21nm for samples of 23nm and 28nm coated resist thickness respectively; like

Figure 12. Post-develop PR1 resist height through a dose of P24 CAR L/S patterns.

Figure 13. Post-develop PR1 resist height through the pitch of CAR L/S patterns at two different RFTH.

the results obtained with our POR photoresist (Figure 11).

We have measured post-develop resist height loss through pitch and plot it through exposure dose for the two resist film thicknesses. We observed the same trend in height loss through dose with an increase at a higher dose and low lines CD, see Figure 13 for illustration. The resist height loss is more pronounced for a thicker coated film with about a 1nm difference, but it remains within the error range. Similarly, the height loss comparison through pitch reveals that at a similar dose there is no big variation in height loss in the pattern's region for P24, P26, or P28. We are probably already in very aggressive feature dimensions.

Exploring through pitch and through dose L/S arrays profile by Atomic Force Microscopy allows us to understand the limits of the Car pattern transfer process, separately from the etching process itself. The first limitation comes from photoresists themselves; in our case, two CAR resists have been analyzed with similar results showing a combined resist thickness loss of 16nm, more than 50% of the initial coted thicknesses of 23 and 28nm. The PR budget for etching is therefore not sufficient to etch the subsequent layers; as explained in Section 3.3, it is a limitation for both Reactive Ion Etching (RIE) and Atomic Layer Etching (ALE) tools. AFM should be systematically used to allow for realistic estimation of the photoresist budget before any etching process development when

it comes to tight pitches like P24.

To overcome this issue, we would investigate alternative CAR resist platforms and compare them in terms of remaining PR and thus anticipate eventual showstoppers.

Next to its use for PR etch budget estimation, AFM has also the potential for accurate imaging in L/S gratings that could reveal additional defects post-development that are not always seen under SEM. It can be for line breaks or bridges for instance. In the early AFM experiment on P24 L/S with POR resist, we have found in the L/S pattern some holes that can be translated as line breaks for certain exposure conditions. When comparing the images with top-down SEM ones, we could barely notice any breaks as illustrated in Figure 14. When calculating and plotting the process window (PW) after development, we should consider including all the stochastic failures, the ones from AFM as well. Those breaks are most probably transferred during the etching of the UL and SoG and limit the PW after etching.
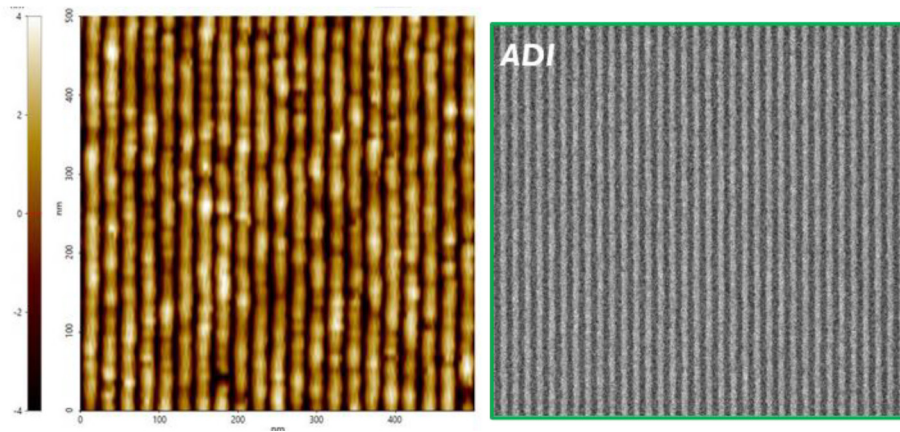
Figure 14. CAR P24 L/S patterns AFM (left) and SEM top-down (right); black holes are considered line breaks.

5. Conclusions

This study investigated the L/S patterning readiness towards high NA. We focused on materials, processes, and etch transfer investigation for P24 Line Space features by using NXE:3400B EUV scanner at 0.33 NA. The goal is to enable full ecosystem development including high resolution resists, new processes availability and advanced etch tools. Additionally, accurate metrology on thin films has been investigated. All wafers were processed in a 300mm fab-like environment. We optimized the aerial image and allowed for fading corrections in illumination sources (high NILS). 24nm pitch L/S printability was shown in both Metal Oxide Resist (MOR) and Chemically Amplified Resist (CAR). We demonstrate pattern transfer of MOR L/S features and investigate CAR pattern transferability challenges. Atomic Force Microscopy (AFM) has been used for better understanding and further mitigation.

To print dense L/S at pitch 24, we have compared two illumination conditions: a half-leaf dipole and a dipole with Z6 injection on Si + SoG and on a representative patterning stack. The dipole with injected Z6 allows for a 15% higher process window thanks to a gain in contrast and reduces dose sensitivity compared to the half-leaf dipole.

By means of a design of experiment in which post-exposure bake and hard bake temperatures are varying as well as photoresist thickness, we demonstrate P24 L/S patterning on a stack with metal oxide resist (MOR) at an exposure dose of 45mJ/cm^2. Lithography conditions were chosen to obtain the best wafer performances after development and L/S features of 11nm at 24nm pitch have been successfully transferred into patterning stack with no or limited defects for coated film thicknesses of 22nm. For the 16nm film thickness case, further optimization is needed on the litho and etch processes to achieve full pattern transfer demonstration.

Furthermore, we study chemically amplified resist (CAR) printability on three resists samples under different lithography process conditions through a design experiment. We show CAR printability performances for L/S features at P24nm with a good process window and limited defects at an exposure dose 60mJ/cm^2. We validate the improvements made towards CAR resist to fulfill the requirements for small feature printing. We investigate patterning stack options for CAR pattern transfer and do some compatibility checks between several materials to find a good combination that will allow etch transfer of L/S features at P24nm. First CAR pattern transfer of L/S into stack results are very promising and pave the path towards P24nm L/S CAR pattern demonstration, despite some stochastic failures such as line breaks or bridges observed.

To investigate patterning issues seen in CAR transfer development, we assess thin film metrology by using Atomic Force Microscopy. We measure post-development resist remaining thicknesses on blanket areas and on dense L/S areas. We found a total resist height loss of 16nm for coated film thicknesses of 23 and 28nm. It helps us understand the additional etch challenges due to the low PR budget for successful pattern transfer of P24nm features. We also explore the impact of total resist height loss through exposure dose and through a pitch. We noticed a trend in resist thickness loss that increases through dose. The variation through pitch is however limited to the three studied pitches of 24nm, 26nm, and 28nm. Finally, we compared resist height loss of two different CAR materials and found no or limited difference which is expected as the two resists came from the same platform.

In summary, the infrastructure's readiness for materials, processes, and etching are now identified at the Imec-ASML advanced patterning center to soon transition to high NA lithography. Preliminary work on thin film metrology has been carried out and further work on going for fundamental understanding and challenges mitigation. We show P24 L/S pattern transfer readiness for metal oxide and chemically amplified resists. Close to that, next generation of dry deposited and dry developed resists are currently under investigation.

6. Acknowledgements

7. References

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■ Global Total Semiconductor Equipment Sales on Track to Record $118 Billion in 2022, Semi Reports

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https://www.semi.org/en/news-media-press-releases/semi-press-releases/global-total-semiconductor-equipment-sales-on-track-to-record-$118-billion-in-2022-semi-reports

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https://investor.lamresearch.com/news-releases/news-release-details/lam-research-entegris-gelest-team-advance-euv-dry-resist

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