PHOTOMASK

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EMCL16 Best Paper Award

Translation of lithography variability into after-etch performance: monitoring of “golden” hotspot.

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Introduction

In the early phases of technology development, designers and process engineers have to converge toward efficient design rules. Their calculations are based on process assumptions and result in a design rule based on known process variability capabilities while taking into account enough margin to be safe not only for yield but especially for reliability. Unfortunately, even if designs tend to be regular, efficient design densities are still requiring aggressive configurations from which it is difficult to estimate dimension variabilities.

Indeed, for a process engineer it is rather straightforward to estimate or even measure simple one-dimensional features (arrays of Lines & Spaces at various CD and pitches), but it starts to be less obvious for complex multidimensional features. After a context description related to the process assumptions, we will outline the work flow which is under evaluation to enable robust me-

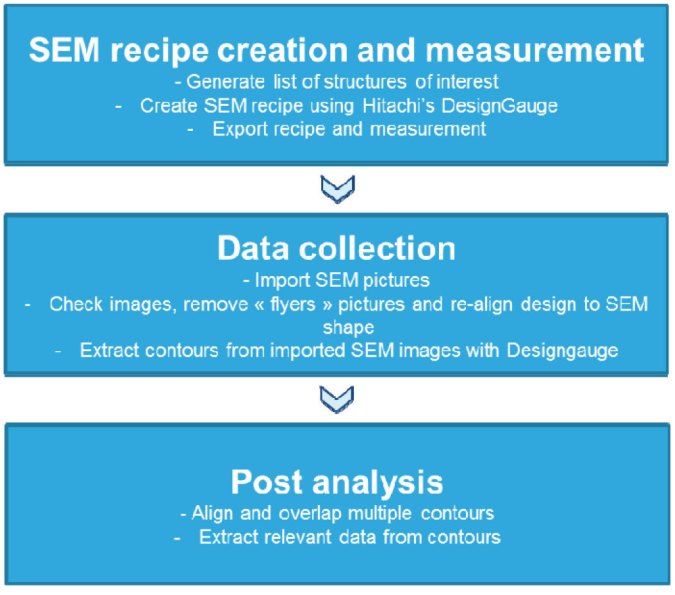

Figure1. Contour extraction flow.

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EDITORIAL

EMLC 2016—The 32nd European Mask and Lithography Conference

By **Uwe Behringer,** UBC Microelectronics, EMLC 2016 Conference Program Chair

European Mask and Lithography Conference (EMLC), the annual two day conference brings together scientists, researchers, engineers, and technologists from research institutes and companies from around the world to present innovations at the forefront of mask lithography and mask technology. EMLC is dedicated to the science, technology, engineering and application of mask and lithography technologies and associated processes, giving an overview of the present status in mask and lithography technologies and the future strategy where mask producers and users have the opportunity of becoming acquainted with new developments and results.

EMLC adopted a different Call for Papers process for this time. In December 2015, 10 members of the EMLC 2016 Program Committee met in Dresden and defined nine topical "highlights." For each highlight, we asked two committee members to bring these sessions to life (i.e. fill with papers).

EMLC 2016's highlight sessions were: "Mask Patterning, Metrology & Process"; "Wafer Lithography"; "EUV"; "Modelling & Computational Process Correction"; "Photonics": "More than Moore, IoT & Manufacturing Challenges"; "Using the Data"; "Novel Approaches" and "NIL".

Beside Mask and Lithography technologies for Semiconductor and MEMS the EMLC Program Committee added, Photonics and IoT (Internet of Things). Photonics is a large community worldwide and they were happy to join us and, no surprise, this group delivered excellent presentations.

As Welcome Speaker and first Keynote speaker we were pleased to introduce Rutger Wijburg, senior vice president and general manager of GLOBALFOUNDRIES Fab 1 in Dresden, Germany. He is also responsible for the global Manufacturing Technology and Central Engineering organizations. His presentation, "The Semiconductor Industry in Transition: An European Perspective," showed that Semiconductors are dominant in value creation: ~$333B Sales in 2014, $1200B Sales in Electronic Systems, $5000B Sales in Services, 25% GDP-growth (EU), 40% productivity growth (EU). He mentioned that the traditional growth market are flattening and the coming IoT market requires new chip solutions with low power and low cost. He also mentioned, that Europe has missed most of the value creation associated with the PC wave (> $300M/year, $1/mm2 Si) and Mobile wave (>$1.5 B/year, $0.25/mm2 Si). The next wave is building: the IoT (>$20-50 B, $0.05/ mm2 Si). Finally he concluded: Besides cost, we need to keep variability under control… with lithography and masks being a major knob. New sophisticated OPC algorithms need to be applied to prevent expensive double patterning at multiple layers: Extensive application of SMO (Source – Mask - Optimization) algorithms taking advantage of ASML's free form source technique. One also requires intensive cooperation between the mask shop and the Fab and establishing a "zero defect" philosophy in the mask shop by AMTC – Fab1 interaction.

As second Keynote speaker, Naoya Hayashi from Dai Nippon Printing presented: "Challenges and Prospects of Next Generation Masks," the status of the worldwide mask technologies. EUVL now has improved source power to >100W at >70% availability. Mask infrastructure program succeeded to introduce Actinic Blank Inspection (ABI) tool for HVM. For NIL, defect reduction for memory device application in template fabrication, wafer process, tool adder, was demonstrated for production. There is an expanding community for memory industry.

Our third Keynote Speaker, Yu Cao from ASML Brion in Silicon Valley, presented "Computational Lithography for Process Window Enhancement and Control". He stated that OPC is required for advance masks to ensure printability. 3D mask effects became important since the 32 nm node. Computational lithography has evolved with lithographic processes and enabled applications in process window enhancement and control. This key metrics are model accuracy, optimization, performance and throughput. The advances required innovation in physical understanding, numerical algorithms and computing technology.

The attendees of the EMLC 2016 voted for the Best Paper / Best Presentation of EMLC 2016. With 65% of all evaluation sheets filled out, the result: "Translation of lithography variability into after-etch performance: monitoring of 'golden' hotspot" presented by Jo Finders from ASML, by J. Finders, T. Kiers, ASML, Veldhoven, The Netherlands; B. Le Gratiet, and A. Lakcher, ST Microelectronics, Crolles, France.

New this year was the session on Photonics. There were 5 presentations from Germany and the Netherlands. What did we learn? In his talk, Mr. Grote from the Fraunhofer Institute for Telecommunication in Berlin presented: 1.) Fabrication of InP based Photonic Integrated Circuits using a Foundry Model. 2.) Hybrid integration: Micro-optical assembly on planar waveguide board (PLC) (silica; silicon(oxy)nitride; polymers). 3) Silicon platform (Si-Photonics), Photodiodes, modulators, passive waveguides, gratings. 4.) III-V (InP): full monolithic integration, Lasers, optical amplifiers; photodiodes, modulators, passive waveguides.

In Summary:
Photonics: There is a tremendous push towards using more and more data from measurements and background modelling to improve process yield. Sophisticated big data methods are integrated and help to find the optimum process. Stitching errors remain the main challenge in lithography when it comes to the fabrication of photonics devices with subwavelength periodic structures, such as diffraction gratings in DFB lasers. The need of combining UV

(CONTINUES ON PAGE 11)

BACUS

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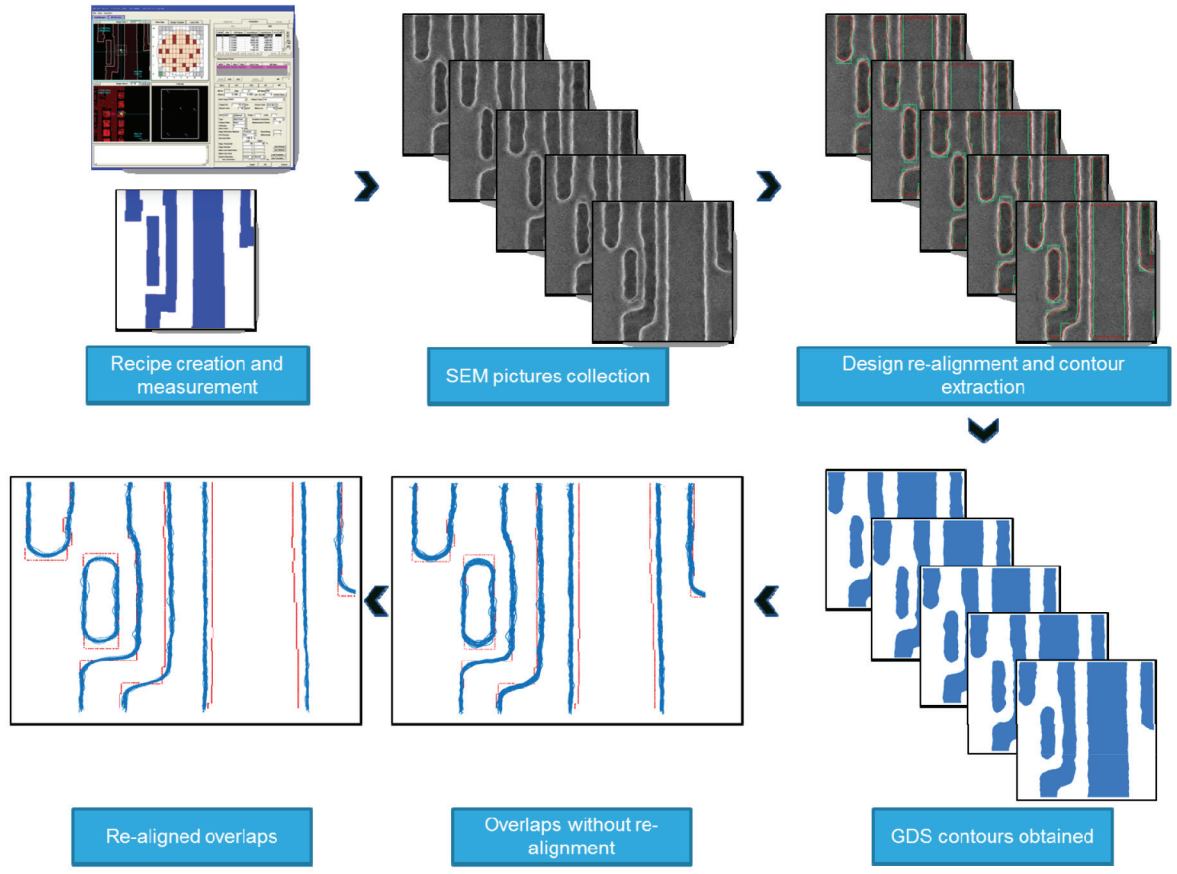


Figure 2. Contour alignment strategy. The overlaps are done with multiple contours extracted after wafer exposure at nominal conditions. The red shape corresponds to the mask structure. After re-alignment, the noise is reduced.

trology of 2 dimensional complex features. Enabling new metrology possibilities reveals that process hotspots are showing complex behavior from lithography to etch pattern transfer.

In this work we studied the interaction of lithography variability and etching for a mature 28 nm CMOS process. To study this interaction we used a test feature that has been found very sensitive to lithography process variations. This so-called "golden" hotspot shows edge-to-edge geometries from 88nm to 150nm, thus comprising all the through pitch physics in the lithography pattern transfer [1,2]. It consists of three trenches. From previous work it was known that through trench there is a systematic variation in best focus due to the Mask 3D effects. At a given chosen focus, there is a distinct difference in profiles for the three trenches that will lead to pattern displacement effects during the etch transfer.

Process Assumption, Need to Know More About Variability

Process tools capabilities are really challenged by the need of aggressive design rules for competitiveness. Design rules used to be defined by "rules out"-rules, saying that everything which is not forbidden is by essence authorized. Since recent nodes and even more aggressively for the 28nm node, the need to run process assumptions is mandatory to accurately calculate design rules that are process capability aware. These calculations have to be made not only looking for yield failure criteria's (say a short or open circuit situation) but mostly for reliability (dielectric breakdown, electro migration, implantation shadowing …), especially when the products are addressing markets like automotive where longevity of the product is required.

Process assumption is a contract between process, process integration and design. If we take a typical process assumption equation for a minimum distance between two layers A and B as an example [Eq.1] we'll find 3 main contributor families.

$$DR = Min_d + \frac{Bias_A}{2} + \frac{Bias_B}{2} + \frac{4}{3}\sqrt{\left(\frac{3\sigma_{CD\_A}}{2}\right)^2 + \left(\frac{3\sigma_{CD\_A}}{2}\right)^2 + \left(3\sigma_{OV\_AB}\right)^2} \quad (1)$$

The Design Rule (DR) is calculated as a function of:

1. A Criterion (Mind) corresponding to a failure mechanism at the origin of the rule (e.g:a dielectric breakdown, a percentage of area coverage).
2. A process Bias (BiasA, BiasB) corresponding to the difference CAD versus Silicon, saying all effects leading to Silicon edge systematically not being placed where it is drawn. This comprises Bias CD, Bias table correction error, Stack effects, OPC edge placement error, Corner rounding and many others systematic process effects that will not be compensated.
3. A process variability estimation (3 sigma: 3sCD, 3sOV) corresponding to the CD uniformity performance, Line Edge Roughness, Overlay, CD slopes effects. From all process sources (Mask, lithography, etching, metrology, OPC ….)

In this kind of equation a 4/3 ratio is used to give enough margin thinking of ppm level of reliability criteria.

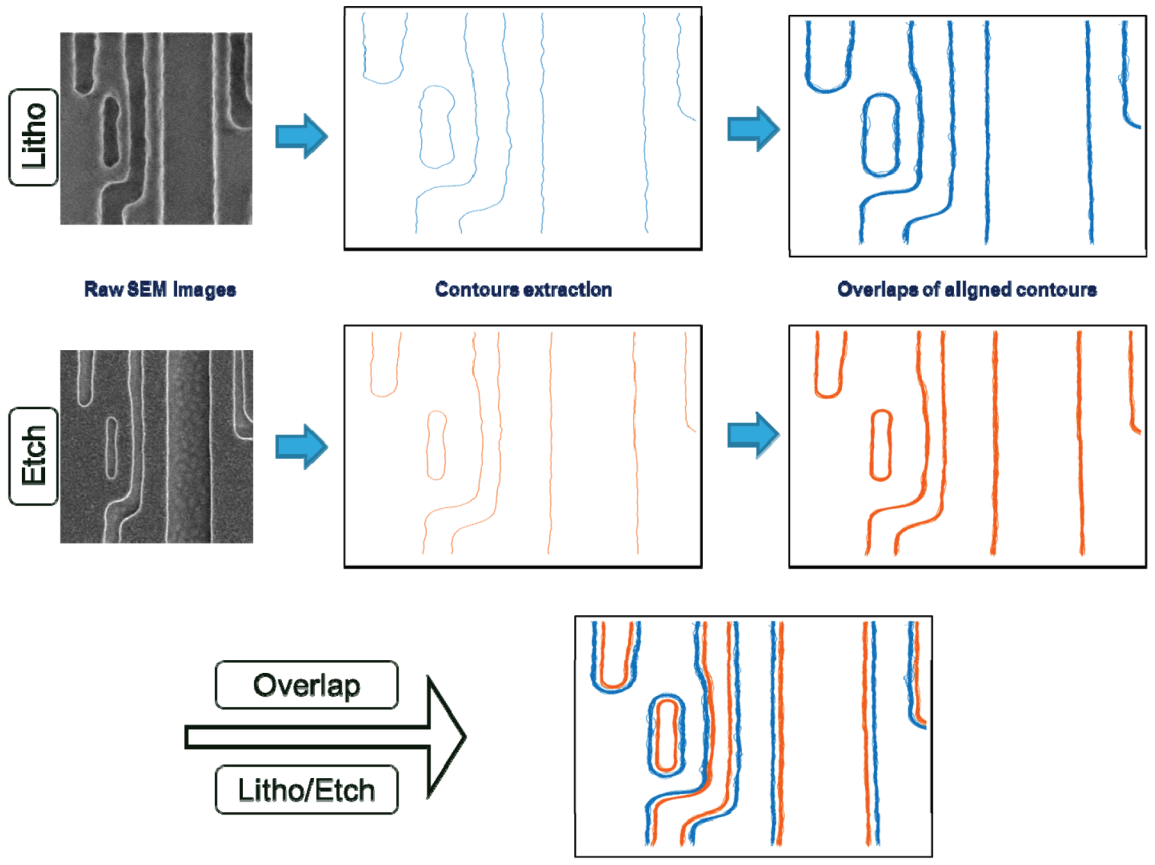


Figure 3. Litho to etch comparison methodology at nominal conditions.

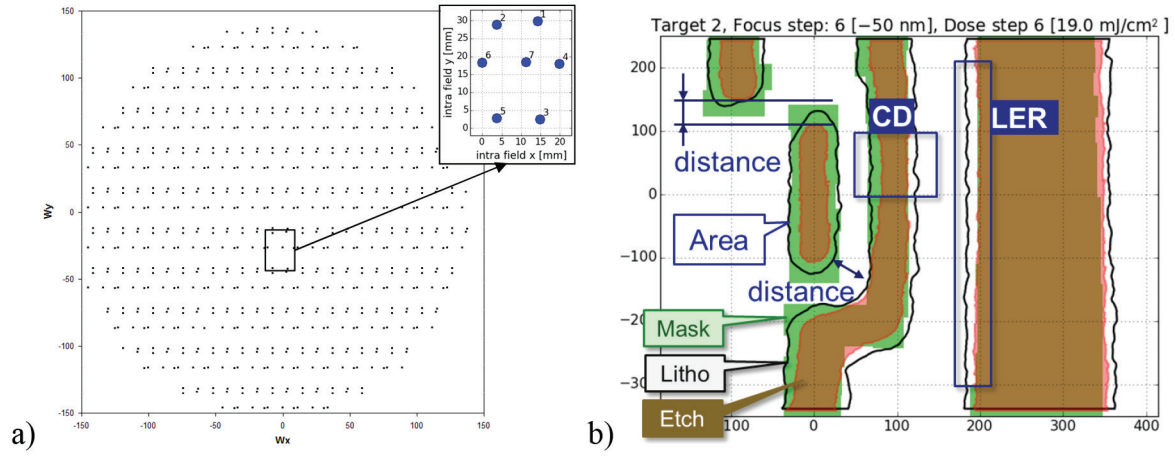


Figure 4. a) Wafer sampling, full map & 7 positions in Field b) Extracted profiles and examples of possible metrics and measurement boxes on aligned patterns (mask, after litho and after etch).

One of the many challenges in these discussions is the estimation of the real process variability of complex configurations like tip-to-tip, tip-to-line, area overlap and corner rounding. Most of the time it comes out of OPC metrology blocks fields that are characterized in terms of PV bands when varying dose and focus on a focus exposure matrix as an example. This is not really a proper estimation of process variability, this one being assessed out of in-line control charts from which a robust metrology is needed (and therefore most of the time 1D arrays). If we are able to give a global budget breakdown in term of lot to lot, wafer to wafer, intra wafer or intra field variations for 1D features, it is often pure extrapolations from OPC PV bands when looking at 2D features. Enabling a new robust complex metrology of these curved shapes is a challenge and a breakthrough for process people who will have access to new information to assess and optimize their processes.

SEM Contour Extraction

CD-SEM images provide a wealth of information that is not easy to handle when it comes to in-line process control. In-line CD-SEM measurements have to be robust, repeatable because they will be linked to control loop systems. Too much noise on the measurement will lead to unstable loops. As a consequence, in-line metrology often relies on 1D array structures from which process capability and set point can be monitored. There is a lot of valuable information that can be extracted from 2D features like tip to tip, tip to line, area, corner rounding and image placement. For some of these examples some measurements would be possible but the measurement boxes must be accurately placed and furthermore the measurement algorithms are somehow limited leading to non-robust and non-repeatable solutions. For others (like edge placement, line end) there is simply no reference visible on the image.

CDSEMs are providing high quality images from which contours

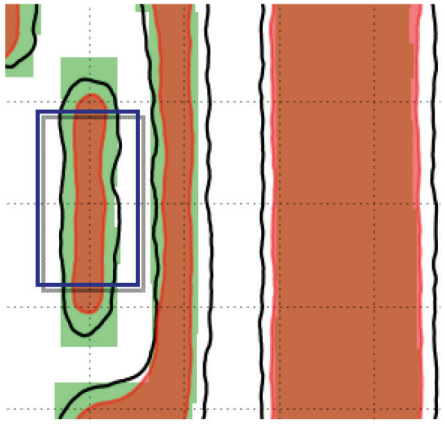


Figure 5. Vertical trench on which CD is measured.

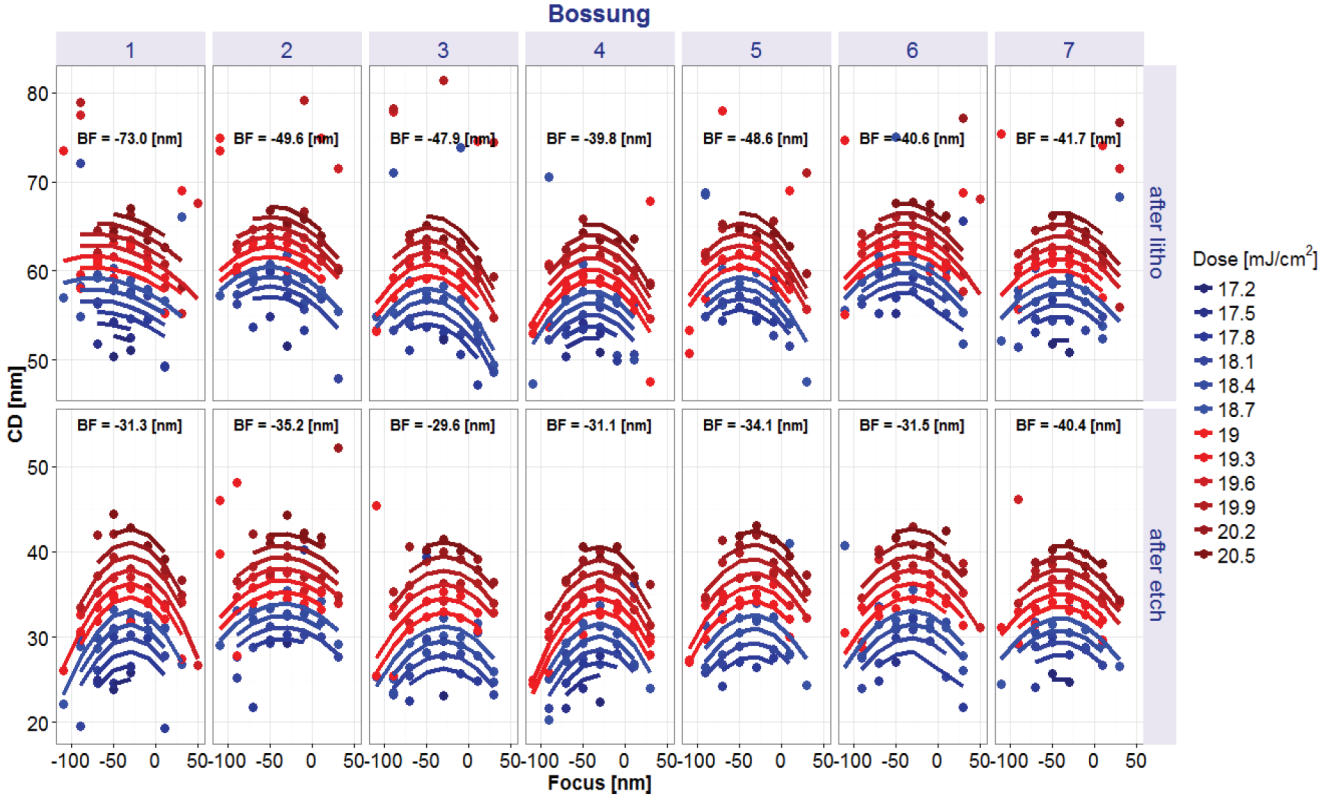


Figure 6. CD as a function of focus and dose for different intra field locations and processing steps: ADI and AEI.

can be extracted and pulled into GDS based tooling which are offering much more possibilities, one of which being the positioning of an image relative to its design GDS target [3]. Using CDSEM as a provider of high quality images and performing remote data treatment in another environment is a solution that is currently investigated by many actors in our industry [4, 5, 6, 7, 8] and this is also presented in this paper. The process flow is then as given in Figure 1.

There are several key steps that need to be handled depending on the purpose of the measurements.

- When looking at process window estimation, with varying dose and focus, 2D patterns tend to quickly change shape due to their reduced process window. In this case contour extraction of a complex hotspot will lead to a broad spectrum of shapes that can be difficult to align together.
- When looking at process variability at process set point, one will want to analyze a high quantity of images in a short time frame. This is especially true, if the measurement results have to be fed back into the in-line production control environment.
- For both cases, when performing a measurement to a reference design there will be a need to align all the contours extracted from many images to a single reference, as well as performing some kind of contour averaging [4, 5, 7] which is not straightforward.

Extracting image contours using tools like in our case Design-gauge gives access to a database of contours that will need further

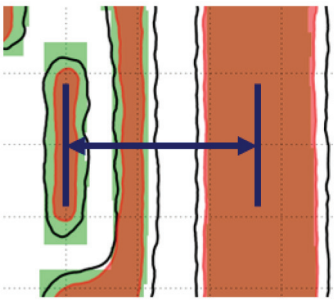


Figure 7. Distance between two patterns.

SEM Contour Metrology

The experimental data set consists of 2 blocks:

- A 'Focus Exposure Matrix' (FEM) in which each field has been given a programmed focus and dose offset. This data is very handy to observe the response of the hot spot due to known focus and dose variations.
- A 'CDU' data set, in which all fields are exposed under the same nominal conditions. This data depicts the across wafer variation.

When comparing the ADI and AEI data, one needs to be aware of the fact that – in this case – not the very same wafer is used.

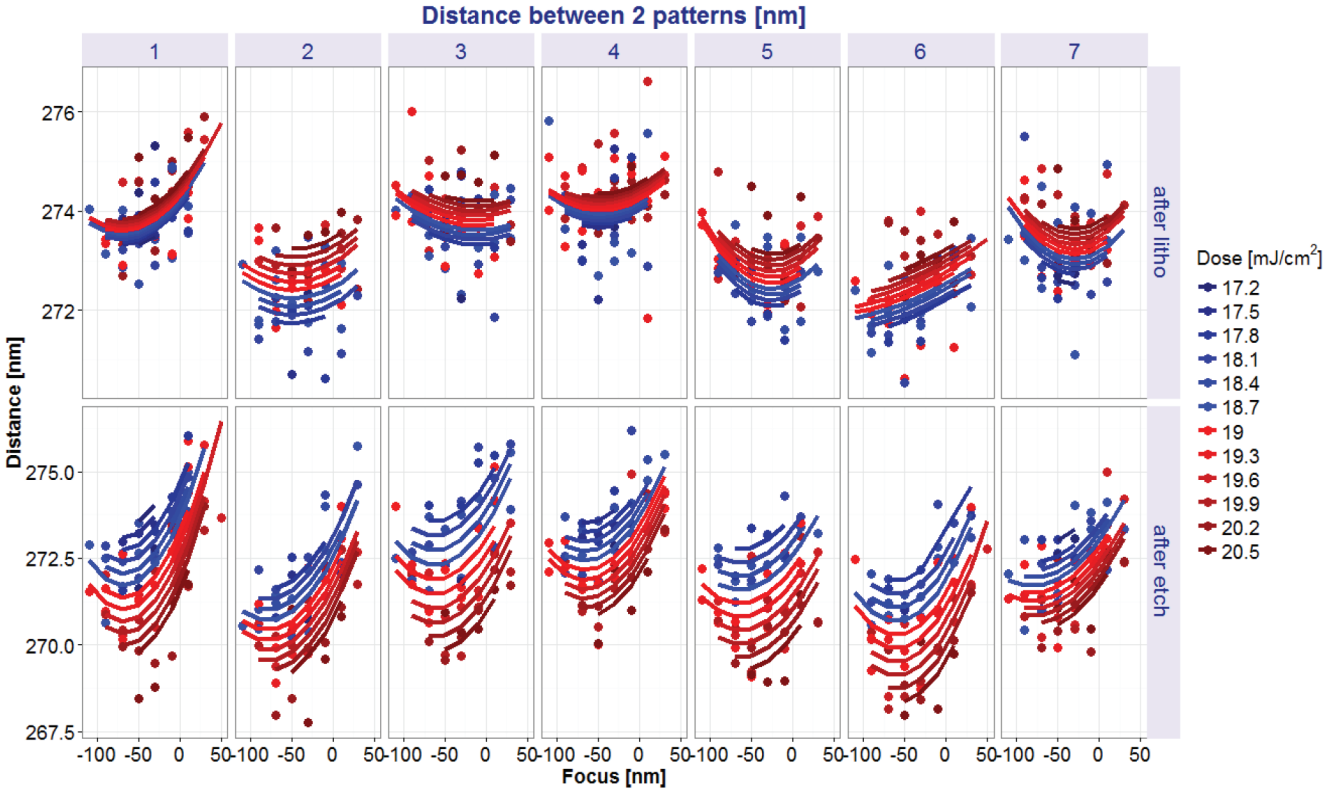


Figure 8. Distance between patterns as a function of focus and dose.

manipulation before undergoing metrology. The first one is the alignment of all the contours (of a same feature) to a reference. If not doing so, image alignment to the reference will generate some noise. Indeed, the way the SEM aligns a structure in an image has to be taken into account. The centering of the structure varies from an image to another. Even if the variation is small compared to the field of view, a few nanometer affects the precision needed for such metrology. The second one is the development of an offline measurement methodology to extract relevant information from the contour data that is generated. This can be done using the obtained contour GDS files.

This paper focuses on the study of a so-called golden hotspot at lithography and etch level. Post lithography and post etch contours are overlapped across process window and at best conditions. The strategy for contour alignment to a reference is shown in Figure 2.

The methodology shown in Figure 2 can be used to study litho to etch effects by comparing exposed wafers to etched wafers in order to measure etch bias.

Hence, subtle differences between the ADI and AEI data can be due to wafer to wafer differences.

After having the contours aligned it is a matter of choosing metrics and placing measurement boxes. In Figure 4 an example with possibilities is shown. Some measurements can be done by the CD SEM, but more complex ones are better done offline, since there it is easier to identify and treat possible outliers. In an exploratory phase the litho and etch engineer need to work together to determine the key performance indicators.

Example 1: a simple Bossung; CD as a function of focus and dose

Using the line width of the small vertical trench – as indicated in figure 5 – for each of the 7 locations in the field a Bossung is measured (cf. figure 6). The Bossung curves look as expected.

The noise in the 'after litho' data is larger than in the 'after etch' data: largely due to the 'line edge roughness'. The contrast in the SEM images on the resist patterns is rather low which leads to large

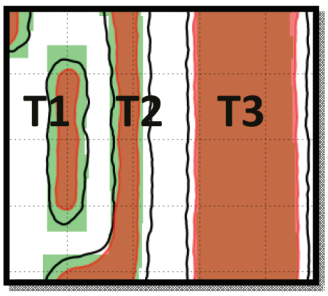
changes in the edge position with small differences in grey scale.

To counter the noise in the Bossungs a simple model was applied in combination with a robust fitting algorithm (weighted least squares).

$$CD = a_{00} + a_{10}.F + a_{20}.F^2 + a_{01}.D \quad (2)$$

The position of the Bossung top after etch is on average (over the 7 intra field locations) -33 nm which is close to the designed value of -30 nm. The positions of the Bossung tops after litho is -45 nm (even when ignoring the Bossung at intra field location 1, which suffers so much from missing points and noise, that the whole curve changed), indicating that the etching process has a different impact on the left side of the pattern and the right side of the pattern.

Figure 9. Pattern labeling.



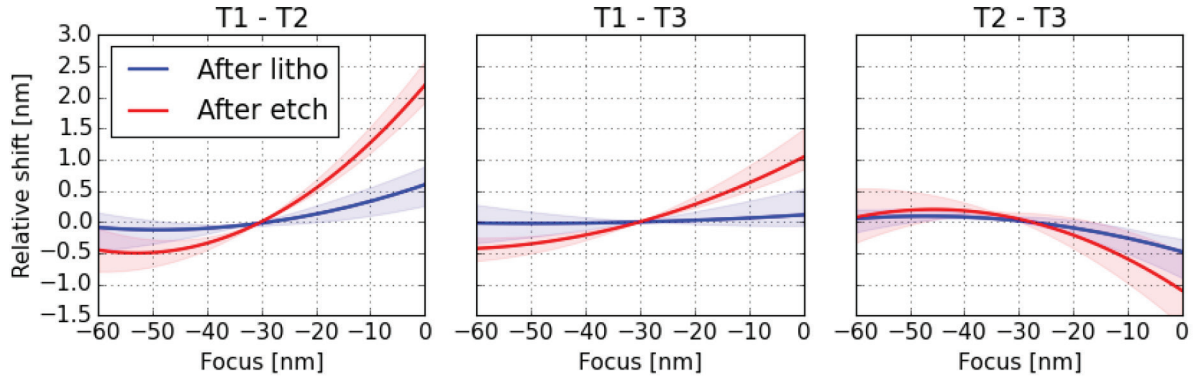


Figure 10. Relative pattern shift (averaged over all intra field locations) as a function of focus. The pale filled contours indicate the minimum and maximum values over the intra field locations.

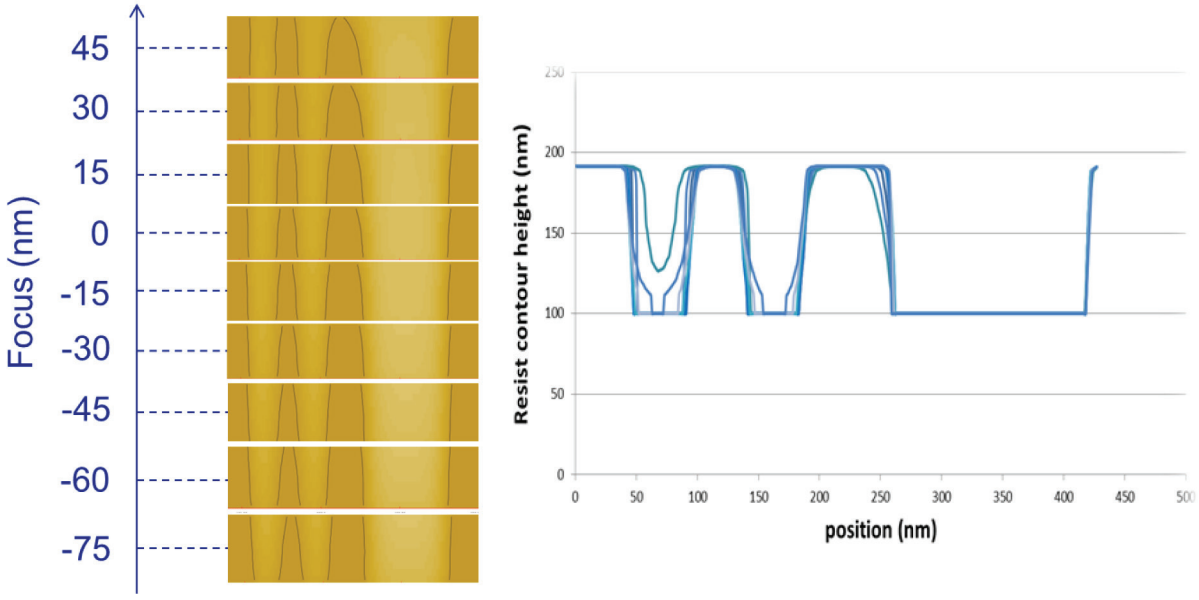


Figure 11. simulated resist cross-sections through focus.

Example 2: Distance between two patterns as a function of focus and dose

Apart from measuring the line width of a pattern, it is also possible to measure the distance between two patterns. An example is given in Figure 7. A measurement box was placed over the lines and the edge locations of the two patterns under consideration were calculated. Going through focus and dose in a FEM causes the line to shrink: not only in width but also in length. Unlike a CD SEM with fixed measurement box height, using the contours it is possible to dynamically adjust the box height in such a way that line ends are never included.

The distances after litho show a “Bossung” type behavior, but the noise is relatively high. Extracting a ‘best focus’ out of these

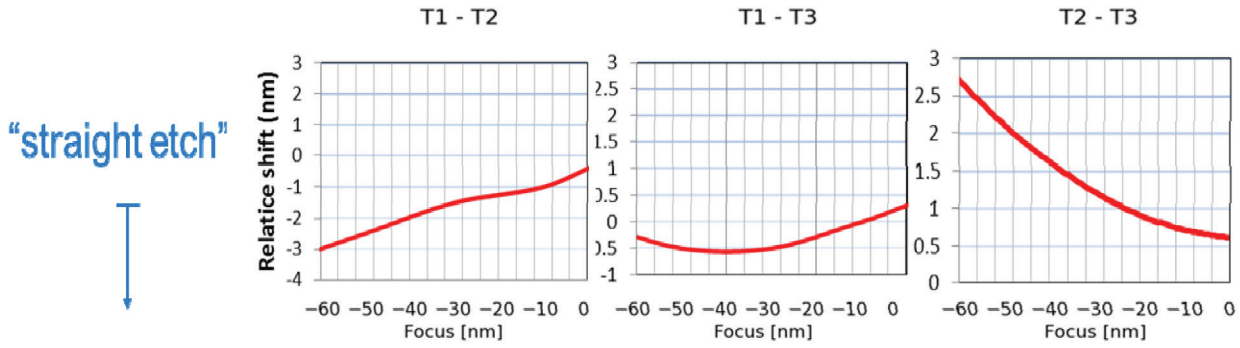


Figure 12. Simulated relative displacement of the three edges after performing a straight etch into the TiN layer.

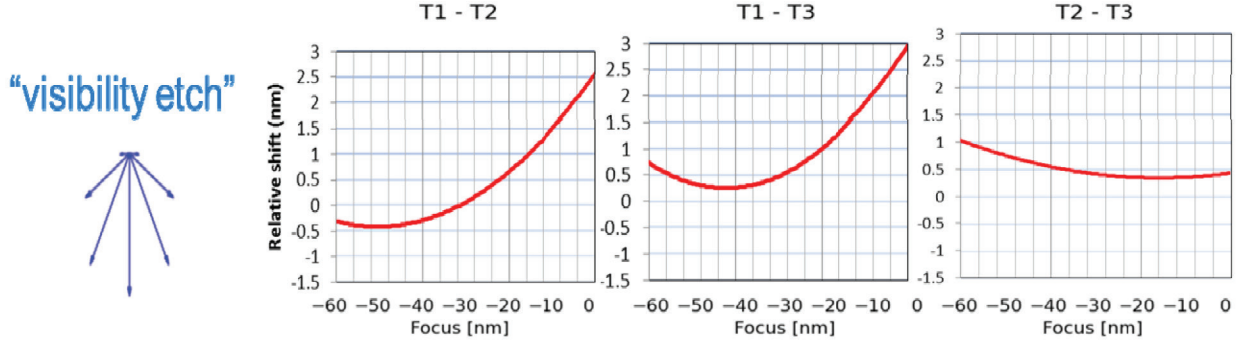


Figure 13. Simulated relative displacement of the three trenches after performing a "visibility" etch into the TiN layer.

Bossungs won't yield meaningful results. The results after etch show a lot less noise and a more clear Bossung behavior. The dependency of these distances of mainly focus implies the presence of a pattern placement error.

Example 3: Pattern placement

Let T1, T2 and T3 be the three patterns as shown in Figure 9. As in the previous example, it is possible to measure the distance between T1 and T2, T2 and T3 and T1 and T3 as a function of focus (cf Figure 10). The after litho data was averaged over the 7 different intra field locations and shows little variation in distance between the patterns as a function of focus. On average, an effect of less than 1 nm is observed when going 30 nm out of focus. The response after etch is much bigger: a pattern shift of 2 nm is observed for all the locations in the field (making this less likely to be a random event). Compared to ever tightening overlay budgets this is a rather big effect.

The root cause of this effect is assumed to be related to side wall (SWA) angle differences through focus. The CD may be constant, but the response to etch may be SWA dependent causing an effective pattern shift.

Pattern Placement Shifting: Studying the Transfer from Lithography to Etch

The observed displacement of the three individual trenches (as shown in Figure 10) which is enhanced after etch gave rise to the questions: which mechanisms are driving this?

Previous work [9] has shown that the three trenches of the hotspot have different profiles. The mask topography leads to enhanced Mask 3D effects which lead to different profile per feature and even per edge.

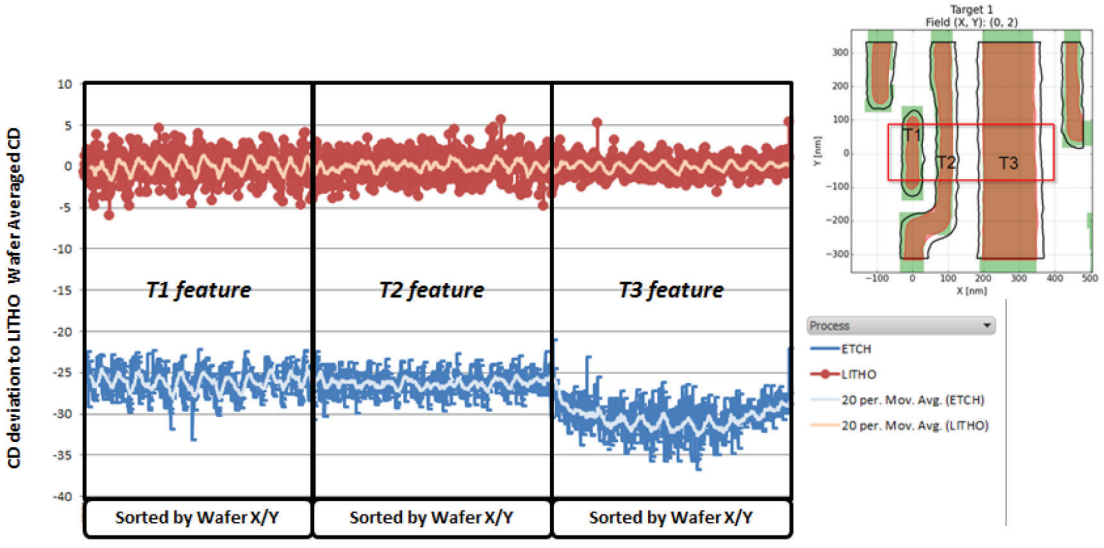
Figure 11a shows simulated cross-sections of the resist profile for the three printed trenches at different focus setting during exposure. For the left trench straight resist profiles are expected at focus setting of 45nm, for the right trench the best profile is observed at -75nm. To illustrate the differences per edge, resist cross-section contours for the 9 focus are overlaid in Figure 11b.

Strong differences are observed per edge. The right edge of trench 3 shows almost no variation through focus, whereas the left edge has the largest variation in SWA at all. For the two smaller trenches the sidewall changes through focus but in a similar way, for left and right edge.

To study the pattern transfer we use Coventor™ software to simulate the etch procedure. The following procedure was followed:

Table 1. Magnitude of relative shifts (nm range) after litho and after etch.

	After litho: experiment	After etch: experiment	After etch: straight	After etch visibility
T1-T2	0.7	2.8	2.5	3
T1-T3	0.2	1.4	0.8	2.6
T2-T3	0.6	1.3	2	0.7



patterns	Criteria		AVG	Bias	3S	3S iW	3S iF
T1	CD	ETCH	31.4	-26.1	5.02	3.94	3.1
		LITHO	57.5	0.0	5.02	3.70	3.4
T2		ETCH	30.9	-26.3	4.08	3.64	1.8
		LITHO	57.3	0.0	4.32	3.77	2.1
T3		ETCH	145.5	-30.6	6.06	5.85	1.6
		LITHO	176.1	0.0	2.94	2.59	1.4

Figure 14. Relative CD distributions and Bias to LITHO (for Etch data) within the Hotspot and CD breakdown.

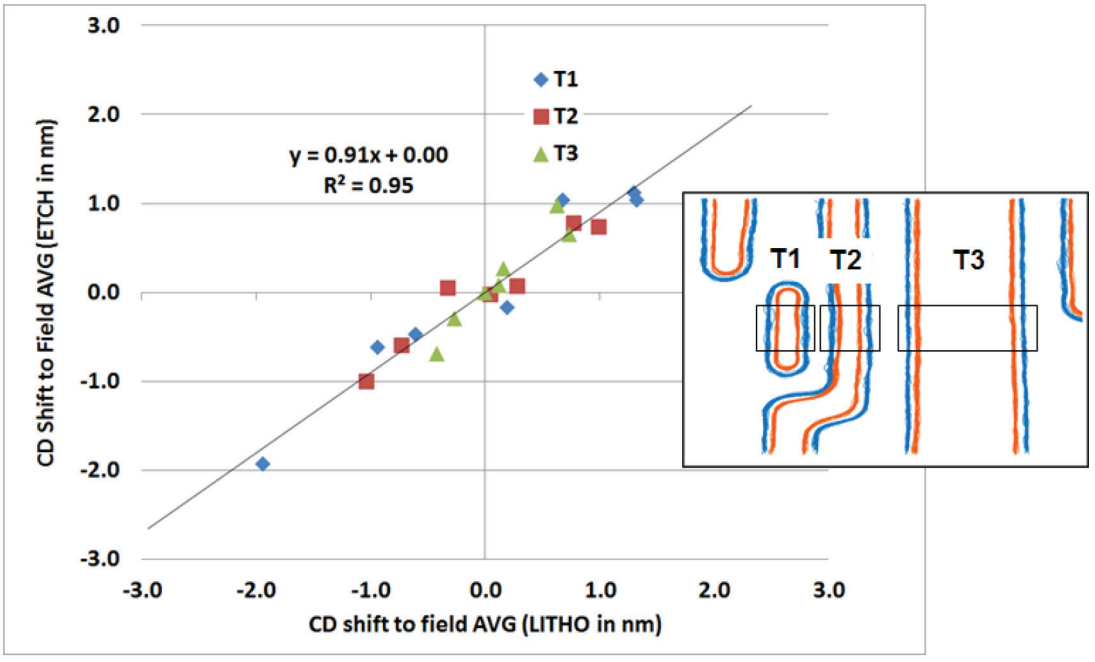
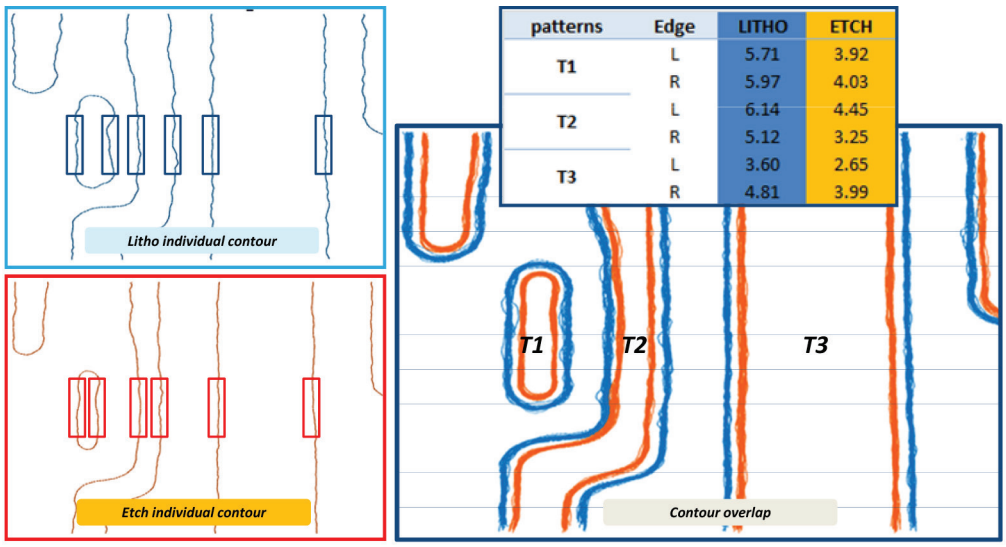


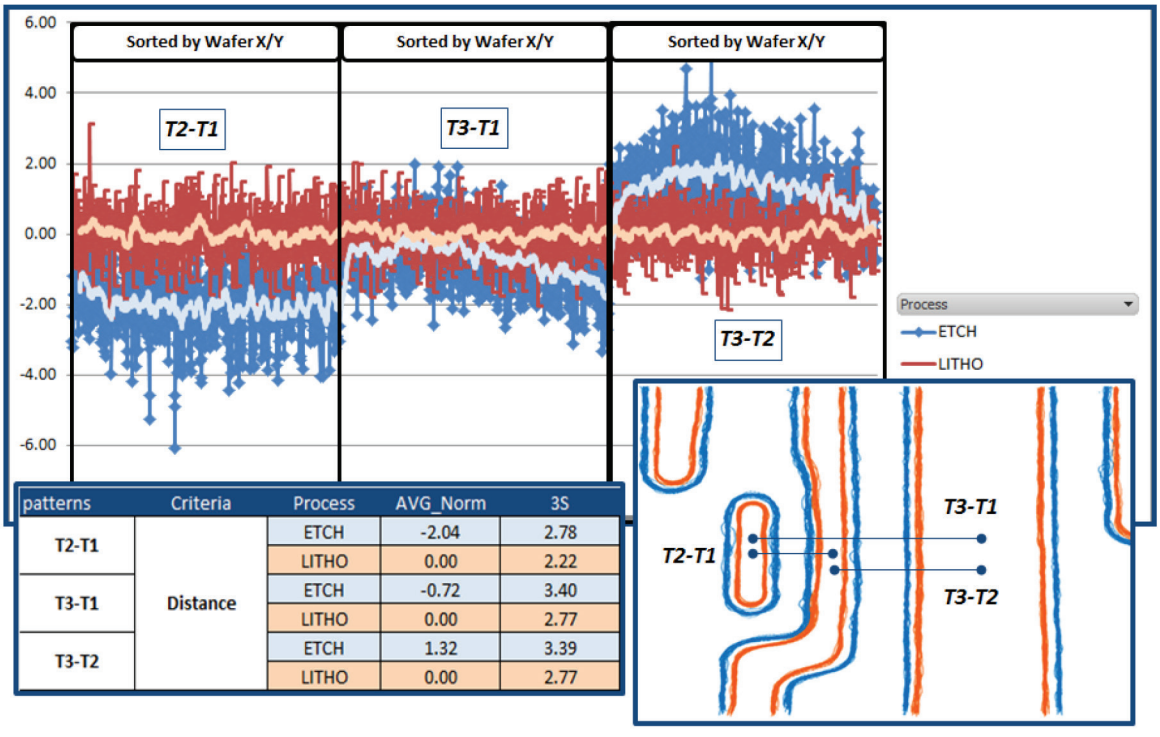
Figure 15. Intafield CD fingerprint correlation between lithography and etching process for trenches CD's within this hotspot.

- For a given focus level the resist profile (as illustrated in Figure 11) is created by Hyperlith™ lithography simulation package.
- The developed resist profile is than imported into the Coventor™ software.
- The stack used for the pattern transfer consists of 90nm resist on top of a thin TiN layer.
- The etch process is mimicked in the simulation and different etch parameters are exploited. So far we probed both a "straight etch" and a "visibility etch". In the "straight" etch all the charged particles propagate perpendicular to the stack surface. In the visibility etch there is an angular spread of the



patterns	Edge	LITHO	ETCH
T1	L	5.71	3.92
	R	5.97	4.03
T2	L	6.14	4.45
	R	5.12	3.25
T3	L	3.60	2.65
	R	4.81	3.99

Figure 16. Within Hotspot Line Edge roughness extraction, compared between lithography and etch.



patterns	Criteria	Process	AVG_Norm	3S
T2-T1	Distance	ETCH	-2.04	2.78
		LITHO	0.00	2.22
T3-T1		ETCH	-0.72	3.40
		LITHO	0.00	2.77
T3-T2		ETCH	1.32	3.39
		LITHO	0.00	2.77

Figure 17. Within Hotspot trench relative position after lithography (reference set to 0) and after Etch.

charged particles.

- Metrology of placement is performed at the foot of the etched TiN layer and position of the individual edges and trench position and CD can be derived.

Figure 12 shows the simulated results for the relative trench displacement when applying a straight etch. The correlation with the experimentally obtained data (see Figure 10) is rather poor, both in magnitude and through focus behavior.

For comparison, the results of the displacement of the three trenches when applying a visibility etch is shown in Figure 13. When changing the etch properties the relative displacements changes significantly per feature. Table 1 summarizes this intermediate result of observed relative pattern shift. Further work is ongoing to optimize etch parameters to better describe the experimental curves.

Golden Hotspot Variability Analysis

As mentioned in the first chapter of this paper, performing off-line metrology on CDSEM contour allows process engineers to have access to some aspects of process variability that are not easy to collect. In this paper we have setup a set of metrology enabling the measurement on wafers at best conditions (post Lithography

and Etch) of individual CD's, relative positioning of the 3 main components of the Hotspot as well as LER based on extracted contour of about 700 images per wafers.

Results obtains are promising in term of variability observation at the scale of a complex feature which has a very different shape compared to the in-line process control feature (1D).

Figure 14 shows a first rather simple observation. CD uniformities of the smallest features (T1 & T2) are smaller than T3 after lithography but post etching the trend is different with an observable intra wafer fingerprint for T3 etch bias (U shape in CD profile). Etch bias of T3 is clearly different. Second observable point is the tiny modulation that can be seen which is correlated to an intra field fingerprint which can be largely related to a known mask contribution. Indeed across a wafer several similar hotspots are measured within one field.

Considering the intra field fingerprint it is often asked whether the fingerprint remains constant between Lithography and Etch process. Figure 15 shows the observed correlation of the intra field fingerprint post lithography and etching (note that the bias difference has been removed from T3 to only highlight intra field fingerprint). From the correlation plot it can be concluded that the intra field signatures are purely Lithography driven for this test case.

Line Edge roughness can also be monitored revealing in number what is observable on overlapped contours. LER observations are very interesting because they can also be linked to resist side wall angle changes where image quality gets degraded. As such we see much higher LER for T1 and T2 compared to T3. It is also very interesting to see that post etch process LER values are significantly reduced and get more uniform across features

Finally, an observation more specific for this paper, a measurement of the relative shift distance between T1/T2/T3 can also be analyzed at best conditions.

From these measurements it can clearly be seen that the T2 trench moves toward the T1 trench and away from the T3 trench. T1 versus T3 is also changing. The amplitude of the phenomenon is about 2nm on average with some significant variability across wafer. This effect seems to be correlated with edge roughness. The shift seems to mainly occur between T2 and T1 where 2 edges are facing with a maximum LER. The hypothesis is that LER would be correlated to lower contrast images then higher resist sidewall angle and as a consequence different local edge position etch biases. An unbalancing of edges etch biases would lead to position shifting.

EDITORIAL (CONTINUED FROM PAGE 2)

lithography with e-beam in a more compatible process was quite evidenced during the photonics session. Patterning technologies for non-CMOS application, such as photonics, MEMS, were interesting and may cover IoT world of our future.

And finally, comments from the EMLC 2016 attendees: "Alternative applications should have more attention." "Regarding the new subject: Photonics, one could say the new topic presented was one of the highlight of the conference." "By including MEMs and Photonics, the EMLC reaches out to more European companies and institutes and their fields of interest." "There is an exploding market related to IoT and mobility for EU wafer fabs that the conference can cover in the future." "Data generation and analysis is a big topic today and for sure we need more and more to keep silicon in specs. Also, modelling in many ways is a source of data that is fundamental."

The EMLC2017 will be held on Tuesday, June 27th to Thursday, June 29th 2017 at the Hilton Hotel in Dresden, Germany, together with a Technical Exhibition.

Conclusion

The methodology presented in this paper offers a lot of possibilities to engineers to better use CDSEM images. Once CDSEM image contours are stored in a database many kind of measurements can be performed retrospectively. In this work we focused essentially on:

- Basic variability observations (CD, LER) which can be done using CDSEM the usual way but requires more complex recipes to be set and measurement time and often a lot of measurements fail on complex shapes.
- New possibilities like the one presented regarding pattern placement / shifting between two process steps. Combining this with simulation tools also enables new ways to characterize these mechanisms that are very difficult to capture otherwise.
- The intra field fingerprint as found after development, is largely (for about 90%) transferred to etch, in spite of the SWA differences after litho.
- After etch, due to SWA differences, patterns can shift a few nm leading to edge placement errors that exceeds OV improvements.

In any case contour "off-line" metrology is a key enabler for proper process characterization to feed process assumption calculations or assessments since it very often addresses design rules referring to features that are not the ones that are monitored quantitatively in line.

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Industry Briefs

TSMC to Adopt Extreme Ultraviolet at 5nm

Alan Patterson, *EE Times*

TAIPEI—Taiwan Semiconductor Manufacturing Co. (TSMC), the world's largest foundry, said it will implement extreme ultraviolet (EUV) lithography to make 5nm chips by the end of this decade. "We estimate that EUV will be cost-effective for high-volume manufacturing by 2020, in time for our 5nm ramp," said TSMC Co-CEO Mark Liu. "We plan to use EUV lithography extensively in 5nm to improve density, simplify process complexity and reduce cost."

The company said it has been using 7nm as a development vehicle for EUV, achieving what it called good integration of EUV scanners, masks and photoresist. TSMC said it is running four state-of-the-art EUV scanners for infrastructure development and will move in another two NXE:3400 EUV production tools from ASML in the first quarter of 2017. TSMC said it has implemented a 125 watt EUV source in its ASML NXE:3350 equipment to improve productivity. In the meantime, the company has also developed in-house EUV mask, material, inspection and repair to integrate its EUV lithography.

Global economics limiting semiconductor business growth

Ed Korczynski, *Solid State Technology*

The near-term outlook for semiconductor manufacturing is challenging, with revenues down slightly but equipment spending up a bit, as reported by experts during the SEMI/Gartner Market Symposium held yesterday afternoon. The global economy is facing extreme uncertainty and is still recovering from the 2008/2009 financial crisis. Duncan Meldrum, Chief Economist with Hilltop Economics, explained why the after-shocks of the 2008/2009 global financial crisis combined with current political uncertainties result in a difficult investment environment. Compared to the 1993-2007 era when world real GDP was +3.2%, there are many indicators that the current ~2.3% GDP growth is the 'new normal.' "Rolling recessions in different regions have been pulling down global growth," explained Meldrum. "Before the financial crisis, all the growth rates tended to be together in a coordinated global market. We're seeing potential growth cut in half. That will create a new speed limit on the global economy, so it'll be a tougher world than we're used to."There's a high correlation between these numbers and semiconductor industry silicon wafer processing in Millions of Square Inches (MSI).

NAND Flash is the long-term bright spot in the industry, with growth driven by solid-state drives (SSD). However short-term oversupply in the second-half of 2016 is expected due to weak end markets, and increased output of planar 3bit/cell products. 3D-NAND represents 19% of the PetaBytes (PB) of total demand in 2016, increasing to 70% by 2020. SSDs are not just for PCs and mobile devices, but are moving into the enterprise segment and data centers, and 84% of SSDs will use 3D-NAND by 2020.

IC innovation at heart of decade of disruption

Pete Singer, *Solid State Technology*

imec – the Leuven Belgium-based research consortium – hosted its annual Technology Forum (ITF) USA, a half-day conference at the Marriott Marquis. With the theme 'Towards the Ultimate System', imec's speakers and industrial keynote speakers looked at the co-optimization of design and new technology, and how technology innovation can deliver the right building blocks to build these systems. Delivering the keynote address at the event was Luc Van den hove, President and CEO of imec. He talked about how the world was in the middle of a decade of digital disruption brought about by integrated circuit innovation. He then provided an outlook of how the industry could continue to stay on the path defined by Moore's Law by moving to nanowires and the 3rd dimension.

Van den hove noted what he said were obvious example of disruption today: Uber, the world's largest taxi company that doesn't own any taxis. Airbnb, the world's largest accommodation provider that doesn't own any real estate. Facebook, the world's largest media provider, that doesn't generate any media content."These are just a few examples, but we will see this kind of disruption everywhere, in every market and every segment," he said. "Companies will have to adapt. They will have to reposition themselves in the value chain and come up with new business models. This is just the beginning."

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Calendar

2016

SPIE Photomask Technology
12-14 September 2016
San Jose Convention Center
San Jose, California, USA
www.spie.org/pm

2017

SPIE Advanced Lithography
26 February-2 March 2017
San Jose Marriott and
San Jose Convention Center
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