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EUV mask observations using a coherent EUV scatterometry microscope with a high-harmonic-generation source

Takahiro Fujino, Yusuke Tanaka, Tetsuo Harada, Takeo Watanabe, and Hiroo Kinoshita, Center for EUV Lithography, Laboratory of Advanced Science and Technology for Industry, University of Hyogo, Kamigori, Hyogo 678-1205, Japan

Yutaka Nagata, Center for EUV Lithography, Laboratory of Advanced Science and Technology for Industry, University of Hyogo, Kamigori, Hyogo 678-1205, Japan; Laser Technology Laboratory, RIKEN, Wako, Saitama 351-0198, Japan

ABSTRACT

In extreme ultraviolet (EUV) lithography, the three-dimensional (3D) structure of the EUV mask, which has an absorber layer and a Mo/Si multilayer on a glass substrate, strongly affects the EUV phase. EUV actinic metrology is required to evaluate the feature of defect printability and the critical dimension (CD) value. The 3D structure modulates the EUV phase, causing the pattern position and focus shift. A microscope that observes in phase contrast necessary. We have developed a coherent EUV scatterometry microscope (CSM) for observing EUV patterns with quantitative phase contrast. The exposure light is coherent EUV light. For the industrial use, we have developed a laboratory coherent source of high-harmonic-generation (HHG) EUV light. High harmonics is pumped by a scale of a Ti:Sapphire laser. In the previous study, a very long exposure time of 1000s was necessary to detect We upgraded the relay optics. The detection performance of an absorber defect using the new relay optics is We observed the line-end oversize defect and the oversize defect in the 112 nm hole pattern and 180 nm hole pattern The upgraded system has a detection size limit of a line-end 24-nm-oversize defect with 100s exposure time, which is 2,688 nm^2 (52 Å~ 52 nm^2) absorber defect. This result shows high performance capability of HHG-CSM for detecting small defect.

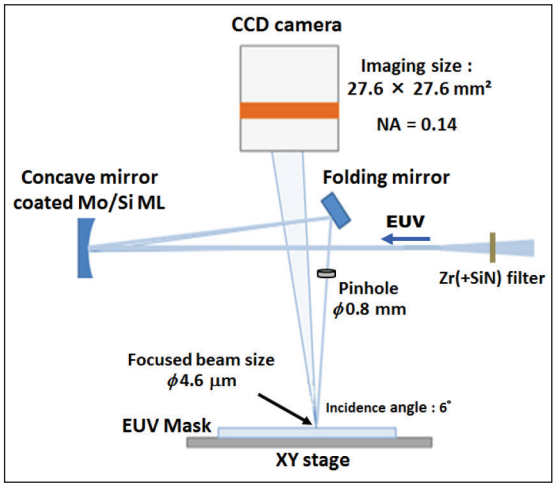

Figure 1. Schematic layout of the CSM system.

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EDITORIAL

At the X-Roads?

Artur Balasinski, Cypress Semiconductor

We are approaching another critical junction in IC manufacturing. This time, the question is, do we want to do it, not whether we can do it. The "X" in the "X-roads" in the title would on the one hand come from the "X-treme" EUVL, which, according to the opening talk of European Litho- and Mask Conference (EMLC 2015), is now a matter of "when" not "if." However, while the long-delayed EUVL was able to grow the source power from 10W to 80 W (vs the needed 250 W), achieve a not-bad 50% uptime (vs. the desired 99%), and the throughput increased from 10 to 1000 wafers/day, it did not become any less expensive nor complicated than before. Only now, it may not require continuous life support. On the other hand, the "X" in the "X-roads" would be due to the uncertainty about the Moore's push. Do we want to keep shrinking or not? Intel's delay of the 10 nm product node is widely commented as a sign of stagnation. It is unclear how the next "killer app" in the customer markets, supposed to be the Internet of Things (IoT), would need the lithography at high cost and advancement level. Looking at the recent edition of EMLC, one can clearly see that the research is ongoing. The big IC makers like to keep the EUVL as their option such that no one would beat them to it, once the time is right. The EMLC participation was more from the research-oriented Europe than from the profit oriented USA or the manufacturing oriented Asia. One may wonder, if at this stage the big players should show off more interest, to keep their competitive edge and not let any startup up-start like Tesla (from another industry) try to steal the show. Well, they do not seem to be too concerned, yet.

Sometimes, I am tempted to substitute the names. How about "NXE" for "A380" and "Intel" for "Emirates"? Europe is trying to develop things many people love. Name, the Cognac, the Concorde, the Opera. America is not paying much attention, they need to make money, based on what they invent and what Asia makes. And in Asia, they do like the luxury, but volume production rules. Based on this parallel, we have to brace for how the A380 (oops, excuse me, the NXE) would be used. There may be an initial volume of orders (maybe from Intel, or, say, Emirates) because they have the money. But the money-conscious folks would disregard the message and focus on cost reduction (a new way of cramming seats in economy class).

Where do we go from here? As opposed to the "dramatic" title, the progress would probably be gradual, and in all directions. The X-roads do not matter anymore. The progress would involve careful sifting through the options in the next few years. Cost reduction would continue, which is not promotive to introducing new equipment at high cost level. One has to keep an eye on Fab closures and mergers. 72 plants went out of business in the past 5 years, but on the other hand, design tools are being developed to create products to fill the remaining ones at 80% capacity. People would not stop flying nor using the IC's. But it is going to be less neck-breaking except for the new materials and concepts.

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Managing Editor/Graphics Linda DeLano
Advertising Lara Miles
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P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 360 676 3290
Fax: +1 360 647 1445
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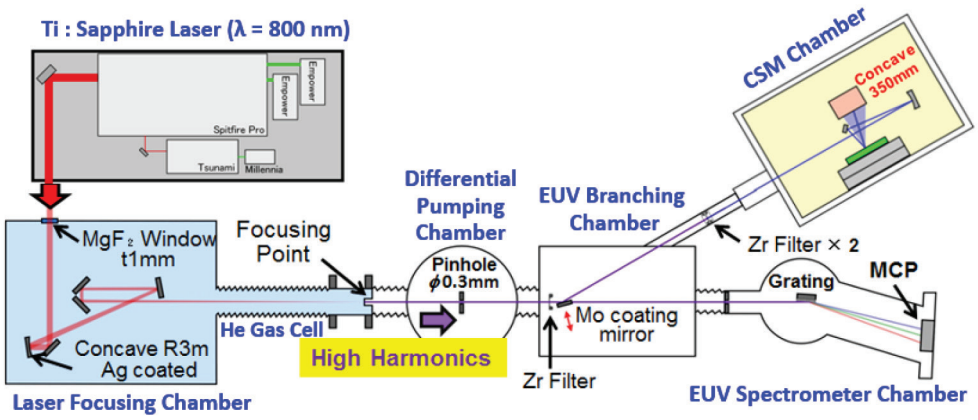

Figure 2. Optical relay system from the HHG EUV source to the EUV mask.

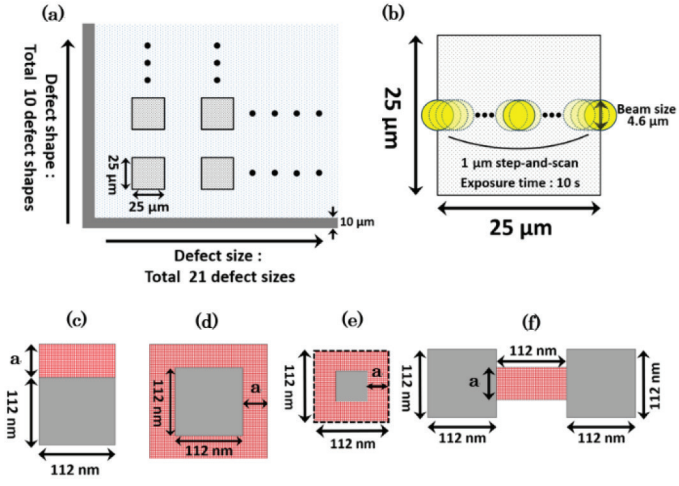

Figure 3. (a) Schematic design of the hole pattern. (b) Measurement procedure of line step-and-scan measurement of the hole pattern region. Defect designs of (c) line-end oversize defect, (d) oversize defect, (e) undersize defect, and (f) bridge defect. "a" corresponds to defect size.

1. Introduction

Extreme ultraviolet (EUV) lithography is an extendable and cost-effective lithography technology. Defects on an EUV mask must be mitigated for high-volume manufacturing.[1-3] In EUV lithography, the EUV mask is a reflection mask composed of a Mo/Si multilayer (280 nm thick), an absorber layer (50–70 nm thick), and a glass substrate (6.35 mm thick). Because the thickness of these layers are larger than the EUV wavelength (13.5 nm), the pattern has a three-dimensional (3D) structure for EUV. EUV actinic metrology[4-7] is required to evaluate the actinic feature of defect printability and the critical dimension (CD). In addition, an EUV image depends on the incidence angle to the mask because an absorber causes shadows and reflections of EUV at the 3D sidewall structure. Moreover, the 3D structure strongly modulates the EUV phase, causing the pattern position and focus shift. Hence, a microscope for observing in phase contrast is necessary. We have developed a coherent EUV scatterometry microscope (CSM) for observing EUV patterns with a quantitative phase contrast. [8-15] The exposure light should be highly coherent. A synchrotron radiation EUV light was used as the coherent source for this CSM work. For industrial use, we have developed a laboratory coherent source of high-harmonic-generation (HHG)[12-16] EUV light. High harmonics[17-19] is pumped by a laboratory-scale femtosecond laser. In our previous paper[24], a very long exposure time of 1000s was necessary to detect defects. We installed a feedback system for the beam position and upgraded relay optics.[25]) The throughput of the new relay optics was improved 130-fold compared with that of the previous optics. In this paper, the detection performance of absorber defects using the new relay optics was evaluated.

2. Experimental Procedure

2.1. CSM system

Figure 1 schematically depicts our CSM based on coherent diffraction imaging, which is a simple system without an objective. The CSM was composed of a concave mirror for focusing on the EUV mask, a folding mirror, an EUV mask, and a CCD camera (Roper Scientific MTE-2048B) with a 27.6 Å~ 27.6 mm^2 image

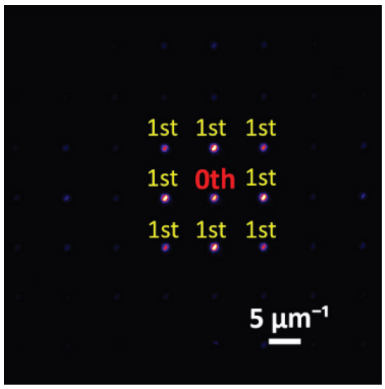

Figure 4. Diffraction image recorded with a CCD camera.

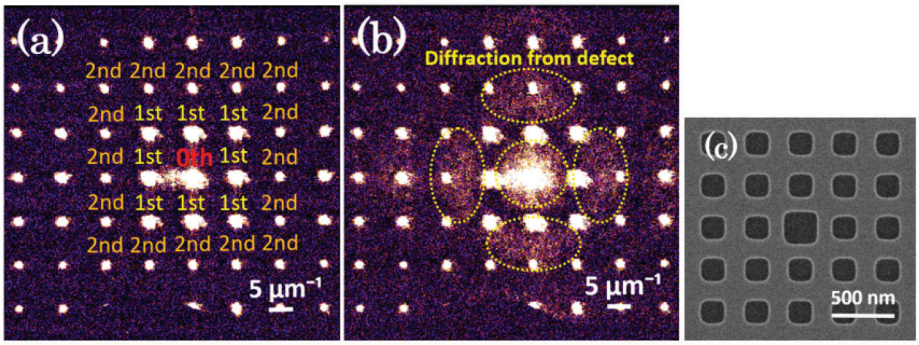

Figure 5. Diffraction images of a 180 nm hole pattern with an optimized contrast for the (a) no defect region and (b) 40-nm-oversize defect. The exposure time is 1 s. (c) SEM image around the defect.

size. The mirrors were coated with a Mo/Si multilayer, which has a bandwidth of about 0.4 nm at a wavelength of around 13.5 nm. This configuration is suitable for the selective reflection of the 59th harmonics. The concave mirror distance was controlled by an actuator (Thorlab Z812V), which optimizes the focus of the mirror. The incidence angle to the mask was 6°, which is same as the EUV exposure tool for high-volume manufacturing. The EUV mask was exposed with a coherent EUV light. A CCD camera directly recorded the diffraction from the EUV mask, which contains amplitude information in the frequency space. The mask was about 95 mm away from the CCD camera. The numerical aperture (NA) of the CCD camera was about 0.14. A 0.8-mm-diameter pinhole was installed between the folding mirror and the EUV mask to reduce the scattering from the optical element. The scattering was recorded as a stray signal. In our previous works with a synchrotron radiation EUV source, the CD was evaluated using the diffraction intensity from the periodic pattern,[8] and aerial-images were reconstructed by an iterative calculation based on coherent diffraction imaging.[11, 13, 14]

2.2. CSM with a HHG source

Figure 2 schematically depicts the HHG-CSM,[12] which is composed of seven parts: (1) a Ti:sapphire fs laser, (2) a focusing chamber, (3) a gas cell, (4) a differential pumping chamber, (5) an EUV branching chamber, (6) a spectrometer chamber, and (7) a CSM chamber. The Ti:Sapphire laser was focused in the gas cell by an Ag-coated concave mirror (R=3 m) in the focusing chamber. The focusing chamber and gas cell were filled with helium gas. A thin MgF_2 crystal (1 mm thick) was used as the vacuum window at the entrance of the focusing chamber to prevent the phase dispersion of the laser. The focused laser pumped the HHG output with a nonlinear interaction of the helium gas. In the differential pumping chamber, gas leaking from the gas cell was evacuated by a turbo molecular pump at 900 L/s. For this differential system, the branching and focusing chambers were in a high vacuum ($\lesssim 10^{-3}$ Pa). The 59th harmonics of the 13.5 nm wavelength was used, where the pumping laser wavelength is near the infrared wavelength of 800 nm. Then, the HHG EUV light was branched to the CSM chamber and spectrometer chamber. Because the HHG source includes both the EUV light and the pumping laser light, which has a power of 10^6–10^7 times higher than that of the EUV light, we installed a thick pinhole with ϕ0.3 mm[16]) in the differential pumping chamber and three Zr filters (200 nm thick) with a Si-nitride back support (50 nm thick) to filter the pump light. The spectrometer chamber

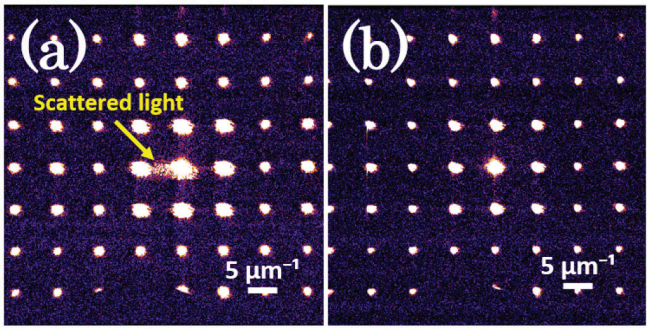

Figure 6. Diffraction images of a 180 nm hole pattern. CSM result of (a) before installation (b) after installation of the pinhole.

was composed of a reflection flat-field grating and a microchannel plate (MCP) assembly coupled to a phosphor screen and a CCD camera. We optimized the HHG generation parameter using this spectrometer to achieve a high EUV power. To branch the EUV light, the new system used a mirror with a Mo layer coating at a grazing incidence of θ15°. The concave mirror in the CSM chamber directly relayed the EUV source image on the mask surface. The curvature radius of the concave mirror in the CSM chamber was about 350 mm. The distance from the EUV source to the focusing mirror and that from the focusing mirror to the mask were 3 m and 175 mm, respectively. The magnification of the relay optics was about 1/17. The beam size on the mask was optimized to ϕ4.6 μm, which is about half the size of the previous system. Because the defect is illuminated with a high EUV power over a small area, the defect sensitivity should be high.

3. Results and Discussion

3.1. Sample EUV mask

We observed the EUV mask with hole patterns using the upgraded HHG-CSM. The pattern design is shown in Fig. 3(a). The hole patterns were fabricated in a square region measuring 25 Å~ 25 μm^2 with a programmed absorber defect in the center. A 10 Å~ 21 region of the hole in a block contained 10 defect shapes and 21 defect sizes. The block was surrounded with an absorber line (10 μm wide). Specifically, we observed two hole blocks (112 and 180nm in diameter). Both have a one-to-one ratio of the hole and

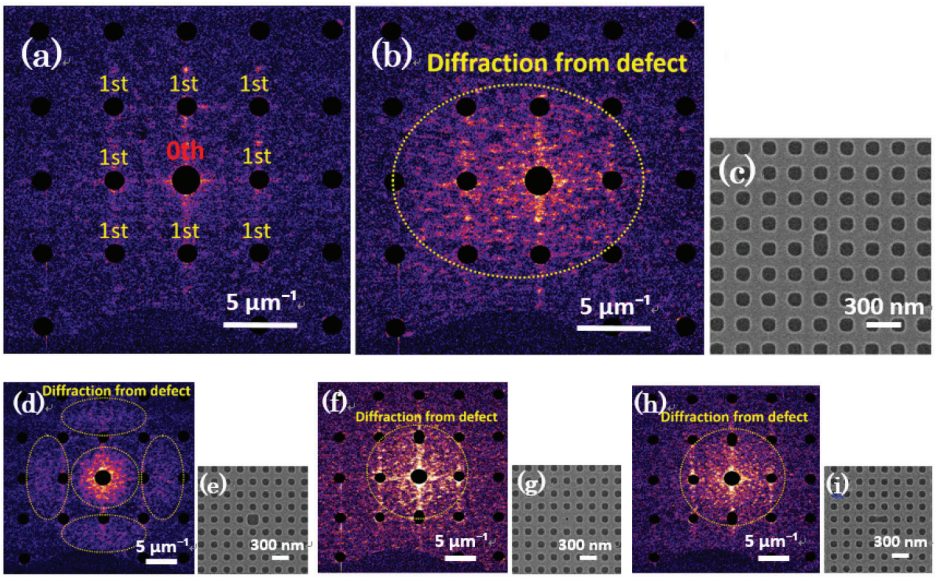

Figure 7. Diffraction image from EUV mask with 112 nm hole pattern and SEM images. CSM result of (a) no defect region, (b) line-end 76-nm-oversize defect, (d) 38-nm-oversize defect, (f) 20-nm-undersize defect, and (h) 80-nm-bridge defect. (c, e, g, i) SEM images of each defect.

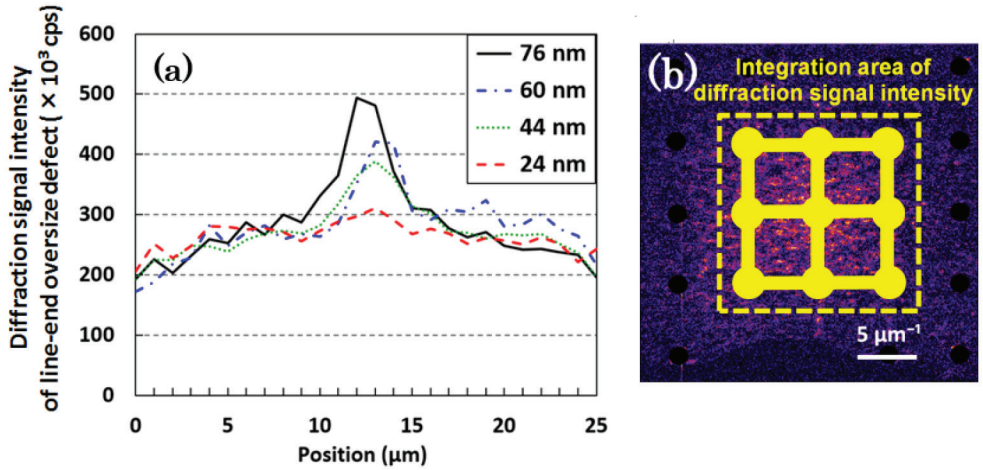

Figure 8. Observation of the line-end oversize defect.

space width. Because the magnification of the exposure tool for EUV lithography is 1/4, the hole diameters correspond to 28 and 45 nm at a wafer plane, respectively. Figures 3(c) – 3(f) show drawings of four absorber-defect shapes. The hatched region indicates an absorber difference from the original hole pattern. The defect size, whose area depends on the hole size and defect shape, is indicated as "a".

3.2. Absorber defects

Figure 4 shows a diffraction image from the 180 nm hole pattern recorded by a CCD camera (NA=0.14) on the full intensity scale. The bright spots indicate diffraction signals from the hole pattern with a 180 nm diameter. The center spot is a 0th-order diffraction, which is a specular reflection from the mask. Around the 0th-order diffraction, there are eight 1st-order diffractions.

Because the diffraction from a defect is weaker than that from hole pattern, Fig. 5 is shown with the optimized contrast. Figures 5(a) and 5(b) show the diffractions without and with a defect, respectively. The defect signal intensity (described in Sect. 3.3) is about 2.5 times higher than that without a defect. Figure 5(b) shows the diffraction with a 40-nm-oversize defect with 1s exposure time. Figure 5(c) shows a defect shape and scanning electron microscopy (SEM) image. The diffraction from the defect clearly spreads around the 0th-order light and between the 1st- and 2nd-order diffractions of the hole pattern. In our previous paper[24], we required an exposure time of 1,000 s to detect the same defect, upgrade system only requires an exposure time of 1s, which is a marked improvement.

Figure 6(a) shows the diffraction image without a defect of a 180-nm hole pattern. The EUV light was scattered with the re-

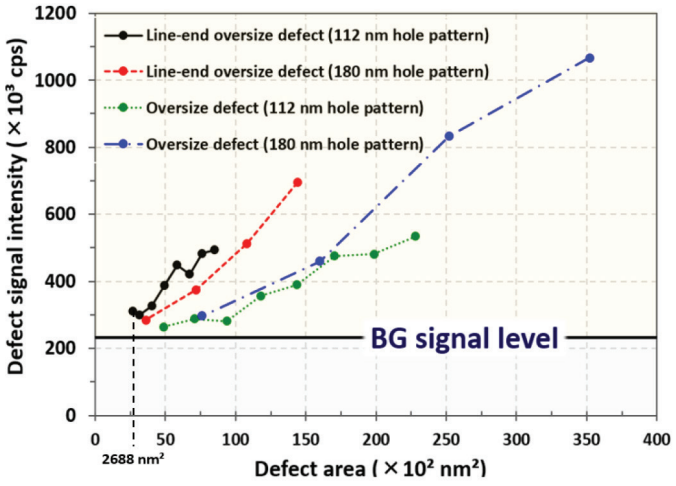

Figure 9. Dependence of the defect signal intensity on the defect area siz e for three types of defects.

flection mirrors (the switching mirror, the concave mirror and the folding mirror). Because the scattered light was not focused on the mask, large area of the mask was exposed. The hole-block shapes were recorded beside the 0-th order diffraction light. We installed the ϕ0.8 mm pinhole between folding mirror and EUV mask for filtering the scattered light, which layout was shown in Fig. 1. After installation of the pinhole, the diffraction image from the 180-nm hole pattern was shown in Fig. 6(b), and no scattered light from the mirrors was recorded.

3.3 Evaluation of the defect-detection sensitivity

Figure 7 shows the diffraction images collected with an exposure time of 10s. Figure 7(a) shows an image without a defect in the 112 nm hole pattern. Figures 7(b), 7(d), 7(f), and 7(h) show the diffraction images for a line-end 76-nm-oversize defect, a 38-nm-oversize defect, 20-nm-undersize defect, and a 80-nm-bridge defect, respectively. Their corresponding SEM images are shown in Fig. 7(c), 7(e), 7(g), and 7(i). Diffractions from the hole patterns are masked with black regions to easily visualize the defect signal. All four defect shapes produce signals where the defect signal distribution corresponds to the defect shape.

We observed these defects with the line step-and-scan method, which is introduced in Fig. 3(b). A defect is observed with a 1 μm step in one direction that is scanned from the edge to the other edge of a hole region (25μm length).

Figure 8(a) shows the diffraction signal distribution via step-and-scan measurements for the line-end oversize defect in the 112 nm hole pattern. The defect sizes are 76, 60, 44, and 24 nm. The horizontal axis shows the exposure position, while the vertical axis shows the diffraction signal intensity recorded by a CCD camera. The diffraction signal intensity is an integrated signal with an integrated area.

Figure 8(b) shows the integration area, which is between the 1st-order light and the 2nd-order light. We set the integration area size to gather the diffraction from the line-end oversize defect efficiently. We set the hole masking areas not to gather the diffraction from the periodic hole pattern. The edge structure of the patterned region generated line diffraction. The linear masking area was set not to gather the diffraction from the edge structure. The 76, 60, and 44nm defect signals, whose intensities depend on the defect size, are detected at the center defect position. The 24 nm defect signal is detected slightly at the center defect position.

Figure 9 shows the relationship between the defect area and the defect signal intensity for two defect shapes in the two size hole pattern. We observed the line-end oversize defect and the oversize defect in the 112 nm hole pattern and 180 nm hole pattern. The horizontal axis indicates the defect area size calculated using the design value. We determined the background signal level using the CCD camera and EUV mask noise. The CCD camera noises are dark current noise and readout noises. EUV mask noises are caused by the roughness of the multilayer and absorber. The defect signal intensities had almost linear relationship with the area size. However, the slope factor depended on the defect shapes. Because the diffraction from an oversize defect had an interference structure similar to a double slit due to its shape, the defect signal intensity in the integrated area was low. As the result, the signals of line-end oversize defects were stronger than that of the oversize defects. Thus, the integrated area should be optimized for its defect signal distribution.

In this study, the detection limit is a line-end 24-nm-oversize defect with 10 s exposure time, which has an area of 2688 nm^2. This area is equivalent to a 52 Å~ 52 nm^2 absorber defect.

4. Conclusions

We developed a CSM with a HHG EUV source. The source is on the laboratory scale and can be applied to industrial use. Our previous system requires an impractical exposure time of 1000s to detect the 40-nm-oversize defect in the 180-nm hole pattern, the upgraded system only requires an exposure time of 1s, which is marked improvement. The upgraded system has a detection size limit of a line-end 24-nm-oversize defect with 10 s exposure time, which is a 2688 nm^2 (52 Å~ 52 nm^2) absorber defect. However, the detection limit strongly depends on the EUV exposure power and illumination size. If we focus the illumination to ϕ1 μm, a 20-fold improvement in defect sensitivity should be achieved. In the near future, we will observe EUV patterns in phase contrast using coherent-diffraction-imaging method with the practical coherent EUV source of the HHG.

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5. Acknowledgement

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Industry Briefs

EUV: Unlike Anything Else in the Fab

By **Pete Singer,** Editor-in-Chief, Solid State Technology

Imagine EUV lithography in high volume production. ASML, working for years to make it happen, has now an order for 15 EUV systems. Because the ASML NXE is vacuum based (with all-reflective 4x reduction optics from Carl Zeiss SMT, a numerical aperture of 0.33, and a maximum exposure field of 26mm by 33mm), it is very different from any other tool in a fab. A main difference is that the system is designed to operate in a continuous mode. The steps such as process, vent, load, unload wafers, and cleaning, have to support it. Knowing the cost, it's also important that the tool is always up.

The vacuum condition in the EUV source is known to be different than the condition in the scanner. The challenge for the vacuum and abatement system is to handle the different conditions in an acceptable footprint in the sub-fab. Hydrogen is used to mitigate the contamination of the mirrors. Pumping hydrogen is a challenge in itself, because H2 is a small molecule. The pumping mechanism needs to accommodate hydrogen, but also other gases. Another main task to enable EUV lithography for volume production is to improve its total energy use.

Intel Hits Snag On The Way To Next-Generation Chips

By **Rachel Courtland,** IEEE Spectrum, 16 Jul 2015

Depending on what stories you've been reading during the last week or so, you'd either think Moore's Law is in very deep trouble or has been rescued yet again from imminent demise. IBM made a splash with news of a 7-nanometer chip, which employs silicon-germanium instead of silicon. Although not yet ready for production, the chip signaled we're still on track to make smaller transistors. Then Intel announced a sticking point with the manufacture of 10-nm chips. The first 10-nm product will now be released in the second half of 2017, a delay of at least six months.

One way of interpreting the above is to conclude that IBM is gaining ground on Intel. But IBM has said little about when 7-nm chips would debut. Another possible interpretation: Moore's Law is faltering. Intel, which has long set the pace, hitting a new node every two years, is now releasing chips with smaller transistors every two and a half years, due to the limited ability to print finer features.

Moore's Law won't grind to a halt overnight. The cadence of Moore's Law has changed before. And if it's happening again, we may see other developments to explore what's possible beyond simple miniaturization. The semiconductor industry has had the good fortune of being able to guide itself by a simple principle for 50 years. Now it seems the way forward is starting to get just a bit more complicated.

Intel's Tweaking Moore's Law, Like Moore's Law Still Matters

By **Stacey Higginbotham,** Fortune, July 17, 2015

Intel CEO Brian Krzanich said that the exponential advances in semiconductor manufacturing that enable faster and cheaper computing and storage every two years are now going to come closer to a rate of every two and half years. If Intel's CEO had said it a decade ago, it would have shocked the tech world. But today, adjusting the formula for what is known as Moore's Law, was an announcement for Intel shareholders and customers, not for the tech industry overall. That's because Moore's Law is less relevant. The need to put more transistors on a chip is still important, which is why everyone was super excited about IBM's announcement that it had made a super-dense 7-nanometer chip. However, it mattered when all you wanted was faster chips that were good at one style of computing. We don't live in that world anymore.

Intel's style of computing is good at corporate jobs on desktops, servers and things that require linear progression, like spreadsheets and word processors. But it's not great for an increasing swath of computing jobs, such as transcoding graphics, networking, climate or seismic simulations which require parallel computing much better handled by graphics processing units (or GPUs) offered by AMD or Nvidia. This isn't a new trend. The GPU folks were calling the end of Moore's Law in 2010. Concerns about power consumption in the data center also helped drive the adoption of GPUs into other types of semiconductors, from novel architectures that never quite caught on, to Intel's own research into chips.

And as mobility became a top concern, Moore's Law took another blow. Storage inside phones still relies on Moore's Law, so the cost of the memory cards and upgrades matters. But when it comes to the brains for the handset, power consumption is the priority. This means the emphasis is on assigning the right task for the right chip, which is why graphics processors and specialized sensor processors inside the iPhone are being popped into handsets. The emphasis isn't on a massive, super-dense semiconductor marching down the process nodes. And as we progress into real-time data processing and artificial intelligence, researchers are looking beyond Intel architectures as well. Google is trying out quantum computing and IBM, HP, the U.S. military and others are spending on processors that mirror the human brain. Others are trying to make computers that are right only some of the time (instead of all of the time) in an effort to cut down on power usage.

So, when Krzanich said of Intel's efforts to follow Moore's Law, analysts paid attention because they want to understand when Intel gets to reap the benefits of its next-generation chip. But the rest of the computing world glanced back, nodded and kept their eyes on the real prize—taking us beyond the limits of Moore's architecture.

Given the flurry of merger and acquisition activity in the semiconductor industry, the skyrocketing cost of new wafer fabs and manufacturing equipment, and as more IC companies transition to a fab-lite or fabless business model, IC Insights expects the number of fab closures to accelerate in the coming years—a prediction that will likely please foundry suppliers but make semiconductor equipment and material suppliers a little bit nervous.

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Calendar

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SPIE.
International Headquarters
P.O. Box 10, Bellingham, WA 98227-0010 USA
Tel: +1 360 676 3290
Fax: +1 360 647 1445
help@spie.org • www.SPIE.org

Shipping Address
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