PHOTOMASK

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Viability of pattern shift for defect-free EUV photomasks at the 7 nm node

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ABSTRACT

Several challenges hinder EUV photomask fabrication and its readiness for high volume manufacturing (HVM). The lack in availability of pristine defect-free blanks as well as the absence of a robust mask repair technique mandates defect mitigation through pattern shift for the production of defect-free photomasks. By using known defect locations on a blank, the mask design can be intentionally shifted to avoid patterning directly over a defect. The work presented here provides a comprehensive look at pattern shift implementation to intersect EUV HVM for the 7 nm technology node. An empirical error budget to compensate for various measurement errors, based on the latest HVM inspection and write tool capabilities, is first established and then verified post-patterning. The validated error budget is applied to 20 representative EUV blanks and pattern shift is performed using OPC'd 7 nm node fully functional chip designs that were also recently used to fabricate working 7 nm node devices. Probability of defect-free masks are explored for various 7 nm mask levels, including metal, contact, and gate cut layers. From these results, an assessment is made on the current viability of defect-free EUV masks for the 7 nm node.

1. Introduction

As extreme ultraviolet (EUV) lithography[1–4] continues to move towards high-volume manufacturing (HVM), photomask blank defectivity has remained a persistent obstacle.[5] Recent efforts have limited total blank defects to >54 nm in size,[6] however much experimental work have shown that smaller defects also requires elimination.[7–13] The lack in high-volume availability of pristine defect-free blanks as well as the absence of a robust mask repair technique[14,15] mandates defect mitigation through pattern shift for intersecting HVM. By using known defect locations on a blank, the mask design can be intentionally shifted to avoid patterning a desired reflective region directly over a defect.[16]

Past work have simulated the probability of perfect defect avoidance at the 65 and 45 nm node[17], as well as using 45 and 32 nm node mask layouts shrunk to 11 – 22 nm node dimensions.[16,18] However, variability and inaccuracies in the inspection and write tools were largely based on estimates

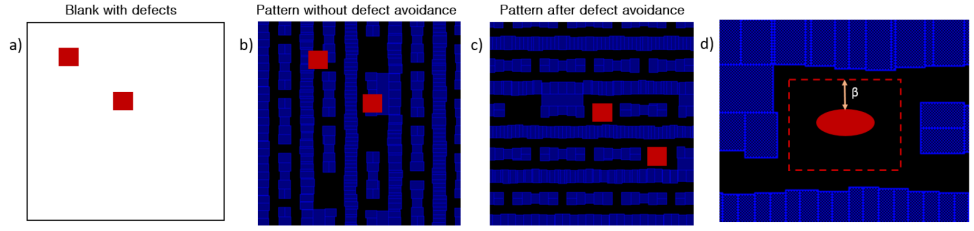

Figure 1. a) Schematic of blank (black box) with identified defects of various sizes (red circles). b) Transparent blue polygon represents intended design, overlapping with known defect locations. c) After implementing defect avoidance, pattern is shifted with respect to the defects such that there is no overlap. d) The ***error budget,*** *β, provides a buffer zone between the defect and pattern such that all errors are accounted for, and defect avoidance is guaranteed.*

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EDITORIAL

Seeing is believing: Metrology and the struggle to keep pace with lithography

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Keeping pace with Moore's law is a constant (and lifetime) challenge, and multiple patterning techniques, including spacer patterning and a combination of litho/etch processes has taken us to the point where it is possible to buy 14 nm node logic devices, 15-16 nm half pitch NAND Flash memory and 20nm class DRAM. However, these supplementary processes add cost to a device, and as a result, alternative solutions such as Extreme Ultraviolet Lithography (EUVL), Nanoimprint Lithography (NIL) and complementary directed self-assembly (DSA) processes are being pursued by both the lithographic tool suppliers and the end users.

In addition, we are also facing a transition in the device fabrication process, spurred by physical constraints as the smallest dimensions push towards 10 nm. NAND Flash memory is in a transition phase, moving from two dimensional to three dimensional architectures, and chip stacking in the memory space is becoming more and more common.

Whenever a lithographic transition occurs in our industry, the first thing typically addressed are resolution experiments, followed by demonstrations of layer to layer overlay and then throughput. The tough work then begins on device integration until a process can be defined that meets cost of ownership requirements. Through the process, we constantly check both process controls and defect levels until we finally reach a point where yields are sufficient to introduce the new lithography tools into the production lines. These checkpoints include metrology methods such as optical pattern inspection for larger areas and scanning electron microscopy for smaller fields.

Our transition away from the more conventional approach of incremental shrinks in exposure wavelength creates gaps in our ability to understand what it is we have created and threatens to slow the entry points of newer technologies.

On the mask side, both EUVL and NIL have significant inspection challenges. An EUV mask must be inspected before and after patterning, and actinic solutions are required in order to correctly account for all possible defects. Tools are now being qualified to address mask blanks and to qualify the optical performance of an EUV mask under scanner equivalent illumination conditions. What is missing, however, is an actinic inspection of the final patterned mask.

For NIL, inspection solutions are required for both master and replica masks. Because these are 1X masks, inspection resolution becomes a significant challenge. The most advanced optical mask inspection tools are capable of detecting breaks or bridges in dense line patterns at 20nm. However, it is likely, that more subtle defects remain undetected and may appear during the pattern transfer process on a replica mask or on the wafer. E-beam inspection provides the needed resolution, but inspection time is prohibitive for the master mask and unrealistic for the replica mask.

On the wafer side, DSA has the promise of providing pitch reduction at a reduced cost and defining smaller contacts then is possible just with conventional lithographic approaches. While significant progress has been made in the understanding of the associated defect mechanisms, we are not yet at the point where the metrology available can satisfactorily observe the DSA process during all phases of fabrication.

Finally, 3D devices provide unique challenges in inspection. 3D NAND Flash, for example, currently defines a 48 layer stack of polysilicon and oxide films, with plans to eventually ramp to at least 128 levels. Channels are then cut into the stack and filled create working bit strings. These structures can have aspect ratios greater than 50:1, and a complete understanding of the etch profile and filling performance are required to qualify device performance and consistency.

As we strive to keep pace with Moore's Law, our lithographic roadmaps must be complemented with plans for inspection solutions that are available at or before the insertion of the new lithography tools. It is certainly possible to exercise new lithography and monitor yield. But as we get closer to meeting device yield targets, the lack of metrology methods will prohibit engineers from doing the root cause analysis that eliminates or minimizes the last few defect modes and thereby realize a true high volume manufacturing solution. Partnerships and collaborations are the key. Without them, we will forever be faced with rising manufacturing costs caused by an inability to provide a total solution package.

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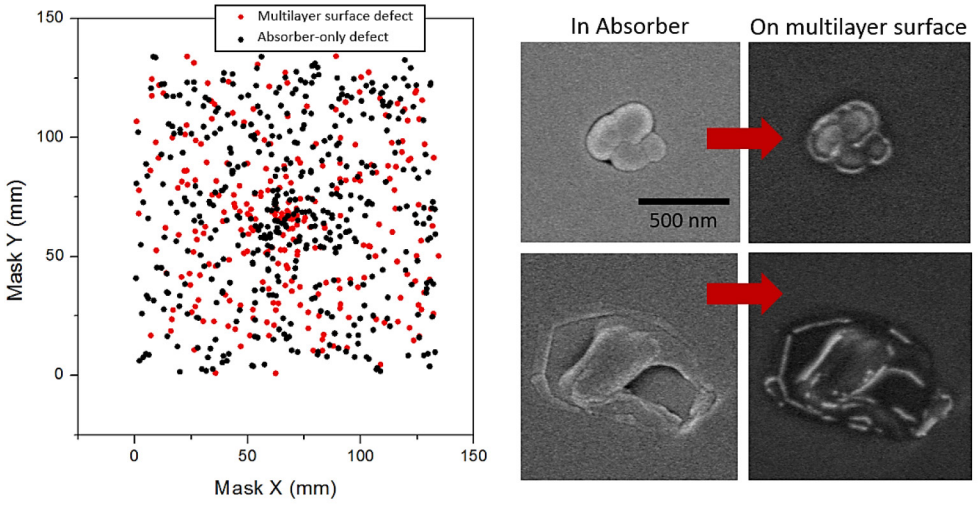

*Figure 2. Defect map of a blank inspection on absorber. Black dots represent **absorber-only defects**, while red dots represent **multilayer surface defects**. SEM images represent a small set of **multilayer surface defects**, showing the defect is present even after the absorber is entirely removed.*

or ideal conditions and not all simulations took into account optical proximity corrected (OPC'd) masks. To address the intersection of EUV for HVM at the 7 nm node (N7), the work presented here establishes an empirical 3-sigma error budget, β, based on the latest inspection and write tool capabilities. Error budgeting and successful pattern shift implementation is experimentally validated post-patterning via scanning electron microscopy (SEM). To access the viability of defect-free masks for N7, the error budget is applied to 20 representative EUV blanks and used for pattern shift simulations on OPC'd N7 full-chip designs that were also used to fabricate working N7 silicon-germanium FinFET chips.[19] From these results, an assessment is made on the current viability of defect-free EUV masks for N7.

2. Experimental Approach

The foundational piece of successful pattern shift implementation is providing appropriate input parameters that encompass current tool capabilities and contains accurate defect information. For example, past work have noted the discrepancy between tool-reported defect size and physically measured defect size, however compensation strategies were not explored.[20] Various experiments are preformed to quantify the variability and error associated with the latest HVM photomask inspection and write tools.

Section 3 discusses in detail how an empirical 3-sigma error budget, β, is established. The error budget is constructed from multiple sources:

Section 3.1: Blank inspection false positives
Section 3.2: Blank inspection coordinate inaccuracy and variability
Section 3.3: Blank inspection defect sizing error
Section 3.4: Blank inspection defect centrality error
Section 3.5: Write tool image placement error and fiducial mark centrality
Section 3.6: Combined error budget

Section 4 discusses implementation and verification of the empirical error budget and pattern shift.

Section 5 assesses the viability of defect-free masks at N7. Relevant N7 EUV mask layers were used for pattern shift simulations, include metal, contact, and gate cut levels. Defect avoidance results based on 20 representative EUV blanks, with the incorporated error budget, will inform the current likelihood of defect-free masks as a function of mask pattern density. The empirically-derived probability of defect-free masks will help guide future direction and focus for enabling HVM.

Section 6 provides a summary of findings and conclusions.

3. Error Budget

To implement defect avoidance via pattern shift, a precise defect map of the blank is required (Fig. 1a). Using a defect avoidance algorithm, the design pattern can be shifted with respect to the defects in order to hide the identified defects under the absorber (Fig. 1b-c). The shifted and/or rotated pattern is then written on the blank, and defect avoidance can be verified through comparison of SEM with the shifted design pattern.

The ***error budget*** defines a buffer zone between the defect and the pattern such that errors and variability accumulated during inspection/patterning is accounted for. Figure 1d illustrates the ***error budget*** as a variable, β, which creates a region (red dotted line) where the defect could potentially be located due to the accumulated sources of error.

Various errors contribute to the defect tolerance budget and must be accounted for. That is, the combined errors of all steps in defect avoidance must be accumulated for before patterning such that hiding the defect under an absorber is guaranteed. The errors incurred is as follows:

Blank inspection @193 nm:

Section 3.1: Blank inspection false positives

Section 3.2: Blank inspection coordinate inaccuracy and variability

Section 3.3: Blank inspection defect sizing error

Section 3.4: Blank inspection defect centrality error

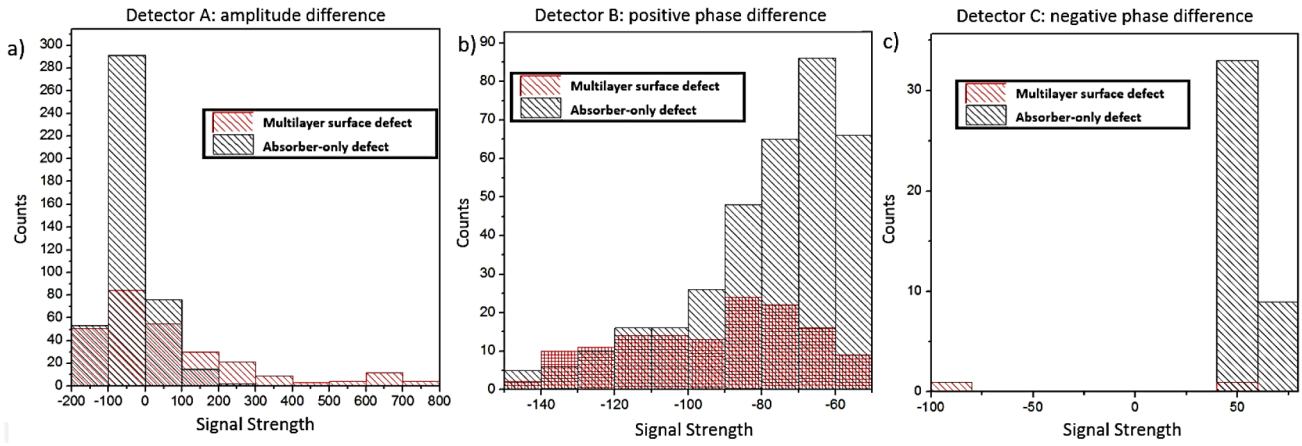

*Figure 3. Histogram of **absorber-only defects** and **multilayer surface defects** as a function of **signal strength** for a)* Detector A*, b)* Detector B*, and c)* Detector C*.*

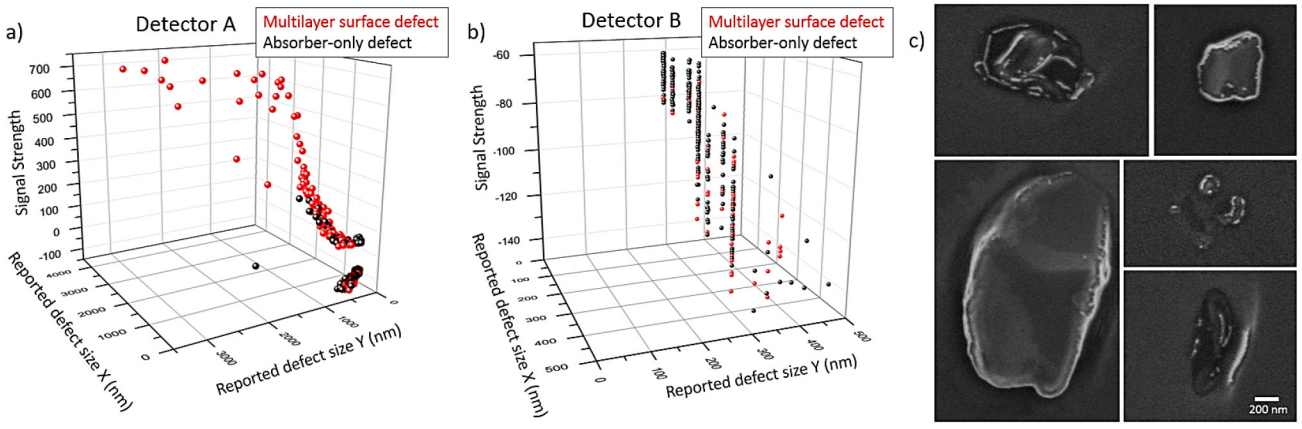

Figure 4. Scatter plot of all available parameters from inspection output for a) Defector A *and b)* Detector B*. Black dots represent **absorber-only defects**, while red dots represent **multilayer surface defects**. c) SEM images of defects with* signal strength *>200 lodged in the multilayer surface.*

Mask write:

Section 3.5: Write tool image placement error and fiducial mark centrality

The choice to use 193 nm blank inspection ensures sensitivity to smaller defects, further differentiating from past work that were largely based on 488 and 266 nm wavelength inspection systems.[6,10,11]

3.1 Blank inspection false positives

EUV blanks were inspected using 193 nm light using three types of detectors. The first defector, *Detector A*, looks for changes in amplitude that arise from scattering/absorption of light, as compared to background. The last two defectors utilize phase contrast microscopy to measure positive phase contrast, *Detector B*, or negative phase contrast, *Detector C*. The inspections were operated at higher sensitives than suggested, in order to safeguard against false negatives.

Hundreds of defects can be identified during blank inspection, however, not all defects warrant avoidance. For example, slight variations in the absorber height could be tagged as a defect due to the phase difference in the reflected light. Therefore, ***absorber-only defects*** that represent slight surface variations or a ***soft defect*** that can be removed during etch, or easily repaired do not represent defects that require avoidance. The assumption is that defects lodged in the multilayer surface (otherwise known as ***multilayer surface defects***) would likely act as an absorber and thus, patterning over them must be avoided. In order to filter out ***absorber-only defects*** from the inspection results, an experiment is devised to understand if there is a unique signature between ***absorber-only defects*** and those defects that are lodged in the multilayer surface.

Blank inspection was performed on a substrate with a 40-pair multilayer stack capped with absorber. The inspection field covered a 134 x 134 mm region. Identified defects were imaged with a scanning electron microscope (SEM). The entire absorber then was selectively etched down to the capping layer that protects the multilayer and all defect locations were imaged again with the SEM. Comparison of SEMs pre- and post-absorber etch provided insight into whether the defect is an ***absorber-only defect*** or a ***multilayer surface defect***.

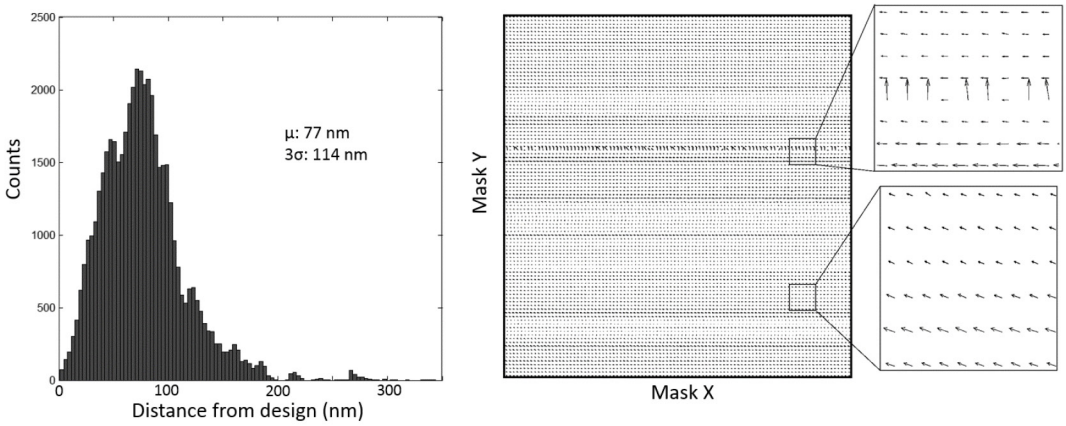

Figure 5. Left) Distribution of difference between reported defect location and design. Right) Vector map across the mask with arrows pointing from design location to reported defect location. Size of arrow indicates the magnitude of the difference in locations.

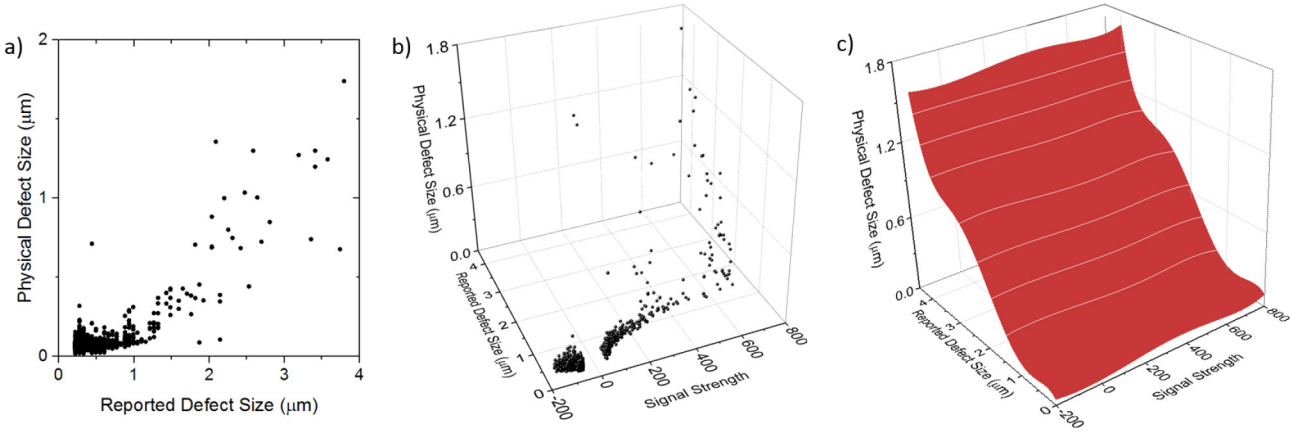

Figure 6. a) Comparison of physical defect size as measured by SEM with reported defect size from the inspection tool. b) Scatter plot of reported defect size *and* signal strength *provided by the inspection tool, and* physical defect size *as measured by SEM. c) 2D polynomial fit of Figure 6b.*

It should be noted that some defects may not show a clear contrast in the electron microscope. It would be rash to call a defect that does not appear in the multilayer SEM image an ***absorber-only defect***, since the defect may have low contrast or suffer from soft focus. This particular issue will be experimentally addressed later in this section using atomic force microscopy (AFM). For the time-being, defects that do not appear in the multilayer SEM are labeled ***absorber-only defects*** and defects that remain on the multilayer surface as verified by SEM are labeled ***multilayer surface defect***.

712 total defects were found during blank inspection on the absorber. Roughly 40% of the defects identified during inspection showed a defect lodged in the multilayer surface after the absorber was removed (Fig. 3, red). The other 60% did not show any defects present in the multilayer (Fig. 2, black). Location dependence is not observed and the two types of defects seem to be randomly distributed. Figure 2 shows the distribution of each defect across mask and also provides representative SEMs of defects that remained after absorber etch.

In order to predict whether a defect is an ***absorber-only defect*** or a ***multilayer surface defect***, the available inspection parameters can be used to try and formulate a predictive model. The parameters provided by the absorber blank inspection results are as follows:

1) *Detectors A, B,* and *C,* as discussed earlier in this section.
2) *Signal strength:* The difference between the reflected optical signal and reference signal.
3) *Reported defect size:* the X and Y defect size as reported by the inspection tool.

The goal is to determine if there are any unique absorber inspection characteristics that point towards distinguishing an ***absorber-only defect*** over a ***multilayer surface defect***. For each detector type, histograms of ***absorber-only defects*** and ***multilayer surface defects*** as a function of absorber inspection signal strength is shown in Figure 3.

From Figure 3a, defects with a *signal strength* >200 from the absorber inspection are likely to remain embedded in the multilayer surface after the absorber is etched. A representative sample of high *signal strength* defects (found by absorber blank inspection) are show in Fig. 4c (SEMs of the defects embedded in the multi-

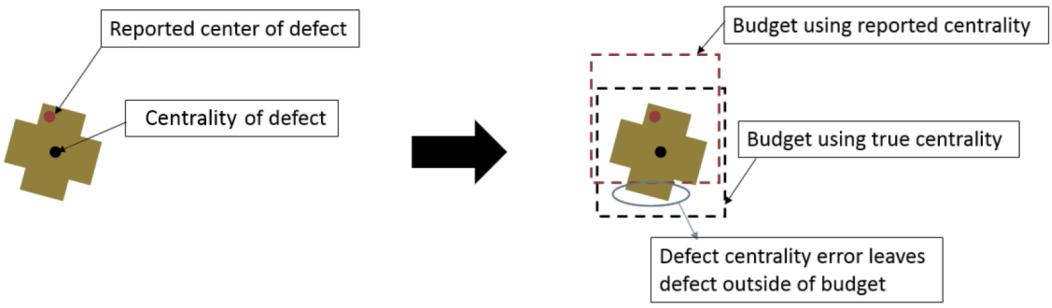

*Figure 7. Schematic of a **defect centrality error** and how it could manifest itself in a parts of the defect outside of the **error budget**.*

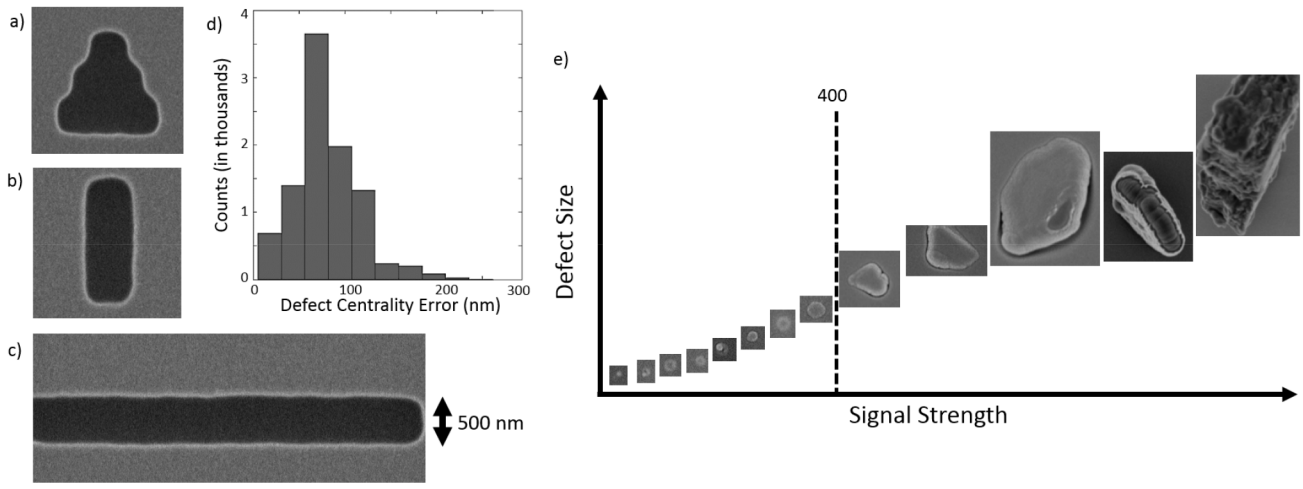

*Figure 8. a-c) SEM of geometrically biased features used to quantify the **defect centrality error**. d) The **defect centrality error** as measured on defects shown in Fig. 8a. e) SEM of native blank defects as a function of* signal strength *reported by the inspection tool.*

layer surface). *Detector A* defects with a *signal strength* <200 and all *Detector B* defects contain a mixture of both ***absorber-only defects*** and ***multilayer surface defects***. Since *signal strength* alone is not enough to distinguish between absorber and multilayer defects, an additional parameter is added: *reported defect size*. Figure 4 shows scatter plots of all defects found by the *Detector A* (Fig. 4a) and *Detector B* (Fig. 4b). Similar to Figure 3a, *Detector A* signal strength >200 consists of all ***multilayer surface defects***. However, even with the addition of the *reported defect size* variable, clustering between the red (***multilayer surface defects***) and black dots (***absorber-only defects***) still occur. The same is true for the *Detector B* defects. This means, using all the parameters provided by the inspection results, it is not possible to predict (separate) which defects are ***absorber-only defects***, for *Detector A* detector defects with a signal strength <200 and all *Detector B* detector defects. Therefore, the entirety of *Detector A* and *B* defects must be included into defect avoidance.

Over 95% of *Detector C* defects are ***absorber-only defects***, as shown in Fig. 3c. This shows that *Detector C* defects are statistically insignificant and can likely be removed from the population of identified defects as requiring avoidance. However, as discussed earlier, it could be that *Detector C* defects are real defects with very low SEM contrast or the defect is out of focus. To investigate this, 30 *Detector C* defects with varying *signal strengths* were characterized with AFM, performed on the absorber before removal. 23% of the absorber defects showed small <5 nm divots. This is consistent with the view that once the absorber is entirely stripped, no physical defect will remain on the multilayer since the defects are just small indents in the absorber. 10% of the defects were bumps in the absorber, with heights ranging from 2 to 30 nm. The other 63% of defects were undetected by AFM. In short, a large majority (90%) of *Detector C* defects are nuisance defects. The other 10% are small (2 nm) to medium size bumps (30 nm), the majority of which are removed during absorber etch and can be deemed as an absorber surface variation. The original conclusion that over 95% of *Detector C* defects are ***absorber-only defects*** is consistent with the AFM results. The high confidence that *Detector C* defects are truly ***absorber-only defects*** justifies the removal of *Detector C* defects from the inspection results.

From this experiment, several conclusions can be made:

1) Roughly 3/4 of defects found by the *Detector A* are ***multilayer surface defects***, however it is not possible to isolate this subset using the available parameters provided by the inspection tool. Thus, all *Detector A* defects must be avoided.

2) Roughly 1/3 of defects found by the *Detector B* detector are ***multilayer surface defects***, however it is not possible to isolate this subset using the available parameters provided

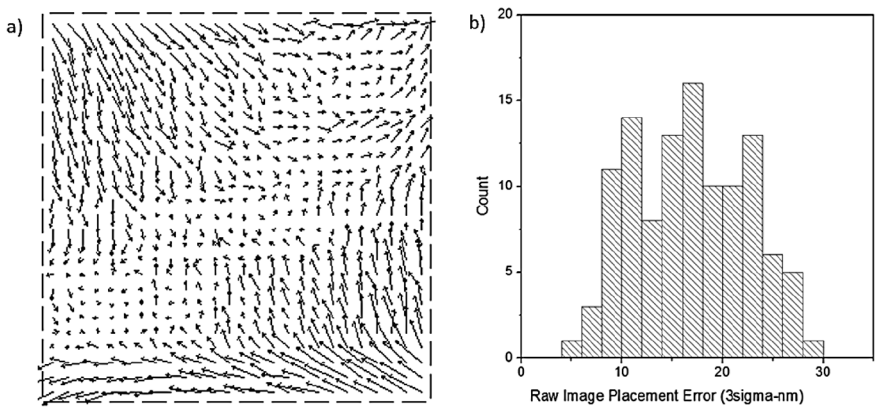

*Figure 9. a) Raw **image placement error** shown as a vector map for a representative EUV mask. b) Raw **image placement error** measured across >60 masks.*

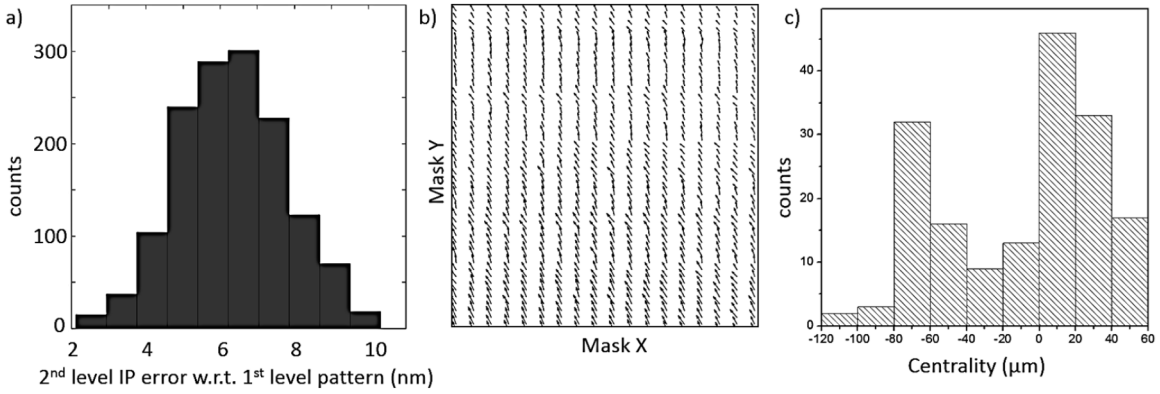

Figure 10. a) Histogram of registered write IP error with respect to a first level pattern as measured by SEM, and its corresponding b) vector map. c) Centrality measured on >60 masks.

by the inspection tool. Thus, all *Detector B* detector defects must be avoided.

3) Less than 4% of defects found by *Detector C* detector are ***multilayer surface defects***. AFM verifies that *Detector C* defects are mainly nuisance defects. *Detector C* defects, or negative phase difference defects, are mainly false positives and can be ignored. However, it's probable that even this 4% may represents enough defects that can result in electrically defective photomasks. For this work, *Detector C* defects are removed from the inspection results.

3.2 Blank inspection coordinate inaccuracy and uncertainty

For pinpointing defects with high accuracy, pre-patterned fiducial marks are needed on the EUV blank to allow for a registered blank inspection. Experimentally, blank ***inspection coordinate inaccuracy*** without fiducial marks have an average error of over 300 µm. With registered inspection, errors are reduced to less than 1 µm. The following section will empirically determine the ***inspection coordinate inaccuracy*** of registered blank inspection.

The coordinates of the defects provided by the inspection tool may not necessarily represent its physical location on mask. In order to budget for any coordinate inaccuracies during blank inspection, a mask is patterned with 30 nm holes spaced 1 mm apart across the entire mask. The mask was inspected five separate times across a 2-month period to include week-to-week variability. Figure 5 shows the calculated distance between the design and inspection-reported hole coordinate for all five inspections. The distribution of difference between design and reported coordinates shows a mean and three-sigma of: $\mu \pm 3\sigma = 77$ nm $\pm$ 114 nm. This value represents the ***inspection coordinate inaccuracy***.

It should also be noted that additional studies have shown location-dependent systematic errors, which could be corrected for across all inspection results to further reduce the coordinate inaccuracy (Fig. 5 vector plot), however, this is not further investigated here as the stability of this error needs to be characterized. Another consideration is the image placement error that could contribute to the $\mu \pm 3\sigma = 77$ nm $\pm$ 114 nm ***inspection coordinate inaccuracy*** value. The raw (ortho and scale not removed) image placement (IP) error was measured on 10,000 700 x 700 nm contacts spaced equidistant across the mask. A 3-sigma image placement error of 10 nm was measured. This error is convoluted with the ***inspection coordinate inaccuracy***, however, represents only a small portion of the total coordinate inaccuracy ($\mu \pm 3\sigma =$ 77 nm $\pm$ 114 nm). Because of the small contribution, steps were not taken to compensate for the distributed IP error across mask.

3.3 Blank inspection defect sizing error

Inspection systems provide an X and Y defect size, but based on past work, discrepancies remain between the physical size of

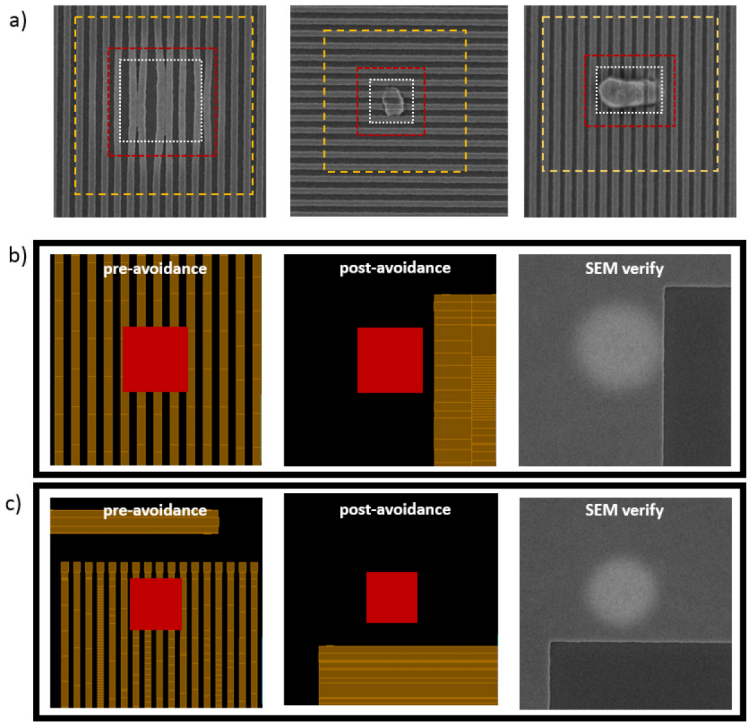

Figure 11. a) Examples of native defects that could not be avoided and its impact on the main pattern. White dotted box represents the predicted defect size. Red dotted box includes the error budget imposed for that particular defect to guard band against variability. Yellow box represents the defect size reported by the inspection system. b-c) Pre- and post-pattern shift of two representative native defects shown in design, along with SEM verification of successful pattern placement post-patterning.

the defect and what is reported.[16,20,21] The following work tries to quantify and compensate for this discrepancy. *Physical defect size* varies drastically from what is provided in the inspection results. Figure 6a shows that *physical defect size* as measured with SEM is roughly two to three times smaller than the *reported defect size* by the inspection tool.

To try and compensate for the ***defect sizing error***, a predictive model is constructed to try and estimate the *physical defect size* from all available parameters in the inspection report. Figure 6b shows a scatter plot of correlation between *physical defect size* as measured by SEM and the r*eported defect size* and *signal strength* provided by the inspection tool.

Fitting this data to a 2D polynomial:

$$z = z_0 + Bx + Cx^2 + Dx^3 + Ex^4 + Fx^5 + Gy + Hy^2 + Iy^3 + Jy^4 + Ky^5$$

Where z is the *physical defect size*, x is the *reported defect size*, and y is the *signal strength*. Figure 6c shows the result of the fit, with a $\mu + 3\sigma$ = 0 nm + 174 nm. Since the 3σ value applies to the entire length of the defect, to incorporate it into β, which is the buffer zone surrounding the entire defect (Fig. 1d), the 3σ value is halved. Note, the 3σ is not halved for the ***inspection coordinate inaccuracy*** because the defect position is allowed to move both + and – directions. By incorporating a predictive model for the physical defect size, the ***defect sizing error*** contribution to β is 3σ = 87 nm.

3.4 Blank inspection defect centrality error

For large defects, the center of the defect could be misrepresented by the inspection system. This could manifests in defects where the real perimeter fall outside of the error budgeted areas. Figure 7 shows an example of a ***defect centrality error*** and how a portion of the defect falls outside of the ***error budget***. To quantify the ***defect centrality error***, an experiment is devised to measure this error.

To compensate for this error, geometrically biased features (Fig. 8a-c) are patterned apart across an EUV blank. The substrate is then inspected in blank inspection mode. To remove the ***defect coordinate inaccuracy***, the vector map shown in Fig. 5 is subtracted from the inspection results. Ideally, the inspection should report the exact center of the programmed defect after compensating for the ***defect coordinate inaccuracy***. Defects shown in Fig. 8b and 8c do not present any ***defect centrality error***. For the defect shown in Fig. 8a, a ***defect centrality error*** of $\mu \pm 3\sigma$ = 80 nm ± 102 nm is measured, as shown in Fig. 8d. This error only manifests in large defects where the center of mass is different from the actual "center" of the defect. That is, defects such as Fig. 8b and 8c have a center of mass at the defect's centrality, thus do not present any centrality error. However, defects where the centrality of the defect is different from its center of mass (Fig. 8a), an error is seen. With this insight, a ***defect centrality error*** must be applied to large defects where its centrality is different from its center of mass. Looking over the SEM of defects and its corresponding *signal strength*, a trend can be observed (Fig. 8e). Defects with *signal strength* <400 are consistently circular, while defects with *signal strength* >400 appear more irregular, indicating that the reported defect center may deviate from its true center. Thus, to account for the ***defect centrality error***, applying a μ +

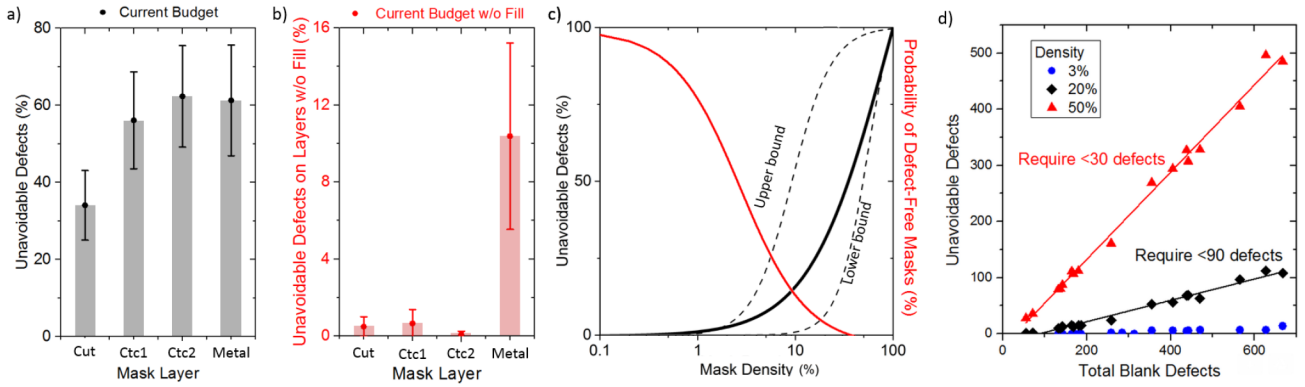

Figure 12. a) Average percentage of defects (per blank) that could not be avoided for N7 node EUV mask layers (gate cut, metal, and two contact levels). b) Average percentage of defects that could not be avoided for layers shown in 12a, fractured without fill. c) Fitted experimental results, showing the average percentage of unavoidable defects as a function of mask density (black) and probability of making a defect-free mask (red). d) Number of unavoidable defects as a function of the total blank defect count for a 3%, 20%, or 50% exposure field pattern density.

3σ = 80 nm ± 102 nm error for defects with *signal strength* >400 is necessary.

3.5 Write tool image placement error and fiducial mark centrality

Raw ***image placement error*** measured across a single mask is shown in Figure 9a. The raw data shown includes scale and orthogonality errors, as this cannot be corrected for during primary pattern write. For the particular mask shown in Figure 15a, there is a raw 3sigma ***image placement error*** of 9.6 nm in X and 11.3 nm in Y. To account for mask-to-mask variability, the raw image placement error across >60 masks is shown in Figure 9b. The following formula is used to obtain an average 3-sigma from the collection of 3-sigma values:

$$3\sigma_{avg} = 3\sqrt{\frac{\sum_{i=1}^{n}\sigma_i^2}{n}}$$

An average 3-sigma of 17.5 nm was extracted as the raw ***image placement error***.

An empirical test was performed to experimentally measure errors incurred from a registered write. A first level pattern of 200 nm wide crosses spaced equidistance across the mask was exposed, along with fiducial marks at the corners of the mask for registered patterning. A second level registered write (relative to fiducial marks) placed 200 nm lines parallel to each cross feature patterned during first level write. SEM was used to measure the XY shift of the second level write relative to first level feature across the mask.

A histogram of the magnitude of all registered write IP errors (magnitude of vector formed between first level and second level write) is shown on Fig. 10a, with a mean and 3sigma of: μ ± 3σ = 6.3 nm ± 4.4 nm. From the vector map (Fig. 10b), systematic errors can be observed. Specifically, arrows tent to have a north-west direction. This is likely due to a registration offset error that would cause a constant offset to all the 2nd level patterns. The variation in the direction and magnitude of the vectors represents the ***image placement error***. While the measured mean+3sigma error of 11 nm for this particular mask includes both a registered image placement error and registration offset error, it is within the measured average 3sigma ***image placement error*** of 17.5 nm shown in Fig. 9b. For the error budget, a 3σ of 17.5 nm will be used for the raw ***image placement error*** for a registered write.

Besides the ***error budget***, there is a physical limit to how much the pattern can be shifted, as defined by scanner centrality spec of ±200 μm. The centrality of the fiducial marks determine the maximum translation allowed for pattern shift. Figure 10c shows the centrality of patterns in close proximity to the fiducial marks measured across >60 EUV masks. The majority of patterns consist of a centrality offset less than 100 μm. Based on the distribution, a maximum pattern shift of ±100 μm is maintained to guard band against shifting a pattern beyond the limits of the scanner.

3.6 Combined Error Budget

The combined error budget, β, can be summarized as follows:

1) Omit the negative phase contrast defects found by *Detector C* (§3.1)
2) ***Inspection coordinate inaccuracy***: μ ± 3σ = 77 nm ± 114 nm (§3.2)
3) ***Defect sizing error***: μ ± 3σ = 0 nm ± 87 nm (§3.3)
4) For defects with *signal strength* >400, apply a ***defect centrality error***: μ ± 3σ = 80 nm ± 102 nm (§3.4)
5) ***Image placement error***: average 3σ = 17.5 nm (§3.5)

To add mean and 3-sigma: $\beta = \sum_{j=1}^{m}\mu_j + 3\sqrt{\sum_{i=1}^{n}\sigma_i^2}$

In summary, the mean+3sigma ***error budget*** is as follows:

$$\beta = \begin{cases} 221\,nm\ , & \text{if signal strength} < 400\ \&\ \text{Detector != negative phase contrast detector} \\ 334\,nm\ , & \text{if signal strength} > 400\ \&\ \text{Detector != negative phase contrast detector} \end{cases}$$

With a maximum design shift allowed of ±100 μm. (§3.5)

4. Experimental Verification

Various methodologies for optimum defect avoidance have been discussed in the past.[16–18,22–30] An X and/or Y translation of the full-chip design relative to the blank is fundamental, however, additional degrees of freedom can also be considered, such as 90-degree rotations, micro-rotations[30], and mask floorplanning[22,29]. Previous work have shown that micro-rotations and floorplanning provides only slight improvements for defect avoidance, despite the considerable complexity and resource allocation needed for HVM implementation.[24]

The following studies will implement pattern shift, with a linear translation limited to ±100 μm (as discussed in Section 3.5), and

also allow for 0º, 90º, 180º, or 270º orientations. Only defects located within the exposure field are used for calculating the pattern shift. For experimental verification of the error budget and successful defect avoidance, a mask design with a 34% pattern density was printed on a blank consisting of 892 defects that required avoidance, of which, theoretically, 431 defects could not be avoided after performing pattern shift.

SEM images of defect locations were taken of the patterned mask. Of the 431 native defects that could not be avoided, roughly 55% did not visibly to impact the mask features post-patterning, while all avoidable defects were successfully hidden under the absorber. The percentage of defects that did not show a visible impact on the final pattern is consistent with the conclusions made in §3.1, that is, that a quarter to two-thirds of defects found by the inspection tool were not visible by SEM. However, even if these defects represented false positives, it is still not possible to predictively filter these defects using the available variables provided from the inspection results (detailed in §3.1) and thus the defect list in its entirety is used for pattern shift.

Pattern shift was successfully implemented. Figure 11a shows SEMs of native defects that could not be avoided, and its impact post-patterning. The grey dotted box represent the predicted defect size (§3.3). Red dotted box includes the error budget imposed for that particular defect to guard band against variability (§3.6), while the yellow box consistently outlines the oversized defect size as reported by the inspection system. Overall, the predictive defect size model consistently shows high accuracy in determining physical defect size for well-defined native defects, as seen in the middle and right SEM of Figure 11a. However, native defects with vaguely defined boundaries, as seen in SEMs shown in Figure 11a left, b, and c, shows the model slightly undersized the visual extent of the defect, however the error budget appropriately attempts to compensate for this error. Figure 11b-c shows the expected location of two native defects in design before and after pattern shift. SEMs of the defect locations verifies that the defects were successfully hidden underneath the absorber and matches the post-pattern shift designs.

This section empirically validates the work done in Section 3 and also verifies successful pattern shift implementation. Based on the validated error budget and current blank defectivity rates, the next section investigates the viability of defect-free masks for relevant N7 layers.

5. Viability of Defect-Free Masks for N7

Twenty EUV blanks were inspected with 193 nm light using detectors that looked for amplitude changes arising from scattering/absorption of light as well as any phase offsets between then reference and reflected light (detailed in §3). The inspections were operated at higher sensitives than suggested, in order to safeguard against false negatives. A custom script is used to correct the inspection results, such as incorporating a predictive defect size model (§3.3) and removing false positives (§3.1), and apply the combined error budget defined in §3.6. Four different N7 EUV mask layers (gate cut, metal, and two contact levels) were used for pattern shift simulations to explore a range of pattern densities and layer types. Figure 12a shows the results of pattern shift on these levels, with 30% - 60% of total blank defects exposed (unavoidable) after implementing pattern shift, indicating defect-free fabrication is unlikely with current blank defect levels. A second set of simulations utilized the same set of mask layers but were fractured without dummy fill patterns. That is, features which do not contribute to the active device are removed from the structures that need to be avoided. Pattern shift results for layers without fill are presented in Figure 12b, showing the percentage of unavoidable defects drops to reasonable levels for cut and contact layers. However, on average 10% of total blank defects still remain for the metal layer. Figure 12c presents a fit to the experimental data, showing unavoidable defect rates as a function of mask density, in black, and the probability of fabricating defect free masks as a function of pattern density, in red.

Depending on how the density is distributed across the exposure field, there could be a high probability of fabricating defect-free masks up to 10% pattern densities (Fig. 2, lower bound). These mask would require a highly uniform pattern density distribution across the entire exposure field. That is, from Figure 2, it is clear that defects are distributed randomly across the blank – if a single large block pattern that represented 10% of the exposure field was the only feature to be printed on mask, it would be nearly impossible to shift the pattern into a defect-free region given the purely random distribution of native defects. The highest probability of creating a defect-free mask would consist of having sparse features uniformly distributed across the entire exposure field such that the overall pattern density sums to 10% coverage of the exposure field. The lower and upper bounds in Figure 12c represent the experimental variability of due to the varying local density distribution of the pattern and also variable blank defect rates.

Figures 12c and 12d represents generalizations of the experimental data. Figure 12c shows that if current blank defectivity remained constant, what types of mask densities would allow for defect-free fabrication, if pattern shift was implemented. Figure 12d shows that there is large variability in controlling blank defectivity, and that a complete EUV mask-set would be possible only if the native defect count reduced to less than one hundred, as found by a 193 nm inspection system. For typical contact and via layers fractured without fill, less than 2% of total blank defects are exposed after implementing pattern shift (Fig. 12b), with $\geq$ 50% likelihood of avoiding all native defects across the mask (Fig. 12c). For higher density metal layers, over 10% of total blank defects are exposed after pattern shift (Fig. 12b), with less than 5% probability of avoiding all defects (Fig. 12c). This would indicate that particular mask layers (e.g., CT, CA, V0, etc.), fractured without fill, are aptly positioned for HVM, while higher density layers (e.g., M1, M2, etc.) requires lower native defects to achieve complete defect avoidance. Figure 12d shows the experimental trend for the number of unavoidable defects as a function of total blank defects. The wide spread of total blank defects, ranging from less than 100 to over 600, indicates the variability of defect control during blank fabrication. However, if the linear trend of unavoidable defects were to scale as a function of total blank defectivity, the experimental results show that higher density patterns would require at blanks with less than one hundred total defects, as found by the 193 nm inspection system. This advocates the continued effort to reduce overall blank defectivity to allow the construction of a complete defect-free mask set.

While this work provides insight into current tool capabilities from the perspective of making defect-free masks, it does not address the fact that not all blank defects can be found during 193 nm blank inspection.[12] To identify all potential defects buried in the multilayer stack, actinic blank inspection (ABI) at 13.5 nm is required.[31] Despite the potential impact on the conclusions made in this work, actinic inspection tools under development are not considered here as it is uncertain when ABI and actinic pattern mask inspection tools will reach HVM availability. The current conclusions could thus remain relevant until a HVM inspection tool is available.

6. Conclusions

Taking into account the latest EUV HVM toolset and their inherent errors/variability, along with current blank defect rates, pattern shifted mask layers with densities ≤ 3% have at least 50% probability of achieving defect-free fabrication. In other words, with four inspected blanks available to choose, there is >93% likelihood of making a defect-free mask, enabled by pattern shift. The results are based on defects found using 193 nm amplitude/phase-contrast blank inspection, which ensures sensitivity to smaller defects and differentiates from past work that were largely based on 488 and 266 nm inspection systems.[6,10,11] The work indicates that particular mask layers (e.g., CT, CA, V0, etc.), fractured without fill, are aptly positioned for HVM. However, despite continued improvements in the overall blank defect count, the native amount is still too high to achieve zero defects for higher density mask layers that were also fractured without fill (e.g., M1, M2, etc.). This advocates the continued effort to reduce overall blank defectivity to allow the construction of a complete defect-free mask set.

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8. References

[1] Pirati, A., Peeters, R., Smith, D., Lok, S., Minnaert, A., van Noordenburg, M., Mallmann, J., Harned, N., Stoeldraijer, J., et al., "Performance overview and outlook of EUV lithography systems," **Proc. SPIE 9422,** 94221P (2015).

[2] Montgomery, W., Chun, J. S., Liehr, M., and Tittnich, M., "The patterning center of excellence (CoE): an evolving lithographic enablement model," **Proc. SPIE 9422,** 94221L (2015).

[3] Mcintyre, G., Teeuwen, L., Sohmen, E., Wood, O., Corliss, D., van den Akker, T., Bouten, S., van Setten, E., Voznyi, O., et al., "Enhancing resolution with pupil filtering for projection printing systems with fixed or restricted illumination angular distribution," **Proc. SPIE 8679,** 86792N (2013).

[4] Qi, Z. J., Gallagher, E., Negishi, Y., Mcintyre, G., Zweber, A., Senna, T., Akutagawa, S., and Konishi, T., "Impact of EUV photomask line edge roughness on wafer prints," **Proc. SPIE 8522,** 85222H (2012).

[5] Jonckheere, R., Van den Heuvel, D., Pacco, A., Pollentier, I., Baudemprez, B., Jehoul, C., Hermans, J., and Hendrickx, E., "Towards reduced impact of EUV mask defectivity on wafer," **Proc. SPIE 9256,** 92560L (2014).

[6] Antohe, A. O., Balachandran, D., He, L., Kearney, P., Karumuri, A., Goodwin, F., and Cummings, K., "SEMATECH produces defect-free EUV mask blanks: defect yield and immediate challenges," **Proc. SPIE 9422,** 94221B (2015).

[7] Badger, K. D., Qi, Z. J., Gallagher, E., Seki, K., and McIntyre, G., "Illuminating extreme ultraviolet lithography mask defect printability," *J. Micro/Nanolithography, MEMS, MOEMS 12(2)*, 021004 (2013).

[8] Badger, K. D., Qi, Z. J., Gallagher, E., and Seki, K., "Illuminating EUVL Mask Defect Printability," **Proc. SPIE 8522,** 85220I (2012).

[9] Rankin, J., Qi, Z. J., Lawliss, M., Narita, E., Seki, K., Badger, K., Halle, S., and Turley, C., "EUV Photomask Defects: What prints, what doesn't, and what is required for HVM," **Proc. SPIE 9635** (2015).

[10] Kwon, H. J., Harris-Jones, J., Teki, R., Cordes, A., Nakajima, T., Mochi, I., Goldberg, K. a., Yamaguchi, Y., and Kinoshita, H., "Printability of native blank defects and programmed defects and their stack structures," **Proc. SPIE 8166,** 81660H (2011).

[11] Mangat, P., Verduijn, E., Wood, O. R., Benk, M. P., Wojdyla, A., and Goldberg, K. a., "Mask blank defect printability comparison using optical and SEM mask and wafer inspection and bright field actinic mask imaging," **Proc. SPIE 9658,** 96580E (2015).

[12] Seki, K., Isogawa, T., Kagawa, M., Akima, S., Kodera, Y., Badger, K., Qi, Z. J., Lawliss, M., Rankin, J., et al., "ENDEAVOUR to understand EUV buried defect printability," **Proc. SPIE 9658,** 96580G (2015).

[13] Takagi, N., Watanabe, H., Van den Heuvel, D., Jonckheere, R., and Gallagher, E., "EUV scanner printability evaluation of natural blank defects detected by actinic blank inspection," **Proc. SPIE 9658,** 96580F (2015).

[14] Takeshi, I., Seki, K., Lawliss, M., Qi, Z. J., Rankin, J., and Akima, S., "Evaluation of multilayer defect repair viability and protection techniques for EUV masks," **Proc. SPIE 9635** (2015).

[15] Lawliss, M., Gallagher, E., Hibbs, M., Seki, K., Isogawa, T., Robinson, T., and LeClaire, J., "Repairing native defects on EUV mask blanks," **Proc. SPIE 9235,** 923516 (2014).

[16] Negishi, Y., Fujita, Y., Seki, K., Konishi, T., Rankin, J., Nash, S., Gallagher, E., Wagner, A., and Thwaite, P., et al., "Using pattern shift to avoid blank defects during EUVL mask fabrication," **Proc. SPIE 8701,** 870112 (2013).

[17] Wagner, A., Burkhardt, M., Clay, A. B., and Levin, J. P., "Mitigation of extreme ultraviolet mask defects by pattern shifting: Method and statistics," *J. Vac. Sci. Technol. B 30* (5), 051605 (2012).

[18] Burns, J. and Abbas, M., "EUV mask defect mitigation through pattern placement," **Proc. SPIE 7823,** 782340 (2012).

[19] "IBM Research Alliance Produces Industry's First 7nm Node Test Chips.", <https://www-03.ibm.com/press/us/en/pressrelease/47301.wss> (9 July 2015).

[20] Bhamidipati, S., Paninjath, S., Pereira, M., and Buck, P., "Automatic classification and accurate size measurement of blank mask defects," **Proc. SPIE 9658,** 96580X (2015).

[21] Gallagher, E., Wagner, A., Lawliss, M., McIntyre, G., Seki, K., Isogawa, T., and Nash, S., "Learning from native defects on EUV mask blanks," **Proc. SPIE 9256,** 92560K (2014).

[22] Ali Kagalwalla, A., Lam, M., Adam, K., and Gupta, P., "EUV-CDA: Pattern shift aware critical density analysis for EUV mask layouts," *Proc. Asia South Pacific Des. Autom. Conf. ASP-DAC,* 155–160 (2014).

[23] Du, Y., Zhang, H., Wong, M. D. F., and Topaloglu, R. O., "EUV mask preparation considering blank defects mitigation," **Proc. SPIE 8166,** 816611 (2011).

[24] Elayat, A., Thwaite, P., and Schulze, S., "EUV mask-blank defect avoidance solutions assessment," **Proc. SPIE 8522,** 85221W (2012).

[25] Kagalwalla, A. A. and Gupta, P., "Comprehensive Defect Avoidance Framework for Mitigating EUV Mask Defects."

[26] Kagalwalla, A. A., Member, S., and Gupta, P., "Design-Aware Defect-Avoidance Floorplanning," *IEEE Trans. Semicond. Manuf. 26 (1)*, 111–124 (2013).

[27] Schmoeller, T., Klimpel, T., Kim, I., Lorusso, G. F., Myers, A., Jonckheere, R., Goethals, a. M., and Ronse, K., "EUV pattern shift compensation strategies," **Proc. SPIE 6921,** 69211B (2008).

[28] Yan, P.-Y., Liu, Y., Kamna, M., Zhang, G., Chen, R., and Martinez, F., "EUVL Multilayer Mask Blank Defect Mitigation for Defect-free EUVL Mask Fabrication," **Proc. SPIE 8322,** 83220Z (2012).

[29] Du, Y., Zhang, H., Wong, M. D. F., Deng, Y., and Topaloglu, R. O., "Efficient multi-die placement for blank defect mitigation in EUV lithography," **Proc. SPIE 8322,** 832210–832231 (2012).

[30] Zhang, H., Du, Y., Wong, M. D. F., Deng, Y., and Mangat, P., "Layout small-angle rotation and shift for EUV defect mitigation," **Proc. ICCAD**, 43–49 (2012).

[31] Takagi, N., Watanabe, H., den Heuvel, D., Jonckheere, R., and Gallagher, E., "EUV scanner printability evaluation of natural blank defects detected by actinic blank inspection," **Proc. SPIE 9658,** 96580F (2015).

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Industry Briefs

EUV Gets $500M Center

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Globalfoundries and SUNY Polytechnic Institute will spend a total of $500 million over five years to create a new R&D center to accelerate the introduction of Extreme Ultraviolet (EUV) lithography into the 7nm process node and beyond. The move is the latest sign EUV will finally make its way into production fabs, albeit probably not until 2018.

The Advanced Patterning and Productivity Center will be located at the Colleges of Nanoscale Science and Engineering (CNSE) in Albany, N.Y. It will have a ASML NXE:3300 EUV scanner and a staff of about 100 researchers. According to Garry Patton, chief technology officer and senior vice president of worldwide R&D at Globalfoundries, EUV "has gone from unrealistic exuberance four or five years ago to pessimism two or three years ago to our current thinking, it's going to be real as early as 2018-2019." The center will work on the full range of outstanding issues to make EUV viable for production fabs: masks, resists, and EDA software, with partners including IBM and Tokyo Electron. "EUV technology has emerged from R&D and the new center will meet the rising demand to commercialize this technology and put it in the hands of end users," said Gishi Chung, a senior vice president at Tokyo Electron. The much delayed EUV effort has required billions of investments from big chip makers including Intel and TSMC.

EUV 2.0 Decision Needed: Time to Start the Engineering, says Mask Expert

Source: **EE Times**

http://www.eetimes.com/document.asp?doc_id=1329033&

It's time to come to consensus about the next generation of extreme ultraviolet lithography systems, even though first-generation EUV steppers have not yet entered production fabs. "We need to nail down the next-gen EUV approach," said Franklin Kalk, chief technology officer of Toppan Photomasks Inc. told *EE Times*. "There's been a lot of talk about an anamorphic approach, not using today's 4x reticle, but one that is 4x one way and 8x another way…if [that's the best approach] the mask and OPC guys need to know that," said Kalk who received a lifetime achievement award at this week's SPIE Photomask Technology conference.

"The design studies I've seen for 4x by 8x look pretty good, I think it's a good solution," said Kalk. "There are all kinds of things people are talking about doing [for next-gen EUV]…but we need to seize on the next-gen concept so engineering work can start," he added.

Moore's Law Goes Post-CMOS

Source: **EE Times**

http://www.eetimes.com/document.asp?doc_id=1328835

Moore's Law has a long life, but pure vanilla CMOS process technology — not so much, according to Intel's top fab executive. "The economics of Moore's Law are sound if we focus on reducing cost per transistor," William Holt told about 3,000 attendees of the International Solid-State Circuits Conference (ISSCC). But beyond CMOS we'll see changes in everything, probably even in computer architecture.

The general manager of Intel's technology and manufacturing group declined to share his thoughts about which of a "rich variety" of post-CMOS technologies chip makers will use or when. New techniques span tunneling FETs, ferroelectric FETs, spintronics, new III-V materials and more. Holt did assert the new techniques won't be in Intel's 10nm process in which Intel is now prototyping its next-generation processors. In general, engineers will stretch CMOS as far as possible. Longer term, chips will be hybrids of different techniques blended with traditional CMOS. "We will see a mixed mode operation…parts [of the wafer] with CMOS and new devices on same wafer optimized for different benefits," he said.

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