PHOTOMASK

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A study on the ESD damage of a silicon oxy-nitride hard mask on the chromium surface of PSM blank

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ABSTRACT

A thin silicon oxy-nitride hard mask on the PSM blank is needed for the feature patterning with the size smaller than 70 nm. It is a good material for hard mask. However, the electrical property of silicon oxy-nitride with the thickness smaller than 10 nm causes the chromium surface damage during the mask processes. From the measurement of the surface damage, we figure out that the chromium surface damage is originated from the charging and the dielectric breakdown phenomena. In our present work, two types of silicon oxy-nitride film with the thicknesses of 5 nm and 12 nm are tested for verifying optimal mask fabrication processes. We find that the occurrence of ESD damage is related to the thickness of silicon oxy-nitride hard mask and mask fabrication process conditions. The optimal fabrication process condition for silicon oxy-nitride thin film hard mask, in which break-down never occurs, is discussed.

1. Introduction

In semiconductor business, phase shifted masks (PSM)[1,2] are important devices which can achieve the more resolution power of a binary mask. Especially, PSM mask is widely used because of its high resolution power among many benefits. Unfortunately, the normal PSM still has patterning size limit because of the limit of Cr mask thickness on the MoSi layer.

Recently, silicon oxide hard masks that enable to resist the lower thickness and the more resolution power without Cr thickness changes have been adopted. It is suggested that the SiO_x(or SiON) hard masks sustain their profile after resist erosion and have no problem in the PSM manufacturing process.

As shown in Figure 1, we report on the electrostatic discharge (ESD) defect of PSM and physical properties of silicon oxide hard mask for the first time. In this paper, we used two methods for solving the ESD problems; one is physical property comparison of silicon oxide (SiO_x) and oxy-nitride (SiON) hard masks and the other is severe test verification for conditions causing ESD defect with hard mask PSM.

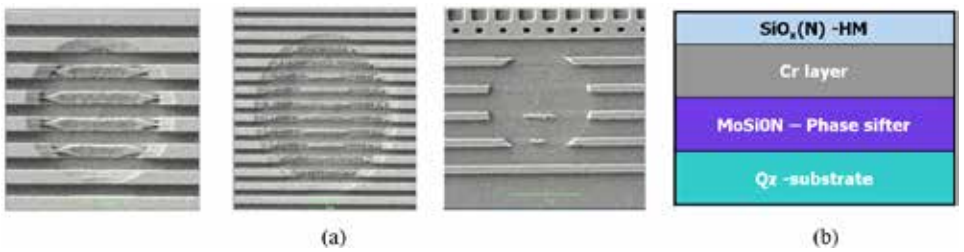

Figure 1. SEM image of electro static discharge damage on PSM blanks due to wet processes (a) and HM-PSM structure (b).

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EDITORIAL

EUV Mask Integration, are we ready?

Bryan S. Kasprowicz, Photronics, Inc.

As one surveys the top inhibitors of EUV, the original ~~usual~~ suspects are still at the top of the list: source power, mask and resist. Recent data suggests that the source power is expected to meet the much relaxed initial expectations of 80 Watts and with a little good fortune, production EUV exposure systems would come online in the second half of 2014. Yet there is still a fair amount of uncertainty with the other two. Resists are still suffering from resolution, LER and sensitivity issues, while masks are languishing due to the lack of adequate mask blank. While we do not want to minimize the importance of the source and resist as key components to the success of the technology; our focus here is on masks.

The industry appears in agreement that the number one EUV mask priority is defect reduction. Number two, defect reduction. Number three, defect reduction. Well, you get the idea. Improving blank quality by reducing defects will not only improve mask manufacturability and drive overall quality blank capacity, but also help enable a successful EUV insertion. Still, there are also other items that the industry has been discussing, such as new targets for CTE due to OOB radiation absorption, absorber and centroid wavelength harmonization to minimize the number of different mask types, and fiducial mark implementation. These are in addition to concerns about mask lifetime, capping layer improvements and the need for a (non-existent) pellicle. While these items impact the blank and its availability, they do not take into consideration fab (mask and wafer) integration or how the masks will be shipped, managed and used. This is an area that perhaps needs more attention as EUV gets introduced into manufacturing.

Over time, wafer fabs have developed various approaches to integrate — manage, monitor and extend the lifecycle — of advanced optical masks. An effective wafer fab management system for masks considers each step from shipping to receiving: incoming qualification, storage, use monitoring, recertification and occasional reprocessing. Certain steps, such as re-pellicle and cleaning, may involve a shipment of the mask from wafer fab to mask operation and back. In the case of the EUV mask, it is conceivable a very different mask management flow may be necessary. So, do we really appreciate the EUV mask integration challenges that lay before us as an industry? Are we aware of unique requirements for managing production grade EUV masks in the wafer fab? Are there any critical infrastructure gaps in the process flow? Do we know what mask processing capability will be required within the wafer fabs to sustain EUV? Systems integration may be one the keys that drive its success or failure.

Now with the insertion of EUV approaching, this attention to details becomes more prevalent. A number of EUV blank and mask related papers were presented at SPIE Advanced Lithography last month. They reviewed new structures, improvements and schemes but there was not much mention of integration. The BACUS panel held as part of the symposium highlighted fab environment integration as the new elephant in the room for EUV masks and attempted to be the catalyst that drives more effort in this area.

Many of us are industry veterans and seasoned enough to have experienced technology and integration advances before with 1X masks then 5x and 4x reduction lithography, DUV – KrF then ArF, high NA, hyper NA immersion and multi-patterning. Each one had their respective challenges early but with perseverance and innovation, they were well integrated into high volume manufacturing environments. EUV masks have a few more requirements, such as the need for inspection (AIMS and pattern) and cleaning before each use due to lack of pellicle. The higher cost of equipment and lower EUV volumes (as compared to optical) will make the initial integration more expensive than optical. However with continued progress on improving blanks, mask manufacturability, pellicles and practical integration, there doesn't appear to be any fundamental technical reason why they can't be added to the list of successes given the appropriate attention.

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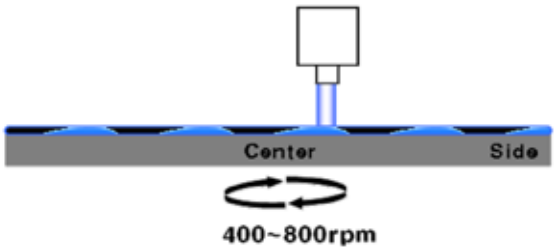

Figure 2. Charging procedure with DI-water rinse process causing ESD defect.

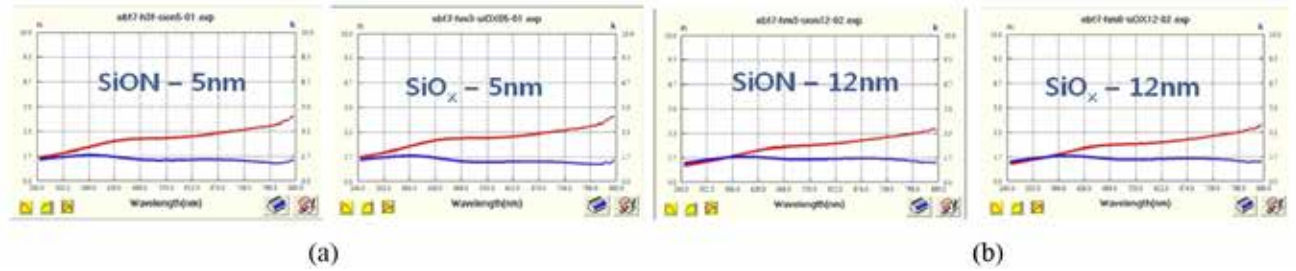

Figure 3. The reflection measurement of N, K specta(two materials with different compositions of H-M on Cr and thicknesses of (a) 5nm and (b) 12nm).

2. Experimental Details

Commercial hard mask (HM) PSM blanks were prepared to test process performance regarding improvement of process stability or defect. To check ESD, we used two different thicknesses of silicon oxide and silicon oxy-nitride hard masks. Each has a slightly different composition. All the materials basically have structures of silicon dioxide but in the case of silicon oxy-nitride, some of oxygen atoms are replaced by nitrogen atoms.

By using the ellipsometer, we find out the optical properties, N and K values. They are measured in order to find the differences of optical properties of SiO_x and SiON. The N and K spectra are measured at the surface of HM-PSM blank.

The morphology was measured by AFM (NanoScope) machine. The extent area of surface morphology measurement region is defined as 25um^2. The measured data were analyzed by averaged total roughness data. To check the etch rate of silicon oxy-nitride (or SiOx) top layer, we used gas A and gas B in this study. The etch rates were compared with two different material samples. And we used negative resist for patterning test.

Finally, we try to do ESD stress test using DI water rinse process for charging up procedure. Figure 2 shows the details of charging procedure. We put the DI-water rinse nozzle at the position which is located at 0.8 cm away from the center. We also observed the defect increase before and after DI water rinse process with blank inspection tool (Magics, M6641).

3. Results

Figure 3 shows the results of optical N and K spectra of two different materials with different thicknesses. From the results of N and K values, we find that there is no difference between SiON and SiO_x.

The surface roughness is measured by AFM machine. The measured roughness is shown in Figure 4. From the results, it is found that the surface morphologies of the two different materials are similar.

Figure 5 shows the etch rate differences of SiO_x and SiON hard mask (HM) components. The etch rate of SiO_x is faster than that of SiON HM component with gas A by 10% as shown in Figure 5 (a). We used two gases for etch rate comparison tests. The etch rates of two HM components with gas A and B are similar as shown in Figure 5 (b). There are no big differences of etch rates with using different gases A and B.

After HM etch rate test, HM-PSM pattering characteristics were checked by using linearity patterns which had 3 different shapes (Iso-Line, Iso-Space, and Line-Space). Figure 6 shows the patterning results. The shape of linearity pattern of SiO_x is slightly different from that of SiON. However, the critical dimension (CD) linearity curves of SiO_x and SiON are different only below the size of 150 nm as shown in Figure 6. This CD linearity difference may result from using the different printing machine grades of Ebeam-5K and Ebeam-8K for SiO_x and SiON, respectively.

Here we report severe test verification for conditions causing ESD defect. As mentioned before, we used DI-water rinse process for ESD test. When the rotation speed was increased, we could make the ESD occurrence probability highly. From the experiment, we took two speed conditions. One is 400 rpm and the other is 800 rpm. Figure 7 shows the experimental results. When the blank rotation speed is over 800 rpm, the ESD defect was formed as expected. And we also changed the thickness of HM from 5 nm to 12 nm. As increasing the thickness of HM, we observed that the number of ESD defect decreased. However the corresponding experimental data were not shown in this paper.

We tested whether the diameter size of ESD defect might have correlation with the material components. Figure 7 shows that the diameter sizes of ESD defect of SiO_x and SiON are

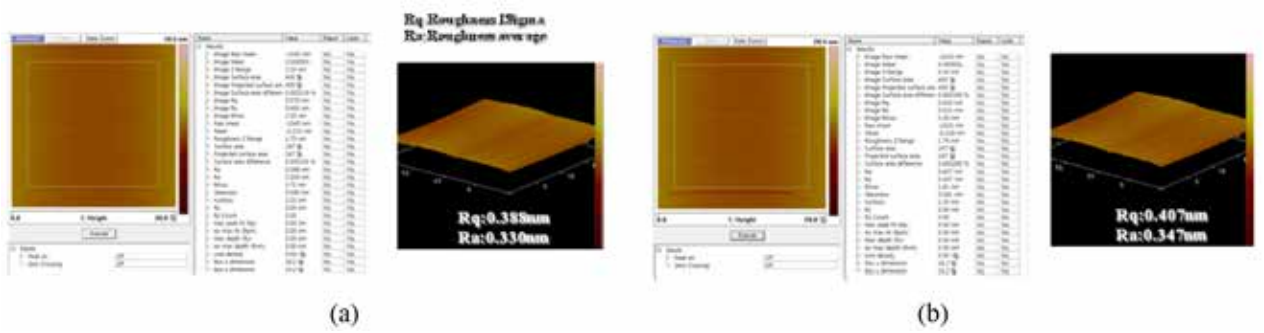

Figure 4. The AFM morphology of (a) SiON(Ra:0.33um) and (b) SiO_x(Ra:0.35um) hard mask components.

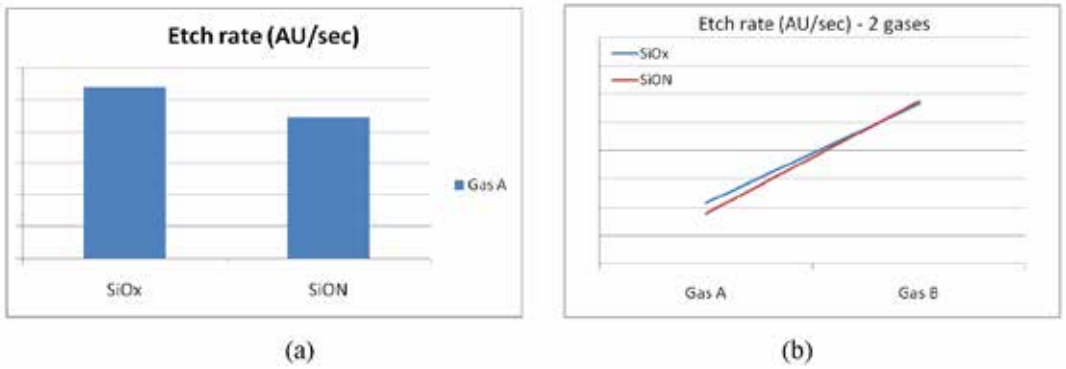

Figure 5. (a) The etch rate difference of SiO_x and SiON HM with gas A. (b) The etch rate difference using different gases A and B.

Table 1. The dielectric permittivity (calculated) from experimental results (using capacitor models).

	SiON	SiOx	Remarks
Dielectric permittivity(ε_r)	5-10	3-4	From experimental results (ESD) and modeling
Roughness	0.40nm	0.36nm	Similar
n, k	1.5-1.6	1.5-1.6	Similar

different. In detail, at the HM thickness of 5nm on Cr, we could find out that the SiON HM has bigger defect diameter size than that of SiO_x. The diameter size of ESD defect is 10 to 20 um. In the case of SiO_x HM, the diameter size of ESD defect is ~1 um. In spite of different material components, the depth of ESD defect is always 50nm, which is the thickness of Cr layer. Especially, we could not observe any ESD defect below 400 rpm in the case of SiO_x material component

Using the diameter size and depth of each defect, we could make a capacitor model for explaining ESD mechanism on Cr surface. In Figure 8, the capacitor model consists of two parts of circular metal plate. From the capacitor model, we calculate the experimental dielectric permittivities of SiO_x and SiON and the values are shown in Table 1.

4. Conclusion

We checked that the probability of ESD defect was related to the hard mask process and hard mask components. We also set up a capacitor model to explain ESD defect mechanism for SiO_x and SiON. We could find that the dielectric permittivity of SiON is 2 or 3 times bigger than that of SiO_x. It implies that SiON HM is a bigger charge capacitor than SiO_x HM. We suggested the effective method for reducing (or removal) ESD defect on HM-PSM blanks. The methods for preventing charge accumulation on the HM (SiO_x) and charge dissipation are to change the component (SiON → SiO_x), to reduce mask rotation speed (800 rpm → 400 rpm), and to increase the thickness of HM for reducing the capacitance of blank itself.

5. References

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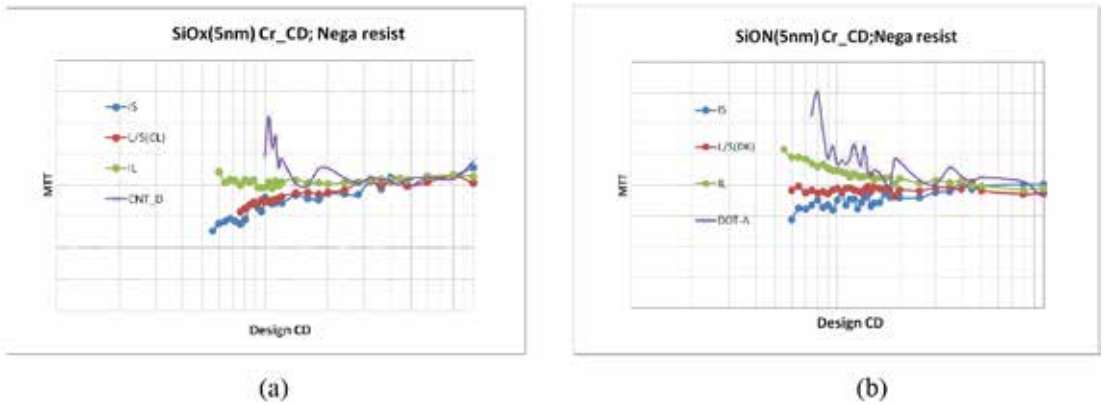

Figure 6. Linearity patterns printing comparison results at hard mask (a) SiOx and (b)SiON.

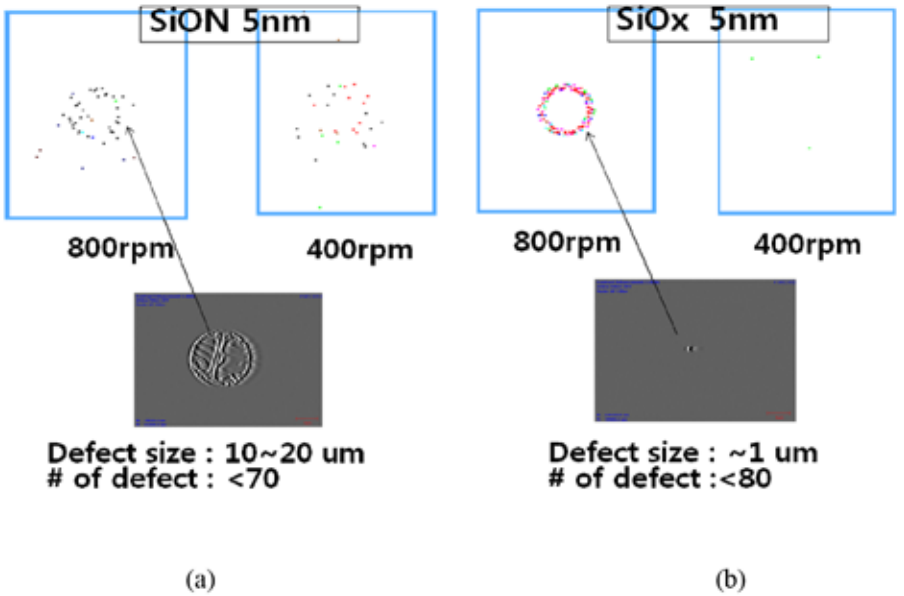

Figure 7. ESD defect size and its generation probability with changing blank rotation speed (400, 800 rpm) at HM compositions (a) SiON and (b) SiOx.

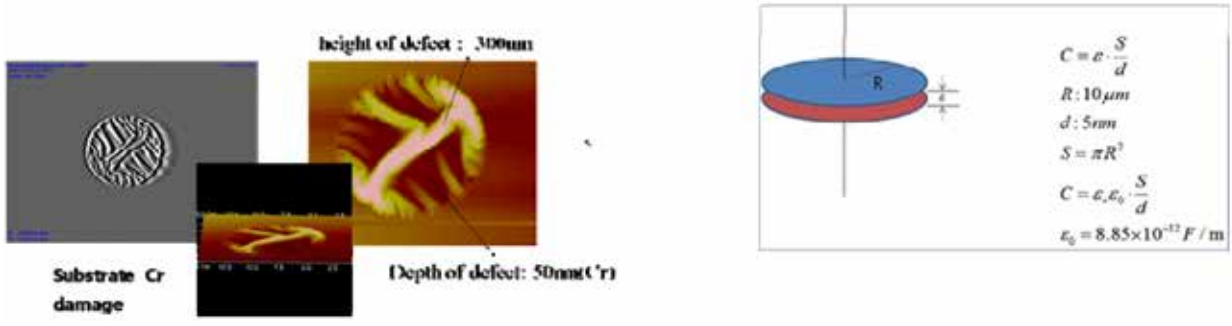

Figure 8. Capacitor model to explain the ESD mechanism on the HM-PSM structure.

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Industry Briefs

N6868 - Molecular Imprints' Semiconductor Business to be Acquired by Canon

By **Dr. Oliver Kienzle**

Molecular Imprints Inc., a market and technology provider for nanopatterning systems and solutions, announced it has signed an agreement to sell its semiconductor imprint lithography equipment business to Canon Inc. of Tokyo, Japan.

According to a release, Canon currently manufactures and markets KrF excimer and i-line illumination optical lithography platforms. Canon began conducting research into nanoimprint technology in 2004 to enter the market for lithography equipment for leading-edge high-resolution patterning. Since 2009, the Company has been carrying out joint development with MII and a major semiconductor manufacturer for mass production using MII's Jet and Flash Imprint Lithography technology.

"After establishing a business alliance with Canon four years ago to provide a technologically enabled low cost nanolithography solution to the semiconductor industry, I'm very pleased to acknowledge the tremendous progress we have achieved in the pursuit of this goal. Based on this success, the merger was a natural next step for our companies," stated Mark Melliar-Smith, CEO of Molecular Imprints.

Semiconductor Industry Posts Record Sales in 2013

The Semiconductor Industry Association (SIA), representing U.S. leadership in semiconductor manufacturing and design, announced that worldwide semiconductor sales for 2013 reached $305.6 billion, the industry's highest-ever annual total and an increase of 4.8 percent from the 2012 total of $291.6 billion. Global sales for the month of December 2013 reached $26.6 billion, marking the strongest December on record, while December sales in the Americas increased 17.3 percent year-over-year. Fourth quarter global sales of $79.9 billion were 7.7 percent higher than the total of $74.2 billion from the fourth quarter of 2012. Total sales for the year narrowly exceeded expectations from the World Semiconductor Trade Statistics (WSTS) organization's industry forecast. All monthly sales numbers are compiled by WSTS and represent a three-month moving average.

"The global semiconductor industry exceeded $300 billion in sales for the first time ever in 2013, spurred by consistent, steady growth across nearly all regions and product categories," said Brian Toohey, president and CEO, Semiconductor Industry Association. "The industry finished the year on a strong note with its best December on record, indicating that recent momentum is likely to carry over into 2014."

Intel, TSMC Revive EUV Hopes

By **Rick Merritt**

In separate talks, Intel and TSMC revealed two new efforts that are rekindling hopes for extreme ultraviolet lithography. EUV has long been seen as one of the most promising tools to ease the mounting complexity of making a future generation of smaller, faster chips.

Intel and TSMC want to use the ultra-fine patterning systems to make their generation of 7 and 10 nanometer chips starting in about 2017. But such aspirations have been dashed many times: EUV was originally targeted at use as early as 2007.

Making chips is "becoming a game of accounting for every nanometer, and that's not possible without a rigorous and mathematically sound approach," said Mark C. Phillips, head lithography engineer for Intel, in an interview with EE Times.

At the SPIE Lithography conference here, Phillips disclosed a new analysis tool under development at ASML for handling edge placement errors in next-generation chips, a growing problem with multiple causes. Just one aspect of the new modeling tool "takes about 10 pages of math to explain," said Phillips who asked ASML to start working on the concept after a meeting last year.

The new modeling tool could be key for so-called complementary lithography, a hybrid approach using existing immersion systems for some jobs and new EUV systems for others, Phillips told us (see chart below). The approach requires using increasingly strict design rules and putting wafers through litho systems multiple times.

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Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

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