Photomask Technology

Conferences + Courses: 17–21 September 2007
Exhibition: 18–19 September 2007

Monterey Marriott and Monterey Conference Center
Monterey, California USA

Technical Program

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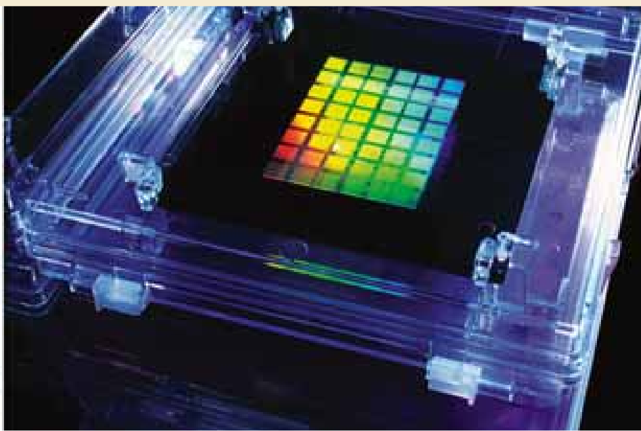

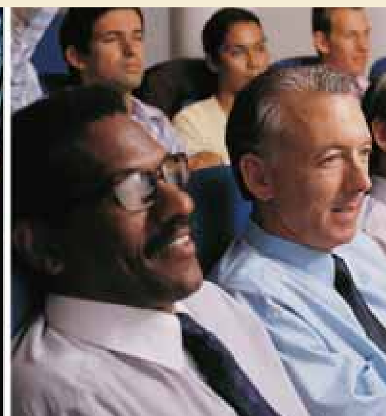

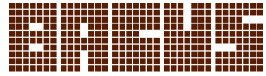

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THE EDA TECHNOLOGY LEADER

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Welcome

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Left cover photo: Courtesy of International Business Machines Corporation. Unauthorized use not permitted. IBM's mask technology center in Burlington, Vermont, develops and manufactures all the masks for the company's 300-millimeter and 200- millimeter wafer fabricators. Masks are used to "print" chip circuitry on wafers in a process similar to photography.

Center cover photo: Courtesy of AMTC.

Welcome to Photomask 2007!

On behalf of SPIE, the Sponsors, and the organizing committee, we would like to welcome you to "The 27th Annual SPIE/BACUS Symposium on Photomask", which is the premier worldwide technical conference and exhibition for the photomask industry. This year's five-day Symposium is held from Monday 17 September through Friday 21 September. The Short Course program on Monday will give you the chance to engage with the most up-to-date research on emerging and on-going issues facing the photomask industry in advanced lithography and their manufacturing and data solutions. The technical conference is scheduled from Tuesday through Friday. With the deep sub-wavelength era upon us, the industry's progress will depend on the successful integration and optimization of design, maskmaking, and wafer fabrication. Based on the success of last years special session on "DFM : Are we there yet?", submissions this year warranted a special track on DFM .

The conference will be opened on Tuesday by Rick Wallace, CEO of KLA-Tencor, speaking on the "Collaboration, Innovation, and Execution: Three Keys to Premium Customer Experience". Over the past 18 years, he has held a number of senior management positions within the company. This will provide valuable insight into the changes and challenges that could alter the industry as we know it. Do not miss it!

This year, the conference received over 216 presentation submissions (new record) and we will continue to run full parallel sessions on all 3 days to give you 124 oral presentations compared to 100 in Photomask 2006! The increase in oral presentations is the result of more submissions and changing to the typical presentation length of 20 minutes. This quickens the pace of the conference, allows you to see more of the papers during the sessions, and also better enables you to see the poster session in its entirety.

Tuesday and Wednesday the exhibition will be open. Please stop in and see what's new from the folks that are the backbone of the photomask industry. Without their active participation and support, it would be very difficult to manufacture a photomask.

Closing out the Photomask week on Friday, is the increasingly popular and valuable, overview of the key issues facing the industry. This year's special session is on "Double Patterning Lithography: Challenges and Approaches to Implementation-Twice the Pain for Twice the Gain", will follow previous year's format by addressing the hottest technical issues, development barriers, and potential roadblocks in the form of a review workshop. We have an outstanding series of topics and speakers lined up for this session. Talks are given by IDMs, academia, tool vendors, EDA vendors and state of the art mask shops in world wide. If you are thinking of leaving early, you will miss one of the highlights of the conference. Check the list of invited speakers in the program to see what we mean.

We challenge you to do four things while you are in Monterey... attend and participate in the technical sessions (challenge the authors, question assumptions, and raise the technical sessions to the next level), visit the exhibitions and most of all... have fun surrounded by state-of-the-art technologies and great sea mammals, and let us know your ideas for Photomask 2008!

Robert J. Naber,
Cadence Design Systems, Inc
2008 Conference Chair

Hiriochi Kawahira,
Sony Corp. (Japan)
2008 Conference Co-Chair

Daily Schedule

Monday 17 September	Tuesday 18 September	Wednesday 19 September	Thursday 20 September	Friday 21 September
Professional Development	**Conference**			
SC856 **Computational Lithography** *(Mansfield)* 8:30 am to 12:30 pm, $280 / $325, p. 18	6730 **Photomask Technology** *(Naber, Kawahira)* p. 8–p. 16			**Special Session Double Patterning Lithography,** p. 16
SC855 **Introduction to Design for Manufacturability** *(Liebmann)* 1:30 to 5:30 pm, $280 / $325, p. 18	**Poster Viewing** 6:00 to 7:30 pm	**Poster Viewing** 10:00 am to 3:00 pm		
SC854 **Nanoscale Metrology - Theory and Practice** *(Potzick, Grenon)* 1:30 to 5:30 pm, $280 / $325, p. 18	**Exhibition** Tuesday, 18 Sept. . . . . 10:00 am to 4:00 pm; 6 to 7:30 pm	**Exhibition** Wednesday, 19 Sept. . . . . . . 10:00 am to 4:00 pm		
SC540 **Applying Optical Proximity Correction and Design for Manufacturability to Product Designs** *(Capodieci, Lucas)* 8:30 am to 5:30 pm, $460 / $545, p. 19				
SC579 **Photomask Fabrication and Technology Basics** *(Duff)* 8:30 am to 5:30 pm, $460 / $545, p. 19				
SC723 **The Limits of Optical Lithography** *(Pierrat)* 8:30 am to 12:30 pm, $280 / $325, p. 21			**Banquet & Entertainment Program** 6:00 to 9:30 pm *See p. 5*	
SC724 **Optical Lithography Extension: Design for Manufacturing and New Resolution Enhancement Techniques** *(Pierrat)* 1:30 to 5:30 pm, $280 / $325, p. 21				

Keynote Presentation

Rick P. Wallace, CEO
KLA-Tencor Corp.

Tuesday 8:10 to 8:50 am
Room: Steinbeck Forum

"Collaboration, Innovation, and Execution: Three Keys to Premium Customer Experience"

Rick Wallace was appointed CEO of KLA-Tencor last January. Over the past 18 years, he has held a number of senior management positions within the company, including president and COO; executive vice president, overseeing the company's Reticle and Photomask Inspection Division, and Films and Surface Technology Division; CTO of the Software and Customer Groups; and executive vice president of the Wafer Inspection Group. He has served as group vice president for the Lithography Control Group, as well as vice president/general manager and vice president of marketing for the Wafer Inspection Division. Wallace joined KLA-Tencor in 1988 as an applications engineer. Earlier, he built his expertise in lithography and yield management through engineering positions with Ultratech Stepper and Cypress Semiconductor. He has a BSEE from the University of Michigan and a master's degree in engineering management from Santa Clara University. KLA-Tencor (San Jose) is a leader in yield management and process control solutions for semiconductor manufacturing and related industries.

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Entertainment

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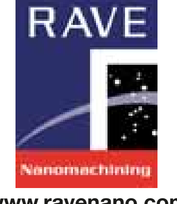
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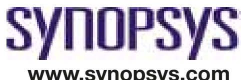
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Floor Plans

Marriott Floorplan

Santa Barbara
Los Angeles
San Francisco
Level 2
Santa Monica
San Diego
San Carlos I
San Carlos II
San Carlos Ballroom III
San Carlos Foyer
San Carlos Ballroom IV
Covered bridge to the Conference Center

Monterey Conference Center Floorplan

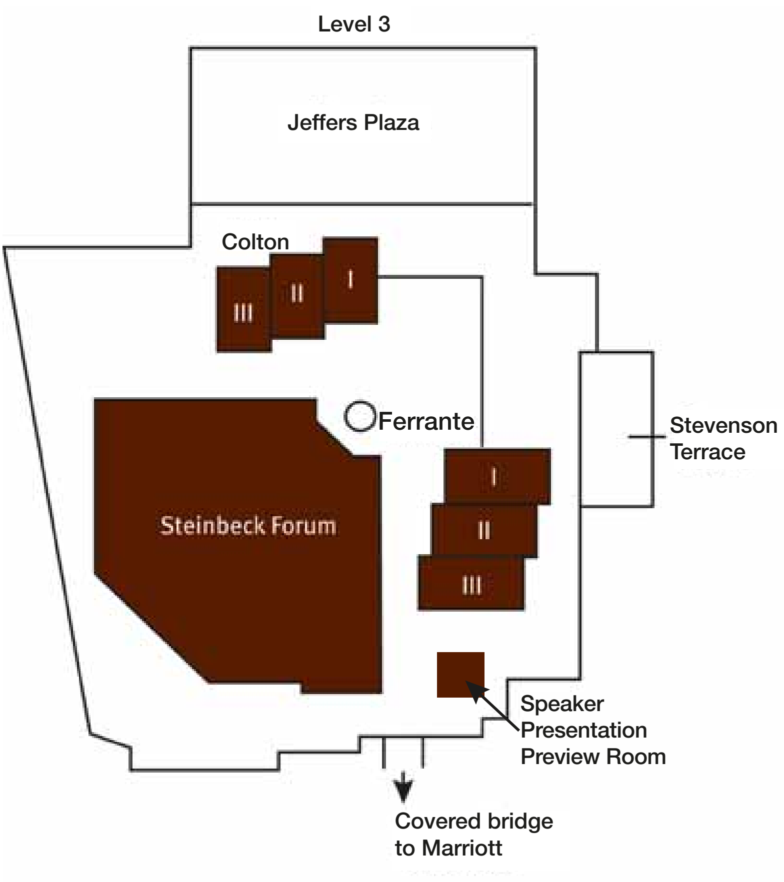
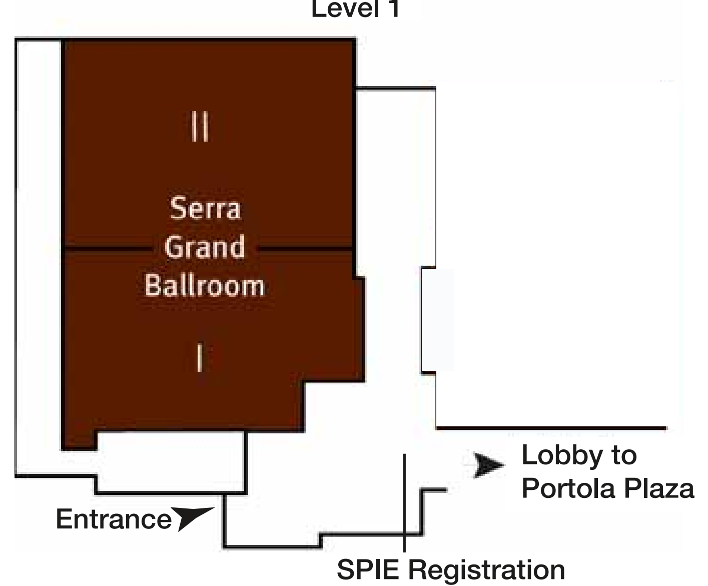


Exhibit Hall



Meet us at the Banquet!

Thursday 20 September, 6:00 to 9:30 pm
Serra Grand Ballroom

- **Reception**
  6 to 7 pm
- **Banquet**
  7 to 8:30 pm
- **Entertainment Program**
  8:30 to 9:30 pm

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Talk to the top vendors in:

- **mask infrastructure**
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- **emerging mask technology**
- **mask business**

Exhibition Hours:

Tuesday .... 10:00 am to 4:00 pm
6:00 to 7:30 pm

Wednesday .... 10:00 am to 4:00 pm

Find detailed exhibitor information in the Exhibition Guide available onsite or visit **spie.org/pmexhibit** for full exhibitor listing.

Conference 6730 • Room: Steinbeck Forum

Tuesday-Friday 18-21 September 2007 • Proceedings of SPIE Vol. 6730

Photomask Technology

Conference Chairs: **Robert J. Naber**, Cadence Design Systems, Inc.; **Hiroichi Kawahira**, Sony Corp. (Japan)

Program Committee: **Ki-Ho Baik**, Intel Corp.; **Artur P. Balasinski**, Cypress Semiconductor Corp.; **Uwe F. W. Behringer**, UBC Microelectronics (Germany); **Robert M. Bigwood**, Intel Corp.; **Ron R. Bozak**, RAVE LLC; **William H. Broadbent**, KLA-Tencor Corp.; **Peter D. Buck**, Toppan Photomasks, Inc.; **Jang Fung Chen**, ASML MaskTools Inc.; **HanKu Cho**, SAMSUNG Electronics Co., Ltd. (South Korea); **Frank A. J. M. Driessen**, Takumi Technology B.V. (Netherlands); **Roxann L. Engelstad**, Univ. of Wisconsin/Madison; **Benjamin G. Eynon, Jr.**, SAMSUNG; **Donis G. Flagello**, ASML US, Inc.; **Emily E. Gallagher**, IBM Microelectronics Div.; **Bernd Geh**, Carl Zeiss / ASML-TDC; **Brian J. Grenon**, Grenon Consulting, Inc.; **Woo-Sung Han**, SAMSUNG Electronics Co., Ltd. (South Korea); **Naoya Hayashi**, Dai Nippon Printing Co., Ltd. (Japan); **Alan J. Leslie**, IBM Corp.; **Chin-Hsiang Lin**, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan); **Paul F. Luehrmann, Jr.**, ASML Netherlands B.V. (Netherlands); **Patrick M. Martin**, Photronics, Inc.; **Mark E. Mason**, Texas Instruments Inc.; **Wilhelm Maurer**, Infineon Technologies AG (Germany); **Warren Montgomery**, Albany NanoTech; **Richard D. Morse**, Silicon Canvas Inc.; **Thomas H. Newman**, Micronic Laser Systems AB; **Steven D. Slonaker**, Nikon Precision Inc.; **Christopher A. Spence**, AMD Saxony LLC & Co. KG (Germany); **Wolfgang Staud**, B^{2}W Consulting; **Geert Vandenberghe**, IMEC (Belgium); **J. Tracy Weed**, Synopsys, Inc.; **Craig A. West**, Toppan Photomasks, Inc.; **Vincent Wiaux**, IMEC (Belgium)

Tuesday 18 September

Opening Remarks and Introduction . . . . 8:00 to 8:10 am

SESSION 1

Room: Steinbeck Forum . . . . Tues. 8:10 to 10:10 am

Invited Session

Chairs: **Robert J. Naber**, Cadence Design Systems, Inc.; **Hiroichi Kawahira**, Sony Corp. (Japan)

Keynote

8:10 am: **Collaboration, Innovation, and Execution: Three Keys to Premium Customer Experience,** R. P. Wallace, KLA-Tencor Corp. . . . . [6730-01]

8:50 am: **Mask Industry Assessment: 2007,** G. V. Shelden, Shelden Consulting; P. Marmillion, SEMATECH, Inc. . . . . [6730-02]

9:10 am: **EMCL 2007 Best Paper: Predicting and correcting for image placement errors during the fabrication of EUVL masks,** R. L. Engelstad, K. T. Turner, J. Sohn, A. R. Mikkelson, M. Nataraju, Univ. of Wisconsin/Madison . . . . [6730-03]

9:30 am: **PMJ 2007 Best Paper: Alternating phase-shift mask and binary mask for 45-nm node and beyond: the impact on the mask error control,** Y. Kojima, M. Shirasaki, K. Chiba, Toppan Printing Co., Ltd. (Japan); T. Tanaka, Toppan Printing Co., Ltd.; K. Iwase, Sony Atsugi Technology Ctr. (Japan); K. Ishikawa, Sony Corp. (Japan); K. Ozawa, Sony Atsugi Technology Ctr. (Japan); Y. Inazuki, H. Yoshikawa, S. Okazaki, Shin-Etsu Chemical Co., Ltd. (Japan) . . . . [6730-04]

9:50 am: **PMJ Panel Discussion Overview: double exposure and double patterning for 32-nm half-pitch design node,** Y. Nagaoka, KLA-Tencor Japan Ltd. (Japan); H. Watanabe, Toshiba Semiconductor Co. (Japan) . . . . [6730-05]

Coffee Break . . . . 10:10 to 10:40 am

Sessions 2-3-4-5 run concurrently with sessions 6-7-8.

SESSION 2

Room: Steinbeck Forum . . . . Tues. 10:40 am to 12:00 pm

Etch

Chairs: **Kiho Baik**, Intel Corp.; **Patrick M. Martin**, Photronics, Inc.; **Warren M. Montgomery**, Albany NanoTech

10:40 am: **Characterizing photomask etch processes through phase component analysis,** R. E. Wistrom, IBM Corp.; M. S. Hibbs, IBM Microelectronics Div.; T. Komizo, Toppan Electronics, Inc.; G. Reid, IBM Corp. . . . . [6730-06]

11:00 am: **The advanced mask CD MTT control using dry etch process for sub-65-nm technology,** S. J. Jo, H. Y. Jung, D. W. Lee, J. Y. Jun, T. Ha, O. Han, Hynix Semiconductor Inc. (South Korea) . . . . [6730-07]

11:20 am: **Hardmask etch process for next-generation photomask fabrication beyond 32-nm technology node,** P. Qu, C. Choi, K. Baik, S. Park, Intel Corp. . . . . [6730-08]

11:40 am: **CD bias control with in-situ plasma treatment in EPSM photomask etch,** K. Yung, C. Choi, K. Baik, Intel Corp. . . . . [6730-09]

Lunch/Exhibition Break . . . . 12:00 to 1:15 pm

SESSION 6

Room: Ferrante . . . . Tues. 11:00 am to 12:20 pm

DFM 1: Masks and Manufacturability

Chairs: **Robert M. Bigwood**, Intel Corp.; **Artur P. Balasinski**, Cypress Semiconductor Corp.; **Han-Ku Cho**, SAMSUNG Electronics Co., Ltd. (South Korea)

11:00 am: **New method of contour-based mask-shape compiler,** R. Matsuoka, H. Sato, Hitachi High-Technologies Corp. (Japan) . . . . . . [6730-21]

11:20 am: **Development of mask-DFM system MiLE: load estimation of mask manufacturing,** Y. Nagamura, K. Hosono, Renesas Technology Corp. (Japan); S. Narukawa, H. Mohri, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan) . . . . [6730-23]

11:40 am: **DFM: design-aware flexible mask-defect analysis,** F. A. J. M. Driessen, Takumi Technology B.V.; J. Westra, M. Scheffer, Takumi Technology B.V. (Netherlands); K. Kawakami, Takumi Technology KK (Japan); E. Tsujimoto, M. Yamaji, T. Kawashima, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan) . . . . [6730-24]

12:00 pm: **Use of layout automation and design-based metrology for defect test mask design and verification,** C. E. Tabery, C. A. Spence, Advanced Micro Devices, Inc.; A. Poock, Advanced Micro Devices, Inc. (Germany); A. C. Dürr, Advanced Mask Technology Ctr. (Germany) . . [6730-25]

Lunch/Exhibition Break . . . . 12:20 to 1:35 pm

Tuesday 18 September

Sessions 2-3-4-5 run concurrently with sessions 6-7-8 *(continued).*

SESSION 3

Room: Steinbeck Forum . . . . Tues. 1:15 to 2:15 pm

Substrate

Chairs: **Uwe F. W. Behringer**, UBC Microelectronics (Germany); **Roxann L. Engelstad**, Univ. of Wisconsin/Madison; **Benjamin G. Eynon, Jr.**, SAMSUNG

1:15 pm: **Effects of exposure environment on pellicle degradation in ArF lithography,** H. Choi, Y. Ahn, J. Ryu, Y. Lee, Y. Cho, J. Kim, SAMSUNG Electronics Co., Ltd. (South Korea) . . . . [6730-10]

1:35 pm: **Development and characterization of a new low-stress molybdenum silicide absorber for 45-nm attenuated phase-shift mask manufacturing,** T. B. Faure, E. E. Gallagher, IBM Corp.; L. M. Kindt, IBM Microelectronics Div.; S. C. Nash, K. C. Racette, R. E. Wistrom, IBM Corp.; T. Komizo, Toppan Electronics, Inc.; Y. Kikuchi, IBM Burlington; S. Nemoto, Toppan Electronics, Inc.; Y. Sasaki, Toppan Printing Co., Ltd. (Japan); T. Suzuki, M. Ushida, Y. Yokoya, HOYA Corp. (Japan) . . . . [6730-11]

1:55 pm: **Evaluation of the effect of mask-blank flatness on CDU and DOF in high-NA system,** C. W. Chang, Nanya Technology Corp. . . . . [6730-12]

SESSION 4

Room: Steinbeck Forum . . . . Tues. 2:15 to 3:15 pm

Imprint

Chairs: **Naoya Hayashi**, Dai Nippon Printing Co., Ltd. (Japan); **Ronald R. Bozak**, RAVE LLC; **Bernd Geh**, ASML US, Inc.

2:15 pm: **The development of full-field high-resolution imprint templates,** S. Yoshitake, H. Sunaoshi, K. Yasui, NuFlare Technology, Inc. (Japan); D. J. Resnick, G. M. Schmid, E. Thompson, Molecular Imprints, Inc.; O. Nagarekawa, H. Kobayashi, T. Sato, HOYA Corp. (Japan) . . . . . . [6730-13]

2:35 pm: **Defect reduction progress in step and flash imprint lithography,** D. J. Resnick, J. G. Maltabes, I. McMackin, J. Perez, K. S. Selinidis, S. V. Sreenivasan, Molecular Imprints, Inc. . . . . [6730-14]

2:55 pm: **Fabrication of nano-imprint templates for dual-Damascene applications using a high-resolution variable shape e-beam writer,** M. Pritschow, J. Butschke, M. Irmscher, H. Sailer, Institut für Mikroelektronik Stuttgart (Germany); D. J. Resnick, E. Thompson, Molecular Imprints, Inc. . . . . [6730-15]

Coffee Break . . . . 3:15 to 3:45 pm

SESSION 5

Room: Steinbeck Forum . . . . Tues. 3:45 to 5:25 pm

Resist

Chairs: **Kiho Baik**, Intel Corp.; **Peter D. Buck**, Toppan Photomasks, Inc.; **Warren M. Montgomery**, Albany NanoTech

3:45 pm: **The study of CD error in mid-local pattern area caused by develop loading effect,** M. Kang, SAMSUNG Electronics Co., Ltd. (South Korea) . . . . [6730-16]

4:05 pm: **Performance improvement of ALTA4700 for 130-nm and below mask productivity,** J. Hsu, D. Lee, C. Tseng, E. Hong, C. Wu, Taiwan Mask Corp. (Taiwan) . . . . [6730-17]

4:25 pm: **The behavior of substrate dependency as surface treatment in the positive chemically amplified resist coated blanks,** S. Yang, S&S TECH (South Korea); H. Cha, Hanyang Univ. (South Korea); C. Yang, J. Kang, S&S TECH (South Korea); J. Ahn, Hanyang Univ. (South Korea); K. Nam, S&S TECH (South Korea) . . . . [6730-18]

4:45 pm: **Design for CD correction strategy using a resist shrink method via UV irradiation for defect-free photomask,** J. Ryu, D. W. Lee, H. Y. Jung, S. P. Kim, O. Han, Hynix Semiconductor Inc. (South Korea) . . . . [6730-19]

5:05 pm: **The impact of mask photoresist develop on critical dimension parameters,** A. C. Smith, D. B. Sullivan, IBM Corp.; K. Sugawara, Y. Okawa, Toppan Electronics, Inc. . . . . [6730-20]

SESSION 7

Room: Ferrante . . . . Tues. 1:35 to 3:15 pm

DFM 2: Manufacturing Models and Physical Design

Chairs: **Robert M. Bigwood**, Intel Corp.; **Mark E. Mason**, Texas Instruments Inc.; **Wilhelm Maurer**, Infineon Technologies AG (Germany)

1:35 pm: **Intel's AMT enables rapid processing and info-turn for Intel's DFM test chip vehicle,** H. M. Hajj, K. M. Srinivasan, Intel Corp. . . . [6730-26]

1:55 pm: **From rule to model-based design: a need for DfP criteria ?,** A. P. Balasinski, Cypress Semiconductor Corp.; N. Kachwala, D. A. Abercrombie, Mentor Graphics Corp. . . . . [6730-27]

2:15 pm: **Accurate lithography analysis for yield prediction,** G. M. Yeric, B. H. Hatamian, R. Kapoor, Synopsys, Inc. . . . . [6730-28]

2:35 pm: **Production-worthy full-chip image-based verification,** Z. Yu, W. Li, Y. Zhang, Brion Technologies, Inc. . . . . [6730-29]

2:55 pm: **Layout verification in the era of process uncertainty: requirements for speed, accuracy, and process portability,** J. A. Torres, Mentor Graphics Corp. . . . . [6730-30]

Coffee Break . . . . 3:15 to 3:45 pm

SESSION 8

Room: Ferrante . . . . Tues. 3:45 to 5:45 pm

DFM 3: Modal Aware Design and Optimization

Chairs: **Artur P. Balasinski**, Cypress Semiconductor Corp.; **Richard D. Morse**, Silicon Canvas Inc.; **Frank A. J. M. Driessen**, Takumi Technology B.V. (Netherlands)

3:45 pm: **A lithography aware design migration using foundry certified models and hotspot detection,** L. N. Karklin, A. Arkhipov, C. Decoin, C. Zelnik, Sagantec North America; M. L. Cote, P. Hurat, Clear Shape Technologies, Inc. . . . . [6730-36]

4:05 pm: **Litho-aware extraction for the 32-nm double-patterning node,** J. A. Huckabay, Q. Chen, C. S. Thayer, R. J. Naber, Cadence Design Systems, Inc. . . . . [6730-32]

4:25 pm: **Silicon-verified automatic DFM layout optimization: a calibration-lite model-based application to standard cells,** K. Lin, B. P. Wong, Chartered Semiconductor Manufacturing, Inc.; F. A. J. M. Driessen, Takumi Technology Corp. (Netherlands); E. Morita, Takumi Technology Corp. [6730-33]

4:45 pm: **Non-uniform yield optimization for integrated circuit layout,** F. G. Pikus, J. A. Torres, Mentor Graphics Corp. . . . . [6730-34]

5:05 pm: **Model-based DFM compilation for standard cell libraries,** D. Yang, Semiconductor Manufacturing International Corp. (China); G. Shou, SMIC Americas; R. Chen, Semiconductor Manufacturing International Corp. (China); Q. Qian, IC Scope Research . . . . [6730-35]

5:25 pm: **Selecting and using a lithography compliance DFM tool for 65-nm foundry production,** R. Kapoor, Synopsys, Inc. . . . . [6730-31]

Posters-Tuesday

Chairs: **Wolfgang Staud**, B²W Consulting; **Hiroichi Kawahira**, Sony Corp. (Japan)

Exhibition/Poster Reception • *Monterey Conference Center, Serra Grand Ballroom* **• Tuesday, 18 September, 6 to 7:30 pm**

Symposium attendees and guests are invited to attend an Exhibition/Poster Reception on Tuesday evening in the Serra Grand Ballroom. The reception provides an opportunity for attendees to meet colleagues, network, and view poster papers. Refreshments will be served. Attendees are requested to wear their conference registration badges.

Poster Viewing
Tuesday 18 September, 6 to 7:30 pm • Wednesday 19 September, 10 am to 3 pm

Poster authors may set up their poster papers between 10 am and 4 pm on Tuesday and will leave them up until Wednesday afternoon. Authors will be present during the Poster Reception 6 to 7:30 pm Tuesday to answer questions and provide in-depth discussion regarding their papers. Any papers not removed by Wednesday at 3 pm will be considered unwanted and will be discarded. SPIE assumes no responsibility for papers left up after Wednesday at 3 pm.

PS1: Inspection

New method of identification of fault defect using defect imaging system, H. Zhang, Holon Co., Ltd. (Japan) . . . . [6730-124]

Study of mask defect inspection optics for hp 45-nm node device and beyond, R. Hirano, K. Takahara, M. Hirono, R. Ogawa, S. Murakami, N. Kikuiri, Advanced Mask Inspection Technology, Inc. (Japan) . . . . [6730-125]

Improving inspectability with KLA TeraScan Thin Line De-sense, C. Chen, D. H. Kim, KLA-Tencor Corp.; K. H. Park, N. Kim, KLA-Tencor Corp. (South Korea); S. Lohekare, KLA-Tencor Corp.; S. Han, J. H. Park, D. H. Chung, SAMSUNG Electronics Co., Ltd. (South Korea) . . . . . [6730-126]

Improvement in defect classification efficiency and useable sensitivity by grouping disposition for reticle inspection, S. Liu, E. H. Lu, KLA-Tencor Corp. . . . . [6730-127]

Improvement in soft defect classification efficiency by grouping disposition for wafer fab reticle re-qual inspection, P. P. Yu, E. H. Lu, KLA-Tencor Corp. . . . . [6730-128]

Enhancing productivity and sensitivity in mask production via a fast integrated T+R inspection on critical layers, P. P. Yu, E. H. Lu, KLA-Tencor Corp. . . . . [6730-129]

ADAS: integrated mask defect analysis for disposition and process control in mask shops and wafer fabs, P. J. Fiekowsky, AVI-Automated Visual Inspection; S. Narukawa, T. Kawashima, Dai Nippon Printing Co., Ltd. (Japan) [6730-130]

PS2: DFM: Design for Manufacturability

Automatic OPC repair flow: optimized implementation of the repair recipe, M. S. Bahnas, M. Al-Imam, Mentor Graphics Corp. (Egypt); J. C. Word, Mentor Graphics Corp. . . . . [6730-132]

Database and data analysis strategy for multidesigner testchips, W. J. Poppe, A. R. Neureuther, Univ. of California/Berkeley . . . . [6730-133]

Router-driven automated correction of lithography hotspots, D. N. Zhang, S. Tong, L. Wen, F. W. Tseng, A. Miloslavsky, K. Kwang, Z. Tang, Synopsys, Inc. . [6730-134]

Assessment of 2D OPC target specifications using electrical testable structures, Q. Zhang, P. J. M. VanAdrichem, Synopsys, Inc. . . . . . [6730-135]

Lateral interactions between standard cells using pattern matching, L. T. Wang, A. R. Neureuther, Univ. of California/Berkeley . . . . [6730-136]

Application of modified jog-filled DRC method on lithography friendly OPC flow, Y. Kim, S. Lee, J. Kang, J. Kim, K. Kim, Dongbu Electronics Co., Ltd. (South Korea) . . . . [6730-137]

PS3: Substrate and Materials

Measurement and experimentation about correlation of pellicle's life time, S. Park, Y. Kang, H. Oh, Hanyang Univ. (South Korea) . . . . [6730-138]

Pellicle dimensions for high-NA photomasks, F. Erber, T. Schulmeier, C. Holfeld, Advanced Mask Technology Ctr. (Germany) . . . . [6730-139]

Evaluation of attenuated-PSM photomask blanks with TF11 chrome and FEP-171 resist on a 248-nm DUV laser pattern generator, K. Xing, C. Bjornborg, H. Karlsson, A. Paulsson, A. Rosendahl, P. Beiming, J. Walford, J. Vedenpää, P. Hogfeldt, Micronic Laser Systems AB (Sweden) . . [6730-140]

PS4: Resist Process and Etch

Bimetallic thermal resists potential for double-exposure immersion lithography and grayscale photomasks, J. M. Dykes, G. H. Chapman, D. K. Poon, Simon Fraser Univ. (Canada) . . . . [6730-141]

A dynamical model of drying process of polymer-blend solution coated on a flat substrate, H. Kagami, Nagoya College (Japan) . . . . [6730-142]

Investigation of limit diffusion length limitation for 45-nm node attenuated and chromeless phase-shift mask, Y. Kang, S. Park, H. Oh, Hanyang Univ. (South Korea) . . . . [6730-143]

Critical dimension control for 50-nm random contact hole array with resist reflow process, J. M. Park, Y. Kang, H. Oh, Hanyang Univ. (South Korea) . . . . [6730-144]

Self-aligned resist patterning with 172-nm and 193-nm backside flood exposure on attenuated phase-shift masks, J. Chun, T. Ha, H. Y. Jung, S. J. Jo, O. Han, Hynix Semiconductor Inc. (South Korea) . . . . [6730-145]

Practical use of hard mask process to fabricate fine photomasks for 45-nm node and beyond, Y. Kushida, H. Handa, H. Maruyama, Fujitsu Ltd. (Japan); Y. Abe, Y. Fujimura, T. Yokoyama, Dai Nippon Printing Co., Ltd. (Japan)[6730-147]

Ovecoming loading challenges in a mask etcher for 45 nm and beyond, M. Chandrachood, T. Y. B. Leung, K. Yu, M. N. Grimbergen, S. J. Panayil, I. M. Ibrahim, A. Sabharwal, A. Kumar, Applied Materials, Inc. . . . . [6730-213]

PS5: Patterning

Resistless mask structuring using an ion multibeam projection pattern generator, J. Butschke, M. Irmscher, F. Letzkus, Institut für Mikroelektronik Stuttgart (Germany); H. Löschner, IMS Nanofabrication AG (Austria); L. Nedelmann, Institut für Mikroelektronik Stuttgart (Germany); E. Platzgummer, IMS Nanofabrication AG (Austria) . . . . [6730-148]

Reconfigurable lithographic applications using polymer liquid-crystal composite films, A. E. Fox, A. K. Fontecchio, Drexel Univ. . . . . . [6730-149]

Laser micromachining of wide band-gap materials for photomask applications, A. A. Tseng, National Taiwan Univ. of Science and Technology (Taiwan) . . . . [6730-150]

Pattern density and process related CD corrections at 32-nm node, Z. Benes, IBM Corp.; J. Kotani, Toppan Electronics, Inc. . . . . [6730-151]

PS6: Extreme NA/Immersion Lithography

Pattern split rules!: feasibility study of rule-based pitch decomposition for double patterning, A. van Oosten, P. Nikolsky, ASML Netherlands B.V. (Netherlands); J. A. Huckabay, Cadence Design Systems, Inc.; J. Park, Brion Technologies, Inc. . . . . [6730-152]

Automatic residue removal for high-NA extreme illumination, J. Moon, B. Nam, J. Jeong, D. Kong, B. M. Nam, D. G. Yim, Hynix Semiconductor Inc. (South Korea) . . . . [6730-153]

PS7: MDP/MRC

Effective area partitioning for preparing a distributed parallel processing in mask data preparation, Y. Satou, A. Satou, H. Tsuchida, Y. Okamoto, Tool Corp. (Japan) . . . . [6730-154]

Compressing MEBES data enabling multithreaded decompression, M. Pereira, A. Parchuri, SoftJin Technologies Pvt. Ltd. (India) . . . . . [6730-155]

Mask calibration dominated methodology for OPC matching, L. Zhu, Shanghai Institute of Microsystem And Information Technology (China) and Graduate School of Chinese Academy of Science (China) and Grace Semiconductor Manufacturing Corp. (China); M. Lu, D. King, Y. Gu, S. Yang, Grace Semiconductor Manufacturing Corp. (China); L. S. Melvin III, Synopsys, Inc. . . . . [6730-156]

Integration of OPC and mask data preparation for reduced data I/O and reduced cycle time, J. Yu, R. E. Morgan, Synopsys, Inc. . . . . [6730-157]

Mask rule check using priority information of mask patterns, K. Kato, SII NanoTechnology Inc. (Japan) . . . . [6730-158]

Improving the efficiency of pattern extraction for character projection lithography using OPC optimization, H. Nosato, National Institute of Advanced Industrial Science and Technology (Japan); T. Matsunawa, Univ. of Tsukuba (Japan); H. Sakanashi, M. Murakawa, National Institute of Advanced Industrial Science and Technology (Japan); T. Higuchi, National Institute of Advanced Industrial Science and Technology (Japan) and Univ. of Tsukuba (Japan) . . . . [6730-159]

A user-programmable link between data preparation and mask manufacturing equipment, W. Zhang, E. Y. Sahouria, S. F. Schulze, G. Davis, Mentor Graphics Corp.; A. Seyfarth, Carl Zeiss SMS GmbH (Germany); E. R. Poortinga, Carl Zeiss SMT Inc. . . . . [6730-160]

Posters-Tuesday

Chairs: **Wolfgang Staud**, B²W Consulting; **Hiroichi Kawahira**, Sony Corp. (Japan)

PS8: Simulation

32-nm half-pitch node OPC process model development for three-dimensional mask effects using rigorous simulation, L. S. Melvin III, Synopsys, Inc. . . . . [6730-161]

OPC verification on cell level using fully rigorous mask topography simulation, V. Domnenko, T. Klimpel, H. Koop, Synopsys, Inc. (Germany); L. S. Melvin III, Synopsys, Inc.; T. Schmoeller, Synopsys, Inc. (Germany) . [6730-162]

EMF simulations of isolated and periodic 3D photomask patterns, S. Burger, L. W. Zschiedrich, F. Schmidt, Zuse Institute Berlin (Germany); R. Koehle, Qimonda AG (Germany); B. Küchler, C. Nölscher, Qimonda Dresden GmbH & Co. OHG (Germany) . . . . . [6730-163]

PS9: Cleaning

The study of haze generation as thin film materials, J. Kang, S&S TECH (South Korea); H. Cha, Hanyang Univ. (South Korea); S. Yang, C. Yang, S&S TECH (South Korea); J. Ahn, Hanyang Univ. (South Korea); K. Nam, S&S TECH (South Korea); J. Kim, S. Choi, PKL Co., Ltd. (South Korea) . . . . . [6730-43]

A method to determine the origin of remaining particles after mask blank cleaning, V. Kapila, A. Rastegar, S. K. Eichenlaub, A. John, P. Marmillion, SEMATECH, Inc. . . . . . [6730-166]

Study of time dependent 193-nm reticle haze, O. P. Kishkovich, Entegris, Inc.; J. S. Gordon, L. E. Frisa, C. M. Chovino, D. Y. Chan, J. Keagy, Toppan Photomasks, Inc.; F. V. Belanger, T. Scoggins, Entegris, Inc. . . . . . [6730-168]

An approach to prevent retilce ESD damage and haze contamination, P. Lee, B. Chiu, L. Liu, A. Chiu, Gudeng Precision Industrial Co., Ltd. (Taiwan) . . . . . [6730-169]

Evaluation of photomask package and storage environment and its effect on haze generation, J. Kim, PKL Co., Ltd. (South Korea) . . . . . [6730-170]

Laser shockwave cleaning of EUV reticles, N. A. Lammers, Technische Univ. Eindhoven (Netherlands) and ASML Netherlands B.V. (Netherlands); A. J. Bleeker, ASML Netherlands B.V. (Netherlands) . . . . . [6730-171]

Mask protection from a haze, T. Umeda, Adhand, Inc. (Japan) . . [6730-172]

PS10: Metrology

Signature evaluation using scatterometry, J. Richter, Advanced Mask Technology Ctr. (Germany); J. C. Lam, n&k Technology, Inc. . . . . . [6730-173]

Parameter sensitive PSM patterns for scatterometry monitoring, J. Xue, Y. Ben, M. A. Miller, C. J. Spanos, A. R. Neureuther, Univ. of California/Berkeley . . . . . [6730-174]

Long-term critical dimension measurement performance for a new mask CD-SEM: S9380M, Z. Wang, K. K. Seet, R. Fukaya, Y. Kadowaki, N. Arai, M. Ezumi, H. Satoh, Hitachi High-Technologies Corp. (Japan) . . . . [6730-175]

Images in photoresist for self-interferometric electrical image monitors, J. A. Holwill, A. R. Neureuther, Univ. of California/Berkeley . . . . [6730-177]

Ultra-fine stage for CD-SEM, K. Takahashi, Holon Co., Ltd. (Japan) [6730-178]

The study for close correlation between mask and wafer to optimize wafer field CD uniformity, M. Kim, Y. Choi, O. Han, Hynix Semiconductor Inc. (South Korea) . . . . . [6730-179]

Development of a captured image simulator for the differential interference contrast microscopes aiming to design 199-nm mask inspection tools, M. Shiratsuchi, Y. Honguh, Toshiba Corp. (Japan); R. Hirano, R. Ogawa, M. Hirono, Advanced Mask Inspection Technology, Inc. (Japan) . . . . . [6730-180]

Mask CD control (CDC) with ultrafast laser for improving mask CDU using AIMS 45i as the CD metrology data source, E. Zait, G. Ben-Zvi, V. Dmitriev, S. Oshemkov, E. Graitzer, G. Gottlieb, Pixer Technology, Ltd. (Israel); R. Birkner, T. Scheruebl, Carl Zeiss SMS GmbH (Germany) . . . . . [6730-214]

PS11: Advanced RET

Improvements in model-based assist feature placement algorithms, B. Painter, L. D. Barnes, J. P. Mayhew, Y. Wang, Synopsys, Inc. . . . . . [6730-182]

An approach of auto-fix post-OPC hot spots, C. Wang, Q. Liu, Semiconductor Manufacturing International Corp. (China); L. Zhang, Mentor Graphics Corp. (China) . . . . . [6730-183]

Three-dimensional mask modeling with oblique incidence and mask corner rounding effects for the 32-nm node, M. Saied, Freescale Semiconductor, Inc. (France); F. Foussadier, STMicroelectronics (France); J. Belledent, NXP Semiconductors (France); Y. Trouiller, Lab. d'Electronique de Technologie de l'Information (France); I. Schanen, École Nationale Supérieure d'Electronique et de Radioélectricité de Grenoble (France); E. Yesilada, C. Gardin, Freescale Semiconductor, Inc. (France); J. Urbani, F. Sundermann, F. Robert, STMicroelectronics (France); C. Couderc, NXP Semiconductors (France); F. Vautrin, STMicroelectronics (France); L. LeCam, NXP Semiconductors (France); G. Kerrien, J. Planchot, C. Martinelli, STMicroelectronics (France); B. Wilkinson, Freescale Semiconductor, Inc. (France); Y. F. Rody, A. Borjon, NXP Semiconductors (France); N. Morgana, Freescale Semiconductor, Inc. (France); J. Di-Maria, V. Farys, STMicroelectronics (France) . . . . . [6730-184]

Model-based mask verification, F. Foussadier, F. Sundermann, STMicroelectronics (France); J. N. Wiley, A. D. Vacca, Brion Technologies, Inc.; K. Hayano, S. Narukawa, S. Kawashima, H. Mohri, N. Hayashi, H. Miyashita, Dai Nippon Printing Co., Ltd. (Japan); Y. Trouiller, Lab. d'Electronique de Technologie de l'Information (France); C. Gardin, Freescale Semiconductor, Inc. (France); J. Urbani, F. Robert, F. Vautrin, G. Kerrien, J. Planchot, STMicroelectronics (France); E. Yesilada, Freescale Semiconductor, Inc. (France); C. Martinelli, J. Di-Maria, V. Farys, STMicroelectronics (France); M. Saied, Freescale Semiconductor, Inc. (France) . . . . . [6730-185]

Inverse lithography technology (ILT): keep the balance between SRAF and MRC at 45 and 32 nm, L. Pang, Y. Liu, D. S. Abrams, Luminescent Technologies, Inc. . . . . . [6730-212]

PS12: RET/OPC

A generic technique for reducing OPC iteration: fast forward OPC, L. Hong, J. L. Sturtevant, Mentor Graphics Corp. . . . . . [6730-187]

More robust model built using SEM calibration, C. Wang, Q. Liu, Semiconductor Manufacturing International Corp. (China); L. Zhang, Mentor Graphics Corp. (China) . . . . . [6730-188]

Safe interpolation distance for VT5 resist model, M. Al-Imam, W. A. Tawfic, Mentor Graphics Corp. (Egypt); G. E. Bailey, Mentor Graphics Corp. . . . [6730-189]

The effect of the OPC setup parameters optimization on the performance of the OPC model, A. Y. Abdo, A. C. Wei, I. P. Stobert, J. M. Oberschmidt, IBM Microelectronics Div.; A. M. Seoud, Mentor Graphics Corp. (Egypt) . . . . . [6730-190]

Optical qualification of OPC simulator to ensure accurate and physics-centric OPC model, Q. Zhang, Synopsys, Inc.; J. K. Tyminski, Nikon Precision Inc.; K. D. Lucas, Synopsys, Inc. . . . . [6730-191]

Modeling polarized illumination for OPC/RET, H. Song, Q. Zhang, J. P. Shiely, Synopsys, Inc. . . . . . [6730-192]

Fundamental study on the error factor for the sub-90-nm OPC modeling, H. Lee, J. Kang, J. Kim, K. Kim, Dongbu Electronics Co., Ltd. (South Korea) . . . . . [6730-193]

OPC development in action for advanced technology nodes, P. J. M. VanAdrichem, A. C. Wang, Synopsys, Inc. . . . . . [6730-194]

A novel methodology for efficient and accurate model calibration across the entire process window, I. Y. Su, Synopsys, Inc. (Taiwan) . . . . [6730-195]

PS13: Mask Business/Management

Industry survey of wafer fab reticle control strategies in the 90-nm/45-nm design-rule age, R. J. Dover, KLA-Tencor Corp. . . . . . [6730-196]

Shuttle fabrication for designs with lifted I/Os, R. Lin, M. Wu, S. Tsai, Yuan Ze Univ. (Taiwan) . . . . . [6730-197]

PS14: EUV and Other Generation Lithography

Development status of EUVL-mask blank, K. Hayashi, Asahi Glass Co., Ltd. (Japan) . . . . . [6730-198]

Performance of actinic EUVL mask imaging using a zone-plate microscope, K. A. Goldberg, Lawrence Berkeley National Lab.; A. Barty, Lawrence Livermore National Lab.; S. B. Rekawa, C. Kemp, F. H. Salmassi, E. M. Gullikson, E. H. Anderson, V. V. Yashchuk, Lawrence Berkeley National Lab.; E. A. Ultanir, T. Liang, Intel Corp.; H. Han, SEMATECH, Inc. . . [6730-199]

The effect of size and shape of sub-50-nm defects on their detectability, A. Rastegar, W. Cho, SEMATECH, Inc.; E. M. Gullikson, Lawrence Berkeley National Lab.; S. K. Eichenlaub, SEMATECH, Inc. . . . . . [6730-200]

Force non-uniformity in electrostatic pin chucks for EUVL mask clamping, S. Veeraraghavan, J. Sohn, R. L. Engelstad, K. T. Turner, Univ. of Wisconsin/Madison . . . . . [6730-201]

A study of precision performance and scan damage of EUV masks with the LWM9000 SEM, I. Yonekura, T. Yoshii, Y. Negishi, K. Oohira, K. Kanayama, M. Kawashita, Y. Sakata, K. Tanaka, Toppan Printing Co., Ltd. (Japan) . . [6730-202]

EUV mask substrate flatness improvement by laser irradiation, K. Takehisa, J. Kodama, H. Kusunose, Lasertec Corp. (Japan) . . . . [6730-203]

Posters-Tuesday

Chairs: **Wolfgang Staud**, B[2]W Consulting; **Hiroichi Kawahira**, Sony Corp. (Japan)

Poster Sessions 14 *(continued).*

Evaluation of EUVL-mask pattern defect inspection using 199-nm inspection optics, T. Amano, Y. Nishiyama, H. Shigemura, T. Terasawa, O. Suga, Semiconductor Leading Edge Technologies, Inc. (Japan) . . . [6730-204]

Study of impacts of mask structure on hole pattern in EUVL, N. Iriki, H. Aoyama, T. Tanaka, Semiconductor Leading Edge Technologies, Inc. (Japan) . . . . [6730-205]

Repair specification study for half-pitch 32-nm patterns on EUVL, H. Aoyama, T. Amano, Y. Nishiyama, H. Shigemura, O. Suga, Semiconductor Leading Edge Technologies, Inc. (Japan) . . . . [6730-206]

EUV process development using DUV inspection system, D. H. Kim, A. Cao, V. Vellanki, KLA-Tencor Corp. . . . . [6730-207]

Developemt of EUV mask fabrication process using Ru capping blank, T. Abe, T. Adachi, H. Mohri, S. Sasaki, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan); K. Ishikiriyama, Intel Kabushiki Kaisha (Japan) . . . . . . [6730-208]

PS15: Imprint

Metrology for templates of UV nano-imprint lithography, K. Yoshida, K. Kojima, M. Abe, S. Sasaki, M. Kurihara, H. Mohri, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan) . . . . [6730-209]

UV-NIL templates for the 22-nm node and beyond, T. Hiraka, Dai Nippon Printing Co., Ltd.; S. Yusa, A. Fujii, S. Sasaki, K. Ito, N. Toyama, M. Kurihara, H. Mohri, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan) . . . . . . [6730-210]

A study of template cleaning for nano-imprint lithography, J. E. Ellenson, L. C. Litt, A. Rastegar, SEMATECH, Inc. . . . . [6730-211]

Wednesday 19 September

Sessions 9-10-11-12 run concurrently with sessions 13-14-15-16.

SESSION 9

Room: Steinbeck Forum . . . . Wed. 8:00 to 10:00 am

EUV and OGL

Chairs: **William H. Broadbent**, KLA-Tencor Corp.; **Han-Ku Cho**, SAMSUNG Electronics Co., Ltd. (South Korea); **Warren M. Montgomery**, Albany NanoTech

8:00 am: **Investigation of mask defectivity in full-field EUV lithography,** R. M. Jonckheere, F. Iwamoto, A. Myers, IMEC (Belgium); J. van der Donck, TNO (Netherlands); T. Liang, Intel Corp.; J. D. Zimmerman, ASML Wilton; G. F. Lorusso, A. Goethals, IMEC (Belgium) . . . . [6730-37]

8:20 am: **Detectability and printability of EUVL-mask blank defects for the 32-nm HP node,** W. Cho, H. Han, P. Kearney, C. Jeon, SEMATECH, Inc. . . . . . . [6730-38]

8:40 am: **Measuring and characterizing the nonflatness of EUVL reticles and electrostatic chucks,** R. L. Engelstad, M. Nataraju, J. Sohn, J. Zeuske, V. S. Battula, A. R. Mikkelson, Univ. of Wisconsin/Madison . . . . [6730-39]

9:00 am: **Recent performance of EUV mask blanks with low-thermal expansion glass substrates,** T. Shoki, T. Yamada, K. Koike, H. Shishido, S. Shimojima, Y. Shiota, M. Hosoya, HOYA Corp. (Japan) . . . . [6730-40]

9:20 am: **Investigation of resist effects on EUV mask defect printability,** Z. J. Zhang, T. Liang, Intel Corp. . . . . [6730-41]

9:40 am: **Impact of mask absorber properties on printability in EUV lithography,** T. Kamo, H. Aoyama, O. Suga, Semiconductor Leading Edge Technologies, Inc. (Japan) . . . . [6730-42]

Coffee Break . . . . 10:00 to 10:30 am

SESSION 10

Room: Steinbeck Forum . . . . Wed. 10:30 am to 12:10 pm

Cleaning I

Chairs: **Naoya Hayashi**, Dai Nippon Printing Co., Ltd. (Japan); **Brian J. Grenon**, Grenon Consulting, Inc.; **Han-Ku Cho**, SAMSUNG Electronics Co., Ltd. (South Korea)

10:30 am: **Capability of eco-friendly cleaning strategy corresponding to advanced technology,** S. Jeong, D. W. Lee, J. Ryu, J. Ryu, S. P. Kim, O. Han, Hynix Semiconductor Inc. (South Korea) . . . . [6730-165]

10:50 am: **Compositional analysis of progressive defects on a photomask,** K. Saga, H. Kawahira, Sony Corp. (Japan) . . . . [6730-44]

11:10 am: **A practical solution for 193-nm reticle haze,** O. P. Kishkovich, T. Kielbaso, D. Halbmaier, Entegris, Inc.; J. Lo, Entegris Asia LLC (Taiwan); X. Gabarre, Entegris Singapore Pte Ltd. (Singapore); B. J. Grenon, Grenon Consulting, Inc. . . . . [6730-45]

11:30 am: **Rapid and precise monitor of reticle haze,** T. E. Zavecz, TEA Systems Corp. . . . . [6730-46]

11:50 am: **Characterization of chemical mobility behavior toward haze defect creation on mask substrate during laser exposure,** H. Lee, SAMSUNG Electronics Co., Ltd. (South Korea) . . . . [6730-47]

Lunch/Exhibition Break . . . . 12:10 to 1:30 pm

SESSION 13

Room: Ferrante . . . . Wed. 8:00 to 11:10 am

Simulation

Chairs: **Bernd Geh**, ASML US, Inc.; **Frank A. J. M. Driessen**, Takumi Technology B.V. (Netherlands); **Roxann L. Engelstad**, Univ. of Wisconsin/Madison

8:00 am: **Simulation of larger mask areas using the waveguide method with fast decomposition technique,** P. Evanschitzky, F. Shao, A. Erdmann, D. Reibold, Fraunhofer Institute of Integrated Systems and Device Technology (Germany) . . . . [6730-59]

8:20 am: **Polarization aberration modeling via Jones matrix in the context of OPC,** Q. Zhang, H. Song, K. D. Lucas, Synopsys, Inc. . . . . [6730-60]

8:40 am: **Validation of a fast and accurate 3D mask model for 25-nm SRAF printability analysis,** P. Liu, Y. Xu, Brion Technologies, Inc. . . . . [6730-61]

9:00 am: **Fast three-dimensional simulation of buried EUV mask defect interaction with absorber features,** C. H. Clifford, A. R. Neureuther, Univ. of California/Berkeley . . . . [6730-62]

9:20 am: **Polarization-induced astigmatism caused by topographic masks,** J. Ruoff, Carl Zeiss SMT AG (Germany); S. Perlitz, Carl Zeiss SMS GmbH (Germany); C. J. Progler, Photronics, Inc.; B. Geh, ASML US, Inc. and Consultant . . . . [6730-63]

9:40 am: **Characterization and monitoring photomask edge effects,** M. A. Miller, A. R. Neureuther, D. P. Ceperley, K. Kikuchi, Univ. of California/Berkeley . . . [6730-64]

Coffee Break . . . . 10:00 to 10:30 am

10:30 am: **Understanding mask topography in attenuated phase-shift masks,** E. Yesilada, M. Saied, Freescale Semiconductor, Inc. (France) . . . . . [6730-65]

10:50 am: **Fast and accurate laser band-width modeling of optical proximity effects,** I. Lalovic, Cymer, Inc.; O. Kritsun, Advanced Micro Devices, Inc.; J. J. Bendik, Dynamic Intelligence; M. D. Smith, C. A. Sallee, KLA-Tencor Corp.; N. R. Farrar, Cymer, Inc. . . . . [6730-66]

SESSION 14

Room: Ferrante . . . . Wed. 11:10 to 11:50 am

Repair I

Chairs: **Ronald R. Bozak**, RAVE LLC; **Benjamin G. Eynon, Jr.**, SAMSUNG; **J. Tracy Weed**, Synopsys, Inc.

11:10 am: **Advanced mask particle cleaning solutions,** T. E. Robinson, A. G. Dinsdale, R. R. Bozak, B. Arruza, RAVE LLC . . . . [6730-67]

11:30 am: **Integrated photomask defect printability check, mask repair, and repair validation procedure for phase-shifting masks for the 45-nm node and beyond,** C. Ehrlich, T. Scheruebl, U. Buttgereit, Carl Zeiss SMS GmbH (Germany); K. Edinger, NaWoTec GmbH (Germany) . . . . [6730-68]

Lunch/Exhibition Break . . . . 11:50 am to 1:10 pm

Wednesday 19 September

Sessions 9-10-11-12 run concurrently with sessions 13-14-15-16 *(continued)*.

SESSION 11

Room: Steinbeck Forum . . . . Wed. 1:30 to 2:30 pm

Cleaning II

Chairs: **Naoya Hayashi**, Dai Nippon Printing Co., Ltd. (Japan); **Brian J. Grenon**, Grenon Consulting, Inc.; **Han-Ku Cho**, SAMSUNG Electronics Co., Ltd. (South Korea)

1:30 pm: **Investigation of airborne molecular contamination adsorption rate as storage materials in mask,** C. Yang, S&S TECH (South Korea); H. Cha, Hanyang Univ. (South Korea); S. Yang, J. Kang, S&S TECH (South Korea); J. Ahn, Hanyang Univ. (South Korea); K. Nam, S&S TECH (South Korea) . . . . [6730-48]

1:50 pm: **Study of time dependent 193-nm reticle haze,** J. S. Gordon, L. E. Frisa, C. M. Chovino, D. Y. Chan, J. Keagy, Toppan Photomasks, Inc.; O. P. Kishkovich, F. V. Belanger, T. Scoggins, Entegris, Inc. . . . . [6730-49]

2:10 pm: **Full sulphate-free process: joint achievement of minimal residual ions and yield improvement,** F. Perissinotti, L. Sartelli, D. Cassago, H. Miyashita, DNP Photomask Europe (Italy) . . . . [6730-50]

SESSION 12

Room: Steinbeck Forum . . . . Wed. 2:30 to 5:40 pm

Extreme NA

Chairs: **Donis G. Flagello**, ASML US, Inc.; **Thomas H. Newman**, Micronic Laser Systems Inc.; **Geert Vandenberghe**, IMEC (Belgium)

2:30 pm: **Using the AIMS™ 193i for hyper-NA imaging applications,** P. De Bisschop, V. Philipsen, IMEC (Belgium); R. Birkner, U. Buttgereit, R. Richter, T. Scheruebl, Carl Zeiss SMS GmbH (Germany) . . . . [6730-51]

2:50 pm: **Mask characterization for double-patterning lithography,** K. Bubke, Advanced Mask Technology Ctr. (Germany); E. P. Cotte, J. H. Peters, Advanced Mask Technology Ctr.; R. de Kruif, ASML Netherlands B.V. (Netherlands); J. van Praagh, ASML Netherlands B.V.; M. V. Dusa, ASML US, Inc.; J. Fochler, B. Connolly, Toppan Photomasks, Inc. (Germany) . . [6730-52]

Coffee Break . . . . 3:10 to 3:40 pm

3:40 pm: **DPL performance analysis strategy with conventional workflow,** N. Toyama, Y. Inazuki, T. Sutou, T. Nagai, Y. Morikawa, H. Mohri, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan); J. Miyazaki, ASML Japan Co., Ltd. (Japan); A. C. Chen, ASML Taiwan Ltd. (Taiwan); N. Samarakone, ASML US, Inc. . . . . [6730-53]

4:00 pm: **Estimating DPL photomask fabrication load compared with single exposure,** N. Toyama, Y. Inazuki, T. Sutou, T. Nagai, Y. Morikawa, H. Mohri, N. Hayashi, Dai Nippon Printing Co., Ltd. (Japan); J. A. Huckabay, Cadence Design Systems, Inc.; Y. Abe, Cadence Design Systems, Inc. (Japan) . . . . [6730-54]

4:20 pm: **Placement or overlay: meeting double-patterning challenges in mask lithography,** R. B. Cinque, T. Wandel, E. P. Cotte, Advanced Mask Technology Ctr. (Germany); K. Bubke, Advanced Mask Technology Ctr.; K. S. Yeo, P. D. Buck, Toppan Photomasks, Inc. . . . . [6730-55]

4:40 pm: **The MEEF NILS divergence for low-k1 lithography,** R. E. Schenker, W. Cheng, G. A. Allen, Intel Corp. [6730-56]

5:00 pm: **Impact of alternative mask stacks on the imaging performance at NA1.20 and above,** V. Philipsen, K. Mesuda, P. De Bisschop, IMEC (Belgium); A. Erdmann, G. Citarella, P. Evanschitzky, Fraunhofer Institut Integrierte System und Bauelem (Germany); R. Birkner, R. Richter, T. Scheruebl, Carl Zeiss SMS GmbH (Germany) . . . . [6730-57]

5:20 pm: **Requirements of photomask registration for the 45-nm node and beyond: is it possible?,** J. Choi, H. Kim, SAMSUNG Electronics Co., Ltd. (South Korea); S. Lee, SAMSUNG Electronics Co., Ltd.; D. Lee, H. Jeong, J. Lee, B. Kim, S. Woo, H. Cho, SAMSUNG Electronics Co., Ltd. (South Korea) . . . . [6730-58]

SESSION 15

Room: Ferrante . . . . Wed. 1:10 to 2:10 pm

Repair II

Chairs: **Ronald R. Bozak**, RAVE LLC; **Benjamin G. Eynon, Jr.**, SAMSUNG; **J. Tracy Weed**, Synopsys, Inc.

1:10 pm: **A semi-automated AFM photomask repair process for manufacturing application using SPR6300,** M. Dellagiovanna, H. Yoshioka, H. Miyashita, DNP Photomask Europe (Italy); S. M. Murai, Dai Nippon Printing Co., Ltd. (Japan); T. Nakaue, O. Takaoka, A. Uemoto, S. Kikuchi, R. Hagiwara, SII NanoTechnology Inc. (Japan); S. Benard, Bs Technology e.u.r.l. (France) . . . . [6730-69]

1:30 pm: **Repairing 45-nm node defects through nano-machining,** D. Brinkley, J. E. Csuy, RAVE LLC . . . . [6730-70]

1:50 pm: **The cleaning effects of mask aerial image after FIB repair in sub-80-nm node,** H. Lee, G. Jeong, S. Jeong, S. Kim, O. Han, Hynix Semiconductor Inc. (South Korea) . . . . [6730-71]

SESSION 16

Room: Ferrante . . . . Wed. 2:10 to 5:40 pm

Inspection

Chairs: **William H. Broadbent**, KLA-Tencor Corp.; **Emily E. Gallagher**, IBM Corp.; **Craig A. West**, Toppan Photomasks, Inc.

2:10 pm: **Wafer inspection as alternative approach to mask defect qualification,** C. Holfeld, Advanced Mask Technology Ctr. (Germany); F. Katzwinkel, U. Seifert, Qimonda Dresden GmbH & Co. OHG (Germany); A. Mothes, Advanced Mask Technology Ctr. (Germany) . . . . [6730-72]

2:30 pm: **A pragmatic approach to high-sensitivity defect inspection in the presence of mask process variability,** S. Han, SAMSUNG Electronics Co., Ltd. (South Korea) . . . . [6730-73]

2:50 pm: **Sensitivity comparison of fast integrated die-to-die T+R pattern inspection and STARlight2™ mode for application in mask production,** J. P. Heumann, T. Schulmeyer, Advanced Mask Technology Ctr. (Germany); H. Schmalfuss, M. Lang, KLA-Tencor GmbH (Germany); K. Bhattacharyya, KLA-Tencor Corp. . . . . [6730-74]

Coffee Break . . . . 3:10 to 3:40 pm

3:40 pm: **Optimizing defect inspection strategy through the use of design-aware database control layers,** D. Stoler, KLA-Tencor Corp.; R. E. Morgan, L. Wang, J. Burns, Synopsys, Inc. . . . . [6730-75]

4:00 pm: **Progressive growth defect disposition and printability for 65-nm and 45-nm ArF immersion lithography,** G. Chua, I. Lee, S. Tan, J. S. Kim, Chartered Semiconductor Manufacturing Ltd. (Singapore) . . . . [6730-76]

4:20 pm: **Characterizing DUV contamination inspection capabilities using programmed defect test reticles,** A. B. Nhiev, J. A. Straub, J. Riddick, C. P. Weins, D. Aguilar, Toppan Photomasks, Inc.; B. Reese, T. A. Hutchinson, A. Dayal, KLA-Tencor Corp. . . . . [6730-77]

4:40 pm: **Mask inspection method for 45-nm node,** S. Oh, Y. Choi, O. Han, Hynix Semiconductor Inc. (South Korea) . . . . [6730-78]

5:00 pm: **Inspection results for 32-nm logic and sub-50-nm half-pitch memory reticles using the TeraScanHR,** F. Mirzaagha, D. H. Kim, P. P. Yu, J. E. Sier, KLA-Tencor Corp. . . . . [6730-79]

5:20 pm: **Automatic optimization of MEEF-driven defect disposition for contamination inspection challenges,** T. Huang, A. Dayal, K. Bhattacharyya, KLA-Tencor Corp. . . . . [6730-80]

Thursday 20 September

Sessions 17-18-19-20 run concurrently with sessions 21-22-23-24.

SESSION 17

Room: Steinbeck Forum . . . . Thurs. 8:00 to 10:00 am

Advanced RET

Chairs: **Wilhelm Maurer**, Infineon Technologies AG (Germany); **Brian J. Grenon**, Grenon Consulting, Inc.; **Alan J. Leslie**, IBM Corp.

8:00 am: **Paving the way to a full-chip gate-level double-patterning application,** H. Haffner, Infineon Technologies NA Corp.; Z. Baum, S. D. Halle, J. E. Meiring, IBM Microelectronics Div. . . . . [6730-81]

8:20 am: **Slanted sub-resolution fill pattern to suppress the lens-heating-induced field distortion by the dipole illumination,** F. Wang, X. Lei, W. A. Stanton, L. K. Somerville, Micron Technology, Inc. . . . . [6730-181]

8:40 am: **Automatic SRAF placement optimization based on process-window variability reduction,** A. M. Yehia, Mentor Graphics Corp. (Egypt); S. Jayaram, L. Hong, H. A. Maaty Omar, M. S. Bahnas, J. L. Sturtevant, Mentor Graphics Corp. . . . . [6730-83]

9:00 am: **Full-chip based assist features correction for mask manufacturing,** B. Jumi, SAMSUNG Electronics Co., Ltd. (South Korea) . . . . [6730-84]

9:20 am: **Etch-proximity correction by model-based retargeting within integrated OPC flow,** S. D. Shang, Y. Granik, Mentor Graphics Corp.; M. Niehoff, Mentor Graphics Corp. (Germany) . . . . [6730-85]

9:40 am: **Resolution enhancement by aerial image approximation with 2D-TCC,** K. Yamazoe, Y. Sekine, M. Kawashima, M. Hakko, T. Ono, T. Honda, Canon Inc. (Japan) . . . . [6730-86]

Coffee Break . . . . 10:00 to 10:30 am

SESSION 18

Room: Steinbeck Forum . . . . Thurs. 10:30 am to 12:10 pm

RET I

Chairs: **Wolfgang Staud**, B^{2}W Consulting; **Christopher A. Spence**, Advanced Micro Devices, Inc.; **Peter D. Buck**, Toppan Photomasks, Inc.

10:30 am: **Exploring the sources of MEEF in contact SRAMs,** E. E. Gallagher, I. P. Stobert, B. R. Liegl, IBM Corp.; M. Higuchi, Toppan Electronics, Inc.; I. Yonekura, Toppan Printing Co., Ltd. . . . . [6730-87]

10:50 am: **The improvement of OPC accuracy and stability by the model parameters' analysis and optimization,** N. Chung, SAMSUNG Electronics Co., Ltd. (South Korea) . . . . [6730-88]

11:10 am: **Simultaneous model-based main feature and SRAF optimization for 2D SRAF implementation to 32-nm critical layers,** A. M. Yehia, Mentor Graphics Corp. (Egypt); A. V. Tritchkov, Mentor Graphics Corp. . . . [6730-186]

11:30 am: **Customizing proximity correction for gate etch, contact etch, and resist reflow,** D. F. Beale, Synopsys, Inc. . . . . [6730-90]

11:50 am: **Fast synthesis of topographic mask effects based on rigorous solutions,** Q. Yan, Z. Deng, J. P. Shiely, Synopsys, Inc. . . . . [6730-91]

Lunch Break . . . . 12:10 to 1:30 pm

SESSION 21

Room: Ferrante . . . . Thurs. 8:00 to 11:10 am

Patterning

Chairs: **Peter D. Buck**, Toppan Photomasks, Inc.; **Thomas H. Newman**, Micronic Laser Systems Inc.; **Patrick M. Martin**, Photronics, Inc.

8:00 am: **Advanced mask process compensation for 45-nm node and beyond,** K. Kageyama, K. Miyoko, Y. Okuda, Toppan Printing Co., Ltd. (Japan); G. Percin, Invarium Inc.; A. Sezginer, J. Carrero, A. Zhu, A. Liu, Cadence Design Systems, Inc. . . . . [6730-103]

8:20 am: **Improvement of mask CD uniformity for below 45-nm node technology,** H. Lee, S. Bae, J. M. Park, J. H. Park, E. H. Jung, D. Nam, B. Kim, S. Woo, H. Cho, SAMSUNG Electronics Co., Ltd. (South Korea) . . . [6730-104]

8:40 am: **Correction technique of EBM-6000 prepared for EUV mask writing,** S. Yoshitake, H. Sunaoshi, J. Yashima, S. Tamamushi, NuFlare Technology, Inc. (Japan); M. Ogasawara, Toshiba Corp. (Japan) . . . [6730-105]

9:00 am: **Coping with double-patterning/exposure lithography by EB mask writer EBM-6000,** K. Takashi, N. Rieko, T. Kaoru, H. Kiyoshi, T. Jun, Y. Shusuke, N. Hiroshi, H. Sunaoshi, T. Shuichi, NuFlare Technology, Inc. (Japan) . . . . [6730-106]

9:20 am: **Performance comparison of techniques for intra-field CD control improvement,** R. Pforr, M. Hennig, J. Reichelt, Qimonda Dresden GmbH & Co. OHG (Germany); M. Sczyrba, Advanced Mask Technology Ctr. (Germany); G. Ben-Zvi, Pixer Technology Ltd. (Israel) . . . . [6730-107]

9:40 am: **Projection maskless patterning (PMLP) for the fabrication of leading-edge complex masks and nano-imprint templates,** E. Platzgummer, H. Löschner, G. Gross, IMS Nanofabrication AG (Austria) . . . . [6730-108]

Coffee Break . . . . 10:00 to 10:30 am

10:30 am: **Improving the CD linearity and proximity performance of photomasks written on the Sigma7500-II DUV laser writer through embedded OPC,** A. Österberg, L. Ivansen, H. Åhlfeldt, H. A. Fosshaug, P. Högfeldt, Micronic Laser Systems AB (Sweden); A. M. Bowhill, E. Y. Sahouria, S. F. Schulze, Mentor Graphics Corp. . . . . [6730-109]

10:50 am: **Contrast properties of spatial light modulators for microlithography,** J. Heber, D. Kunze, P. Dürr, D. Rudloff, M. Wagner, Fraunhofer-Institut für Photonische Mikrosysteme (Germany); P. B. Björnängen II, J. Z. Luberek, U. Berzinsh, T. Sandstrom, T. Karlin, Micronic Laser Systems AB (Sweden) . . . . [6730-110]

SESSION 22

Room: Ferrante . . . . Thurs. 11:10 to 11:50 am

Metrology I

Chairs: **Thomas H. Newman**, Micronic Laser Systems Inc.; **Bernd Geh**, ASML US, Inc.; **Emily E. Gallagher**, IBM Corp.

11:10 am: **Accuracy of mask pattern contour extraction with fine pixel SEM images,** S. Yamaguchi, E. Yamanaka, M. Kariya, H. Mukai, T. Kotani, H. Mashita, M. Itoh, Toshiba Semiconductor Co. (Japan) . . . . [6730-111]

11:30 am: **Two-dimensional measurement using CD SEM for arbitrarily shaped patterns,** H. Lee, SAMSUNG Electronics Co., Ltd. (South Korea) . . . . [6730-112]

Lunch Break . . . . 11:50 am to 1:10 pm

Thursday 20 September

Sessions 17-18-19-20 run concurrently with sessions 21-22-23-24 *(continued)*.

SESSION 19

Room: Steinbeck Forum . . . . Thurs. 1:30 to 4:20 pm

RET II

Chairs: **Wolfgang Staud**, B²W Consulting; **Christopher A. Spence**, Advanced Micro Devices, Inc.; **Peter D. Buck**, Toppan Photomasks, Inc.

1:30 pm: **Improving hyper-NA OPC using targeted measurements for model parameter extraction,** B. S. Ward, IMEC (Belgium); K. D. Lucas, Synopsys, Inc. . . . . [6730-92]

1:50 pm: **Selective process aware OPC for memory device,** S. Suh, W. Shim, S. Lee, SAMSUNG Electronics Co., Ltd. (South Korea); R. M. Lugg, F. P. Amoroso, S. Lee, Synopsys, Inc. . . . . [6730-93]

2:10 pm: **Validating optical proximity correction,** S. R. Marokkey, Infineon Technologies North America; E. Conrad, E. E. Gallagher, IBM Corp.; H. Ikeda, Toppan Electronics, Inc.; J. Bruce, M. Lawliss, IBM Corp. . . . . [6730-94]

2:30 pm: **The study of phase-angle and transmission specifications of 6% att-EAPSM for 90-nm, 65-nm, and 45-nm nodes wafer manufacturing patterning process,** G. Chen, C. M. Garza, Freescale Semiconductor, Inc. . . . . [6730-95]

2:50 pm: **Better on wafer performance and mask manufacturability of contacts with no or non-traditional serifs,** D. J. Samuels, I. P. Stobert, IBM Corp. . . . . [6730-96]

Coffee Break . . . . 3:10 to 3:40 pm

3:40 pm: **Optimization of OPC runtime using efficient optical simulation,** M. Al-Imam, W. Tawfik, Mentor Graphics Corp. (Egypt) . . . . [6730-97]

4:00 pm: **Full-chip process window OPC capability assessment,** P. J. M. VanAdrichem, Synopsys, Inc. . . . . [6730-98]

SESSION 20

Room: Steinbeck Forum . . . . Thurs. 4:20 to 5:20 pm

Mask Business/Management

Chairs: **Han-Ku Cho**, SAMSUNG Electronics Co., Ltd. (South Korea); **Mark E. Mason**, Texas Instruments Inc.; **Paul F. Luehrmann, Jr.**, ASML Netherlands B.V. (Netherlands)

4:20 pm: **EBDW is free,** L. A. Glasser, KLA-Tencor Corp. . . . . [6730-100]

4:40 pm: **Driving photomask supplier quality through automation,** D. R. Russell, A. P. Espenscheid, Freescale Semiconductor, Inc. . . . . [6730-101]

5:00 pm: **Multi-layer reticle (MLR) strategy application to double-patterning/double-exposure for better overlay error control and mask cost reduction,** Y. Yamamoto, Cadence Design Systems, Inc. (Japan); R. Rigby, J. Sweis, Cadence Design Systems, Inc. . . . . [6730-102]

SESSION 23

Room: Ferrante . . . . Thurs. 1:10 to 3:10 pm

Metrology II

Chairs: **Thomas H. Newman**, Micronic Laser Systems Inc.; **Bernd Geh**, ASML US, Inc.; **Emily E. Gallagher**, IBM Corp.

1:10 pm: **Resist CD metrology and profile characterization using CD SEM technology,** Y. Cui, M. Tavassoli, K. Baik, P. Qu, K. Yung, S. Chegwidden, Intel Corp. . . . . [6730-113]

1:30 pm: **Preliminary verifiability of the aerial image measurement tool over photolithography process,** H. Lee, G. Jeong, S. Kim, O. Han, Hynix Semiconductor Inc. (South Korea) . . . . [6730-114]

1:50 pm: **Calibration of contact areas: the influence of corner rounding,** J. Richter, T. Marschner, E. Zerbe, Advanced Mask Technology Ctr. (Germany) . . . . [6730-115]

2:10 pm: **Measurements of corner rounding in 2D contact holes on phase-shift masks using broadband reflectance and transmittance spectra in conjunction with RCWA,** J. C. Lam, n&k Technology, Inc.; J. Richter, Advanced Mask Technology Ctr. (Germany); R. C. Howell, n&k Technology, Inc.; A. Gray, Univ. of California/Davis; S. S. Chen, n&k Technology, Inc. . . . . [6730-116]

2:30 pm: **Photomask applications of traceable atomic-force microscope dimensional metrology at NIST,** R. G. Dixson, N. G. Orji, J. E. Potzick, J. Fu, National Institute of Standards and Technology . . . . [6730-117]

2:50 pm: **Laterally resolved off-axis phase measurements on 45-nm node production features using Phame™,** S. Perlitz, U. Buttgereit, Carl Zeiss SMS GmbH (Germany); K. M. Lee, M. Tavassoli, Intel Corp. . . . . [6730-118]

Coffee Break . . . . 3:10 to 3:40 pm

SESSION 24

Room: Ferrante . . . . Thurs. 3:40 to 5:20 pm

MDP

Chairs: **Richard D. Morse**, Silicon Canvas Inc.; **Artur P. Balasinski**, Cypress Semiconductor Corp.; **Patrick M. Martin**, Photronics, Inc.

3:40 pm: **LRC techniques for improved error detection throughout the process window,** V. Lee, S. H. Tsai, United Microelectronics Corp. (Taiwan); J. Zhu, L. Wang, D. L. White, Synopsys, Inc. . . . . [6730-119]

4:00 pm: **Tera-computing for mask data preparation,** J. T. Nogatch, H. Kirsch, J. Yeap, Synopsys, Inc. . . . . [6730-120]

4:20 pm: **Parallel hierarchical method in mask data preparation,** O. V. Malinochka, L. I. Timchenko, Kiev Univ. of Economy and Transport Technology (Ukraine) . . . . [6730-121]

4:40 pm: **Mask manufacturability improvement by MRC,** A. P. Balasinski, D. L. Coburn, Cypress Semiconductor Corp.; P. D. Buck, Toppan Photomasks, Inc. . . . . [6730-122]

5:00 pm: **Reduction of layout complexity for shorter mask write time,** T. Lewis, S. Hannon, S. Goad, Advanced Micro Devices, Inc.; E. Y. Sahouria, H. T. Vu, S. F. Schulze, K. R. Jantzen, Mentor Graphics Corp. . . . . . [6730-123]

Friday 21 September

Room: Steinbeck Forum . . . . Fri. 8:00 am to 1:00 pm

Friday Special Session on Double Patterning Lithography: Challenges and Approaches to Implementation- Twice the Pain for Twice the Gain

Chairs: **Hiroichi Kawahira,** Sony Corp. (Japan); **Artur P. Balasinski,** Cypress Semiconductor Corp.; **Paul F. Luehrmann, Jr.,** ASML Netherlands B.V. (Netherlands)

Introduction . . . . 8:00 to 8:05 am

Chair: **Hiroichi Kawahira,** Sony Corp. (Japan)

8:05 to 8:20 am: **Summary of BACUS Panel Discussion on ITRS-DPL at Advanced Lithography (2007), Artur Balasinski,** Cypress Semiconductor Corp.

Room: Steinbeck Forum . . . . Fri. 8:20 to 10:05 am

Lithography Perspectives

8:20 am: **Donald Samuels,** IBM Corp.

8:35 am: **Robert M. Bigwood,** Intel Corp.

8:50 am: **Jongwook Kye,** Advanced Micro Devices, Inc.

9:05 am: **Steven R. J. Brueck,** CHTM/The Univ. of New Mexico

9:20 am: **Mircea V. Dusa,** ASML US, Inc.

9:35 am: **Tommy Oga,** Cymer, Inc.

9:50 am: **Geert Vandenberghe,** IMEC (Belgium)

Room: Steinbeck Forum . . . . Fri. 10:05 to 10:35 am

EDA Perspectives

10:05 am: **Judith A. Huckabay,** Cadence Design Systems, Inc.

10:20 am: **Frank M. Schellenberg,** Mentor Graphics Corp.

Coffee Break . . . . 10:35 to 10:55 am

Room: Steinbeck Forum . . . . Fri. 10:55 am to 12:55 pm

Mask Perspectives

10:55 am: **Takashi Kamikubo,** NuFlare Technology, Inc. (Japan)

11:10 am: **William H. Broadbent,** KLA-Tencor Corp.

11:25 am: **Junwei Bao,** Timbre Technologies, Inc.

11:40 am: **Terrance E. Zavecz,** TEA Systems Corp.

11:55 am: **Han-ku Cho,** SAMSUNG Electronics Co., Ltd. (South Korea)

12:10 pm: **Nak Seong,** Photronics, Inc.

12:25 pm: **Naoya Hayashi,** Dai Nippon Printing Co., Ltd. (Japan)

12:40 pm: **Frasnklin D. Kalk,** Toppan Photomasks, Inc.

Closing Remarks . . . . 12:55 to 1:00 pm

Chair: **Hiroichi Kawahira,** Sony Corp. (Japan)

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Computational Lithography

SC856

NEW!

Course level: Intermediate
CEU .35 $280 / $325 USD
Monday 8:30 am to 12:30 pm

Computational Lithography (CL) has proven to be an enabling technology, not only in Optical Proximity Correction and Verification, but in the specification of design rules and the development of new Resolution Enhancement Techniques (RET). This course will cover a broad spectrum of the field of CL; from the need for simulation, to its use in RET development and Design for Manufacturability (DfM), to recent advances in modeling techniques. The course material assumes a basic understanding of lithography processes and methods to characterize those processes, and will focus primarily on applications of CL. RET development will be discussed with an emphasis on double patterning. Future challenges in predictive modeling, along with the special challenges of modeling for DfM applications, will also be presented.

LEARNING OUTCOMES

This course will enable you to:

- define computational lithography and its applications
- explain the challenges of traditional RET, such as subresolution assist features, along with more recent double-patterning techniques
- describe predictive modeling and the challenges of process modeling in DfM

INTENDED AUDIENCE

This material is intended for anyone with an interest in the application of Computational Lithography in RET development, design rule specification and DfM.

INSTRUCTOR

Scott Mansfield currently develops predictive modeling techniques and applications in support of IBM's broader computational lithography initiatives. He has lead the development of advanced RET within IBM's Semiconductor Research and Development Center including attenuated phase shift masks, sub-resolution assist features and various double-exposure techniques. He has explored the relationship between RET and design through his role in the definition of design rules down to 32nm.

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Introduction to Design for Manufacturability

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Monday 1:30 to 5:30 pm

Design for Manufacturability (DfM) means different things to different people: those on the design side of our business see it as the art of reducing dimensional and parametric conservatism while protecting aggressive time to market targets, those on the manufacturing side look to DfM to preserve profitability in light of increasing process complexity. Regardless of individual motivations, it is clear that DfM will continue to gain importance as traditional CMOS scaling is rapidly coming to an end.

This short course will review the most popular manufacturability analysis techniques and their uses in DfM-enhanced design flows. Model-based techniques such as critical area analysis, lithography hotspot detection, and CMP thickness prediction will be contrasted to rules based techniques such as recommended design rules or enhanced routing rules. Differences between feed-back techniques such as process aware layout optimization and feed-forward techniques such as restricted design rules and design aware manufacturing will be discussed. The advantages and challenges of introducing manufacturability knowledge early in the design flow will be compared to those of applying manufacturability considerations late. Finally, the most prominent opportunities for innovation in DfM for technology nodes beyond 65nm will be reviewed.

LEARNING OUTCOMES

This course will enable you to:

- summarize established DfM analysis and optimization techniques
- recognize key components of a generic design to silicon flow and appreciate the DfM opportunities in it
- discuss the complex tradeoffs that have to be made in optimizing an integrated DfM solution

INTENDED AUDIENCE

This course is intended for anyone who is interested in getting a broad overview of DfM capabilities, opportunities, and challenges.

INSTRUCTOR

Lars Liebmann comes to DfM with a background in advanced lithography where he spent the first 13 years of his career developing and implementing layout manipulation solutions for optical proximity correction and resolution enhancement techniques (RET). His work on layout intensive RET for leading edge logic products lead to his pioneering work on restricted design rules (RDR) as a practical means of implementing DfM. Now Dr. Liebmann is charged with the strategic integration and execution of all aspects of DfM in IBM's Semiconductor Research and Development Center.

Nanoscale Metrology - Theory and Practice

SC854

NEW!

Course level: Introductory
CEU .35 $280 / $325 USD
Monday 1:30 to 5:30 pm

This course provides attendees with a basic working knowledge of the principles of metrology, with emphasis on measuring the size or placement of features on IC wafers and photomasks. The course covers the metrology concepts defined by ISO (the International Organization for Standardization) and used by national metrology laboratories around the world, and shows how to reduce these concepts to practice in a research or manufacturing environment. Practical examples will be given.

LEARNING OUTCOMES

This course will enable you to:

- understand concepts like accuracy, measurement uncertainty, error, and traceability
- determine which measurement errors are most significant and reduce them
- quantitatively determine the ISO uncertainty of a measurement
- critically interpret a measurement result
- calculate the cost/benefit ratio of a measurement in IC manufacturing
- decide how much accuracy is sufficient in a given situation

INTENDED AUDIENCE

This material is intended for anyone who measures IC feature size, placement, overlay, LER, etc., in manufacturing or research; anyone who manages a metrology activity; anyone involved in the critical evaluation of measurement results.

INSTRUCTORS

James Potzick has held staff positions at the National Institute of Standards and Technology (NIST) for over 30 years, with over 50 publications and 3 patents.

Brian Grenon has been involved with IC metrology and manufacturing for many years. He is a past president of BACUS.

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Applying Optical Proximity Correction and Design for Manufacturability to Product Designs

SC540

NEW!

Course level: Introductory
CEU .65 $460 / $545 USD
Monday 8:30 am to 5:30 pm

Optical proximity correction (OPC) is now a requirement for advanced semiconductor manufacturing. OPC alters the designed layout to compensate for systematic patterning distortions and/or to implement process latitude improving methods. Accurate and practical model-based OPC implementation is needed with essentially all lithography resolution enhancement techniques (RET) on complex real world designs. This practical example-oriented class will prepare attendees to implement manufacturable rule and model-based OPC on their product designs and introduce them to optimized OPC, design & process solution methods known as lithographic Design for Manufacturability (DFM).

LEARNING OUTCOMES

This course will enable you to:

- describe detailed OPC techniques, capabilities and issues
- build, apply, optimize and debug Model-based OPC for your process/RET/design style
- implement precise verification and risk mitigation steps into the RET flow
- compare OPC software capabilities & implementation on specific practical criteria
- apply DFM analysis & correction techniques to critical design/process spaces
- evaluate and minimize the negative impact of OPC in the tapeout/design flow
- estimate and/or justify OPC process/software/hardware costs to management

INTENDED AUDIENCE

This class is intended for lithography, device, product, tapeout, design engineers, and managers who need specific knowledge of OPC & DFM implementation techniques, concepts and issues. The course will be of value to those who develop lithographic processes, implement OPC, or have their designs OPC'd.

INSTRUCTORS

Luigi Capodieci received his doctorate in Electronic Engineering and Computer Science from the University of Bologna, Italy in 1988, and a Ph.D. in Electrical Engineering in 1996, from the University of Wisconsin-Madison, where he worked at the Center for X-Ray Lithography (now Center for Nanotechnology). Dr. Capodieci joined the Advanced Process Development group at Advanced Micro Devices in Sunnyvale, California, in 1996, working on Optical Proximity Correction, Phase Shift Masks, imaging simulations and lithography R&D. At AMD he pioneered the field of Design For Manufacturability (DFM) merging physical design practices with rigorous printability modeling. He is now a Senior Member of Technical Staff at AMD, coordinating the OPC and DFM development for the 65nm Technology Node.

Kevin Lucas joined Motorola Semiconductor in Austin, TX in 1994 after completing his Ph.D. in Electrical & Computer Engineering from Carnegie Mellon Univ. He led Motorola's lithography simulation work and started the internal programs in Optical Proximity Correction (OPC) and lithographic design rules. In 2000, he was an assignee at IMEC working on model-based OPC for the 90nm generation. From 2003-2006 he was an assignee to the Motorola/Freescale-Philips-ST Alliance in Crolles, France coordinating lithography/RET-design rules and RET QA/verification. He is currently with Synopsys in Austin, TX managing a team focused on future RET/DFM applications.

Photomask Fabrication and Technology Basics

SC579

Course level: Introductory
CEU .65 $460 / $545 USD
Monday 8:30 am to 5:30 pm

This course provides attendees with a working knowledge of photomask technology. The course focuses on process flow with emphasis in the challenges associated with design data conversions, lithography, process, metrology, inspection, and advanced mask manufacture. Other topics such as the application of SPC, signature matching, Phase Shifting Masks, and Imprint Templates will also be covered.

LEARNING OUTCOMES

This course will enable you to:

- have an understanding and appreciation of mask making and how it differs from wafer process
- understand mask specification and its impact
- comprehend the constraints and impact of design conversion and replication on the mask
- compare the benefits of various mask writing tools and their respective writing strategies
- identify potential challenges in current and future design, lithography, and metrology strategies

INTENDED AUDIENCE

This material is intended for anyone who needs to learn about mask making and its impact in the microlithography process. As there is a focus on design data conversion and its impact, those who work with advanced semiconductor designs or deal with mask specification will find this course valuable.

INSTRUCTOR

John Duff has been involved in the photomask industry in an engineering/R&D capacity for over 20 years. His focus has been on design database conversion, e-beam and laser lithography, metrology, SPC, inspection, and design for manufacturability. John received his B.Sc. from Glasgow University, Glasgow, Scotland, and has worked with Texas Instruments, Toppan, Photronics, and Molecular Imprints. He has been responsible for managing technical programs for various companies and research establishments. John is an ISO Certified Lead Assessor.

The Limits of Optical Lithography

SC723

Course level: Advanced
CEU .35 $280 / $325 USD
Monday 8:30 am to 12:30 pm

Over the past decade, optical lithography has remained at the forefront of the patterning of ICs in spite of the ever decreasing feature sizes required. Incremental improvements of the optical systems in combination with the use of resolution enhancement techniques (RET) have made this transition possible. The implementation of some of these techniques has lead to major infrastructure adjustments and changes covering a wide spectrum of fields including the EDA industry, the photo-mask industry, and the semiconductor equipment industry.

This course will explain the fundamental limits of optical lithography from a theoretical standpoint including the description of partially coherent imaging as well as polarization and aberration effects on the imaging quality. Commonly used resolution enhancement techniques such as off-axis illumination, phase-shifting mask, and proximity effect correction will be explained and their practical implementation will be reviewed. This course is the first part of a two part sequence but each part can be taken separately.

LEARNING OUTCOMES

This course will enable you to:

- describe partially coherent imaging, vector model, polarization and aberration effects as well as mask 3D effects
- list the benefits and limitations of resolution enhancement techniques like off-axis illumination, phase-shifting mask (alternating, attenuating, chromeless), optical proximity effect correction (OPC)
- explain the infrastructure changes required for using resolution enhancement techniques in production and their implication on data conversion, photo mask manufacturing and photo lithography processing
- explain the theory and practical ways of optimizing the illumination conditions and the mask layout for a given resolution enhancement technique

INTENDED AUDIENCE

The course is intended for those involved in the semiconductor lithography business, including but not limited to engineers, scientists, and technicians.

INSTRUCTOR

Christophe Pierrat is the director of Research and Development at the Advanced Mask Technology Center (AMTC), a joint venture between AMD, Infineon, and Toppan Photomasks. With his experience at AT&T Bell Laboratories, Micron Technologies, Numerical Technologies and Takumi, Dr. Pierrat provides comprehensive solutions to lithography issues covering the fields of data conversion, photo-mask manufacturing, and lithography. He has authored over 30 technical papers and over 100 patents in the field.

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Optical Lithography Extension: Design for Manufacturing and New Resolution Enhancement Techniques

SC724

Course level: Advanced
CEU .35 $280 / $325 USD
Monday 1:30 to 5:30 pm

Optical lithography has been extended through the use of resolution enhancement techniques (RET) like off-axis illumination, phase-shifting mask, and proximity effect correction. As these techniques reach their limits, their practical implementation becomes more dubious and requires a careful consideration of their use at the design phase in order to achieve sufficient yields.

Recently the field of design for manufacturing (DFM) has enjoyed a large success in part because of the poor ramp-up of the latest technology nodes due to limited process latitude at low k1.

At the same time, the industry is looking for new ways to improve the resolution and the process latitude on the wafer by using new resolution enhancement techniques going beyond the established techniques (off-axis illumination, phase-shifting mask, and proximity effect correction). These new techniques include immersion lithography, the use of polarized sources, or the use of multiple exposures.

This course will describe the most relevant design for manufacturing techniques and their practical implementation. The fundamentals of the new resolution enhancement techniques will also be explained and their implementation will be discussed. This course is the second part of a two part sequence but each part can be taken separately.

LEARNING OUTCOMES

This course will enable you to:

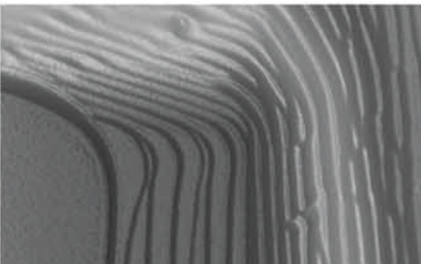
- describe design for manufacturing techniques and their implementation including the concepts of lithography-friendly designs and manufacturability check at the design phase
- use design intent information in order to speed up OPC and mask data preparation as well as reduce mask complexity and cost
- list the benefits and limitations of new resolution enhancement techniques like immersion lithography, polarized illumination, and multiple exposures
- describe the infrastructure changes required for these new resolution enhancement techniques to be transferred to production
- explore more exotic resolution enhancement techniques that might be implemented in the future

INTENDED AUDIENCE

The course is intended for those involved in the semiconductor lithography business, including but not limited to engineers, scientists, and technicians.

INSTRUCTOR

Christophe Pierrat is the director of Research and Development at the Advanced Mask Technology Center (AMTC), a joint venture between AMD, Infineon, and Toppan Photomasks. With his experience at AT&T Bell Laboratories, Micron Technologies, Numerical Technologies and Takumi, Dr. Pierrat provides comprehensive solutions to lithography issues covering the fields of data conversion, photo-mask manufacturing, and lithography. He has authored over 30 technical papers and over 100 patents in the field.



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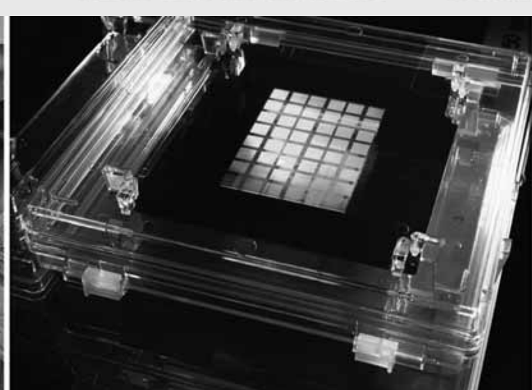

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Photomask Technology 2007

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6730-01, Session 1

Collaboration, Innovation, and Execution: Three Keys to Premium Customer Experience

R. P. Wallace, KLA-Tencor Corp.

Abstract not Available

6730-02, Session 1

Mask Industry Assessment: 2007

G. V. Shelden, Shelden Consulting; P. Marmillion, SEMATECH, Inc.

Microelectronics industry leaders routinely name the cost and cycle time of mask technology and mask supply as top critical issues. A survey was created with support from SEMATECH and administered by SEMI North America to gather information about the mask industry as an objective assessment of its overall condition. The survey is designed with the input of semiconductor company mask technologists, merchant mask suppliers and industry equipment makers. This year's assessment is the sixth in the current series of annual reports. With continued industry support the report can be used as a baseline to gain perspective on the technical and business status of the mask and microelectronics industries. The report will continue to serve as a valuable reference to identify the strengths and opportunities of the mask industry. The results will be used to guide future investments on critical path issues. This year's survey is basically the same as the 2006 survey. Questions are grouped into categories: General Business Profile Information, Data Processing, Yields and Yield Loss Mechanisms, Delivery Times, Returns and Services, Operating Cost Factors, and Equipment Utilization. Within each category is a multitude of questions that create a detailed profile of both the business and technical status of the critical mask industry.

6730-03, Session 1

EMCL 2007 Best Paper: Predicting and correcting for image placement errors during the fabrication of EUVL masks

R. L. Engelstad, K. T. Turner, J. Sohn, A. R. Mikkelson, M. Nataraju, Univ. of Wisconsin/Madison

Abstract not Available

6730-04, Session 1

PMJ 2007 Best Paper: Alternating phase-shift mask and binary mask for 45-nm node and beyond: the impact on the mask error control

Y. Kojima, M. Shirasaki, K. Chiba, Toppan Printing Co., Ltd. (Japan); T. Tanaka, Toppan Printing Co., Ltd.; K. Iwase, Sony Atsugi Technology Ctr. (Japan); K. Ishikawa, Sony Corp. (Japan); K. Ozawa, Sony Atsugi Technology Ctr. (Japan); Y. Inazuki, H. Yoshikawa, S. Okazaki, Shin-Etsu Chemical Co., Ltd. (Japan)

Abstract not available

6730-05, Session 1

PMJ Panel Discussion Overview: double exposure and double patterning for 32-nm half-pitch design node

Y. Nagaoka, KLA-Tencor Japan Ltd. (Japan); H. Watanabe, Toshiba Semiconductor Co. (Japan)

The technologies on immersion lithography are extensively studied and are intensely used for the leading edge LSIs in these years. The 45nm half pitch technology node is surely in the scope of 193nm ArF immersion lithography.

The limit of resolution by the lithography of single exposure with the theoretically maximum N.A. of 1.4+ for DIW is thirty some (35-40)nm in half pitch. We can improve the resolution twice by the techniques of double exposure and of double patterning in simple minded estimation. By the estimation, the ArF immersion lithography with double exposure and double patterning techniques shall be available in the 32nm half pitch technology node.

We took a panel discussed on "Double Exposure and Double Patterning for 32nm half-pitch Design Node" with the panelists of Rik Jonckheere, IMEC (Belgium), Tsann-Bim Chiou, ASML Taiwan Ltd. (Taiwan), Yoshimitsu Okuda, Toppan Printing Co. Ltd. (Japan) and Judy Huckabay, Cadence Design Systems, Inc. (USA) place in PMJ2007, held at Yokohama Japan on April 18, 2007.

By the talks of panelists, we recognized; the difficulties of the technology in the process steps in LSI fabrication, in the error of overlay brought about by lithography tools and in photomasks and EDA of data splitting without data conflict are predicting issues which we shall take into account. On photomasks, less than 4nm three times sigma CD variation and less than 6nm three times sigma deviation in pattern placement are required.

These difficulties are big challenge for both LSI and photomask engineering, however, we have confirmed some solutions are already examine by the theoretical and experimental works of the people in research on the technology. Despite of the above difficulties, we are convinced that the immersion lithography with double exposure and double patterning techniques is one of the mostly promising candidates of the lithography for 32nm half pitch LSIs.

Besides reporting the discussion on the technology of double exposure and double patterning, we will also report the opinions from the attendee of the conference on the technology obtained by the questionnaire on the technology.

6730-06, Session 2

Characterizing photomask etch processes through phase component analysis

R. E. Wistrom, IBM Corp.; M. S. Hibbs, IBM Microelectronics Div.; T. Komizo, Toppan Electronics, Inc.; G. Reid, IBM Corp.

One of the most important parameters of attenuated phase shift (att PSM) masks is the uniformity of the phase over the active area of the mask. Phase uniformity is an important component of lithographic process window stability. Typically, an Attenuated Phase Shift Mask (APSM) blank consists of a quartz substrate upon which a Molybdenum Silicide (MoSi) attenuating film and a Chromium (Cr) film has been deposited to act as a hard mask for the MoSi etch. There are many factors that contribute to phase non-uniformity of the final mask: thickness non-uniformity of the films, non-uniformity of the Cr etch and MoSi etch, and non-uniformity of the MoSi overetch into the quartz substrate. Phase non-uniformity of a completed mask is routinely measured, but quantifying how these individual components contribute to the overall non-uniformity is more difficult. This report focuses on understanding how MoSi etch contributes to phase non-uniformity. Phase uniformity is compared for three different MoSi etch processes.

6730-07, Session 2

The advanced mask CD MTT control using dry etch process for sub-65-nm technology

S. J. Jo, H. Y. Jung, D. W. Lee, J. Y. Jun, T. Ha, O. Han, Hynix Semiconductor Inc. (South Korea)

As the design rule of the semiconductor circuit shrinks, the specification for photomask becomes tighter. So, more precise control of CD MTT (Critical Dimension Mean to Target) is required. We investigated the CD MTT control of the attenuated PSM (Phase Shift Mask) by additional Cr dry etch. In conventional process, it is difficult to control CD MTT precisely because about 5 factors - Blank Mask, E-beam writing, Resist develop, Cr dry etch, MoSiN dry etch - affect CD MTT error. We designed the new process to control CD MTT precisely. The basic concept of the new process is to reduce the number of factors which affect the CD MTT error. To correct CD MTT error in the new process, we measured CD before MoSiN dry etch, and then additional corrective Cr dry etch and MoSiN dry etch was performed. So, the factors affecting CD MTT error are reduced to 2 steps, which is additional corrective Cr dry etch and MoSiN dry etch. The reliability of CD measurement before MoSiN dry etch was evaluated. The generable side-effect of the additional corrective Cr dry etch was analyzed. The relationship between'CD shift'and'additional corrective Cr etch time'was found for various patterns. As a result, accurate CD MTT control and significant decrease of CD MTT error for attenuated PSM is achieved.

6730-08, Session 2

Hardmask etch process for next-generation photomask fabrication beyond 32-nm technology node

P. Qu, C. Choi, K. Baik, S. Park, Intel Corp.

As the minimum feature size decreases in mask fabrication processes, pattern resolution becomes one of most critical factors to determine the success of next generation mask technology. In addition, due to tighter requirements on mask etch bias and Cr loading effect, hardmask with thin resist system is considered as one of the primary paths in mask making technology of 32nm node or below. In this paper, etch selectivity, etch profile, and loading effect of several hardmask materials were investigated. Thin resist used in the hardmask process improved the process window without pattern collapse. Cr etch process was adjusted to improve etch profile and critical dimension (CD) bias for very small features. The etch profiles with hardmask were also compared to conventional Cr etch with photoresist mask. As a result, it was demonstrated that hardmask could enable to deliver better CD performance which would be required in next generation mask fabrication of 32nm node or below.

6730-09, Session 2

CD bias control with in-situ plasma treatment in EPSM photomask etch

K. Yung, C. Choi, K. Baik, Intel Corp.

As mask feature size decreases, etch bias control during Cr and shifter etch becomes more critical factor in Embedded Phase Shifter Mask (EPSM) mask making processes. Since the etching characteristics of the shifter materials, Molybdenum Silicide (MoSi), are sensitive to etching surface condition, Critical Dimension (CD) performance of the shifter layer strongly depends on incoming surface condition from Cr etch. In this paper, lateral etch component of MoSi etch was investigated as a function of various substrate conditions so that a new in-situ plasma treatment was suggested to control the CD bias during MoSi etch. The CD performance was characterized within the surface treatment plasmas and also correlated with some plasma parameters and substrate temperature. As a result, it was found that plasma surface modification could be an in-situ technique to better control the shifter CD in EPSM process and an essential option for redundancy tools in mask production environment.

6730-10, Session 3

Effects of exposure environment on pellicle degradation in ArF lithography

H. Choi, Y. Ahn, J. Ryu, Y. Lee, Y. Cho, J. Kim, SAMSUNG Electronics Co., Ltd. (South Korea)

In ArF lithography era, photo-induced defects such as haze problem and pellicle degradation have more negative effects to the photomask quality and productivity than in former generation of lithography such as KrF lithography. Due to its high intensity energy, ArF laser accelerates photochemical reactions generating a non-organic crystal defect called as haze, so that it makes a cleaning cycle of photomask quite short. Moreover, high energy of ArF laser affects pellicle degradation in direct because C, F, O single bonding energy composing ArF pellicle film is quite smaller than ArF laser energy. In order to resolve these inevitable problems, dry gas purge method has been investigated by many researchers in academic and business world.

Dry gas purge method is usually applied to two phase. First, it can be used to a storage environment such as reticle stocker, reticle SMIF pod and reticle library in scanner. In this manner, a dry gas will be filled in space between reticle and pellicle, so that various airborne molecular contaminations and humidity can be eliminated from a storage phase not to affect a generation of haze. Second, dry gas purge is applied to exposure chamber inside a scanner at exposure phase. This method is more effective to eliminate AMCs and humidity than a storage purge because a dry gas participates in a photochemical reaction in direct to decrease an efficiency of photochemical reaction.

In general, two gases are applied to a dry gas purge method, those are nitrogen and CDA (clean dry air). In this study, an experimental method has been focused on exposure phase and especially the experiments of pellicle degradation according to the type of dry gas, nitrogen or CDA, have been performed. The chamber of ArF laser exposure apparatus has been purged by nitrogen and CDA respectively. The reticle mounted with ArF pellicle was loaded to confirm how much the thickness of pellicle decreased due to a damage in each dry gas environment during ArF laser exposure. To compare the effect of dry gas purge with that of a normal cleanroom air, the results of ArF laser exposure in a cleanroom air was adopted as a reference. The energy intensity of ArF laser at the reticle level is 2.0mJ/cm2/pulse and its frequency is 200Hz. The total energy of exposure is 800J. The thickness of pellicle after ArF laser exposure is measured using a reflectometer.

In the experimental result, it is confirmed that there is all the difference about the degree of pellicle damage according to dry gas. First, the degradation of pellicle in CDA is weaker than in a normal cleanroom air, reference. Second, the degradation of pellicle in nitrogen is much more severe than the reference. In comparison between CDA and nitrogen, the thickness of pellicle in nitrogen atmosphere is reduced about 10 times faster than in CDA. The reason why the degradation of pellicle in CDA atmosphere is not severe is that oxygen in CDA has effect of curing the surface of pellicle film damaged by ArF laser. On the other hand, there is no factor curing the damage of pellicle in nitrogen atmosphere.

In conclusion, CDA is more appropriate rather than nitrogen when dry gas purge is applied to a reticle stage in direct or a reticle library as storage environment.

6730-11, Session 3

Development and characterization of a new low-stress molybdenum silicide absorber for 45-nm attenuated phase-shift mask manufacturing

T. B. Faure, E. E. Gallagher, IBM Corp.; L. M. Kindt, IBM Microelectronics Div.; S. C. Nash, K. C. Racette, R. E. Wistrom, IBM Corp.; T. Komizo, Toppan Electronics, Inc.; Y. Kikuchi, IBM Burlington; S. Nemoto, Toppan Electronics, Inc.; Y. Sasaki, Toppan Printing Co., Ltd. (Japan); T. Suzuki, M. Ushida, Y. Yokoya, HOYA Corp. (Japan)

As optical lithography is extended for use in manufacturing 45 nm devices, it becomes increasingly important to maximize the lithography process window and enable the largest depth of focus possible at the wafer stepper. Consequently it is very important that the reticles used in the wafer stepper must be as flat as possible. The ITRS roadmap requirement for mask flatness for 45 nm node is 250 nm. To achieve this very tight reticle flatness requirement, the stress of each of the film present on the mask substrate must be minimized. Another key reticle specification influenced by film stress on the mask blank is image placement. The ITRS roadmap requirement for mask image placement for the 45 nm

node is 6 nm. In this paper, we will describe the development and detailed characterization of Hoya's new low stress Molybdenum Silicide (MoSi) film for use in manufacturing 45 nm node critical level attenuated phase shift masks to be used in 193 nm immersion lithography. Data assessing and comparing the cleaning durability, mask flatness, film stress, film composition, image placement, critical dimension (CD) performance, dry etch properties, phase performance, and defect performance of the new low stress MoSi film versus the previous industry standard Hoya A61A higher stress MoSi attenuator film will be presented. Data comparing the key mask CD parameters which affect Optical Proximity Correction (OPC) performance on wafer will be included in detail. The results of our studies indicate that the new low stress MoSi film is suitable for 45 nm mask manufacturing and can be introduced with minimal changes to the mask manufacturing process.

6730-12, Session 3

Evaluation of the effect of mask-blank flatness on CDU and DOF in high-NA system

C. W. Chang, Nanya Technology Corp.

In lithography systems, the need for increased resolution requires larger numerical apertures and shorter illumination wavelengths. Both of these requirements cause a reduction in the system's depth of focus, resulting in the need for tighter mask blank flatness specifications to fit the next generation requirement.

Moreover, the non-flatness of the mask patterned surface will manifest itself as image placement errors on the device wafer. Mask blank and finished mask flatness are becoming more serious concerns for mask fabrication.

The experiment involves using three masks of different type, 0.3T, 0.5T, and 1T. Mask flatness data is from all mask fabrication process each steps measured directly by Tropel UltraFlat200 Mask Metrology Instrument. The pattern is using patterns of DRAM 58 nm generation that is more critical among all of lithography process and is exposed by 193nm ArF scanner. Then, the effect of mask blank flatness on CD uniformity and depth of focus of wafer print are verified.

6730-13, Session 4

The development of full-field high-resolution imprint templates

S. Yoshitake, H. Sunaoshi, K. Yasui, NuFlare Technology, Inc. (Japan); D. J. Resnick, G. M. Schmid, E. Thompson, Molecular Imprints, Inc.; O. Nagarekawa, H. Kobayashi, T. Sato, HOYA Corp. (Japan)

Small feature imprint lithography has existed for several years. The original technique involved the use of a patterned template which is impressed onto a thermo plastic material and, with the combination of heat and pressure, the pattern in the template was transferred to the substrate. Compact disks were one of the early applications for the technology. Recently the technique has been significantly improved with the development of Step and Flash Imprint Lithography (S-FIL™).1 This technique involves deposition of a low viscosity monomer on the substrate, lowering a template into the fluid which then flows into the patterns of the template. Following this fill step, the monomer is exposed to UV light to cross-link it and convert it into a solid, and the template is removed leaving the solid pattern on the substrate.2 The advantages of this development make it uniquely capable for CMOS applications.

Critical to the success of the technology is the manufacturing 1X templates. Several commercial mask shops now accept orders for 1X templates. Recently, there have been several publications addressing the fabrication of templates with 32nm and sub 32nm half pitch dimensions using high resolution Gaussian beam pattern generators.3,4 Currently, these systems are very useful for unit process development and device prototyping. In this paper, we address the progress made towards full field templates suitable for the fabrication of CMOS circuits.

The starting photoplate consisted of a Cr hard mask (< 15nm) followed by a thin imaging layer of ZEP 520A. The EBM-5000 and the EBM-6000 variable shape beam pattern generators from NuFlare Technology were used to pattern the images on the substrates. Several key specifications of the EBM-6000, resulting in improved performance over the EBM-5000 include higher current density (70 A/cm2), astigmatism correction in the subfields, optimized variable stage speed control, and improved data handling to increase the maximum shot count limitation.

To fabricate the template, the patterned resist serves as an etch mask for the thin Cr film. The Cr, in turn, is used as an etch block for the fused silica. A mesa is formed by etching the non-active areas using a wet buffered oxide etch (BOE) solution. The final step in the template process is a dice and polish step used to separate the plate into four distinct templates.

Key steps in the fabrication process include the imaging and pattern processes. ZEP520A was chosen as the e-beam resist for its ability to resolve high resolution images. Although ZEP520A is slow relative to chemically amplified e-beam resists, it is only necessary to pattern 1/16th the area relative to a 4X reduction mask. Figure 1 depicts Metal1 and contact patterns resolved in the resist, demonstrating resolution well below 40nm. In addition to resolution, image placement requirements are tighter for a 1X template than for a comparable 4X mask. Figure 2 shows results for a 1X template after exposure for a 26 mm x 32 mm field. After correction, the maximum 3 values were less than 4nm. Other topics to be discussed include pattern transfer, write time, and CD uniformity, and imprint quality.

1. Colburn, et al., Proc. SPIE Int. Symp. on Microlithography, Vol. 3676, pp. 379-389, March 1999.

2. M. Bender et al., Microelectronic Engineering, 61- 62 (2002), pp. 407-413.

3. D. J. Resnick, et al., Proc. SPIE, Vol. 6517, in Press, 2007.

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6730-14, Session 4

Defect reduction progress in step and flash imprint lithography

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Despite the remarkable progress made in the past decade in extending optical lithography to deep sub-wavelength imaging, the limit for the technology seems to be fast approaching. At 22nm half pitch design rules, neither very high NA tools (NA 1.6), nor techniques such as double patterning, are likely to be sufficient. The extension of photon based systems to EUV remains very challenging, and this has opened up the opportunity for imprint lithography as a viable NGL alternative. There is accelerating interest in S-FILTM (Step and Flash imprint lithography(r)) in particular, as an NGL solution. The advantages of a drop on demand imprint make it uniquely capable for CMOS applications.

Key to the development of any NGL alternative is progress in resolution, overlay, and defect control. Recent work has demonstrated that templates can be fabricated with half pitch features as small as 21nm. Overlay results of better than 20nm 3 across an entire 200mm wafer have also been demonstrated. However, it is well understood that the commercial viability of a production process also depends on limiting the accumulation of defects. Acceptance of imprint lithography for CMOS manufacturing will require demonstration that it can attain defect levels commensurate with the requirements of cost-effective device production. In this paper, the progress in defect reduction is reviewed in detail.

The defect reduction in the imprint process over the course of the last three years is depicted in Figure 1. Metal 1 and Contact patterns printed on 200mm wafers, using both an Imprio I100 and an Imprio I250, were inspected at a minimum pixel setting of 200nm using a KLA-Tencor 2132 system. Minimum feature size was 350nm in order to avoid false defect detection on the inspection tool. Defect densities have been reduced by nearly four orders of magnitude over the three years. Key contributors to the reduction include: improved monomers, improved adhesion layers, clean starting wafers, and high quality low defect templates from commercial suppliers.

The improvements in template defectivity continue to drive imprint defectivity lower and the effect is noted in Figures 2 and 3. Figure 2 shows total defects on a newly designed template at three different stages

of the fabrication process as detected with a KLA-T 5xx tool: first level patterning in Cr and quartz, the creation of the pedestal, and the final imprint surface after Cr strip. Defect counts are low in all cases, typically remaining below four. For one template, the defect count was zero for each inspection stage. It should be noted that no attempt was made at repair to further reduce defectivity. One template was then imprinted and a defect density summary from the 68 fields printed on the wafer is shown in Figure 3. The average defect density was 1.6 defects/cm2. Major contributors to the defect count include a repeating defect and various random defects. Details of the template and imprint process, sources for defects, and detection of smaller defects using electron beam inspection will also be discussed.

6730-15, Session 4

Fabrication of nano-imprint templates for dual-Damascene applications using a high-resolution variable shape e-beam writer

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There are an increasing number of UV Nano Imprint Lithography (UV-NIL) applications like fabrication of patterned media, photonic crystals or LEDs [1]. In addition, consortia in Europe, Asia and North America are evaluating this promising technology for the CMOS production at the 32nm node and below. For example, patterning of contact holes is addressed as a first target. Especially beneficial and cost effective appears the application of the UV-NIL when applying for the Dual Damascene technology. Combined with a UV printable low-k material the UV Nano Imprint Lithography can dramatically simplify this process [2]. After imprinting of vias and metal lines at once and a subsequent clearing of the remaining low-k material in the vias, the Cu metallization will be done followed by the final CMP process.

Of course, one challenge for this approach is the manufacturing of the corresponding 3D template with high resolution, high complex features and a precise overlay between the two tiers via and metal. While imprinting in resist requires quartz etch depths of around 100-150nm the direct patterning of the dielectric needs the full feature height in each layer. This size depends on the tier and the technology and is expected to be in the range of 150 to 500nm.

We developed a 3D template process which enables the generation of high resolution, high aspect pillars on top of the later metal lines. Because of the complexity of state of the art CMOS designs we considered only a variable shape e-beam (VSB) writer combined with chemically amplified resists (CAR) for the patterning process. The VSB writer Vistec SB352HR equipped with Vistec's latest column design especially developed for the high resolution approach and targeting the 32nm node, was available for the e-beam exposure.

We focussed our work especially on the generation of high aspect pillars with a diameter below 50nm and the development of suitable overlay strategies for getting a precise alignment in between the two template tiers. In this context we investigated the influence of exposure strategies, alignment marks and conductive top coats on the overlay result and investigated them across the entire imprint area of 25mm x 25mm.

Finally, we realized templates according to the MII standard with real CMOS designs and confirmed their printability on a MII tool.

[1] Mark Melliar-Smith, "Lithography beyond 32nm: a role for imprint? Plenary presentation SPIE Advanced Lithography Conference, 2007

[2] Susan MacDonald et al., Design and fabrication of highly complex topographic nano-imprint template for dual Damascene full 3-D imprinting, Proc. SPIE Vol. 5992, 59922F

6730-16, Session 5

The study of CD error in mid-local pattern area caused by develop loading effect

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As the design rule has decreased in semiconductor manufacturing, the ITRS roadmap requires significantly tighter critical dimension control. Especially, CD error caused by develop loading become significant in the overall error budget and has approached to over 5nm. It is very difficult to control dissolution product making the change of dissolution rate by chemical flow direction in develop process.

These days, the study of develop loading within global area has significantly progressed. However, we will focus on CD error in mid-local area by using a detailed analysis. And we evaluate these phenomenon caused by pattern density difference, called chemical flare. Even though using several developer types, CD error appears at the chip to chip boundary. It is impossible to correct CD error in this area by electron beam correction. Therefore, this paper analyzed about CD error in a value of several tens ~ hundreds nm. In view of develop loading, we will optimize develop process for improvement of CD error.

6730-17, Session 5

Performance improvement of ALTA4700 for 130-nm and below mask productivity

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Chemically amplified resist Fuji FEP171 resist is widely used in advance technology mask manufacturing. Chemically amplified resist dependent upon a two step mechanism to achieve patterning in the resist film. First, exposure to UV radiation or e-beam causes a photoacid generator to produce photoacid within the film. Second, the generated photoacid catalyzes a thermal deprotection reaction that render the resist matrix polymer soluble in an aqueous developer. In the second step, post-exposure baking (PEB) is applied to overcome activation energy of the deprotection reaction. Because of patterning mechanism is heavily dependent upon the presence of photoacid and the deprotection reaction within resist, the proper post-exposure baking temperature should be addressed.

In our previous paper, the ALTA4700 capability in 130nm mask making is demonstrated. Currently, ALTA4700 was using the same FEP171 resist which was using on e-beam writer system with the similar PEB, develop and dry etching. The performance of global CD uniformity is about 6nm (3), local CD uniformity is 4.5nm (3), CD linearity is 8.5nm. Therefore, we try to find out the best process window for ALTA4700/FEP171 and improve the CD performance, and then ALTA4700 is capable to meet the state-of-the-art mask specification.

6730-18, Session 5

The behavior of substrate dependency as surface treatment in the positive chemically amplified resist coated blanks

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Positive chemically amplified resist (PCAR) is using widely because of its benefit of high resolution in the semiconductor industry. But many studies have been reporting that resist pattern error such as resist scum and adhesion fail at the interface between substrate and PCAR is caused by the substrate dependency. Hence resist pattern error must be minimized so we observed the phenomena at the PCAR coated blanks. And then we applied various surface treatment methods to the Cr film to minimize resist pattern error in this study.

Firstly resist pattern error was occurred by the substrate dependency in the PCAR coated blanks. And we investigated the root cause of pattern error so could find that nitrogen in the Cr film behaves as lewis acid and that could combine with proton in the PCAR easily. So we used various surface treatments to minimize the detrimental effects of substrate dependency to the PCAR. And we observed the behavior of substrate dependency after etch process by various analyses to verify the effect of surface treatment method. The results showed that substrate dependency could be controlled by surface treatment in the PCAR coated blanks.

6730-19, Session 5

Design for CD correction strategy using a resist shrink method via UV irradiation for defect-free photomask

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As the specification for photomask becomes tighter, it is strongly demanded for achieving precise CD MTT (critical dimension mean to target) and enhanced defect controllability in photomask fabrication. First of all, it is necessary that reducing the factors of CD MTT error and introducing the reliable method to correct CD error for accurate CD requirement of attenuated PSM (phase shift mask). From this point of view, one of CD correction methods which consist of Cr CD measurement step after resist strip (strip inspection CD: SI CD) and additional corrective Cr dry etch step was developed. Previous SI CD correction process resulted in accurate CD control within the range of CD MTT. However it was not appropriate for defect control due to additional resist processes for selective protection of Cr pattern during CD correction process.

In this study, the method for achieving precise CD MTT by correcting CD error without any resist process is investigated. It is not suitable for the CD correction process to control CD MTT precisely that Cr etched resist (etch inspection CD: EI CD) is very vulnerable to E-beam scanning during CD measurement. Otherwise, photoresist after Cr etch selectively shrinks via UV irradiation under ozone (O3) condition, which drives a reduction of CD MTT error as a result of accurate CD measurement (UV-irradiation inspection CD: UI CD). Moreover, it is not necessary any resist process for Cr protection due to UV irradiated resist as enough for a etch barrier. It is a strong advantage of novel CD correction method. This strategy solves the problems such as both CD measurement error on the EI CD correction method and defects originated from resist process on the SI CD correction method at once. For the successful incorporation of UI CD correction method, several items related with CD should be evaluated: accuracy and repeatability of CD measurement under UI CD, control of CD MTT and CD uniformity, additional corrective etch bias for UI CD, independence of corrective Cr etch process from UV irradiated resist, isolated-dense CD difference,.. etc. In this paper, strategy of design for the progressive CD correction method for defect-free photomask and process details will be discussed.

6730-20, Session 5

The impact of mask photoresist develop on critical dimension parameters

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As the tolerances for photomask Critical Dimension (CD) become smaller, more focus has been placed on all processes and their contribution to final mask CD. One key contributor to final mask feature dimensions is the resist develop process and it is the focus of this work. We have studied different resist develop methods to determine optimum process conditions for 45 nm critical photomasks. In searching for the optimum conditions, special consideration was made to study the influence of pattern density effects. We focused on variations in develop nozzle and developer concentration. Results of their impact on pattern density and long range pattern density effects will be presented, for both positive and negative chemically-amplified resists.

6730-21, Session 6

New method of contour-based mask-shape compiler

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We have developed a highly precise contouring technique for the mask shape that is used for semiconductor manufacture.

Currently, as semiconductor manufacture moves towards even smaller feature size, this necessitates more aggressive optical proximity correction (OPC) to drive the super-resolution technology (RET).

On the other hand, from the DFM perspective, dramatic increase in data processing cost associated with more refined MDP, which in turn drives the cost for mask manufacture sky-high has become a serious issue.

In other words, there is a trade-off between highly precise RET and mask manufacture, and this has a big impact on the semiconductor market that centers on the mask business.

As an optimal solution to these issues, we provide a DFM solution that extracts 2-dimensional data for a more realistic and error-free simulation by reproducing accurately the contour of the actual mask, in addition to the simulation results from the mask data.

The principal part of this system consists of the following three points.

1. Automatic generation of design-based recipe: Specify the pattern set as the object of a model calibration in the design data.

This operation interfaces with the coordinates information of the HotSpot detected from an OPC simulation, and is fully automated.

2. Image measurement in the Design base: The measurement image based on the recipe of a Design base is acquired automatically. The automation is highly robust, since the image acquisition is performed by a proactive approach using a large range of the Design.

3. Generation of contouring and GDS data: For the above results, contouring processing is done for the acquired image using a metrology algorithm that is based on a image profiling system with high fidelity. This processing is capable of edge detection of sub-pixel order, and accuracy in sub-nanometer can be realized. And, by generating these edge detection as a GDS format in the form of design data, it is possible to mediate between highly precise outline information to various EDA systems including simulation.

Going by the above-mentioned flow, full automation is achieved as everything is centered on the Design data.

With this, an optimization and verification environment for full automation of model calibration is provided.

Moreover, complete unification with an EDA system is realized for input and an output by considering it as a Design data oriented system configuration.

And this technology covers a bridge between a chip fabrication factory and a designer's EAD system.

From these, this technique is a strategic DFM approach in the field of measurement technique for semiconductor.

6730-23, Session 6

Development of mask-DFM system MiLE: load estimation of mask manufacturing

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Load of photomask manufacturing for the most advanced semiconductor devices is increasing due to complexity of mask layouts caused by highly accurate RET or OPC, tight specification for 2D/3D mask structures, requirements of quick deliveries. The mask cost becomes a concern of mask customers especially in SoC businesses, because number of the masks required throughout the wafer process is almost same in each product regardless of the variety of production volume when a unified platform is applied to the designs. Shares of mask cost within total production cost cannot be ignored especially in small volume SoC products.

DFM (design for manufacturing) is inevitable in a mask level as well as in a wafer level to solve the cost problem. "Mask-DFM" is a method to decrease difficulties of mask manufacturing and to improve yield and quality of masks, by not only modification of mask pattern layouts (design) but also all other things including utilization of designer's intents. We develop our Mask-DFM system called "MiLE", that calculates load of mask manufacturing through layout analyses combining information of mask configuration and visualizes the consequence of Mask-DFM efforts.

"MiLE (Mask manufacturIng Load Estimation)" calculates a relative index which represents load of mask manufacturing determined by fac-

tors of 1) EB writing, 2) defect inspection/repair, 3) materials and processes and 4) specification. All the factors are computed before tape-outs for mask making by the following methods in the system. To estimate EB writing time, we applied high-throughput simulator and counted a number of "shot", minimum figure unit in EB writing, by using post-OPC layout data. Mask layout that caused troubles and extra load in mask inspection or repair was specified from MRC (mask rule checking) of the same post-OPC data. Additional layout analysis perceives designer's intents that are described in the layout data and reflects them to calculation of the "MiLE" index. Finally, chip arrangement on a mask is retrieved from so-called electronic mask spec sheets to complete whole mask layout analyses.

"MiLE" notifies designers of the index of mask manufacturability, which is fluctuated by mask layout and specification when modification and adjustments of design or OPC are iterated to maximize device productivity in early design phases. Therefore, designers can judge and control the mask manufacturability, or mask cost by designs and additional intents useful for mask making. In production phases, the system releases useful information for mask manufacturing to a mask shop and decreases load of mask manufacturing. In this paper, we report outline and functions of MiLE system and results of mask manufacturability calculation using post-OPC layout data.

6730-24, Session 6

DFM: design-aware flexible mask-defect analysis

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We present a novel software system that combines design intent as known by EDA designers with defect inspection results from the maskshop to analyze the severeness of defects on photomasks. The software -named Takumi Design-Driven Defect Analyzer (TKD3A)- analyzes defects by combining actions in the image domain with actions in the design domain and outputs amongst others flexible mask-repair decisions in production formats used by the maskshop. Furthermore, TKD3A outputs clips of layout (GDS/OASIS) that can be viewed with its graphical user interface for easy review of the defects and associated repair decisions. As inputs the system uses reticle defect-inspection data and the respective multi-layer design layouts with the definition of criticalities.

The system does not require confidential design data from IDM, Fabless Design House, or Foundry to be sent to the maskshop and it also has minimum impact on the maskshop's mode of operation. The output of TKD3A is designed to realize value to the maskshop and its customers in the forms of:

1) improved yield,

2) reduction of delivery times of masks to customers, and

3) enhanced utilization of the maskshop's installed tool base.

The system was qualified together with a major IDM on a large set of production reticles in the 90 and beyond 65 nm technology nodes of which results will be presented that show the benefits for maskmaking. The accuracy in detecting defects is extremely high. We show the system's capability to analyze defects well below the pixel resolution of all inspection tools used, as well as the capability to extract multiple types of transmission defects. All these defects are analyzed design-criticality-aware by TKD3A, resulting in a large fraction of defects that do not need to be repaired because they are located in non-critical or less-critical parts of the layout, or, more importantly, turn out to be repairable or neglectable despite of originally being classified as unrepairable. Finally, we show that the runtimes of TKD3A are relatively short, despite the fact that the system operates on large designs.

6730-25, Session 6

Use of layout automation and design-based metrology for defect test mask design and verification

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Traditionally there have been two types of inspection test masks. On one hand we have those that have defects placed on ideal layouts (iso/dense, no-OPC) on a specific grid and are used to quantify the defect capture rate of the inspection tool at some specific settings. On the other hand we have masks that are either product or product-like layouts which are used to test the "runability" of the inspection tool (i.e., the rate of false defect identification) at the same settings.

This paper describes the design of a test mask that can serve both purposes. A contact level mask was built from layout clips from real devices and with the actual OPC treatment for the technology node used to pattern the layout. Programmed defects were placed at specific locations within the post-OPC layout. Extensive simulated printability studies were performed using calibrated OPC models at the exact co-ordinate locations of the defects. From these simulations, and an understanding of the resolution limits of the mask making process, an appropriate range of defect sizes to test both mask inspect-ability and wafer printability was selected.

Furthermore, SEM recipes were automatically created using the defect co-ordinates to support mask and wafer metrology. These wafer data were directly compared to the simulations from the calibrated OPC and also used to identify critical reticle defects that will compromise patterning on the wafer.

We will describe the design methodology and show the correlation between defect detect-ability and the printability based on simulation, AIMS and wafer data and also discuss the extendibility of this approach to other masking layers.

6730-26, Session 7

Intel's AMT enables rapid processing and info-turn for Intel's DFM test chip vehicle

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Transistor dimensions are quickly approaching atomic levels. Metrology is already a challenge. Several new technologies (e.g. scatterometry, bare wafer inspection,) are emerging to keep pace. Litho critical dimensions, registration and pitch are the forefront of the barrier. Variability in these measurements presents an even greater challenge to assess and control. Intel's AMT (Automated Manufacturing Technology) modules have helped overcome many of these limitations. As a matter of fact, Intel's position as an IDM (Integrated Device Manufacturer) company has put the company in a unique position to take full advantage of AMT. The cycle starts from the definition of the test chip vehicle to getting results back from EOL (End of Line) metrology, and feeding adjustments back to process and design constraints. In this paper, we will review how AMT enables optimal design for manufacturing.

The x-chip is Intel's vehicle to optimize product and process specifications and achieve optimal DFM (Design for Manufacturing). Experiments for product design and process designs are embedded within test chip and SRAM cells. Experiment results feed the refinement for both product and process. AMT's tape-in module enables the automated definition of test structures and connections across the x-chip. This module provides a friendly user interface and customizes the CAD interfaces for Intel's speedy definition of the layout. The tape-in module stores Intel's custom layout specifications, and allows the designers to retrieve and analyze the established definitions for troubleshooting. AMT reduces cycle-time to tape-in and maximizes engineering efficiency with several advanced features such as template specifications, batch mode execution, and automated built-in design rule checker. Once the x-chip layout definition is complete, the resulting specs are used to generate the mask and reticle specifications for different layers. Here, AMT's tape-out module enables automated execution of design, reticle and mask validations. Custom configurations are automatically generated as validation recipes.

At this stage, the x-chip is fully defined, validated and has the reticle generated with the required OPC (Optical Proximity Correction). The x-chip enters the manufacturing phase, where it is greeted by AMT's MES (manufacturing execution system) module. MES enables the specification of FAB experiment routes along with any variations on different wa-

fers. AMT's PCS (Process Control Systems) module gets configured with design layout rules and Silicon process targets. These configurations form the basis for control of process variability as the x-chip is manufactured. As AMT's AMHS (Automated material handling system) gently but rapidly carries the x-chip through the different equipment and process steps, PCS manages variability through active monitoring and intelligent control. Intel's PCS systems are pervasively applied to all tools. Advanced APC (Automated Process Control) analytics and models are further applied at critical steps such as in the control of Litho variability. APC helps maintain minimal variability across all operation steps, and pushes towards zero variability at critical junctions. Simultaneously, AMT's Inline yield analysis system enables timely identification of die failures.

As the x-chip exits the processing of all layers, it enters the last phase of TD manufacturing. It enters the phase of electrical test and sort measurements. These measurements are the most critical as they represent the final performance of the x-chip experiments and the resulting design and process manufacturing refinements. The data provides critical clues on successes and performance limitations. AMT's Advanced Device and EOL Yield analysis systems help with the analysis of hundreds of thousands of test parameters. The systems provide intelligent synthesis and help the engineers focus on root cause of transistor and yield limitations. These modules have a sophisticated grid of connections and access to the whole data pipeline from tape-in to front-end device manufacturing, back-end metals, and EOL test data. In a matter of minutes, engineers are able to relate root cause of excursions and anomalies. The issues help point to earlier versions of product specifications and provide key feedback for the next generation of x-chip design and manufacturing. Design and process changes are subsequently made, and the x-chip cycle starts again.

To summarize, we will discuss in this paper AMT's modules that enable rapid and consistent DFM. These modules enable rapid operation and info-turn of Intel's DFM vehicle: x-chip setup, data patterning and validation, product & process modeling and setup, intelligence and control to minimize variability, rapid yield learning, and rapid product design learning.

6730-27, Session 7

From rule to model-based design: a need for DfP criteria ?

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Traditional design rules to ensure device functionality and yield are defined by multiple criteria, divided into two groups. The first group, e.g., the minimum conductor linewidth for current density and isolation spaces for breakdown voltage, is to determine if the device would work electrically assuming it was possible to manufacture it. The second group, covering e.g., mask/litho resolution and overlay tolerances, would ensure that the device is manufacturable to the physical specifications. The underlying business related criterion, whether a device built and functioning to all these requirements would be an economical success is usually not verified directly. While it used to be ensured prior to the launching of technology generation into manufacturing (with mask shops treated as the element of equipment supply), with the fabless detachment of technology from design, the physical aspect of design rules is becoming more flexible. Instead, the tradeoff is developing between the device size as dictated not only by the manufacturing capabilities but increasingly more often by the viability of electrical rules and the business success. The power distribution, variability reduction, testability, functionality, electromagnetic interference, and signal integrity, could become more limiting than the manufacturability and yield issues. In this work we propose a methodology to define a set of design recommendations aimed at device profitability, or DfP. In this methodology, rule-based design would be gradually replaced with a model-based one, which is to also include reticle manufacturability issues. Physical verification should be done using benchmark comparisons rather than a 100% pass criteria.

6730-28, Session 7

Accurate lithography analysis for yield prediction

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New DFM tools appearing on the market hold a promise of assessing parametric and functional yield loss due to lithography effects. The accuracy of underlying models can limit the veracity of results. For example, many lithography effects are extremely non-linear and might be difficult to model. Furthermore, inputs used in calibrating a model can limit its accuracy, and most organizations are challenged to characterize the exact needs of a lithography model at a statistically relevant sampling size. This paper describes how models are tuned for a lithography compliance tool which is being used in production for tapeouts. Technical sources of inaccuracy and impact of such accuracy on DFM analysis are discussed.

After discussing potential sources of inaccuracy in modeling, the paper will describe a methodology for yield prediction based on accurate modeling. Such methodology can quantify feature yield. Actual quantification from such experiments is presented on real foundry data.

6730-29, Session 7

Production-worthy full-chip image-based verification

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At 65nm technology node and below, with the ever-smaller process window, it is no longer sufficient to apply traditional model-based verification at only the nominal condition. Full-chip, full process-window verification has started to integrate into the OPC flow at the 65nm production as a way of preventing potentially weak, post-OPC designs from reaching the mask making step. Through process-window analysis can be done by way of simulating wafer images at each of the corresponding focus and exposure dose condition throughout the process window using an accurate and predictive FEM model. Alternatively, due to the strong correlation between the post-OPC design sensitivity to dose variation and aerial image (AI) quality, the study of through-dose behavior of the post-OPC design can also be carried out by carefully analyzing the AI. These types of analysis can be performed at multiple defocus conditions to assess the robustness of the post-OPC designs with respect to focus and dose variations. In this paper, we study the AI based approach for post-OPC verification in detail.

For metal layer, the primary metrics for verification are bridging, necking, and via coverage. In this paper we are mainly interested in studying bridging and necking. The minimum AI value in the open space gives an indication of its susceptibility to bridging in an over-dosed situation. The lower the minimum intensity, the lesser the risk of bridging. Conversely, the maximum AI between the metal lines provides indication of potential necking issues in an under-dosed situation.

At times, however, in a complex 2D pattern area, the location as to where the AI reaches either maximum or minimum is not obvious. This requires a full-chip, dense image-based approach to fully explore the AI profile of the entire space of the design. We have developed such an algorithm to find the AI maximums and minimums that will bear true relevance to the bridging and necking analysis. In this paper, we apply the full-chip image-based analysis to 65nm metal layers. We demonstrate the capturing of potential bridging or necking issues as identified by the AI analysis. Finally, we show the performance of the full-chip image-based verification.

6730-30, Session 7

Layout verification in the era of process uncertainty: requirements for speed, accuracy, and process portability

J. A. Torres, Mentor Graphics Corp.

A few years ago model-based layout verification was mostly used along mask data preparation as a safety net to prevent limited printability performance prior to mask fabrication. In this manner, if there were layout

locations that would transfer poorly onto the wafer, the mask data was intercepted preventing yield loss associated to “mask issues”. Such mask related issues come primarily from three sources: Mask manufacture bias, OPC limitations and intrinsic layout configurations.

While mask manufacture and OPC limitations can be addressed during the final stages of mask synthesis and manufacture, some layout configurations may exhibit poor lithographic performance for a given process and they cannot be modified without considering the electrical effect such new topologies will induce in the modified layout.

In principle, marginally performing layouts can be removed from the design by adequately interpreting geometric design rules. Unfortunately while such rules are strictly defined for 1D, they are not so for arbitrary 2D configurations. For that reason, several approaches have been pursued to transfer sufficient process information to the layout synthesis tools to prevent the presence of layout configurations incompatible with the production process.

But when the process is not fully developed such approach can potentially limit the portability of the layout. In this paper we list different approaches to define reasonable layout verification targets by exploring methods to reduce verification time, maintain accuracy and improve layout portability.

To reduce verification time, we have implemented a method to quickly scan the layout for large variations without the need to run the actual OPC recipe. This work describes the characteristics of a model that defines a pseudo-OPC process. Because the pseudo-OPC process can not be mapped exactly to the real OPC process there are accuracy limitations when using only the pseudo-OPC process. To overcome these limitations the verification system follows an incremental approach in which those regions previously selected are evaluated with the full mask synthesis recipe to reduce the number of falsely detected errors. Finally to investigate the issue of portability, we evaluate how different errors evolve with maturing process and OPC recipe conditions for different layout patterns.

6730-31, Session 8

Selecting and using a lithography compliance DFM tool for 65-nm foundry production

R. Kapoor, Synopsys, Inc.

DFM tools have been all the rage in recent years. By exposing potential manufacturability, timing and variation issues early, these tools can help the designers correct such issues before the tapeout, thus delivering a faster yield ramp for the product. For the lower volume devices, the faster yield ramp can help meet the market window while for higher volume devices it can mean millions of dollars in cost savings. While there have been several product announcements, case studies focusing on actual usage of such tools are not publicly available.

In this article a TSMC 65nm fabless customer will share its experience in evaluating and using the lithography compliance tool. By focusing on the motivation to use such a tool, the article will first quantify the expected value from such a tool. Next the article will present the detailed evaluation criteria for choosing a tool. Finally, actual error data from production tapeouts and performance metrics of the LCC tool will be presented showing runtime, scalability and memory numbers.

6730-32, Session 8

Litho-aware extraction for the 32-nm double-patterning node

J. A. Huckabay, Q. Chen, C. S. Thayer, R. J. Naber, Cadence Design Systems, Inc.

A methodology to predict the impact of mask overlay and litho-induced process variations on Statistical Timing for Double Patterning is presented. As we migrate to the 32nm node and Double Patterning techniques, Mask Makers, Ebeam providers and Scanner providers are given very aggressive requirements for maintaining overlay accuracy. This method takes into account Mask CD Uniformity and Mask Image placement error budgets presented in the 2006 ITRS. It is assumed the ITRS requirements are met. This methodology combines the infrastructure used in Single Exposure Litho-Aware Layout Implementation tools with Double Patterning decomposition results to determine a meaningful layout-specific analysis for pre-tape-out timing sign-off. Traditional timing analysis uses a set of look-up tables for simulating device distortions. These tables have been proven to require excessive guardbanding in Single Exposure masks. Adding the additional dimension of overlay distortion to these tables will have the effects of hiding parametric failures, or requiring excessive guardbanding to ensure timing predictability. Results will be shown that describe the timing effects with and without taking into account these distortions, as well as design samples that contribute to these distortions.

6730-33, Session 8

Silicon-verified automatic DFM layout optimization: a calibration-lite model-based application to standard cells

K. Lin, B. P. Wong, Chartered Semiconductor Manufacturing, Inc.; F. A. J. M. Driessen, Takumi Technology Corp. (Netherlands); E. Morita, Takumi Technology Corp.

DFM considerations have become an indispensable and integral part of advanced nanometer semiconductor product designs. Traditional first-generation DFM tools have focused on functional lithography hot-spot detections. While useful, these tools offer designers few hints on the complex layout fixings and the intricate trade-off decisions required. With these limitations, DFM layout optimization has become a tedious and inconsistent design endeavor. In addition, the long and intense calibration cycle required for the traditional DFM models have hindered their effectiveness and timeliness. An automatic DFM layout optimization system that performs systematic multi-objective functional and parametric DFM optimizations at early design phase will be introduced. A calibration-lite methodology that has expedited the DFM model set-ups will be discussed along with the silicon validation test pattern designs. Finally, both simulation and silicon SEM experiment results will be presented.

6730-34, Session 8

Non-uniform yield optimization for integrated circuit layout

F. G. Pikus, J. A. Torres, Mentor Graphics Corp.

One of the challenges in quantitative manufacturability analysis has been establishing a single design quality metric able to describe how a given region in the layout would perform under a specific manufacturing process condition. Historically, critical area analysis has been sufficient to evaluate the possible yield of a design, but as the relative importance of systematic mechanisms increases, this purely statistical approach needs to be enhanced by incorporating additional process information.

Recently, several attempts were made at devising a consolidated metric and a system that can analyze multiple process conditions and different design configurations to arrive at an optimal solution. This solution is based on a cost function which depends on the characteristics of the manufacturing process. As expected, calculations show that the optimal combination of yield and manufacturability enhancements depends on the manufacturing conditions. This is not surprising, considering that most yield enhancement techniques counter one of few yield loss mechanisms but incur some yield penalty due to other causes of yield degradation. For example, redundant via insertion reduces via failure but often increases critical area.

Previous works attempted to select a single combination of design enhancements which presents the optimal trade-off between different yield loss mechanisms and optimizes the total yield. In this paper we explore whether this optimal solution is global for the entire design or varies from location to location. We show that, under realistic conditions, the optimal solution depends on the layout features on a small scale, thus the best yield can be achieved by selecting different combinations of enhancements in different locations. We introduce a general form of the cost function and compare different layout configurations taking into account lithography process variations, random defect distributions, and

recommended design rules. Since all layout configurations represent the same electrical devices, it is possible to dynamically determine the most robust layout implementation according to the cost function that incorporates the relative importance of each yield loss contributor. We compare the globally optimized layout, where the sequence of yield enhancements is selected based on the overall design yield, with locally optimized layouts where the enhancements are fine-tuned for each location.

6730-35, Session 8

Model-based DFM compilation for standard cell libraries

D. Yang, Semiconductor Manufacturing International Corp. (China); G. Shou, SMIC Americas; R. Chen, Semiconductor Manufacturing International Corp. (China); Q. Qian, IC Scope Research

Existing model based DFM flow today centers on hotspot detection and fixing. It reacts to often subjective definition of hotspots with a time consuming verification-fixing loop which requires constant support from manufacturing. In this paper, we present a new yield enhancement technology where a physical lithography model is used to directly drive layout construction. The new technology, we termed DFM compilation, examines every layout and every layer through the critical lens of a processing model. The analysis results are used to automatically drive polygons to a new configuration that has higher immunity to systematic process variations. DFM compilation optimizes layout on a continuous basis without using subjective detection thresholds and thus delivers widespread improvements across the entire chip. We will quantify yield gain resulting from DFM compilation technology using a high performance library from SMIC consisting of 600 cells. A DFM scoring tool that is calibrated with production data is used as standard for grading each layout. We compare the yield score for each cell before and after DFM compilation and measured extensive yield enhancement for 90% of the layouts. A majority of layouts received multi-percentage point gain in estimated yield. Similar extent of improvements would require hand editing on the order of ten thousand hotspots using existing DFM tools. We set the optimizer such that the output GDSII maintained the same area and pin locations as the original input. Independent DRC/LVS checks on both cell interior and boundaries confirm the correctness of optimized results. The experiment used a universal tapeout model and first principle simulation without requesting any confidential processing recipe. No hand editing is performed and all cells used the same optimization settings. The quality of results will further improve with foundry specific models, individual tuning of optimization settings, and with a small amount of hand editing. This is, to our knowledge, the first report of automatic standard cell library construction using lithography models. It demonstrates that new technologies such as DFM compilation can effectively help to increase manufacturing efficiency and bring cost saving benefits to our customers.

6730-36, Session 8

A lithography aware design migration using foundry certified models and hotspot detection

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An automated litho-aware design migration solution has been implemented to enable designers to port existing IP layouts (custom, library, block) to nanometer technologies while optimizing printability and yield.

With rapidly shrinking technology nodes, the industry consolidation toward fabless or fab-lite manufacturing, demand for second-sourcing and dramatic increase in cost of IP development, the automation of “vertical” (between nodes) and “horizontal” (between chip manufacturers) migration becomes a very important task. The challenge comes from the fact that even within the same technology node design and process-induced rules deviate substantially among different IDMs and foundries, which lead to costly, error-prone and time consuming design changes. At the same time, fast and reliable adjustments to design and ability to switch between processes and chip manufacturers could represent significant improvement to ROI. Using conservative rules (or common design rules) is not a viable option because of the area, performance and yield penalties. The difficulty of migration is augmented by the fact that design rules are not sufficient to guaranty good printability, maximum process window and high yield. Model-based detection of lithography-induced systematic yield-limiting defects (a.k.a. hotspots) is becoming a vital part of the design-for-manufacturing flow for advanced technology nodes at 65nm and below.

Driven by customer demand, a collaborative effort between EDA vendors provides a complete design-for-manufacturing migration solution that allows sub-90 nanometer designers to comprehensively address the impact of manufacturing variations on design yield and performance during layout migration.

First, the physical hard IP is migrated from its existing 90nm process to a more advanced 65nm process, resulting in an area-optimized DRC-clean 65nm design retaining the original hierarchy to facilitate further editing and design verification the original hierarchy is maintained.

Then, the design manufacturability is checked using a model-based hotspot detection solution, applying foundry-certified models. Along with hotspots, it is also critical for the hotspot detection tool to generate directives on how to modify the layout to fix hotspots and prevent creation of new hotspots. Several alternative fixing guidelines, ranked by amount of design perturbation, are generated to provide focus and maximum flexibility to the correction tool.

The correction tool reads hotspot locations, severities along with the fixing guidelines, identifies area to be fixed and converts the fixing guidelines into geometry constraints. Correction is then done on each area while respecting design rules, managing ripple effects thru multiple layers and preserving the hierarchy. When all the corrections are completed areas that have been affected are identified to allow these to be incrementally checked by the lithography verification tool and re-assembled. In case new or residual hotspots are detected, this fix-verify flow iterates over to converge on a DRC and lithography-compliant design. Usually one to three iterations are needed to output hotspot-free, DRC-compliant design.

We present the results of this fully automated lithography-aware migration flow on layout IPs ranging from 90 nm to 65 nm design and migrated across foundries. We present and discuss the influence of different tool settings such as jog introduction and fixing window size. We also discuss different strategies on correction advice and their combined effect on the quality of the fixed and lithography-optimized layout. Results show substantial layout quality improvements, reduced design sensitivity to process variability by eliminating hotspots. Run-time and quality metrics are given for both “horizontal” and “vertical” layout migrations.

6730-124, Poster Session

New method of identification of fault defect using defect imaging system

H. Zhang, Holon Co., Ltd. (Japan)

In worldwide reticle mask inspection market, some equipment maker just provides Die- to Die(DD) defect review function. Instead, HOLON develops world leading advanced “Defect Imaging System” (DIS), which one step further enable the combination between Scanning Electron Microscope Image(SEI) and Die- to-Database(DB) function.

This system shows CAD references pattern, SEI and superimposed image between CAD and SEI (Superimposed image)

In contact hole layer case, HOLON DIS is able to measure CD, area and corner rounding values by CAD/SEI/Superimposed images simultaneously.

As far, DIS also provides following feature functions for optimized process tuning. (1)Bias parameter adjustment for simulation mask match optimized value.(2) Edge roughness measurement.

By presenting the totally new concept of inspection process, HOLON DIS can help to verify defect on reticle mask into different categories.

6730-125, Poster Session

Study of mask defect inspection optics for hp 45-nm node device and beyond

R. Hirano, K. Takahara, M. Hirono, R. Ogawa, S. Murakami, N. Kikuiri, Advanced Mask Inspection Technology, Inc. (Japan)

The usage of ArF immersion lithography for hp 45nm node and beyond leads to the increase of mask error enhancement factor in the exposure process. This makes preferable the inspection wavelength to be consistent with that of lithography tool. We have already developed the mask inspection system using 199nm wavelength. This system is capable of simultaneous transmission and reflection inspection, and is a strong candidate for hp 45nm node mask inspection.

The demand for inspecting smaller dimensions is, however, ever increasing. The greater the image magnification and smaller the CCD pixel size, the smaller the size of resolvable mask defects. However, as the image magnification increases given a fixed CCD pixel size, the image field as well as photons reaching the image sensor decreases. This lengthens the inspection time per mask since the size of image field that can be inspected at a time decreases while the image sensor requires greater time to accumulate sufficient amount of photons. Therefore, the least image magnification necessary in order to obtain a desired inspection performance is an important index in designing the next generation mask inspection system.

In hope to meet the demand, a captured image simulator has been developed to study the theoretical performance limit of our inspection system. The simulator accurately models inspection optics including the pixel size of image sensor. The interaction of light with mask features is calculated rigorously using RCWA (Rigorous Coupled-Wave Analysis) method. The calculation of the simulator has been verified against experimental data. By using this image simulator, we analyzed the captured images of ArF-HT mask with dot/hole defects among L/S pattern in both transmission and reflection.

According to the analysis, various interesting traits have been found for our system. The results show that in general, hole defects are better resolved in reflection while dot defects are better resolved in transmission. Also, this characteristic reverses as L/S dimension nears the resolution limit. In short, the transmission optics and reflection optics compensate each other in terms of resolution, making the capability to inspect in both transmission and reflection optics essential in detecting small defects. Further, optical contrast tends to decrease faster in transmission than in reflection as L/S dimension decreases. Finally and most important, the inspection system using 199nm wavelength was found to be capable of inspecting beyond hp 45nm node.

6730-126, Poster Session

Improving inspectability with KLA TeraScan Thin Line De-sense

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As the design rule continues to shrink towards 65nm and beyond and the cost of mask making increases, more mask makers and designers are introducing more aggressive OPCs, such as SRAF (Sub-Resolution Assist Feature), to enhance mask quality. These features are sub-resolution in nature. Even the most advanced mask writers have a hard time resolving them on the mask with consistent edge and line-end quality. Consequently, the inconsistent writing of these SRAFs brings new challenges to the inspection process, even when die to die inspection is used. If a single sensitivity setting is used on the entire mask, users may be forced to substantially lower this sensitivity in order to achieve the inspectability that is required for a given inspection flow. This decrease in sensitivity may cause critical, or printable, defects on the main pattern to be passed. In some cases, this could result in yield lost on the final wafer. In response to this new challenge, KLA-Tencor is releasing TLD (Thin Line De-sense), an addition to the current die to die HiRes 1 detector. With cooperation from Samsung electronics, KLA-Tencor successfully demonstrated that TLD on KT53x using 90nm pixel can successfully increase inspectability without sacrificing sensitivity on the main pattern.

6730-127, Poster Session

Improvement in defect classification efficiency and useable sensitivity by grouping disposition for reticle inspection

S. Liu, E. H. Lu, KLA-Tencor Corp.; E. Guo, C. Liu, Semiconductor Manufacturing International Corp.

ABSTRACT

The continuous evolution of IC design rule brings aggressive OPCs features such as opaque and clear sub-resolution assists in order to enhance image printing quality on wafers. The inconsistent sub-resolution features give mask defect inspection tools a challenge. Reviewing large number of nuisance and false defects impose an extraordinarily heavy burden on the operators and therefore defect classification efficiency becomes more significant. ReviewSmart provides an efficient defect classification method by the concept of grouping disposition according to defect environments and similarity. In other hand to inspect insonsistant assist bars or line-end shortening, mask inspection engineers have to desense sensitivity to achieve inspectability. ReviewSmart is able to eliminate the false defects caused by aggressive OPC and improve useable inspection sensitivity on main features. It is valuable to explore the most efficient use of ReviewSmart to improve productivity and improve usable sensitivity.

6730-128, Poster Session

Improvement in soft defect classification efficiency by grouping disposition for wafer fab reticle re-qual inspection

P. P. Yu, E. H. Lu, KLA-Tencor Corp.

ABSTRACT

193nm litho accelerates haze seeding and haze growth due mainly to higher optical energy than the optical energy of 248nm litho. The amount of haze and crystal progressing defects increases significant and inspection engineers have to spend a lot of time to review these soft defects and track critical defects. To eliminate the burden on engineers and to improve productivity, we investigate an effective defect classification and binning method - ReviewSmart. The defects disposition is according to defect environments and similarity. It is able to bin soft defects on clear area into groups. Therefore engineers are able to save time and to monitor early warning of reticle re-qualification efficiently. In other hand ReviewSmart is also able to eliminate the false defects caused by aggressive OPC and improve useable inspection sensitivity on main features. It is valuable to explore the most efficient use of ReviewSmart to improve inspection productivity and to improve usable sensitivity in wafer fabs.

6730-129, Poster Session

Enhancing productivity and sensitivity in mask production via a fast integrated T+R inspection on critical layers

P. P. Yu, E. H. Lu, KLA-Tencor Corp.

ABSTRACT

Individual Transmitted Light (dbT) and Reflected Light (dbR) pattern inspection are widely employed by mask makers in order to detect pattern defects on photomasks during the mask inspection process. The sensitivity of the Fast Integrated dbTR inspection is the better of the Transmitted light detections and the Reflected light detections. For example, pinhole defects and inside corner defects are typically better detected by Reflected Light. Conversely, pindot defects and outside corner defects are better detected by Transmitted Light. Conventionally to achieve such sensitivity needs a two-pass inspection to detect Reflect sensitive

defects and Transmitted sensitive defects.

In this paper we introduce the 'Fast Integrated T+R' capability and investigate the properties of this combination of Transmitted (T) and Reflected (R) light inspection. 'Fast Integrated T+R' has the capability to reduce a two-pass inspection to a single set-up and single pass inspection resulting in a substantial saving of inspection time with the best sensitivity of either dbT or dbR. During this study we collect and analyze inspection data on a critical layer provided by the Taiwan Semiconductor Manufacturing Company, Ltd. Compared to the 2-pass individual mode pattern T and R inspections, a single scan 'Fast Integrated T+R' demonstrates the capability to capture additional real defects, improves reticle inspectability and first time success rate, and results in a enhancement in productivity and sensitivity. Based on empirical data collected in this study, the Fast Integrated T+R is able to improve inspection throughput approximately 45% at P90.

6730-130, Poster Session

ADAS: integrated mask defect analysis for disposition and process control in mask shops and wafer fabs

P. J. Fiekowsky, AVI-Automated Visual Inspection; S. Narukawa, T. Kawashima, Dai Nippon Printing Co., Ltd. (Japan)

ADAS (Automated Defect Analysis Software) is the first product to fully automate mask defect analysis for mask shops and fabs. ADAS classifies and dispositions photomask defects both quickly and accurately based on defect size and simulation based printability measurements. Full analysis of inspection reports with 100 defects requires 2 seconds. Printability measurements match AIMS within 5 percent at 3 sigma on 65 nm test masks. Reproducibility is 3 percent at 3 sigma over multiple inspections. ADAS can reduce the need for production AIMS measurements by 90%, reduce operator review time by 95%, and eliminate operator review errors and the re-pelliclizations they cause. ADAS increases overall inspection efficiency for mask shop first-inspection and final inspection. It should be valuable for fab requalification inspections and for eliminating the need for incoming inspection in fabs.

6730-22, Poster Session

Analyses of mask corner-rounding behavior

N. Seong, Photronics, Inc.

Understanding corner rounding behavior of mask is important as the use of small corners and small jogs are increased with use of OPC. Different corner rounding of post OPC mask patterns can lead to different corner behavior on wafer and ultimately it can change electrical characteristics of the final circuits. Corner rounding of mask patterns were measured from custom test patterns and critical parameters deciding corner rounding characteristics will be discussed. The impacts on wafer imaging were modeled for various mask shapes covering multiple technology generations and wafer verification of model results were followed. Various matching approaches of different corner rounding mask shapes were explored including active data corrections.

6730-132, Poster Session

Automatic OPC repair flow: optimized implementation of the repair recipe

M. S. Bahnas, M. Al-Imam, Mentor Graphics Corp. (Egypt); J. C. Word, Mentor Graphics Corp.

Virtual manufacturing that is enabled by rapid, accurate, full-chip simulation is a main pillar in achieving successful mask tape-out in the cutting-edge low-k1 lithography. It facilitates detecting printing failures before a costly and time-consuming mask tape-out and wafer print has occurred. The OPC verification step role is critical at the early production phases of a new process development, since various layout patterns will be suspected that they might to fail or cause performance degradation, and in turn need to be accurately flagged to be fed back to the OPC Engineer for further learning and enhancing in the OPC recipe. At the advanced phases of the process development, there is much less probability of detecting failures but still the OPC Verification step act as the last-line-of-defense for the whole RET implemented work.

In recent publication the optimum approach of responding to these detected failures is addressed and a solution was proposed to repair these defects in an automated methodology and fully integrated and compatible with the main RET/OPC flow. In this paper the authors will present further work and investigations on this Repair flow.

An automated analysis methodology for root causes of the defects and classify them to cover all possible cases will be discussed. This automated analysis approach will conclude all the learning experience of the previously highlighted causes and include any new discoveries. Next, according to the automated pre-classification of the defects, application of the appropriate approach of OPC repair (i.e. OPC knob) on each classified defect location can be easily selected, instead of applying all approaches on all locations. This will help in cutting down the runtime of the OPC repair processing and reduce the needed number of iterations to reach the status of zero defects. An output report for existing causes of defects and how the tool solved/handled them will be generated. The report will help further learning and enhancing the main OPC recipe. Accordingly, the main OPC recipe can be more robust, converging faster and probably in less number of iterations.

6730-133, Poster Session

Database and data analysis strategy for multidesigner testchips

W. J. Poppe, A. R. Neureuther, Univ. of California/Berkeley

A database and data analysis strategy is proposed for multi-designer test chips that involve a wide array of different test structures designed for process characterization. A well-designed database helps facilitate collaboration and forces structure into measurement and design related data, which is necessary for comparison of data among designers. All data is centrally located, so each designer has access to all measured data as well as layout designs and analysis results from other designers. The database can be made web accessible for designers of the current testchip as well as all engineers that might be involved in future testchip designs or those that are interested in analyzing current results.

This paper will describe the details of a database as well as the strategy that will be employed to analyze the data. Statistical tools such as using cluster analysis on correlation matrixes based on different attributes will be used to identify trends and to classify different test patterns. Methods based on ANOVA analysis can be used to test if test structure results are confounded by unforeseen process effects and if those effects can be filtered out. As different patterns have different sensitivities to MEEF, defocus, LER, and other process non-idealities, it is possible to identify and characterize individual effects when looking at multiple test structures together.

With this comprehensive strategy, a database has been custom built for a multi-designer testchip that has over 40 different types of test structures aimed at characterizing various process non-idealities. Misalignment, MEEF, systematic across wafer variation, Line Edge Roughness, Random Dopant Fluctuations, corner rounding, dose offsets, defocus, as well as other pattern dependent phenomena will be studied (1). The database has been implemented in MySQL and will be made web accessible through Ruby on Rails and PHP. As electrical results are not expected to be available at the time of the conference, data analysis will be based primarily on simulation results. The database will be populated with simulation results from the Parametric Yield Simulator (2), which will be used to simulate test structures under different process conditions. Since each measurement or simulation result will be associated with a set of attributes ranging from layout description to process conditions, trends will be analyzed and test structures will be classified into different groups. With a thorough understanding of the different test structures and their response to different process non-idealities, it will be possible to leverage the benefits of having 41 different types of test structures on one chip. This comprehensive test chip strategy should prove to be useful as process flows constantly evolve and one way to prepare for the unexpected is with wide arrays of different test structures and a robust data analysis strategy.

(1) Wojtek Poppe, et al, “Building Transistor Based Electrical Test Structures for Process Characterization”, SPIE, 6520 (2007)

(2) Wojtek Poppe, et al, “Platform for collaborative DFM”, SPIE, 6156 (2006)

6730-134, Poster Session

Router-driven automated correction of lithography hotspots

D. N. Zhang, S. Tong, L. Wen, F. W. Tseng, A. Miloslavsky, K. Kwang, Z. Tang, Synopsys, Inc.

As semiconductor manufacturing march towards increasingly aggressive process nodes, more design constraints are arising from the need for manufacturing process margin to improve yield. One of main yield limiters is the increasing number of lithographic “hot-spots” that arise from the complexity of design layouts as technology nodes shrink to 65nm and below. Lithography understanding in design tools is no longer a feature but a necessity. Designers now have the additional burden of eliminating these litho hotspots during the physical design stage. This process is done manually today by trial and error or with limited guidance that does not take into account the design rules. The approach of purely rule-based detection and correction has the drawback of introducing large amount of false positives. The convergence of hotspots may also be jeopardized using a blind guidance system that some have attempted. In this paper, we introduce a novel hybrid correction methodology that combines the rule-based correction approach and model-based guided correction and verification. We accomplish two main goals in this method: 1. 100% litho hotspots correction is achieved; 2. area penalty is maintained at zero and design parametric variations such as power and timing are minimized by not over-correcting false-positive areas. These goals are realized by integrating an automated Place and Route System that converges on each hotspot while being aware of design rule constrains with a foundry qualified highly accurate model-based detection system that allows the tool to pinpoint only true wafer yield limiters.

6730-135, Poster Session

Assessment of 2D OPC target specifications using electrical testable structures

Q. Zhang, P. J. M. VanAdrichem, Synopsys, Inc.

It is only in the last few technology nodes that the 2D behavior of lithographic model is getting more attention. There is a very simple reason for this: devices in the most advanced technology nodes experience much more rounding than in previous generations. This is a direct result of the decreasing k1 factor, the number denoting the ratio between the required optical resolution and the available resolution power.

Today the only method of assessing the 2D model behavior is overlaying the model-predicted contour with the measured CDSEM image. This ‘geometry-only’ based method is highly subjective, and it does not characterize 2D behavior impact on electrical performance of the transistor. In the absence of systematic correlation methods between 2D model behavior and electrical device performance, there is a almost natural tendency to over specification.

In this paper methods are described to assess lithographic/OPC 2D target specifications using circuit electrical performance as criteria and how they can be verified using electrical measurable test structures. In the first part of this work, lithography simulation and circuit analysis are performed to evaluate the impact of corner rounding to the transistor electrical performance using a simple close-form first order approximation. In order to verify the validity of this approach, we also investigated a more rigorous approach, which computes the transistor electrical performance using HSPICE based on simulated non-triangular gate contour from lithographic simulator. Our work demonstrated very good agreement between the simple close-form approach and HSPICE based rigorous approach.

Finally we proposed using some novel electrically testable devices to validate the efficacy of the aforementioned HSPICE based rigorous approach by comparing the real-silicon transistor performance to the simulated one. The methodology presented here can also be extended and used to optimize other lithographic/OPC parameters and some design rules.

6730-136, Poster Session

Lateral interactions between standard cells using pattern matching

L. T. Wang, A. R. Neureuther, Univ. of California/Berkeley

This paper proposes a novel method of identifying interactions between neighboring standard cells via fast-CAD pattern matching. Depending on the illumination and k1 factor, the optical proximity influence can be as many as 5 feature sizes in diameter. Moreover, optical proximity influence alternates in sign with distance. Thus, the influences from next-next neighbors are not so easily understood or efficiently captured in design rules. Also, many combinations of possible neighbors must be evaluated quickly for a multitude of process window conditions and additional process non-idealities. By automating this evaluations process by fast-CAD pattern matching, cells that are aggressive neighbors or weak victims can be quickly identified and redesigned.

We present our studies on 90 nm technology standard cell interactions, concentrating on poly and metal layer 1, which have fundamental different layout strategies. We demonstrate through examining pair-wise combinations of standard cells that lithography hotspots arise due to neighboring cell interactions. Furthermore, by varying the distances between these sensitive combinations, oscillations in pattern match factors are observed with 10% peak-to-peak variance in pattern match factor. The oscillations indicate that lithography hotspots that arise from neighboring cell interaction may be intelligently alleviated by moving the aggressor standard cell to an optimal distance away from the victim standard cell. Results are verified through simulations in SPLAT for 100 nm depth of focus, NA of 0.85, λ of 193 nm, and σ of 0.3. Changes in linewidth vary quadratically with pattern match factors, which can be modeled by a parabolic equation with an r-squared value of 0.77.

6730-137, Poster Session

Application of modified jog-filled DRC method on lithography friendly OPC flow

Y. Kim, S. Lee, J. Kang, J. Kim, K. Kim, Dongbu Electronics Co., Ltd. (South Korea)

Lithography friendly design (LFD) method have been recently high addressed since it is dramatically improved cycle of design revision as well as number of learning cycles to reach yield target. Lithography friendly design is, for example, the reduction number of small jogs and notches in original data base in other word pre-OPC data base. We can call them as OPC-unfriendly patterns since they make very complicated pattern after OPC. They usually meet design rule so that DRC step does not filter them. Also, they make many errors after OPC because OPC model recognizes just as one of small features what we should care. This generates many false alarms after OPC verification and mask rule check.

General method to implement LFD is update rule table or design rule after having actual yield data or device failure analysis data into database handling flow. Another method is utilization of simulation tool to predict lithography unfriendly design. They take time to setup excellent rule to predict accurately even if they are very good approach as fundamental solution for LFD. It will be better if a simple solution having fast setup time and improving major lithography unfriendly design such as small jogs and notches.

In this paper, we proposed new type of LFD flow which is application of modified DRC step on LFD flow. This modified DRC checks OPC-unfriendly patterns and changes to <OPC-friendly\> as well as design rule violation. It is pre-OPC database handling method for removing the small jogs and notches. After finding small jogs or notches, DRC software fills jogs and notches to simplify patterns including them, in this case, unnecessary fragments should not be generated. Using this jog-fill technique, we can dramatically reduce the incidence of necking or bridging and increase contact coverage and it enhances the final yield and reliability of circuit.

6730-138, Poster Session

Measurement and experimentation about correlation of pellicle's life time

S. Park, Y. Kang, H. Oh, Hanyang Univ. (South Korea)

Recently, a pattern size gradually has reduced to enhance the integration of semiconductor device. According to recently proposed roadmap, ArF immersion lithography will be used for 65 nm to 45 nm technology nodes. As minimum linewidth has shrunk, the exposure wavelength has also progressively shrunk. Expose wavelength shrink caused some serious problems. In exposure process, the pellicle's adhesives on the mask is becoming the serious matter and problem in semiconductor industry. Pellicle's life time is important to exposure process and is affected by exposure intensity.

Also, The crystal growth and haze formation on the mask are becoming serious matter in the semiconductor industry.. This growing defect on the reticle is called the haze. Haze is a kind of surface contamination on the photomask and the lithography optics that made by photochemical reaction. Various material contribute to photomask and pellicle formation including : chemical residuals from mask cleaning, out-gassing from pellicle glue/materials, and contaminants from the scanner ambient. The haze produces serious problems such as the drop of transmission, the increase of scattered light and poor pattern formation. So we need to investigate the haze defects that considered these effects. The typical haze grows slowly as time goes by in the initial stage, however the haze spreads suddenly in a later time. The haze also appears from the outer region of the mask, and it grows into inner region of the mask.

We consider the life time of pellicle and the haze of photomask by intensity and position of exposure. We used 193 nm (ArF) excimer laser and measured pellicle's adhesive strength and haze on the mask and pellicle life time. We investigated binary intensity mask with 193 nm ArF lithography for pellicle's life time study by changing the transmittance and exposure intensity. And we study about correlation of the pellicle's life time and the haze. Also, we research about interaction of the pellicle's adhesives and the haze on the photomask.

6730-139, Poster Session

Pellicle dimensions for high-NA photomasks

F. Erber, T. Schulmeier, C. Holfeld, Advanced Mask Technology Ctr. (Germany)

When the crystal growth phenomena rose on the horizon of wafer lithographers and photomask makers, the pellicle and its properties in fact for the first time have come into serious visual gaze of the IC manufacturing chain. With the extension of optical 193nm lithography by high NA immersion and double patterning techniques, pellicle properties are now more than ever part of considerations for optimized imaging techniques. Basic properties like pellicle height and size though, must not fall behind in attention when preparing for the physical and environmental changes expected in the future.

At photomask manufacturing, post pellicle inspection suffers from an interference of pellicle size and height dimensions with the inspection equipment requirements causing a pellicle shadow. Depending on the image field size, this shadow can range even into the active area of the customer design causing non-reliable inspection results.

Since the extended 193nm lithography roadmap will require pellicles on advanced photomasks throughout 2012 and maybe even far beyond, the evolution of this effect as well as similar potentially upcoming effects during other lithography processes need to be understood in order to identify potential problems ahead of time and prepare the industry accordingly.

We have studied the pellicle shadowing effect during photomask inspection for different samples from several pellicle vendors using different types of inspection equipment and extrapolated the results for next generation inspection equipments. We have studied shadowing effects at wafer lithography and mask through pellicle registration measurement for potential problems in the future.

We will present the results of these studies and summarize recommendations on how to cope with shadowing effects in the near and in the longterm using high NA lithography.

6730-140, Poster Session

Evaluation of attenuated-PSM photomask blanks with TF11 chrome and FEP-171 resist on a 248-nm DUV laser pattern generator

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Tighter requirements on mask resolution, CD and image positioning accuracy at and beyond the 45nm technology node push the development of improved photomask blanks. One such blank for attenuated phase-shift masks (Att-PSM) provides a thinner chrome film, named TF11, with higher chrome etch rate, compared to the previous generation Att-PSM blank (NTAR5 chrome film) from the same supplier. Reduced stress in the chrome film also results in less image placement error induced by the material.

FEP-171 is the positive chemically amplified resist (PCAR) that is most commonly used in advanced mask manufacturing with both 50 keV variable shaped e-beam (VSB) and DUV laser pattern generators. TF11 allows an FEP-171 resist film down to about 2000 Å thickness with sufficient etch resistance, while the standard resist thickness for NTAR5 is around 3000 Å.

This work has experimentally evaluated the use of TF11 chrome and FEP-171 resist together with a 248 nm DUV laser pattern generator, the Sigma7500-II.

First, patterning performance in resist with thicknesses from 2000 Å to 2600 Å, in steps of 100 Å, was tested with respect to swing curve and basic lithographic parameters including resolution, CD linearity, CD iso-dense bias and dose sensitivity, etc. Patterning results on mask showed a swing minimum at around 2200 Å and a swing maximum at around 2500 Å, which correspond to reflectivity measurements for 248 nm wavelength performed by the blank supplier. It was concluded that the overall patterning performance was best close to the swing maximum.

Thereafter the patterning performance using TF11 at two resist thicknesses, 2000 Å and 2550 Å, was studied in more detail and compared to performance using NTAR5 with 3200 Å resist. The evaluation showed that the Sigma7500-II offered good compatibility with TF11, especially using the optimized FEP-171 resist thickness of 2550 Å. It also showed that patterning capability with the Sigma7500-II using TF11 and 2550 Å resist is improved compared to using NTAR5 and 3200 Å resist.

6730-141, Poster Session

Bimetallic thermal resists potential for double-exposure immersion lithography and grayscale photomasks

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Double Exposure/Patterning is considered the best candidate for extending 195nm Optical Lithography significantly below 40nm resolution. However, double exposure requires a resist that does not experience superposition: where the result of two exposures at one intensity level is not the same as a single exposure at twice that intensity. A class of negative thermal resist that strongly show this effect are bimetallic thin-films consisting of Bismuth on Indium (Bi/In) or Tin on Indium (Sn/In). The films are bilayered structures until sufficiently heated by a laser exposure pulse (7 mJ/sq. cm for 4 nsec) which then converts the film into a transparent eutectic oxide alloy. A noted property of thermal resists is their ability to remain almost unaffected during a sub-threshold exposure that does not reach the activation energy. Experiments with interference lithography at 266nm in air demonstrated that Bi/In resists have a resolution limit <42nm, the exposure system limit. Further investigations into immersion interference lithography systems on bimetallic resists are being conducted. As a first investigation, the response of bimetallic resists to underwater exposure was examined. Sn/In films were exposed using various laser exposure levels using our in-house mask-writing system in both air and water immersion conditions. The film was developed using a diluted RCA-2 solution (HCl:H2O2:H20 \@ 1:1:48) and the resulting structures examined. The Sn/In film demonstrated successful

development as thermal resist for immersion lithography and the power level required to convert the film was at most marginally higher than the level required for exposing the film in air. These results allow us to describe the requirements for an immersion exposure system that can perform interference lithography or double exposure methods to investigate the resolution limits of these thermal resists.

When exposed beyond the initial threshold, additional oxidation changes the resist transparency which increases as a function of the laser power, enabling their application as grayscale photomasks. Bimetallic films have demonstrated transmittances <0.1% when unexposed and \>60% when highly exposed to an Argon Laser. Utilizing a direct-write method, grayscale photomasks can be patterned onto the films by adjusting the power level of the writing laser. However, the direct laser writing approach causes fine variations in the mask's transparency due to the Gaussian power profile of the beam. To correct this problem, a grayscale beam-shaping mask is designed to manipulate the power profile of the unfocussed laser beam and make it more uniform. SEM imaging and XRD analysis of the patterned areas are presented showing the improvement in the photomasks written using the beam-shaped laser. To measure mask transparency at a fine resolution level suitable for characterizing a photomask's grayscale, two photodiode sensors were added to the writing system. With its positioning abilities, focused laser beam and high resolution (24-bit) sensors, the combined system allows transparency to not only be measured within a micrometer sized area but can also profile the transparency across a given distance. The smaller scanning area for this system allows the use of test structures 100x smaller then previously required in calibrating a photomask's grayscale characteristics.

6730-142, Poster Session

A dynamical model of drying process of polymer-blend solution coated on a flat substrate

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We have proposed and modified a model of drying process of polymer solution coated on a flat substrate for flat polymer film fabrication and have presented the fruits through Photomask Japan 2002, 2003, 2004 and so on. And for example numerical simulation of the model qualitatively reappears a typical thickness profile of the polymer film formed after drying, that is, the profile that the edge of the film is thicker and just the region next to the edge's bump is thinner. Then we have clarified dependence of distribution of polymer molecules on a flat substrate on a various parameters based on analysis of many numerical simulations. Then we drove nonlinear equations of drying process from the dynamical model and have introduced initial results of numerical simulations of the nonlinear equations and approached essential qualities of nonlinearity in non-equilibrium process of drying process through consideration of roles of various parameters. The fruits were reported at Smart Materials, Nano-, and Micro-Smart Systems 2006 and so on.

Then we done a few kinds of experiments so as to verify the modified model and reported the results of them through Photomask Japan 2005, 2006 and 2007. We could observe some results supporting the modified model.

The subject of above studies was limited to solution having one kind of solute though the model could essentially deal with solution having some kinds of solutes. But nowadays discussion of drying process of a solution having some kinds of solutes is needed because drying process of solution having some kinds of solutes appears in many industrial scenes. For example, polymer blend solution is one instance. And typical resist consists of a few kinds of polymers. So, in fact, considering drying process for the flat resist film fabrication, we need to consider drying process of polymer blend solution.

Now we can easily deal with solution having some kinds of solutes or polymer blend solution through a few improvements of the former model of drying process as stated above. And since this model is general and simple, we can apply the model to general solute-blended solution.

But, speaking reversely, phenomena caused by polymer's own property can not be reproduced by the model. Concretely, while polymer's stratified (graded) structure can be reproduced by the model, polymer's sea-island structure which is frequently observed after drying a polymer blend solution can't be reproduced by the model. If we want to reproduce above-mentioned polymer's sea-island structure using the model, we have to improve the former model vastly through adding effects of solubility, phase transition, crystallization and so on to it. But, in this study, we minimize the improvements of the model so as to maintain generality of the model.

In this presentation, at first, we introduce a dynamical model of drying process of polymer blend solution (solution having some kinds of solutes) coated on a flat substrate. Then we introduce results of numerical simulations of the dynamical model and consider mechanisms of various structures' formation.

6730-143, Poster Session

Investigation of limit diffusion length limitation for 45-nm node attenuated and chromeless phase-shift mask

Y. Kang, S. Park, H. Oh, Hanyang Univ. (South Korea)

Microlithography has shown an amazing development over the last decades and continue to be one of the critical success factors for enabling ever smaller feature sizes. The fabrication of leading edge devices strongly relies on the use of chemically amplified resist (CAR), where the post exposure bake is among the most important processing steps for obtaining CD control.

Post exposure bake (PEB) sensitivity is defined as the dependency of pattern size (or critical dimension, CD) variation on the perturbation of the PEB temperature and time through out this paper. Beginning of ArF (193 nm) lithography PEB sensitivity becomes serious problem because ArF photoresist show very severe dependency on PEB temperature. PEB sensitivity relies largely on photo-generated acid diffusion. If acid diffusion can be effectively controlled, PEB sensitivity will be improved. As pattern size decreases for a higher density device, this variation can be more than 10 % of target CD.

Therefore, PEB sensitivity and diffusion length becomes vary important property for sub-90 nm pattern.

As the lithography community has moved to ArF processing on 300 nm wafers for 90 nm design rules of 90 nm and below the process characterization continues to highlight the thermal requirements for the post exposure bake (PEB) process step. The PEB is regarded as the most critical. Step for the 45 nm node photomask, and subsequent technology node generation, the performance requirements for baking systems significantly exceed from those of currently available equipment. In comparison with silicon wafers, photomask substrates exhibit markedly different thermal properties.

These differences conspire to make photomask precision baking far more difficult than is the case for wafer baking. In particular, as the thermal systems have become increasingly uniform, the transient behavior of the thermal processing system has received the focus of attention. This paper demonstrates the effect of acid diffusion length for each PEB time (90 s ~ 110 s). At the completion of the optimization process, the within wafer CD uniformity displayed a significant improvement when compared to the previous process. We also compared the acid diffusion lengths as a function of PEB time. And we calculated distribution as functions of PEB time and diffusion length.

6730-144, Poster Session

Critical dimension control for 50-nm random contact hole array with resist reflow process

J. M. Park, Y. Kang, H. Oh, Hanyang Univ. (South Korea)

50 nm random contact hole array by resist reflow process (RRP) was studied to make 32 nm node device. Patterning of smaller contact hole array is harder than patterning the line & space. RRP have a lot of advantages, but RRP strongly depend on pattern array, pitch, and shape. So we must have full knowledge for pattern dependence after RRP, and then we need to have optimum optical proximity corrected mask including RRP to compensate the pattern dependence in random array.

To make optimum optical proximity and RRP corrected mask, we must have better understanding that how much resist flows and where the

contact holes locations are after RRP. A simulation is made to correctly predict RRP result by including the RRP parameters such as viscosity, adhesion force, surface tension and location of the contact hole. As a result, we made uniform 50 nm contact hole patterns even for the random contact hole array and for different shaped contact hole array by optical proximity corrected RRP.

6730-145, Poster Session

Self-aligned resist patterning with 172-nm and 193-nm backside flood exposure on attenuated phase-shift masks

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We have investigated self-aligned resist patterning (1) for a patterning accuracy of photo mask. Self-aligned Resist Pattern can be formed by backside flood exposure on photo-mask. It had been already proved by the experiments with 248 nm light source exposure on binary (Cr on Quartz) and KrF attenuated phase shift masks.(1) Attenuated phase shift masks are generally composed of Cr/MoSiN/Quartz, MoSiN/Quartz, and Quartz layers. MoSiN layers of attenuated phase shift mask have the optical property of 6% transmittance at 248 nm light source, and the interference of the 6%-transmitted light makes the undesirable resist pattern profile on MoSiN-Quartz boundary. This paper shows the fresh possibility of the self-aligned resist pattern fabrication on attenuated phase shift masks using backside flood exposure. To solve the optical property of MoSiN layer, self-aligned resist patterns of KrF attenuated phase shift mask was fabricated using 193 nm wavelength backside flood exposure and ArF attenuated phase shift mask used 172 nm wavelength. The shorter wavelength than the normal could minimize transmittance on MoSiN area. Besides we used Negative PR to make the self-aligned resist pattern on exposed regions. These experimental concepts help to form the selective PR patterning on only quartz regions of attenuated phase shift mask.

6730-147, Poster Session

Practical use of hard mask process to fabricate fine photomasks for 45-nm node and beyond

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Photomasks for 45nm-node and beyond demand fine pattern resolution and strict CD control from fabrication process. In general, loading effect in Cr dry-etching is a major cause of CD errors in uniformity, linearity and through-pitch. Degree of this phenomenon is much affected by Cr etching selectivity and higher Cr load gives lower selectivity that makes it more remarkable. For this reason, bright-field masks as typified by gate-layer often show critically large Cr etching bias and CD range among different kinds of pattern. Although adoption of thin Cr film blanks is one of effective techniques both in reduction of etching bias and CD errors due to different Cr loads, thinning of Cr thickness has already reached its limit to keep enough optical density for ArF lithography. Most of technical issues mentioned above are caused by characteristics of Cr, and fabrication process of photomask should be reconsidered drastically to solve them.

Photomask blank with inorganic hard-mask layer is one of promising materials for 45nm-node. Advantage of this hard-mask blank is that most part of conventional process is applicable, and any special techniques are not necessary for etching, because this blank has the same structure as conventional one except for hard-mask layer.

In this study, conditions of hard-mask process have been optimized. As for dry-etching condition, adoption of highly anisotropic etching both for hard-mask layer and Cr is possible with the blanks. Much reduction of CD shift during etching was effective to suppress loading effect. It was shown that this property much contributed to improve CD performance both in linearity and through-pitch. Inorganic hard-mask layer on Cr enables to adopt the thin resist film thinner than 200nm. This contributed to improve CD controllability of fine patterns as typified by SRAFs. In resist coating, surface treatment of the blanks before coating has also been optimized to make enough adhesion of the resist on surface of the hard-mask. This technique is necessary in hard-mask process to prevent fine resist patterns from collapsing and keep pattern fidelity.

For practical use of this technique, its validity has been evaluated through the fabrication of bright-field photomasks for 45nm-node. It was confirmed that photomasks from the hard-mask blanks showed negligible small CD difference among different kinds of pattern, especially in sparse/dense and SRAFs. These results satisfied our technical demands for 45nm-node photomasks that were supposed to be difficult with conventional blanks. Patten defectivity is also a critical issue in production of advanced photomasks. Pattern defects on our hard-mask process were proved to be within the tolerance for practical use of 45nm-node photomasks.

As mentioned above, fabrication process using hard-mask blanks is applicable to the production of photomasks for 45nm-node. We believe that this technique is also effective to the photomasks of next generation, 32nm-node. Lithographic performance of the masks is under investigation. It will be also shown in this report.

6730-213, Poster Session

Ovecoming loading challenges in a mask etcher for 45 nm and beyond

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Resolution Enhancement Techniques (RET), such as (aggressive) Optical Proximity Correction (OPC) will continue to be employed for extending the limits of optical lithography at the 45 nm (half-pitch) node. Sub-resolution OPC features have burdened mask process margins. In order to improve the resolution, immersion lithography is planned to be used for 45nm, which will help to reduce the wavelength from 193nm to 132nm. Increasingly complex RET techniques need to be used in the sub wavelength regime which will drive up the mask costs, as well as the design costs. Some of the RET techniques used involve using OPC, PSM and hard mask. In order to reduce the costs it is desirable to have uniform performance on a shuttle mask, which can help to reduce the manufacturing costs. The micro loading and macro loading are of concern to the mask makers because of the varying loads being etched within the mask. It is critical to have a mask etcher that provides excellent CD uniformity, CD bias, CD linearity and etch profile in order to have image fidelity of the OPC structures as well as sustainable yields. This paper demonstrates solutions for micro and macro loading challenges on BIM and APSM masks using Applied Materials Tetra ™ III next generation mask etcher.

6730-148, Poster Session

Resistless mask structuring using an ion multibeam projection pattern generator

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The expected extension of the immersion lithography down to the 32nm node and possibly below will generate new challenges for mask makers. Dimensions of OPC features will be in the range of the smallest feature size on the wafer combined with line edge roughness problems induced by sensitive chemically amplified resists. The OPC resolution enhancement technique leads to a dramatically increased number of shots which have to be exposed by the pattern generator. Correspondingly, there will be also a significant drop in throughput when using a conventional single e-beam tool.

The multi-beam approach is considered to overcome the throughput problem. When using ions instead of electrons combined with precursor gases a resist-less pattern generation of high resolution and complex designs with an acceptable throughput becomes reality. We evaluated the IMS Nanofabrication proof of concept tool of an ion multi-beam projection pattern generator, designed for 40,000 multi-beam operation, for the resist-less patterning of a binary Cr mask.

For this purpose we used a blank, provided by a commercial supplier, consisting of the quartz substrate, a 70nm chrome and a 20nm hard mask layer. This blank type has been developed for high resolution mask making. The achievable resolution in conventional mask making using a chemically amplified resist (CAR) on top of the chrome is usually limited by pattern collapse in resist on one hand and a significant etch bias on the other hand. Etching of a Cr layer with a thickness of 50 - 70nm requires a resist film of more than 200nm and the pattern collapse occurs from an aspect ratio of 1:3. Applying the blank stack with a hard mask on top of the Cr allows reducing the resist film down to 100nm and below which improves the resolution capability. The structured resist will be etched into the hard mask and after resist stripping the hard mask can be transferred into the chrome layer underneath. In preparation of our ion patterning evaluation we developed a first structuring process for the hard mask blank using a most recent pCAR and the Vistec variable shape e-beam writer SB352HR. A resolution of 50nm features in 70nm Cr with vertical side walls has been demonstrated.

For the resist-less blank patterning the thin hard mask has been patterned by Ar ion beam milling directly. Afterwards, we applied our developed chrome etch process and transferred the hard mask into the chrome. We will demonstrate the achieved resolution, line edge roughness and feature profile. In addition, we calculated on the basis of our experimental results the throughput of a production tool, operating with precursor gases and 900.000 ion beams.

6730-149, Poster Session

Reconfigurable lithographic applications using polymer liquid-crystal composite films

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The proposed application of holographically formed polymer dispersed liquid crystal (H-PDLC) thin films is a real-time dynamically reconfigurable mask for the resist exposure step in the photolithographic process. H-PDLC films, or thin periodic nanostructures of alternating layers of polymer and liquid crystal have unique electro-optic properties including the ability to modulate a particular wavelength as a function of bias applied to the film. Current photolithography technology requires a static mask to prevent UV exposure of selected areas on the patterning surface in order to form structures in photoresist. The exposure and development process can be repeated several times with different masks to fabricate 3D structures. A real-time reconfigurable mask will allow generation of 3D structures including peaks, valleys, and grades in the resist substrate, and can potentially reduce the number of development stages in forming 3D structures.

The H-PDLC photomask device consists of a pixilated array with independent bias control over each pixel. This is achieved by etching optically clear yet electrically conductive indium-tin-oxide electrodes on the glass confining the H-PDLC film. This mask has been used to cure Shipley 1800 series positive photoresist at its peak wavelength of 436nm. A 10nm full-width half-max Gaussian wavelength filter is used to attenuate extraneous UV wavelengths emitted from the curing source. Structures formed using the H-PDLC photomask device have been compared to similar structures formed with a static photomask using an optical profilometer. Near vertical walls have been achieved using the H-PDLC photomask with resolution nearing 100μm. Line width between structures formed using the H-PDLC mask and static photomask differ by less than 15%. Additionally, comparisons have been made between adaptable photomasks made from scattering mode polymer dispersed liquid crystal films (PDLC) and H-PDLC films.

H-PDLC is formed by holographically exposing a homogeneous mixture of liquid crystal and photosensitive monomer. The resulting film microstructure consists of planes of cured polymer stabilizing regions of liquid crystal droplets in a periodic pattern. In its unbiased state, the liquid crystal droplets align randomly, creating an index mismatch between the polymer and LC regions. Reflection due to the index mismatch has a wavelength determined by the spacing of the LC and polymer layers within the film microstructure. Application of electric field across this film aligns the liquid crystal droplets along a common axis, the reflection is suppressed and the film becomes transparent.

6730-150, Poster Session

Laser micromachining of wide band-gap materials for photomask applications

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A high-precision microfabrication technology integrating two excimer laser-based techniques, laser-induced backside wet etching (LIBWE) and contour scanning, has been developed for machining wide band-gap (WBG) materials. The integrated technology developed has been applied for patterning masks using two WBG materials: calcium fluoride (CaF_2), and magnesium fluoride (MgF_2). While CaF_2 is the primary optical material for the next generation 157-nm lithography, MgF_2 has superior transmission properties to accommodate to even more restrictive optical conditions. Because of their high binding energy and great mechanical stability, the micromachining of the WBG materials, especially the CaF_2 and MgF_2 considered in this proposal, is still restricted. In this paper, the associated fundament machining behavior, including the material removal rate and the surface quality of the micromachined components as well as the efficacy of the technology developed for machining the WBG materials have been studied. The technology developed is really a single-step process without post-processing for surface quality and precision improvement. Consequently, the cost saving in fabricating the proposed high precision and high quality WBG-material masks will be essential.

6730-151, Poster Session

Pattern density and process related CD corrections at 32-nm node

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With mask critical dimension (CD) uniformity requirements becoming tighter with each new technology node, mask manufacturing must deploy a wide range of corrections to meet the CD specifications. These corrections compensate for e-beam proximity effects, fogging effects, etch loading effect, and other global process non-idealities. In this paper, we present data demonstrating that the current capability of universal e-beam dose corrections meets 32nm CD uniformity requirements in the presence of various systematic CD errors. Given that the resist process demonstrates enough latitude to accommodate the required dose variations, it is the stability and repeatability of the process itself that limits the ability to meet CD requirements. Substrates, resist coating, post-coat delay, develop variations, and etch stability all contribute to CD variations. Rather than simply focusing on reducing systematic errors, the process stability must be addressed.

6730-152, Poster Session

Pattern split rules!: feasibility study of rule-based pitch decomposition for double patterning

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To fulfill Moore's law the R&D stage of the 3x nm node will have to be reached in 2008. ArF double patterning (DP) is the main candidate to achieve this in time. Geometrical pattern split, doubling the pitch, is one of the major steps of DP technology.

In this paper we present a feasibility study of the Rule Based (RB) DP approach to pattern splitting based on a representative and reviewed selection of clips and full-mask designs.

The elements of this approach include split rules derived from Process Window simulations; Rule Based algorithm developed and trained by applying it to selected designs and RB post-split checks tested on selected designs.

The limitations of the RB pattern split were investigated on various clips and full-chip layouts. The necessity of Design for Manufacturing (DfM) and Model Based (MB) pitch split is discussed.

6730-153, Poster Session

Automatic residue removal for high-NA extreme illumination

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An epidemic for smaller node has been that, as the device architecture shrinks, lithography process requires high NA(Numerical Aperture), extreme illumination system. This, in turn, creates many lithography problems such as low lithography process margin (DOF , EL), unstable CD uniformity and restricted guideline for device design rule and so on. Especially for high NA extreme illumination such as immersion illumination systems, above all the related problems, restricted design rule due to forbidden pitch is critical and crucial issue. This forbidden pitch is composed of numerous optical effects but majority of these forbidden pitch compose of photo resist residue and these residue must be removed to relieve some room for already tight design rule.

In this study, we propose automated algorithm to remove photo resist residue do to high NA and extreme illumination condition. This algorithm automatically self assembles assist patterns based on the original design layout, therefore insuring the safety and simplicity of the generated assist pattern to the original design and removes any resist residue created by extreme illumination condition. Also we will evaluate our automated algorithm on full chip FLASH memory device and show the residue removal effect for both commercial verification tools as well as on actual wafer.

6730-154, Poster Session

Effective area partitioning for preparing a distributed parallel processing in mask data preparation

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Mask Data Preparation (MDP), which typically consists of Boolean operations, sizing, and fracturing, requires intense computing power. For today's increasingly large data, utilizing distributed parallel processing with multiple CPUs or using a host server is an established approach to reduce turn around time (TAT). Before starting a parallel process, a data analysis is required for the preparation process, which has to be executed in sequential manner and thus heavily affects the overall TAT. An inadequate preparation process however causes uneven load distribution for the parallel processing; therefore increases TAT. It is a difficult task for balancing especially when a large number of parallel processes are used. The methodology of an effective preparation process is suggested in this paper, where MaskStudio fracturing system is used for testing and analysis. In the preparation process, MaskStudio uses methods of area-based partitioning. In this process, the OASIS format is applied for intermediate file regardless of the input data type, and the hierarchy of the input data for GDSII or OASIS layout-data is preserved. After this preparation step, each partitioned data is processed for Boolean operation, sizing and mask rule check (MRC) in parallel processing. This resulted preventing of TAT increase even for running a large number of parallel processing.

6730-155, Poster Session

Compressing MEBES data enabling multithreaded decompression

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With the resolution enhancement techniques such as OPC (Optical Proximity Correction) and SRAF (Sub-Resolution Assist Features), the size of layout data have grown significantly. It is quite common now to find layout files that are tens of GBs in size. Unlike GDSII which can store data hierarchically, mask data formats such as MEBES are essentially flat and more voluminous. Moreover, polygonal data present in layout data files are fractured and thereby increasing the data volume before getting stored in MEBES data format. This results in very huge MEBES files. As per the ITRS roadmap of 2005, for a 45nm half-pitch node that is expected to be in use by 2010, the mask data volume for a single layer is expected to reach up to 825 GB. Storing and transferring such large mask data are issues for which the mask industry needs solutions.

Historically, MEBES is the most prevalent EB format in the industry. Moreover, in many MDP flows, the MEBES format is being used as de-facto standard for specifying the fractured EB data even though the final target EB machine might be different. In this paper we present techniques for lossless reversible compression of MEBES data, i.e., when the compressed file is decompressed, the generated uncompressed file matches the original MEBES file bit-by-bit. By applying these compression techniques a compression ratio of 5X to 15X can be obtained.

In practice, compressing MEBES files is usually a one-time task, but decompression of compressed files is expected to be done multiple times as every time a compressed MEBES file needs processing, it has to be decompressed. MEBES is essentially an efficient data format and the geometries are stored compactly. As a result the compression/decompression techniques described in this paper are quite computation intensive in order to achieve higher compression ratio. This in turn leads to higher CPU time for compression/decompression compared to generic compressors such as gzip. However, as the format-specific compressors produce higher compression ratios, the disk I/O time for compression and decompression is expected to be less compared to the generic compressors such as gzip and gunzip. In spite of this, the format-specific decompressors are usually 3-5X times slower than the generic decompressor such as gunzip. Since decompression is expected to be done more frequently compared to compression, speeding up decompression is highly desirable. We present a compression technique for MEBES data which enables multiple threads to decompress the compressed MEBES data. With the multi-core multiprocessor machines becoming quite inexpensive and common, the multi-threaded decompression is expected to be close to disk I/O time on such machines.

The paper details out the techniques, experimental results in terms of comparative compression ratios, compression and decompression speed using single threads and multiple threads. The possibility of getting higher compression ratios as well as higher or comparable decompression speed makes it more practical to use format for specific reversible compression schemes rather than using generic compressors. Even though, the paper focuses on compression and decompression of MEBES, it can be easily extended to GDSII.

6730-156, Poster Session

Mask calibration dominated methodology for OPC matching

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As microlithography moves to smaller critical dimension, optical proximity correction (OPC) is widely used in the semiconductor industry to compensate for optical proximity effects and process variation occurring when printing features below exposure wavelength. However, it is not easy to achieve a stable OPC model or OPC algorithm, because many process-induced errors will reduce OPC accuracy. While the optical system can be physically described by Hopkins Equations, the characterization of mask, resist and etch loading effects is mainly empirically derived, which requires the collection of a significant amounts of test pattern data.

Generally speaking, the effectacy of the OPC model depends greatly on test pattern data calibration that accurately captures mask and wafer processing characteristics. The CD deviation caused by an off-center mask process can easily consume the majority of the lithography process CD budget. Mask manufacturing variables such as write tools' resolution, etch process effects, and pre-bias of the fractured data have great impact on OPC model performance. As a result, wafer performance using masks from different mask shops vary, even if the masks have the same pattern and use the same manufacturing specification, due to differences in mask manufacturing process. However, it is common for a FAB without a mask shop to cooperate with several mask shops to meet

cost and timing goals. Since sometimes it is impossible for a FAB to re-build an OPC model due to an urgent tape-out schedule or turn around time (TAT), how OPC calibrate the new mask process can be a problem.

Conventional papers concerning mask making and OPC modeling mainly focus on the tradeoff between mask rule and aggressive OPC dissection or mask manufacturing process-induced OPC performance variation, without addressing this FAB-oriented problem. According to our study, there are two methods to solve this problem: the mask calibration dominated method, which calibrates mask manufacturing while keeping the OPC model constant, or OPC model calibration dominated method, which calibrates the OPC model without introducing the mask calibration procedure. In this paper, we will focus on the former method. For the first time, we propose the methodology and flow of mask manufacturing calibration in order to make OPC model consistent. The methodology consists of two parts: mask manufacturing calibration and wafer-level OPC accuracy verification. Mask manufacturing process and metrology are calibrated separately. The OPC model is built based on the database of the first-party mask shop, and OPC verification is carried out by wafer data using the newly calibrated mask from the second-party mask shop. By checking wafer performance of both OPC model matrix items and complicated 2D structures, the CD difference and the overlap between simulation contour and SEM images are briefly presented, from which we can draw the conclusion that different mask shops can share one common OPC model with rigorous mask calibration. This methodology leads to a lower engineering cost, a shorter turn around time and robust OPC performance.

6730-157, Poster Session

Integration of OPC and mask data preparation for reduced data I/O and reduced cycle time

J. Yu, R. E. Morgan, Synopsys, Inc.

As process geometries continue to shrink, the resulting increases in design complexity and chip pattern density have fueled a data explosion on advanced semiconductor designs. This extends product development cycles and potentially impacts product yield.

Two areas in the design flow that are most adversely affected include both mask synthesis (OPC, RET) and Mask Data Preparation. Minimizing data I/O and providing an integrated OPC and mask data preparation solution, plays an increasingly critical role in reducing the mask synthesis and mask data prep total cycle time.

In this paper, an integrated flow of Proteus OPC and CATS MDP are discussed. This integrated flow virtually eliminates the data I/O step between OPC and MDP pre-processing and delivers faster total turn around time by effectively eliminating the time originally spent on MDP pre-processing. The integrated flow and its turn around time performance will be presented.

6730-158, Poster Session

Mask rule check using priority information of mask patterns

K. Kato, SII NanoTechnology Inc. (Japan)

Mask rule check (MRC) has become an essential process before manufacturing photomasks as patterns on photomasks are getting more complex due to RET and OPC technologies. MRC can contribute to the reduction of mask costs and TAT by not only rejecting erroneous mask data before writing them with e-beamEB/laser drawing machines but also feeding forward false error candidates to mask inspection machines to avoid numerous false errors detection. In the last presentation (2006), we introduced our mask rule check software SmartMRC. It was shown that SmartMRC can check on mask manufacturability of handle huge volume mask Jobdeck data within reasonable time.

Since 2006, Association of Super-Advanced Electronics TechnologiesResearch Department

(ASET) has started a project called "Mask Design, Drawing and Inspection Technology (MaskD2I)" with the sponsorship from The New Energy and Industrial Technology Development Organization (NEDO). SIINT has joined the MaskD2I project and we have been developing MRC software considering DFM information for more effective data inspection.

By converting design level information called as "Design Intent" to the priority information of mask manufacturing data called as "Mask Data Rank (MDR)", the MRC process based on the importance of reticle patterns is possible. Our main purpose is to build a novel data checking flow with the priority information of mask patterns extracted from the design intent. The information we refer to as design intent includes the following information:

- dummy metal/cell information
- critical net names
- shield metal lines
- active regions of transistor gates

In this paper, we address the effectiveness of MRC technologies which have been widely applied in many mask data fields. Then we present the current status of the new MRC development, its experimental results so far and the future outlook using further Design Aware Manufacturing (DAM) information.

A part of this work was done at ASET with the support of NEDO.

6730-159, Poster Session

Improving the efficiency of pattern extraction for character projection lithography using OPC optimization

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This research proposes an approach to improve the pattern extraction efficiency for character projection lithography (CPL). CPL is one of the promising technologies in electron beam direct-write lithography. CPL has the advantage in reduced electron beam (EB) shot numbers, compared with conventional variably shaped beam lithography, because the each of character patterns that frequently appear in the layout can be collectively written by one EB shot with the CP aperture mask. Namely, it is important to extract frequently used character patterns and prepare the CP aperture masks in order to reduce the EB shot numbers. However, in the random logic devices, one character pattern may be generated many diversified patterns with complicated optical proximity correction (OPC) features, and they can not be extracted as a unique CP aperture mask.

In order to overcome this problem, we propose the method to improve the pattern extraction efficiency for CPL in the random logic devices using OPC optimization. Our proposal method can reduce the variety of diversified patterns with two developed algorithms: (1) the pattern grouping algorithm which categorizes diversified patterns and extracts some typical pattern groups, (2) the OPC optimization algorithm which regards the patterns in a group as one typical pattern and corrects the OPC features of the typical pattern to become the CP aperture mask. In conducted experiments, we successfully achieve the 30% improvement in the extraction efficiency.

6730-160, Poster Session

A user-programmable link between data preparation and mask manufacturing equipment

W. Zhang, E. Y. Sahouria, S. F. Schulze, G. Davis, Mentor Graphics Corp.; A. Seyfarth, Carl Zeiss SMS GmbH (Germany); E. R. Poortinga, Carl Zeiss SMT Inc.

In order to fully exploit the design knowledge during the operation of mask manufacturing equipment as well as to enable the efficient feedback of manufacturing information upstream into the design chain close communication links between the data processing domain and the machine are necessary.

With shrinking design rules and modeling technology required to drive

simulations and corrections the amount and variety of measurements for example is steadily growing. This requires a flexible and automated setup of parameters and location information and their communication with the machine.

The paper will describe a programming interface based on the tcl/tk language that contains a set of frequently reoccurring functions for data extraction and search, site characterization and filtering, coordinate transfer . It enables the free programming of the links adapting to the flow and the machine needs. The interface lowers the effort to connect to new tools with specific measurement capabilities and reduces the setup and measurement time. The interface is capable of handling all common mask writer formats and their jobdecks as well as OASIS and GDSII data.

The application of this interface is demonstrated for the Zeiss AIMS TM system.

6730-161, Poster Session

32-nm half-pitch node OPC process model development for three-dimensional mask effects using rigorous simulation

L. S. Melvin III, Synopsys, Inc.

32 nm half-pitch node processes are rapidly approaching production development, but most tools for this process are currently in early development. This development state means that significant data sets are not yet readily available for OPC development. However, several printing effects are thought to become more prominent at the 32 nm half-pitch node. One of the most significant effects is the three dimensional (3D) mask effect where the mask transmittance and phase are impacted by the mask topography. Already at larger process nodes this effect impacts imaging performance, especially when sub-resolution assist features are employed. For the 32nm node it is essential that this effect is correctly captured by the OPC model. As wafer data for the 32nm half-pitch is difficult to obtain, the use of rigorous lithography process simulation has proven to be invaluable in studying this effect. Using rigorous simulation, data for OPC model development has been generated that allows the specific study of 3D mask effect calibration. This study began with Kirchhoff based simulations of 32 nm node features which were calibrated into Hopkin's based OPC process models. Once the standard Kirchhoff effects were working in the OPC model, 3D mask effects were included for the same data by performing fully rigorous electromagnetic field (EMF) simulations on the mask. New EMF compensation methodologies were developed to approximate 3D mask effects in a fast OPC process simulation. These methodologies modify the phase and transmission of features to compensate for 3D mask effects in a fast OPC model. The OPC model was then refit including the 3D mask effect and found to generate as much as 5 nm differences between the fit Kirchoff data and the fit 3D mask data. In addition, the Hopkin's based OPC model with new EMF compensation methodologies has been able to fit the 3D mask data with an RMSE value of 0.52 nm and a range of 2.76 nm.

6730-162, Poster Session

OPC verification on cell level using fully rigorous mask topography simulation

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Starting with the 45nm node, the minimum feature sizes on the mask have reached sub-wavelength dimension. In this regime the electromagnetic field induced in the mask is significantly impacted by the mask topography. These so called mask topography effects play an important role in the image formation process and need to be compensated for in the OPC model. Looking ahead to the 32nm process node, mask topography effects will become even more pronounced. So, including these effects into the OPC model has become a must for advanced process nodes. Modern OPC engines start to apply electromagnetic field (EMF) compensation techniques to take these effects into account. Of course, due to the severe run time constrains on OPC model generation these EMF aware OPC models need to rely on approximate methods. A reliable OPC verification process therefore should include a fully rigorous treatment of the mask topography effects with taking into account oblique light incidence. In this paper we present the impact of rigorous mask topography simulation on the reliability of the OPC verification step and determine the influence of EMF aware OPC models on OPC quality. For this, we use lithography simulations on OPCed layout cells where we apply a fully rigorous parallel EMF solver to the mask model. Two different OPC models are used in this study, one using EMF compensation techniques and one based on the conventional approach. The results of the lithography simulations are used to verify both OPC models. The impact of the EMF simulation on OPC verification quality is shown by direct comparison to corresponding Kirchhoff simulations for both OPC models.

6730-163, Poster Session

EMF simulations of isolated and periodic 3D photomask patterns

S. Burger, L. W. Zschiedrich, F. Schmidt, Zuse Institute Berlin (Germany); R. Koehle, Qimonda AG (Germany); B. Küchler, C. Nölscher, Qimonda Dresden GmbH & Co. OHG (Germany)

Rigorous EMF simulations have become an important tool for mask design in low k_1 applications.

As has been shown in previous works finite-element simulations are superior in terms of simulation accuracy, convergence rate and computation speed when compared to other presently used EMF simulation methods [1,2].

We report on the current status of the finite-element solver JCMsuite, incorporating higher-order edge elements (up to 9th order), adaptive refinement methods, and fast solution algorithms.

We present results from the application of the solver to 3D isolated and periodic photomask patterns. The authors are responsible for the content of the paper.

[1] S. Burger, R. Koehle, L. Zschiedrich, W. Gao, F. Schmidt, R. Maerz, C. Noelscher, Proc. SPIE Vol. 5955, 18-26 (2005).

[2] S. Burger, R. Koehle, L. Zschiedrich, H. Nguyen, F. Schmidt, R. Maerz, C. Noelscher, Proc. SPIE Vol. 6349, 192 (2006).

6730-43, Poster Session

The study of haze generation as thin film materials

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Exposure wavelength has been shortening from i-line to ArF laser to embody the high resolution as critical dimension (CD) shrinkage and the specifications have been stricted for high quality products in semiconductor and mask industry. However, new defect issue called haze was appeared as shortening of wavelength. This defect was caused by photoreaction of chemical residues among SO42-, NH4+ and others by exposure. Accordingly, we investigated the haze characterization and mechanism as compounds of molybdenum (Mo) and silicon (Si) based thin film materials in this paper.

For fabrication of various thin films, the materials were deposited on the quartz substrate with sputtering conditions and reactive gases. Firstly, haze defects were inspected after exposure to evaluate the difference of haze generation as thin film materials. And then, the ions and aromatic hydrocarbon compounds on the surface were measured by thermal desorption gas chromatography/mass spectrometer (TD GC/MS) and ion chromatography (IC). Also, the relation between haze generation and thin film materials such as composition ratio of N, C, O and metal was observed and the effects of heat treatment were investigated to minimize haze generation as materials.

6730-166, Poster Session

A method to determine the origin of remaining particles after mask blank cleaning

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Extreme ultraviolet lithography (EUVL) is a strong contender for the 32 nm generation and beyond. A defect-free mask substrate is an absolute necessity for the manufacturing of EUV mask blanks. The mask blank substrates are, therefore, cleaned with different cleaning processes to remove all defects down to 30 nm. However, cleaning suffers from the defects added by various sources such as the fab environment, chemicals, ultra pure water, and the cleaning process itself. The charge state of the substrate during and after cleaning also contributes to the number of adder defects on the substrate. The zeta potentials (Fig.1) on the substrate surface and the defect particles generated during the cleaning process determine whether the particles get deposited on the surface. The zeta potential of particle or substrate surfaces depends on the pH of the cleaning fluids. Therefore, in this work, pH-zeta potential maps are generated for quartz substrates during the various steps of mask cleaning processes. The pH-zeta potential maps for defect particles commonly seen on mask substrates will be measured separately. The zeta potential maps of substrate and contaminant particle surfaces will be used to determine whether particles are attracted to or repulsed from the substrate. In practice, this technique is especially powerful for deriving information about the origin of added particles in a cleaning process. For example, for a known adder with a negative zeta potential, all cleaning steps with a positive zeta potential substrate could be the source of added particles. Additionally, a zeta potential map versus cleaning step is useful for tool matching purposes.

6730-168, Poster Session

Study of time dependent 193-nm reticle haze

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While significant progress has been made in reducing the occurrence rate of progressive defect growth on photomasks at 193nm, the issue continues to be a problem for many semiconductor fabs. Increasing evidence from multiple sources indicates that further reduction in haze risk involves closely controlling the storage and exposure environment of the photomask. Further controlled testing is necessary to characterize the impact of environment and individual components on growth. In this way, photo mask users, equipment and material providers may be better prepared to ensure the proper storage and use of photomasks in order to reduce the risk of haze growth.

In continuation of work previously reported by Toppan Photomask, advanced test apparatus, recently designed and built, now enables researchers to generate and maintain stable and controlled levels of multiple impurities which potentially effect haze growth down to single part-per-trillion range. Supported by on-line and off-line analytical methods and instrumentation, new experimental set-up enables unprecedented accuracy in the testing and validation of research concepts.

Different classes of pollutants in multiple combinations have been studied to more precisely characterize environmental sensitivity of varying types of 193 nm reticles.

Authors report further groundbreaking progress on the study of the effect of environmental conditions on severity and rate of haze formation to provide insight into the requirements for reducing or even preventing such conditions.

6730-169, Poster Session

An approach to prevent retilce ESD damage and haze contamination

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The control of ESD and haze contamination on reticles have been gaining an ever-increasing focus as semiconductor manufacturers face yield losses attributed to them. Yield improvement through the reduction of haze and ESD damage on reticles is now a significant challenge as the use of 193nm light source and shrinkage of line width on reticles. In this study, we focus on the choice of material of reticle SMIF pod (RSP) and the design of RSP in order to reduce the ESD damage and haze contamination.

To avoid the ESD/EMI issue on the reticles, our first step is to avoid electrostatic charge generating on the reticle, and the second is if ESC is generated, slow dissipation of ESC to ground is the key to avoid ESD damage. Reticle is normally stored in RSP in the fab, and metal is considered to be the best to protect the reticle in term of electrostatic shielding; however, the weight is an important issue to limit its application. PEEK is a good material based on previous study, but the cost is much higher than all other engineering polymer. ABS, PC, PMMA, PEEK and a new EMI shielding material were used as material of RSP in this study, and electrostatic field and electromagnetic shielding effect of these RSP were tested. Our results show that EMI shielding material shows the best result on these tests. The design of RSP in order to safely dissipate ESC to ground is discussed, and ESD control strategy in a mass production fab is also proposed. The outgas of RSP material is believed to be one of the causes of haze by various previous studies, and the outgas and leaching data of these materials for RSP were also tested and compared.

For RSP design, common solutions for haze prevention are purging with N2/CDA, the use of chemical filter, choose of low outgases material for RSP...etc. In this study, we proposed the use of a sulfate adsorption plate to chemically react with SOx in RSP to prevent the formation of ammonia sulfate. The color of adsorption plate is an indicator of when the adsorbent on the plate is depleted.

6730-170, Poster Session

Evaluation of photomask package and storage environment and its effect on haze generation

J. Kim, PKL Co., Ltd. (South Korea)

Haze defect issues are becoming more and more serious issues, as ArF lithography became main part of photolithography area these days. Also many photomask makers are now finding solutions such as Chemical Free Cleaning, adapting Hot DI water rinse, thermal treatment and UV treatment in cleaning process, etc. However, It turns out that haze defect is not only mask cleanness problem but also there are environment factors.

In this study, we focus on environment issues where photomask lies from delivery condition to shelf atmosphere. And what we should do for the mask not to generate haze defects during not only exposure condition but also shelf condition. Delivery and mask storage materials are evaluated depending on its material, outgassing element, and its effect on mask surface.

6730-171, Poster Session

Laser shockwave cleaning of EUV reticles

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Because EUV reticles need to be operated without a pellicle, they are likely to be subjected to organic and inorganic particle contaminations. These particles need to be removed from the reticle, because they can cause serious defects in the projected image at wafer level. Therefore a cleaning method needs to be developed, that can remove particles as small as 30 nm without damaging the reticle.

Laser Shockwave Cleaning (LSC) is a cleaning method that shows great promise as a fast and dry cleaning process. This method is based on the shockwaves generated by the optical breakdown of air, which is accomplished by focusing the light of a Nd:YAG laser pulse. To test the effectiveness of this method, a number of cleaning experiments were performed on wafers contaminated with glass and polymer spheres at both

atmospheric and reduced pressure. The results of these experiments showed that both gap distance and laser power are important cleaning parameters. Time resolved Schlieren imaging experiments were done to study the properties of the shockwave. The acquired Schlieren images revealed information about the shape and velocity of the shockwave. The interaction of the shockwave with the surface of the wafer was also clearly visible.

Laser power is an important cleaning parameter for LSC, but the price of high powered laser systems makes the step towards higher pulse energies economically unattractive. To circumvent this problem, a modified LSC method was developed to improve the cleaning efficiency at lower laser pulse energies.

6730-172, Poster Session

Mask protection from a haze

T. Umeda, Adhand, Inc. (Japan)

Mask Protection from a Haze While Shipping and Storage

Haze issue is one of critical matter in photolisography process. To protect mask from a haze while shipping and storage, there are two efficient ways. One is to use low out gas material for shipping and storage case and the other one is set absorbents in them.

Low out gas material for case

We recommend PC+CF material. Because of the TOC density is one tenth compare with PMMA material (Fig. 1).

Absorbents

Even if PC+CF material have outgas and this is cause to growth a haze while shipping and storage in the case. An absorbent decreases TOC density in the case and absorb penetrate gas (Fig.1).

Fig 1. The various of TOC density for PMMA or PC+CF case and with or without an absorbent.

6730-173, Poster Session

Signature evaluation using scatterometry

J. Richter, Advanced Mask Technology Ctr. (Germany); J. C. Lam, n&k Technology, Inc.

The current abilities for active feedback loops to correct for various parameters challenge metrology groups to provide exact input data for these correction cycles. One of the most important one is the feed back loop that triggers improvements of the CD (critical dimension) uniformity of printed structures. Recently methodologies like the exponentially weighted penalty approach called TPS (thin plate splines) have been developed that separate between the somehow true signatures on the millimetre scale from the noise of the micrometer measurements. In this paper, we will close one existing gap which is the question what signature TPS actually describes. We show that the found statistically stable CD signature of a CD SEM measurement is equal to the raw measurement data of a scatterometer and we show that raw measurement data of a scatterometer equal the TPS fit of the same data.

This is of high importance since TPS and scatterometer do essentially the same, they average out micrometer noise with the only difference being: TPS does it theoretically and a scatterometer does it experimentally. Thus, we report on the extremely fortunate situation where theory and experiment give the same results. Hence, it can be looked either way, the scatterometer measures indeed macroscopic stable CD signatures and TPS is indeed the right method to extract these signatures from any given raw data.

In all we show the equivalence of two very different techniques to extract statistically stable CD signatures. This is a major step forward for the process development and active correction of CD uniformity.

6730-174, Poster Session

Parameter sensitive PSM patterns for scatterometry monitoring

J. Xue, Y. Ben, M. A. Miller, C. J. Spanos, A. R. Neureuther, Univ. of California/Berkeley

Parameter specific scatterometry test patterns and their sensitivities are assessed through simulation verification. The test patterns utilize phase shifting-masks to create unusually sensitive resist images that can be read by scatterometry and

quantitatively interpreted. Line based patterns have been designed with enhanced sensitivity to focus and illumination. The patterns are based on spillover among features that takes into account the phase of the spillover and the relative phase and partial-coherence of the illumination. This paper will first describe the design concepts that utilize the diffraction limited and aberrated point spread functions. The linear phase variation across the mask with off-axis illumination is also considered. The paper then describes several 1D patterns suitable for reading with commercial scatterometry. The performance of these patterns is then simulated to estimate sensitivity. The patterns utilize a thin non-printing test line as a detector that produces an intensity of about 0.25. This test line is then induced to print in the presence of the particular

phenomena under test. For focus, a 90 degree phase shifted test line is used onto which adjacent lines spillover with defocus. This leads to resist removal proportional to the amount of defocus. For a 90o test-line, the response is nearly linear with negative defocus at the slope of 0.6 clear field per Rayleigh unit. This target is thus several times more sensitive to defocus than typical device patterns, for which the spillover is out of phase. Off-axis illumination can be detected in a similar style of

patterns in which the line phase and adjacent line spacing are adjusted.

6730-175, Poster Session

Long-term critical dimension measurement performance for a new mask CD-SEM: S9380M

Z. Wang, K. K. Seet, R. Fukaya, Y. Kadowaki, N. Arai, M. Ezumi, H. Satoh, Hitachi High-Technologies Corp. (Japan)

The S9380M is a new mask CD-SEM (Critical Dimension Scanning Electron Microscope) developed for measurement and inspection of 45nm node photomask (mass production) and 32 nm node photomask (research phase). Newly developed optical modes, image processing technique, and an integrated mask pre-treatment module enable the S9380M to have superior performance for a wide variety of photomasks (binary, phase shift, resist, etc) A difficult issue in metrology is to acquire long-term repeatability for CD measurements. We showed that measurements taken using the S9380M have good short-term dynamic repeatability ($3\sigma< 0.6$ nm), as well as long-term dynamic repeatability ($3\sigma< 1.0$ nm).

Short-term dynamic measurement is defined as 10 dynamic measurements with stage movement and auto-focus carried out without mask load/unload. Optical modes customized for different photomasks are designed to balance the incoming and outgoing electrons, minimizing undesirable effects of charge-up and drift during SEM observations. Measurements were carried out at a magnification of 80~100k, higher than the conventionally used 50k, to obtain better image resolution for 45 nm node photomask pattern. Superior magnification linearity ensures variations in CD values are within dynamic measurement errors in the magnification range of 50k~100k. Besides, a new algorithm for contact hole pattern recognition has been introduced to enhance the pattern matching and measurement box location precision, which is sensitive to pattern irregularity and edge roughness. With these optimizations, we achieved a $3\sigma$of less than 0.6 nm (without trend modification) for 10 dynamic measurements of line and hole patterns (pattern size ~500 nm).

Long-term dynamic measurement is defined as a 5-day measurement loop, by repeating the short-term dynamic measurement once per day with load/unload. With measurement conditions optimized for short-term dynamic measurement, we identified that two main factors contributing to long-term measurement errors are electron beam instability and variation in the mask surface condition. It is known that electron beam instability can induce a magnification change and/or focus error during mea-

surements. As a counter-measure to electron beam instability, a built-in function is constructed to automatically adjust the beam prior to recipe measurements. In addition, a 172nm ultra-violet (UV) cleaning unit is integrated into the SEM system for pre-treatment of the mask, to clean the surface and remove static charge. UV irradiation is an effective method to remove contaminations on the mask and prevent adhesion of contaminants during beam observation. It can also remove static charge on the mask caused by daily mask handling. By adopting all these measures, typical 3σ(without trend modification) result smaller than 1 nm for the long-term dynamic measurement is achieved.

A more detailed description for the methodology and measurement data will be presented in the proceeding. Linearity and screen unification adjustments by utilizing a standard magnification calibration specimen, microscale will be discussed. Versatile measurement techniques appropriate for optical proximity correction (OPC) patterns, and 2D metrology will also be given.

6730-177, Poster Session

Images in photoresist for self-interferometric electrical image monitors

J. A. Holwill, A. R. Neureuther, Univ. of California/Berkeley

Self-interferometric electrical image monitors have been designed and tested in photoresist, which are sufficiently sensitive to produce an open circuit after 0.6 Rayleigh Units defocus, and thus detect when the process is at the edge of the process window. The monitor is an adaptation of the highly sensitive Pattern-and-Probe monitors for focus, and has been modified to enable electrical testing to replace SEM image inspection. An automated process using a probe station can be used to detect either an open or short circuit, which indicates the range of the aberration present in the stepper. In this paper, results are presented with SEM images of the lines which would be electrically probed, if metal had been used, showing breaks in the circuits at higher levels of defocus and short circuits closer to best focus. One such result is shown in Figure 1, with a 0.15μm line.

The experiment was conducted in a preliminary double exposure version of the monitor, which is eventually to be integrated into a single exposure design. The approach taken is to perform a double exposure, of which one is a minimum-sized feature with electrical probe pads. Before developing, the second exposure is made of the highly sensitive interferometric pattern, centered on the minimum-sized line. The presence of aberration in the system causes an open to be made on the line. Misalignment is accounted for by placing multiple patterns on the mask, translated a small amount so that at least one will be centered exactly over the line.

A large number of parameters of the monitors were varied in the experiement, such as the number of rings, linewidth and center probe size. The reactions of the monitors to variations in these parameters are explored, and recommendations for the optimal combination of parameters for the design are given.

The Pattern-and-Probe monitors for this experiment were placed on a multiple student phase shift mask, and were validated by means of SEM images in photoresist on wafers shot at 0.193nm with an NA of 0.85, with 40nm focus steps.

6730-178, Poster Session

Ultra-fine stage for CD-SEM

K. Takahashi, Holon Co., Ltd. (Japan)

The Critical Dimension Scanning Electron Microscope; CD-SEM is an indispensable system in mask and wafer manufacturing.

As the feature size of future technology node is getting smaller, the requirement for CD-SEM performance will be tougher and tougher. The number of measurement points may tend to increase. It is getting very important for CD-SEM to position the measurement patterns precisely. CD-SEM needs to be improved in stage positioning accuracy (or repeatability).

Holon has developed the Ultra Fine Stage system which combines the fine controlled stage, current Ultra Sonic Motor Stage and our originally designed “Stage mapping method”.

The CD-SEM might be possible enough to meet the requirements of 32nm node or beyond. The conventional CD-SEM usually requires the stage positioning at low magnification. As the new development system can make accurate positioning without the process, it gives a big improvement in the throughput.

Holon has completed development of the Ultra Fine Stage System installed for next generation of CD-SEM and would like to introduce it to users of CD-SEM in this paper.

6730-179, Poster Session

The study for close correlation between mask and wafer to optimize wafer field CD uniformity

M. Kim, Y. Choi, O. Han, Hynix Semiconductor Inc. (South Korea)

As device pattern size is shrinking to below 65nm on wafer, the small amount of CD variation on wafer field determine the wafer yield. The most of wafer field CD variations come from mask CD variation across mask field. By correction of dose and transmittance on mask using wafer field CD variation, wafer CD uniformity can be extremely enhanced. To get fine correction of wafer field CD uniformity, we have developed various methods to get close correlation between mask and wafer field CD uniformity by SEM, scatterometry and area CD methods. Especially, area CD from CD SEM and optical CD measurement tools are developed to represent each area of masks. By optimizing measurement methods, repeatability and correlation of CD uniformity between mask and wafer are enhanced to get more than 0.9 of correlation between mask and wafer. And these give us the correction method to compensate field CD variation of mask CD on wafer. More than mask specification requirement on 65nm tech of DRAM memory device has been achieved.

6730-180, Poster Session

Development of a captured image simulator for the differential interference contrast microscopes aiming to design 199-nm mask inspection tools

M. Shiratsuchi, Y. Honguh, Toshiba Corp. (Japan); R. Hirano, R. Ogawa, M. Hirono, Advanced Mask Inspection Technology, Inc. (Japan)

The CD (critical dimension) of semiconductor production is getting smaller and smaller each year. A phase shifting mask is one of the expected technologies to be developed to further reduce the CD. To utilize such masks of new types it is inevitable to develop a mask inspection technology to check them properly, and such technology is not established yet.

Among many observation methods, the DIC (differential interference contrast) is one of a few methods that can be used to observe a differentiated phase shift of transmitted light through an object with high resolution. Therefore, we need to grasp the performance of DIC as one candidate for phase mask inspections.

Formerly, we reported on a development of a captured image simulator based on rigorous coupled-wave analysis (RCWA) to study optical setup that is suitable for inspection of Alt-PSM. It can calculate accurate image profiles expected to be captured by inspection systems. It also takes into account of varieties of pupil conditions and 3-dimensional structure of masks. However, our former simulator cannot handle the DIC systems because of the complex structure. So we decided to develop a new captured image simulator to study a behavior of DIC systems.

The basic scheme of our simulator is the same as our former simulator. We have adopted a partial coherent imaging system as a model of the optical setup for the simulation. Diffractions on the mask surface are calculated with RCWA. There are some components that are not in the normal observation optics, namely polarizers and birefringent components as Wollaston (or Nomarski) prisms. Our former simulator can already take into account the effect of polarizations. Further, we modeled a Wollaston prism as a phase shifting plate, on which the amount of phase shift attached to e-light is linearly increasing along one axis, and to o-light linearly decreasing.

With this simulator, we did some simulations to see sensitivities of DIC for bumps or divots with several sizes as test cases, and we have got some interesting results. We found that total amount of light decrease with adoption of DIC system, but that the differences caused by defects are kept almost the same, and contrast for small defects with size around 20 to 50 nm is much higher, comparing to the normal observation optics (with sigma 1). Furthermore, we can see the difference of sensitivity between longitudinal and lateral directions, and also we can see that the line width of the captured image may vary with the same shear length but in opposite directions.

DIC requires special optical setups, but it has some interesting characteristics and it should be a candidate for phase mask inspection optics. We made sure that our simulator could be a useful tool for studying, designing, and developing mask inspection tools.

6730-182, Poster Session

Improvements in model-based assist feature placement algorithms

B. Painter, L. D. Barnes, J. P. Mayhew, Y. Wang, Synopsys, Inc.

Demanding process window constraints have increased the need for effective assist feature placement algorithms that are robust and flexible. These algorithms must also allow for quick ramp up when changing nodes or illumination conditions. Placement based on the optical components of real process models has the potential to satisfy all of these requirements. We present enhancements to such a model-based assist feature method that has been discussed previously. These enhancements include

— image-processing improvements for contact-via layer AF placement,

— model-based MRC conflict resolution,

— application to line-space patterns, and

— a novel placement technique for contact-via using a specially-built single modeling kernel.

6730-183, Poster Session

An approach of auto-fix post-OPC hot spots

C. Wang, Q. Liu, Semiconductor Manufacturing International Corp. (China); L. Zhang, Mentor Graphics Corp. (China)

With the design rule shrinks rapidly, full chip robust Optical Proximity Correction (OPC) will definitely need loger time due to the increasing pattern density. Furthermore, to achieve a perfect OPC control recipe becomes more difficult. For, the critical dimension of the design features is deeply sub exposure wavelength, and there is only limited room for the OPC correction. Usually very complicated fragment commands need to be developed to handle the shrinking designs, which can be infinitely complicated. So when you finished debug a sophisticated fragment scripts, you still cannot promise that the script is universal for all kinds of design. So when you find some hot spot after you apply OPC correction for certain design. The only thing you can do is to modify your fragmentation script and try to re-apply OPC on this design. But considering the increasing time that is needed for applying full chip OPC nowadays, re-apply OPC will definitely prolong the tape-out time. We here demonstrate an approach, through which we can automatically fix some simple hotspots like pinch, bridging. And re-run OPC for the full chip is not necessary now. However, this work is only the early study of the auto-fix of post OPC hot spots. There is still a long way need to go to provide a perfect solution of this issue.

6730-184, Poster Session

Three-dimensional mask modeling with oblique incidence and mask corner rounding effects for the 32-nm node

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The perpetual shrinking in critical dimensions in semiconductor devices is driving the need for increased resolution in optical lithography. Increasing NA to gain resolution also increases Optical Proximity Correction (OPC) model complexity. Some optical effects which have been completely neglected in OPC modeling become important. Over the past few years, off-axis illumination has been widely used to improve the imaging process. OPC models which utilize such illumination still use the thin film mask approximation (Kirchhoff approach), during optical model generation, which utilizes a normal incidence. However, simulating a three dimensional mask near-field using an off-axis illumination requires OPC models to introduce oblique incidence. In addition, the use of higher NA systems introduces high obliquity field components that can no longer be assimilated as normal incident waves. The introduction of oblique incidence requires other effects, such as corner rounding of mask features, to be considered, that are seldom taken into account in OPC modeling.

In this paper, the effects of oblique incidence and corner rounding of mask features on resist contours of 2D structures (ie line-ends and corners) are studied. Rigorous electromagnetic simulations are performed to investigate the scattering properties of various lithographic 32nm node mask structures. Simulations are conducted using a three dimensional phase shift mask topology and an off-axis illumination at high NA. Aerial images are calculated and compared with those obtained from a classical normal incidence illumination. The benefits of using an oblique incidence to improve hot-spot prediction will be discussed.

6730-185, Poster Session

Model-based mask verification

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One of the most critical points for accurate OPC is to have accurate models that properly simulate the full process from the mask fractured data to the etched remaining structures on the wafer. In advanced technology nodes, the CD error budget becomes so tight that it is becoming critical to model the process as close as possible. Current technology models used for OPC generation and verification are mostly composed of an optical model, a resist model and sometimes an etch model. The mask contribution is nominally accounted for in the optical and resist models. Mask processing has become ever more complex throughout the years so properly modelling this portion of the process has potential to improve the overall process modelling accuracy. Also measuring and tracking individual mask parameters such as CD bias can potentially improve wafer yields by detecting hotspots caused by individual mask characteristics. In this paper we will show results comparing a new approach that incorporates mask process modelling to the current modelling approach. We will also show results of testing a new dynamic mask bias application used during OPC verification.

6730-212, Poster Session

Inverse lithography technology (ILT): keep the balance between SRAF and MRC at 45 and 32 nm

L. Pang, Y. Liu, D. S. Abrams, Luminescent Technologies, Inc.

Increasingly, for semiconductor manufacturers moving to advanced nodes - 90nm, 65, 45, and below - the greatest challenge is lithography. This is because lithography is fundamentally constrained by basic principles of optical physics. At 65 nm and below, a line is less than a third of the effective wavelength of 193nm; optical diffraction and interference are becoming fundamental obstacles, not just second order effects.

It has long been known that the best lithography that is theoretically possible can be achieved by considering the design of photomasks as an inverse problem; and then solving the inverse problem to find the optimal photomask for a given process using a rigorous mathematical approach. These Inverse Lithography Technologies (ILT) have been explored for many years. Although these early approaches to ILT often resulted in superb lithography, they were generally impractical in a production environment. Run-times were many orders of magnitude too slow, and the resulting masks were often too complex to manufacture.

In this paper, we discuss the first ILT approach that can rapidly solve for the optimal manufacturable photomask design and is suitable for use in a production environment. We will discuss the latest development of ILT, in particular, in the areas of Sub-Resolution Assist Features (SRAFs) and Mask Rule Compliance (MRC), such as model-based SRAF generation during inversion calculation, SRAF optimization simultaneously with main features, Manhattan constraint mask and MRC for both main features and SRAF. Results collected internally and from customers demonstrated that, by optimizing each element of the process and keeping a good balance between SRAF and MRC, ILT can improve the lithography in term of resolution and process window, while maintaining the mask cost to a managed level.

6730-187, Poster Session

A generic technique for reducing OPC iteration: fast forward OPC

L. Hong, J. L. Sturtevant, Mentor Graphics Corp.

The drive toward advanced technology node has drastically increased the computational complexity of optical proximity correction (OPC). Applying full-chip OPC to all critical layers has become one of the most computational demanding steps in the tape-out process. Tuning for fast and accurate OPC recipes has also become one of the most critical and time consuming steps in the OPC recipe development process. OPC is by design an iterative cycle, where a iteration is a single simulation and polygon fragmentation shift sequence. Typically an accurate OPC recipe requires eight or more iterations to converge to a final best solution. The number of iterations in a recipe directly impacts the full-chip OPC runtime. Engineers often find themselves spending hours tuning OPC recipe to reduce just one iteration. The author will present a generic technique called Fast Forward OPC (FFOPC). FFOPC will help to reduce any golden OPC recipe that meets certain requirements to a fixed 4.5 iterations with minimum accuracy lost. Most importantly this technique can be easily implemented as a plug-in with any programmable OPC tools such as OPCpro and Calibre nmOPC.

6730-188, Poster Session

More robust model built using SEM calibration

C. Wang, Q. Liu, Semiconductor Manufacturing International Corp. (China); L. Zhang, Mentor Graphics Corp. (China)

More robust Optical Proximity Correction (OPC) model is highly required with integrated circuits' CD (Critical Dimension) being smaller. Generally a lot of wafer data of line-end features need to be collected for modeling. Scanning Electron Microscope (SEM) images are sources that include vast 2D information. Adding SEM images calibration into current model flow will be preferred. This paper presents a method using Mentor Graphics' Calibre SEMcal to integrated SEM calibration into model flow. Firstly simulated contour is generated and aligned with SEM image automatically. Secondly contour is edited by fixing the gap etc. CD measurement spots are applied also to get a more accurate contour. Lastly the final contour is extracted and inputted to the model flow. EPE will be calculated from SEM image contour. Thus a more stable and robust OPC model is generated. SEM calibration can accommodate structures such as asymmetrical CDs, line end pullbacks and corner rounding etc and save a lot of time on measuring line end wafer CD.

6730-189, Poster Session

Safe interpolation distance for VT5 resist model

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Resolution Enhancement Techniques rely on the creation of accurate simulation environments that capture the behavior of the lithographical system used for silicon printing. Models are the backbone that supports this environment and give confidence to recipe developers while tackling different challenges. Optical models have been developed over the years based on physical analysis of the light behavior in the exposure system, this made it possible to obtain good parameterized models, however the case is different for resist models that mostly depend on curve fitting of calibration data.

VT5 resist models calculate the resist response due to aerial image projected into it. The model needs to be calibrated with a versatile amount of data that resembles different structures encountered in design layouts. VT5 can be viewed as a multi-dimensional curve fitting polynomial that have the aerial properties of the projected image, and the density of layout features as its independent variation space. There has been systematic approaches to compare the multi-dimensional space for design features and those for calibration features, features from design that are not closely surrounded by features from calibration in the independent variation space might be poorly predicted.

In this paper we present an approach to qualify calibration test patterns, a metric of how close a design pattern should be to a calibration pattern is defined as the Safe Interpolation Distance is presented. Analysis of design layouts are made, and the metric is used to determine the confidence in the simulation results.

6730-190, Poster Session

The effect of the OPC setup parameters optimization on the performance of the OPC model

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Model Based Optical Proximity Correction (MB-OPC) is essential for the production of advanced Integrated Circuits (ICs). As the speed and functionality requirements of ICs production always require reducing the Critical Dimension (CD), the demand is continuously increasing for more accurate and sophisticated OPC models.

The OPC model is implemented on any design data through a set of rules which we call the "setup parameters". The OPC setup parameter optimization is an essential step that is performed in order to maximize the benefit of the OPC model by customizing how the model should treat specific designs. The setup parameters very much affect the OPC model in a way that makes the OPC model succeed or fail for producing the target shapes.

In this paper, we investigate the ability of the setup parameters optimization to compensate for the weakness of OPC model, or from the other end, how not optimizing the setup parameters can cause a very good OPC model to function poorly. Our approach here is to use three OPC models: a reference OPC model, a very good OPC model, and a weak OPC model. The setup parameters will be optimized to the weak OPC model trying to see how that will improve the model. On the other hand, bad setup parameters will be used with the good OPC model to see how this will weaken its performance; all will be compared with respect to the reference model.

The result from this work is very important for the OPC modelers and

setup parameters optimizers in order to improve the quality and performance of the produced OPC.

6730-191, Poster Session

Optical qualification of OPC simulator to ensure accurate and physics-centric OPC model

Q. Zhang, Synopsys, Inc.; J. K. Tyminski, Nikon Precision Inc.; K. D. Lucas, Synopsys, Inc.

The OPC modeling accuracy becomes increasingly stringent as the semiconductor industry enters sub-0.1um regime. Targeting at capturing the pattern printing characteristics through the lithography process, an OPC model is usually in the form of the first principle optical imaging component, which is refined by some phenomenological components such as resist and etch. The phenomenological components can be adjusted appropriately in order to fit the OPC model to the silicon measurement data. The optical imaging component is the backbone for the OPC model, and it is the key to build a stable and physics-centric OPC model.

Scanner second order characteristics such as illuminator pupil-fill, lens aberration, apodization, flare and etc, previously ignored without accuracy sacrifice at large technology nodes, are playing non-negligible roles at 45nm node and beyond. In order to ensure OPC modeling tool can accurately model these second order scanner characteristics, the core engine (i.e. the optical imaging simulator) of OPC simulator must be able to model these characteristics with sufficient accuracy.

In this paper, we studied the optical proximity effect of the aforementioned scanner second order characteristics on several 1D (simple line space, doublet line and doublet space) and 2D (dense line end pullback, isolated line end pullback and T-bar line end pullback) OPC test patterns. The predicted OPE from our OPC simulator matches well with the one from industry standard lithography simulator, and this laid the foundation of accurate and physics-centric OPC model with these second order scanner characteristics incorporated.

6730-192, Poster Session

Modeling polarized illumination for OPC/RET

H. Song, Q. Zhang, J. P. Shiely, Synopsys, Inc.

Recent research has shown that properly polarized light source enhances image contrast in photolithography for manufacturing integrated circuit (IC) devices, thus improves the effectiveness of optical proximity correction (OPC) and other resolution enhancement techniques (RET). However, current OPC/RET modeling software can only model the light source polarization of simple types, such as TE, TM, X, Y, or sector polarization with relatively simple configuration. Realistic polarized source used in scanner is more complex than the aforementioned simple ones. As a result, simulation accuracy and quality of the OPC result will be compromised by the simplification of the light source polarization modeling in the traditional approach. With the ever shrinking CD error budget in the manufacturing of IC's at advanced technology nodes, more accurate and comprehensive light source modeling for lithography simulations and OPC/RET is needed.

In this paper, we present a modeling framework that takes arbitrarily polarized light source. Based on Stokes vector descriptions of the light source, it unifies optical simulations with unpolarized, partially polarized, and completely polarized illuminations. We built this framework into Synopsys' OPC modeling tool ProGen. Combined with ProGen's existing capability to handle vectorial aberration by the projection lens, large angles due to hyper NA, and thin film effects, this framework represents a general vectorial model for optical imaging with the state-of-the-art scanners. Numerical experiments were performed to study impact of illumination polarization on the accuracy of lithography simulation and the quality of OPC results.

6730-193, Poster Session

Fundamental study on the error factor for the sub-90-nm OPC modeling

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As design rule is getting tight to the sub-90nm, the requirement for accurate OPC (Optical Proximity Correction) model is increasing. In the low-k1 imaging lithography process with KrF, however, it is difficult to make the accurate OPC model not only because of factors caused by unstable process such as large CD (Critical Dimension) variation, large MEEF (Mask Error Enhancement Factor) and very poor process margin but also because of potential error factors induced during OPC model fitting. In order to minimize those issues it is important to reduce the errors during OPC modeling at least. The OPC modeling is generally performed by continuous sequence of optical model fitting and resist model fitting. In this study, we approach to find out main error factor in two ways for OPC model fitting. First, through comparing illumination shapes between ideal and real source, we observe the influence of the illumination system on the OPC model error by analyzing model fitness results and SEM (Scanning-Electron-Microscope) image verification. In case of resist modeling, in general, there are two different mechanisms to fit resist model which are scalar modeling and vector modeling. For the scalar modeling, a concept of black box model which doesn't reflect any information like physical properties of resist, developing behavior, and acid diffusion length during resist coating is adopted. Besides, the vector model employs sub-stack information including n, k value of resist and BARC (Bottom-Anti-Reflect-Coating), thickness of resist and BARC, etc. By comparing both vector and scalar model, we have investigated whether the resist information influences on the OPC model or not.

6730-194, Poster Session

OPC development in action for advanced technology nodes

P. J. M. VanAdrichem, A. C. Wang, Synopsys, Inc.

Over the years many techniques and novel ideas for advanced OPC treatments has been reported. Only a handful of these techniques is actually in use today, and made the step from theory to practice. OPC flow developments for advanced technologies are quite demanding. Areas which are experienced as difficult include, modeling, specifications and spec definition. Combining different types of OPC, such as rules and model based, or staged corrections, brings its own set of problems, which need to be addressed. In this paper practical OPC techniques are described and critical elements in the whole OPC flow are pointed out.

Another problem area that becomes more and more problematic is measurements used for model calibration. More and more special tricks need to be used to filter measured data. It is obvious that poor measurement data will not deliver quality models. But identifying poor data points is not straightforward. In this paper some of these techniques are demonstrated.

6730-195, Poster Session

A novel methodology for efficient and accurate model calibration across the entire process window

I. Y. Su, Synopsys, Inc. (Taiwan)

For 65nm node and below, process window is largely reduced and the error budget for CD is extremely tight. Hence an accurate OPC model for best condition is no longer sufficient. Now OPC models must be able to predict process variations accurately and reflect the real wafer behaviors throughout process window.

In this paper, methodologies and examples of developing stable and predicative models across the entire process window will be discussed. Enhanced modeling accuracy and predictability will be demonstrated through litho verifications which demonstrated that more hot spots are captured by enhanced model accuracy.

6730-196, Poster Session

Industry survey of wafer fab reticle control strategies in the 90-nm/45-nm design-rule age

R. J. Dover, KLA-Tencor Corp.

Reticle quality control in wafer fabs is different from quality control in mask shops. As such an industry-wide survey was undertaken to benchmark different strategies and approaches taken. This paper summaries the results while retaining the different wafer fabs' anonymity and confidentiality The focus was on wafer fabs with design rules below 90nm, and thus users of 193nm wavelength lithography. The approach taken for the survey was specifically designed to be impartial and independent of any tools, solutions or applications available from KLA-Tencor.

6730-197, Poster Session

Shuttle fabrication for designs with lifted I/Os

R. Lin, M. Wu, S. Tsai, Yuan Ze Univ. (Taiwan)

As foundries sprint toward 45nm node, shuttle run (multi-project wafer) becomes an important vehicle not only for design prototyping but also for low-volume production. With multi-layered process technology, the designs in a shuttle run may use different number of metal layers. The wafers fabricated for the chips using the least number of metal layers will leave wafer lots first, those for the chips using the second least number of metal layers leave next,..., etc. This not only complicates the wafer fabrication process, but also wastes more wafers. In this paper, we propose a method to address this problem. Our idea is that a design can keep using as fewer metal layers as possible, but its I/O pads should be lifted to the highest metal layer possibly used by any design in a shuttle run. We call this task LIO. LIO can be performed by designers, design service companies, or foundries. With LIO, all the wafers for a shuttle run will leave wafer lots at the same time. Since any of these wafers can be used to produce dice for any design, wafer wastes can be reduced.

LIO will not increase mask fabrication cost, but it can potentially increase wafer exposure cost because more wafers get fabricated with more metal layers. To evaluate its merits, we consider the following shuttle fabrication programs:

(1). Without LIO, but employing multiple mask sets, each of which is made for the designs using the same number of metal layers.

(2). Without LIO, but employing a single mask set for all the designs.

(3). Without LIO, but employing two mask sets.

(4). With LIO, but employing a single mask set for all the designs.

(5). With LIO, but employing two mask sets.

For each fabrication program, we perform a design space exploration using the state-of-the-art reticle floorplanning and simulated wafer dicing methods. For fabrication programs (3) and (5), a multi-reticle floorplanning method is used to determine which designs should be put into the same mask set. The intention of using more than one mask set is to reduce wafer waste. Based on the mask cost and wafer fabrication cost data for a 90nm node, our experimental results for some industry test cases show that fabrication program (4) for low-volume production is marginally better than fabrication program (2). However, the margin increases as production volume increases, achieving 11% increase for a volume up to a few ten thousand dice per design. Wafer cost reduction coming from employing more than one mask set (i.e., fabrication programs 1, 3, and 5) does not outweigh mask cost increase. The time takes to evaluate a fabrication program for a test case is less than two hours. Our methodology can be extended to study the problem of selectively doing LIO only for some particular designs. Besides the fabrication cost issue, employing LIO should also take into account whether lifted I/O pads would upset the timing behavior of a design and delay completing wafer fabrication for the underlying shuttle run.

6730-198, Poster Session

Development status of EUVL-mask blank

K. Hayashi, Asahi Glass Co., Ltd. (Japan)

Extreme ultraviolet (EUV) lithography is one of the candidate lithographic technologies to fabricate the integrated circuit devices with 32-nm feature size and smaller. Several technical issues have to be solved in order to realize EUV lithography. For instance, there are various kinds of requirements for EUV mask blank such as thermal properties of substrate material, substrate flatness, substrate roughness, reflective optical properties, and defect as small as 30nm. Most of these requirement are much more stringent than those for the optical lithography mask blanks and some are specific requirements to EUV lithography, so that the realization of the EUV mask blank with all of these requirements is one of the most critical issues in the EUV lithography.

We have been providing the photomask substrates since 1982 and have recently started to develop the EUV mask blank. Out development of EUV mask blank includes the developments of all essential materials and processes: the low thermal expansion material itself, its synthetic and polishing processes with low defect and low flatness, the coating materials and processes of reflective and absorber layers with low defect and precise thickness control. In the presentation, we will show the latest improvements of these properties of EUV mask substrate and blank.

6730-199, Poster Session

Performance of actinic EUVL mask imaging using a zone-plate microscope

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Owing to the wavelength-specific resonant reflective properties of extreme ultraviolet (EUV) reticles, inspection with EUV light is essential for early learning. Actinic imaging provides quantitative aerial image feedback in ways that photoresist printing and non-EUV inspection methods cannot. Of particular interest is the printing sensitivity to phase and amplitude pattern defects, and defect-repair sites. Correlation with scanning electron microscope (SEM) and EUV lithographic printing provides a detailed understanding of the factors that influence the final image quality.

The SEMATECH Berkeley Actinic Inspection Tool (AIT) is a unique, dual-mode, scanning and imaging EUV microscope designed for pre-commercial EUV mask research. In scanning mode the tool measures the reflectivity and scattering properties of EUV masks with spatial resolution from 1-5 μm, and 0.1-0.2% sensitivity. In imaging mode, the tool operates as a high-resolution EUV zoneplate microscope, measuring the reflected intensity directly, at-wavelength, with spatial resolution designed to emulate a 0.25 NA stepper. The tool operates on a bending magnet beamline which provides stable, in-band, EUV illumination. The light from the zoneplate lens is projected directly onto an EUV CCD camera with a magnification of approximately 800x.

We report high quality actinic EUV mask imaging with resolution below 150-nm half-pitch, (37.5-nm wafer equivalent size). Dramatic improvements in image quality have been made by the replacement of several critical optical elements. Progress have been achieved in the areas of image distortion, illumination non-uniformity, vibration-stability, imaging aberrations, and illumination alignment. In particular, a higher-quality zoneplate lens was installed incorporating auxiliary pupil alignment features for accurate beam positioning, and a 45-degree turning mirror between the zoneplate and the CCD was replaced with a research-grade flat mirror multilayer coated for relatively broad angular bandpass. A capacitive height sensor to monitor the distance between the mask and the zoneplate lens, coupled with a new linear height-actuator, enables the acquisition of stable through-focus data series with 0.1 μm resolution. Operating in the focus of the illuminating lens reduces illumination non-uniformities; while scanning the final beamline mirror's tilt angle paints out the pupil and provides a smoothly illuminated area up to approximately 25-μm wide. Typical exposure times range from 0.3 seconds during alignment, to approximately 30 seconds for high-resolution images.

This paper will focus on the results of imaging performance evaluation measurements and benchmarking with other measurement techniques.

6730-200, Poster Session

The effect of size and shape of sub-50-nm defects on their detectability

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Current semiconductor manufacturing research is focused on building devices with the critical size of 32 nm and below. To achieve this goal engineers should be able to detect defects of size of 30 nm and below. Therefore, the defect inspection tools are using shorter wavelength light to increase the defect detection resolution. The Lasertec M7360 is a defect inspection tool for EUV mask blanks designed to detect PSL spheres with diameter of 30 nm on the surface of quartz or MoSi multilayers. However, the naturally occurring (i.e. native) defects are different in many aspects from PSL spheres. Native defects are irregularly shaped and usually composed of multiple elements. One metric of the size of an irregularly shaped defect is the Sphere Equivalent Volume Diameter (SEVD). SEVD is the diameter of a virtual sphere with the same volume as defect. In order for this to be a useful metric the detectability of a defect should be proportional to the SEVD size of the defect. Most of the dark or bright field inspection tools use directly (or indirectly) the scattered light for defect detection. According Rayleigh scattering the intensity of the scattered light in far field is a function of the defect volume and also the dielectric constant of the material.

Our recent experimental data with the Lasertec M7360 for optical detection and AFM for size analysis shows that defect shape and its composition play an important role in its detection ability.

Lasertec M7360 is a unique bright field confocal inspection tool which is able to detect native defects as small as 20 nm SEVD on quartz surface by using light with wavelength of _ nm

This paper will discuss defect detection capability of Lasertec M7360 versus composition and shape of defects. In particular we will present the calibration curves of deposited particles, such as Au, Ag, SiO2 Si3N4, Fe2O3, CuO with different sizes Their actual sizes, as measured by AFM, will be compared with their optical size as determined by the contrast in the M7360.. Our data will be compared with theoretical simulation studies which will consider the defect shape and composition.

6730-201, Poster Session

Force non-uniformity in electrostatic pin chucks for EUVL mask clamping

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Electrostatic chucks (ESCs) are used to support and flatten masks during EUV lithography to remove long wavelength flatness variations and, as a result, reduce image placement (IP) errors. Previous research has focused on the design and characterization of ESCs to make them compatible with semiconductor processing requirements and to generate sufficient force for EUV chucking applications. Traditionally, the design of ESCs has focused on achieving a specified average electrostatic pressure across the chuck, but knowledge of the distribution of electrostatic pressure, which can be non-uniform, is essential to accurately simulate EUV mask chucking. In this work, we report measurement methods to characterize the non-uniformity of electrostatic pressure on EUV chucks and finite element simulations that examine the sources of non-uniformity. Two methods to characterize electrostatic force non-uniformity that are based on measuring wafer distortion around mesas lithographically defined on a test wafer or measuring the distortion of a thin wafer between the pins during chucking have been developed. In both cases, finite element models have been developed that allow the local pressure to be determined from the measurements of wafer distortion. In addition to the experimental methods, potential sources of electrostatic pressure non-uniformity have also been examined in this work. Specifically, the effect of various pin- chuck design parameters on electrostatic pressure uniformity have been examined through an electrostatic finite element analysis. The models capture the effect of fringe fields around the pins and the electrodes and allow the role of design parameters, including the electrode gap, dielectric thickness, pin height, and pin pitch, on the fringe width to be identified. Experimental and simulation results pertaining to ESC non-uniformity for EUV mask chucking will be discussed in detail.

6730-202, Poster Session

A study of precision performance and scan damage of EUV masks with the LWM9000 SEM

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The International Technology Roadmap for Semiconductors (ITRS) for 2006 requires 2.7nm, 3 sigma CD uniformity for EUV masks in 2010. Given the resolution requirements and feature sizes for EUV masks it is important to evaluate CD SEM tools and their performance on EUV masks for precision performance and possible EUV film scan damage (reflectance changes). An evaluation was performed on an EUV mask using the LWM9000 SEM produced by Vistec/Advantest.

The performance of the LWM9000 SEM was optimized on the EUV mask to obtain similar performance results as those obtained on Chrome and MoSi photomasks. Because the LWM9000 SEM uses Ozone for in-situ cleaning of the work chamber, the interaction between the electron beam and Ozone presence was investigated. The EUV mask was evaluated at the inspection wavelength before and after e-beam scanning and measurements to determine any changes in reflectance or mask characteristics.

6730-203, Poster Session

EUV mask substrate flatness improvement by laser irradiation

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EUV mask substrate flatness of less than 50nm PV (peak-to-valley) is required because of using non-telecentricity optics by the oblique illumination. Since achieving the flatness requirement is quite difficult, flatness-improving techniques are quite important.

However conventional methods such as local polishing and/or deposition have some problems such as surface roughness and contamination. Therefore quick and more accurate technique of improving the flatness is necessary.

We have demonstrated a new technique for the improvement of the substrate flatness by using a pulsed laser. Laser pulses from an ArF excimer laser were focused in a quartz mask substrate to make spots. Experiments showed that the substrate surface can be locally swelled out where spots are formed a little beneath the surface without making any damages on the surface. While the surface can be locally sunken where spots are formed at the depth closer to the opposite surface.

This surface controlling technique can be applied to the final adjustment of the substrate flatness control since no additional process is necessary afterward. Also because the surface changes can be controlled by the depth of the laser spots and the distribution of the shots.

6730-204, Poster Session

Evaluation of EUVL-mask pattern defect inspection using 199-nm inspection optics

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Extreme ultraviolet lithography (EUVL) is the most progressive next generation lithographic (NGL) technology after 193nm immersion lithography. However, there are some technological issues concerning source power, particle-free mask handling, resist material development, and so on. From the view point of EUVL mask fabrication, mask pattern inspection seems to be one of the critical issues. Since ULSI pattern feature size by EUVL is smaller than that for optical lithography, a higher resolution compared to that used in optical mask inspection is required. In addition, EUVL mask can't be inspected through transmitted light im-

ages.

In order to improve the technology of the mask pattern inspection, shorter wavelength DUV inspection light is one of the most useful key technologies. The effectiveness to introduce the shorter wavelength DUV light for inspection system is enhancement of the resolution and the image contrast for device patterns and defects. And also inspection sensitivities for smaller defects will be improved.

In this presentation, we will report some experiment data for the EUVL mask inspection sensitivities with using 199nm inspection optics. The test mask was based on commercially available EUVL blanks. Evaluated defects were opaque extension defects, clear extension defects and so on in the 1:1 dense line (hp180, 260, 360nm on mask).

This work was supported by New Energy and Industrial Technology Development Organization (NEDO).

6730-205, Poster Session

Study of impacts of mask structure on hole pattern in EUVL

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Extreme Ultra Violet Lithography (EUVL) is a promising candidate for the next-generation lithography because of its excellent resolution for hp 32 nm technology node. Especially, its introduction into hole patterning process is expected to be more attractive as compared to the very costly double patterning process of optical lithography. In order to manage CD error factors and to construct production worthy EUVL hole process technology, it is very important to carry on process window analysis relating to mask structure. For cost reduction, stringent specification for each error source should be avoided. Therefore, we focus on understanding the relational effects ranging from mask to exposure tool and resist.

Distinctive characteristics resulting from the simulation studies on hole printability are available for specification of EUVL mask structure. We have evaluated impacts of mask structures on resist profiles using EUVL simulation. We have investigated impacts of absorber sidewall angle on process window. The process windows consist of exposure dose and defocus tolerance for 10% CD variation of 35nm hole resist pattern on wafer. We evaluated impacts of sidewall angle and incident total dose by varying the top dimension of mask structure, whereas keeping the bottom (reflecting surface) dimension fixed at 40 nm (on wafer scale). For example, each of both process windows of a mask structure where the top dimension is 42 nm and sidewall angle is 88.6 degree, and a mask structure where the top dimension is 47 nm and sidewall angle is equal to 85.0 degree has more than 10% exposure latitude and 120nm depth of focus. However, as required dose reduces according to top size increase, a common process window giving the same CD at bottom of resist profile deteriorates.

We think that flexible specifications based on latitudinous understanding of relational effects using simulation technologies can offer options that can make specifications more relaxed.

6730-206, Poster Session

Repair specification study for half-pitch 32-nm patterns on EUVL

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One of the key issues with extreme ultra violet lithography (EUVL) is the influence of defect on resist because of EUVL's high resolution printability at sub 32-nm half pitch (hp) technology node. In order to address this issue it is necessary to appreciate the critical size of a defect in terms of its repair by deposition of some other repairing material by focus ion beam or e-beam tool; here factors like the size of the repairing material, its height, and its optical constant have to be taken into consideration.

In this study, we employed a commercial simulator SOLID-EUV for rigorous 3D mask calculation and considered specification of clear defect and repair for hp 32-nm using off-axis EUVL illumination. The defect of Ta absorber was set on line-edge of a 32-nm-width and 80-nm-hight patterns lying perpendicular to the incident angle of light.

By evaluating the threshold of the calculated aerial images, the critical dimension (CD), that could be printed, was found to correspond with the size of the square of the defect area. Since the defect was repaired with Ta, which has same optical property as of the absorber material, the printed CD error was caused mainly by repairing the CD error and was not caused by the height error which was within 25% of Ta material. The optimal optical constant of the material was estimated by varying the optical constants for reflection coefficient from 0.92 to 0.99, and for the extinction coefficient form 0.01 to -0.05. We found that carbon as repaired material could be available for maintaining CD error within 0.5 nm around 64 nm2 defect size because the maximum reflection value should be below 0.97. This work is supported by New Energy and Industrial Technology Development Organization (NEDO).

6730-207, Poster Session

EUV process development using DUV inspection system

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As the design rule continues to shrink towards 45nm and beyond the lithographers are searching for new & advanced methods of mask lithography such as immersion, double patterning and extreme ultraviolet lithography (EUVL). EUV lithography is one of the leading candidates for the next generation lithography technologies after 193 nm immersion and many mask makers and equipment makers have focused on stabilizing the processes. With EUV lithography just around the corner, it is crucial for advanced mask makers to develop and stabilize EUV processes. As a result, an inspection tool is required to monitor and provide quick feedback to each process step.

The intent of this paper is to demonstrate EUV inspection capabilities in both die-to-die and die-to-database using reflected light inspection.

6730-208, Poster Session

Developemt of EUV mask fabrication process using Ru capping blank

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Extreme Ultra Violet Lithography (EUVL) is considered to be a major candidate for the Next Generation Lithography.

To achieve reflective optics, EUV mask consists of absorber layer, reflective multilayer (ML) with protection capping layer.

Buffer layer can be used for silicon capped EUV blanks to enhance the etch selectivity against absorber etching.

It has been reported that Ruthenium (Ru) material has better property on oxidation resistance compared to standard silicon (Si) capping layer.

Ru capping layers have advantage for its high etch selectivity, which enables buffer layer less EUV mask structure. However Ru layers should be limited thin due to relatively high light absorption.

In this paper, we evaluated current process performance of Ta-based absorber etching on Ru capped ML blanks, which includes Ru capping layer etch effect as well as CD uniformity, linearity, Line Edge Roughness (LER) and selectivity between absorber and Ru capping layer.

6730-209, Poster Session

Metrology for templates of UV nano-imprint lithography

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Nano-imprint lithography (NIL) is one of the most promising candidates for high throughput and low cost patterning of nanostructures. The resolution of NIL isn't limited by light diffraction or beam scattering in other lithography technologies and is defined by the resolution depended on

the template. In addition, feature sizes of the templates for UV-NIL have the same as the wafer pattern, though current photomasks have four times the sizes of those on the wafer. This potentially makes the template manufacturing more difficult than the photomask manufacturing. Therefore metrology is also one of the challenge items to fabricate templates for UV-NIL. There are many issues in metrology for the templates, for instance, necessity of the further resolution for measurement tools, charging issues without conductive layers, and surface energy measurement on templates.

In this paper, we will focus on metrology of the templates for UV-NIL. And also some measurement techniques are described about detail results using scanning probe microscope, CD-SEM, scattermetry and so on.

6730-210, Poster Session

UV-NIL templates for the 22-nm node and beyond

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Nano-imprint lithography (NIL) is expected as one of the candidates for 32nm node and below. NIL needs 1X patterns on template(mask) and a transit from 4X to 1X means a big and hard technology jump for the mask industry. Therefore, we have been focusing on the resolution limit on the template, during recent years. We reported in PMJ2007 that we could achieve 22nm dense lines, 22nm holes and 28nm pillars by using a 100keV spot beam exposure tool and Non-CAR

In this paper, as a continuation of our previous works1-3, we are showing further improvement to achieve below 22nm resolution by optimizing exposure and process conditions and also using new non-CAR. We are also showing the high performance pattern profile by optimizing the dry etching.

6730-211, Poster Session

A study of template cleaning for nano-imprint lithography

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Nano-imprinting lithography (NIL) is being evaluated as a possible avenue/method for obtaining the lithography requirements needed for the 32nm half-pitch node and below. NIL is included in the International Technology Roadmap for Semiconductors (ITRS) as a potential choice for advanced lithography. In evaluating this technology, the template or mold is a critical component in achieving the requirements needed for 32nm half-pitch nodes and below. One of the issues with NIL is the high probability of defects while imprinting. Since the template is in contact with a fluid being cured by ultraviolet (UV) radiation, the ability to clean the template to the degree needed to met the ITRS requirements without damaging or changing critical dimensions is imperative. In this paper, we will discuss the results obtained from several different NIL template cleaning methods using SEMATECH's Mask Blank Development Center facilities. A comparison will be made showing the effectiveness of different operating conditions as well as several different chemistries. Several dimensions of NIL template topography structures will be compared using an atomic force microscope (AFM) throughout multiple cleaning steps.

6730-37, Session 9

Investigation of mask defectivity in full-field EUV lithography

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EUV lithography is the leading candidate for 32nm half-pitch device manufacturing and beyond. The world's first 0.25 NA full field EUV scanner, i.e., ASML's Alpha Demo Tool (ADT), is available for preparation work towards pre-production based on EUV lithography. Initial imaging performance results clearly prove sub-40nm half pitch imaging capability [1,2].

The present paper discusses the results obtained in two reticle defectivity related topics within IMEC's EUV lithography program: defect printability and evaluation of particle adders during mask handling.

The objectives of the defect printability activity is to investigate which types and sizes of defects are printable and which defects can be effectively repaired. Four types of defects will be discussed: absorber defects, particles, local reflectivity loss and buried defects (in or underneath the ML). Defects in this multilayer are of the greatest imaging concern for EUV masks. Improvements in mask blank defectivity has resulted from major initiatives such those as at the Sematech MBDC [3,4]. There are still significant concerns with defects, especially with buried defects in or underneath the multilayer, which print more easily as phase defects because of the small wavelength and because of the late availability of an appropriate defect inspection tool for screening these defects in masks.

The first part of the paper will discuss simulation results obtained with Solid-EUV from Sigma-C (Synopsys), for each of the 4 defect types mentioned. As much as possible, exposure tool related settings are chosen to mimic the ADT. The mask stack is as has been published for the Schott blank [5]. For absorber type defects, we have started from the historical rule of thumb, i.e., that at mask scale, the critical defect size equals the critical dimension at wafer scale. We have found the results require further diversification: An opaque defect located in the centre of a space in a 40nm lines and space pattern already causes more than a 10% change in the space width from 70% of the space width onwards (\>28nm at mask scale, \>7 nm at wafer scale). In this worst case, the historical rule of thumb underestimates the printability. Opaque defects further away than 50nm (at wafer scale) from an isolated absorber line, do not cause any influence on that line width until the defect itself starts to print as a feature. Absorber type clear defects start affecting line width in 40nm lines and spaces from about twice the size of an opaque defect. Particles simulated as carbon cubes have a similar effect as absorber type opaque defects that are approximately twice their size. Further results will include other particle materials and buried defects. Experimental plans for comparison of simulations to exposures on the IMEC Alpha Demo Tool will be included.

The second part of the paper will review our activities to investigate mask handling in and around the ADT in the absence of an EUV pellicle. IMEC used the particle scanner reported in Ref. 6. Its performance has been benchmarked based on PSLs against the Lasertec M1350 tool, which has been the work horse of the work at the MBDC [3,4] and at mask shops. The paper will review this comparison and report on the investigation of mask handling in and around the ADT.

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6730-38, Session 9

Detectability and printability of EUVL-mask blank defects for the 32-nm HP node

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The readiness of a defect-free extreme ultraviolet lithography (EUVL) mask blank infrastructure is one of the main enablers for insertion of EUVL technology into production. It is essential to have sufficient defect detection capability and sufficient understanding of defect printability to develop a defect-free EUVL mask blank infrastructure. The SEMATECH Mask Blank Development Center (MBDC) has been developing EUVL mask blanks with low defect densities with the Lasertec M1350 and M7360, the 1st and 2nd generation of visible light EUVL mask blank inspection tools, respectively. Although the M7360 represents a signifi-

cant improvement in our defect detection capability, it is time to start developing a 3rd generation tool for EUVL mask blank inspection. The goal of this tool is to detect all printable defects; therefore, understanding defect printability criteria is critical to this tool development.

In this paper, we will investigate the defect detectability of a 2nd generation blank inspection tool and a patterned EUVL mask inspection tool. We will also compare the ability of the inspection tools to detect programmed defects whose printability has been determined from wafer printing experiments.

6730-39, Session 9

Measuring and characterizing the nonflatness of EUVL reticles and electrostatic chucks

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Stringent flatness requirements have been imposed for Extreme Ultraviolet Lithography (EUVL) mask substrates due to the nontelecentric illumination during scanning exposure. The industry is proposing to use an electrostatic chuck to support and flatten the mask in the exposure tool. The EUVL Mask and Chucking Standards, SEMI P37 and SEMI P40 [1,2], specify the flatness of the mask frontside and backside surfaces, as well as the chucking surface, to be within 30 to 100 nm peak-to-valley (p-v). However, measuring and characterizing the shape of a reticle or chuck surface and specifying a nonflatness value associated with a particular shape is not well-defined or well-understood. The current research is focused on identifying the most accurate procedures for measuring and subsequently describing the nonflatness of these surfaces.

It is generally accepted that the reticle and chuck would be measured interferometrically, but the two may need to be supported in completely different orientations. The mask substrate should be held vertically to eliminate gravitational distortions; in addition, any mechanical constraints must have negligible effects on the out-of-plane distortions (OPD) of the surface. In this paper, finite element (FE) models have been developed to analyze the effects of three types of fixtures that are currently being used by the industry when experimentally measuring the glass substrates. Results from the FE simulations illustrate the advantages and disadvantages of each, and recommendations are made for standard specifications on fixturing. For the electrostatic chuck designs currently proposed, it may be necessary to measure the dielectric surface with the chuck in a horizontal configuration. Again FE models are employed to identify the OPD induced by gravity versus the actual nonflatness of the dielectric layer.

After interferometric data is obtained, it must be analyzed to determine a representative p-v nonflatness value. According to SEMI P37 and SEMI P40, flatness definitions are based on the p-v values of the surface that is defined by the plane that “minimizes the maximum deviation of the surface,” known as the minimax plane. This nonflatness value is significantly different from results obtained by using the least-squares best-fit plane or interferometric analysis software. For illustration purposes, experimental data was collected on 12 EUVL substrates (i.e., 24 surfaces). The p-v nonflatness values obtained using the least-squares and the minimax methods were compared against the values calculated by the interferometric software. In many cases differences were greater that 50%. A complete analysis of this study, along with recommendations for changes in the SEMI Standards, will be presented in the paper. Final comments on fitting interferometric data to Legendre polynomials are provided as guidelines when attempting to characterize the overall surface shape. Two fitting techniques have been investigated (the continuous least squares method and the general least-squares method) and the numerical procedures for each will be described in detail.

In summary, comprehensive analyses have been completed on the techniques proposed for measuring and characterizing the nonflatness of EUVL mask substrates and electrostatic chucks. Experimental and numerical data are used to illustrate the difficulties that arise in implementing the SEMI EUVL Mask and Chucking Standards. Results will aid in identifying modifications and clarifications that are needed in the Standards to facilitate the timely development of EUV lithography.

[1] SEMI P37-1102, SEMI Standard Specification for Extreme Ultraviolet Lithography Mask Substrates.

[2] SEMI P40-1103, SEMI Standard Specification for Extreme Ultraviolet Lithography Mask Substrate Chucking.

6730-40, Session 9

Recent performance of EUV mask blanks with low-thermal expansion glass substrates

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An EUV mask blank with LR-TaBN absorber and CrN buffer layer formed on Mo/Si multilayer (ML) have been developed, where a glass substrate with low thermal expansion (LTE) was used to minimize mask distortion caused by thermal road during EUV exposure process. An LTE glass with low coefficient of thermal expansion (CTE) of +/- 10 ppb, meeting class B specification in SEMI standard, can be commercial available from some glass suppliers. Critical challenges of EUV blanks are to attain near zero defects at 30 nm on ML blanks, high flatness of less than 50 nm on both sides of glass substrates and high EUV reflectivity of more than 66% on ML films, simultaneously. We are in beta type development phase for full field mask used in alpha EUV exposure tools and mainly focusing on defect reduction, flatness improvement and reflectivity improvement toward the production targets.

In this paper, recent progress in EUV blanks development and recent performance of the EUV blanks will be presented. Defects and flatness qualities on the EUV blanks have been steady improved. Recently, EUV blanks with flatness of less than 100 nm, low defects of less than 0.2 def/cm2 at 80 nm sensitivity, and peak reflectivity of more than 65% at EUV light was successfully demonstrated by improving polishing and ML coating processes. Moreover, LR-TaBN absorber stacks with excellent uniformity of less than +/-1% in thickness and low defects were obtained by using production type sputtering tool.

6730-41, Session 9

Investigation of resist effects on EUV mask defect printability

Z. J. Zhang, T. Liang, Intel Corp.

Extreme Ultraviolet lithography (EUVL) is considered as a leading patterning technology for manufacturing future nodes of semiconductor devices. The ability to fabricate defect-free EUV masks has always been one of the primary challenges in enabling production-worthy EUVL. There are three general categories of defects on a finished EUV mask, namely blank defects embedded in the reflective multilayer blank, hard defects from absorber patterning, and soft defects from contamination during handling and use. We have been carrying out systematic studies of the printability as well as inspectability of all these defects in a progressive manner from careful defect characterization to aerial image model simulations then to actual resist wafer prints with the availability of continuously improved EUV exposure tools. While it is important to characterize the nature of the defects for defect reduction and mask-making process improvement, the ultimate measure for defect specification must come from the evaluation of impact on resist CDs. We have observed major printability differences between aerial image simulations and experimental resist print data. We contribute such discrepancies to resist effects.

In this paper, we report our recent investigations into the effect of resist process. Simulations are conducted using both aerial image threshold and resist model in an attempt to determine the critical defect size and the effect of resist process. There is a good agreement between the resist model simulation and the printing data obtained using EUV MET exposure tool and a programmed defect mask with edge defects of 70nm semi-iso lines. The aerial image threshold CD error introduced by edge defects is larger than that obtained by the resist model and the actual printing results. However, this favorable difference vanishes for edge defects on 30nm lines. Mask error enhancement factor (MEEF) models can be used to understand the discrepancy between the aerial image and resist model, and the feature-size dependent defect printability effect. CD error introduced by soft defects (oxide and organic defects) located on the line edge is also studied as a function of defect size and thickness, and the critical soft defect parameters are determined for 30nm isolated and dense lines. Image quality (NILS) and resist processing (ex-

posure latitude) are closely related to affect the defect printability. The intrinsic nonlinear behavior presents a challenge for defining defect specifications for the 32nm node and beyond.

6730-42, Session 9

Impact of mask absorber properties on printability in EUV lithography

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Extreme Ultraviolet lithography (EUVL) with 13.5nm exposure wavelength is most promising to attain ULSI devices with 32nm half-pitch (hp) and beyond. Mask plays a key role in any lithography and should be regarded as an integral part of a lithographic system.

The requirements for EUVL mask from ULSI chip vendors are high lithographic performances, such as high imaging contrast, low shadowing effect due to reflective mask and oblique illumination, low thermal expansion material substrate, high flatness control and high durability against EUV light exposure, etc. Meanwhile, the requirements from mask vendors are high performances in the mask making processes, such as high selectivity of absorber's etching to buffer layer, no damage of multilayer during etching, high CD control, low defect density, high durability against cleaning, and so on. In addition, high performances of defect inspection and repairing, such as high imaging contrast at inspection wavelength, high selectivity of absorber's etching to buffer layer, no damage of multilayer during repairing are also required by the mask vendors.

In this paper, we present the impact of mask absorber properties on printability in EUV lithography from the viewpoint of the lithographic requirements, which obtain the high imaging contrast at EUV exposure, and reduce the shadowing effect. By using typical absorber's refractive index, we simulate absorber reflectivity on multilayer blanks, wafer plane aerial image, printed CD and printed pattern shift depending on absorber thickness, and we predict optimum absorber thickness.

Several patterned masks of LR-TaBN absorber with various thicknesses were prepared. Measurements of reflectivity at EUV light for such masks were in good agreement to reflectivity simulation results. And each patterned masks was exposed with the newly developed small-field-exposure-tool (SFET). The SFET printed results depending on mask absorber thickness will be discussed comparing with lithography simulation results.

This work is supported by New Energy and Industrial Technology Development Organization (NEDO).

6730-44, Session 10

Compositional analysis of progressive defects on a photomask

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Progressive mask defects are a critical mask reliability issue in DUV lithography. It is well-known that the majority of the defects are ammonium sulfates.

We have found that metallic atoms are localized at ammonium-sulfate defects on the mask surface by ToF-SIMS analysis, can influence the growth of the defects.

Carbon compounds containing nitrogen atoms are also localized at the some defects. These carbon compounds are the result of the adsorption of organic volatiles outgassing from a reticle SMIF pod.

Metal residues and organic contamination on a photomask as well as airborne acidic and basic contamination must be controlled to avoid progressive defects on photomasks.

6730-45, Session 10

A practical solution for 193-nm reticle haze

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The authors have developed and successfully implemented a practical, yet effective solution for haze formation in the production fab. Based on a novel mechanism of haze formation described earlier, along with a thorough understanding of the reticle surface chemistry changes during the manufacturing process, the authors found an unexpectedly simple way to prevent haze formation. This is possible regardless of the origin of the reticle by controlling the purity of the immediate reticle environment.

The authors provide step-by-step detailed information on how to create and maintain the required level of reticle environment purity, and give practical recommendations on implementing this solution in fabs with different layouts and various types of production equipment.

6730-46, Session 10

Rapid and precise monitor of reticle haze

T. E. Zavecz, TEA Systems Corp.

Reticle Haze results from a chemical residue of a reaction that is initiated by Deep Ultra Violet (DUV) and higher frequency actinic radiation. Haze can form on the backside of the reticle, on the chrome side and on the pellicle itself.

The most commonly observed effect of haze is a gradual loss in transmission of the reticle that results in a need to increase exposure-dose. Since haze formation is non-uniform across the reticle, transmission loss results in an increase in the Across Chip Linewidth Variation (ACLV) and corresponding reduction in the manufacturing process window. Haze continues to grow as the reticle is exposed to additional low wavelength radiation.

The onset of reticle haze results in a degradation of Best Focus, Depth of Focus and the Exposure latitude of the production sequence. Normal process-space variation will therefore result in a direct loss of lithographic yields, an increase in rework rates and an ultimate loss in overall final-test yield.

The contour plot of dose uniformity, shown in figure 1, illustrates a reticle dose response after haze has formed on the reticle (left contour) and after reticle cleaning (right image). Here the contour plots the dose-energy that must be exposed on each portion of the reticle in order to achieve an on-target feature size.

The haze-free reticle image on the right shows an exposure from the same reticle that has a brighter center-scan than the field edges. The field edges therefore would require a higher dose, as shown, to achieve target feature size. The response of the haze-free reticle on the right is typical for a scanner and the loss of exposure on the left and right sides of the reticle are an artifact of the intensity profile of the scanner lens-slit.

Testing for haze does not require an inspection of the entire plate. A sampled inspection of a regular array of points across the exposure field will detect any form of reticle haze. A model-driven method for the detection of reticle-haze using basic feature metrology is developed in this study along with application results from a production reticle.

This methodology presents a highly accurate illustration of the reticle exposure-response since focus errors of the exposure-tool have been removed from the analysis. A small amount of haze formation on the reticle will change the required exposure-dose.

Dose uniformity, and therefore reticle haze, can be monitored in production on a periodic basis by simple focus-dose exposures. Analyses conducted during the lifetime of a reticle are then monitored using trend charts such as the one shown in figure 2. Trend charts provide a rapid and cost effective method of detection for reticle haze.

6730-47, Session 10

Characterization of chemical mobility behavior toward haze defect creation on mask substrate during laser exposure

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The frequency of haze occurrence on photomasks is greatly dependent upon mask layer and substrate material. Despite many studies on haze defect, no clear mechanism for haze formation has been reported yet.

Diffusion of sulfur and ammonium ions on mask substrate seems to be one of key factors to induce haze defect seed formation and crystal growth during laser exposure. Diffusion rates of sulfur or ammonium ions are different depending on each substrate, which is mainly due to the discrepancy in the adhesion force between each substrate and corresponding ions.

In this paper, we have investigated migration behavior of chemical ions within each substrate material (Qz, MoSiON, and Cr) during laser exposure. We also investigated whether surface roughness and bulk morphology of each substrate would affect chemical ion mobility towards haze defect creation on the mask surface. The result of this work can be used to disclose suitable reason why haze defects are created mostly on Qz substrate during exposure and suggest appropriate cleaning methods customized for different mask types and layers.

6730-165, Session 10

Capability of eco-friendly cleaning strategy corresponding to advanced technology

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In sub-60nm technology node, cleaning process becomes specialized to clear the defects without pattern damage as decreasing critical particle size to control. Recently, it is the problem that cleaning process is not confined within a viewpoint of clearness of defect any more. While cleaning process has to meet the primary requisite, removal of particle including organic residue and prevention of particle re-deposition, it should enable to suppress haze phenomena for a long life of photomask. However, to solve the problem of haze, the chemical materials caused haze seed should be hardly used and physical force becomes strengthen as the compensation for cleaning efficiency. Unfortunately it brings about another problem, pattern damage seriously.

In this paper, adequate cleaning conditions which are applicable in sub-60nm technology node are evaluated to meet the dilemma among three requirements, prevention of haze phenomenon, high cleaning efficiency, and prevention of pattern collapse. All cleaning steps in photomask process were set up using only 172nm UV irradiation as oxidation source for degradation of organic contaminants and deionized water (DI) with acoustic power for particle removal. The effect of UV and DI cleaning on haze phenomena and cleaning efficiency was derived from carrying out chemical and physical analysis simultaneously. Also, we could quantify the statistical probability of pattern collapse in each of technology node and layer shape as different condition of megasonic frequency and power. As a result, it was known that this cleaning process have various merits to make out dilemma mentioned above, if it satisfies optimized conditions.

6730-48, Session 11

Investigation of airborne molecular contamination adsorption rate as storage materials in mask

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The issue of a related haze has gradually increased in the 65nm node technology and below. This haze has been reporting that it is caused by chemical reaction among ions like SO42-, NH4+ and aromatic hydrocarbon compounds such as butylated hydroxy toluene (BHT), toluene on the mask by 193 nm laser in general. And it is decreasing lifetime of the mask and that causes pattern defect. However, these ions and aromatic hydrocarbon compounds on the mask are generated from storage materials as well as chemical residue in the mask process. Therefore we investigated the adsorption rate of airborne molecular contamination (AMC) as quartz and Cr-layer and as storage materials which were assumed source of the haze generation.

We analyzed quantitative and qualitative of adsorbed ions and aromatic hydrocarbon compounds on the each layer to verify the effects as storage materials for some storage periods by various analysis technique such as thermal desorption gas chromatography/mass spectrometer (TD GC/MS) and ion chromatography (IC). From the experimental results, we could verify that the adsorption rate of AMC was different as storage materials and layers.

6730-49, Session 11

Study of time dependent 193-nm reticle haze

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While significant progress has been made in the reducing the occurrence rate of progressive defect growth on photomasks at 193nm the issue remains significant for semiconductor fabs. Increasing evidence from multiple sources indicates that further reduction in haze risk involves closely controlling the storage and exposure environment of the photomask. Controlled testing is needed to characterize the impact of environment and individual components on growth in order to guide photomask users and equipment and material providers in proper storage and use of photomasks in order to reduce the risk of haze growth.

In continuation of work reported by Toppan Photomask previously new test apparatus was built that allows generating and maintaining stable and controlled levels of different impurities potentially effecting haze growth down to single part-per-trillion range. Supported by on-line and off-line analytical methods and instrumentations new experimental set-up allows to conduct experiments of unprecedented accuracy.

Different classes of pollutants in different combinations have been studied to exactly characterize environmental sensitivity of different types of 193 nm reticles.

Authors report further progress on the study of effect of environmental conditions on severity and rate of haze formation.

6730-50, Session 11

Full sulphate-free process: joint achievement of minimal residual ions and yield improvement

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Reducing the amount of ionic residues coming from cleaning chemistry became necessary for photomask manufacturing process in order to eliminate the major cause of haze, especially on photomask for short wavelength exposure.

The achievement of this target involves using sulphate-free steps from resist removal to final cleaning, maintaining good performances on particles or residues removal as well as minimization of pattern damages and preservation of the substrate properties.

In this paper several characteristics of cleaning for high-end mask production are discussed and a tight dependency on substrate and contamination type is highlighted as the major aspect that influences the good performances for ozone-based.

The sulfate-free cleaning used is based on the common strategy using hydrogenated and ozonated water combined with megasonic treatment, chemically doped water and rinses.

The data collected from both tests and real production show that the key point to achieve the full effectiveness is the careful definition of the sequence of treatments and rinses; the details will be discussed focusing on minimization of pattern damages due to chemical’s interaction.

The cleaning capability of the full sulphate-free process is tested on contaminants arising from manufacturing steps and handling and a general improvement of the cleaning performances is demonstrated, achieving an excellent removal performance for contaminations of sizes down to 100nm.

Nevertheless, the careful separation of the tests shows that this approach is not sufficient in case of special contaminants, such as some pellicle adhesives, which are hardly removed in standard conditions. For these cases we developed and applied a pre-treatment before the cleaning in order to reduce the interaction between contamination and substrate,

thus enlarging the removal capability of the ozone-based cleaning and allowing successful reworks also for mask recertification.

The focusing combination of surface preparation and cleaning treatments that interacts reciprocally brings to a collective effect that extends to all the contaminants the repeatability of the results in terms of cleanliness and preservation from damages. The ion chromatography measurements confirm that the sulphate residues can be reduced by more than 75% with respect to our best achievement SO4 cleaning.

6730-51, Session 12

Using the AIMS™ 193i for hyper-NA imaging applications

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AIMS™ tools have traditionally been used for reticle repair verification and for reticle defect review by hardware emulation of the aerial image under scanner conditions. The newest generation of these tools, AIMS™45-193i, however, also offers the ability to convert the measured image intensity-maps into a scanner-equivalent image, by taking into account emulation of vector-, and polarization effects in immersion lithography. The result is an image that should correspond to the actual image-in-resist of a Hyper-NA immersion projection system, obtained with the actual mask used in the experiment. As such, this tool can be used to look at Hyper-NA imaging-related topics.

The current work presents the results of an initial exploration study, in which we compared measurement results obtained from the AIMS™45-193i with simulation data and wafer measurements (primarily from exposures on an ASML XT:1700Fi NA=1.20 immersion scanner). The goal of this comparison was twofold:

- Test the validity of the Hyper-NA emulation mode of the AIMS™45-193i, by doing experiments with a known outcome or one that can be quantitatively compared to data from exposed wafers, without (too much) 'interference' from resist effects.
- Try out some of the potential imaging applications that one could potentially use an AIMS™45-193i for. This included Exposure-Latitude (EL), MEF and Depth-of-Focus (DOF) comparison of different structures and mask stacks, as well as CD- and Bossung-curve measurements from 2D litho structures and OPC-related measurements.

All these data were obtained in the Hyper-NA scanner-emulation mode, and for all data we generated comparative material either from wafer-CD measurements or from rigorous simulations.

The current paper will present the results of all these experiments. The results from this work can be summarized as follows. The test in which we tried to validate the Hyper-NA emulation mode yielded very positive results: the AIMS™45-193i measurements were in very good agreement with expected results or with the results we measured from exposed wafers. The comparison of DOF, MEF en EL showed similar trends between AIMS™45-193i and wafer data. Also CD measurements from 2D structures from intensity contours extracted from AIMS™45-193i images were found to show comparable trends as direct measurements from printed wafers.

In summary, this initial evaluation study of the use of AIMS™45-193i for Hyper-NA imaging related studies turned out to be quite encouraging. AIMS™45-193i seems to be able to predict correct trends for a number of lithography quantities, and also allows to preview imaging performance at NA values that are not yet available on existing scanners, always taking into account the correct mask-contribution. As such, AIMS™45-193i takes a position between the idealized world of the rigorous simulators and the Hyper-NA lithography scanners (where then also resist effects play their role). We therefore plan to explore the possible applications of AIMS™45-193i in more detail in further work.

6730-52, Session 12

Mask characterization for double-patterning lithography

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Double patterning (DPT) lithography is seen industry-wide as an intermediate solution for the 32nm node if high index immersion as well as extreme ultraviolet lithography will not be ready in time for production. Apart from the obvious drawbacks of additional exposure and processing steps and therefore reduced throughput, DPT possesses a number of additional technical challenges. This relates to exposure tool capability, the actual applied process in the wafer fab but also to mask performance and metrology.

To characterize the mask performance in an actual DPT process, conventional parameters need to be re-evaluated. Furthermore new parameters might be more suitable to describe mask capability. This refers to, e.g., mask pair overlay but also to CD differences between masks of a DPT reticle set. Besides that, local CD variations and local displacement become critical. Finally, the actual mask metrology for determination of these parameters might not be trivial and needs to be set up and characterized properly.

In this paper we report on the performance of two-reticle sets based on a design developed by ASML to study the impact of mask global and local placement errors on a DPT dual line process.

In a first step we focus on reticle overlay. The overlay between two masks evaluated for different wafer overlay targets is compared with results from standard crosses and, most importantly, with measurements on actual resolution structures. The accuracy of registration measurements on structures near the resolution limit of the mask registration tool is evaluated.

In a second step, mask to mask CD variations are addressed. Off-target CD differences as well as variations of CD signatures on both reticles are investigated.

Finally, local CD variations and local displacements are examined. To this aim, local variations of adjacent structures on the reticle are characterized. Local displacements measured by both the mask registration tool and SEM are compared. The contribution of local effects to the overall CD and registration budget is estimated.

6730-53, Session 12

DPL performance analysis strategy with conventional workflow

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Since DPL(Double Patterning Lithography) has been in public as one of candidates for 45nm or 32nm HP since ITRS2006update disclosed, a lot of report of the performances and issues were published. The current main concerns for DPL are evaluation the infrastructures such as decomposition software, advanced photomasks, higher-NA exposure and leading-edge hard-mask process. If there is simpler procedure to evaluate DPL using conventional environment without hard-mask process, the development of DPL is accelerable. Here, the simple evaluation procedure for DPL using actual photomasks and exposure will be presented and combining exposure as the pseudo DPL result in terms of mask CD uniformity, image placement and overlay will be demonstrated. In this evaluation procedure, decomposition restriction, mask latitude and fabrication load are also discussed.

6730-54, Session 12

Estimating DPL photomask fabrication load compared with single exposure

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Since DPL (Double Patterning Lithography) has been identified as one of candidates for 45nm and 32nm HP since ITRS2006 update, several reports of the performance benefits and implentation challenges have been published. DPL requires at least two photomasks with tighter specification of image placement and the difference of mean to target according to ITRS2006 update. On the other hand, approximately half of whole features are written on each photomask and the densest features are eliminated with pitch relaxation. Then the photomask writing data of two sets for DPL and single set for single exposure are evaluated for photomask fabrication load. The design will be automatically decomposed with EDA tool and OPC will be tuned as DPL or single exposure. Not only number of fractured features but also feasibility study of automatic decomposition will be presented and discussed... The consequences of relaxed pitch on process, inspection, repair, yield, MEEF and cycle time will be discussed with results as available.

6730-55, Session 12

Placement or overlay: meeting double-patterning challenges in mask lithography

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Abstract: Mask lithography is already hard pressed to meet placement goals as specified in the International Technical Roadmap for Semiconductors (ITRS). Write and metrology tools must improve basic placement precision; substrate charging imposes complex systematic placement errors; stress relief from the removal of etched absorber affects in-plane distortion. The recent industry move towards the adoption of double patterning techniques accelerates this already challenging specification.

The intent of a placement specification is to infer the relative placement error of one mask to another, a characteristic known as overlay. Placement is the preferred metric because the reference is a known calibration standard, not another mask. Placement assumes mask positional errors are mostly random. Overlay of any two masks can be inferred from the sum of their placement variances. However, many mask placement error sources are systematic, not random. By understanding the characteristics of the systematic error sources it is possible to devise mask use schemes where systematic errors are correlated and thus cancel in the analysis of overlay.

In this paper, we will analyze placement and overlay characteristics of masks manufactured using advanced write and metrology tools as well as the performance expectations of various use cases. In particular we will evaluate the impact of using multiple write and metrology tools on placement and overlay, and we will investigate the impact of temporal placement signature drift on overlay.

6730-56, Session 12

The MEEF NILS divergence for low-k1 lithography

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The extension of 193nm lithography to the 32nm and 22nm semiconductor nodes by use of immersion lithography has substantially increased the influence of thick-mask effects on critical layer patterning. Several recent publications characterize low k1 patterning of various mask stack and materials1-5 and in at least some cases6 simultaneously considered the effect of biasing. Those works generally evaluated contrast, NILS or exposure latitude (all three are proportional to each other) for one-dimensional features as the initial metric for comparison between different mask stacks.

This work takes a different approach for evaluation of mask stacks in that it emphasizes MEEF as a primary metric. This is necessary as the conventional conception that MEEF is proportional to 1/NILS7 and that 'a better contrast will be reflected in a better MEEF'5 is found not be the case for 80nm pitch patterning with 1.35NA. Simulation and experimental data will be presented that show examples where masks that produce higher NILS and higher contrast in fact have significantly worse MEEF than masks with lower NILS and contrast under the same illumination and bias conditions. A wide range of single and dual material mask stacks will be compared for MEEF performance for a variety of illumination and bias conditions.

Analytical MEEF equations are derived describing MEEF as a function of mask bias and EPSM transmission for c-Quad and dipole illumination. While only exact for scalar imaging, thin mask imaging and a threshold resist model; the equations help provide insight into the origin of MEEF not tracking with 1/NILS. The equations show that even when patterning in the regime where thick mask effects are negligible, the optimal bias conditions for MEEF and contrast are different and therefore one must tradeoff contrast for MEEF in selection of bias. The equations also suggest that MEEF is approximately proportional to 1/(image slope) rather than 1/(image log slope). Rigorous thick mask vector simulation with a resist model also find MEEF to be roughly proportional to 1/(image slope).

Usually, the total overlapping process window of most semiconductor layers is limited by the process window of 2D structures rather than nested 1D structures. The process windows of 2D features after basic OPC are compared for different mask stacks and 1D bias conditions. In some cases, mask stack and biasing choices to improve 1D structure process windows can degrade 2D structure process windows and therefore overall layer process window.

1) Yoshizawa, Masaki et al., SPIE Vol. 6283.
2) Erdmann, Andreas et al., SPIE Vol. 6520.
3) Cheng, Wen-hao et al., SPIE Vol. 6520.
4) Kim, Sung-Hyuck et al., SPIE Vol. 6520.
5) Cangemi, Michael et al., SPIE Vol. 6349.
6) Sato, Kazuya et al., SPIE Vol. 6520.
7) Mack, Chris et al., SPIE Vol. 4000.

6730-57, Session 12

Impact of alternative mask stacks on the imaging performance at NA1.20 and above

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The lithographic performance of current state-of-the-art resolution enhancement techniques (RET) will become critical at hyper numerical aperture (NA\>1) due to mask 3D effects. We have studied the impact of the mask material on the lithographic performance at NA 1.2 and above. More precisely, we will use the mask material as RET and search both by rigorous simulations and experiments for improved lithographic performance of line/space (L/S) imaging of the 45nm half-pitch (HP) node at NA1.2 and 1.35.

This work started as a one pitch - one metric optimization [1-3]. Now we broaden the scope to through-pitch imaging evaluation of multiple metrics such as exposure latitude (EL), mask error factor (MEF), and depth-of-focus (DOF). The assessment, both by rigorous simulations and experiments, involves the standard mask stacks, Cr binary mask (BIM) and MoSi 6% attenuated phase shift mask (attPSM), as well as alternatives such as thick Cr BIM, 1% and 6% attenuated Ta/SiO2 PSM, and 1% attenuated Ta/SiON PSM.

In a first phase a thorough simulation study is performed using the rigorous electro-magnetic field (EMF) image and resist lithography simulator DrLiTHO, internal research and development software of the Fraunhofer institute IISB. Commercially available alternative mask materials are explored by optimizing their thickness in combination with the mask structure to increase the contrast taking into account the trade-off with MEF. Next, a through-pitch evaluation of the 45nm HP node at NA1.2-1.35 is

carried out examining max. EL, DOF, best focus shifts, and MEF behavior for the various mask stacks. In the simulation phase we also explore the n&k mask material space in search for a hypothetical mask stack and compare its through-pitch imaging performance to that of standard mask stacks.

The second phase concerns the experimental assessment. Exposures with all mask stacks are performed on a 1.2NA immersion scanner (ASML XT:1700Fi) and a hyper-NA AIMS tool (Zeiss AIMSTM45-193i). For the validation of the simulation methodology a correlation is made between scanner, AIMS, and simulation results indicating the importance of the mask quality and mask properties. For the experimental proof-of-concept we considered the broader scope of optimizing several metrics through-pitch as well as optimizing for one single pitch. Based on the lithographic performance and the mask manufacturability we put together a ranking of the commercially available mask stacks for the 45nm HP node at NA 1.2 and 1.35.

[1] M.Yoshizawa, et al., “Impact of the absorber thickness variation on the imaging performance of ArF immersion lithography”, Proc. SPIE 5853, 243 (2005).

[2] M.Yoshizawa, et al., “Optimizing absorber thickness of attenuating phase-shifting masks for hyper-NA lithography”, SPIE 6154-51,1E, (2006).

[3] M.Yoshizawa, et al., “Comparative study of bi-layer attenuating phase-shifting masks for hyper-NA lithography”, SPIE 6283, 1G, (2006).

6730-58, Session 12

Requirements of photomask registration for the 45-nm node and beyond: is it possible?

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As semiconductor features shrink in size and pitch, the pattern placement error at photomask, that is, the registration becomes more important factor to be reduced. Following ITRS roadmap, the registration for sub-45 nm node is required to be less than 5 nm but this specification still corresponds to the challengeable goal. Among several reasons to induce registration, here, we have focused on the three major registration errors: e-beam positioning error, the effect of absorber etching, and the effect of pellicle attachment. We quantify each error after tuning and optimization and analyze it with the help of finite element modeling. Furthermore, we compare the registrations due to absorber etching between binary mask and phase-shift mask and between conventional blank and stress-free blank. Based on these results, we present the current status and the goal of each error for the roadmap of sub-45 nm node and discuss it according to the kind of mask and blank type.

6730-59, Session 13

Simulation of larger mask areas using the waveguide method with fast decomposition technique

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In the framework of the integrated European research project “More Moore” Fraunhofer IISB has developed a new rigorous electromagnetic field (EMF) solver for fast three dimensional (3D) EUV lithography mask near field simulations based on the waveguide method. Because of the excellent EUV simulation performance, an extension of the solver for optical lithography mask simulations (e.g. at 193 nm) was implemented. In the optical case, the convergence is a basic problem of all EMF solvers based on modal methods. After extensive speed and convergence optimizations a very good performance for this case could be realized too. However, with this approach full 3D simulations of larger mask areas (e.g. 10 μm x 10 μm, mask scale) are not possible within an acceptable time frame. Therefore a decomposition technique for the waveguide method with an optimized field composition in the frequency domain was developed. This new approach enables both fast 3D simulations and 3D simulations of larger lithography mask areas.

This paper presents the basic theory of the new simulation approach. Application examples of state of the art optical and EUV lithography masks demonstrate the superior performance in terms of computation time, memory requirement, and convergence. Special attention is paid to the comparison and verification of the new approach with full 3D simulations providing the most accurate results and serving as reference. Based on detailed simulation studies of state of the art lithography systems like hyper-NA and EUV systems the range of validity of the new approach and deviations from full 3D simulations are investigated.

6730-60, Session 13

Polarization aberration modeling via Jones matrix in the context of OPC

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The increasingly stringent demand for shrinkage of IC device dimensions has been pushing the development of new resolution enhancement technologies in micro- lithography. High NA and ultra-high NA (NA\>1.0) applications for low k1 imaging strongly demand the adoption of polarized illumination as resolution enhancement technology since proper illumination polarization configuration can greatly improve the image contrast hence pattern printing fidelity. For polarized illumination to be fully effective, all the components in the optical system ideally should not alter the polarization state during propagation from illuminator to wafer surface. In current lithography and OPC modeling tools, it is typically assumed that the amplitude and polarization state of the electric field do not change as it passes through the projection pupil. However, in reality, the projection pupil does change the amplitude and the polarization state to some extent, and ignorance of projection pupil induced polarization state and amplitude changes may cause CD error out of specification at 45nm device generation and beyond.

We developed an OPC-easily-deployable modeling approach to model polarization aberration imposed by projection pupil via Jones matrix format. The polarization aberration modeling has been integrated into Synopsys OPC modeling tool, ProGen, and its accuracy and efficiency has been validated by comparing with industry standard lithography simulator SolidE. Our OPC simulation showed that the impact of projection pupil polarization aberration on optical proximity effect could be as large as several nanometers, which is not negligible given the extremely stringent CD error budget at 45 nm node and beyond. This modeling approach is applicable to arbitrary polarization aberration imposed by other elements (e.g. mask pellicle induced polarization) in the lithography system as long as it can be characterized in Jones matrix format.

6730-61, Session 13

Validation of a fast and accurate 3D mask model for 25-nm SRAF printability analysis

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As the lithography process entered below the 45 nm node, 4x reticles for leading-edge chip designs have minimum feature sizes much smaller than the wavelength of light used in advanced exposure tools. The traditional thin-mask approximation is no longer accurate at sub-wavelength dimensions, where topographic effects arising from the vector nature of light become noticeable. Although rigorous 3D electromagnetic filed simulation has become necessary in aerial image formation of a thick-mask, i.e., a PSM mask, it often is computationally too expensive and hence is not viable for full-chip lithography modeling. A new 3D thick mask model has been developed to create fast and accurate image-based mask 3D model that incorporate polarization and scattering effects as well as the non-Hopkins oblique incidence effects commonly found in immersion lithography systems.

In this work, we first validate the 3D mask model by comparing the simulation results from the 3D mask model to the results from rigorous electromagnetic field simulation using a mask consisting of many 25 nm SRAF features placed with various CDs and pitches. We then build a group of 3D mask models for both bright-field and dark-field attPSM

and binary masks to investigate the severity of 3D mask effects and the printability of 25 nm SRAF features for the masks under study. The simulations are for 193 nm immersion lithography with various illuminations, such as dipole, quasar, and annular illumination as well as different polarizations. Next, we show the robustness of the 3D mask model to various mask feature errors, for example, CD variation. Finally, in order to predict CD sizes of the targeted features formed on a substrate while various sized SRAFs are applied, we use a resist model to simulate the effect of 3D mask aerial images interacting with the photosensitive resist layer and the subsequent post-exposure bake (PEB) and development process. Our simulation results show that the 3D mask model provides improved accuracy compared to the thin-mask model.

6730-62, Session 13

Fast three-dimensional simulation of buried EUV mask defect interaction with absorber features

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To simulate the interaction of buried defects and absorber features in EUV masks, a full three-dimensional, fast, integrated, simulator based on ray tracing and a thin mask model is presented. This simulator allows rapid assessment of the effects of buried defects on EUV printing. The most important qualities of this simulator are its high speed and low memory requirements. It can perform accurately on a single processor personal computer in minutes, a simulation that would require a multiprocessor cluster and many hours of runtime if done using a rigorous method.

This 3D simulator uses the same general methodology as the 2D simulator presented in [1]. The multilayer and absorber pattern are simulated separately using a different method for each. The multilayer is simulated using a ray tracing program [2], and the absorber is simulated using a propagated thin mask model [3]. These simulators are optimized for EUV multilayer blanks and absorber patterns respectively. Two Fourier transforms are performed, one for the downward propagation and one for the upward reflection, to link these simulators together. The Fourier transforms convert the complex near field output of one simulator into a set of plane waves that can be input into the other. The simulator also models the growth of an EUV multilayer with a buried defect using the models described in [4].

Simulation examples will be given to demonstrate the accuracy of the simulator, as well as give insight into the effects of defects on EUV printing. Comparisons with experimental results, as well as rigorous FDTD simulations will be given. The nature of the fields after each step of the program will be examined to help isolate the effects of the defect and absorber to better understand the interaction between the defect and the pattern. This fast simulator will allow the characterization of many defect pattern combinations, and initial results and trends will be shown to help determine what defects can and can't be tolerated in EUV printing.

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6730-63, Session 13

Polarization-induced astigmatism caused by topographic masks

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With the continuous shrink of feature sizes the pitch of the mask comes closer to the wave length of light. It has been recognized that in this case, polarization effects of the mask become much more pronounced and deviations in the diffraction efficiencies from the well known Kirchhoff approach can no longer be neglected. To accommodate these effects, most modern lithographic simulation tools nowadays possess the capability to simulate the topographic effects by rigorously solving Maxwell's equations for the given mask structures. It is not only the diffraction efficiencies that become polarization dependent also the phases of the diffracted orders tend to deviated from Kirchhoff theory when calculated rigorously. These phase deviations can mimic polarization dependent wave front aberrations, which in the case of polarized illumination can lead to non-negligible focus shifts that depend on the orientation and the size of the mask features. This orientation dependence results in a polarization induced astigmatism offset, which can be of the same order of magnitude as polarization effects stemming from the lens itself. Hence, for correctly predicting polarization induced astigmatism offsets, one has to both consider lens and mask effects at the same time. In this paper we present a comprehensive study of polarized induced phase effects of topographic masks for various CD through pitch series. We compare our simulations against measurements using both full resist experiments and scanner equivalent PHAME phase and transmission measurements for attPSM and COG masks.

6730-64, Session 13

Characterization and monitoring photomask edge effects

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An experimental technique for quantitatively characterizing edge effect contributions in thick photomasks is described and evaluated through an electromagnetic simulation of the experiment. At 65 nm both Alternating Phase Shifting Mask (ALT-PSM) and Attenuationg Phase Shifting Mask (ATT-PSM) have significant edge effects. For example, it was reported that in ordering ALT-PSM the phase-shift depends on feature size. Also, the particular feature size for the 180o phase-shift must be specified in advance [1]. Further, even the slight transmission of the chrome can contribute to the performance of ALT-PSM [2].

Our experimental approach is based on the observation that edge effects on line equal space dense patterns are similar on both edges and for an ALT-PSM have a period of roughly one half that of the physical mask. This makes the added diffraction from the edge contributions appear in the position of the zero order diffraction from a thin masks model of the physical mask. Since the thin mask model of the line equal space has no first order diffraction energy, the edge contributions are directly observable. By slightly varying the duty cycle around 50% to induce a known and real thin-mask electric field component, both the real and imaginary parts of the edge effect contribution can be deduced. The real electric field component from the edges is proportional to the shift in the position of the minimum energy in the zero order from 50% duty cycle. The square root of the minimum zero order diffraction energy normalized to a clear mask then gives the imaginary edge contribution. A similar approach works for the ATT-PSM with a N:1 ratio, where N depends on the transmittance of the attenuating layer.

We will report on the simulation verification of a planed experiment with test layouts measured via an ellipsometer run in transmission mode. The simulation consisted of using TEMPEST to run FDTD electromagnetic simulations of mask openings. ALT-PSMs were simulated with varying opening size, ranging from 30 to 70 percent duty cycle. Simulations results show the expected “V”shape of the zero order diffraction and its dependence on pitch. The edge source strengths were then extracted from the simulation versus period. By modeling the additional field components as rectangles centered at the edge location with unity height, the contributed fields can be described by the width of these boxes. For a chromeless mask with TE illumination, the additional fields were approximately 0.1 wavelengths for the real and 0.15 wavelengths per edge for the imaginary components. TM illumination showed a smaller effect on the real contribution and larger addition from the imaginary fields, with corrections of 0.05 and 0.25 wavelengths per edge respectively. Similar analysis of ATT-PSM will be presented.

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[2] Shoji Hotta, Thomas V. Pistor, Konstantinos Adam, Andrew R. Neureuther, "Effects of shifter edge topography on through focus performance," Proc. SPIE Vol. 4186, p. 827-837, Jan 2001.

6730-65, Session 13

Understanding mask topography in attenuated phase-shift masks

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Lithographer of the early 1980's declared the end of optics for sub-0.5μm imaging. However, significant improvements in optics, photoresist and mask technology continued through the mercury lamp lines (436, 405 & 365nm) and into laser bands of 248nm and to 193nm. As each wavelength matured, innovative optical solutions and further improvements in photoresist technology have demonstrated that extending imaging resolution is possible thus further reducing k1. Several authors have recently discussed manufacturing imaging solutions for sub-0.3k1 and the integration challenges. At such low k1 values the primary mask patterns can be on the order of the wavelength of a conventional exposure system and even lower. Thus making the topography effects important.

As previously discussed in the literature, mask topography causes a smooth transition of intensity at the feature's edges and some intensity modulation within and outside the feature which brings in extra phase information or phase errors that cause a focus shift and tilt of the focus exposure curves. These effects are pitch dependent resulting in a reduction of the common process window. EMF calculations show that the phase errors can be compensated by changing the phase angle on the mask such that the best focus of different pitches are centered at zero defocus. We have extended the previous work and found that the phase errors increase with increasing mask transmission, making phase angle correction on the mask more important at higher transmissions. In this paper the authors will explain these effects through rigorous EMF calculations of diffraction efficiencies and phases of the diffracted orders as a function of mask transmission and provide a guideline for which mask transmission these topography effects should be addressed during mask manufacturing.

6730-66, Session 13

Fast and accurate laser band-width modeling of optical proximity effects

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The development of ultra-high NA lithography systems is enabling continued density scaling of semiconductor devices by providing improved resolution and lower overlay tolerances. In addition to resolution and overlay, device scaling requires improvements in quality and stability of both the lithography equipment and process in order to minimize all sources of variability which diminish the effectiveness of the optical proximity correction (OPC). A decade of improvement in excimer laser bandwidth stability has scaled with the reduction in usable depth of focus (uDOF) and increasing numerical apertures in KrF and ArF lithography. The characterization of imaging effects due to laser bandwidth has been gaining importance[1-6] and is starting to be introduced for improved OPC modeling.

As the industry continues beyond 65nm and 45nm IC node manufacturing, lithography simulation enters the domain where the image-model residual errors need to be lower than 1nm,[7] placing importance on understanding computation errors and quality of the simulation input parameters. Physically-accurate estimates are needed for the optical material properties of the imaging medium and photomask topography in addition to characteristic fingerprints of the imaging system. Although, for OPC, calibrated reaction-diffusion resist models are replaced with empirical transfer functions, the imaging model requires equivalent (<<1nm) accuracy so that post-OPC edge-placement errors are minimized.

In this work, we consider the effects of common approximations for modeling the contribution of finite (non-monochromatic) laser bandwidth, namely the modified Lorentzian[8] and Gaussian forms. Although the approximations are simple to use, they induce significant CD error when compared to usage of representative spectral shapes which can be obtained using high-resolution spectrophotometry. Recent advances in commercial lithography simulation tools have enabled direct input of actual measured laser spectra and, for example, PROLITH[9] now features a benchmark full brute-force calculation and several high-speed approximations for imaging using finite laser bandwidth.[10] For our work here, we assess the accuracy-speed tradeoff and demonstrate the need for inclusion of laser spectrum information for accurate OPC. We propose a novel physically-based spectrum approximation method, which considerably reduces computation time at a cost of <0.25nm residual error from fully accurate image calculation. Additionally, we compare 45nm-node calibrated resist model to latent image results for 0.92NA dry and 1.2NA immersion processes including measured illumination pupil profiles and the presence of lens aberrations. Finally, the sensitivity of 2D line-end patterns and typical logic gate-process OPC designs are considered. Our conclusions point to extensions and approaches for integration with EDA tools for OPC model generation and process-variability verification.

6730-67, Session 14

Advanced mask particle cleaning solutions

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The majority of trends in lithography technology necessitate the use of smaller, higher aspect, patterns on photomasks which are increasingly sensitive to traditional cleaning processes. Particle defects are of increasing concern since, in deep and even overhanging structures, they can become fixed to the surface with such strength that any traditional cleaning technique would destroy any small, high-aspect, mask structures. A series of advanced new solutions are presented here which have been shown to remove these types of problem particles as applied to 45 nm node nanomachining mask repair with a RAVE nm450 system. In the first method, a cryogenic cleaning system is modified to greatly enhance selective removal of nanoparticles from high aspect structures. In the second method, the nm450 repair tool itself is applied to selectively remove targeted particles from a nanoscale area of the mask surface thus only affecting the region of interest and not touching any sensitive surrounding surfaces or structures.

6730-68, Session 14

Integrated photomask defect printability check, mask repair, and repair validation procedure for phase-shifting masks for the 45-nm node and beyond

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The decreasing feature sizes as induced by the ITRS and other proprietary roadmaps have a growing impact on the cost of current and future photolithographic masks. The assessment, repair and repair validation of these expensive masks has become a very substantial factor of the total mask production cost. The introduction of immersion lithography and the proposed introduction of double exposure strategies will further amplify this trend.In order to make the whole procedure more manageable in a production environment, with its constraints on timing and resource allocation, a seamless workflow of the

named procedure is sought. A proposed way to achieve this is the set up of a dedicated tool set with a backbone infrastructure designed for this workflow as well as for the specific high resolution task. In this paper we concentrate on masks with feature sizes relevant for the 45nm node and defects with typical size and shape as they appear in production. Phase shifting masks with defects have been selected and the printability of the defects analyzed with an AIMS 45-193i. In part the defect outline and three-dimensional shape as well as further characteristics have been visualized with a photomask specific Zeiss SMART-LE electron microscope, prior to repairing them with an electron beam based

repair system. The specifics of the repair process step, including pre- and post-repair imaging, will be explained in great detail. The final step of the process will be a subsequent validation of the repair, again under the same illumination scheme as the immersion scanner utilized by the masks end user.

In addition we will show the behavior of the phase of the mask in the region of interest, that is in this case the repair area and its immediate vicinity. This will be done by a special new tool, named PHAME, developed for measuring the actual phase of smallest mask features in-die. We will outline how the employment of the proposed workflow and the integration of the toolset will significantly enhance the output of a maskshop by guaranteeing a very high success rate of single-pass repairs.

In the summary we will give an outlook how the proposed workflow and the employed technologies will behave with regards to masks as expected to emerge for the 32nm node and which enhancements will need to be implemented to extend the technologies to cope with the respective requirements.

6730-69, Session 15

A semi-automated AFM photomask repair process for manufacturing application using SPR6300

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The Photomasks complexity, their tight specifications and relevant production cost have induced the improvement of Repair capabilities, which have been recognized as primary vehicles to recover the Yield of High-End masks.

Nanomachining technique for repairing photomask defects has marked the expected jump forward.

This technique, studied in the last decade, is based on AFM (Atomic Force Microscopy) and applies a mechanical removing of the defect with almost negligible quartz-damage, high accuracy of the edge-placement and without spurious depositions (stain, implanted elements, etc.) that may affect the optical transmission.

Now AFM Nanomachining approach is going to reveal properties of repeatability and user-friendly utilization that make it suitable for the Production environment.

SII NanoTechnology Inc. (SIINT) has carried out a joint-development project with DNP Photomask Europe S.p.A. (DPE) that has allowed the installation in DPE of the next generation state-of-the art AFM based system SPR6300 to meet the repair specifications for the 65 nm Node.

The first application, developed on the SPR6300, is a process to remove particles/contaminations. An AFM based scanning method, making use of a diamond probe and cantilevers with low spring constant, pushes the particles away, modifying their adhesion so that the next wet cleaning process is effective in washing them out.

Since the implementation of this method in DPE up to now, 1-year period, the success rate of the particle removal process is practically 100%. No damage on Quartz has ever been revealed by AIMS certification.

The second application is the Repair process of hard defects on Molybdenum Silicide (MoSi) and Binary Chrome on Glass (COG) photomasks.

Drift phenomena represent the major obstacle in whichever kind of manipulation (imaging and material or pattern modification) by “nano-probes”. The new repair method, called New DLock, implemented on SPR6300, is an automated one by which the Drift amount, regardless of its origin, is estimated before repairing and compensated during the process. The Scratch repair process is a recipe composed by one Drift forecast, followed by programmed multiple scratching steps. The diamond probe is mounted on a cantilever with high spring constant in response to MoSi and chrome hardness.

This approach has been applied to repair 100 nm edge-defects both on ArF-MoSi and COG masks. The remarkable results, in agreement with the requirements for the 65 nm Node, are: Edge placement 3* error within 10 nm and AIMS FAB 193nm light-transmission loss less than 3% , associated with CD variation at defocus(±0.2μm) less than 7%.

Both the Particle Removal and Repair processes are assisted by a new imaging contact-less AFM scanning, called SIS (Sampling Intelligent Scan), which allows a reliable and extremely soft interaction with the substrate.

In conclusion, peculiar features concerning accuracy, automation and Drift-compensation, make SPR6300 process a suitable AFM approach to repair hard defects inside a manufacturing context.

6730-70, Session 15

Repairing 45-nm node defects through nano-machining

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Recently questions have been raised about whether high aspect ratio (HAR) NanoBits™ can be effectively utilized to repair extension defects in 45 nm node and beyond. The primary concern has been how the effect of NanoBit™ deflection impacts edge placement and depth control repeatability. Higher aspect ratio diamonds are required for defects that arise as mask feature sizes become smaller. As the aspect ratio of the NanoBit™ continues to increase to meet these demands, the cross sectional area of the diamond used for nanomachining becomes thinner and more susceptible to bending under the forces applied during the nanomachining process. This is especially true when deeper features that require the HAR NanoBits™ are being repaired. To overcome this trend RAVE LLC has developed a new repair process that utilizes the strength of the diamond shape. Repair of 45 nm node defects that require HAR NanoBits™ will be demonstrated as well as comparisons of the new and old repair processes.

6730-71, Session 15

The cleaning effects of mask aerial image after FIB repair in sub-80-nm node

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The Aerial Image Measurement Tool (AIMS) can estimate the wafer printability without exposure to wafer by using scanner. Since measured aerial images are similar with wafer prints, using AIMS becomes normal for verifying issue points of a mask. Also because mask design rule continues to shrink, defects and CD uniformity are at issues as factors decreasing mask yield. Occurred defects on a mask are removed by existing mask repair techniques such as nanomachining, electron beam and focused ion beam. But damages and contaminants by chemical and physical action are found on the mask surface and contaminants above special size lead to defects on a wafer. So cleaning is necessary after repair process and detergency has been important. Before AIMS measurement, cleaning is done to make same condition with shipped mask, which method brings repeated process - repair and cleaning - if aerial image was not usual.

So cleaning effect after the FIB repair is tested by using the AIMS to find the optimized process minimizing the repeated process and to get similar scanner results. First, programmed defect mask that includes various defect size and type is manufactured on some kinds of patterns in DRAM device and sub-80nm tech. Next the defects on the programmed mask are repaired by FIB repair machine. And aerial images are compared after the chemical cleaning, non-chemical cleaning and without cleaning.

Finally, approximate aerial images to scanner results are taken regardless of cleaning process. It means that residue originated from repair process dosen’t affect aerial images and flexible process is possible between AIMS, repair and cleaning process. But as the effect of minute particles and contaminations will be increased if pattern size is much smaller, it needs to reconfirm the effect below the sub-65nm in DRAM device.

6730-72, Session 16

Wafer inspection as alternative approach to mask defect qualification

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Defect qualification is one of the key processes during the manufacturing and life time of high-end photomasks. The absence of any printing defect on the patterned mask is an ultimate requirement, and considerable effort by defect inspection and repair is required in order to eliminate these defects.

Ever shrinking feature sizes make especially the defect inspection increasingly difficult. This holds for both the detection of critical defects and the inspectibility of small mask features including sub-resolution assist features (SRAF). On mask level, critical defects as small as 26nm and minimum assist features below 50nm are expected for the 32nm node by the ITRS 2006. Direct imaging of the photomask with DUV light is todays standard approach. It was improved considerably by a reduction of the inspection wavelength and the development of smaller pixels. However, the mask features and defects to be inspected will be far below the inspection wavelength in the future.

This paper evaluates the feasibility of wafer inspection as an alternative approach to the mask defect qualification. Here, the mask is first printed on wafer which is then inspected with standard wafer-inspection tools. Mask defects show up as repeating defects in the various exposure fields and can be filtered efficiently from process or stochastic defects.

Although more process steps are required for wafer inspection compared to direct mask inspection there are some fundamental advantages inherent to an inspection of the printed image. The real wafer pattern is inspected including all lithography and resist effects and omitting non-printing defects. Also, the inspection of SRAFs is strongly facilitated since they do not print on the wafer and only their impact on the final image is assessed. Last, this approach relies on infrastructure of IC fabs with much stronger market penetration.

The investigations focus on the detection performance of wafer inspection and a proof of concept for a potential process flow. Programmed defects of various types were distributed in dense line/space patterns of 65nm technology. These patterns were printed on a bare Si wafer and the resist pattern was inspected with a single recipe. We were able to inspect patterns both with and without SRAFs. A similar detection threshold was found for all defect types with minor gap only to printability. Finally, the back-tracking of detected defects from wafer to mask was successfully evaluated in order to enable a subsequent defect repair on the mask.

6730-73, Session 16

A pragmatic approach to high-sensitivity defect inspection in the presence of mask process variability

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As design rules continue to shrink towards 4x nm, there are increase usage of aggressive OPCs in reticle manufacturing. One of the most challenging aggressive OPCs is Sub Resolution Assist Feature (SRAF) such as scattering and anti-scattering bars typically used to overlap isolated and dense feature process windows. These SRAF features are sub-resolution in that these features intentionally do not resolve on the printed wafer. Many reticle manufacturers struggle to write these SRAFs with consistent edge quality even the most advanced E-Beam writers and processes due to resolution limitations. Consequently, this inconsistent writing gives reticle inspection challenges. Large numbers of such nuisance defects can dominate the inspection and impose an extraordinarily high burden on the operator reviewing these defects. One method to work around inconsistent assist feature edge quality or line-end shortening is to adjust the mask inspection system so that there is a substantial sensitivity decrease in order to achieve good inspectability, which then compromises the sensitivity for the defects on main geometries.

Modern defect inspection tools offer multiple modes of operation that can be effectively applied to optimize defect sensitivity in the presence of SRAF feature variability. This paper presents the results of an evaluation of advance inspection methods and modes such as die to database selective thinline desense, transmitted & reflected light inspections, and die to die selective desense to increase inspectability and usable sensitivity using challenging production and R&D masks. Key learnings are discussed.

6730-74, Session 16

Sensitivity comparison of fast integrated die-to-die T+R pattern inspection and STARlight2™ mode for application in mask production

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Fast Integrated Die-to-Die T+R pattern inspection and STARlight2 TM (SL2) contamination inspection are employed by mask makers in order to detect pattern defects and contamination defects on photomasks for in process inspection steps.

In this paper we systematically compare the detection capabilities of the two modes on real production masks with a representative set of contamination and pattern defects.

During the study we collect and analyze inspection data on several critical layers such as lines & spaces and contact holes. Besides performance of the modes on product plates characterization was done using a test mask with programmed defects.

Additional advantages of Fast Integrated Die-to-Die T+R mode found in the study are improvements for productivity and ease of use.

6730-75, Session 16

Optimizing defect inspection strategy through the use of design-aware database control layers

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Resolution limitations in the mask making process can cause differences between the features that appear in a database and those printed to a reticle. These differences may result from intentional or unintentional features in the database exceeding the resolution limit of the mask making process such as small gaps or lines in the data, line end shortening on small sub-resolution assist features etc creating challenges to both mask writing and mask inspection. Areas with high variance from design to mask, often referred to as high MEEF areas (mask error enhancement factor), become highly problematic and can directly impact mask and device yield, mask manufacturing cycle time and ultimately mask costs.

Specific to mask inspection it may be desirable to inspect certain non-critical or non-relevant features at reduced sensitivity so as not to detect real, but less significant process defects. In contrast there may also be times where increased sensitivity is required for critical mask features or areas. Until recently, this process was extremely manual, creating added time and cost to the mask inspection cycle. Shifting to more intelligent and automated inspection flows is the key focus of this paper. A novel approach to importing design data directly into the mask inspection to include both MDP generated MRC errors files and LRC generated MEEF files.

The results of recently developed inspection and review capability based upon controlling defect inspection using design aware data base control layers on a pixel basis are discussed. Typical mask shop applications and implementations will be shown.

6730-76, Session 16

Progressive growth defect disposition and printability for 65-nm and 45-nm ArF immersion lithography

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In this paper, progressive growth defect disposition and printability for 45nm and 65nm lithography are evaluated using an Automated Mask Defect Disposition tool (AMDD). Preprogrammed hard defect defects on mask with minimum defect size of 160nm are studied. These mask defects are scanned by STARlight inspections with different pixel sizes of P90, P125, and P150 for mask defect capturing. Aerial Image Measurement System (AIMS) and printed photoresist feature are used for modeling. Line, space and hole in both bright and dark filed are used for model set up. Printability for these programmed mask defects is determined from process critical dimension (CD) variability. Experiment result using 193nm immersion tool with effective NA of 1.2 imaging lens is used to expose the programmed defect mask. The resist CDs response to the mask defect area are measured under the different process conditions, i.e., different exposure dose or focus. The correlation of AIMS CD, AMDD CD and wafer CD for different defect types and sizes to the printability is performed. Scan result of progressive defects are captured and verification of its printability using AMDD are obtained.

6730-77, Session 16

Characterizing DUV contamination inspection capabilities using programmed defect test reticles

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The ORION™ series of test reticles have been used for many years as the photomask industry standard for evaluating contamination inspection tools and algorithms. The deposition of PSL (Polystyrene Latex) spheres on various reticle pattern designs allow STARlight™ tool owners to measure the relative contamination inspection performance in a consistent and quantifiable manner. However, with recent inspection technology advances such as shorter laser (light source) wavelengths and smaller inspection pixels, PSLs have been observed to physically degrade over relatively short time periods: especially for the smallest sized spheres used to characterize contamination inspection performance at the most advanced technology nodes.

Investigations into using alternative materials or methods that address the issue of PSL degradation have not yet proven completely successful. Problems such as failing to properly adhere to reticle surfaces or identifying substances that can produce consistent and predictable sphere sizes for the reliable manufacture of these critical test masks are only some of the challenges that must be resolved. Even if these and other criteria are met, the final substance must appear to inspection optics as pseudo soft defects in order to resemble actual contamination that inevitably appears on production reticle surfaces. In the interim, programmed pindot defects present in the quartz region of the SPICA™ test reticle are being used to characterize contamination performance while a suitable long-term solution to address the issue of degrading PSLs on ORION™ masks can be found.

This paper examines the relative effectiveness of different test reticles as system monitors for DUV contamination inspection tools. The characteristics of an operative inspection tool standard will be outlined and presented. Finally, a newly developed programmed defect test reticle designed specifically to evaluate contamination algorithms will be introduced and compared with existing standards.

6730-78, Session 16

Mask inspection method for 45-nm node

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Abstract

As required sensitivity specification of mask defect inspection tool is shrinking to below 50nm of defect size at the 57nm tech node, manufacturable solutions are not known. To enhance sensitivity of inspection tool, various inspection methods are applied to enhance the resolution of system, such as higher NA, shorter wavelength, confocal optics and RET(resolution enhancement technique). Permitted defect sizes are determined by feature size and pattern layout, because the performances of inspection tools are different according to defect type, size, pattern size and layout. In this paper, we will describe the required defect specification of various pattern layouts of memory device at 65nm node to 45nm node. And various inspection tools with different characters are evaluated on these mask patterns.

Specially, high NA (0.85) inspection tool will be evaluated to compare the sensitivity, through-put, scattering bar size and minimum feature size of other inspection tools on 45nm node.

Keywords: Inspection, sensitivity, required defect size, high NA inspection tool, RET.

6730-79, Session 16

Inspection results for 32-nm logic and sub-50-nm half-pitch memory reticles using the TeraScanHR

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Results from the recently available TeraScanHR reticle inspection system were published in early 2007. These results showed excellent inspection capability for 45nm logic and 5xnm half-pitch memory advanced production reticles, thus meeting the industry need for the mid-2007 start of production. The system has been in production use since that time. In early 2007, some evidence was shown of capability to inspect reticles for the next nodes, 32nm logic and sub-50nm half-pitch memory, but the results were incomplete due to the limited availability of such reticles. However, more of these advanced reticles have become available since that time. Inspection results of these advanced reticles from various leading edge reticle manufacturers using the TeraScanHR are shown. These results indicate that the system has the capability to provide the needed inspection capability for continued development work to support the industry roadmap.

6730-80, Session 16

Automatic optimization of MEEF-driven defect disposition for contamination inspection challenges

T. Huang, A. Dayal, K. Bhattacharyya, KLA-Tencor Corp.

Ever-tightened design rules and ensuing aggressive OPC features pose significant challenges for wafer fabs in the pursuit of compelling yield and productivity. The introduction of advanced reticles considerably augments the mask error enhancement factor (MEEF) where progressive defects or haze, induced by repeated laser exposure, continue to be a source of reticle degradation threatening device yield. High resolution reticle inspection now emerges as a rescue venue for wafer fabs to assure their photomask integrity during intensive deep UV exposure. Integratedly designed in the high resolution reticle inspection, a MEEF-driven lithographic detector “Litho3” can be used run-time to group critical defects into a single bin. Previous investigations evinced that critical defects identified by such detector were directly correlated with defects printed on wafer, upon which fab users make cogent decisions towards reticle disposition and cleaning therefore reduces cycle time.

One of the challenges of implementing such detector resides in the lengthy set up of user-defined parameters, from practitioner standpoint, can considerably extend reticle inspection time and inevitably delay production. To overcome this, an automatic off-line program has been written to optimize Litho3 settings based off a pre-inspection in which only default Litho3 values are needed. Upon completion of the pre-inspection, the images are then scanned and processed to extract the optimal Litho3.A, Litho3.B and Litho3.C values that are largely dependent upon the feature size characteristics and local MEEF. Thus optimized Litho3 parameters can then be input into the recipe set up to enable a real-time inspection, as such fab user can timely access the defect criticality information for subsequent defect disposition. In the interest of printability

validation, such defect information and associated coordinates can be passed onto defect review via XLINK for further analysis. Corresponding MEEF values are also available for all identified critical defects. Through this automatic program the set up time for Litho3 can be reduced by up to 90%.

For high capacity production fabs running a pre-inspection is deemed infeasible; this automatic optimization program can also serve as a direct interpretation of any regular reticle inspection even without invoking Litho3, yet in the end provide output in the context of defect criticality. Results acquired from this program were found in good accordance with those from the real-time Litho3 inspection, for both critical and non-critical layers of 90 nm design node. Such capability allows detailed study of defect criticality in relation to its size, defect optical transmittance, residing surface, its proximity to a printing pattern as well as lithography parameters such as NA and sigma. Furthermore, coupling this automatic program with high resolution inspection also assists in determining lithography process window and an in-depth comprehension of defect progression mechanism.

6730-81, Session 17

Paving the way to a full-chip gate-level double-patterning application

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Double patterning lithography processes can offer significant yield enhancement for challenging circuit designs. Many decomposition (i.e. the process of dividing the layout design into first and second exposures) techniques are possible, but the focus of this paper is on the use of a secondary “cut” mask to trim away extraneous features left from the first exposure. This approach has the advantage that each exposure only needs to support a subset of critical features (e.g. dense lines with the first exposure, isolated spaces with the second one). The extraneous features (“printing assist features” or PrAFs) are designed to support the process window of critical features much like the role of the sub-resolution assist features (SRAFs) in conventional processes. However, the printing nature of PrAFs leads to many more design options, and hence a greater process and decomposition parameter exploration space, than are available for SRAFs.

A decomposition scheme using PRAFs was developed for a gate level process. A critical driver of the work was to deliver improved across-chip linewidth variation (ACLV) performance versus an optimized single-exposure process while providing support for a larger range of critical features. A variety of PRAF techniques were investigated by simulation, with a PrAF scheme similar to standard SRAF rules being chosen as the optimal solution [1].

This paper discusses in its first part aspects of the code development for an automated PrAF generation and placement scheme and the subsequent decomposition of a layout into two mask levels. While PrAF placement and decomposition is straightforward for layouts with pitch and orientation restrictions, it becomes rather complex for unrestricted layout styles. Because this higher complexity yields more irregularly shaped PrAFs, mask making and inspection concerns become critical drivers of the optimum placement and clean-up strategies. Examples are given of how those challenges are met or can be successfully circumvented. During subsequent decomposition of the PrAF-enhanced layout into two independent mask levels, various geometric decomposition parameters have to be considered. As an example, the removal of PrAFs has to be guaranteed by a minimum required overlap of the cut mask opening past any PrAF edge. It is shown that process assumptions such as CD tolerances and overlay as well as inter-level relationship ground rules need to be considered to successfully optimize the final decomposition scheme.

This paper’s second part discusses simulation and experimental results regarding not only ACLV but also across-device linewidth variation (ADLV). Additionally, examples are given that show how complex two-dimensional layout configurations causing irregular PrAF and decomposition solutions could be successfully transferred to a manufacturing process with real life tolerances.

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6730-83, Session 17

Automatic SRAF placement optimization based on process-window variability reduction

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Placement rules for sub-resolution assist features (SRAF) needs to be optimized for maximizing the process window and CD control of the main feature as well as insuring the non-printability of the SRAFs across the process variation. Various factors including the illumination schemes, image contrast and also other edge and image based goals have been used for optimizing these placement rules. With the continuously shrinking technology nodes, the generation of these traditional rule-based SRAFs is becoming an expensive process in terms of time, cost and complexity.

In this paper, we propose using an automated model-based flow to obtain the ideal SRAF insertion rules, which reduces the time and effort required to achieve the best rules. In this automated flow, we optimize the SRAF placement by iteratively generating the SRAF rules and assessing their performance against process variability metrics. Different metrics are used in the flow. PVband (Process Variability band) thickness is a good indicator of the process window enhancement. Also, NILS (Normalized image log-slope) and DOF (Depth of focus) are highly descriptive metrics for gauging the effectiveness of the rules generated at each iteration.

6730-84, Session 17

Full-chip based assist features correction for mask manufacturing

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Sub Resolution Assist Features are now main option for enabling low-k photolithograpy. This technical challenges for the 45nm node, along with the insurmountable difficulties in EUV lithography, has driven the semiconductor mask-maker into the low-k lithography era under the pressure of ever decreasing feature sizes. Extending lithography towards lower K1 puts heavy demand on the resolution enhancement technique (RET), exposure tool. However, current mask making equipments and technologies are faced with its limits. Particularly, due to smaller feature size, the critical dimension (CD) linearity on both mask main cell patterns and Sub Resolution Assist Features (SRAFs) falls down. There are certain discrepancies of CD linearity line from ideal case. For example, as the CD size gets smaller, the bigger CD discrepancy will be. Therefore, to achieve better CD issues control, assist features correction is applied to improve photomask fabrication. In other words, in order to compensate this CD linearity, the sizing technology with SRAFs is applied in data process flow. In the field of mask data preparation flow, we strive to enhance SRAFs linearity by adding a new correction algorithm. In this paper, we will describe in detail the implement of our study and present results on a full 65nm node with experimental data.

6730-85, Session 17

Etch-proximity correction by model-based retargeting within integrated OPC flow

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Model-based Optical Proximity Correction (OPC) usually takes into consideration optical and resists process proximity effects. However, the etch bias proximity effect usually can not be completely eliminated by etch process optimization only and needs to be compensated for in OPC flow for several critical layers. Since the understanding of the etch pro-

cess effect is getting better and accurate etch bias modeling is available now, people starts to migrate from rule-based correction to model-based correction. Conventionally when etch bias is considered in model-based correction, optical/resist/etch effect is corrected in one step by using the input layout as the final etch target. In this paper, we proposed a new flow in which etch and optical/resist process effect are separated in both model calibration and layout correction. This double separation allows easier control over etch and resist target, resulting in drastic reduction of OPC runtime. In addition it enables post-OPC verification at both resist and etch level. Advantages of the new integrated model-based retarget/OPC flow in RET implementation will also be discussed.

6730-86, Session 17

Resolution enhancement by aerial image approximation with 2D-TCC

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A newly developed sub-resolution assist feature (SRAF) placement technique with two-dimensional transmission cross coefficient (2D-TCC) will be described in this paper. The SRAF placement concept with 2D-TCC is physically similar to that of the interference mapping lithography (IML) technique[1] but is based on different algorithm. IML sets SRAFs according to the interference map computed from singular value decomposition of four-dimensional TCC. On the other hand, SRAF generation with 2D-TCC is based on the approximated point spread function (PSF) of partially coherent imaging. More concretely, Hopkins equation with four-dimensional TCC[2] is decomposed into the sum of the Fourier transforms of the diffracted light weighted by decomposed 2D-TCC, introducing the convolution of mask layout and approximated PSF to create the approximated aerial image so as to place the SRAFs to a given mask layout. SRAFs are placed at the peak position of the approximated aerial image to enhance the resolution. Since the approximated aerial image depends on the illumination condition, the SRAFs can be automatically optimized to the given illumination condition to generate the optimized reticle, which differs from our previous work based on the rule-based SRAF placement[3]. As the approximated aerial image is based on the TCC computation, the effects of aberration and the polarization can be included. Furthermore, since four-dimensional TCC is decomposed into 2D-TCC, the computer memory can be reduced significantly, leading to fast calculation of the approximated aerial image. Therefore, one can use a large number of pupil sampling mesh to handle the aberration and polarization more precisely.

The validity of this technique has been confirmed by the contact hole exposure experiment performed by Canon FPA6000-ES6a, 248 nm with an NA of 0.86. Binary reticle optimized by this technique with mild off-axis illumination is used in this experiment and the 100 nm contacts (k1=0.35) including isolated and dense contacts have been successfully resolved with the aid of this technique (Fig. 1).

In the presentation, the basic theory, simulation results, the reticle optimization concept and experimental results will be explained in detail. The approximated aerial image has the negative intensity, which corresponds to the 180 degree phase shift; therefore, phase shifting mask can be generated with this technique. We will also discuss the reticle optimizing concept with phase shifting mask design. In addition, an experimental results by ArF exposure tool with an NA of 0.90 targeting 75 nm (k1=0.35) line pattern will be shown.

[1] R. Socha et al., “Contact Hole Reticle Optimization by Using Interference Mapping Lithography (IML(TM)),” Proc. SPIE 5377, 223-254 (2004).

[2] H. H. Hopkins, “On the diffraction theory of optical image,” Proc. Roy. Soc. A, 217, 408-432 (1953).

[3] K. Yamazoe et al., “Full-Chip implementation of IDEALSmile on 90-nm-Node Devices by ArF Lithography,” Jpn. J. App. Phys., 44, No. 7B 5526 -5534 (2005).

6730-181, Session 17

Slanted sub-resolution fill pattern to suppress the lens-heating-induced field distortion by the dipole illumination

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Certain reticle patterns with off-axis illumination have caused lens heating (LH) issues, i.e., the non-uniform light energy distribution within the scanner’s lens introduces lens deformation. As a result, this deformation causes image parameter drifts, such as critical dimension (CD) variation and overlay error within the scanning field. The LH effect is reticle pattern dependent and is also illumination dependent. It appears to be the most severe with the dipole-type illuminations (e.g., the Dipole-X 35o causes a serious LH issue for the 70nm node vertical line/space pattern), and the LH effect decreases with other specialized Cquad-100X30Y, Annular, and Cquad illuminations. LH does not seem to be problematic for the Quasar and conventional illuminations. In this paper, we propose a solution from the reticle perspective to reduce the LH effect for the most severe dipole illuminations. The solution is to introduce a slanted sub-resolution fill pattern in the reticle’s open area, if there is an open area, which will diffract the light energy distribution in the lens pupil from the dipole fashion to the four-pole Cquad fashion. Effectively, the averaged light concentration on the lens will balance the heat distribution throughout the lens and thereby reduce the LH effect within the scanning field. The proposed slanted sub-resolution fill pattern can be laid out in the line/space fashion oriented in 45o angle (i.e., diagonal) or other close angles, although the diagonal line/space is usually preferred to facilitate the mask manufacturing.

6730-87, Session 18

Exploring the sources of MEEF in contact SRAMs

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Optical Proximity Correction (OPC) relies on predictive modeling to achieve consistent wafer results. To that end, understanding all sources of variation is essential to the successful implementation of OPC. This paper focuses on challenging SRAM layouts of contacts to study the sources of wafer variation. A range of shape geometries and contact configurations are studied. Contact shapes are no longer restricted to simple rectangles on the mask, some more complex OPC outputs may include shapes like H’s or T’s or even more fragmented figures. The result is a large group of parameters that can be measured at both mask and wafer level. The dependence of mask variation on geometry is studied through the statistical distributions of parameter variations. The mask metrology output is expanded from traditional linear dimensional measurements to include area, line edge roughness, corner rounding, and shape-to-shape metrics. Wafer mask error enhancement factor (MEEF) is then calculated for the various contact geometries. This collection of data makes it possible to study variation on many levels and determine the underlying source of wafer variations so that, ultimately, they can be minimized.

6730-88, Session 18

The improvement of OPC accuracy and stability by the model parameters’ analysis and optimization

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The OPC model is very critical in the sub 45nm device because the Critical Dimension Uniformity (CDU) is so tight to meet the device performance and the process window latitude for the production level. The OPC model is generally composed of an optical model and a resist model. Each of them has physical terms to be calculated without any wafer data and empirical terms to be fitted with real wafer data to make the optical modeling and the resist modeling. Empirical terms are usually related to the OPC accuracy, but are likely to be overestimated with the wafer data and so those terms can deteriorate OPC stability in case of being overestimated by a small cost function.

Several physical terms have been used with ideal value in the optical property and even weren't be considered because those parameters didn't give a critical impact on the OPC accuracy, but these parameters become necessary to be applied to the OPC modeling at the low k1 process. Currently, real optic parameter instead of ideal optical parameter like the laser bandwidth, source map, pupil polarization including the phase and intensity difference start to be measured and those real measured value are used for the OPC modeling. These measured values can improve the model accuracy and stability. In the other hand these parameters can make the OPC model to overcorrect the process proximity errors without careful handling.

The laser bandwidth, source map, pupil polarization, and focus centering for the optical modeling are analyzed and the sample data weight scheme and resist model terms are investigated, too. The image blurring by actual laser bandwidth in the exposure system is modeled and the modeling result shows that the extraction of the 2D patterns is necessary to get a reasonable result due to the 2D patterns' measurement noise in the SEM. The source map data from the exposure machine shows lots of horizontal and vertical intensity difference and this phenomenon must come from the measurement noise because this huge intensity difference can't be caused by the scanner system with respect to the X-Y intensity difference specification in the scanner. Therefore this source map should be well organized for the OPC modeling and a manipulated source map improves the horizontal and vertical mask bias and even OPC convergence. The focus parameter which is critical for the process window OPC and ORC should be matched to the tilted Bossung plot which is caused by uncorrectable aberration to predict the CD change in the through focus with a new devised method. Pupil polarization data can be applied into the OPC modeling and this parameter is also used for the unpolarized source and the polarized source and specially this parameter helps Apodization loss to be 0 and is evaluated for the effect into the modeling.

With the analysis and optimization about the model parameters the robust model is achieved in the sub 45nm device node.

6730-90, Session 18

Customizing proximity correction for gate etch, contact etch, and resist reflow

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Fast, full-chip, model-based correction tailored specifically for etch and other processes is now available as a complete calibration, correction and verification flow. This approach, which is based on an algorithm fundamentally different from optical correction algorithms, has proven successful in fitting accurate models and correcting 45 nm data from IMEC[1] and from foundaries. This paper will discuss enhancements to this etch correction flow for specific frabrication processes, including resist trim for gate etch, contact etch and resist reflow for contacts. Advantages of the approach described here include:

1. process parameters as well as traditional CD-SEM measurements of etch bias and resist reflow skew are taken into account.

2. Additional physics-based calculations are done using the process data.

The result is improved accuracy and reduced effort spent in model building and correction tuning.

[1]Combining Resist and Etch modeling and Correction for the 45 nm node, M. Drapeau, D. Beale, Photomask 2006

6730-91, Session 18

Fast synthesis of topographic mask effects based on rigorous solutions

Q. Yan, Z. Deng, J. P. Shiely, Synopsys, Inc.

Topographic mask effects can no longer be ignored at technology nodes of 45 nm, 32 nm and beyond. As features become comparable to the mask topographic dimensions and the exposure wavelength, the popular thin mask model breaks down where the mask transmission no longer follows the layout. A reliable mask transmission function has to be derived from Maxwell equations. Unfortunately, rigorous solutions of Maxwell equations are only managible for limited field sizes, but impractical for full-chip optical proximity corrections (OPC) due to the prohibitive runtime. Approximation algorithms are in demand to achieve a balance between acceptable computation time and tolerable errors.

In this paper, a fast algorithm is proposed and demonstrated to model topographic mask effects for OPC applications. The ProGen Topographic Mask (POTOMAC) model synthesizes the mask transmission out of Maxwell solutions from the SOLID-E engine, an industry leading rigorous simulator of optical lithography. The integral framework presents a seamless solution to the end user. The prototype was applied to full fields of a 45 nm design. Preliminary results indicate the overhead by introducing POTOMAC is contained within the same order of magnitude in comparison to the thin mask approach. Fig.1 shows a local aerial image.

6730-186, Session 18

Simultaneous model-based main feature and SRAF optimization for 2D SRAF implementation to 32-nm critical layers

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Sub-resolution Assist Feature (SRAF) insertion is one of the most important Resolution Enhancement Techniques (RET) for the 65 nm, 45 nm nodes and beyond. In this paper, we are proposing a novel approach for the optimum placement of 2D SRAF structures using state of the art Calibre RET flow. In this approach, the optimal SRAF shapes are achieved simultaneously during the OPC step. The SRAF and Main features are optimized to account for their edge placement and process window metrics (aerial image slope/contrast, out of focus/dose EPE, etc...). The resulting mask shapes deliver some of the properties that can be obtained using the Inverse Lithography Techniques (ILT), such as excellent Process Window Performance, while there is almost no impact on the runtime. The implemented Model-based optimization flow remains compatible with the current OPC production flows. As shown on Figure 1. rules-based SRAF placement (yellow) provides limited process window. Simultaneously optimized SRAF and Main features (Red) widen the process window. (Dose ±10%, Focus ± 100 nm)

6730-92, Session 19

Improving hyper-NA OPC using targeted measurements for model parameter extraction

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Accurate OPC Models are critical for functioning silicon in sub-90nm processes. At 45nm, OPC model fitting uses thousands of metrology data points, therefore, a large effort is required in order to achieve physically accurate and stable model fits. Double Patterning will further exacerbate modeling difficulty because multiple models are required for each double patterned layer. Fortunately, new SEM measurement tools are enabling automation of extremely large measurement data sets for OPC model fitting.

Historically, every good data measurement is used for fitting every parameter in a model. This is inefficient when many metrology pattern types are used. Instead, only test patterns that have a high sensitivity to a model parameter should be included when fitting that parameter. By targeting specific test patterns to each model parameters, we can decrease the number of measurements that are fitted for each model parameter by an order of magnitude.

The first advantage of this method is that it decreases noise. When test patterns with low parameter sensitivity are used in a fit, their non-parameter related variations are included in the model fit. These unnecessary data points contribute noise that camouflages the actual effects of the model parameter. Removing such data points will allow the model parameters to be fit with higher precision.

The second advantage of this technique is faster time-to-results. Only data measurements that demonstrate a direct relation to the fitted parameter will be used. This can decrease the number of data measurements for each parameter fit by an order of magnitude, decreasing the number of variables used for each parameter fit. In addition, the decreased noise will allow model fitting tools to converge to the best fit

more efficiently.

This paper will present a baseline process flow for establishing parameter sensitivities for any OPC calibration test pattern. To demonstrate the process, trends will be calculated for multiple styles of test patterns in a 32nm logic patterning process. The test pattern parameter sensitivities will be compared to generate rules for which test pattern measurements should be used when fitting model parameters. Finally, the rules will be applied to sub-45-nm logic node measurement data. Two models will be fit to the data, one with the parameter sensitivity rules, and one without. The resulting models will be compared for quality of results, model stability and time to results.

6730-93, Session 19

Selective process aware OPC for memory device

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Many issues need to be overcome in creating a production-worthy sub-k1 (<0.25) process. The repeating photo-etch sequential method for clear and dark mask type is susceptible to overlay issues while accuracy of first pattern is critical for the space technology. Both technologies require improved model accuracy and process margin. Because of this, even traditionally non-critical regions of a layout may contain process margin-limiting defects for double patterning technology. An integrated OPC-Verification-Selective OPC procedure is developed to improve quality of results for non-critical regions while retaining fast TAT. The first step utilizes a fast OPC method with reduced TAT. Next, a lithographic verification tool is used to perform a thorough check of the OPC results, including process window analysis. This determines which points limit process margin. Finally, advanced OPC methods are applied to reprocess the areas limiting process margin. These advanced OPC techniques may include broader lithographic analysis, field-based correction and process window consideration. Since advanced OPC methods are only applied to part of the design, TAT is fast. TAT can be further improved by treating critical regions differently. Critical regions will not be processed in the initial OPC or intermediate verification steps, but will be corrected by the advanced OPC methods. This methodology is called Incremental OPC as it applies the most appropriate OPC techniques to each area of the design. As a result, process margin limiting defects, side-lobe printing and sub-resolution assist feature printing can be eliminated prior to mask tape-out with minimal impact to TAT. In this paper, Incremental OPC is compared to “all-or-nothing” OPC techniques which must be applied across an entire pattern.

6730-94, Session 19

Validating optical proximity correction

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Complex Optical Proximity Correction (OPC) must be deployed to meet advanced lithography requirements. The OPC models are used to convert input design shapes into mask data that often deviate significantly from both the initial design and the final wafer image in resist. The process includes selective shape biasing, applying pattern-specific corrections, and modeling the effect at multiple exposure conditions. It is important to verify the results of the OPC model and this is done by invoking OPC verification programs. The verification models identify points of failure to specific criteria. For example, failure points can be defined to capture the transition to feature sizes smaller or larger than 10% of target. Since these models are built for use in OPC verification, they may only be well-calibrated at feature sizes near target. This can introduce uncertainties in the failure predictions. This paper will explore options for validating the OPC verification models and methods. While wafer prints are an obvious source of feedback on the simulated results, there are also options at mask level. In this paper, we study the effect of programmed defects at wafer level, mask level and through a process window OPC verification method. For each test case, five points in the process window space are chosen to provide comparison data between OPC verification measurements, mask-level Aerial Image Microscope System (AIMS) and wafer measurement of patterned photoresist. The results permit correlation to measurable metrics and provide an improved understanding of OPC verification validity.

6730-95, Session 19

The study of phase-angle and transmission specifications of 6% att-EAPSM for 90-nm, 65-nm, and 45-nm nodes wafer manufacturing patterning process

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Attenuated embedded PSM (Att-EAPSM) has been widely used in semiconductor wafer manufacturing at 90nm, 65nm and 45nm nodes. To maximize the potential att-EAPSM manufacturing yields and reduce associated mask production costs, it is important for the industry to develop a comprehensive mask specification that can fully meet the wafer level lithography requirements without over-constraining the control parameters in the att-EAPSM manufacturing process. Although the CD and registration specifications of an att-EAPSM can be easily derived based on the MEEF (mask-error effect) of the lithography process and the required wafer level CD and OL control, the phase-angle and transmission specifications of an att-EAPSM are rather complicated since they did not have a direct correlation to the wafer level CD and OL performances. The current industry practice is to use the scaling factor to reduce the phase-angle and transmission tolerance of an att-EAPSM the same way as CD and registration when the wafer process node advances from 90nm to 65nm and 45nm.

Previously, we have fabricated a multi-phase 6% att-EAPSM mask and used the mask to study the effect of phase-angle and transmission errors to wafer lithography printing process at 90nm node. We experimentally established a direct correlation between the phase-angle error (out of 180 degree) and wafer best-exposure focus shift on an ASML 1/1200 based 90nm process 1. In this paper, we will use photolithography aerial-image simulation software to study the phase-angle error and best-exposure focus shift at 90nm, 65nm and 45nm lithography process conditions. To account for mask re-clean caused absorption loss, we will also study the interaction of transmission change to phase-angle error induced best-exposure shift. We will also describe our methodology of using aerial-image distribution to derive the best-exposure focus, and study the impact of phase-angle and transmission to photolithography process at various technology nodes. Contrary to common wisdom, our study reveals that as the photolithography process moves from 90nm to 45nm node, (the NA increases from 0.67 to 1.20), the same amount of phase-angle error results in less amount of best-exposure focus shift. In addition, the mask re-clean caused absorption losses can worsen the best-exposure focus shift caused by the same amount of phase-angle error. Based on these computer simulation results and previous wafer printing verification work, we will propose a phase-angle and transmission specifications of 6% att-EAPSM masks for semiconductor wafer manufacturing at 90nm, 65nm and 45nm nodes.

Reference:

1. Phase errors in PSMs at the 90nm Node. G. Chen, G. Hughes, W. Chou, S.M. Yen. Semiconductor International Vol.27, No. 10, 56-59, September, 2004.

6730-96, Session 19

Better on wafer performance and mask manufacturability of contacts with no or non-traditional serifs

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In the course of using Optical Proximity Correction (OPC) to optimize contact printing, the obvious solution is not always the correct solution. This paper will explore two different types of contacts, with two different sets of objectives. In the first type of contact, the objective is to achieve area uniformity over minimizing edge placement error at a finite set of locations on the edges. The contacts are all drawn at the same time. For these contacts, use of contacts without serifs over contacts with traditional corner serifs, will not only result in a mask that has a lower volume

data input to the mask writer, as well as an easier time in inspection and repair, but also on the wafer it will result in a tighter distribution of contacts in both area and CD, as well a larger process window over contacts with serifs. In second type of contact, there are additional complicating factors over the first type of contact in that there are different sizes of contacts that must be printed simultaneously. As contacts get pushed close together on corner to corner type spacing, traditional serifs will be more likely to drive mask inspection issues and high mask error enhancement factor (meef). One way to address this is with OPC that employs inverse serifs, with the center fragment of the rectangle pushed out and the corners pushed in. This approach reduces meef and provides better image parameters for lower variability through process window. However, this solution does not lend itself to very aggressive correction to achieve aggressive contact aspect ratios. We compare these two OPC strategies and describe the strengths and weaknesses of each approach. Finally the type of simulation that is done to calculate the metrics is also considered, as the industry transitions from sparse calculations to pixel based calculations. The differences in these simulation techniques are also explored.

6730-97, Session 19

Optimization of OPC runtime using efficient optical simulation

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Model based Optical Proximity Correction can be found in nearly all Resolution Enhancement recipes used in leading technology integrated circuits fabrication facilities. The industry is relying more and more on MBOPC to compensate optical effects that are induced during exposure of lithography masks. These masks have features of dimensions less than the exposure wave length which result in light diffraction effects distorting the image projected on wafer, however important is the MBOPC step, it is usually the highest computational time contributor to the total RET flow runtime.

MBOPC procedures include segmentation of layout edges into a number of fragments that can be manipulated by the software engine to improve the image transferred to wafer. In sparse MBOPC approach each fragment receives one or more optical simulation site. The simulation site is a one dimensional array of points where intensity of light is sampled and calculated. For each simulation site, the number of points has to be enough to ensure extension of the site to a certain distance from the fragment in order to correctly capture the resist behavior at this location, adding more points beyond this distance will not add any benefit but can significantly increase the runtime.

In this paper we present an automated method to analyze layouts for different technology nodes that depend on sparse simulations as their MBOPC engine, and to report the optimized number of simulation points that need to be in the simulation site in order to get the desired accuracy and optimum runtime performance.

6730-98, Session 19

Full-chip process window OPC capability assessment

P. J. M. VanAdrichem, Synopsys, Inc.

In the past technology generations, Optical Proximity Correction (OPC) has been applied using a model capturing the Optical proximity effects in a single focal plane. In the newer generations, this method is more and more difficult to maintain because of very small process windows in specific situations. These specific situations include 1D configurations (e.g. isolated small lines) but increasingly complex 2D configurations.

In the more advanced technology nodes 2D configuration are starting to play a much bigger role. Process windows need to be preserved in all cases, and so this brings about another challenge for the OPC flow. The more traditional OPC approaches may result in un-acceptable small process window in such cases, whereas well characterized Process Window OPC (PW-OPC) can provide better results, with much less engineering interventions.

In this paper methods of Process Window OPC are applied on a bigger scale and large scale (full chip) verifications and assessments are demonstrated and compared with alternatives. In the past OPC engineers have been pushing for more and more design constrains in order to allow the OPC flow to be successful. The PW-OPC approach is more adaptive compared with traditional single focal plane OPC, and can still converge to an acceptable solution in complicated (unforeseen) layout configurations, without the need to introduce complicated design constraints.

6730-100, Session 20

EBDW is free

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It is widely understood that at a lithography capacity of a few critical wafer-levels per hour, e-beam direct write (EBDW) would have a significant impact on semiconductor business models. Despite the fact that EBDW has been a “technology of the future” for 40 years-it was mentioned as such in Gordon Moore’s first paper on Moore’s Law-the challenges and costs of multi-patterning and EUV lithography have given new impetus to EBDW efforts.

In this paper we point out that even at 1 wafer-level per hour, there are economically interesting cases where EBDW is advantageous for surprisingly large chip runs, on the order of million die. The controlling factors are chip size, design cost, and, of course, reticle cost. For small ASICs, a few square mm’s, with relatively inexpensive design cost, the number of wafers needed to satisfy the minimum economic market is fewer than 100 wafers while the breakeven for EBDW vs Mask is closer to 200 wafers. The business that resides in this gap becomes unlocked by EBDW lithography. In this paper we examine the doubly-constrained economically advantageous EBDW set: that is those cases where there are enough wafers to pay for the design costs yet few enough wafers that mask costs are disadvantaged.

For small chips, over a million die can be manufactured in production runs of 200 wafers or less. Ironically, it is the high-profile designs with large area and 10’s of millions of dollars in design costs that drive the development of lithographic systems that all products must use. These high profile designs are least suitable for EBDW for the total return needed to obtain acceptable ROI on the high fixed cost of design is immense.

However, even in cases where volume production is best performed with Masks, it can often make sense to start the production ramp with critical layers done with EBDW. The reason for this harks back to a strategy used by Dell, in the early days when it was a small company, to compete with IBM and other established PC makers. By focusing on cycle time and build-to-order efficiencies, Dell was able to take advantage of the steep decline in chip prices. Dell realized lower effective costs than their larger competitors by taking advantage of the quickly declining chip prices by buying “just in time.”

It turns out that the numbers and strategy work out similarly for reticles today. Advanced reticle prices can drop 30% per year in the early days of a technology node. By using EBDW to produce the early part of a product ramp, especially during product qualification, one can potentially delay the time when expensive reticles are required. The reticle price drop that can occur during this delay, which can exceed a million dollars for the critical mask levels, can more than pay for the costs of EBDW. (Note that there are limitations to this for product qualification since the idiosyncrasies of the optical litho process would not be qualified in this scenario.)

Thus the potential economically advantageous range of EBDW applications include prototyping, product derivatives (low design cost), qualification (with the limitation discussed), volume production of small die (with low design cost and few wafers), and early product ramp (to delay, and thereby reduce the cost of, the critical reticles).

6730-101, Session 20

Driving photomask supplier quality through automation

D. R. Russell, A. P. Espenscheid, Freescale Semiconductor, Inc.

In 2005, Freescale Semiconductor’s newly centralized mask data prep organization (MSO) initiated a project to develop an automated global

quality validation system for photomasks delivered to Freescale's fabs. The system handles Certificate of Conformance quality metric collection, validation, reporting and an alert system for all photomasks shipped to Freescale fabs from all qualified global suppliers. The completed system automatically collects 30+ quality metrics for each photomask shipped. Other quality metrics are generated from the collected data and quality metric conformance is automatically validated to specifications or control limits with failure alerts emailed to fab photomask and mask data prep engineering. A quality data warehouse stores the data for future analysis, which is performed quarterly. The improved access to data provided by the system has improved Freescale's ability to spot trends and opportunities for improvement with our supplier's processes. This paper will review each phase of the project, current system capabilities and quality system benefits for both our photomask suppliers and Freescale.

6730-102, Session 20

Multi-layer reticle (MLR) strategy application to double-patterning/double-exposure for better overlay error control and mask cost reduction

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As the lithography process node moves to HP-32nm and below, it becomes very difficult to print the original design onto a wafer even if various lithography techniques like OPC, use of immersion Scanner, Phase Shift mask, etc are all applied. The most frequent use of the light wavelength for the advanced lithography is ArF (193nm) with a liquid immersion exposure system but still many lithography challenges exist. One of the techniques that the industry has become interested in is the Double Patterning Technique (DPT) or the Double Exposure Technique, where a one-layer design (or layout) is split into two(2) or more than two(2) patterns so that the narrowest pitch for the original design is relaxed. The split patterns are printed separately to two(2) or more than two(2) photomasks (reticles). Each pattern is exposed separately onto a wafer, effectively combining the previously-split patterns on the wafer.

This technique is believed to be a solution in order to establish the 32nm and below process node until EUV lithography infrastructure is ready.

However, the big challenge with this technique is the overlay budget along with critical dimension (CD) control. Use of multiple masks(reticles) to form a original design(layout) while maintaining tight CD and registration control on the wafer is very difficult with today's manufacturing specifications. The overlay budget is associated with equipment accuracy, mask-to-mask accuracy and how the pattern is split.

In this paper, we propose that instead of using multiple masks(reticles) for the DPT(STD DPT), multiple split patterns are printed on a single mask(reticle) so that each pattern is separately or simultaneously exposed onto a wafer in order to reduce the mask-to-mask overlay error. This can also reduce the mask cost and mask manufacturing time compared with STD DPT, at the expense of reducing manufacturing throughput.

We propose two ideas about how to place the split patterns in a single mask(reticle) and simulate corresponding shot yield comparisons. Cadence's MaskCompose™ was used for simulating the wafer shot counts.

The results show that by using Multi Layer Reticle(MLR) strategy for splitting the original layout into 2 split patterns onto a single mask(Method(1)), we can get the following advantages: 1) eliminate mask-to-mask overlay error factor 2) single mask (hence reducing mask cost). The disadvantage to this strategy is that the wafer shot throughput is 50% of that achieved by STD DPT. The results also show that by using our new approach of placing multiple-split patterns to form the array within the mask scribe(Method(2)) we achieve the following advantages: 1) eliminate mask-to-mask overlay error factor 2) single mask (hence reducing mask cost) and 3) drastically improved wafer shot throughput (roughly 90% of the STD DPT, 180% of Method(1)). The disadvantage of our new approach is that Method(2) requires that die array have an even number of die in either the x or the y axis.

Finally, we mention a little about the possibility of a Triple Patterning Technique for shot maps with Method(2) with the die array being either a combination of [multiple of three] by [X], or [X] by [multiple of three].

6730-103, Session 21

Advanced mask process compensation for 45-nm node and beyond

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In recent years, critical dimension (CD) control became increasingly important in mask making process. The ITRS roadmap shows the mask CD requirements exceeding those of the wafer side with the 45nm node going forward. Specifically, CD linearity and CD uniformity specifications are getting tighter as the technology node becomes smaller. In this presentation, a novel mask process compensation (MPC) method that consists of an OPC-type approach to compensate mask proximity and other effects is used for improving CD linearity in the mask. The computational models for e-beam lithography and etch process are calibrated using CD measurements from several test masks written and processed. The computational model consists of terms to model pattern density effects and phenomenological plasma etch effects. Short-range (or equivalently proximity) correction is carried out using the computational models calibrated. We present the results of the model verification using SEM images and the results of the short-range correction. 65nm process tools were used for this work. The mask writing errors, i.e. final inspection CD minus incoming design CD, for line and space patterns (with values of 60nm-1600nm) without MPC has a range 3.4X larger then the one with MPC. The mask writing errors for square hole and dot patterns (with values of 80nm-1600nm) with MPC has a range improvement of 1.7X. In summary, a novel mask process compensation method is developed that shows significantly improved mask writing errors. Moreover, using current process tools combined with MPC, it is feasible to stretch the existing equipment platform to meet the specifications for at least another future technology node.

6730-104, Session 21

Improvement of mask CD uniformity for below 45-nm node technology

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In a mask process, pattern density, layout and process-induced CD trend are the most important factors affecting mask CD uniformity. Much more efforts have been taken to analyze and correct this kind of CD errors but solutions have not been clearly suggested. The function for phenomena of pattern density like fogging and loading effect have been supported by electron beam machine on the other hand, the process-induced errors which is not the function of pattern density have been corrected with the type of fixed and discrete map. But for various pattern densities containing long, short, even middle ranges, process-induced CD error is not stationary on each pattern density, that is, the function for process-induced CD error should be changed according to each density layout. In this paper, the case of varying process CD error is introduced and the relationship between pattern densities and process-induced CD error also discussed. And effective correction method for less-separated CD error into pattern density component and process-induced component is proposed at the conclusion.

6730-105, Session 21

Correction technique of EBM-6000 prepared for EUV mask writing

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EUV lithography is the promising candidate for 32nm generation and beyond.

EUV exposure system needs to be operated under vacuum condition to

avoid weakening exposure light. Reflective optics is necessary for EUV exposure system due to the lack of lens materials that would not absorb EUV light. Electro-static chuck, ESC, is going to be used to hold mask in the vacuum of EUV scanner.

When a mask is held by ESC, additional image placement error from two error sources will be unavoidable; error induced by non-telecentricity and another error induced by mask distortion. EUV light is obliquely injected onto the mask and reflected at the angle of six degrees. Therefore, the error induced by non-telecentricity mainly comes from variations of surface conditions of reflective plane caused by mask non-flatness, mask thickness variations, and surface roughness of ESC. Another error induced by blank deformation comes from film stress and chucking.

Image placement errors of the mask caused by ESC should be studied to increase confidence level to use ESC, because no metrology tool for EUV mask with ESC is available. Vacuum chuck of LMS-IPRO2 has also been prepared for testing purpose to understand the grid distortion on the flat chuck. However, firm conditions to obtain desirable image placement repeatability have not been found as yet.

Nevertheless, early access to EB writer should be helpful for mask development of 32nm generation mask. NuFlare Technology, Inc. has developed the correction methodology, OBBTC, due to obtain image placement on the simulated grid such as an ideal flat plane in pattern writing. Using OBBTC, each blank can be corrected in accordance with the blank backside topography. This correction technique also enables to compensate for not only blank deformation induced by the blank backside topography but also blank thickness variation and ESC surface roughness. We will report this optional methodology of additional grid correction for EBM-6000 to write EUV mask in this paper.

6730-106, Session 21

Coping with double-patterning/exposure lithography by EB mask writer EBM-6000

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Double exposure / Double pattering methodologies are being adopted to extend 193nm optical lithography until the next generation lithography, most likely the EUV, is solidified. The Double exposure / Double patterning methodologies require tighter image-placement accuracy and Critical Dimension (CD) controls on a mask than the conventional single exposure technique.

NuFlare Technology's mask writer, EBM-6000, is capable of achieving the required CD control and high patterning resolution as fine as 35 nm, that are required for the hp 45nm lithography with Double exposure / Double patterning methodologies, when newly developed resist (i.e. "low-sensitivity" resist) is used, as shown at several occasions to date. Further, image-placement control with EBM-6000 has been improved based on extensive error budget analysis to comply with the tight image-placement specifications required by the Double exposure / Double Patterning lithography.

This paper will show the results of the analysis and improvement of the image-placement accuracy of EBM-6000 series mask writers.

6730-107, Session 21

Performance comparison of techniques for intra-field CD control improvement

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Intra-field CD variation is a main contributor to the total CD variation budget in IC manufacturing. It is caused by various sources, such as imperfections of the scanner projection system, intra-field defocus and mask CD errors. In advanced memory device manufacturing the printed minimum features have sizes close to the resolution limit of the projection system resulting in a large mask error enhancement factor. To fulfill the requested CD control specifications an extremely tight mask features size control is required, which results in a significant enlargement of the mask costs and hence large litho process costs. As a consequence lithographers are searching for appropriate techniques [1] - [3], which allow to reduce the impact of systematical contributions to the intra-field CD variation budget at reasonable costs.

Intention of the paper is to compare two major techniques of intra-field CD control improvement: a scanner based technique, and a novel technique based on mask blank transmittance control (CDC - CD Control). Main criteria for this analysis are CD uniformity improvement potential and correction accuracy. But also influences of these techniques on various lithographic performance parameters will be investigated. Furthermore the quality of the two main correction options, i.e. mask and wafer data based correction will be compared. The pro's and con's of the correction approaches, specifically their implementation efforts and their stability will be discussed.

Figure 1 shows a comparison of the intra-field CD uniformity before and after applying the discussed correction techniques. In both cases an improvement of the CD uniformity has been achieved.

[1] J. van Schoot et.al.: CD uniformity improvement by active scanner corrections, Proc. SPIE Vol. 4691, p.304-314 (2002).

[2] E. Zait et.al.: "CD Variations Correction by Local Transmission Control of Photomasks done with a Novel Laser based Process", SPIE Proc. 6152-76 (Feb. 2006).

[3] J. R. Park et.al.: Improvement of shot uniformity on wafer by controlling backside transmittance distribution of a photomask. Proc. SPIE Vol. 5040, p. 553-559 (2004).

6730-108, Session 21

Projection maskless patterning (PMLP) for the fabrication of leading-edge complex masks and nano-imprint templates

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The reliable and cost-effective fabrication of 2D and 3D structured nanosurfaces is prerequisite for a number of industrial and emerging applications: (i) leading edge complex masks, (ii) high precision nanoimprint templates, and (iii) nano-functionalised surfaces and 3-D structures for applications in nano-photonics, nano-magnetics, and nano-biotechnology. Projection Mask-Less Patterning (PMLP) is based on many hundred thousands of ion beams (H+, He+, Ar+, C60- or cluster ions) working in parallel. With PMLP technology 2D and 3D design data can be transferred directly into almost any material surface of a substrate without using resist. A PMLP proof-of-concept tool has been realized as part of the European project CHARPAN (Charged Particle Nanotech, www.charpan.com). A programmable aperture plate provides 40,000 beams as a first step to demonstrate the performance of the PMLP technology. The novel ion beam projection optics with 200x reduction already shows 16nm halfpitch resolution. The next phase PMLP Prototype Tool is targeted to more than 900,000 programmable beams with < 10nm resolution capability providing <10h realization time for 22nm node leading edge complex masks and <1h for nanoimprint templates. Thus PMLP provides a significant advantage to a high value-added mask and template fabrication and to emerging nano-manufacturing industries. PMLP principles will be explained and proof-of-concept tool results will be presented.

6730-109, Session 21

Improving the CD linearity and proximity performance of photomasks written on the Sigma7500-II DUV laser writer through embedded OPC

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Optical proximity correction (OPC) is widely used in wafer lithography to produce a printed image that best matches the design intent while opti-

mizing CD control. OPC software applies corrections to the mask pattern data, but in general it does not compensate for the mask writer and mask process characteristics. The Sigma7500-II deep-UV laser mask writer projects the image of a programmable spatial light modulator (SLM) using partially coherent optics similar to wafer steppers, and the optical proximity effects of the mask writer are in principle correctable with established OPC methods.

To enhance mask patterning, an embedded OPC function, LinearityEqualizer™, has been developed for the Sigma7500-II that is transparent to the user and which does not degrade mask throughput. It employs a Calibre™ rule-based OPC engine from Mentor Graphics, selected for the computational speed necessary for mask run-time execution. A multi-node cluster computer applies optimized table-based CD corrections to polygonized pattern data that is then fractured into an internal writer format for subsequent data processing. This embedded proximity correction flattens the linearity behavior for all linewidths and pitches, which targets to improve the CD uniformity on production photomasks.

Printing results show that the CD linearity is reduced to below 5 nm for linewidths down to 200 nm, both for clear and dark and for isolated and dense features, and that sub-resolution assist features (SRAF) are reliably printed down to 120 nm. This reduction of proximity effects for main mask features and the extension of the practical resolution for SRAFs expands the application space of DUV laser mask writing.

6730-110, Session 21

Contrast properties of spatial light modulators for microlithography

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Spatial light modulators based on tilt-type micromirror arrays (MMAs) have become a viable solution for lithography applications as programmable masks. Essential features of MMA elements are their high-speed operation, deep-UV capabilities (reflection principle), and the continuous deflection of each micromirror. Especially the latter point - analog control of each micromirror - permits the fine positioning of image features well below the projected pixel size of the rasterized, programmable mask, and can be used furthermore for mask resolution enhancement techniques to meet key requirements of microlithography.

The diffractive working principle of MMA elements, where a programmable surface structure (diffractive phase modulation) converts to a defined intensity pattern within the optical system by means of a filter of spatial frequencies, therefore becomes one of the essential points to be considered for the accurate design and simulation of applicable MMA structures.

The present study introduces steps for a realistic simulation of optical MMA properties based on different stages of diffraction analysis. While several aspects of optical mask properties like line-edge roughness or CD-uniformity might be of interest, the article focuses on global contrast properties as an elementary base for further MMA consideration. Central point will be a discussion of effects that determine the global MMA contrast and how to introduce them into simulation. Comparison is made with experimental data to validate the theoretical assumptions.

6730-111, Session 22

Accuracy of mask pattern contour extraction with fine pixel SEM images

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The specification of photomask patterns is defined for each semiconductor device technology node based on the ITRS (International Technology Roadmap for Semiconductors). The quality of the photomask patterns has been managed by using a metrology tool for critical dimension (CD) and an inspection tool for pattern shape. According to shrinkage of semiconductor device patterns, the lithography margin has gradually become smaller. Consequently, the quality of photomask patterns has been managed by observing small lithography margin patterns in addition to the conventional quality management patterns with the conventional metrology tool. Furthermore, recently, as each successive device generation has become shorter, rapid improvement of not only turnaround time of photomask manufacturing but also yield of semiconductor device manufacturing has become necessary. Therefore, the importance of the flexible mask specifications concept is increasing.

The quality of photomask patterns with respect to the specifications are judged in terms of pass/fail based on the allowable lithography margin. The methodology is that small lithography margin patterns are selected, micrographs of the selected photomask patterns are acquired by a metrology tool, photomask pattern contours are extracted with the micrographs, resist patterns exposed on Si wafer are simulated by using the photomask pattern contours with lithography simulation under actual exposure conditions, the lithography margin is calculated and the quality of the photomask is judged in terms of pass/fail criteria based on the lithography margin for each generation, device and layer.

For management of the quality of photomask patterns based on the flexible mask specifications, it is necessary to measure two-dimensional patterns such as hot-spot patterns for each critical layer in devices having small lithography margin. Therefore, in order to manage quality in the case of flexible mask specifications, a two-dimensional photomask pattern contour extraction tool was studied and developed. The photomask pattern contour extraction tool realizes the combination of acquisition of fine-pixel SEM images of the photomask patterns in wide field and extraction of photomask pattern contours by using the acquired fine-pixel SEM images.

There have been many reports on the repeatability and reliability of CD and two-dimensional pattern metrology tools based on the conventional specifications. However, there are very few reports on the repeatability and reliability of photomask pattern metrology tools based on flexible mask specifications. In this report, using small lithography margin patterns, firstly, the fine-pixel SEM images of photomask patterns are acquired.

Secondly, contours of the photomask patterns are extracted with the SEM images. Thirdly, contours of resist patterns on Si wafer are simulated with lithography simulation under actual exposure condition by using the actual photomask pattern contours. Finally, the lithography margin is calculated by using focus exposure matrix for the simulated contours of resist patterns.

This flow is repeated. The lithography margin with this flow is compared with that of actual exposed wafers. Repeatability and reliability of the lithography margin is evaluated. As a result, accuracy of the photomask pattern contour extraction tool is discussed.

6730-112, Session 22

Two-dimensional measurement using CD SEM for arbitrarily shaped patterns

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As the design rule of lithography becomes smaller, accuracy and precision in Critical Dimension (CD) and controllability of pattern-shape are required in semiconductor production. Critical Dimension Scanning Electron Microscope (CD SEM) is an essential tool to confirm the quality of a mask such as CD control, CD uniformity and CD mean to target (MTT).

Basically, the quality of a mask is determined by the degree of equality with design data, i.e. pattern shape and CD target of the mask should be the same as those of the design. Various proposals of Resolution Enhancement Technology (RET), however, were made and applied to the recent mask technology. With the RET know-how being developed, the mask pattern shape is getting complicated due to the deformed, shrunk and rounded patterns.

In case of extremely narrow region of arbitrarily shaped patterns, the measured CD can be easily fluctuated depending on Region of Interest (ROI) in a rounded area. It is very difficult to define real error budget and MTT of masks using the conventional CD SEM systems which are based on 1-dimensonal (1D) measurement algorithm. To overcome this difficulty, it is needed to analyze the CD with a 2-dimensonal (2D) method and interpret 2D data into 1D format.

The conventional CD SEM systems supply area measurement function only for simple contact and dot patterns, but cannot support 2D function for complex and arbitrarily shaped patterns. In order to get 2D data of arbitrarily shaped patterns, we have shared ideas and concepts with system manufacturers. As a result, we construct a system that can measure the area of arbitrarily shaped patterns, and evaluate a method to analyze 2D data from the 1D point of view.

This paper summarizes the evaluation results that compare error budget between 1D and 2D data using CD SEM and other optical metrology systems.

6730-113, Session 23

Resist CD metrology and profile characterization using CD SEM technology

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Inline CD SEM resist metrology provides critical information for module based mask process control. The challenges to provide reliable and consistent resist metrology in production environment is partially due to the facts that resist CDs have more profile variations and surface roughness. To make situation worse, concern of the resist shrinkage has limited beam energy use for CD SEM imaging. As a result, resist SEM images usually have relatively lower signal to noise ratio, and higher measurement uncertainty compared to chrome CD measurements. In this paper, we will quantify the measurement uncertainty for various resist features and resist types, and identify methods for improvements.

CD SEM measurement is fundamentally two dimensional images of three dimensional features. Thus, the SEM imaging sensitivity to resist profile variation is the first step toward understanding of the resist measurement uncertainty. This paper will study methods to differentiate the noise sensitivity from feature sensitivity and develop key indicators to identify the correlation between the resist profile and the CD SEM measurements.

CD SEM measurement involves many trade-offs, such as resolution vs. throughput, resist shrinkage vs. image contrast, and repeatability vs. sensitivity, etc. Understanding and quantifying their impact is the next step to improve the measurement uncertainty. This paper will evaluate these trade-offs and their impact on measurement uncertainty. This will also help to establish the methods to control the measurement uncertainty.

Even though there have been some studies on CD SEM characterization, but most of them are limited to chrome CD condition. Extending the CD SEM characterization in resist mode can be challenging, as well as rewarding, since the resist mode measurements can provide better inline monitoring of process modules and provide valuable early feedbacks. The measurement uncertainty in resist mode plays key role in process control.

6730-114, Session 23

Preliminary verifiability of the aerial image measurement tool over photolithography process

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The AIMS fab 193i (Aerial Image Measurement Tool) measures approximate aerial images to scanner results by adjusting the numerical aperture, illumination type and partial parameters. Accordingly, AIMS tool is used generally to verify the issue points during manufacturing a mask. Normally using a mask for photolithography needs two verifications. One is the qualification in the mask shop. The other is verification over the photo process using the mask in the wafer fab. If evaluated data at AIMS can be trusted about photo process ability including energy latitude (EL), depth of focus (DOF), CD uniformity (CDU), pattern fidelity and mask defects including repair area, AIMS can function as a first filter before shipping the mask. That means the AIMS data can be used as a preliminary data in the wafer fab.

So this study is focused on correlation between measured data at AIMS fab 193i and ArF scanner over the photo process such as EL, DOF, CDU, pattern fidelity and mask defects. First, various patterns are made on attenuated PSM at 80 and 65nm tech. Next correlations are calculated about EL, DOF and CDU by using same optical conditions, measurement points and etc at AIMS and Scanner. Also the aerial image from AIMS is compared with scanner results on defective side how those are matched with each other.

Consequently calculated DOF, EL margin and CDU map at AIMS have similar trend with the scanner. In CDU point of view, AIMS exceeds the predictive ability of the mask CD SEM. Moreover it means that wafer CDU can be corrected independently on the CDU result of the wafer fab by using CDU correctable femto laser tool which reduces transmittance of the mask. Surprisingly, it is possible. And Aerial image about mask defects including repair area is useful to predict the problem of the mask, since it is similar to wafer results. But aerial image compared with wafer image has more difference at 65nm technology node than at 80nm. If adjustment of threshold or measuring method can be done, prediction of the scanner result will have no matter. In conclusion, predictive results at AIMS over photo process can be applied as a preliminary data and it can be used to another index verifying the mask quality.

6730-115, Session 23

Calibration of contact areas: the influence of corner rounding

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The precise reporting of critical dimension (CD) features on photolithographic masks is an essential part of the mask production process. A wide range of external (standardization by national institutes) and internal (standardization within mask houses to match different tools) methods has been set up to ensure calibration consistency for the simple one dimensional case. One of the current developments is to expand these concepts to area measurements. This is to achieve better reproducibility of CD tools and to achieve a better characterization of contacts with respect to their imaging behaviour in wafer scanners. Here, we report some very fundamental constrains of this approach that have to be taken into account regardless of the actual measurement strategy. The major result is that for two dimensional contacts the shape has to be considered. This is due to the fact that the usually constant offset for calibration of critical dimensions in one dimension is no longer a constant but depends on the absolute size of the contact and the value of the corner rounding. For standard values of 200 nm contacts with corner rounding of 75 nm and calibration offsets around 20 nm maximum systematic differences of about 2nm will be obtained. Given the fact that even 40 nm calibration differences for photomask standards can be observed even for national institutes, these systematic errors can be easily as large as 6 nm for 200 nm structures. This systematic error clearly exceeds the road map targets for critical dimension off-target specifications for the coming technology node. This statement is even emphasized by the fact that in future contact layer specifications will be smaller than for lines/space layers. Once tool independent characterization of contact areas has to be achieved, area measurement in each mask house needs a second thought to implement these systematic constrains. Here, we show that the additional measurement of the corner rounding ís a relatively easy method to accomplish this.

6730-116, Session 23

Measurements of corner rounding in 2D contact holes on phase-shift masks using broadband reflectance and transmittance spectra in conjunction with RCWA

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For the first time, Rigorous Coupled-Wave Analysis (RCWA) is used for the analysis of both polarized broadband reflectance and transmittance spectra with the purpose of measuring the degree of corner rounding in

2D contact holes. The use of transmittance spectra proves to be advantageous for the characterization of the shape of the contact holes. In contrast with the conventional reflectance-only techniques, transmittance measurements prove to be more sensitive to the angstrom-level variations in the shape of the contact hole. Therefore, the new technique is capable of accurately determining the degree of rounding of the contact hole corners and characterizing a variety of shapes - from perfectly round to perfectly square. Additionally, the high intensity of the transmitted spectra improves the signal-to-noise ratio and guarantees better repeatability of the results. Finally, an off-axis incident angle for the broadband spectra is used to ensure that the two polarizations of reflectance and transmittance are distinct from one another, thus addressing a shortcoming of analyzing symmetric 2D structures with normal incident light.

For the current study, 2D arrays of contact holes of various pitches are measuresd on an After Clean Inspection (ACI) phase-shift mask, using a spectrophotometer-based instrument capable of collecting four continuous spectra during one measurement - two polarized reflectance spectra (Rs and Rp) and two polarized transmittance spectra (Ts and Tp). The measured spectra are analyzed using the Forouhi-Bloomer dispersion equations, in conjunction with RCWA, and applied simultaneously to reflectance and transmittance spectra. The method provides accurate and repeatable results for the degree of corner rounding of these samples. In addition, the method provides trench depth, critical dimension, film thickness, and optical properties (n and k spectra from 190 - 1000 nm) of phase-shift photomasks. The results of the measurements are represented as high-resolution uniformity maps are obtained for all the parameters mentioned above. The results show excellent correlation with conventional CD metrology techniques.

6730-117, Session 23

Photomask applications of traceable atomic-force microscope dimensional metrology at NIST

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The National Institute of Standards and Technology (NIST) has a multifaceted program in AFM dimensional metrology. Two major instruments are being used for traceable measurements. The first is a custom in-house metrology AFM, called the calibrated AFM (C-AFM), and the second is the first generation of commercially available critical dimension AFM (CD-AFM) the Veeco SXM320. Both of these instruments have useful applications in photomask metrology.

The NIST C-AFM has displacement metrology for all three axes traceable to the 633 nm wavelength of the Iodine-stabilized He-Ne laser. This is accomplished through the integration of a flexure x-y translation stage, heterodyne laser interferometers, and a z-axis piezoelectric actuator with an integrated capacitance sensor. This capacitance sensor is calibrated with a third interferometer. Pitch and height measurements for both internal and external customers have been performed with the C-AFM. In the previous generation of the C-AFM, the approximate limits on the standard uncertainty of pitch and step height measurements were slightly larger than 0.1 % for pitch measurements at the 1 μm scale and step heights at the 100 nm scale.

In the current generation of the system these uncertainties will be reduced - potentially by an order of magnitude. At present, however, this level of performance has not been fully validated. Toward this end, we recently participated in an international comparison of measurements of

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two dimensional gratings for AFM calibration, and have plans to participate in an upcoming comparison on one dimensional gratings, and are also performing measurements on a traceable grating manufactured at NIST using atom beam lithographic techniques. [1] If the uncertainties of step height measurements can be pushed lower, this could have implications in the calibration of phase offset for phase shifting mask (PSM) standards. For example, the uncertainties of some recent attempts at phase calibration using traceable step heights [2] might be reduced by a factor of three.

Providing linewidth reference metrology is an important application of CD-AFM - in both the photomask and wafer metrology arenas. Indeed, CD-AFM reference measurement were used to support the most recent release of the NIST photomask linewidth standard reference material (SRM) - which was SRM2059. [3] The SXM320, since it has the capability of measuring vertical sidewalls, complements the C-AFM. Although it does not have intrinsic traceability, it can be calibrated using standards measured on other instruments - such as the C-AFM, and we have developed uncertainty budgets for pitch, height, and linewidth measurements using this instrument. We use the SXM primarily for linewidth measurements of near-vertical structures. As a result of the NIST single crystal critical dimension reference material (SCCDRM) project, it is possible to calibrate CD-AFM tip width with a 1 nm standard uncertainty. [4] It is also expected that we will use this tool to support the next generation of the NIST photomask SRM.

We will report on the performance and uncertainties of both NIST AFM tools and on their applications to height and width metrology for photomasks.

6730-118, Session 23

Laterally resolved off-axis phase measurements on 45-nm node production features using Phame™

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As lithography mask process moves toward 45nm and 32nm node, phase control is becoming more important than ever. To ensure an accurate printing both attenuated and alternating PSMs (Phase Shift Masks) need precise control of phase as a function of both pitch and target sizes. However critical target CDs fall much below conventional phase metrology tools capability. Interferometer-based phase shift measurements are limited to large CD targets and require custom designed features in order to function properly, which limits phase measurement. AFM (Atomic Force Microscopy) methods are able to capture small feature sizes but do not consider any diffraction effects which are caused by the topography of the features itself when getting close to the used wavelength.

Imaging simulations, both, in a rigorous and a Kirchhoff regime, show the dependency of the phase in the image plane of a microlithography exposure tool on numerical aperture and pitch due to the loss of phase information in the imaging pupil. Additionally, for small features the phase is strongly impacted by polarization and 3D mask effects. For these feature sizes, the image phase does not coincide with the etch depth equivalent phase calculated from the nominal depth and optical constants of the shifter material. Deviations up to 20° have been observed leading to strong variations in the imaging quality and process window variations during scanner printing. Considerations of CD variation between 0 and pi features by simulation show lowest 0/pi CD variation and therefore largest process window if the scanner relevant phase is at 180°. The simulation results illustrate the importance to measure the scanner relevant phase, effective in the image plane of the scanner.

Consequently Zeiss, in collaboration with Intel, has developed a laterally resolving Phase Metrology Tool - Phame™ - for in-die phase measurements. The optical metrology tool is able to perform in-die phase measurement on alternating PSM, attenuated PSM and CPL masks down to 120nm half pitch. On-axis measurement results have already been published.

In this paper we present first off-axis measurement results over varying features sizes using different illumination conditions. The results will be compared to simulation. Further on process window considerations will be done and compared to the phase measurements.

6730-119, Session 24

LRC techniques for improved error detection throughout the process window

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Litho rule checking (LRC) is now an established component in the mask synthesis flow. Yet the requirements placed on LRC have grown as process complexity has increased. At 65nm and beyond, new techniques are required to thoroughly and efficiently evaluate a layout for potential lithographic problems.

This paper examines new modeling and checking techniques which improve the detection of lithographic errors. For more thorough error detection across a wider range of process points, a process window technique provides checking of potential lithographic errors at nine different process points. To better detect potential pinches or bridges induced by deep subwavelength lithography, a technique which identifies problems regardless of orientation is used. These techniques provide more thorough checking, both better accuracy and improved run time performance across the complete process window

6730-120, Session 24

Tera-computing for mask data preparation

J. T. Nogatch, H. Kirsch, J. Yeap, Synopsys, Inc.

Current and future Mask Data Preparation continues to see larger file sizes and longer processing times. Distributed Processing using multiple processors provides more compute power, but file Input/Output time remains a significant portion of MDP processing. Data compression, fast disk storage, and fast network hardware are shown to provide some benefit, but are not sufficient for unlimited scalability. Most MDP file formats store pattern data in a single disk file, which creates a performance obstacle in the process flow. Dividing data into multiple files is shown to improve writing speed, and to facilitate pipelined execution of multistage process flows. The advantages, disadvantages, and system management of Distributed Files in the terabyte regime are described.

6730-121, Session 24

Parallel hierarchical method in mask data preparation

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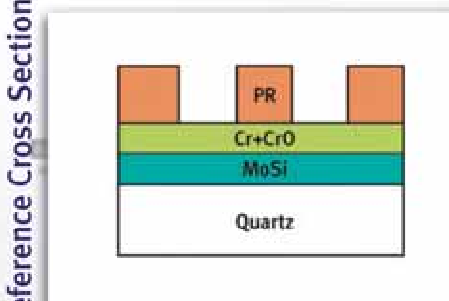
The given work offers new approach to the creation of computing medium - of parallel-hierarchical (PH) networks, being investigated in the form of model of neurolike scheme of data processing. The approach has a number of advantages as compared with other methods of neurolike formation media (for example, already known methods of artificial formation neural networks). The main advantage of the approach is the usage of multilevel dynamics parallel interaction of information signals at different hierarchy levels of computer networks, that enables to use such known natural features of computations organization in cortex as: topographic nature of mapping, simultaneity (parallelism) of signals operation, inlaid cortex, structure, rough hierarchy of the cortex, spatially correlated in time mechanism of perception and training. The formation of multi-stage PH networks assumes the process of correlated and formation sequential transformation of neural networks decorrelated in time elements at its transition from one stable state into another. The key feature of the offered approach is analysis of spatially correlated mechanism dynamics of neural networks resultant elements current and formation transformation. Such mechanism allows presenting in a new way the processing in neural networks as the process of parallel-sequential transformation of various components of image and account of transformation time responses. Physical contents of neural networks input elements, which participate in correlation - decorrelation, such as, for example, the amplitude or frequency, signals phase or energy, images cohesion or texture, is determined by the type of transformation being used, the selection of which depends on the class of problems being solved.

Reference Cross Section



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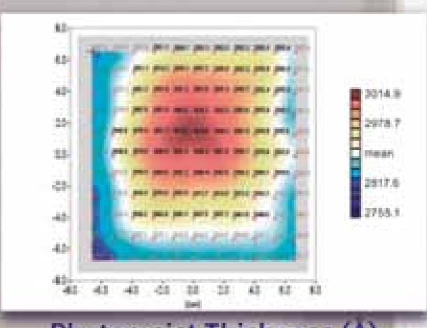
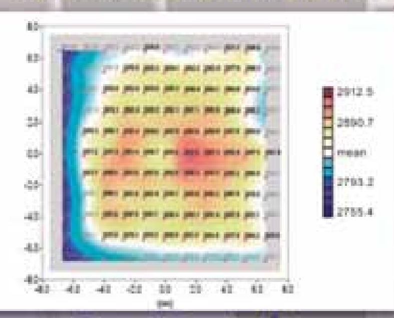
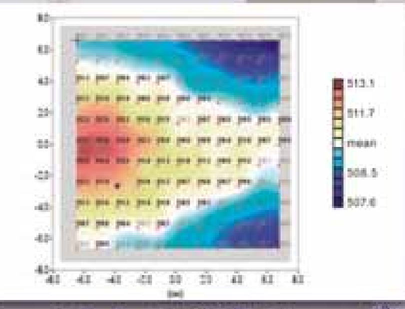
Film Thickness Measurement Uniformity Maps



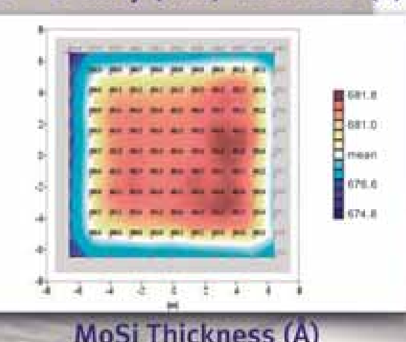
Photoresist Thickness (Å)



Trench Depth (Å)

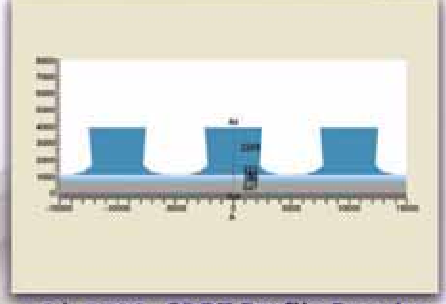


Cr + CrOxNy (ARC) Thickness (Å)



MoSi Thickness (Å)

Profile Measurement Comparison of ADI Structure



n&k 5700-CDRT Profile Results
Presence of Resist Footing Detected

SEM Profile Results
Presence of Resist Footing Exhibited

6730-122, Session 24

Mask manufacturability improvement by MRC

A. P. Balasinski, D. L. Coburn, Cypress Semiconductor Corp.; P. D. Buck, Toppan Photomasks, Inc.

Poor mask data quality makes it necessary for the mask shop to interfere with design issues in the absence of design guidelines. Mask makers may introduce potential defects to device properties by snapping geometries to grid, misrepresenting design based sizing, detuning inspection tools to release the mask in the production cycle, and waiving minimum CD rules compromising high fidelity of die pattern transfer to wafer. These actions may be done without contextual analysis which should include correlations to the overlying and underlying mask layers as well as device models. The key reason for this situation is design layout-to-mask post-processing for OPC and fill pattern for which design has no intention or knowledge to intervene. This post-processing, which effectively detaches design responsibility from the mask shop actions, has other severely detrimental effects on the production cycle such as iterative defect analysis and long write times due to the large polygon count. In this work we propose mask rule check based on the principles to which the masks are being written and inspected. Running this mandatory rule set should reduce the product cycletime, benefit the cost and improve mask quality and reproduction of design intent. It feeds the prospective mask information back to the layout time making it possible to make design adjustments in the interest of pattern fidelity and device parameters.

6730-123, Session 24

Reduction of layout complexity for shorter mask write time

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As tolerance requirements for the lithography process continue to shrink the complexity of the optical proximity correction is growing. Smaller correction grids and smaller fragments as well as the introduction of pixel based simulation lead to highly fragmented data - fueling the trend of larger file sizes as well as increasing writing times of the vector shaped ebeam systems commonly used for making advanced photomasks. The paper will introduce an approach of layout modifications to simplify the data considering fracturing and mask writing constraints in order to make it more suitable for these processes. The trade-offs between these simplifications and OPC accuracy will be investigated. A data processing methodology that allows preserving the OPC accuracy and modifications - all the way to the mask manufacturing and will be described.

The study focuses on 65nm and 45nm designs.

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Carl Zeiss Mask Solutions

Global CDU Map - quality assessment of total mask area

Printability tests for defect evaluation

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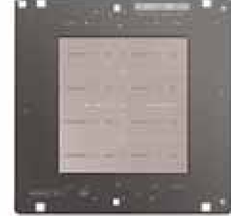

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17-21 September 2007

Monterey Marriott and Monterey Conference Center
1 Portola Plaza, Monterey, California 93940 USA

Registration and Information Hours

Monterey Conference Center, Portola Lobby

Monday, 17 September. . . . . 7:30 am to 4 pm
Tuesday, 18 September . . . . 7 am to 4 pm
Wednesday 19 September . . . . 7:30 am to 4 pm
Thursday, 20 September. . . . . 7:30 am to 4 pm
Friday, 21 September . . . . 8 am to 10 am

Exhibition Hours

Monterey Conference Center, Serra Ballroom

Tuesday, 18 September. . . . . 10 am to 4 pm; 6 to 7:30 pm
Wednesday, 19 September . . . . 10 am to 4 pm

Coffee Breaks

Coffee will be served at the following times and locations. Please check the conference listings for exact times.

Monterey Conference Center, Serra Grand Ballroom
Tuesday/Wednesday, 18-19 September . . 10 to 10:30 am; 3:10 to 3:30 pm

Monterey Conference Center, Steinbeck Lobby
Thursday, 20 September. . . . . 10 to 10:30 am; 3 to 3:30 pm
Friday, 21 September . . . . 10:30 to 11 am

Breakfast Breads

Monterey Conference Center, Steinbeck Lobby

Hosted breakfast beads will be served from 7:30 to 8:30 am, Tuesday through Friday for symposium attendees in the Steinbeck Lobby.

Exhibition/Poster Reception

Monterey Conference Center, Serra Grand Ballroom

Tuesday, 18 Sepember . . . . 6 to 7:30 pm

Symposium attendees and guests are invited to attend an Exhibition/Poster Reception on Tuesday evening in the Serra Grand Ballroom. The reception provides an opportunity for attendees to meet colleagues, network, and view poster papers. Refreshments will be served. Attendees are requested to wear their conference registration badges.

Poster Viewing

Tuesday 18 September. . . . . 6 to 7:30 pm
Wednesday 19 September . . . . 10 am to 3 pm

Poster authors may set up their poster papers between 10 am and 4 pm on Tuesday and will leave them up until Wednesday afternoon. Authors will be present during the Poster Reception 6 to 7:30 pm Tuesday to answer questions and provide in-depth discussion regarding their papers. Any papers not removed by Wednesday at 3 pm will be considered unwanted and will be discarded. SPIE assumes no responsibility for papers left up after Wednesday at 3 pm.

SPIE-Hosted Lunches

Hosted lunches will be served at the Monterey Marriott in the San Carlos Ballroom at the following times:

Tuesday-Thursday, 18-20 September . . . . 11:50 am to 1 pm

Please check the technical conference listings for exact times.

Complimentary tickets for these lunches will be included for full conference registrants. Exhibitors and Students may purchase tickets in the SPIE registration area in the Portola Lobby.

Desserts

Dessert will be served Tuesday and Wednesday in the Exhibition located in the Monterey Conference Center Serra Grand Ballroom from 3 to 3:30 pm. A complimentary ticket for dessert will be included in attendee and exhibitor registration packets.

Onsite Services

Speaker Presentation Preview Room

Monterey Conference Center • Open during Registration Hours

All Conference rooms will have a computer workstation, LCD projector, screen, lapel microphone, and laser pointer. All presenters are encouraged to visit the Speaker Presentation Preview Room to confirm display compatibility of their presentation, whether using a memory device or laptop, with the audiovisual equipment supplied in the conference rooms.

Speakers who have requested equipment, prior to the request deadline, are asked to report to the SPIE Registration Desk to confirm their requested equipment.

Online Employment and Recruiting

SPIEWorks, the SPIE job site, is uniquely positioned to serve you. SPIEWorks was developed to serve the career needs of optics, photonics and imaging professionals. This website provides job seekers with: job listings by region, technology, and keywords, email alerts, and research resources such as the Technical Library and company listings. Employers may post jobs and gain access to a resume database, create a Resume Alert, and participate in career fairs (events tightly integrated with major SPIE conferences). For all you employment and recruiting needs SPIEWorks is here to serve you. For further information visit us at SPIEWorks.com. Contact our sales staff at sales@spieworks.com or phone: (360) 715-3705.

Internet Pavilion

Monterey Conference Center, Steinbeck Lobby

There will be several computer stations for attendees to access their internet e-mail during the conference. There will be a 10-minute time limit per each person's internet session.

Business Center

For attendees staying at the Monterey Marriott they may use their hotel room key to access the on-site Business Center which offers use of a free on-line computer. A copying machine is available at the front desk - first 20 copies are free, over 20 copies are 10 cents per page. A fax machine, also located at the front desk is available for $1.00 per page for domestic usage, and $3.00 per page for international usage. Each hotel room is equipped with data ports for hookup to high-speed internet service for $9.95 for 24 hours from noon-noon.

The closest off-site business center is Fedex Kinko's located at 799 Lighthouse Ave., Ste. A, Monterey, CA, 93940, Phone: (831) 373-2298. It is 1.3 miles from the Monterey Marriott (approx. 5 minutes driving time). Go north on Calle Principal, left onto Del Monte Ave., right onto Pacific St., right onto ramp to merge onto Lighthouse Ave.

SPIE Message Center

The SPIE Message Center telephone number is (831) 646-5312. Ask for SPIE Registration Desk.

Messages will be taken during registration hours Monday through Friday, 17-21 September 2007. Please check the message board at the SPIE Registration area frequently to receive your messages.

Child Care Services

The Monterey Marriott suggests the following child care service companies in Monterey: Parents Time Out, (831) 375-9269

Corporate Kids Events, Inc

Phone: (831) 277-9328

Email: info@corporatekidsevents.com or garen@corporatekidsevents.com

http://corporatekidsevents.com

SPIE does not imply an endorsement or recommendation of this service. It is provided on an "information only" basis for your further analysis and decision. Other services may be available.

Policies

Laser Pointer Safety Information

SPIE supplies tested and safety approved laser pointers for all conference meeting rooms, and for short course rooms if instructors request one. For safety reasons, SPIE requests that presenters use our provided laser pointers available in each meeting room.

If using your personal laser pointer:

- Please have it tested at your facility to make sure it has <5 mW power output. Laser pointers in Class II and IIIa (<5 mW) are eye safe if power output is correct - but don't automatically trust the labeling. Commercially available laser pointers, red or green (or any color), could be incorrectly labeled as to their wavelength and power output.
- We require that you to come to the Registration Desk onsite and test you pointer on our power meter. If the pointer fails the safe power level you may not use the pointer at the conference. You will be required to sign a waiver releasing SPIE of any liability for use of potentially non-safe laser pointers.
- Use of a personal laser pointer at an SPIE event represents user's acceptance of liability for use of a non-SPIE supplied laser pointer device. Misuse of any laser pointer could lead to eye damage. In California, it is a criminal misdemeanor to shine a laser pointer at individuals "who perceive they are at risk."

Underage Persons on Exhibition Floor

For safety and insurance reasons, no persons under the age of 16 will be allowed in the exhibition area during move-in and move-out. During open exhibition hours, only children over the age of 12 accompanied by an adult will be allowed in the exhibition area.

Audio, Video, Digital Recording Policy

In the Meeting Rooms and Poster Sessions: For copyright reasons, recordings of any kind are strictly prohibited without prior written consent of the presenter in any conference session, short course or of posters presented. Each presenter being taped must file a signed written consent form. Individuals not complying with this policy will be asked to leave a given session and asked to surrender their film or recording media. Consent forms are available at the SPIE Audiovisual Desk.

In the Exhibition Hall: For security and courtesy reasons, photographing or videotaping individual booths and displays in the exhibit hall is allowed ONLY with explicit permission from on-site company representatives. Individuals not complying with this policy will be asked to surrender their film and to leave the exhibit hall.

Monterey Marriott Hotel

350 Calle Principal, Monterey, CA, 93940

Hotel Front Desk Phone: (831) 649-4234
Hotel Front Desk Fax: (831) 372-2968

Monterey Conference Center

No Suitcasing Policy

Suitcasing is the act of soliciting business in the aisles during the exhibition or in other public spaces, including another company's booth or a hotel lobby.

Please note that while all meeting attendees are invited to the exhibition, any attendee who is observed to be soliciting business in the aisles or other public spaces, in another company's booth, or in violation of any portion of SPIE Exhibition Policy will be asked to leave immediately. Additional penalties may be applied. Please report any violations you may observe to show management.

Unsecured Items

Personal belongings such as briefcases, backpacks, coats, book bags, etc. should not be left unattended in meeting rooms or public areas. These items will be subject to removal by security upon discovery.

17-21 September 2007

Monterey Marriott and Monterey Conference Center
1 Portola Plaza, Monterey, California 93940 USA

Parking at the Monterey Conference Center

Public parking is available in the East Garage, two blocks down from the hotel. Drive down Franklin Street (one-way), turn left on Washington Street, and turn left into the parking garage. You can also enter the parking garage turning left on Del Monte Street or left on Tyler Street (both one way streets). To park, pay the flat rate per day of $5, payable in exact change (one five dollar bill or five one dollar bills) as there is no attendant on duty to make change. MasterCard or Visa is also accepted. No in/out privileges. City Parking Lots (831-646-3953) http://www.monterey.org/parking/

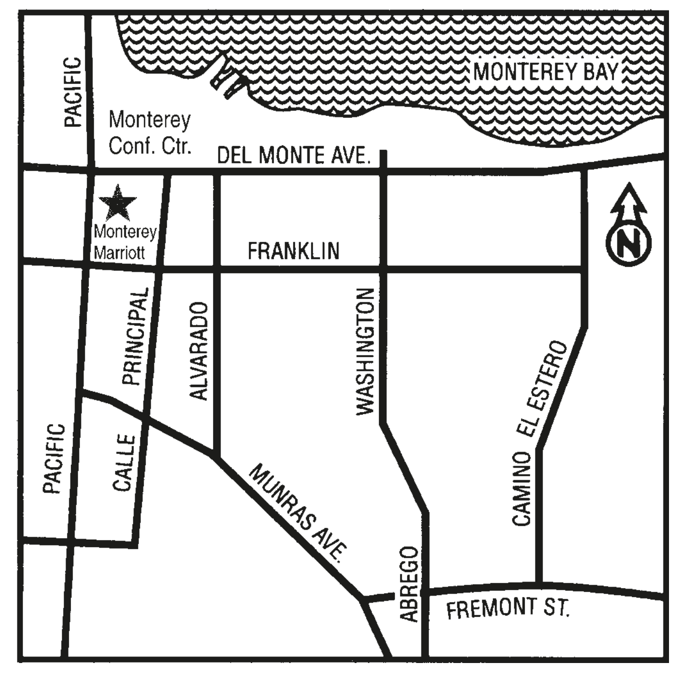
Parking is also available in the West Garage across from the East Garage, which has an attendant on duty, open 24 hours with in/out privileges. Drive down Washington Street; go left on Del Monte Street and left on Tyler. The lower level has a time limit maximum of 90 minutes and parking in this lower level is free. The upper level charges $1.00/hour or $8.00 per day, with the first hour free. They accept cash or American Express, MasterCard or Visa, and the attendant will make change.

Additional Conference Center Parking at the Portola Plaza Hotel Lot

Conference Center guests can park at the Portola Plaza Hotel for $2 for the 1st hour, $1 each additional half hour, maximum $17 in 24 hrs., payable with cash only. There is an attendant on site. Portola Plaza Hotel phone number is 831-649-4511. The hotel is directly across from the Marriott, and both are connected to the Monterey Conference Center by a footbridge.

All parking rates are subject to change without notice.

Car Rental has been selected as the official car rental agency for this Symposium. To reserve a car, identify your-



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As host to events that bring together scientists and engineers from around the globe, SPIE is committed to making our symposia as environmentally friendly as possible.

SPIE's ongoing efforts include using non-disposable materials such as glass plates and metal flatware as often as possible, and encouraging facilities to donate surplus meals to soup kitchens. Many partnering facilities have robust recycling programs for paper, plastic and aluminum products. SPIE continues to collaborate with venues, hotels, suppliers and the local Chambers of Commerce to assess and ease the conference's environmental impact. SPIE is currently working to implement solutions from the Green Meetings Industry Council guidelines* with a goal to take our environmental efficiency to a whole new level.

When at this event, SPIE encourages you to take advantage of recycling bins, to reuse towels at your hotel, to carpool whenever possible, and to walk or use public transportation during your stay in Monterey.

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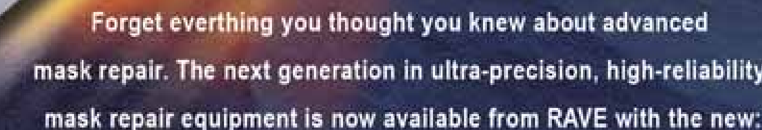

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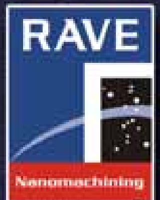

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