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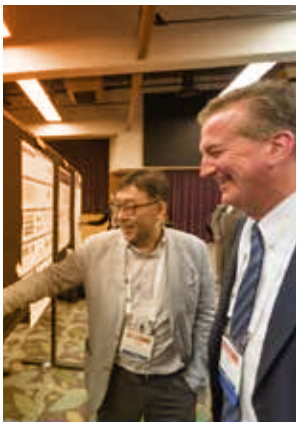

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Contents

SPIE.

9235-1, Session 1

Many ways to shrink: The right moves to 10 nanometer and beyond (Keynote Presentation) *(Keynote Presentation)*

Martin van den Brink, ASML Netherlands B.V. (Netherlands)

With mobile devices such as smartphones outpacing other market segments, the demand for low-power chips, enabled by continued device shrink, continues to be strong. The semiconductor industry's drive to innovate is relentless, R&D pipelines are filled, and IC manufacturers have multiple options to continue scaling. This presentation will examine the different technology options for the 10 nanometer node and beyond.

9235-2, Session 2

EUV mask infrastructure: Don't miss the train! *(Invited Paper)*

Oliver Kienzle, Carl Zeiss SMS GmbH (Germany)

While the extension of 193 immersion lithography is driven to enable further shrinking, the related overall lithography process complexity and design restrictions become a headache.

Undoubtedly, with its outstanding imaging performance EUV will reduce complexity with less lithography steps and less overall process complexity. Furthermore, the full two-dimensional imaging capabilities reduce design constraints and node shrinking can then be fully exploited for device shrinking.

Currently, however, EUVL is not yet competitive mainly due to the lack in EUV source power. As counter measure, the industry is investing tremendously to overcome the remaining limitations and a solution can be expected shortly.

On the EUV mask infrastructure Sematech with its EMI initiative has started several projects regarding EUV Actinic Blank Defect Detection (ABI) and EUV Aerial Image Measurement System (AIMS™). Other technologies like EUV Mask Defect repair and Registration Metrology are progressing or are already available. However, some crucial building blocks of EUV mask infrastructure are not yet set on a clear path forward.

In my presentation I will review the EUV mask infrastructure from a mask equipment supplier's perspective: What is there and what is missing? How to bridge existing gaps and what could be done to catch the EUV train.

9235-3, Session 3

Layout compliance for triple patterning lithography: an iterative approach *(Invited Paper)*

Bei Yu, The Univ. of Texas at Austin (United States); Gilda Garreton, Oracle (United States); David Z. Pan, The Univ. of Texas at Austin (United States)

As the semiconductor process further scales down, the industry encounters many lithography-related issues.

In the 14nm logic node and beyond, triple patterning lithography (TPL) is one of the most promising techniques for Metal1 layer and possibly Via0 layer.

As one of the most challenging problems in TPL, recently layout decomposition efforts have received more attention from both industry and academia.

Ideally the decomposer should point out locations in the layout that are not triple patterning decomposable and therefore manual intervention by designers is required.

A traditional decomposition flow would be an iterative process, where each iteration consists of an automatic layout decomposition step and manual layout modification task.

However, due to the NP-hardness of triple patterning layout decomposition, automatic full chip level layout decomposition requires long computational time and therefore design closure issues continue to linger around in the traditional flow.

Challenged by this issue, we present a novel incremental layout decomposition framework to facilitate accelerated iterative decomposition.

In the first iteration, our decomposer not only points out all conflicts, but also provides the suggestions to fix them.

After the layout modification, instead of solving the full chip problem from scratch, our decomposer can provide a quick solution for a selected portion of layout.

We believe this framework is efficient, in terms of performance and designer friendly.

9235-4, Session 3

Double-patterning optimization in 20nm SRAM design

Qi Lin, Toshiyuki Hisamura, Nui Chong, Hans Pan, Yun Wu, Jonathan Chang, Xin Wu, Xilinx, Inc. (United States)

As semiconductor critical dimension (CD) is shrunk to 20nm node and beyond, the doubling patterning or triple patterning technology becomes necessary for current 193nm optical lithography. However, the new technology induces a new variation factor of the two or three mask pattern mismatching in terms of the wafer CD or alignment performance on silicon. This mismatch can degrade matching circuit performance such as SRAM and analog circuit. In this paper, we address the impact on our 20nm CRAM (configuration RAM used in FPGA circuit) performance caused by pattern decomposition (coloring) manner. Furthermore, we propose a methodology to optimize the coloring and OPC (Optical Proximity Correction) based on an alignment performance assessment and CD control of two mask patterns printed on silicon wafer. The silicon results show that after the optimization, the impact of coloring-induced mismatch on CRAM performance can be reduced significantly.

9235-5, Session 3

Pattern-based pre-OPC operation to improve model-based OPC runtime

Piyush Verma, Fadi Batarseh, Shikha Somani, Jingyu Wang, Sarah McGowan, Sriram Madhavan, GLOBALFOUNDRIES Inc. (United States)

Optical Proximity Correction is a mandatory step in the mask manufacturing flow for sub-wavelength lithography. In a typical Optical Proximity Correction step at these nodes, optical and resist models are used to modify the drawn layer such that the layout features can be accurately reproduced by the lithography process onto the wafer. Due to the complexity of the models and the iterative nature of the correction, OPC is a runtime intensive step in the photomask manufacturing flow. Additionally, the time duration between the tapeout of the physical design and the arrival of the photomask is extremely critical as it directly relates to the wafer starts at the fabrication plant.

Due to complex photolithography sources, a large correction has to be applied via the OPC step to obtain the photomask shapes for certain geometric configurations. Depending upon the specific pattern and process, this correction can be as large as several 10s of % of the drawn feature size. The standard practice in the OPC step is to start with the drawn shapes, fragment the edges of the polygons and apply an iterative correction using a sophisticated control system. Due to the large correction that the OPC step has to achieve, several iterations (~10-20) have to be performed before accurate mask shapes can be obtained, thereby increasing the runtime. A pre-OPC biasing step can be used to reduce the total OPC runtime as proposed in previous work [1,2]. However, the pre-OPC biasing is typically based on rules, which are difficult to develop, implement and maintain. The technique described in this paper utilizes pattern search tools plus a feedback mechanism to improve the accuracy and reduce runtime as more learning is achieved. Pattern based techniques for OPC have been demonstrated in the past to improve OPC runtime [3,4], however a pattern based approach alone may result in reduced OPC accuracy. The technique in this paper works by first performing a pattern search and replacement on the drawn design based on a pre-populated library to obtain a 'biased' design. The pattern replacement library is built beforehand by performing model based OPC on simple 'building-block' patterns. The regular model based OPC correction is then applied to this new 'biased' design. Since a significant portion of the correction has already been performed during the fast pattern replacement step, fewer iterations of model based OPC are required to achieve the same correction accuracy. Further intelligence can be built into the pattern replacement library by performing a pattern analysis on the final mask shapes of the full chip design and updating the library accordingly. This hybrid pattern-based and model-based OPC approach can be used to significantly reduce the tapeout cycle time while retaining the photomask accuracy.

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9235-6, Session 3

Conducting OPC retargeting as guided by principles of classical dynamics

Jingyu Wang, Piyush Verma, GLOBALFOUNDRIES Inc. (United States); Alexander Wei, Mentor Graphics Corp. (United States); William Wilkinson, GLOBALFOUNDRIES Inc. (United States)

While optical proximity correction (OPC) aims at reproducing a comprehensive optical and resist environment as possible, its correctness is necessarily limited by the pre-defined collection of test patterns used for model building. The effectiveness of the OPC engine in predicting certain geometries' wafer printability may be impacted by either a repeatable lithography process offset or multi-layer topographic effects. In those cases, a certain degree of local retargeting becomes essential for robust manufacturability. However, OPC engine settings such as fragmentation, iteration, feedback and target choices are previously aligned with model settings and design dimensions, they may not readily accommodate manual adjustment of target shapes. Given this potential misalignment, retargeting is in some sense rendered a trial and error attempt. To provide insights into a best practice and better organize simulation resources, we treat the OPC engine with a classical thermo/dynamics perspective. That is, we visualize an intentional local retargeting as always opposed by the "inertia" of the original design with its associated mask shapes. Specifically, we start with a one dimensional spring model, and extend it to a two dimensional string problem, to account for single fragment and multi-fragment retargeting, respectively. We extract the exact variation amount of mask shape and simulation contour from each OPC iteration. By analyzing the convergence to the retargeted shape, we compare the "force/energy" applied with "displacement/work" completed, to assess the efficiency in the retargeting algorithm. The methodology enables us to systematically characterize established designs, and depending on which, evaluate available retargeting strategies.

9235-7, Session 4

Evolution of mask data preparation *(Invited Paper)*

Aki Fujimura, D2S, Inc. (United States)

We are amidst a discontinuity in mask data preparation. Shapes narrower than three sigma of blur radius, non-orthogonal edges written with orthogonally shaped apertures, and the impending shift to multi-beam based mask writing all point to a vastly different set of considerations for the mask data preparation flow. The paper will start with conventional fracturing and its quality metrics and build the discussion through model-based requirements of the leading edge masks.

9235-8, Session 4

Model-based virtual VSB mask writer verification for efficient mask error checking and optimization prior to MDP

Robert C. Pack, GuoXiang Ning, Todd Lukanc, Fadi Batarseh, Piyush Verma, GLOBALFOUNDRIES Inc. (United States); Aki Fujimura, D2S, Inc. (United States)

A methodology is described wherein a calibrated model-based 'Virtual' Variable Shaped Beam (VSB) mask writer process simulator is used to accurately verify complex RET mask designs prior to MDP and mask fabrication. This type of verification addresses physical effects which occur in mask writing that may impact lithographic printing fidelity and variability.

The work described here is motivated by requirements for extreme accuracy and control of variations in the patterning of MOSFET gates for today's most demanding IC products. For 28nm and smaller technology nodes, these gates are routinely biased based on their function by fractions of a nanometer to achieve optimal performance, power, and yield requirements. These extreme demands necessitate detailed analysis of all potential sources of uncompensated error or variation and extreme control of these at each step of the design retargeting/ RET/MDP/Mask/ silicon lithography flow.

At the RET stage, the cause-effect nature of residual lithographic printing variations are well-known and verification methods exist and are used commonly to reliably flag errors and unacceptable excursions. If an error occurs, an efficient short-loop correction method may then be implemented. However at the mask level the cause-effect nature of lithographic printing variations are not as well-known and comparable verification methods are not typically used for feedback into MDP. When a hotspot, error, or inherent weak point exists, a long-loop iteration between the RET and MDP may occur. Or worse, an inherent statistical marginality goes undetected resulting in a product that does not achieve its potential performance or yield.

The important potential sources of variation we focus on here originate on the basis of VSB mask writer physics and other errors inherent in the mask writing process. The deposited electron beam dose distribution may be examined in a manner similar to optical lithography aerial image analysis and image edge log-slope analysis. This approach enables

one to catch, grade, and mitigate problems early and thus reduce the likelihood for costly long-loop iterations between Retargeting/RET, MDP, and wafer fabrication flows. It moreover describes how to detect regions of a layout or mask where hotspots may occur or where the robustness to intrinsic variations may be improved by modification to the RET, choice of mask technology, or by judicious design of VSB shots and dose assignment.

Design-thru-mask-thru-silicon simulation and fabrication of 28nm, 20nm, and 14nm technology is examined in detail for planar MOSFET and FINFET gates.

9235-9, Session 4

Mask model calibration for MPC applications utilizing shot dose assignment

Ingo Bork, Peter D. Buck, Mentor Graphics Corp. (United States); Sankaranarayanan Paninjath Ayyappan, Kushlendra Mishra, Mentor Graphics (India) Pvt. Ltd. (India); Christian Bürgel, Advanced Mask Technology Ctr. GmbH Co. KG (Germany); Gek Soon Chua, GLOBALFOUNDRIES Singapore (Singapore); Keith P. Standiford, GLOBALFOUNDRIES Inc. (United States)

Shrinking feature sizes and the need for tighter CD (Critical Dimension) control require the introduction of new technologies in mask making processes. One of those methods is the dose assignment of individual shots on VSB (Variable Shaped Beam) mask writers to compensate CD non-linearity effects and improve dose edge slope. Using increased dose levels only for most critical features, generally only for the smallest CDs on a mask, the change in mask write time is minimal while the increase in image quality can be significant. However, this technology requires accurate modeling of the mask effects, especially the CD/dose dependencies. This paper describes a mask model calibration flow for MPC applications with shot dose assignment.

The first step in the calibration flow is the selection of appropriate test structures. For this work a combination of line/space patterns including tip to tip line ends and space ends as well as a series of contact patterns are used for calibration. Features sizes vary from 30nm up to several micrometers in order to capture a wide range of CDs and pattern densities. After mask measurements are completed the results are carefully analyzed and measurements very close to the process window and outliers are removed from the data set.

One key finding in this study is that by including patterns exposed at various dose levels the simulated contours of the calibrated model very well match the SEM contours even if the calibration was based entirely on gauge based CD values. In the calibration example shown in this paper, only 1D line and space measurements as well as 1D contact measurements are used for calibration. However, those measurements include patterns exposed at dose levels between 65% and 150% of the nominal dose. The best model achieved in this study uses 3 e-beam kernels and 4 kernels for the simulation of development and etch effects. The model error RMS on a large range of CD down to 30nm line CD is below 1nm.

The calibrated model is then used to generate 2D contours for line ends, space ends and contacts and those contours are compared to SEM images. For all patterns including those very close to the resolution limit very good contour overlay is achieved. It appears that by including the various dose levels in the calibration a very good separation of the e-beam model components from the etch components is possible and that this also results in very accurate 2D model quality.

In conclusion, very accurate mask model calibration is achieved for mask processes using shot dose assignment. Standard test patterns can be used for calibration if they include the dose variations intended for correction.

9235-10, Session 4

Automated hotspot analysis with aerial image CD metrology for advanced logic devices

Ute Buttgereit, Thomas Trautzsch, Carl Zeiss SMS GmbH (Germany); Min-Ho Kim, Jung-Uk Seo, Young-Keun Yoon, Hakseung Han, Dong-Hoon Chung, Chan-Uk Jeon, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); Gary Meyers, Synopsys, Inc. (United States)

Continuously shrinking designs by further extension of 193nm technology lead to a much higher probability of hotspots especially for the manufacturing of advanced logic devices. The CD of these potential hotspots needs to be precisely controlled and measured on the mask. On top of that, the feature complexity increases due to high OPC load in the logic mask design which is an additional challenge for CD metrology. Therefore the hotspot measurements have been performed on WLCD from ZEISS, which provides the benefit of reduced complexity by measuring the CD in the aerial image and qualifying the printing relevant CD. This is especially of advantage for complex 2D feature measurements.

Additionally, the data preparation for CD measurement becomes more critical due to the larger amount of CD measurements and the increasing feature diversity. For the data preparation this means to identify these hotspots and mark them automatically with the correct marker required to make the feature specific CD measurement successful. Currently available methods can address generic pattern but cannot deal with the pattern diversity of the hotspots. The paper will explore a method how to overcome those limitations and to enhance the time-to-result in the marking process dramatically. For the marking process the Synopsys WLCD Output Module was utilized, which is an interface between the CATS mask data prep software and the WLCD metrology tool. It translates the CATS marking directly into an executable WLCD measurement job including CD analysis.

The paper will describe the utilized method and flow for the hotspot measurement. Additionally, the achieved results on hotspot measurements utilizing this method will be presented.

9235-11, Session 4

OPC-Lite for gridded designs at low k1

Valery Axelrad, Sequoia Design Systems, Inc. (United States); Michael C. Smayling, Tela Innovations, Inc. (United States); Koichiro Tsujita, Koji Mikami, Canon Inc. (Japan); Hidetami Yaegashi, Tokyo Electron Ltd. (Japan)

Highly regular gridded designs are generally seen as a key component for continued advances in lithographic resolution in a time of limited further progress in lithography hardware [1]. With a given process technology tool set, higher pattern density (lower k1) and quality are achieved using gridded design rules (GDR) in comparison to conventional 2D designs.

GDR is necessary for designs with k1 approaching the theoretical limit ~ 0.25. The regular structure of gridded designs offers the opportunity to use an optimized approach to Optical Proximity Correction (OPC), one taking full advantage of the design style to achieve best possible accuracy and speed and at the same time small mask file size and good manufacturability. In this work we describe our GDR-tailored OPC tool called OPC-Lite [6]. The OPC-Lite approach is discussed and compared to conventional 2D OPC. Sub-20nm silicon data are shown, validating predictive quality of our simulation and OPC techniques. Implications of OPC-Lite to mask manufacturability and cost are discussed.

Gridded designs construct complete circuits from regular lines and cuts electrically separated at required locations by cuts. This is typically implemented using a double-patterning lines+cuts approach cite{spie2014-contacts}, although alternative single-patterning implementations are also possible cite{spie2014-opc}. Example GDR

patterns and sub-20nm SEM data cite{spie2012} are shown in Fig. ref{fig:lines_cuts_example}. The full paper will discuss application of OPC-Lite to all critical layers of the design including gate, Metal-1 and contacts.

Design intent is implemented by cuts, which create the required circuit connectivity. Their locations relative to each other cause proximity effects, which may be severe and must be compensated for by OPC. In contrast to conventional 2D-OPC, GDR target shapes are simple rectangles, one for each cut (Fig. ref{fig:lines_cuts_example}). There are no complex 2D shapes to image, only cuts whose sole purpose it is to create electrical separation of a line at the desired location. The actual shape of the patterned cuts is electrically irrelevant and can therefore be ignored by the OPC algorithm.

We construct the target cuts layer from a group of rectangular layout elements, one for each cut. The dimensions of each cut are iteratively adjusted based on simulated CD cite{sispad2012} calculated for this cut (Fig. ref{fig:opc-lite}, left). Cuts are either directly adjacent in groups, or otherwise spaced relatively far apart (a minimum of one Rayleigh distance $0.25 cdot lambda/NA$). Because of this, local iterative correction (OPC) exhibits good convergence properties. Table ref{tab:convergence} shows the convergence of CD error for a test layout at different technology nodes and the same KrF lithography tool set.

In comparison to conventional 2D-OPC, where layout segments are shifted to control local edge placement error, our algorithm has several benefits: begin

{itemize} item faster convergence and $<1nm$ CD error in few iterations since GDR cuts are spaced much farther apart than layout segments in 2D-OPC

item much lower MEEF cite{bacus2012} due to minimal layout complexity (rectangles)

item minimal mask complexity and small mask file size cite{bacus2012} since each cut is represented by only one rectangle

end{itemize}

9235-12, Session 5

Plasma technology for advanced quartz mask etching *(Invited Paper)*

Munenori Iwami, Hirotsugu Ita, Yoshihisa Kase, Hidehito Azumano, Kazuki Nakazawa, Yoshie Okamoto, Hiroki Shirahama, Tomoaki Yoshimori, Makoto Muto, Shibaura Mechatronics Corp. (Japan)

Recently there is serious discussion going on about the production of 9 inch masks for efficient processing of next-generation 450 mm wafers. Reticle dry etching on these larger masks requires stringent uniformity and reproducibility over quartz plates which are not only larger, but also thicker, and RF bias control for such thick substrates is not straightforward. In this contribution we discuss dry etching on the thicker quartz plates focusing on the issues of RF biasing.

The RF voltage across the sheath is sustained by the RF source at the bias.

Mask processing should proceed at the ion energies and sheath voltages established for 6 inch plats in order to capitalize on the state of the art established for them. On the other hand, RF voltages across both the sheath and the quartz plate are proportional to the respective RF impedances, and the higher impedance of the thicker quartz plates would cause weaker sheath coupling, lower sheath voltages, and poorer ion energy controllability, unless the sheath impedance is increased, too. The sheath impedance is known to depend on the RF frequency, thus we propose to change the bias frequency in a way compensating for the increased substrate thickness. Another idea for sheath voltage control is to aim for a series resonance of the inductive plasma bulk and the capacitive sheath.

9235-13, Session 5

Increasing efficiency and effectiveness of processes related to airborne particles in reticle mask environments

Allyn Jackson, CyberOptics Corp. (United States)

Minimizing airborne particles in Photo Lithography semiconductor fab manufacturing applications remains a critical success factor. Stringent manufacturing requirements and a focus on maximizing yields and tool uptimes drives a need for best-in-class practices for a contamination-free process environment. Quickly identifying when and where airborne particles originate as well as the source of the contamination proves challenging with traditional surface scan wafer methods.

Whether it's for equipment diagnostics, particle qualification or preventative maintenance, equipment engineers need the ability to identify and troubleshoot airborne particle issues as efficiently and effectively as possible. Legacy methods are not real time and they can also be time consuming and result in long delays for results. It can also involve tearing down the fab tool or running a series of test wafers, which can be time consuming and costly in terms of downtime. These drawbacks lead to delays in equipment qualification and release to production as well as delays in equipment maintenance cycles.

CyberOptics will review the advantages of using the wireless wafer-like real-time particle counter method as a more efficient and effective means of quickly locating and troubleshooting airborne particles in real-time with the ReticleSense™ Airborne Particle Sensor (APSR) in reticle environments.

In the photolithography application, this solution is ideal for quickly checking the dozens of particle sensitive chambers that otherwise might take days to check, replacing the need for time-consuming multiple surface scan wafers.

With the ParticleView™ software and the device, particles can be recorded to compare past to present as well as tool to tool. It follows the Reticle path and can travel to multiple areas of the tool to detect where particles fall with the highest level of accuracy and precision. The Airborne Particle Sensor and the Airborne Particle Sensor Reticle) measurement devices are capable of detecting and counting particles as small as 100 nm (0.1 micron), reports data wirelessly in real-time to a PC and provides graphical and numerical analysis with the highest accuracy and precision. Tests or calibrations can be conducted under production conditions for seamless ease-of-use. Ultimately, these advantages over legacy solutions, result in compelling bottom lines – improved yields, optimized maintenance and increased equipment uptime – saving time and money.

Specific, quantified results using the APS device and accompanying software, in terms of cost savings, time savings, reduction in manpower requirements and throughput will be highlighted.

9235-14, Session 5

Performance of GFIS mask repair system for various mask materials

Fumio Aramaki, Tomokazu Kozakai, Osamu Matsuda, Anto Yasaka, Hitachi High-Tech Science Corp. (Japan); Shingo Yoshikawa, Koichi Kanno, Dai Nippon Printing Co., Ltd. (Japan); Hiroyuki Miyashita, DNP Photomask Europe S.p.A. (Italy); Naoya Hayashi, Dai Nippon Printing Co., Ltd. (Japan)

The photomask repair technology has been evolved to achieve more precise process with the shrinkage of device design rules. Recently, most of defects on high-end masks are repaired with electron beam (EB). The minimum repairable dimension of the current state-of-the-art repair systems is approximately between 20 nm and 30 nm, but it is not small enough to repair the next generation masks. Meanwhile, new mask materials are going to be introduced to improve the durability

against exposure and cleaning, but the etching selectivity between those materials and quartz under EB repair process is not high enough to control etching depth.

Recently, focused ion beam (FIB) systems using gas field ion source (GFIS) are well known as tools for high resolution imaging and processing. Those can emit ions of various species by changing source gas.

In the last few years, we have developed the mask repair technology by using GFIS. At SPIE 2011, we reported the results of repairing an EUV mask with hydrogen ions emitted by GFIS. At PMJ 2012, we reported the results of repairing a new material MoSi mask with nitrogen ions emitted by GFIS. At BACUS 2012, we reported that the repairable dimension of our GFIS system was less than 10 nm. In order to introduce GFIS systems into actual repair process at various mask shops, it is expected that more various mask materials are evaluated.

The objective of this study is to verify the feasibility of GFIS technology for repairing various masks made of the above new materials. Specifically, the minimum repairable dimension, image resolution, scan damage and etching selectivity between each material and quartz were evaluated. Furthermore, we repaired programmed defects and evaluated the edge placement accuracy and the through-focus behavior on AIMS. The latest results of our evaluation are reported in this paper.

9235-15, Session 5

Defects caused by blank masks and repair solution with nanomachining for 20nm node

Hyemi Lee, ByungJu Kim, HoYong Jung, SangPyo Kim, DongGyu Yim, SK Hynix, Inc. (Korea, Republic of)

As the number of masks per wafer product set is increasing and low k1 lithography requires tight mask specifications, the patterning process below sub 20nm tech. node for critical layers will be much more expensive compared with previous tech. generations. Besides, the improved resolution and the zero defect level are necessary to meet tighter specifications on a mask and these resulted in the increased the blank mask price as well as the mask fabrication cost.

Unfortunately, in spite of expensive price of blank masks, it is fact that the certain number of defects on the blank mask transform into the mask defects and its ratio are increased. But using high quality blank mask is not a good idea to avoid defects on the blank mask because the price of a blank mask is proportional to specifications related to defect level. Furthermore, particular defects generated from the specific process during manufacturing a blank mask are detected as a smaller defect than real size by blank inspection tools because of its physical properties. As a result, it is almost impossible to prevent defects caused by blank masks during the mask manufacturing.

In this paper, blank defect types which is evolved into mask defects and its unique characteristics are observed. Also, the repair issues are reviewed such as the pattern damage according to the defect types and the repair solution is suggested to satisfy the AIMS (Arial Image Measurement System) specification using a nanomachining tool.

9235-44, Session PS2

Chemical stability of graphene as a EUV pellicle

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As EUV lithography comes closer to high volume manufacturing, it is increasingly important to maintain a defect-free reticle. Pellicles are widely used to prevent particles from depositing on the reticle in lithography. However, conventional pellicles are not suitable for EUV due to their high absorption in the EUV. In the past, several investigations of Si-based pellicle were reported. However, these pellicles suffer from the imaging performance degradation, manufacturing issues, and unmanageable heat loads. Recently, advances in 2D materials, such as graphene, have led to new potential candidates for an EUV pellicle.

Graphene, a two-dimensional hexagonal packed sheet of carbon atoms, has attracted a lot of attention from different research fields due to its unique physical and chemical properties. Graphene has a theoretical transmission of 99.8% at 13.5 nm. And also, it is reported as one of the strongest materials with a Young`s modulus of 1 TPa and tensile strength of 130 GPa. The thermal conductivity of graphene was reported at approximately 5x10^3 W/mK. The high thermal conductivity and ultra-low interfacial thermal resistance between graphene and metal could be an important advantage in thermal management. All these remarkable properties make graphene a promising candidate material for a pellicle. However, the chemical stability of graphene during EUV exposure is of critical importance for lifetime considerations, and is not yet fully understood.

In this paper, we focus on the investigation of chemical stability of graphene layers under EUV irradiation. Multi-layer and single layer graphene on different substrates (Ni, Cu, SiO2), as well as suspended single-layer graphene, were investigated. Our results show that defects were created in graphene after EUV irradiation. The experimental data demonstrate that, under EUV radiation in the presence of residual water in the exposure chamber, defects were generated through reaction with water, resulting in the graphene being etched, forming cracks and holes. The reaction process originates from the dissociation of water by EUV. In addition, the defect density was found to be proportional to the water partial pressure in the exposure chamber.

By introducing a physical barrier (naturally accumulated hydrocarbon on graphene) between the graphene and residual gas, it was found that EUV photons and photoelectrons directly generate defects in graphene also. To understand if the defects are photo-generated, or electron-generated, an electron gun system was used to mimic the abovementioned photoelectrons (3.7 eV-80 eV) emitted from the substrate. Depending on the flux and electron energy, an increase in defects was observed. However, the observed defect density is, in this case, not dependent on the water partial pressure. It was concluded that low energy electrons (photoelectrons) can directly break sp2 bonds, which will induce defects in graphene.

Based on our experimental data, we conclude that at relatively high water partial pressure (1x10^-5 mbar) in the exposure chamber, residual water gases, dissociated by the absorption of EUV, is the main source of defects. Both EUV photons and photoelectrons can generate defects directly, but this mechanism only dominates in relatively good vacuum conditions. Our results help develop lifetime predictions for graphene-based pellicles.

9235-45, Session PS2

Phase and amplitude measurements of EUV masks

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Mask roughness at 13.5-nm-wavelength has been examined using actinic scatterometry to show that the effective roughness is generally less than the roughness measured by AFM, however reflectivity variations were not measured [1]. We have developed a method using through-focus image data, collected on an EUV microscope to extract both effective phase and effective amplitude roughness (reflectivity variation) of the reflective multilayer coating. Additionally, because the roughness

is extracted from images, the phase and amplitude roughness measured are aligned to each other, so the relationship between the two can be examined. Several EUV masks have been measured on SHARP, an EUV microscope at Lawrence Berkeley National Laboratory [2]. The masks have varying substrate roughness that was measured using AFM before and after multilayer deposition and using EUV scatterometry.

The effective roughness is recovered from images using a new iterative algorithm designed to handle partial coherence and varying illumination. The algorithm takes advantage of the strong DC reflectivity in the image of the mask blank to perform a type of on-axis interferometry. The relatively weak perturbations from the DC, that the roughness produces, results in fast convergence of the algorithm allowing many images to be combined into one reconstruction. The algorithm is an extension of previous work modeling the speckle caused by the roughness [3].

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9235-46, Session PS2

Impact of B4C capping layer for EUV mask on the sensitivity of patterned mask inspection using projection electron microscope

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B4C is one of candidate for capping layer of multilayer (ML) in EUV mask due to its better chemical, mechanical and electrical resistance and optical properties than Ru.

We have been developing a projection electron microscope (PEM) for patterned EUV mask and we have evaluated its feasibility. PEM has an advantage of giving a considerably higher throughput than achievable in the case of conventional scanning electron microscope (SEM) type inspection system, because PEM probes sample target with areal illumination, whereas SEM probes it with spot beam.

We already reported that 16 nm sized defect on hp 64 nm mask pattern was detectable with 10 times higher signal intensity than the standard deviation by using PEM technique when the Ru capping layer was used in EUV mask. It was also found that the sensitivity of defect detection was predictable by measuring the secondary electron yield curves of Ta based absorber layer and Ru capped ML.

In this paper, we investigated the secondary electron yield curves of B4C capped ML, and analyzed the optimal condition of patterned mask inspection using PEM technique. The overall secondary electron yield of B4C was smaller than that of Ru. And the conductivity of B4C capped ML was good enough to suppress the image degradation due to charging effect. Therefore, the pattern contrast of the B4C capped ML and absorber layer was 1.5 times higher than the case of using Ru capped ML. Simulation results suggested that the sensitivity of 16 nm sized defect detection in the case of B4C was higher than that in the case of Ru capping layer These results indicate that B4C capping layer has an advantage for high sensitivity of patterned mask inspection besides its good durability.

9235-47, Session PS2

Recent results from EUVL patterned-mask inspection using projection electron microscope system

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Extreme Ultraviolet Lithography (EUVL) stands as the foremost next-generation lithographic technology after the ArF immersion lithography has reached its limit to deliver smaller features. EUVL mask pattern defect detection is one of the major issues to realize device fabrication with EUV lithography. As prescribed by the ITRS2013 and based on defect printability simulation, the sensitivity requirement for EUV patterned mask inspection system at sub-14 nm nodes is investigated.

We have designed a novel Projection Electron Microscopy (PEM) system, which appears to be quite promising for hp 1Xnm node mask inspection. For the illumination optics, an electron beam is generated from a photoelectron source, and then the beam is deflected by a beam separator to illuminate the surface of an EUVL Mask. The mask pattern image, by scattered electrons, is focused on a time-delay integration (TDI) image sensor through the projection optics. In scanning the full area during a mask inspection, the mask is scanned in Y direction, and its swath image on TDI sensor is captured when operating in its TDI mode. By repeating the step and scan movement, the full mask area can be inspected. The illuminated area is sufficiently large to cover the entire sensor area, which relaxes the limitation of resolution by space charge effect, a serious issue with SEM (Scanning Electron Microscopy) system. Currently, the PEM optics is integrated with the pattern inspection system for the defect detection sensitivity evaluation. Model EBEYE-V30 ("Model EBEYE" is an EBARA's model code) inspection system has a high-resolution and high-throughput electron optics. To observe the PEM optics system, its potential for making to the 1X nm node have been addressed by evaluating its die-to-die defect detection sensitivity. A programmed defect mask was used for demonstrating the performance of the system. Defect images were obtained as difference images by comparing PEM images with-defects to the PEM images without-defects. The image-processing system was also developed for die-to-die inspection. A targeted inspection throughput of 19-hour inspection per mask with 16 nm pixel size for hp 16 nm node defect detection was attained.

In this paper, we described targeted defect detection size and show the specification of sub-14-nm node PEM system and verification. Moreover, we also reported on the recent results of EUVL patterned mask inspection using the developing PEM system, and we discuss the systems extendibility to sub-14-nm node defect detection with system improvements in the PEM optics, image capturing unit, and defect detection signal processing.

This study is supported by New Energy and Industrial Technology Development Organization (NEDO) and Ministry of Economy, Trade and Industry (METI).

9235-48, Session PS2

Determination of line profile on nanostructured surfaces using EUV and x-ray scattering

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According to the International Technology Roadmap for Semiconductors

(ITRS), dimensional metrology solutions for technology steps beyond the currently launching 22 nm-node are insufficient or not even known. Non-imaging solutions like X-ray scattering are supposed to play an important role. PTB has been working on the development of EUV scattering methods for the characterization of line structures on EUV photomasks for several years. We now commissioned a new versatile Ellipso-Scatterometer which is capable of measuring 6" size mask substrates in a clean, hydrocarbon-free environment with full flexibility regarding the direction of the polarization of the incident light. Small angle X-ray scattering (SAXS) in transmission geometry was performed at other facilities for silicon wafers but is not suited for thicker or non-crystalline substrates. In grazing incidence geometry (GISAXS), X-ray scattering is also applicable for photomasks. The photon energy can be adapted to the sample system, e.g. taking advantage of X-ray absorption edges to improve the contrast. At PTB, the available photon energy range extends from 50 eV up to 10 keV at two adjacent beamlines.

Besides characterizing EUV mask structures with a highly reflecting multilayer mirror underneath the absorber structures, we now demonstrated the feasibility to characterize gratings etched into silicon as a model of wafer-level structures and "chrome-on-glass" photomask structures with radiation in the spectral range from EUV to X-ray. The silicon test structures were fabricated with electron beam lithography with nominal values of 25 nm to 100 nm for the line width (CD) and a pitch down to 50 nm. We use a FEM-based Maxwell solver for the evaluation of the data, with respect to the geometrical parameters line width, line height, sidewall angle and corner rounding. A fast structure reconstruction is achieved by a reduced-basis approach for the FEM calculation in combination with a particle swarm optimizer. Using statistical procedures for the inclusion of roughness based on an effective Debye-Waller factor we also derive reliable estimates for the line roughness. Furthermore, discrete frequency contributions in the diffuse scatter intensity can be correlated to process parameters of the e-beam writer used for grating production. We demonstrate the respective advantages of measurements in different wavelength regimes and show that a multi-wavelength approach yields complementary information.

Results are part of the project IND17 within the European Metrology Research Programme (EMRP).

9235-49, Session PS2

Particle reduction and control in EUV etching process

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As the device design rule shrinks, photomask manufacturers need to have advanced defect controllability during the ARC ans ABS etch in the process of extrene ultraviolet (EUV) mask. Particle generated by plasma ignition in etch. Etching lead to defect which is an obstacle in ARC etch. Because plasma is stable from ARC etch to ABS etch, no defect is added in ABS etch.

We studied etching techniques of EUV absorber film that is composed of ARC and ABS to find out for the possibility of particle evasion. With In-Situ etching methode,the amount of defects generated during ABS film etching process could be reduced compared to standard etching process while properties of the in-situ EUV dry etching process technique for ARC and ABS,which reduces the defect level significantly.

Analysis tools used for this study are as follows, TEM(for cross-sectional inspection),SEM(for in-line monitoring) and OES (for checking optical emission spectrum)

9235-50, Session PS3

A reusable framework for data-mining mask shop tools

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The Semiconductor Communication Standard (SECS) is ubiquitous throughout the semiconductor industry for automating fab tool control and data collection. However, SECS automation is not in pervasive use within the mask shop for a variety of reasons.

Even in the best circumstances, the overhead required for robust SECS communication implementations is steep: specialized knowledge of the SECS protocol and related Generic Equipment Model (GEM), extensive testing to validate and understand a tool's SECS capabilities, development to implement a tool control interface and craft a translation layer to interact with the Manufacturing Execution System (MES), and a significant MES infrastructure for full automation integration. Even if the infrastructure pieces are in place, implementation timelines for SECS automation can be unpredictable and projects often wind up consuming much more time than planned.

Limitations specific to the mask shop further complicate SECS automation implementations. Many tools have no SECS messaging implementation at all, while many others provide only a minimal implementation emphasizing tool control. Some mask tools are modifications of their wafer fab cousins and have unreliable SECS implementations because mask shop-oriented tool modifications can conflict with the original (unmodified) wafer fab-oriented SECS implementation.

In the final analysis, only a subset of mask shop tools have adequate SECS communication implementations, and only a subset of those provide the ability beyond tool control for data collection and tool alarm/event-monitoring. So while it may be possible to control a mask shop tool using SECS communication, there is likely a wealth of data that languishes on mask shop tools virtually untapped and unused – data that could provide key insights toward improvements in tool performance, processes and utilization. The question is how to mine that data in a structured manner, and how to do so in a way that can be reused across different tools.

This paper discusses a generic, lightweight framework for mining data from mask shop tools using tool log files as the data source. Virtually all fab tools have log files that are used for diagnostic purposes by the tool vendor's software engineers, field service engineers, mask shop equipment technicians, and process engineers. The data in these files range from simple event information (i.e., run start and complete) to tool alarms (i.e., sensor set-point alarms, robot handling errors) to comprehensive telemetry information (i.e., raw data streams for temperature, pressure, humidity).

The paper describes a novel tool-based process that can efficiently monitor tool log files and be configured to detect specific events and trigger actions as they occur. A number of data-mining scenarios are discussed, including tool event and alarm detection and logging, tool utilization monitoring, telemetry data collection, and tool report identification and data extraction. Triggerable actions are also discussed, including simple event-logging, real-time data evaluation, data upload, and automated notifications. The paper also discusses the implications of running non-tool processes on tool workstations and the need to minimize process footprint to prevent adverse impacts to tool performance.

Finally, the paper proposes a generic log file format that equipment vendors can implement on both new and existing mask shop tools to simplify future efforts to unlock valuable tool data. The proposed generic log file would provide a consolidated, chronological sequence of tool events that improves system troubleshooting in the field; speeds mask shop tool data-mining implementations; and reduces equipment vendors' development costs by reducing or eliminating the need for SECS implementations for non-control scenarios.

The overarching message is that a formal SECS communication implementation is not the only method – and perhaps not the best method – to automate data collection from mask shop tools. There is another way that might just be better than SECS.

9235-52, Session PS4

Phase defect detection signal analysis: dependence of defect size and shape

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The influence of phase defects embedded in Extreme ultraviolet (EUV) mask blanks on wafer printing has always been a center of attention because the phase defects as small as 1.0 nm in height or depth are most likely to be printed on wafer at half-pitch 16 nm lines-and-spaces pattern [1]. To detect printable phase defect on the EUV mask blanks, several inspection techniques that employ EUV light or deep ultraviolet light have been developed [2, 3]. Among these techniques, an at wavelength dark-field inspection technique is a prime candidate for the EUV mask blank inspection method for 16 nm technology node [4].

In this study, to investigate the influence of shape and size of the phase defect on the defect detection signals of the at wavelength dark-field inspection system, we prepared programmed phase defect EUV mask blanks. The defect type was pit and the lateral shapes of the defects were square-shape and rectangular-shape (1 to 3 and 1 to 5 ratio) with orientations of 0, 45, 90, and 135 degrees. The designed sizes were from 14 to 100 nm (the short side). The defect sizes were measured, before and after coating the multilayer, using scanning prove microscope. The imaging optics of the dark-field inspection system utilized in this study consists of a concave and a convex mirror so-called a Schwarzschild optics. The optics has a magnification of 26X with its inner and outer numerical aperture of 0.1 and 0.27.

The experiment showed that the defect volumes on the multilayer were varied in accordance with the designed sizes. In addition, about 20 percent of variations in the defect volumes were also observed even if the variations in the defect volumes on the substrate were negligibly small. The defect detection signal intensities were strongly associated with the defect volumes. Besides, the 20 percent of variations in defect volumes on the multilayer as described above also caused fluctuations in the defect detection signal intensity. As a result, the at wavelength dark-field inspection system can predict the small variations of the defect volumes.

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9235-53, Session PS4

Best-practice evaluation methods for wafer-fab requalification inspection tools

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Requalifying semiconductor photomasks remains important and is increasingly challenging for 20nm and 14nm node logic reticles. Patterns are becoming more complex on the photomask, and defect sensitivity requirements are more stringent than ever before. Reticle inspection tools are critically important to effective process development and the successful ramp and sustained yield for high volume manufacturing. These tools are all expensive but are differentiated in terms of performance and throughput as well as extendibility. Performing a thorough evaluation and making a technically sound choice which explores these many factors is critical for success of a fab. This paper examines the methodology for evaluating two different photomask inspection tools. The focus is on ensuring production worthiness on real and advanced product reticles as well as evaluating sensitivity and throughput on those product reticles. Finally, the “ultimate” test is described that evaluates how the tools would perform in a real production use-case on a contaminated plate. This unique test unveils the performance differentiation that leads to the final decision.

9235-54, Session PS4

Automatic classification of blank substrate defects

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Mask preparation stages are crucial in the development of a mask, since this mask is to later act as a template for considerable number of dies to be manufactured. The presence of any defects on the initial blank substrate, and subsequent cleaned and coated substrates, can have a profound impact on the usability of the finished mask. This emphasizes the need for early and accurate identification of blank substrate defects. Detailed information on these defects helps select appropriate job-decks to be written on the mask by defect avoidance tools.

Automatic Defect Classification (ADC) is a well-developed technology for inspection and measurement of defects on patterned wafers in the semiconductors industry. For blank mask inspection though, ADC is in very early stages. Calibre NxADC is a powerful analysis tool for fast, accurate, consistent and automatic classification of defects on blank masks. Accurate classification leads to better usability of masks by avoiding critical defects while writing the pattern on mask. The inspection tool operator manually examines each defect and classifies based on a set of predefined rules and human judgment. The automated classification approach avoids the inconsistency due to subjectivity of humans.

Smart algorithms separate critical defects from the potentially large number of non-critical defects or false defects. The blank mask is inspected at specific steps where blank defects could be transferred to the imaged mask pattern. The ADC engine retrieves the transmitted and reflected images produced by the mask blank inspection tools for the classification. Some mechanisms adopted by Calibre NxADC to identify and characterize defects include location and defect size, defect polarity (opaque, clear) in transmitted and reflected images, distinguishing defect signals from background noise in defect images. The Calibre NxADC engine then uses a decision tree approach for classification of defects.

This paper focuses on the results from the evaluation of Automatic Defect Classification (ADC) product at MPMask for the 25nm technology node. Improvements in blank inspection capability allow the detection of increasing numbers of defects, all of which need to be analyzed in order to identify any critical defects. The Blank ADC tool was qualified on high volume production mask blanks against the manual classification. The classification accuracy is greater than 95% for critical defects with an overall accuracy of 90%. The sensitivity to weak defect signals and locating the defect in the images is a challenge we are resolving. The performance of the tool is proven on multiple mask types and is ready for deployment in full volume mask manufacturing production flow. Implementation of Calibre NxADC at MPMASK is projected to reduce the misclassification of critical defects by 80%, resulting in reductions in repairs, rework and scrap.

9235-75, Session PS4

Study of high-sensitivity DUV inspection for sub-20nm devices with complex OPCs

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EUV lithography has been delayed due to well-known issues (such as source power, debris, pellicle, etc) for high volume manufacturing. For this reason, conventional optical lithography has been developed to cover more generations various kinds of Resolution Enhancement Techniques (RETs) and new process technology like Multiple Patterning Technology (MPT). Presently, industry lithographers have been adopting two similar techniques of the computational OPC scheme such as Inverse Lithography Technology (ILT) and Source Mask Optimization (SMO). Sub-20 nm node masks including these technologies are very difficult to fabricate due to many small features which are near the limits of mask patternning process. Therefore, these masks require the unseen level of difficulty for inspection. In other words, from the viewpoint of mask inspection, it is very challenging to maintain maximum sensitivities on main features and minimum detection rates on the Sub-Resolution Assist Features (SRAFs). This paper will describe the proper technique as the alternative solution to overcome these critical issues with Aerial Imaging (AI) inspection and High Resolution (HR) imaging inspection.

9235-25, Session PS5

Development and characterization of advanced phase-shift mask blanks for 14nm node and beyond

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Recently, the development of semiconductor process for 14nm node and beyond is in progress. The mask-making process demands higher resolution and CD accuracy to meet requirements. Current conventional ArF PSM has several problems such like higher 3D effect and higher loading effect due to the thicker film. These problems cause the CD performance degradation.

This study is about the manufacturing of advance ArF PSM, which has thinner phase shift layer and higher etch rate Cr absorber film. The thickness of phase shift film is less than 56nm and the total etch-time for the Cr absorber film is reduced more than 30%.

The mask CD performance of this new blank was evaluated in terms of CD uniformity, CD linearity, pattern resolution, and loading effect and so on. Adapting this new blank, we can achieve the better CD performance by reducing the loading effect. In addition, the chemical durability and ArF exposure durability were also improved.

In conclusion, the mask-making process margin was extended by using this new blank, and it is expected that we can achieve the required specifications for 14nm node and beyond.

9235-55, Session PS5

New grade of 9-inch size mask blanks for 450mm wafer process

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6-inch size (known as 6025QZ) binary Cr mask is widely used in the semiconductor lithography for over 20years. Recently for the 450mm wafer process, high grade 9-inch size mask is expected. For this application, we have studied and developed new grade 9-inch size mask blanks for recent 450mm wafer process requirement.

There are three types of glass substrates material use and select as 9inch size mask blanks and for required applications by the users.

Each glass material has advantage and disadvantage for lithography process as well as wafer process.

By knowing the each glass substrate material characteristics and quality level the users enable to select the proper 9inch mask blanks for their targeting applications.

9235-56, Session PS5

The feasibility of the additional process for improving pattern collapse in develop process

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As EUV Lithography has been delayed because of technical difficulties, ArF-immersion technology is seen to be utilized in future years. To progress constantly chip's miniaturization with ArF, the adoption of too many SRAF is inevitable. this trend is giving the big challenge in Photomask industry such as pattern collapse, pattern wiggling. we studied the way to decrease surface tension by using the surfactant at drying step in develop process and verified the effect of this process on preventing pattern collapse

9235-57, Session PS5

Bringing mask repair to the next level

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Mask repair is an essential step in the mask manufacturing process as the extension of 193nm technology and the insertion of EUV are drivers for mask complexity and cost. The ability to repair all types of defects on all mask blank materials is crucial for the economic success of a mask shop operation. In the future mask repair is facing several challenges. The mask minimum features sizes are shrinking and require a higher resolution repair tool. At the same time mask blanks with different new mask materials are introduced to optimize the mask regarding optical performance and long term durability. For EUV masks new classes of defects like multilayer and phase defects are entering the stage. In order to achieve a high yield, mask repair has to cover etch and deposition capabilities and must not damage the mask. These challenges require sophisticated technologies to bring mask repair to the next level. For high end masks ion-beam based and e-based repair technologies are the obvious choice when it comes to the repair of small features. Both technologies have their pro and cons. The scope of this paper is to review and compare the performance of ion-beam based mask repair to e-beam based mask repair. We will analyze the limits of both technologies theoretically and experimentally and show mask repair related performance data. Based on this data, we will give an outlook to future mask repair tools.

9235-76, Session PS5

The patterned ferre-electrics for optical designs

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The patterned ferroelectrics with domain modulation can be fabricated by the electric field poling technique, for example, the periodic poling LiNbO3 crystal (PPLN) was widely used for quasi-phase-matched (QPM) optical parametric interaction. Conventionally in order to realize the integration of multiple optical functions, such as second harmonic generation (SHG), splitting and focusing, two domain modulated crystals are needed: the first one for SHG and the second one for splitting and focusing of SHG through external voltage using electro-optic effects. Can we integrate such optical effects in patterned domain materials without electro-optic effect?

Transverse patterning of periodic gratings for QPM at the micron scale leads to a multitude of nonlinear optical devices based on familiar physical optics effects. The spatial control over the amplitude and phase of a second-harmonic beam in multiple slit diffraction devices and in QPM lenses has been demonstrated. [1] The method above is simple and efficient for single beam focusing because of the known fact that ideal thin lens has parabolic phase forms. However, due to its semi-empiricism, the designing method will be confronted with difficulties when more optical functions (for example, dual SH beam splitting and focusing) and more complicated domain structures are needed.

For QPM to be realized, the wave vectors (including G) should be all well defined. If not, would it be possible to develop a method with which nonlinear optical processes can be realized efficiently? Actually QPM will be out of work when wave vectors (including G) are temporal or spatial dependant. We proposed the full theory and technique to solve this problem.

9235-58, Session PS6

Further beyond: registration and overlay control enhancements for optical masks

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Mask registration control is one of the key performance specifications during the mask qualification process. It is becoming an important factor for yield improvement with the continuously tightening registration specs driven by tight wafer overlay specs. Understanding the impact of miss classified masks on the final wafer yield is gaining more and more attention especially with the appearance of Multiple Patterning Technologies where mask to mask overlay effect on wafer is heavily influenced by mask registration.

ZEISS has established a promising close loop solution implemented in the mask house, where the PROVE® system – a highly accurate registration and overlay metrology measurement tool is being used to feed the RegC® - a registration and mask to mask overlay correction tool that can also accurately predict the correction potential in advance. The well-established RegC® process is typically demonstrating 40-70% improvement of the mask registration/overlay error standard deviation. The PROVE® - RegC® close loop solution has several advantages over alternative registration control methods apart of the mask re-write saving. Among the advantages is the capability to correct for pellicle mounting registration effects without the need to remove the pellicle.

This paper will demonstrate improved method for enhanced mask to mask overlay control which is based on a new scheme of data acquisition and performance validation by the PROVE®. The mask registration data as well as additional mask information will be used to feed the correction process. Significantly improved mask to mask overlay correction results will be discussed and presented in details.

9235-59, Session PS6

New critical dimension uniformity inspection method for multi-die logic reticles

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Critical Dimension Uniformity (CDU) control plays a critical role in maintaining the size of the process window for semiconductor lithography. However, until now there have been limited solutions to characterize CDU effectively for logic plates, especially in the wafer fab. A new method for characterizing the Critical Dimension Uniformity (CDU) of multi-die reticles without the use of the design database is described. This approach has been evaluated and compared to wafer print with good correlation results. With the use of a threshold on this high density CDU map, this approach can act as both an incoming quality control (IQC) measure in the wafer fab and as an outgoing quality control (OQC) measure in the mask shop. Reticles that fail the CDU spec should be rejected by the wafer fab to ensure good process yield. Using this approach to characterize reticles in the mask shop should allow process improvement to deliver superior mask quality. Indeed failure to capture some of these yield limiting defects can lead to end of line electrical test failures as there is no other solution inline to capture such regions of interest.

9235-60, Session PS6

A method of utilizing AIMS to quantify lithographic performance of high-transmittance mask

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EUV(Extreme Ultraviolet) Lithography has been delayed caused by several technical problems such as EUV mask , source power and etc,. So ArF immersion lithography has been continued with adopting new technology. Especially, the lithography of wafer is tend to increase rapidly NTD(Negative Tone Develop) process for overcoming high resolution such as small hole type patterns. For wafer NTD process, pattern shape in mask has changed from hole patterns to dot patterns. For NTD process in wafer, Local CD Uniformity of Areal Image becomes tighter than normal PTD(positive tone Develop) process because half-pitch is getting shrink. In this paper , we studied Local CD uniformity of Areal image between high transmittance HT-PSM and conventional 6% HT-PSM aerial images from AIMS tool. Additionally, several cell sizes were analyzed to find an optimum target cell size which has good wafer performance and AIMS aerial image. And we analyzed NILS factor which represent wafer photolithographic performance. Furthermore, we analyzed not only AIMS NILS simulation, but also wafer lithographic performance.

9235-61, Session PS6

On the benefit of high resolution and low aberrations for in-die mask registration metrology

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With the introduction of complex lithography schemes like double and multi – patterning and new design principles like gridded designs with cut masks the requirements for mask to mask overlay have increased

dramatically. Still, there are some good news too for the mask industry since more mask are needed and qualified. Although always confronted with throughput demands, latest writing tool developments are able to keep pace with ever increasing pattern placement specs not only for global signatures but for in-die features within the active area. Placement specs less than 3nm (max. 3 Sigma) are expected and needed in all cases in order to keep the mask contribution to the overall overlay budget at an accepted level. The qualification of these masks relies on high precision metrology tools which have to fulfill stringent metrology as well as resolution constrains at the same time.

Furthermore, multi-patterning and gridded designs with pinhole type cut masks are drivers for a paradigm shift in registration metrology from classical registration crosses to in-die registration metrology on production features. These requirements result in several challenges for registration metrology tools. The resolution of the system must be sufficiently high to resolve small production features. At the same time tighter repeatability is required. Furthermore, optical proximity effects, tool induced shift (TIS) limit the accuracy of in-die measurements.

This paper discusses and demonstrates the importance of low illumination wavelength together with low aberrations for best contrast imaging for in-die registration metrology. Typical optical effects like optical proximity and tool induced shift are analyzed and evaluated using the ZEISS PROVE® registration metrology tool,

Additionally, we will address performance gains when going to higher resolution The direct impact on repeatability for small features by registration measurements will be discussed as well.

9235-62, Session PS7

Using rule-based shot dose assignment in model-based MPC applications

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Shrinking feature sizes and the need for tighter CD (Critical Dimension) control require the introduction of new technologies in mask making processes. One of those methods is the dose assignment of individual shots on VSB (Variable Shaped Beam) mask writers to compensate CD non-linearity effects and improve dose edge slope. Using increased dose levels only for most critical features, generally only for the smallest CDs on a mask, the change in mask write time is minimal while the increase in image quality can be significant.

This paper describes a method combining rule-based shot dose assignment with model-based shot size correction. This combination proves to be very efficient in correcting mask linearity errors while also improving dose edge slope of small features.

Shot dose assignment is based on tables assigning certain dose levels to a range of feature sizes. The dose to feature size assignment is derived from mask measurements in such a way that shape corrections are kept to a minimum. For example, if a 50nm drawn line on mask results in a 45nm chrome line using nominal dose, a dose level is chosen which is closest to getting the line back on target. Since CD non-linearity is different for lines, line-ends and contacts, different tables are generated for the different shape categories.

The actual dose assignment is done via DRC rules in a pre-processing step before executing the shape correction in the MPC engine. Dose assignment to line ends can be restricted to critical line/space dimensions since it might not be required for all line ends. In addition, adding dose assignment to a wide range of line ends might increase shot count which is undesirable. The dose assignment algorithm is very flexible and can be adjusted based on the type of layer and the best balance between accuracy and shot count. These methods can be optimized for the number of dose levels available for specific mask writers.

The MPC engine now needs to be able to handle different dose levels and requires a model which accurately predicts mask shapes at all dose levels used. The calibration of such a model is described in a separate paper.

In summary this paper presents an efficient method for combining rule-based VSB shot dose assignment with model-based shape corrections in MPC. This method expands the printability of small features sizes without the need for increasing the base dose of the e-beam writer which reduces backscattering and increases the lifetime of the electron gun of the writer.

9235-63, Session PS7

Short feedback loop for OPC model based on wafer level CD

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Optical proximity correction (OPC) allows the accurate prediction of wafer printing results based on geometrically defined features. The idea of OPC modelling is that the wafer printing result is identical with simulation data. However, there is a challenge to achieve this demand considering the influence of reticle, resist and etch performance. OPC model build is to minimize the deviation between simulated edge-placement-errors (EPE) and empirical EPE. The empirical EPE is from both, reticle and wafer data. The wafer level critical dimension (WLCD) technique can significantly improve and fasten the OPC model building, if the correlation between WLCD and wafer CD is good. In this work, the CD correlation between WLCD and wafer CD for OPC model building is quantified. In addition, the correlation between WLCD and wafer CD for different dummy effects will also be illustrated. Different mask blanks contribute to the wafer CD and WLCD data are presented from a phase shift mask (PSM) and an advance binary mask. The effect of different layout mythologies to the correlation will be presented.

9235-64, Session PS7

Shot overlap fracturing of pixel-based OPC layouts

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Resolution enhancement techniques such as Optical Proximity Correction (OPC) have enabled the semiconductor manufacturing industry to continuously shrink the critical dimension of integrated circuits. However, these techniques result in increasingly complex masks leading to excessively long mask write times. In previous work, we have proposed model-based shot overlap fracturing algorithms for layouts resulting from both pixel-based and edge-based OPC. In doing so, we minimized shot count by optimizing for shot location, size, and dosage from the target mask and manufacturing model parameters.

A major limitation of our previous solution for model based fracturing of pixel-based layouts is its computational complexity. In this work we aim to alleviate this by converting a pixel based OPC layout into a rectilinear mask in order to apply our previously developed model based fracturing algorithms originally designed for edge based OPC layouts. Thus, the first step of our proposed method consists of converting the pixelated layout from a pixel based OPC solution into a Manhattan layout, with only 90 degree corners. This is done by gridding the pixelated layout; however, since there are many possibilities for the location of the center of the grid, to keep computational complexity low, we need to develop machinery to choose the best center location without exhaustively fracturing the resulting layout for each center location. To do so, we opt to use a machine learning algorithm to predict the best grid center location resulting in minimum shot and smallest pattern fidelity error. The training step of the proposed method consists of (a) creating a training set by taking various pixelated layouts, (b) considering all Manhattan versions of the layout by shifting the center of the grid, and (c) finding the fracturing for each shifted version. During this training we record various

input features such as minimum and maximum edge lengths, number of corners, difference between the true pixel layout and the Manhattan layout, and area of the Manhattan layout. After applying the model based fracturing algorithms for edge based OPC to the resulting Manhattanized layout, we record the number of shots and quality of the fracturing as the output features.

Next, we design a linear predictor to relate the input features to the output features for the training set by using the cross-covariance and auto-covariance of the input and output features. To apply the linear predictor to a new test layout resulting from pixel based OPC, we first generate all possible Manhattan versions of the pixelated layout and extract the input features. Next, we use our linear predictor to predict the number of shots and mask error for each possible grid center. We then take the top K candidates among all possible grid center locations and compute the true rectilinear model based fracturing for each of them. This is the most computationally expensive step of our overall pixel based fracturing algorithm. The "top" candidates can be chosen either in terms of shot count or mask fidelity metrics. Finally, we select the candidate with the fewest shots or lowest mask error among the top K depending on the chosen metric.

We have tested our proposed algorithm on a small SRAM clip with 400 polygons and compared results with (a) Manhattanizing without optimizing for the grid center, and (b) with the best possible grid center obtained exhaustively that results in the fewest shots. Assuming K=5, our approach has 15% fewer shots than (a) and 13% more shots than (b). The computational complexity of our approach is K=5 times higher than (a) and 20 times lower than (b). We additionally compared our proposed algorithm with random selection of the center of the grid and found that on average it results in 3% fewer shots; it also results in a lower shot count than 80% of the random selection solutions.

9235-65, Session PS7

Efficient model-based dummy-fill OPC correction flow for deep sub-micron technology nodes

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Dummy fill insertion is a necessary step in modern semiconductor technologies to achieve homogeneous pattern density per layer. This benefits several fabrication process steps including but not limited to Chemical Mechanical Polishing (CMP), Etching, and Packaging. As the technology keeps shrinking, fill shapes become more challenging to pattern and require undergoing aggressive model based optical proximity correction (MBOPC) to achieve better design fidelity. MBOPC on Fill is a challenge to mask data prep runtime and final mask shot count which would affect the total turnaround time (TAT) and mask cost.

In our work, we introduce a novel flow that achieves a robust and computationally efficient fill handling methodology during mask data prep, which will keep both the runtime and shot count within their acceptable levels. In this flow, fill shapes undergo a smart MBOPC step which leads to improving the final wafer printing quality and topography uniformity without degrading the final shot count or the OPC cycle runtime. This flow is tested on both front end of line (FEOL) layers and backend of line (BEOL) layers, and results in an improved final printing of the fill patterns while consuming less than 2% of the full MBOPC flow runtime.

9235-66, Session PS7

Calibration and application of a DSA compact model for grapho-epitaxy hole processes using contour-based metrology

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Significant interest from the integrated circuit (IC) industry has been placed on directed self-assembly (DSA) for sub 10nm nodes. DSA is being considered as a cost reduction complementary process to multiple patterning (MP) and an enabler of new technology nodes.

However, to realize the potential of this technology, it is essential to count with the necessary infrastructure from the point of view of materials, hardware, software, process integration and design methodologies which enable its deployment in large volume manufacturing.

One key aspect in enabling DSA processes is the ability to count with full chip mask synthesis and verification methods which mirror the functionality of existing tools used in production. One of those critical components is the ability to accurately model the placement of the target phases in the DSA process, as well as determining the conditions at which unwanted phase transitions start to occur.

Self-consistent field theory and Monte Carlo simulators have the capability to probe and explore the mechanisms driving the different phases of a diblock copolymer system. While such methods are appropriate to study the nature of the self-assembly process, they are computationally expensive and they cannot be used to perform mask synthesis operations nor full chip verification.

The nature of a compact model is to make a series of approximations allowing a simpler description of the problem in a way that the phenomena of interest can be sufficiently captured even if it is at the expense of its generality.

In this case we focus our effort in establishing the minimum set of conditions that a compact model for the manufacture of contact holes using a grapho epitaxy process for a PS-PMMA diblock copolymer system needs.

By focusing in the phase of interest (i.e., cylinder forming conditions), it is possible to reformulate the problem in a phenomenological formulation which accounts for the interaction among cylinders, the volume fraction of the respective co-polymers and the interaction with the confinement walls.

As such, a 2D approximation to the 3D environment can be applied to simplify the representation of the DSA process. This enables the use of a 2D contour for compact model training and verification. Further simplification is not recommended due to the nature of the grapho-epitaxy guiding patterns (figure 1), where a simple CD measurement is not sufficient to capture the 2D environment of post routed contact patterns for sub 10nm nodes (figure 2).

In this paper, we will study the application of the DSA compact model to a via layer of imec's 7nm technology node standard cells. ArF immersion lithography will be used to pattern the guides, and the layout will be DSA compliant to determine the mask complexity as well as the sensitivity of the solution to mask biases for the contact layer.

9235-67, Session PS7

Efficient full-chip QA Tool for design to mask (D2M) feature variability verification

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Solutions to control Across Chip CD Variation are very important to IC designs, since it directly impacts the electrical timing and functionality of the designs. VLSI designs today include a rich variety of electrical devices (different gate oxide thicknesses, different threshold voltages, etc.) to provide the much needed flexibility to the chip designer. These devices occur at different proximities and different densities on a full chip design. Each of these devices has a separate technology specification that is manifested as a device dependent sizing, usually as a pre–OPC step. The pre-OPC step is performed on the full chip layout and it is critical to verify the original specification of the sizing is met because cases where the sizing is not met due to improper biasing, software

or coding bugs lead to additional device variability. In this paper, we describe a method for improving and ensuring OPC quality via a quantitative relationship between design specification and full chip post-OPC results. This is done by applying a spatial sampling technique with the aim of capturing the randomized representation of all the device types on the full chip. This method ensures device biasing control and yields promising results for capturing and reducing variation related to the OPC flow.

9235-68, Session PS7

Full-Flow RET creation, comparison, and selection

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Patterning using 193i patterning will continue mainstream use for the foreseeable future. This continues reliance on optimized illumination in order to meet increasingly strict patterning requirements. To meet these requirements, a new RET Selection flow has been built. This flow includes SMO, Mask synthesis to further tune the output mask, Verification, and Analysis. The entire flow is session based, allowing runs to be cloned, queued, and compared. The flow is built on a robust GUI framework featuring persistent database integration. The new SMO algorithm offers improved scalability using parallel implementation, and improved accuracy using thick mask modeling and resist models. An inverse lithography component allows large area patterns to be included for RET benchmarking purposes. Finally, the analysis and visualization stages of the flow allow a particular solution to be compared against other candidates using any image metric desired. Comparison metrics can be customized for layer and customer requirements. In this paper, we will summarize the key points of our new SMO algorithm, and show the flexibility of our flow using several testcases, highlighting the quality of solution, time to solution, and ease of use.

9235-69, Session PS8

Assessment of carbon layer growth induced by resists outgassing in multi e-beams lithography

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The development of multiple e-beam lithography equipment is seen as an alternative for next generation lithography. However, similarly to EUV lithography, this technology faces important challenges in controlling the contamination of the optics due to deposition of hydrocarbon layer induced by the outgassed chemical species from resist under electron bombardment. It is thus important to understand the mechanisms of the carbon layer growth and its links with resists formulations, e-beams characteristics and outgassed components.

The experimental setup built at LETI is designed to study the species outgassed by the resist under an electron bombardment and the hydrocarbon layer deposition induced by this outgassing. As shown in Figure 1, this setup consists of a high vacuum chamber in which an electron gun exposes a 100 mm wafer through a mimic. This mimic is a silicon membrane with micro-machined apertures that simulate the multiple parallel beams of the multi e-beam lithography tool optics system. A wafer stage moves the wafer under the electron to expose the resist at a suitable dose. The vacuum chamber is also equipped with a Quadrupole Mass Spectrometer (QMS) that monitors the resist outgassing. This monitoring is completed by an ex-situ analysis: the TD/GC/MS-FID (Thermo Desorption - Gas Chromatography coupled to Mass Spectroscopy and Flame Ion Detector) in order to identify the outgassed chemical components. The morphology of the hydrocarbon contamination layer deposited on the mimic has been characterized with a Scanning Electron Microscope (SEM) (see Figure 2) and its composition determined by X-Ray Photoelectron Spectroscopy (XPS).

This paper will report the influence on the contamination layer growth of various parameters such as e-beam current density, pressure of outgassed species surrounding the mimic, resists formulations and the addition of a top coat layer above the resist. This paper will also present the links between outgassing components and the resulting hydrocarbon layer deposition and give insights of the influence of the resists and the top coat formulations on the kinetic of the contamination layer growth.

The research leading to these results has been performed in the frame of the industrial collaborative consortium IMAGINE.

9235-70, Session PS8

General shot refinement technique on fracturing of curvy shape for VSB mask writer

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As a process node shrinks, the complexity of RET increases. Inverse lithography technique (ILT) is one of the promising technologies to improve the process window but still has not gone mainstream due to its complexity and corresponding cost increase of mask fabrication. This is especially true using a VSB mask writer because an ILT photomask consists of curvilinear shapes which cannot be fractured simply into rectangles, which is the elemental shot of a VSB mask writer.

Several methods have been proposed to fracture ILT curvilinear shapes into rectangles efficiently using the smoothing effect caused by the mask manufacturing process and they have achieved significant shot count reduction while taking the tolerance of edge placement error into account.

We had developed a pure geometric processing based fracturing algorithm for curvilinear shapes and we now extend it with a post-processing technique which refines the original shot arrangement using a model-based algorithm to improve its reliability and the pattern fidelity.

9235-71, Session PS9

Impact of reticle writing errors on the on-product overlay performance

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The on-product overlay specification and Advanced Process Control (APC) are getting extremely challenging particularly after the introduction of multi-patterning applications like Litho-Etch-Litho-Etch (LELE). While the Reticle Writing Error (RWE) contribution could be marginalized for quite some time in the layer-to-layer overlay budget, it will become one of the dominating overlay contributors when the intra-layer overlay budget is considered. While most of the overlay contributors like wafer processing, scanner status, reticle transmission, dose, illumination conditions drop out of the intra-layer overlay budget, this is certainly not the case for reticle to reticle writing differences.

In this work, we have studied the impact of the RWE on the on-product

overlay performance. We show that the RWE can be characterized by an off-line mask registration tool and the modelled results can be sent as feed-forward corrections to the ASML TWINSCANTM. By doing so, the overlay control complexity (e.g. send-ahead wafers, APC settling time) can be reduced significantly. Off-line characterization enables that all reticles virtually become equal after correction (at least to the level of correction capability of the scanner). This means that all higher order RWE contributions (currently up to a third order polynomial) can be removed from the fingerprint. We show that out of 50 production reticles (FEOL, 28-nm technology), 30% can be improved on residual level when non-linear feed-forward corrections are considered as well. The additional benefit of feeding forward linear corrections to the scanner is even higher: it is anticipated that a large portion of the APC variation might find its origin in the RWE contribution.

In order to send feed-forward corrections to the scanner, we obviously rely on the quality of the off-line RWE measurements. These measurements are usually provided by a registration tool at the mask shop. To secure the quality, an independent experimental verification test was developed to check if off-line RWE measurements can be used as feed-forward corrections to the scanner. The test has been executed on an ASML NXT: 1950i scanner and was designed such to isolate the reticle writing error contribution. The match between the off-line measurements and the experiment is striking.

9235-72, Session PS9

The defect printability study for 28nm mode mask

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For the volume mask production of 28nm node and beyond, the defect disposition specification is an important factor for mask process. With the scaling feature sizes and advanced resolution enhancement technologies, the study on the printability defects' evaluation, which determines whether mask defects have effect on the wafer and provides information of defect repair's quality to decrease repair risk, is a practical challenge for advanced mask manufacturers.

To get the better resolution about defect printability on wafer and the available specifications for defect disposition, various series of 28nm programmed defects were systemically made on different patterns mask, consisted of Line/Space and Contact/Via. The defect designed has multiple types (such as extrusion, intrusion, bridge, and shrink) and a range of sizes for each type (from 4 nm to 120 nm in 4 nm increments). The AIMS, predicting the lithographic imaging performance without wafer printability, is the industry standard for the mask repair verification and used to emulate the patterns with programmed defects printability, accompanied with the immersion scanner, presenting the actually effects of programmed defect on wafer, and the CDSEM, measuring the CD of patterns with programmed defects on mask and wafer. In brief, the programmed defect on the mask were measured by AIMS , and printed on wafer. The analysis curve is the combination of the programmed defects status on wafer and AIMS, resulting from the comparison defect patterns with corresponding normal ones.

Based on the analysis of various defects' printability, we systemically established a series of specifications for different mask patterns to qualify the mask patterns and verify the repair process. it is found that the defect printability specification is an effective and industrialized approach to perform mask defect qualification for production.

9235-73, Session PS9

Characteristics and issues of haze management in a wafer fabrication environment

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The haze nucleation and growth phenomenon on critical photomask surfaces has periodically gained attention as it has significantly impacted wafer printability for different technology nodes over the years. A number of process solutions have been promoted in the semiconductor industry which has been shown to suppress or minimize the propensity for haze formation, but none of these technologies can stop every instance of haze. Fortunately, a novel technology which uses a dry (no chemical effluents) removal system, laser-based, through pellicle process has been reported recently. The technology presented here avoids many of the shortcomings of the wet clean process mentioned previously. The dry clean process extends the life of the photomask; maintains more consistent CD's, phase, and transmission; avoids adjustment to the exposure dose to account for photomask changes, reduces the number of required inspections and otherwise improves the efficiency and predictability of the lithography cell.

We report on the performance of photomask based on a design developed to study the impact of metrology variations on dry clean process. In a first step we focus on basic characteristics: CD variation, phase, Cr/MoSi transmission, pellicle transmission, registration variations. In a second step, we evaluate haze removal and prevention performance and wafer photo margin. Haze removal is studied on the masks for several haze types and various exposure conditions. The results of this study show that some of metrology variation likely to be a problem at high technology node, and haze removal performance is determined whether the component of haze.

9235-74, Session PS9

Qualification of local advanced cryogenic cleaning technology for 14nm photomask fabrication

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Challenges in Photomask cleaning have gotten substantially more difficult. The march toward tighter design rules, and thus smaller defects, has resulted in very different surface adhesion issues than in past generations. Current state-of-the-art wet clean technologies utilize functional water and various energies in an attempt to produce similar yield to the acid cleans of previous generations, but without some of the negative side effects. Still, wet cleans have continued to be plagued with issues such as persistent particles and contaminations, SRAF and feature damage, leaving contaminants behind that accelerate photo-induced defect growth, and others.

Cryogenic (cryo) cleaning technology utilizes a physical momentum transfer from carbon dioxide snow particles to clean reticles. Cryogenic cleaning has showed promise in the past to overcome the issues associated with wet cleans, and to have value as a complementary cleaning technology. However, cryogenic cleaning has had its own issues including: the size of snow particles has been too large to clean inside tight lines and spaces (particularly for Nanomachining debris removal); deposition of hydrocarbons on the reticle owing to the fact that CO2 acts as a solvent for hydrocarbons (HC) and particle adders causing yield failures both from defectivity and feature damage that can result when large particles become entrained in the CO2 stream and accelerated to the surface of the Photomask.

This paper details work done through design of experiments (DOE) to qualify an improved cryogenic cleaning technology for production in the Advanced Mask Technology Center (AMTC) advanced production lines for 20 and 14 nm processing. All work was conducted at the AMTC facility in Dresden, Germany using technology developed by Eco-Snow Systems and RAVE LLC for their VC1200 platform. The system uses gaseous CO2 to reduce snow particle size, extensive filtering to remove hydrocarbons and avoid particle adders, and other technologies to overcome the prior limitations of cryogenic cleaning. AMTC has successfully qualified this technology and is using it regularly to enhance production yields even at the most challenging technology nodes.

9235-16, Session 6

PMJ Best Paper: In-die registration measurement using novel model-based approach for advanced technology masks *(Invited Paper)*

Shunsuke Sato, Toppan Printing Co., Ltd. (Japan)

No Abstract Available

9235-17, Session 6

The intra-field CDU map correlations between SEMs and aerial images

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The reticle critical dimension uniformity (CDU) is considered one of major sources to wafer CDU which include both inter-field CDU and intra-field CDU. Generally, the wafer critical dimension (CD) measurement sample of inter-field CDU is much less than intra-field CDU. The intra-field CDU correction contributes to the time-consuming of metrology tool. In order to improve wafer intra-filed CDU, several methods can be applied as intra-field dose correction to improve wafer intra-field CDU which can be divided to CDs and aerial images. Reticle CDU map and wafer CDU map is in the scanning electron microscope (SEM) metrology level, and reticle inspection intensity map and wafer level critical dimension (WLCD) is in the aerial images or optical level. Reticles inspectors can offer the ability to collect optical measurement data such as KLA and NuFlare to get optical CDU map. WLCD of Zeiss is implemented the same illumination condition as scanner to measure the aerial images or optical CD. In this work, the CDU map correlation will be demonstrated for reticle CD, wafer CD, optical CD, and WLCD. In addition, different mask blank and patterns contributes to the CDU map correlation will also be illustrated.

9235-18, Session 7

Imaging impact of multilayer tuning in EUV masks: experimental validation

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The EUV mask has a significant impact on EUV imaging performance, i.e., a larger horizontal-vertical print difference due to shadowing and larger pattern placement errors. In the current binary mask technology the reflective multilayer coating is optimized for incident EUV light at 6deg, the chief-ray angle for the currently available full-field EUV scanners from ASML. When used with extreme off-axis illumination and larger chief-ray angles to push the resolution limit, the multilayer coating has to deal with a wider range of incidence angles. The non-telecentricity at mask level will manifest itself at wafer level as a pattern shift through focus [1].

Simulations using a calibrated binary mask stack model [2] predict a strong increase in pattern shifts through wafer focus for pitches at the resolution limit of NA > 0.25. Our study showed that this telecentricity error can be reduced by tuning the multilayer period by ~2%. Based on this work we suggested that a binary mask with an alternate multilayer period be used to validate experimentally its telecentricity impact mitigation on imaging at NA 0.25 and beyond.

A dedicated binary mask with a tuned multilayer has been fabricated using a high-resolution mask process to ensure aggressive line/space patterning in the absorber down to 10nm half-pitch (1X). The mask characterization in terms of mask linewidth, absorber profile, multilayer reflectivity and diffractometry at various mask incidence angles, is used to improve the mask stack model in the simulator. Wafer level verification is obtained on imec's NXE:3100 scanner operating at NA 0.25 and on the SHARP (SEMATECH high-NA actinic reticle review project [3]) microscope at NA > 0.3. Furthermore, we developed a single exposure methodology to measure pattern shift through focus on wafer of a resolution pitch relative to a larger reference pitch (see Fig. 1).

In this work we will present the experimental characterization of telecentricity errors at wafer level through pitch for an NA range of 0.25 to 0.50. Fig. 2(a) shows the experimentally measured pattern shift through wafer focus for 54nm pitch relative to a reference pitch of 162nm obtained from exposure of the tuned-multilayer mask at NA0.25 using Dipole Y illumination. The corresponding simulation result using a calibrated mask stack model shown in Fig. 2(b) is in qualitative agreement with the measured data. By incorporating exposure tool specific information (measured pupil and aberrations) in the simulator we will show improvement on the correlation. Furthermore, the simulations show that this relative pattern shift is mainly induced by the larger reference pitch, partly because the multilayer was tuned for near resolution imaging at 0.42 NA. Lastly, we will also demonstrate the impact of multilayer tuning on shadow biasing and best-focus behavior through pitch.

In this work we experimentally demonstrate that by actively tuning the periodicity of the multilayer in the EUV mask we can manipulate the EUV-specific pattern shift through focus, with minor impact on other imaging metrics such as best focus and shadow biasing. By means of diffractometry, scanner exposures and SHARP measurements the EUV mask stack model is validated for use in a rigorous mask 3D simulator to enhance the predictability of the imaging behavior of binary mask stacks at NA 0.25 and 0.33. Moreover, this investigation allows a more realistic imaging exploration of mask technologies for use at high-NA EUV (> 0.33NA).

[1] J. Ruoff et al., Proc. SPIE 7823 (2010) 782341.

[2] V. Philipsen et al., Proc. SPIE 8886 (2013) 888619.

[3] K. Goldberg et al., Proc. SPIE 8679 (2013) 867919.

9235-19, Session 7

A broader view on EUV-masks: adding complementary imaging modes to the SHARP microscope

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SHARP, the SEMATECH High-NA Actinic Reticle review Project, is an actinic, synchrotron-based microscope dedicated to extreme ultraviolet (EUV) photomask research. We are expanding the capabilities of the tool by implementing complementary imaging modes.

SHARP has been designed to closely emulate image formation in printing tools like the ASML ADT, 3100 and 3300 scanners in terms of mask-side NA, illumination and variation of the plane of incidence across the ring field. In addition, the instrument's programmable Fourier Synthesis Illuminator and its use of Fresnel zoneplate lenses as imaging optics provide a versatile framework, facilitating the implementation of diverse modes beyond conventional imaging. These include, for example, cubic phase modulation, Zernike phase contrast, dark field imaging, and differential interference contrast, all designed to extract more information

or increase the sensitivity of defect detection. We will demonstrate the operation of several of these imaging modes.

Cubic phase modulation is a technique that increases the depth of focus of an imaging system without affecting its resolution and light gathering power. Eliminating defocus and reducing the impact of aberrations it allows for a larger field of view and faster navigation. Zernike phase contrast provides increased detection sensitivity to sub-resolution, and pure-phase defects. Dark field imaging facilitates automated detection of isolated features on bright regions of a photomask or on a mask blank. Differential interference contrast provides sensitivity to phase changes e.g., at the edge of a feature. Together with the illumination coherence control, these complementary imaging modes increase the sensitivity and versatility of SHARP, provide additional information about the sample, and allow faster mask navigation.

SHARP features multiple nanofabricated arrays containing over 200 individual zoneplate lenses total. Each zoneplate acts as an independent, user-selectable imaging objective. Switching between lenses can be done in less than a minute. The illuminator allows for instant adjustment of the central ray angle, coherence and pupil-fill with the selected lens and imaging mode.

The zoneplates are produced at the CXRO Nanofabrication Lab on silicon nitride membranes using high-resolution e-beam lithography. The silicon nitride membrane windows were designed to accommodate a large number of zoneplates without compromising their robustness and flatness. With outer zone widths down to 19 nm and mask-side numerical apertures up to 0.156 (0.625 4xNA), SHARP has coherent and incoherent resolution cutoffs at 86 nm and 43 nm respectively, (22 nm and 11 nm on the wafer).

We have created software that efficiently calculates zone patterns for a wide range of applications including wave front modification based on Zernike-polynomials. From a web interface, the software generates pattern files that can readily be used with an e beam lithography system. The typical calculation and optimization time for an individual lens, drawn to sub-nm resolution, is below one minute.

Zoneplates for the SHARP microscope are currently in production.

Visible-light experiments and simulations compliment the implementation of additional imaging modes at 13.5nm wavelength. Experimental data and simulation results will be presented.

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9235-20, Session 7

Phase-enhanced defect sensitivity for EUV mask inspection

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The improvement of phase defect sensitivity by the Zernike phase contrast method is demonstrated experimentally and a method for optimally detecting both phase and amplitude defects at the same time is introduced. Our previous results show that in-focus inspection with increased defect signal for phase defects can be achieved by phase contrast method. However, in order to study both amplitude and phase defects, this leads to a requirement for multiple scans. We will explore the answer for optimal detection by simulation and experiment.

The Zernike phase contrast method is an effective way to achieve in-focus sensitivity to phase defects. If instead of using the conventional 90° phase shift in the pupil which only benefits the phase defects, an optimized phase-shift can be found allowing both amplitude and phase defects to reach acceptable defect sensitivity at focus. Simulation results show that with an optimized phase-shifted angle, we can increase the signal strength of the phase defects to 60% of its peak signal at 90° phase shift, and only reduce the signal strength of the amplitude defects to 70% of its original intensity at focus. This indicates the opportunity that we can simultaneously observe both phase and amplitude defects at focus on the EUV mask. In addition to mask blanks, we also consider patterned mask inspection. The result shows the Zernike phase contrast method to be an efficient method to characterize the phase defect beneath the patterned structure. Moreover, we show that noise reduction by further implanting apodization in the pupil plane improves the signal to noise ratio.

Based on the simulation results, experimental demonstration using programed Fresnel zone plates in the SEMATECH Berkeley mask inspection microscope (SHARP) will be presented. With various phase shifts and apodization on the zone plates, we will demonstrate the ideas of using the Zernike phase contrast method to study the phase defects on the EUV mask, the improvement on the signal to noise ratio, and optimal detection for phase and amplitude defects at focus.

This research is sponsored by IMPACT+ (Integrated Modeling Process and Computation for Technology). Member companies – Applied Materials, ARM, ASML, Global Foundries, IBM, Intel, KLA-Tencor, Marvell Technology, Mentor Graphics, Panoramic Tech, Photronics, Qualcomm, Samsung, SanDisk and Tokyo Electron.

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9235-21, Session 7

Capability of particle inspection on patterned EUV mask using model EBEYE M

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According to road map shown in ITRS [1], EUV mask requirement for defect inspection is to detect particle size of sub- 20 nm. EB (Electron Beam) inspection with high resolution is one of the promising candidates to meet such severe defect inspection requirement. However, conventional EB inspection using SEM method has a problem of low throughput. Therefore, we have developed an EB inspection tool, named Model EBEYE M?. The tool has PEM (Projection Electron Microscope) technique and image acquisition technique to acquire image with TDI (Time Delay Integration) sensor while continuous stage moving to meet high throughput [2].

In our previous study, we showed performance of the tool applied for 2X nm node in a production phase for particle inspection on EUV blank. In the study, the sensitivity of 20 nm with capture rate of 100 % and the throughput of 1 hour per 100 mm square were achieved, which is higher than conventional optical inspection tool for EUV mask inspection [3].

Such particle inspection is required for not only on the EUV blank but also on the patterned EUV mask. It seems to be valuable for inspection after defect repair and final cleaning for EUV mask fabrication. Moreover, it is useful as particle monitoring tool between exposures for wafer fabrication until EUV pellicle is available. However, since the patterned EUV mask consists of 3D structure, it is more difficult than that on the EUV blank.

In this paper, we will show that the particle inspection on the EUV blank using the tool is applied for the patterned EUV mask. The capability of particle inspection on the patterned EUV mask applied for 2X nm node is demonstrated. As a result, the particles of around 20 nm are detected on the patterned EUV mask with throughput of 1 hour per 100 mm square.

[1] International Technology Roadmap for Semiconductors (ITRS) 2013 Edition, Lithography, table LITH6

[2] M.Miyoshi et al., “Development of A Projection Imaging Electron Microscope with Electrostatic Lenses”, J.Vac. Sci. Technol. B17, (6), pp.2799-2802 (1999)

[3] Masato Naka et al., “Capability of Model EBEYE M for EUV Mask Production”, Proc. SPIE Vol.8522, 85220K (2012).

9235-22, Session 7

AIMS™ EUV first light imaging performance

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Overcoming the challenges associated with photomask defectivity is one of the key aspects associated with EUV mask infrastructure. In addition to establishing specific EUV repair approaches, the ability to identify printable defects that require repair as well as to verify if a repaired site was successful are absolutely necessary. Such verification can only be performed using the same illumination conditions with which the photomask will be exposed in the wafer by an actinic tool, the AIMS™ EUV. ZEISS, in collaboration with the SEMATECH EUVL Mask Infrastructure (EMI) consortium are currently developing the AIMS™ EUV system and have recently achieved First Light on the prototype system, a major achievement. First light results will be presented in addition to the current development status of the system.

9235-23, Session 8

Negative tone development process for ArF immersion extension *(Invited Paper)*

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Negative tone development (NTD) process is now being applied to HVM of advanced devices.

Immersion lithography extension is one of the candidates for further pitch shrink down to 2x nm and below design rule device manufacturing due to the delay of EUV lithography application to high volume manufacturing. Several double patterning processes were proposed for immersion lithography extension at early stage around 2007, and a few of them have become matured. Spacer defined process is being applied to the flash memory devices manufacturing. Positive tone freezing process is one of the candidates as cost reduction process of litho-etch-litho-etch (LELE) double line process, and has been studied by material supplier and equipment supplier in the viewpoint of material and process respectively. However, these processes are mainly for line and space patterning, and there was no proposal for trench and contact hole patterning except for negative tone development (NTD) process at the early stage of double patterning study.

NTD process has a large advantages for narrow trench and contact hole pattern imaging, since negative tone imaging enables to apply bright mask for these pattern with significantly high optical image contrast compared to positive tone imaging. There are two methods for negative tone imaging. One is a process with negative tone resist and conventional alkaline developer, the other is a process with conventional positive tone resist and new negative tone developer. The NTD process in this presentation uses the latter materials. The resist material of NTD at exposed area has highly hydrophilic property due to generated carboxylic acid unit by the de-protection reaction, which can not dissolve to organic solvent. Currently, NTD has become the mainstream.

NTD is planned to be applied to 14nm node, 10nm node, and depending on the schedule of EUV, 7nm node as well. In this presentation, the advantage of NTD and its future application will be explained.

9235-24, Session 8

Characterization of a new polarity switching negative tone e-beam resist for 14nm and 10nm logic node mask fabrication and beyond

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At the 14 nm and 10 nm logic nodes the critical layers are typically patterned on wafer using bright field imaging with negative tone develop. Consequently, this strategy relies on the use of high quality bright field masks. The critical features on bright field masks are typically either opaque lines for gate level and metal levels or opaque dots for contact and via levels. In order to meet the tight critical dimension (CD) requirements on these opaque features on the mask the use of a high quality negative tone chemically amplified e-beam resist (NCAR) is required. Until very recently the only negative tone ebeam resists available for use by the mask industry were the traditional cross linking type in which e-beam exposure cross links the material and makes it insoluble in developer. These traditional types of NCAR e-beam resists are prone to swelling and scumming issues especially in tight geometries and in heavily background written features such as isolated spaces. In this paper we will describe the performance of a new polarity switching type of NCAR resist that works by changing the solubility of the exposed resist without cross linking. This has the advantage of significantly reduced swelling and scumming and resulted in major improvements in the resolution of heavily nested features and small clear features on the mask that are generated by the aggressive optical proximity correction algorithms used by the 14 nm and 10 nm wafer lithography processes. In addition, line edge roughness, corner rounding, line end shortening, CD uniformity, linearity, pattern fidelity (mask inspectability), dry etch resistance, and thru pitch performance data for the polarity switching resist will be shown and compared to results from a typical cross linking type resist for both OMOG binary and attenuated phase shift masks . A summary of work to improve and optimize the defect performance of the new resist to achieve manufacturable defect levels will also be presented. Based on the significant performance benefits demonstrated versus traditional crosslinking NCAR materials , it was found that the new polarity switching NCAR was suitable for producing critical level masks for the 14 nm and 10 nm logic nodes.

9235-26, Session 8

CDU improvement in mask making using negative chemically amplified resist by reducing the border effect

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As technology progresses toward the 10-nm node and beyond, requirement of the mask critical dimension (CD) uniformity becomes very stringent. Tracking the sources of CD error and minimizing the error are very important tasks in state-of-the-art mask production. Generally,

the mask CDU error can be decomposed into location-dependent and pattern-dependent components. In the mask making process with negative-tone chemically amplified resist, obvious CD deviation is observed in areas along the borders of the scanner field. Secondary electrons generated while the border is exposed result in greater CD deviation on the patterns along the border than those inside the scanner field. We call this phenomenon the border effect. In this study, source of the border effect is investigated and various corrective methods such as the new multi-level dose modulation method and Global CD correction functions in the 50keV e-beam pattern generator are applied. Our results indicate successful elimination of the border effect and 45% improvement in CDU.

9235-27, Session 8

Laser-written binary OMOG photomasks for high-volume non-critical 193-nm photolithographic layers

Rémi Rivière, Selvi Gopalakrishnan, Martin Mazur, Nevzat Öner, Sven Mühle, Rolf Seltmann, GLOBALFOUNDRIES Dresden Module Two, GmbH & Co. KG (Germany)

Photomasks are key elements of photolithographic processes, implying that their degradation must be reliably monitored and strongly mitigated. Indeed, the photo-induced oxidation of Cr in Cr On Glass (COG) photomasks and the concomitant electrostatic-field migration present in high-volume production using 193-nm photolithographic scanners severely deteriorate the pattern transfer quality, therefore limiting the lifetime of these reticles. To moderate this effect, Opaque MoSi On Glass (OMOG) photomasks, significantly less prone to such degradation, are currently being massively used in leading-edge microfabrication flows. The type of mask fabrication process normally used involving e-beam writing is however not adapted for non-critical photolithographic layers that do not yet benefit from its inherent performances but still suffer from its high cost and its long processing time. It is therefore proposed in this work to combine the simplicity of laser writing and the resistance of MoSi to degradation by using laser-written binary OMOG photomasks for the non-critical layers (e.g. ion-implantation) of a 28-nm production flow. To evaluate one of this new reticle, its pattern transfer fidelity is compared to the one of a laser-written binary COG mask already qualified for production from a photolithographic quality perspective, both masks being treated using the same optical proximity correction (OPC) model. Dispersive and dissipative properties, critical dimension uniformity, pattern linearity and pattern proximity are directly measured on wafer level, subsequently revealing that both photomasks match in terms of OPC parameters. The utilized OPC model is moreover proven robust against the use of both types of masks, consequently making the conversion from COG to OMOG particularly simple. These experimental results therefore qualify the new mask fabrication type and pave the way for a major utilization in high-volume production.

9235-51, Session 8

Increasing reticle inspection efficiency and reducing wafer print-checks at 14nm using automated defect classification and simulation

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IC fabs inspect critical masks on a regular basis to ensure high wafer yields. These requalification inspections are costly for many reasons including the capital equipment, system maintenance, and labor costs. In addition, masks typically remain in the “requal” phase for extended, non-productive periods of time. The overall “requal” cycle time in which reticles remain non-productive is challenging to control. Shipping schedules can slip when wafer lots are put on hold until the master critical layer reticle is returned to production. Unfortunately, substituting backup critical layer reticles can significantly reduce an otherwise tightly controlled process window adversely affecting wafer yields.

One major requal cycle time component is the disposition process of mask inspections containing hundreds of defects. Not only is precious non-productive time extended by reviewing hundreds of potentially yield-limiting detections, each additional classification increases the risk of manual review techniques accidentally passing real yield limiting defects. Even assuming all defects of interest are flagged by operators, how can any person’s judgment be confident regarding lithographic impact of such defects? The time reticles spend away from scanners combined with potential yield loss due to lithographic uncertainty presents significant cycle time loss and increased production costs

An automatic defect analysis system (ADAS), which has been in fab production for numerous years, has been improved to handle the new challenges of 14nm node automate reticle defect classification by simulating each defect’s printability under the intended illumination conditions. In this study, we have created programmed defects on a production 14nm node critical-layer reticle. These defects have been analyzed with lithographic simulation software and compared to the results of both AIMS™ optical simulation and to actual wafer prints.

9235-28, Session 9

MDP challenges from a software provider’s perspective *(Invited Paper)*

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This industry faces a new challenge every day. It gets tougher as process nodes shrink and the data complexity and volume increase.

In mask data preparation (MDP), fracturing is commonly used to prepare data for mask writers. Slivers have been a traditional challenge since variable-shaped electron-beam mask writers were introduced because slivers lower mask yield due to critical dimension (CD) errors.

Handling huge data volume is also a challenge. At mask shops, one of the biggest investments is the mask writer, and the machine time must be utilized as much as possible. Even with huge data volumes, preparing the data has to be faster than the write time to avoid idle writing machines.

Write time is a big headache. Even if MDP eliminates slivers and prepares data quickly, mask writers can take days to make a mask for advanced nodes because the high number of shots exposed on the mask.

MDP now has to take care of not only geometric data manipulation but also mask process correction using a model-based approach to improve the pattern fidelity. CD linearity must be corrected to resolve narrow and complicated patterns on the mask as geometry shrinks.

These are typical challenges, and many solutions have been commercially available and/or proposed (i.e. fine slicing, distributed processing, shot reduction, multi-beam, MPC, etc.). In addition, all these challenges are related each other. For example, fine slicing could help not only eliminating slivers but in reducing the number of shots.

We have been providing a MDP software to the industry more than 20 years. Such MDP challenges and solutions from a software provider’s perspective are discussed.

9235-29, Session 9

Effective corner rounding correction in the data preparation for electron-beam lithography

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Technologien (Germany); Clyde H. Browning, Thiago R. Figueiro, Aselta Nanographics (France); Christoph K. Hohle, Michael Kaiser, Fraunhofer-Institut für Photonische Mikrosysteme (Germany) and Fraunhofer-Ctr. Nanoelektronische Technologien (Germany); Patrick Schiavone, Aselta Nanographics (France)

The specifications and requirements of lithography are becoming tighter and more extreme as the semiconductor technology node is moving down towards sub-20nm. This demands finer and more delicate corrections in electron beam (e-beam) lithography, whether it is for mask manufacturing or direct writing, not only on the CDs, LER and LWRs but also on the line end shortening (LES) or corner rounding (CR). The corrections of the latter two are related each other and it is getting more important as the advanced lithography concept like the self-aligned double patterning (SADP) combined with the complimentary lithography is introduced. One of the draw backs in the data correction of LES and CR is increasing of the exposure time, which also increases the shot counts of corrected data in the case of variable shaped beam exposure tool.

New correction algorithms were developed and inspected through the test exposure to figure out the quality and advantages of the built up method. The main objectives of this development is not only enhancing the accuracy of correction but also find a way to avoid or reduce the fall back of it, which is gaining of exposure shot counts after the correction. Inscale® from Aselta Nanographics is used to prepare the data with improved correction and for simulation to check the aftermath. Fraunhofer IPMS-CNT exposed the prepared data using a Vistec SB3050DW? and observed it with an Applied Materials Verity 4i CD-SEM.

9235-30, Session 9

Photonic curvilinear data processing

Clyde H. Browning, Patrick Schiavone, Thomas Quaglio, Thiago R. Figueiro, Aselta Nanographics (France); Sébastien Pauliac, Jérôme Belledent, Aurélien Fay, CEA-LETI (France); Jean-Christophe Marusic, Soitec S.A. (France); Jessy Bustos, STMicroelectronics (France)

With more and more photonic data presence in e-beam lithography, the need for efficient and accurate data fracturing is required to meet acceptable manufacturing cycle time. Large photonic based layouts now create high shot count patterns for VSB based tools. Multiple angles, sweeping curves, and non-orthogonal data create a challenge for today's e-beam tools that are more efficient on Manhattan style data. This paper describes techniques developed and used for creating fractured data for VSB based pattern generators.

Proximity Error Correction is also applied during the fracture process, taking into account variable shot sizes to apply for accuracy and design style. Choosing different fracture routines for pattern data on the fly allows for fast and efficient processing. Data interpretation is essential for processing curvilinear data as to its size, angle, and complexity. Fracturing data into "efficient" shot counts or results from an ILT standpoint is no longer practical as shot creation requires knowledge of the data content as seen in photonic based pattern data.

Simulation and physical printing results prove the implementations for accuracy and write times compared traditional VSB writing strategies on photonic data. Geometry tolerance is used as part of the fracturing algorithm for controlling edge placement accuracy and tuning to different e-beam processing parameters.

9235-31, Session 10

Mask data processing in the era of multibeam writers *(Invited Paper)*

Frank E. Abboud, Michael Asturias, Maesh Chandramouli, Intel Corp. (United States); Yoshihiro Tezuka, Intel Kabushiki Kaisha (United States)

Mask Writers' architectures have evolved through the years in response to ever tightening requirements for better resolution, tighter feature placement and CDs control, and tolerable write time. The unprecedented extension of optical Lithography and the myriad of Resolution Enhancement Techniques have tasked current mask writers in terms of shot count and therefore write time. Once again, we see a transition to a new type of mask writers, based on a Massively Parallel Architecture. These platforms offer a step function improvement in dose and the ability to process massive amount of data. Both higher dose and the almost unlimited appetite for edge corrections, open new windows for opportunity to further push the envelope. Further these architectures are also naturally capable of producing curvilinear shapes, making the need to approximate a curve with multiple Manhattan shapes unnecessary. This talk will look into the requirements and considerations for mask processing to take advantage of the new architectures.

9235-32, Session 10

EBM-9000: EB mask writer for product mask fabrication of 16nm half-pitch generation and beyond

Hidekazu Takekoshi, Takahito Nakayama, Kenichi Saito, Hiroyoshi Ando, Hideo Inoue, Noriaki Nakayamada, Takashi Kamikubo, Rieko Nishimura, Yoshinori Kojima, Jun Yashima, Akihito Anpo, Seiichi Nakazawa, Tomohiro Iijima, Kenji Ohtoshi, Hirohito Anze, NuFlare Technology, Inc. (Japan); Victor Katsap, Steven D. Golladay, Rodney A. Kendall, NuFlare Technology, Inc. (United States)

In the TN=11nm/HP=16nm generation, the shot count on a mask is expected to exceed 1T shots. In addition, the resist sensitivity needs to be lower to reduce the shot noise effect so as to get better LER. Both of these trends result in longer write time than that of the previous generations. At the same time, most mask makers request masks to be written within 24 hours. Thus, a faster mask writer with better writing accuracy than mask writers of previous generations is needed.

With this background, a new electron beam mask writing system, EBM-9000, was developed to satisfy such requirements of the hp 16nm generation. The development of EBM-9000 focused on improving throughput for larger shot counts and improving the writing accuracy. Three new major features of the tool are : A) a new electron gun with higher brightness to achieve current density of 800 A/cm^2, B) a three stage deflection system and a high speed DAC amplifier to accurately position the beam with shorter settling time, and C) an electron optics column with a newly designed "deep immersion objective lens" to achieve beam resolution to be the same as EBM-8000, even with higher current density such as 800A/cm^2.

In addition to the new key technologies mentioned above, EBM-9000 equips the following new technologies to improve patterning performance.

An electron detector was newly designed based on simulations of the electron trajectory. As a result, the S/N ratio in EBM-9000 improved about two times compared to EBM-8000, making the EOS calibration more accurate.

Also, to reduce the error attributed to mechanics, a new interferometer system was adopted for stage motion control to reduce non-linearity errors, and a mounting structure to hold the optics was revised to reduce mechanical vibrations. Furthermore, to reduce mechanical vibration during stage motion, NuFlare improved the stiffness in stage and optimized the parameter for motion control based on the transfer function of each tool.

The user interface (UI) was also renewed and improved to make the operation more user friendly, and was provided as a WEB base application. New data formats, VSB-12i and OASIS.MASK, are also available, capable of containing additional information such as dose modulation to provide more flexibility in mask design for mask manufacturers.

Also in parallel of aggressive introduction of new technologies, EBM-

9000 inherits 50kV variable shaped electron beam / vector scan architecture, continuous stage motion and VSB-12 data format handling from the preceding EBM series to maintain high reliability accepted by many customers.

Our results show that the performance of EBM-9000, developed as the mass production mask writer for the hp16nm node, will satisfy the requirements of that generation. Some customers suggest that shot count will not increase as expected for now, because of development delay in EUV lithography and progress in multi-exposure technology. Such trends would influence the strategy for our next tool, but technologies and knowledge verified on the EBM-9000 will be inherited to the next tool as our advantages.

9235-33, Session 10

Study of heating effect in multi-beam mask writing

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We study heating effect by e-beam exposure on the mask. The heat effect can be decided by total applied energy which is comprised by acceleration voltage and applied dose. And the total applied dose is determined by current density and exposure time. Therefore, the heat distribution trend on the mask can be different according to writing scheme and exposure condition.

Recently, the high current density is being applied and writing pass is being reduced to improve the throughput by reducing total writing time. Also the high dose reacting PR (photo-resist) was applied to improving the CDU (critical dimension uniformity).

In this paper, we compare and analyze with VSB (variable shaped beam) writing and multi-beam writing in heat distribution. The writing concept of multi-beam writing is based on gray writing with multi-array beam. Relatively, the low current density was applied for each beam, and the writing scheme is different with VSB writing.

The influence on LCD (local critical dimension) by heating was analyzed and compared according to writing scheme. The global heating effect was simulated and compared for analyzing the heat effect to the global registration. The heat distribution was also simulated according to the applied current density and writing pass.

At the specific condition of total dose of 25?C/cm2, the exposure time of VSB is over 200 times than multi-beam writing. Therefore, in case of VSB writing, the maximum temperature of local beam exposed area is higher than multi-beam writing. It means that the LCD can be stable in terms of heating effect in the multi-beam writing. However the global temperature distribution related with global registration should be considered in the result of multi-beam heat simulation.

9235-34, Session 10

Resist charging effect correction function qualification for photomasks production

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The residual image placement (IP) error due to resist charging during photomask electron beam lithography is one of the major contributors to the overall registration error budget [1-2]. Minimizing or eliminating resist charging is a challenging and necessary task in order to fabricate chips at state of the art technology nodes. One of the methods to mitigate resist charging is through application of a compensation map during photomask electron beam lithography, also known as a charging effect correction (CEC).

Previous reports have presented CEC model specifics of Nuflare electron beam pattern generators [3-5]. The capability of preliminary CEC models needs improvement [3], while latest versions, which takes into account time-dependent charging factors, was reported to be production ready [4-5].

We report on the latest Nuflare CEC model for production of advanced photomasks. This CEC model includes functionality for the simulation of static and time-dependent charging effects, together with an improved calibration method that considers multiple fitting parameters for various beam scattering effects. This latest CEC model is generated using a special test design with variations of pattern density across a mask, allowing for fine tuned resist charging compensation maps for different layers. This latest CEC model yields a significant reduction in photomask IP, as well as improving overlay between critical neighboring layers at the photomask level. Furthermore the correlations between achieved IP improvement and versus single mask parameters are presented and discussed. The layer design specifics, resist and blank material, and exposure parameters are observed to be the major influences on CEC model performance.

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9235-35, Session 11

PMJ Panel Discussion Overview: EUV mask inspection technologies for the 10nm and beyond

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No Abstract Available

9235-36, Session 12

EMLC 2014 Best Paper: Contact hole multiplication using grapho-epitaxy directed self-assembly: Process choices, template optimization, and placement accuracy

Joost P. Bekaert, Jan Doise, Vijaya-Kumar Murugesan Kuppuswamy, Roel Gronheid, Boon Teik Chan, Geert Vandenberghe, IMEC (Belgium); Yi Cao, YoungJun Her, AZ Electronic Materials USA Corp. (United States)

Directed Self Assembly (DSA) of Block Co-Polymers (BCP) has become an intense field of study as a potential patterning solution for future generation devices. The most critical challenges that need to be understood and controlled include pattern placement accuracy, achieving low defectivity in DSA patterns and how to implement this process as a patterning solution. The DSA program at imec includes efforts on these three major topics.

Specifically, in this paper the progress for the templated DSA flow within the imec program will be discussed. An experimental assessment is

made based on a 37 nm BCP pitch material. In particular, the impact of different process options is illustrated, and data for CD and placement accuracy of the DSA holes in their template is provided.

9235-37, Session 13

EUV mask fabrication readiness and challenges for HVM *(Invited Paper)*

Guojing Zhang, Pei-Yang Yan, Ted Liang, Kishore K. Chakravorty, Seh-jin Park, John F. Magana, Su Xu, Brittany M. Mcclinton, Robert J. Chen, Yongbae Kim, Intel Corp. (United States)

EUV is a leading candidate of the lithography technology for HVM in the next generation. One of the essential enablers EUV lithography is the MASK. The expectation of EUV mask readiness to the mask shops for delivering a high quality and defect free EUV mask has been increasingly raised in the industry. As the chip feature size continues to shrink for the future generations, mask patterning resolution, structure fidelity and defect control become more challenging.

In this paper, we will expand on such requirements for EUV mask infrastructure and manufacturing. We will show the status and discuss challenges with the respect to mask blanks, patterning capability, process defectivity and handling requirements. Some of the concerns and possible solutions along with blank availability mask cleaning, mask stability and its lifetime will also be addressed.

9235-38, Session 13

EUV mask black-border evolution

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The black border is a frame created by removing all the multilayers on the EUV mask in the region around the chip. It is created to prevent exposure of adjacent fields when printing an EUV mask on a wafer. Papers have documented its effectiveness [1]. As the technology transitions into manufacturing, the black border must be optimized from the initial mask making process through its life. In this work, the black border is evaluated in three stages: the black border during fabrication, the final sidewall profile, and extended lifetime studies.

This work evaluates the black border through simulations and physical experiments. The simulations address concerns for defects and sidewall profiles. The physical experiments test the current black border process. Three masks are used: one mask to test how black border affects the image placement of features on mask and two masks to test how the multilayers change through extended cleans. Data incorporated in this study includes: registration, reflectivity, multilayer structure images and simulated wafer effects.

By evaluating the black border from both a mask making perspective and a lifetime perspective, we are able to characterize how the structure evolves. The mask data and simulations together predict the performance of the black border and its ability to maintain critical dimensions on wafer. In this paper we explore what mask changes occur and how they will affect mask use.

[1] Davydova et al. “Impact of an etched EUV mask black border on imaging and overlay,” Proc. SPIE 8522, 852206 (2012).

9235-39, Session 13

Feasibility of EUV lithography for printing circuits with 4nm feature size

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One of the main concerns about EUV lithography is whether or not it can be extended to very high numerical aperture. Since the mask must be illuminated by obliquely incident EUV light in order to separate the reflected light from the incident light, increasing the NA would require using a larger chief ray angle. This would lead to greater shadowing effect of the absorber and therefore to lower aerial-image contrast, as well as to greater non-telecentricity of the aerial image on the wafer side. Recently, various authors have suggested the use of alternative mask concepts, multilayer tuning and increased reduction ratio to mitigate some of the problems associated with larger chief ray angles. In this paper, we will explore these concepts further, as well as propose new concepts, to extend EUV lithography to the 4 nm technology node.

We will first show by rigorous electromagnetic simulation that there are some very interesting and hitherto undiscovered electromagnetic phenomena occurring in the sub-6 nm feature size regime. These new phenomena can be exploited to enable the printing of 4-nm lines and spaces with excellent aerial-image contrast (>90%) and peak intensity, using NA = 0.95 and 4X reduction ratio. This is shown in the figure below for both absorber mask and etched multilayer mask.

The ability to print 4 nm lines and spaces is not enough for the manufacturing of circuits, since a real circuit, especially logic circuit, contains more or less random patterns. Therefore we also discuss the possibility of printing random circuits with 4 nm feature size. We will show how it is possible to print such a circuit using an absorber mask, with suitable tuning of the absorber and multilayer thicknesses, reduction ratio, exposure technique and optical proximity correction. The figure below shows our initial simulation result for a SRAM mask with 4 nm feature size. Further application of optical proximity correction will improve the pattern fidelity shown in the figure and we will discuss this further optimization in the paper.

Based on the above very encouraging results, we believe that EUV lithography will be useful for many years to come, up to the 4 nm technology node.

9235-40, Session 14

Capability of etched multilayer EUV-mask fabrication

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Extremely Ultraviolet Lithography (EUVL) is the most leading lithographic technology used to fabricate hp1x nm node devices. When target pattern size shrinks around 10nm, numerical aperture (NA) of EUVL tool must be more than 0.4. When NA increases with keeping projection optics with 4X magnification, CRA (Chief Ray Angle) must be more than 6 degrees. However, larger CRA number leads to larger mask 3D effect with conventional EUVL mask structure, which negatively affects the performance to form horizontal line pattern (perpendicular to EUV light direction). And that induces the degradation of lithography process margin. As a method to avoid the degradation, increasing magnification of projection optics with larger mask size or reducing exposure field size have been proposed. [1] However, the former method needs new infrastructures to fabricate EUVL mask using big size blank and these lead to high mask cost, on the other hand, the latter method degreases throughput of lithography process and it leads to high process cost. In order to resolve this issue, studies of etched multilayer structure for high-NA EUVL have been recently accelerated under the condition of increased CRA without changing magnification, mask size, and exposure field size .[2][3]

In this paper, we present process development of patterning etched

multilayer mask such as resist patterning process, etch process, and cleaning durability of high aspect ratio etched multilayer pattern. And capability of etched multilayer EUV mask fabrication will be discussed.

References:

[1] W.Kaiser, “EUVL Roadmap: High NA Optics”, SEMATECH Litho Forum 2012, Vancouver, 2012

[2] J.T.Neumann, et al, “Mask effects for high-NA EUV: impact of NA, chief-ray-angle, and reduction ratio”, Proc. SPIE 8679, 867915, 2013

[3] K.Takai, et al, “Patterning of EUVL binary etched multilayer mask “, Proc. SPIE 8880, 88802M, 2013

9235-41, Session 14

Repairing native defects on EUV mask blanks

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Mask defectivity is a serious problem for all lithographic masks, but especially for EUV masks. Defects in the EUV mask blank are particularly challenging because their elimination is beyond the control of the mask fab. If defects have been identified on a mask blank, patterns can be shifted to place as many blank defects as possible in regions where the printing impact will be eliminated or become unimportant. For those defects that cannot be mitigated, repair strategies must be developed. Repairing defects that occur naturally in the EUV blank is challenging because the printability of these defects varies widely. This paper describes some types of native defects commonly found and begins to outline a triage strategy. Sample defects best suited to nanomachining are treated in detail: repairs are attempted, characterized using mask metrology and then tested for printability. Based on the initial results, the viability of repairing native defects is discussed.

9235-42, Session 14

Carbon removal from trenches on EUV reticles

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With the insertion of EUV being postponed towards the 7 nm node, the feature size on reticles is also decreasing towards less than 30 nm. Besides the increasing risk of particles becoming a killer defect at these critical dimensions the contribution of EUV induced carbon in the trenches can seriously affect the optical performance of the reticle. For the particles the discussion on a pellicle has recently been fired up again as a protective measure, however this will not solve the carbon contamination problem. With EUV powers needed for the HVM production of the 1X nm node growing towards 1 kW the growth of carbon is also increasing. Although wet cleaning has been reported as successful it can be questioned if the liquid can enter to the bottom of the trench to remove the carbon when he size of the trench approaches 30 nm with an aspect ratio of 3 to 5.

We report on our investigation of dry cleaning of reticles with a microwave induced hydrogen plasma on dummy reticles. The dummy reticles were manufactured with 70 nm ALD grown TaN on a Ru surface and test structures were patterned with lines and spaces ranging between 60 and 400 nm. After processing the test structures were contaminated with e–beam grown carbon and exposed in our plasma facility to remove the carbon. Analysis of the samples was performed with SEM/EDX and with SIMS-SPM to verify the complete removal of carbon from the bottom of the trench.

9235-43, Session 14

The study on EUV mask cleaning without Ru surface damage

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In this paper, we will discuss about the effective EUV mask cleaning technology solutions for mask operations. We developed the deoxidize process for oxidized Ru surface, it means an increase in reflectance. We show the analysis results of the deoxygenation process at first, discuss the mechanism next.