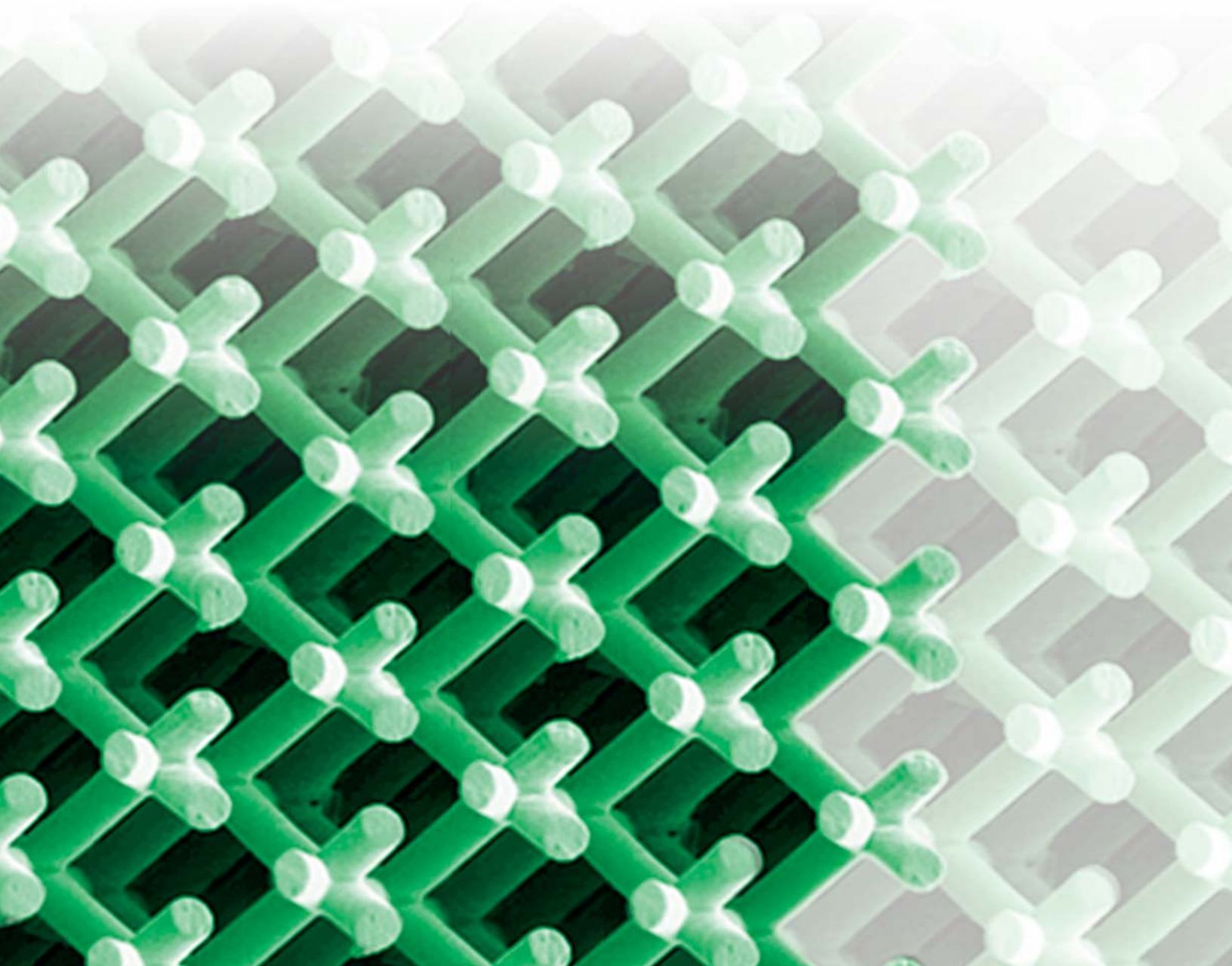
Technical Abstract Summary Digest

SPIE Advanced Lithography

25 February–2 March 2007
San Jose Convention Center and San Jose Marriott
San Jose, California USA



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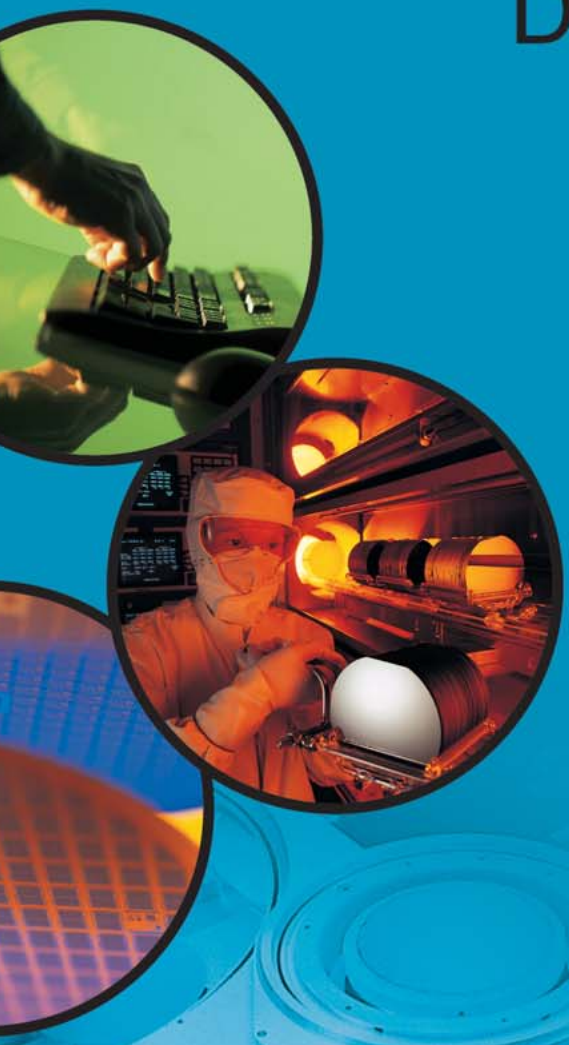

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Technical Abstract Summaries

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Conference 6517: Emerging Lithographic Technologies XI

Tuesday-Thursday 27 February-1 March 2007

Part of Proceedings of SPIE Vol. 6517 Emerging Lithographic Technologies XI

6517-01, Session 1

Milliped probe-based storage

M. Despont, IBM Corp. (Switzerland)

No abstract available

6517-02, Session 1

Optical meta-materials at IR wavelength fabricated by nanoimprint lithography

W. Wu, Hewlett-Packard Labs.; E. Kim, Univ. of California/Berkeley; E. Ponizovskaya, Hewlett-Packard Labs.; Y. Liu, Univ. of California/Berkeley; Z. Yu, A. M. Bratkovski, Hewlett-Packard Labs.; N. X. Fang, Univ. of Illinois at Urbana-Champaign; X. Zhang, R. Shen, Univ. of California/Berkeley; S. Wang, R. S. Williams, Hewlett-Packard Labs.

Optical negative index meta-materials (NIM) that exhibit unique refractive and focusing properties have recently become a focus of research worldwide. They have opened up new opportunities in nano-photonics and optical integration. The important issue of how to fabricate these meta-structures with high-precision, high-throughput, and low-cost remains a challenge, especially for short wavelengths of radiation (e.g. infrared or even visible range). On the other hand, nanoimprint lithography (NIL) is low-cost, high-throughput and high-resolution, even though the yield and overlay issues haven't met the requirements of semiconductor industry standard yet. However, given the much relaxed requirement on overlay and yield, optical applications are ideal for early adoption of NIL. Here, we report on the development of a fabrication procedure of optical meta-structures using NIL.

We will report two types of meta-structures both are fabricated by NIL: L-shaped resonators (LSRs), which have a negative permeability at 5 micron range and "fishnet" structure, which is supposed to have both negative permittivity and permeability, hence negative refractive index at around 1.5 micron range. We fabricated the LSRs with smallest feature at 45 nm and better than 10 nm critical dimension (CD) control. LSRs on various substrates, such as Si, Si with Si3N4 film and free standing Si3N4 membrane were characterized and consistent with theoretical predictions.

We also studied and fabricated the metal/dielectric/metal stack fishnet structure which is more scalable for shorter wavelength. Our theoretical simulation shows that the structure has both negative permittivity and permeability, therefore negative refractive index at 1.5 micron range. More details in theoretical studies, fabrication and characterization will be presented too.

6517-03, Session 1

Drop on demand

No abstract available

6517-04, Session 2

SEMATECH's EUV program: a key enabler for EUVL introduction

S. Wurm, C. Jeon, M. J. Lercel, SEMATECH, Inc.

With the introduction of alpha tools, extreme ultraviolet lithography (EUVL) has reached a key milestone. Users of those tools must have access to critical EUV infrastructure capabilities to evaluate the technology in a pilot line operation. In cooperation with universities, national laboratories, suppliers, integrated device manufacturers, and other industry consortia, SEMATECH has been spearheading the worldwide effort to develop this EUV infrastructure in the source, mask, optics, and resist areas. In the process, SEMATECH's Mask Blank Development Center, its EUV Resist Test Center, and the EUV expertise built within the SEMATECH EUV program have become key enablers for a successful introduction of EUV technology. We will highlight the significant contributions that the SEMATECH EUV Program has made, and continues to make, to the worldwide EUV infrastructure development effort.

Moving beyond the alpha tool phase, the industry must have a clear understanding of the challenges that need to be addressed before EUV beta tools could be successfully introduced as early as 2009. We will identify those areas that still need a substantial effort to overcome technical and business challenges to meet 32 nm half-pitch requirements in time. Though some of those areas are clearly EUV-specific, others are generic and impact other lithography technologies as well.

One of the major attractions of EUVL is that it is an extendible technology that can likely support patterning for several technology generations. We will review the outlook for EUVL technology extendibility and discuss what the industry needs to start working on to enable EUVL's bright future and long lifetime.

6517-05, Session 2

EUV lithography with the Alpha Demo Tools: status and challenges

N. Harned, ASML Wilton; M. Goethals, IMEC (Belgium); R. Groeneveld, ASML Netherlands B.V. (Netherlands); P. Kuerz, M. Lowisch, Carl Zeiss SMT AG (Germany); H. Meijer, H. Meiling, ASML Netherlands B.V. (Netherlands); K. G. Ronse, IMEC (Belgium); J. Ryan, M. D. Tittnich, Albany NanoTech; H. Voorma, ASML Netherlands B.V. (Netherlands); J. D. Zimmerman, ASML Wilton

ASML has built and shipped two full field step-and-scan exposure tools for extreme ultraviolet lithography (EUVL). These tools, known as Alpha Demo Tools, will be used for process development and to set the foundation for the commercialization of this technology. The main objectives for the program are to minimize the risk of EUVL for the 32-nm node and beyond, and to support the development of the global infrastructure of masks, sources, and resist.

In this paper we will present results from the set-up and integration of both systems, and we will report on the on-site installation progress of these tools and results achieved thus far. Details will include data on modules and imaging, and an update on the key technology areas, such as contamination control and source operation.

Since the availability of resist and masks is critical to the success of this technology, we will provide a summary of the current status against the desired specifications to support 32nm lithography.

Both Alpha Demo systems will play a central role in research programs that cover a wide range of areas of EUV investigation, including imaging development, machine characterization, particle free reticle handling and reticle manufacture.

Albany Nanotech and IMEC have planned key projects that will further EUVL system knowledge, and facilitate the building of the infrastructure. We will summarize the planned projects, since the results expected, along with hands on experience using EUV lithography system, will provide the foundation for commercialization of EUV.

With the shipment of ASML's two Alpha Demo tools, EUVL has crossed a major hurdle in becoming a solution for lithography at 32nm and beyond. IMEC and Albany Nanotech, together with their industry affiliates and ASML, will use these systems to create a wealth of EUV knowledge and know how, and in the process, provide a strong boost to solving the challenges that still need to be met to make EUVL ready for volume production.

6517-06, Session 2

Nikon EUVL development progress update

T. Miura, K. Murakami, K. Suzuki, Y. Kohama, K. Morita, K. Hada, Y. Ohkubo, Nikon Corp. (Japan)

Extreme Ultra Violet Lithography (EUVL) is considered as the most promising technology below hp45nm node, following ArF immersion lithography in light of trend of decreasing process K1 factors. In this presentation Nikon would like to present significant progress on the development of EUV exposure tool. There are several key important areas which should be developed to realize EUVL to be feasible such as reflective mask, resist, and tool itself. The reflective mask features such characteristics as pellicle-less, ultra-smooth blank flatness and defect free. The resist should be of high sensitivity and small line edge roughness (LER) as well as fine resolution. EUV exposure tool itself consists of major modules such as EUV light source, projection optics, vacuum body, vacuum stages, and so on. As far as EUVL optics development is concerned, through the development of high-NA small-field EUV exposure system (HiNA) in conjunction with EUVA (Extreme Ultraviolet Lithography System Development Association) projects, we have developed new polishing technologies such as ion-beam figuring and elastic emission machining, and new high-precision interferometers for aspheric surface metrology. Wave front sensor system has been also developed partly in EUVA project. A new wave front sensor system which can be used for evaluating the projection optics with EUV light has already been installed in New SUBARU synchrotron facility in University of Hyogo. Our multi-layer coating technology has been also remarkably improved. High reflective Mo/Si multi layer coating has been successfully achieved and irradiation tests using synchrotron radiation have been conducted. Successful achievement of those developments enables us to fabricate high-precision aspheric mirrors for EUV pre-production and process development tool called EUV1.

Nikon has been also heavily involved in the infrastructure development such as reticle standardization and reticle handling development. Nikon has studied reticle protection method and proposed Dual Pod Concept in cooperation with Canon. Nikon also has been developing its own reticle cover as a method of reticle protection with the support of Nuflare Technology, which is scheduled to be implemented in EUV1 tool.

Nikon has almost completed fabrication of all modules such as full-field projection optics module, illumination optics module, vacuum body module, vacuum compatible reticle/wafer stage modules, reticle/wafer loader modules, EUV light source. Nikon will get into module integration phase to meet tool development schedule. Proto-typing of full-field projection optics was completed. Preparation of complete set of production and metrology tools necessary for projection optics production was completed and all tools are now in operation.

Nikon announces that EUV1 tool is scheduled to be delivered in 1st half of 2007. Development of production tool dubbed EUV2 is also considered.

6517-07, Session 2

Path to the HVM in EUVL through the development and evaluation of the SFET

S. Uzawa, H. Kubo, Y. Miwa, H. Tsuji, H. Morishima, Canon Inc. (Japan)

We have constructed a small field exposure tool (SFET) in collaboration with EUVA. This machine is not only the booster for resist and mask development, but also is positioned as a cornerstone of the manufacturing technologies for the EUVL beta tool. The SFET has a field size of 0.6*0.2mm2, a LPP source and two-mirror projection optics of Schwartzchild type. It also has an optical focus scope with the z-direction interferometer for precise focus settings. The SFET has two load lock chambers, one for automatic carrying mask in and out and the other for wafer handling in same manner. The throughput of SFET is estimated more than 5 wafers/hour with the in-line coater/developer.

We will report the exposure results and the optical performance of the SFET. The exposed results are affected by the aberration and the flare of the projection optics. The aberration indicated by the Zernike coefficients is closely related to the exposed pattern deformation. We will discuss the relation between the mirror surface condition and the exposed pattern deformations. On the other hand, the flare decrease image contrast. Recent studies indicate that the flare is not only generated by the mirror surface roughness in MSFR (1um to 1mm wave length), but also higher frequency parts of LSFR (1mm to 3mm). We will also discuss the relation between flare and mirror surface based on the simulation and exposure results.

In construction of the SFET projection optics, we developed the wavefront measurement tool (PAL) and the ion beam etching equipment (IBF). The PAL was developed in cooperation with the LLNL and we slightly modified for the SFET. The PAL brought out good measurement accuracy in adjustment process of the SFET projection optics. On the other hand, The IBF was developed in the EUVA project supported by NEDO. The IBF has a sharp ion beam making a very small etching and is used to finish off the fine mirror surface. We will introduce the abstracts of these two machines and the performance demonstrated in SFET making.

We will introduce an outline of Canon's activities in EUVL beta tool development, such as development of the mirror surface shaping and the wave front metrologies, the mask cassette handling, contamination and removal technologies studies for optics and mask. There are two types of EUV source, DPP and LPP. However both types are not yet sufficient in power, stability, durability and the cost/performance. We will discuss about the desired performance at HVM, the current performance and possibilities in future from our experiences for both the LPP and the DPP sources. We will also discuss the desired performance of HVM exposure tools for 45 nm to 32 nm generations and say our future plans for HVM tools.

6517-08, Session 2

EUV lithography program at IMEC

A. Goethals, R. M. Jonckheere, G. F. Lorusso, J. Hermans, K. G. Ronse, IMEC (Belgium)

EUV lithography is a leading candidate for 32nm half-pitch device manufacturing and beyond. Large efforts world wide are currently delivering improvements in a variety of areas, such as exposure tools, reflective optics, sources, reticle manufacturing and resist development. The world's first 0.25 NA EUV full field scanner is now built and initial imaging performance results were reported [1]. IMEC is currently (August 2006) installing such an Alpha Demo Tool (ADT) from ASML in its 300mm research facility. Based on this infrastructure, a research program on EUV lithography has started at IMEC, focusing on EUV resists and process, EUV reticles and ADT performance monitoring. As such, the program is intended to tackle the main challenges for EUV as identified during the previous EUVL Symposium (2005, San Diego). This paper will discuss the obtained imaging performance of the ADT at IMEC and the progress made in the research program on EUV lithography.

EUV resist, or more specifically the issue of simultaneously addressing resolution, dose, and LER in resists, is currently identified as the number one critical issue for EUVL implementation. In preparation for a resist process for the ADT, resist screenings have been carried out using EUV interference lithography. By its superior aerial image contrast, this provides excellent resolution [2] (<20nm in PMMA) allowing to investigate the limits of resist performances. Best resolution demonstrated in chemically amplified resist with the interference set-up at PSI is 30nm L/S [3]. However, as flare is high in EUV, intrinsically and especially on the first full field scanners (flare levels \>10%), the obtained image in resist will be affected. Presently the effect of flare on the resist performance is under investigation through contrast demodulation experiments on the interference set-up. Based on the performance data, a resist process will be selected and implemented on the ADT tool.

Availability of defect-free reticle handling and protection during storage and use, in the absence of a conventional pellicle, is another critical challenge for EUV. Early experiences with the reticle handling procedure designed for the ADT will be reported. The additional reticle requirements specific for EUV and the status of the EUV mask making infrastructure will also be reviewed. Other near-term project work includes preparation for a defect printability study on the ADT.

Finally the status of the ADT will be reviewed and first imaging

performance will be discussed. The ADT is designed to print down to 30nm isolated and 40nm dense lines, and 55nm contact holes. Results from the IMEC ADT including critical dimension uniformity (CDU), horizontal-vertical difference, and contact hole ellipticity will be presented.

[1] H. Meiling, et al, Proc. SPIE 6151 (2006), 615108

[2] Roel Gronheid et al, Microelectronic Engineering 83 (2006), 1103-1106

[3] A.M. Goethals et al, J. Photopolym. Sci. Technol., vol.19 N0 4 (2006), 501-506

6517-09, Session 3

Fast simulation of buried EUV mask defect interaction with absorber features

C. H. Clifford, A. R. Neureuther, Univ. of California/Berkeley

To simulate the interaction of buried defects and absorber features in EUV masks, a prototype 2D, fast, integrated, simulator based on ray tracing and a thin mask model is presented. This simulator allows rapid assessment of the effects of buried defects on EUV printing. Rigorous computational electromagnetic methods can be used to simulate the mask, but are very slow. This new method gives a 50x-100x speed increase compared to Finite Difference Time Domain (FDTD) simulators.

The propagated thin mask model for absorber layout transmission, proposed in [1], has been generalized to accurately model varying angles of incidence and absorber thicknesses by examining the even and odd orders of an isolated absorber edge. This generalized absorber simulator has been linked to the ray tracing multilayer simulator, presented in [2], to simulate interactions between buried defects and absorber features. This linked program consists of three steps: the inward push, the buried defect interaction, and the outward push.

The inward push consists of simulating a single plane wave through only the absorber pattern by running the absorber simulator once. For the buried defect interaction step, the resulting near field from the inward push is Fourier transformed into plane waves and each plane wave, that must be considered based on the NA of the system, is used as an input for a multilayer simulator run. The near fields output by the multilayer simulator are summed producing the near field that must be pushed back up through the absorber layout. For the outward push the near field output by the previous step is Fourier transformed and each appropriate plane wave is used as the input to an absorber simulator run. The output of each of these runs is summed to give the complex near field reflected by the mask.

Simulation examples will be given that demonstrate the accuracy of the overall simulator. The nature of the fields after each step in the program will also be examined. This will help isolate the effects of the absorber layout and the buried defect on the final field which will assist the creation of a fast 3D mask simulator and the development of techniques to correct for the effects of the buried defects. Specific examples for varying defect sizes and locations in relation to the layout absorber will also be given.

References:

[1] M.C. Lam, ‘Fast Simulation Methods for Non-Planar Phase and Multilayer Defects in DUV and EUV Photomasks for Lithography,’ Ph.D. Dissertation, University of California at Berkeley, 2005.

[2] M.C. Lam and A.R. Neureuther, ‘A 3D substrate and buried defect simulator for EUV mask blanks’, Proc. of SPIE, vol. 5751, 2005.

Acknowledgements:

This research was funded by a grant from Intel.

6517-10, Session 3

EUV MET printing and actinic imaging analysis on the effects of phase defects in wafer CDs

H. Han, SEMATECH, Inc. and Samsung Electronics Co., Ltd. (South Korea)

Recently, EUV lithography has been gradually developed and the industry is now progressing toward Beta EUV lithography processes. However, very little has been reported on the effects of phase defects on wafer CD, and on tolerable defect sizes.

We have fabricated program defect masks with programed substrate pits and absorbing line patterns using two different methods. The substrate pit depth ranged from ~2-3 to ~6-10 nm and the FWHM varied from 45 to 150 nm. One one mask, the line-pattern was created using an e-beam writer on an absorber layer; on the other mask, a line-pattern was etched into the reflective multilayer coating using focused-ion beam (FIB) milling.

In this paper, we will present an analysis of the measured relationship between phase defect size and CD change using data obtained with an EUV micro-exposure tool (MET) and from an actinic imaging microscope at Lawrence Berkeley National Laboratory. Based on these results, we derive mask blank specifications regarding substrate defect size at the 32-nm half-pitch node.

This research is supported by SEMATECH, Samsung, Lawrence Berkeley National Laboratory, and Lawrence Livermore National Laboratory.

6517-11, Session 3

EUV and non-EUV inspection of reticle defect repair sites

K. A. Goldberg, Lawrence Berkeley National Lab.; A. Barty, Lawrence Livermore National Lab.; P. Seidel, SEMATECH, Inc.; R. Fettig, NaWoTec GmbH; P. A. Kearney, H. Han, O. R. Wood II, SEMATECH, Inc.

The production of defect-free mask blanks for extreme ultraviolet (EUV) lithography is a central challenge that can only be met if mask inspection tools of unprecedented sensitivity can be created and qualified in time for volume production. Presently, it is an open question whether or not EUV inspection tools will ultimately be required. One area where EUV at-wavelength inspection, also called actinic inspection, has recently provided unique feedback is in the evaluation of EUV multilayer coating defect repair efforts.

It is well known that the resonant reflectivity of EUV multilayer coatings is highly sensitive to any disturbance of the coating surface or layer structure: including substrate bumps and pits which cause phase-defects, and absorbing particles or surface material which causes local reflectivity loss. Multilayer defect repair efforts seek to restore the local optical properties of the multilayer and minimize the impact of coating imperfections on printed patterns. The development of effective defect-repair techniques requires detailed feedback that, realistically, can only come from at-wavelength evaluation. Non-EUV inspection tools may be able to verify the restoration of the top surface quality, but they are insensitive to the multilayer properties that de¬ter¬mine the EUV reflectivity. EUV printing can be an effective evaluation technique where available, but it is unlikely to provide accurate, quantitative feedback for open-field defect repairs.

In an effort to evaluate different multilayer defect repair methods and recipes, we have recently scanned defect repair sites on an EUV mask blank with the actinic mask inspection tool at Lawrence Berkeley National Laboratory using both actinic brightfield (BF) and darkfield (DF) dectection with sub-micron spatial resolution and sensitivity to reflectivity variations as small as 0.2%, as shown in Table 1. Interestingly, some repair sites that exhibit large BF reflectivity losses have very small DF scattering strengths. Furthermore, we did not observe a strong predictive correlation between DF scattering and BF reflectivity loss, as shown in Figure 1. This observation has important implications for the design of next-generation EUV mask inspection tools.

In the talk we will report the cross-calibration of the EUV measurements with AFM measurements and non-EUV commercial inspection tools.

This work is funded by SEMATECH, Carl Zeiss, and the U.S. Department of Energy.

6517-12, Session 3

EUV mask-blank inspection at the SEMATECH Mask Blank Development Center with the Lasertec M7360

W. Cho, P. A. Kearney, SEMATECH, Inc.; E. M. Gullikson, Lawrence Berkeley National Lab.; A. Jia, SEMATECH, Inc.; T. Tamura, A. Tajima, H. Kusunose, Lasertec Corp. (Japan); C. Jeon, SEMATECH, Inc.

EUVL mask blanks must be free of printable defects. The SEMATECH Mask Blank Development Center (MBDC) is focused on driving down the defect density of EUVL mask blanks by providing a collaborative environment for EUVL mask substrate and equipment suppliers and a state of the art analytical tool set for them to improve their products. Multilayer coating, substrate cleaning, and substrate suppliers are on site improving their products with a tool set that includes defect inspection, multilayer deposition, and substrate cleaning capabilities. X-ray diffraction (XRD) and EUV reflectance measurement capability as well as focused ion beam scanning electron microscopy/energy-dispersive X-ray (FIBSEM/EDX) and atomic force microscopy (AFM) for defect characterization are on site.

The SEMATECH MBDC has just installed a Lasertec M7360 advanced EUV mask blank inspection tool. The M7360 operates at a much shorter wavelength than the previous generation of confocal scanning inspection tools (266nm vs. 488nm for the M1350). The M7360 represents a significant improvement in our defect detection sensitivity. This talk will center around the capabilities of this new tool and show initial inspection results on EUV multilayers at sensitivities well below those that have been previously reported.

6517-13, Session 3

EUVL mask substrate defect print study

J. Cullins, Y. Tezuka, I. Nishiyama, Association of Super-Advanced Electronics Technologies (Japan)

Mask substrate defects continue to be one of the critical issues for EUV technology development. Current specifications call for allowable defects in the 25nm size range for production masks blanks. Simulations seem to indicate that defects as small as 3nm high will cause printable defects on the wafer.

To study the effects of small aspect defects on the printed image we undertook a study to look at 10nm height (mask substrate size) defects. A mask was fabricated with 10nm height defects in arrays based on area. Defects of 150nm, 180nm, 200nm, 250nm, and 1000nm were fabricated. Multi-layers were then deposited and the mask was patterned with line/space patterns with pitches (mask size) of 300nm, 400nm, and 500nm.

Wafers were then exposed using a well characterized resist and the results were analyzed. All sizes of defects printed at least once. The largest defect size (1000nm mask) caused multiple bridges to form (Figure 1) while even the smallest defect size (150nm mask) could cause a bridge on the 300nm (mask size) pitch (Figure 2).

6517-14, Session 4

Atomic hydrogen cleaning of Ru-capped EUV multilayer mirror

K. Motai, H. Oizumi, S. Miyagaki, I. Nishiyama, Association of Super-Advanced Electronics Technologies (Japan); A. Izumi, T. Ueno, Y. Miyazaki, A. Namiki, Kyushu Institute of Technology (Japan)

Since the projection optics in EUV lithography require a very long reflectivity lifetime, contamination control is very important for EUV multilayer mirrors. The two primary contaminants that degrade the reflectivity of a multilayer mirror exposed to EUV light are carbon and surface oxide, which result from the photodecomposition of residual hydrocarbons and water, respectively.

Cleaning methods to remove carbon already exist, and our previous studies for carbon contamination showed that atomic hydrogen generated by a heated catalyzer consisting of a W wire removes sufficient carbon to restore the reflectivity. However, no cleaning technology has been established to reduce the oxide layer. The most promising way of suppressing the formation of surface oxide is to cap a multilayer with Ru, although its oxidation resistance is not really good enough. Therefore, a new cleaning technology which is effective against both carbon contamination and oxidation is strongly required.

In this study, to reduce surface oxide on Ru-capped Mo/Si multilayer mirrors for EUVL, we employed the same cleaning with atomic hydrogen. The atomic hydrogen generated by a heated catalyzer consisting of a W wire was applied to the surface of a Ru capping layer, which had been slightly oxidized by ECR plasma; and the effectiveness of atomic hydrogen in deoxidizing it was examined.

AES profiles of a Ru-capped Mo/Si multilayer mirror show that ECR plasma made the surface oxide thicker, and that atomic-hydrogen treatment reduced it to the initial as-deposited level. The RMS surface roughness measured by AFM indicates that oxidization with ECR plasma roughens the surface slightly, while atomic hydrogen does not. An XPS analysis of the surface composition of the Ru cap of as-deposited, oxidized, and treated samples revealed that, for typical experimental conditions, a thin Ru oxide layer was deoxidized after treatment with atomic hydrogen for several minutes. The EUV reflectivity of a multilayer mirror was also measured before and after cleaning; and atomic-hydrogen treatment was found to restore the reflectivity degraded by oxidization. These results demonstrate that cleaning with atomic hydrogen generated by a heated catalyzer consisting of a W wire is a promising way of simultaneously removing carbon contamination and reducing the amount of surface oxide on a Ru-capped multilayer mirror for EUVL, and thus restoring the reflectivity.

The transport of atomic hydrogen was attempted using a quartz tube. Although this technique may increase the time needed for cleaning, the results indicate that in-situ cleaning may be possible since transported atomic hydrogen did, in fact, reduce the amount of surface oxide. In order to find a way to increase the production of atomic hydrogen, it is worthwhile to examine the process conditions by measuring the density of hydrogen radicals.

6517-15, Session 4

Critical parameters influencing the EUV-induced damage of Ru-capped multilayer mirrors

S. B. Hill, I. Ermanoski, C. Tarrio, T. B. Lucatorto, National Institute of Standards and Technology; T. E. Madey, Rutgers Univ.; M. Chandhok, M. Fang, Intel Corp.

Ongoing endurance testing of Ru-capped multilayer mirrors (MLMs) at the NIST synchrotron facility has revealed that the damage resulting from EUV irradiation does not always depend on the exposure conditions in an intuitive way. Previous exposures of Ru-capped MLMs to EUV radiation in the presence of water vapor demonstrated that the mirror damage rate actually decreases with increasing water pressure. We will present results of recent exposures showing that the reduction in damage for partial pressures of water up to 5Å $\times$ 10-6 Torr is not the result of a spatially uniform decrease in damage across the Gaussian intensity distribution of the incident EUV beam. Instead we observe a drop in the damage rate in the center of the exposure spot where the intensity is greatest, while the reflectivity loss in the wings of the intensity distribution appears to be independent of water partial pressure. (See Figure 1.) We will discuss how the overall damage rate and spatial profile can be influenced by admixtures of carbon-containing species (e.g., CO, CO2, C6H6) at partial pressures one-to-two orders of magnitude lower than the water vapor partial pressure. An investigation is underway to find the cause of the non-Gaussian damage profile. Preliminary results and hypotheses will be discussed. In addition to high-resolution reflectometry of the EUV-exposure sites, the results of surface analysis such as XPS will be presented. We will also discuss how the bandwidth and time structure of incident EUV radiation may affect the rate of reflectivity degradation. Although the observations presented here are based on exposures of Ru-capped MLMs, unless novel capping layers are similarly characterized, direct application of accelerated testing results could significantly overestimate mirror lifetime in the production environment.

6517-16, Session 4

Sn cleaning methods for extended collector life time: an innovative approach for successful EUV lithography

S. N. Srivastava, H. J. Shin, D. N. Ruzic, Univ. of Illinois at Urbana-Champaign

Tin is the preferred fuel in EUV sources due to its higher conversion efficiency (3%) compared to Xe (1%.) However, there are several critical challenges to overcome before Sn can be used. Sn is a condensable fuel, which deposits on nearby surfaces. The light is collected in this technology using reflective collector mirrors, which are placed near to the plasma pinch area. Collection efficiency of these mirrors and their ability to direct EUV light to the intermediate focus depends heavily on its reflectivity, which in turn depends on the surface morphology and composition. Tin contamination reduces the reflectivity of the mirror surfaces. High energy tin ions or neutrals, contaminate the surface, makes it rougher and also erode it away. Due to these effects mirrors would need to be changed frequently, which increases the cost of ownership. The Plasma Material Interaction group at the UIUC is expanding efforts to develop cleaning methods for Sn off of EUV compatible surfaces. Reactive ion etching methods are developed as an effective tool for this process. An in-house RIE chamber is used to investigate Sn etching by Ar/Cl2 plasma. Gas flow rates, chuck bias, sample temperatures and the chamber geometries are being analyzed to optimize the etching. Results are very promising and encouraging towards an extended collector life time. Etch rates are measured for Sn and its selectivity is studied over SiO2 and Ru, which shows that the method adopted at UIUC for Sn etching is a potential solution to this problem. Additional experiments for cleaning Sn off a mock collector mirror geometry, shows the potential to integrate this method in real technology. A kinetic model is developed which aids of understanding the chemistries and the entire etching process.

6517-17, Session 4

Interface engineering of Mo/Si multilayers for enhanced reflectance in EUVL applications

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For commercial application in EUV lithography tools, strict requirements are posed for the lifetime and throughput of illuminator and projection optics. It is generally accepted that such requirements can be met by modifying the “traditional” Mo/Si multilayer stack by means of ultra-thin layers, to act as diffusion barriers. The resulting reduced interdiffusion at the Mo/Si interfaces creates a sharper optical contrast, thereby enhancing reflectance. Due to the inverse relation between diffusion barrier thickness and peak reflectance at EUV wavelength, the current challenge lies in understanding layer growth mechanisms in order to create ultra-thin physical and/or chemical barriers.

In this work, we present recent results on Mo/Barrier/Si/Barrier multilayers, deposited by e-beam and magnetron sputtering, with the emphasis on reflection enhancement. We study composition of the formed interlayers with XPS. We show that ultra-thin reflectance enhancement interfaces can be deposited with low added multilayer stresses. A near-normal incidence reflectivity of 70.3% at 13.5 nm was obtained in these systems. Ultra-thin barrier layers can also be applied in capped multilayers to counterbalance the inherent loss of reflectance that is often present when using thick diffusion and or protective layers in the capping system. We present new data on capped multilayers that show improved reflectivities, without sacrificing the protective nature of the capping layer.

6517-18, Session 4

Development of optics for EUV lithography tools

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Nikon is now conducting the development of projection optics and illumination optics for EUV1 which will be delivered 1st half of 2007. EUVL using radiation with very short wavelength of 13.5nm requires severe precision of optics. Wavefront error of the projection optics must be less than 1nmRMS. It is very tough to achieve such a precision in reflection optics using aspheric mirrors.

Nikon has improved figuring and metrology technology for aspheric mirrors through the development of high-NA small-field exposure system (HiNA). In the 2-mirror projection optics of HiNA, we have already achieved wavefront error of less than 1nmRMS. For the 6-mirror system of full-field EUV exposure tools, we needed further improvement of our technology. For the metrology of aspheric surface, we have developed high-precision interferometers which have measurement repeatability of less than 50pm. For the figuring process, new polishing technologies including ion-beam figuring (IBF) and elastic emission machining (EEM) have been developed in EUVA (Extreme Ultraviolet Lithography System Development Association) project. High-precision figuring process with reduced MSFR (Mid-Spatial-Frequency Roughness), that causes flare, has been successfully developed. Using these new technologies polishing of mirrors for EUV1 projection optics has been almost completed.

For the coating process, we are using ion-beam sputtering and magnetron sputtering. Process conditions of Mo/Si multilayer coatings have been optimized to obtain high reflectivity, low internal stress and graded coating, simultaneously. Performance of capping layer has been tested using a synchrotron source in NTT Atsugi and we found that durability to oxidation of Ru capping layer strongly depended on the deposition condition. Sufficient oxidation durability was obtained by optimization of deposition condition.

In the optical housings of projection optics, improved holding mechanism with very low holding deformation developed for HiNA was used. New temperature control system of mirrors with reduced deformation has also been developed.

A non-EUV wavefront metrology system and an EUV wavefront metrology system (EWMS) have been developed for adjustment of projection optics. The former is now used for the adjustment of EUV1 projection optics. EWMS, which was developed in EUVA project, has already been installed at the New Subaru synchrotron facility in University of Hyogo and we are now preparing wavefornt metrology.

Illumination optics for EUV1 consists of collimator mirrors and reflection-type optical integrators to achieve Koeller illumination condition in ring-shape illumination field efficiently. A new machining tool for the optical integrators has been installed and machining process has been developed. Fabrication of mirrors for illumination optics for EUV1 has been almost completed.

A part of this work was supported by NEDO.

6517-19, Session 5

Multilevel step and flash imprint lithography for direct patterning of dielectrics

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In modern integrated circuit fabrication, the copper interconnects that make up the Back End of Line (BEOL) electrical connectivity are often made with the dual damascene process, where several thin film, litho, and etch steps are needed to construct each copper interconnect layer. With the increasing number of interconnect layers in modern devices, as many as eight or more in a state of the art chips, the total number of BEOL processing steps increase rapidly, often exceeding 100 unit processes in state of the art devices.

Step and Flash Imprint Lithography (SFIL) coupled with directly patternable dielectric materials provides an opportunity to significantly reduce the number of processing steps in BEOL wiring. Multi-level SFIL processing allows patterning of both the trench and via levels of an interconnect layer simultaneously, and the use of directly patternable dielectrics (DPD) simplifies the subsequent pattern transfer steps. Significant reduction in cost and time can be achieved by successfully implementing the dual damascene SFIL strategy.

Successful integration requires imprint templates with multi-level interconnect features, an imprint tool with a repeatable imprint process,

and directly patternable dielectric materials. The multi-level templates have been fabricated and reported in previous work 1,2. Earlier publications disclosed the composition and properties of novel DPD materials3. Since these DPD materials will be used as both imprint material and permanent dielectric, they must meet the material requirements of both roles. The dielectric property requirements include low dielectric constant, thermal stability, and mechanical stability, while the SFIL processing necessitates low viscosity, rapid photo-induced polymerization and minimal curing shrinkage in the DPD materials.

A set of materials compatible with SFIL processing has been examined for use as DPD materials. Formulations of inorganic/organic hybrid materials derived from oligomeric silsesquioxane, siloxanes, and acrylates show promise for this application. This paper presents progress towards integrating multi-level SFIL into a copper CMP process flow at ATDF, Inc. in Austin, Texas.

1. Proceedings of SPIE (2005), 5751(Pt. 1, Emerging Lithographic Technologies IX), 210-218.

2. Schmid, Gerard et. al. J. Vac. Sc. B. 2005

3. Proceedings of SPIE (2006), 6151(Pt. 1, Emerging Lithographic Technologies X).

6517-20, Session 5

A study of imprint-specific defects in the step and flash imprint lithography process

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Researchers have demonstrated that imprint lithography techniques have remarkable replication resolution and can pattern sub-5nm structures [1]. However, a fully capable lithography approach needs to address several challenges in order to be useful in manufacturing. For successful insertion of Step and Flash Imprint Lithography (S-FIL) into IC manufacturing, the following practical process related challenges need to be addressed: (i) Printing sub-50nm structures with non-uniform pattern densities; (ii) Precise alignment and overlay with the ability to mix-and-match with photolithography; (iii) Availability of 1X templates; (iv) Achieving appropriate throughput for acceptable cost of ownership; and (v) Minimizing template and imprint process-induced defects to allow acceptable process yields. Demonstrating the ability to achieve low defect densities is one of the biggest challenges for S-FIL to be accepted in IC fabrication.

This presentation will focus on results obtained using a KLA 2132 wafer inspection with a 200nm defect detection capability. While the inspection resolution is not at the leading edge, it provides useful insight into imprint-specific defect modes. Reduction of defects arising from the template fabrication process has been recently reported in the literature [2]. This paper uses templates fabricated by standard mask processes as reported in [2] to focus on imprint-specific wafer defects.

6517-21, Session 5

Critical issues study of nano-imprint tool for semiconductor volume production

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Nano-imprint lithography (NIL) has the capability to transfer very fine patterns. As NIL was described in ITRS Roadmap in 2003, there are activities to apply NIL to semiconductor volume production at 32nm node. To apply NIL to semiconductor volume production, there are a lot of critical issues that have to be solved.

This study is about the critical issues of nano-imprint tool for semiconductor volume production.

For the scanner maker, CANON, overlay control is not a critical issue for nano-imprint lithography because CANON has many experiments from proximity X-ray lithography (PXL).

CANON can build an overlay system for nano-imprint tool using the CANON PXL's alignment and chip magnification correction technologies easily.

This study is more focused on the Cost of Ownership (CoO) considering mold life time test. The determination of CoO of NIL, and comparing EUV lithography, and clarification are the required specification of NIL from the viewpoint of productivity which are described within this study.

6517-22, Session 5

Imprint time optimization in hot embossing lithography

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Nanoimprint lithography (NIL) is henceforth known has a promising emerging lithography, as for high resolution patterns[1], as for complex 3D shapes[2]. Even tough pattern quality has reached up adequate level; industrial use of this technology is now requesting a significant improvement of manufacturing throughput.

In this study, we have characterized reflow behaviour of thin patterned resist films as a significant parameter of hot-embossing throughput. Cooling down the resist to obtain a glassy polymer for demolding may take a too long time, even if it guarantees pattern quality. One solution consists in demolding at a temperature close to embossing temperature. Therefore, patterned resist should not reflow during this demolding at high temperature in order to keep critical dimensions, sidewall angles and minimize the top rounding effect on resist patterns.

Resists used in this study are photolithography resist, nanoimprint dedicated resist and model polymers. Advantages and drawbacks of thermo-curable resists are showed. Resist thickness has been tuned between 50 nm and 200 nm. Experiment consists in a hot-embossing step with a demolding below the glass transition temperature (Tg) (figure 1-1), followed by a high temperature post backing step and a quench (figure 1-2). This step allowed a time-controlled patterned resist reflow.

20x2mm dies with a grating of 250nm iso dense lines (figure) have been design on a 200mm stamp. Printing experiments have been performed on an EVG520(r)HE tool on 200mm substrates. Time dependant measurements were performed on a Veeco X3D Atomic Force Microscope (AFM) with flared tips[3]. This device gives accurately whole profile of patterns, and allows to access side slope and curvature of top rounding (figure 2).

It has already been showed that effective viscosity of resist may vary by several orders of magnitude as a function of its thickness[4], that is to say that thickness strongly impacts on behavior of resist flow of the nanoimprint step, but also on the demolding reflow.

Imprinting temperature demolding obviously implies a fall of pattern quality. Knowing, the temperature and time dependencies of resist flow, we will show that it is possible to choose a printing and demolding temperature and a quench velocity to keep the required pattern quality (figure 3).

We will show that the knowledge of reflow velocity according to temperature is a basic criterion of choice in order to determine the best process window for hot temperature demolding. Thanks to our approach we will be now able to optimize the process throughput by determining the one temperature high enough to have a good printing and low enough to have a quick demolding.

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[2] Beauvais, J., Lavalleé, E., Zanzal, A., Drouin, D., Lau, K.M., Veres, T., Cui, B, "Fabrication of a 3D nano-imprint template with a conformal dry vapor deposited electron beam resist", Proc SPIE, 5751 (I), pp. 392-399

[3] Foucher, J., Miller, K., "Study of 3D metrology techniques as an alternative to cross-sectional analysis at the R&D level", Proc. SPIE, 5375(I), pp. 444-455

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6517-23, Session 6

Laser-produced EUV light source development for HVM

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The key technologies developed at EUVA for HVM EUVL are a RF-excited CO2 drive laser and a Sn droplet target. This approach enables cost-effective high-conversion efficiency (CE) and power scaling. The RF-excited CO2 laser has a MOPA (master oscillator power amplifier) configuration and operates at a repetition rate of 100kHz. The Sn droplet target has been optimized for the drive laser including droplet size and speed. The development status of the key technologies and the system performance will be described in detail. In addition, topics relevant for HVM including mirror lifetime, i.e. debris and magnetic ion mitigation, and the future light source development towards 115/180W will be outlined.

This work was supported by the New Energy and Industrial Technology Development Organization (NEDO), Japan.

6517-24, Session 6

EUV source development for high-volume chip manufacturing tools

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Xenon-fueled gas discharge produced plasma (DPP) sources were integrated into Micro Exposure Tools already in 2004. Operation of these tools in a research environment gave early learning for the development of EUV sources for Beta-Tools. Further experiments with these sources were performed for basic understanding on EUV source technology and limits, especially the achievable power and reliability. The intermediate focus power of Beta-Tool sources under development is measured to values above 10 W. Debris mitigation schemes were successfully integrated into the sources leading to reasonable collector mirror lifetimes due to the effective debris flux reduction. Source collector mirrors, which withstand the radiation and temperature load of xenon-fueled sources, are under development to support intermediate focus power well above 10 W. Temperature measurements of the collector mirrors have been performed for verification.

To fulfill the requirements for High Volume chip Manufacturing (HVM) applications EUV sources with higher efficiency are under development. The fuel of these sources has been selected to be tin and the conversion efficiency is 2-3x higher compared to xenon. New excitation schemes allow for the efficient power injection into the plasma.

To extend the lifetime of the electrodes significantly, the static electrode systems of Beta-Tool sources are replaced by rotating electrodes. The EUV power achieved from these sources today in combination with the collector mirrors developed for the Beta-Tool sources should support 50 W intermediate focus power. Development work is ongoing to increase the power directly from the DPP source by 2.5x. Simulations of the source-collector performance at this higher power levels is under preparation. Power and lifetime scaling considerations as well as the progress in the development of the HVM source technology made at XTREME technologies for HVM applications will be presented.

6517-25, Session 6

LPP EUV source development for HVM

D. C. Brandt, I. V. Fomenkov, A. I. Ershov, N. R. Bowering, A. N. Bykanov, G. O. Vaschenko, W. N. Partlo, D. W. Myers, Cymer, Inc.

This paper provides a detailed review of development progress for a laser-produced-plasma (LPP) extreme-ultra-violet (EUV) source with performance goals targeted to meet joint requirements from all leading scanner manufacturers. We present the latest results on drive laser power and efficiency, source fuel, conversion efficiency, debris mitigation techniques, multi-layer-mirror coatings, collector efficiency, intermediate-focus (IF) metrology, mass-limited droplet generation, laser-to-droplet targeting control, and system use and experience. Results from several full-scale prototype systems will be presented. In addition, a multitude of smaller lab-scale experimental systems have also been constructed and tested. This presentation reviews the latest experimental results obtained on these systems with a focus on the topics most critical for an HVM source.

Laser produced plasma systems have been researched as a probable candidate for light-source to an EUV scanner for optical imaging of circuit features at 32nm and beyond nodes on the ITRS roadmap. LPP systems have inherent advantages over alternate source types, such as Discharge Produced Plasma (DPP), for power scalability, etendue, collector efficiency, and component lifetime. The capability to scale LPP power with repetition rate and modular design will be shown. A path to meet requirements for production scanners planned well into the next decade will be presented.

This paper will include current testing results using a 320mm diameter normal incidence elliptical collector, now in it's second year of operation. With the collector in-situ, intermediate focus (IF) metrology capability is enabled, and data will be presented that describes the quality of light at IF. Debris mitigation designs and lifetime testing of the coated multi-layer-mirror (MLM) will be described and used to support the useful lifetime estimation of the device.

6517-26, Session 6

Recent developments on the Philips' EUV source

M. Corthout, J. Pankert, Philips GmbH (Germany)

In the talk, recent developments of the Philips' EUV source will be presented. The source is built on the Sn based vacuum sparc concept, whereby a laser triggers a gas discharge between two Sn containing electrodes. The laser is at the same time ablating the right amount of Sn wherein the discharge happens.

The electrodes rotate to enable very high power loads. Moreover, they are covered with a liquid Sn film with a built-in regeneration mechanism. This enable long-life of the electrodes.

The talk will specifically address the following sujects:Scaling of the output power, lifetime of the electrodes, debris mitigation, collector lifetime.

Finally, results on the sources that are integrated in the EUV scanners will be presented.

6517-27, Session 6

Tin inventory for HVM EUVL sources

M. C. Richardson, K. Takenoshita, T. Schmid, College of Optics & Photonics/Univ. of Central Florida

Tin is shown to be the most efficient source material for producing emission into the 13 nm region, with both gas discharge plasma sources and laser produced plasma source schemes being developed for EUV lithography [1, 2]. Unlike Xenon, which was the material commonly investigated for the EUVL source application, recycling of the target materials is not necessary for tin due to its relative abundancy in nature, thus low cost and availability . However, in assessing the benefits of different source architectures, there are large differences in the size of the tin inventory used, and there are consequences that ensue. In this paper, we make a first attempt to compare these differences, and assess the impact on the source component projection for the stepper tool.

Our approach to developing a tin-doped droplet laser plasma source uses a mass-limited target concept [3] that not only minimizes the debris produced from plasma generation, but also the total amount of tin used. A single droplet target contains only about 10e13 tin (~ 2 ng) atoms. For a 30 kHz source satisfying HVM requirements, it is estimated that the total mass of tin used over a 30,000 hr source lifetime to be about 6 kg. We compare this inventory of tin to that used in current source configurations under development by source suppliers. By comparing 1 micro gram usage of tin in a gas discharge plasma source [4], the tin-doped droplet target consume a factor of 500 less tin than

the configuration. By comparing tin liquid droplet target with diameter of 100 microns [5] which should contain about 2e16 (~ 2 micro grams) tin atoms, the tin-doped droplet target consumes only a thousandth of the tin content in the liquid tin droplet. Even if the lower operation frequencies which are considered for application with these source configurations, the total amount of tin over the specified source lifetime will exceed 100 kg. Thus, as proven here, the mass-limited source scheme is a necessity, not only for debris, but also to provide sufficient tin inventory for the specified source operation life.

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6517-28, Session 6

Microdischarge EUV-source array and illuminator design for a prototype lithography tool

B. E. Jurczyk, R. A. Stubbers, D. A. Alman, Starfire Industries LLC; R. M. Hudyma, M. Thomas, Hyperion Development LLC

The joint specification projected in-band EUV power requirements at the intermediate focus will rise beyond 185W 2%-bw to maintain the necessary 80-100WPH throughput for economic viability. New improvements in photon efficiency and mask illumination are needed to reduce reflections and power demand, as well as improving source spatial uniformity.

In 2006, Starfire Industries presented a microdischarge plasma light source concept for consideration as a potential HVM solution for high-power spatial and temporal multiplexing. Using a distributed array architecture, thermal and particle loadings become manageable when spread over 100s to 1000s of discrete units allowing power scalability. In addition, a key tenant is the potential for novel collection and illumination geometries that could simulate Kohler and pupil fill effects found in conventional fly's-eye mirror systems; thus leading to a reduction in optical elements and a factor of 2-4 increase in total throughput.

A top-level illuminator optical design based on the microsource array technology is presented, as well as projections for illumination efficiency, reticle uniformity, partial coherence and uniformity of the pupil fill for a realistic EUV source array. In addition, experimental data from xenon-based sources will be presented with a suite of plasma and optical diagnostic instruments, including conversion efficiency, spectral purity and debris generation.

6517-29, Session 7

Initial experience establishing an EUV baseline lithography process for manufacturability assessment

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The International Venture for Nanolithography (INVENT) initiative announced in mid 2005, a very unique industry-university consortium between the College of Nanoscale Science and Engineering (CNSE) at Albany and leading edge integrated device manufacturers (IDM's) has initiated an extensive R&D program on EUV lithography.

The overall status and scope of the INVENT program, our assessment of the major challenges to establishing a baseline EUV process on a full field scanner and the progress made on some of the critical issues will be presented. Details of our experience evaluating EUV photoresists, reticle handling and contamination are covered. A custom test reticle design including flare, focus uniformity, resolution and aberration characterization will be described. The methodologies for EUV process evaluation and control as well as some of the EUV-specific characterization techniques required for EUV optics will be included.

The relative performance limiters for 32nm (and beyond) EUV lithography will be reviewed versus other studies presented prior to the availability of full field EUV tools.

Finally, with this model for strategic partnering, an outlook to bring EUV lithography to manufacturing readiness will be presented.

6517-30, Session 7

Recent results from the Berkeley 0.3-NA EUV microfield exposure tool

P. P. Naulleau, Lawrence Berkeley National Lab.; C. N. Anderson, Univ. of California/Berkeley; K. R. Dean, SEMATECH, Inc.; P. E. Denham, K. A. Goldberg, B. Hoef, Lawrence Berkeley National Lab.; B. M. La Fontaine, T. I. Wallow, Advanced Micro Devices, Inc.

Operating as a SEMATECH resist test center, the Berkeley 0.3-NA EUV microfield exposure tool1 continues to play a crucial role in the advancement of EUV resists and masks. Here we present recent resist characterization results from the tool as well as tool characterization data. The tool-characterization data includes lithographic-based aberration measurements demonstrating the long-term stability of the tool.

6517-31, Session 7

EUVL mask dual pods to be used for mask shipping and for mask handling in exposure tools

Y. Gomei, Canon Inc. (Japan); K. Ota, Semiconductor Leading Edge Technologies, Inc. (Japan); J. Lystad, D. L. Halbmaier, Entegris, Inc.; L. He, SEMATECH, Inc.

In Extreme Ultra-Violet Lithography (EUVL), the light is so absorptive that mask protection membrane (pellicle) cannot be used. A way to solve this issue is that mask carriers are specially designed to protect masks from particle contamination. In this scheme, EUVL masks are final-cleaned in mask houses, put in the carrier, shipped to wafer Fabs and then directly loaded to exposure tools for use. The tool operates in vacuum to avoid EUV absorption, so the mask has to be protected from particles during pump-down in a tool load-lock chamber. A dual pod concept has been proposed, and the inner pod is capable to accommodate the pump-down process1. The mask is located by the orientation in which the pattern side faces to the inner pod base plate for protection. The mask is transferred from the load-lock chamber to a mask stage in this orientation. The inner pod cover is removed somewhere in-between, and the mask is finally set to an electro-static chuck of a mask stage. We thought that this dual pod concept is also applicable for mask shipping and decided to build hardware for testing.

We have chosen to use RSP200 (Reticle SMIF Pod) as an outer pod. The load-lock chamber of exposure tools is interfaced to RSP 200, and only the inner pod is transferred into the chamber. The inner pod cover is made of a vacuum-compatible nonmetallic material, and the base plate is aluminum. The cover has a rout for gas transport with particle filtering function. The mask is supported by pads which are located on the corners of the inner pod base plate. The mask is confined from movement during shipping by additional support mechanisms, the force of which is applied by closing the RSP 200 upper cover. We have carefully selected a material for these contact positions by carrying out tapping, scratching and model shipping tests. We have also tested a few materials about outgassing to select the best for the inner pod cover.

Figure 1 shows the shipping test results. A mask substrate was packed in the carrier and shipped back and forth between Albany, NY and Austin, TX. The substrate was inspected for particle adder with the highest sensitivity of 54 nm PSL equivalent. The alpha and beta carrier shown in the figure was only slightly different to accommodate manual handling. New Pozzeta boxes were used as witness. The Pozzeta results show consistent performance of our test. Our carrier showed

zero adder in 5 out of 8 cases with average of 0.6 adders per shipping. We believe that some adders were from manual handling of mask substrates. Inner pod vacuum test was also conducted at SEMATECH. The inner pod with a mask substrate was evacuated to 4 mTorr in 90 s and then pressurized. Particle adder in a multi-cycle test was 0.3/cycle. These results clearly indicate that our dual pod is highly feasible to use for both mask shipping and handling in exposure tools. Further work is being continued.

Reference:

1. B. Blum, et al., presented in 1st Int. EUV Lithography Symposium, Dallas, 2002 (distributed by CDROM from International SEMATECH).

6517-32, Session 7

Assessment of optimal focus point in EUV lithography

M. Sugawara, Sony Electronics Inc.

In extreme ultraviolet lithography (EUV), off-axis incident light on a reflective mask causes a difference of phase between plus and minus order diffracted rays on a pupil plane in the projection optics. The difference of phase brings about a shift of the center position of the printed images and degradation of symmetry of contrast at the edges of patterns 1), as if coma aberration might be on the pupil plane.

In this study, we focused on how the difference of phase between plus and minus order diffracted rays affected the optimal focus point by using TEMPEST simulator. Phase at the pupil was obtained by using Fourier transform of light intensity distribution on a mask surface for line-and-space patterns in considering various pitches. Modified illuminations, annular and dipole, were applied to evaluate the printed images for a numerical aperture (NA) of 0.25, because the modified illuminations partly block 0th-order diffracted rays so that an impact upon the optimal focus point increases. We also used normal illumination condition as a reference.

Figure 1 shows an example of the phase distribution which is obtained by taking the Fourier transform of the light intensity distribution on a mask surface for TE polarization. TM polarization provides the same distribution as TE does. Here, the phase of 0th-order rays is set to 0°. The critical dimension is 44 nm with a pitch of 88 nm by unit on wafer. For the phase distribution in Fig. 1, the direction of the projection vector of off-axis incidence onto a mask surface is perpendicular to the absorber edges. The Fourier transform of the asymmetric light intensity distribution on the mask surface yields the difference of phase between plus and minus order diffracted rays on the pupil plane in a far field as shown in Fig. 1. The printed image on wafer is obtained by taking inverse Fourier transform of the diffracted rays. The optimal focus point for the dense pattern is different from that for the sparse pattern, because the pattern pitch determines the orders of the diffracted rays to create the printed image on wafer.

Next, we observe the symmetrical phase distribution for parallel configuration in which the direction of the projection vector of off-axis incidence becomes parallel to the absorber edges. Since the phase distribution of diffracted rays in parallel configuration is different from the distribution in perpendicular configuration, the optimal focus point becomes different between parallel and perpendicular configurations.

This paper will make clear what magnitude of difference of the optimal focus points is allowable for the specifications of depth of focus.

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6517-33, Session 7

Electrostatic chucking of EUVL reticles

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EUVL, a promising next-generation lithography technology, is under development to be used for the sub-32 nm node. Electrostatic chucks will be used in the exposure tool in order to support and flatten the mask to the required specifications as per the EUVL Mask and Chucking Standards, SEMI P37 [1] and SEMI P40 [2]. Understanding and characterizing the clamping ability of the electrostatic chuck and the effect on the mask flatness is therefore a critical issue. To facilitate this study, finite element (FE) models have been developed to simulate electrostatic chucking and to obtain predictions of the final pattern surface shape after chucking. These FE predictions have been compared to experimental chucking results to establish the validity of the models. While reasonable correlation has been obtained in the past [3,4], there were several areas where improvements were needed in order to ensure repeatability and predictability. This paper summarizes the latest results that have been obtained after significant changes in the FE model as well as the experimental procedure. This research has led to an improvement in the understanding of electrostatic chucks. An EUV reticle was measured using a Zygo interferometer to obtain the frontside and backside surface flatness data. These data were processed and subsequently fitted with Legendre polynomials, which have been proven to be effective in representing square EUV substrate surface shapes. Flatness data for an electrostatic chuck (Fig. 1) were also obtained and were also fitted with Legendre polynomials. These polynomial coefficients for the reticle and the chuck were used to input the initial surface shapes for the FE modeling. Electrostatic chucking was simulated using a coupled electro-mechanical FE model of the reticle and chuck. This model accounted for electrostatic forces that vary as a function of the nonflatness of the chuck and backside surfaces as the reticle is being chucked. Electrostatic chucking experiments were conducted in a cleanroom facility to minimize contamination due to particles. This set-up is shown in Fig. 2(a). The previously measured chuck was placed on the 3-point mount (Fig. 2(b)) and the reticle was lowered on to the chuck in vacuum using the motorized reticle lifter (Fig. 2(b)). Voltage was applied to the chuck and the measured flatness of the final chucked pattern surface (Fig. 3) was compared to the FE simulation predictions. Repeatability studies were also performed using varying voltages (pressures). The main objective of this research is to assess the capability of electrostatic chucks to reduce low-spatial frequency mask flatness variations and to validate the numerical models developed at the UW-Madison. Experimental and numerical data will be used to assist in the implementation of the SEMI EUVL Mask and Chucking Standards.

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6517-34, Session 8

Technology mapping technique for enhancing throughput of multi-column-cell systems

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Character projection (CP) is utilized for maskless lithography and is a potential for the future photomask manufacture. Throughput of the CP is much higher than the variable shaped beam (VSB) projection. The throughput of the CP is, however, needed to be improved, compared with the throughput of photolithography.

The CP lithography has been studied especially for a single column-cell (SCC) system. The weak point of the SCC-based CP lithography is that not all logic cells used for IC design can be placed on a CP mask. The logic cells off the CP mask must be projected with VSB projection. This VSB projection deteriorates the throughput of the equipment.

It is natural to adopt multiple column-cells for higher throughput of projection equipment. A multi-column-cell (MCC) system, which has multiple column-cells as shown in Figure 1, is one of the solutions to the low throughput of CP lithography. It accommodates several column-cells, each of which has an electron gun and a CP mask for projecting chips in parallel. Parallelizing projection with multi-column-cells contributes to higher projection throughput. Simply speaking, projection throughput is proportional to the number of column-cells.

For MCC systems, a CP mask set of a column-cell is not necessarily same as that of the others even if multiple column-cells are utilized to project in parallel. We have proposed a CP mask development methodology for MCC systems [2] and a mathematical optimization [3]. The CP mask development methodology builds multiform CP masks for a layer and loads as many logic cells on CP masks as possible. In the methodology, frequently-referred logic cells are projected with many column-cells, moderately-referred logic cells with a few column-cells, and infrequently-referred logic cells with the VSB method. The objective of this CP mask development methodology is not to generate a netlist but to build the optimal CP masks for minimizing projection time for a given netlist.

In this paper, we present a technology mapping technique for MCC systems, which generates an optimal netlist for minimizing projection time. Formerly, we proposed a technology mapping technique for SCC systems [1]. The technology mapping technique for SCC systems is not directly applicable to MCC systems because building multiform CP masks for a layer causes necessity of balancing projection time between all column-cells. We have developed a logic cell library generator for optimizing design area, delay as well as projection time in logic synthesis. In our experiments, the technology mapping technique has achieved about 20 % less projection time than a conventional one. We will present more detailed experimental results in our camera-ready paper.

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6517-35, Session 8

Stage position measurement for e-beam lithography tool

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With an evident requirement for Gaussian electron beam direct write lithography for prototyping and development on 300 mm substrates below the 45 nm node, Vistec Lithography Limited (Vistec) began the development of a new tool. A key requirement of this tool development was the integration and use of an interferometry solution for stage position measurement. As existing products had shown limitations in their practical application and performance, a new solution was sought by the design team. Vistec entered into a development programme with Renishaw plc (Renishaw) to utilise their newly developed interferometry systems, resulting in the Renishaw RLE20 differential interferometer system being integrated into the new tool.

The RLE20 consists of a fibre coupled laser source which delivers light to differential interferometer units mounted on the outside of the vacuum chamber. These differential interferometers measure the position of two plane mirror target optics, allowing a direct measurement of the stage position relative to the optical lens, thus removing translation effects of the vacuum chamber side-wall.

In this paper we will discuss the integration of the interferometry system with the electron beam lithography tool, the design requirements and their subsequent solutions. We will show the changes made to the objective lens of the system to permit the use of a reference mirror arrangement directly coupled to the electron optical lens. This arrangement provides a stable datum for the metrology system and allows easy scaling of the design.

Results will be presented comparing the new tool with the previous one, showing the enhancement made with the new stage position measurement approach. Data will be presented to show reduction in the noise measured on tool, and improvements in long term position drift.

6517-36, Session 8

Defect inspection of positive and negative sub-60-nm resist pattern printed with variable shaped e-beam direct write lithography

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E-beam direct writing on silicon wafers for critical layers is currently discussed as an option for early device and technology development as well as for fast prototyping. For logic devices this approach recently has been successfully demonstrated by integration of variable shaped beam (VSB) E-beam direct writing into semiconductor device manufacturing (1).

Throughout the last year, a center-of-competence for E-beam lithography has been established at Qimonda Dresden / Fraunhofer CNT using a variable shaped E-beam tool with a voltage of 50KV. A resolution of 50nm dense L/S has been demonstrated using negative and positive resist processes that recently have been developed within collaboration between IMS Chips and Vistec Electron Beam (2).

Due to write time limitations of E-beam lithography, defect inspection as a means for quality and process control in general is restricted by the low mean coverage of currently printed E-beam pattern. Other than in optical lithography, only minor parts of the wafer can be printed in a reasonable timeframe and the wafer throughput in general is low.

The ITRS (International Roadmap for Semiconductors) predicts the 50nm node (half pitch) to be realized in 2009 (3). By that time defect density will not be allowed to exceed 0.03 defects/cm(c)¯ (\>30nm in size).

In order to realize these targets, a special defect learning pattern including partial lattice fill structures for etch experiments was printed on 300mm wafers using chemically amplified positive and negative E-beam resists. The mean coverage on the wafer comprising L/S pattern down to 50nm was about 50% in the filled areas.

For defect inspection a dark field inspection tool with defect sensitivity down to 35nm has been used. Compared to commonly use of bright field inspection, a unique high numerical aperture dark field method was used. That comprises a higher contrast and enables a clear separation between tool related and process related defects. Particle measurements were also performed.

We will give an overview about the influence of different E-beam writing methods and strategies on defect density such as double / single pass, variable stripe widths and writing speeds on printing quality. Additionally we will demonstrate how the resist process can be optimized in order to reduce the particle load.

The overall observed defect density in general was found to be low (53 counts for the chips with fill structures (Fig. 1) vs. 140 w/o fill), mainly ruled by shot related non uniformities (stitching / butting effects) or deformed pattern close to the resolution limit of the E-beam tool. Only a small number of development related defects and particles was found.

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6517-37, Session 8

Monte Carlo simulation using voltage contrast by low-energy electron beam

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Low-energy electron beam lithography is an effective exposure tool that makes a fine pattern, because of the use of high-sensitivity resist and the slight proximity effect. However, it is difficult to detect an alignment mark located at a considerable depth from the surface because low-energy electron has a short range in the material. To solve this problem, we have examined a mark detection method using voltage contrast. It is necessary to optimize the mark structure and the detection condition in order to achieve highly accurate alignment.

In this study, using computer simulation, we have examined a mark detection method using voltage contrast. This simulator is composed of the electron scattering calculation based on the Monte Carlo simulation method, the charge movement calculation, and the potential calculation. For an elastic scattered model, we have considered the partial wave expansion method. For a non-elastic scattering process, we have considered the inner shell electron excitation, the electron excitation on valence band, the electron excitation on conduction band, and the plasmon excitation. Figure 1 shows the mark structure and the simulation result for incidence electron energy of 5keV. We obtained the voltage contrast image under low-energy electron beam condition. This result is in agreement with the voltage contrast image obtained from the experiment.

Using the simulator developed in the course of this study, turn around time (TAT) of a device development is reduced and the mark structure optimized. Moreover, this simulator, which is based on an understanding of the phenomenon of mark detection using voltage contrast, is a useful tool because it makes visible the scattering in the sample, the trajectory of the electron emitted from the surface, and the potential of the sample.

6517-38, Session 8

Alignment method of low-energy electron-beam direct writing system EBIS using voltage contrast image

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We have developed the Electron Beam Integrated System (EBIS), which is a character projection (CP) type low-energy electron-beam direct writing (LEBDW) system as a tool for QTAT of semiconductor manufacturing and maskless lithography for the small volume devices with large variety. In this system, the proximity effect due to backscattering electrons is very small on the condition that the energy of primary electron is 5 keV. It's possible to adopt the high sensitive resist process so that an improvement of throughput expected, in comparison with high energy EBDW. Besides, the very small electro-optical column with in-lens multi-deflection system and static lenses were adopted to decrease Coulomb blur of low electron beam. EBIS can reduce EB shots greatly by a character projection (CP) aperture, which is composed of hundreds of common characters extracted from standard-cell library. The CP type direct writing on EBIS can obtain the same effect as maskless writing.

However, there is the serious problem, which the signal of the mark buried under a thick insulator couldn't be detected on EBIS. To overcome this problem, we adopted the mark detection method using Voltage Contrast (VC) image. As primary electrons irradiating an insulator(resist), the sample surface is charged negatively, and then the number of detected secondary electrons according to the underlayer structure helps us to recognize whether the mark were buried in a insulator or not. The remaining electrons might induce the contrast of voltage level on the surface because there is a difference of a discharge rate by the space charge conduction between the positions where the mark were buried in a insulator or not.

Using the method which is mentioned above, in fact we detected the alignment mark signal and expose some patterns with alignment on EBIS. Figure1 shows the alignment mark image that is detected by VC method. The energy of primary electron is 5 keV. Insulators (total thickness: ~600 nm) are stacked below a thin resist. Electron beam, whose shape is 1 um squares, is scanning with a current density of 0.2 A/cm2. The mark width is 2μm. The mark image is very clear with a sufficiently high contrast. Moreover, the asymmetry originating from VC is mitigated by means of scanning back and forth.

In this paper, we will report the detail of alignment system on EBIS and alignment exposure result using VC mark detection method.

6517-39, Session 9

An electrical defectivity characterization of wafers imprinted with step and flash imprint lithography

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Imprint Lithography continues to gather traction as an alternative patterning technique for a variety of applications. As evidenced by insertion of the technology into the ITRS roadmap as a contender for the Next Generation Lithography title, semiconductor applications drove much of the early interest. More recently, however, some of that interest has turned towards other markets, most notably areas as diverse as light emitting diodes for solid state lighting applications, patterned media for portable storage, and lens arrays for optical systems.

Much of the attraction with imprint lithography relates to the perceived reduced cost of ownership for the technology which ostensibly opens the door for the ability to cheaply fabricate lower margin devices. While many variations of imprint lithography exist, one principal version is Step and Flash Imprint Lithography (SFIL). Much of the abovementioned cost advantage is realized because SFIL does not require an expensive optical system to perform exposures. Rather, the fundamental concept is similar to that of contact printing. Whereas, historically, contact printing has been studied in detail, the defectivity associated with imprint lithography has not been well characterized.

In the past, imprint defectivity studies have focused on, mostly, SEM-based inspection of templates [1], although more recent work has incorporated die-to-database comparisons on both wafers [2] and templates [3]. While this latter technique is sure to prove to be invaluable for capturing smaller defects, it has also been performed on a very small sample set. To the best of our knowledge, the work of the present study is groundbreaking in that large volumes of wafers were characterized using a variety of electrically testable devices that were imprinted and pattern-transferred in an effort to quantitatively understand defectivity issues of the imprint process from a basic, yet practical, perspective.

For this work, a 25 x 25 mm template was created with radially distributed patterns of snakes and comb structures. Variation in linewidth for the snake and comb test structures employed ranged from 50 nm to 1 μm, and other parameters including pitch and overall length were also varied. On each eight inch wafer imprinted, 29 dies were arranged. The overall goal was to be able to characterize imprint defectivity within a die, within a wafer, wafer to wafer, and lot to lot. Exemplary data depicting the variation in resistance for a 250 nm snake is shown. Material that will be covered includes comprehensive SEM and electrical characterization, optical inspection results, an analysis of the mechanisms of failure, yield results, and template lifetime findings.

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6517-40, Session 9

Pattern quality and porosity characteristics of ultra-low dielectric insulator films directly patterned by nanoimprint lithography

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Directly patterning dielectric insulator materials via nanoimprint lithography has the potential to simplify fabrication processes and significantly reduce the manufacturing costs for semiconductor devices. However, the prospect of mechanically forming these materials, especially in their porous form, raises concerns regarding their physical integrity and pore structure. We report the direct imprinting of sub-100 nm features into a high modulus methylsilsequioxane-based resin. An excellent fidelity of the pattern transfer process is quantified with nm

precision using critical dimension small angle X-ray scattering and specular X-ray reflectivity. Upon vitrification of the pattern into a hard organosilicate material above 400 °C, a modest amount of shrinkage occurs in the vertical direction of the pattern, with very little shrinkage in the lateral direction. X-ray porosimetry and positron annihilation lifetime spectroscopy measurements indicate that imprinting increases the native microporosity of the silsequioxane resin. When a porogen (pore generating material) is added, imprinting decreases the population of mesopores associated with the porogen while retaining the enhanced microporosity. The net effect a decrease in the porosity of the pattern as a function of increasing height towards the top of the pattern as well as decrease of the pore interconnectivity. There is also evidence for a sealing effect that is interpreted as an imprint induced dense skin at the surface of the porous pattern.

6517-41, Session 9

Ultra-violet nanoimprint lithography applicable to thin film transistor liquid-crystal display

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Thin-film transistor liquid-crystal display (TFT-LCD) can be easily found in products as cellular phones, monitors, and television (TV). LCD-TVs are expected to occupy the largest flat-panel display (FPD) market share. However, for adoption to become popular, the price of LCD-TV must be reduced, which will be made possible through higher yields or lower process costs. Thus, new low-cost processes are strongly required for enabling the production of higher-quality TFT-LCD panels at affordable price points.

Several emerging lithographies such as extreme ultraviolet (EUV) lithography, Maskless lithography (ML2), nanoimprint lithography (NIL) [1-4], etc. have been developed in efforts to reduce feature size below 100 nm in semiconductor application. Among them, NIL is known as a low-cost method of fabricating nano-scale patterns as small as 6 nm. In this paper, we present a very large-area (\> 20 inch) ultraviolet nanoimprint lithography (UV-NIL) process as a breakthrough strategy for TFT-LCD industry. The large-area UV-NIL process is a promising alternative for the expensive conventional optical lithography for production of TFT-LCD panels.

We propose a very large-area UV-NIL process using a hard stamp in a low vacuum environment for TFT-LCD patterning. Vacuum environment is employed to ensure that air bubble defect is not formed during imprinting. Overlay is going to be a very critical issue as we start using very large size stamp and substrate. Compared to the soft stamp made from polymer, the hard stamp made from quartz or glass can decrease misalignment error due to deformation and distortion of stamp during loading and imprinting.

The micro-scale patterns as small as 1um on a flat glass stamp are fabricated using laser writing lithography and reactive ion etching (RIE). Low-viscosity resin droplets with a nano-liter volume are dispensed on the stamp or a glass substrate. The overlay is achieved by aligning the stamp and the substrate. Following pressing of the stamp, the stamp is illuminated with UV light to cure the resin; and then the stamp is separated from patterned resist layer on the substrate. Finally RIE treatment removes the residual resist in the compressed area ready for further process.

In this paper, UV-NIL process and its apparatus for TFT-LCD patterning is presented. As shown in Figure 1, it is demonstrated that the glass stamp can be used for imprinting 20 in. substrates on single-step UV-NIL in a low vacuum environment. Experimental results demonstrate the potential of our approach as a low-cost lithography applicable to flat panel display.

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6517-42, Session 9

Toward 22 nm for unit process development using step and flash imprint lithography

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Imprint lithography has been shown to be an effective technique for replication of nano-scale features (1). When the imprint material is a photocurable liquid, it is possible to perform the patterning process at low temperature and ambient pressure, which enables accurate overlay and reduces process defectivity (2). The resolution of the imprint approach is strictly dependent on the ability to create a 1X master template, and improvements in resolution can be achieved without new optical systems or photoresist materials. In this sense, imprint lithography is a multi-generational technique that can be used to facilitate device and process prototyping at several upcoming lithography nodes. This paper will provide a detailed description of processes that have been used to create imprint templates for patterning features relevant to semiconductor lithography at or below the 32 nm node. The prospects for extending the template fabrication process to 22 nm and below will also be discussed.

Step and Flash Imprint Lithography (S-FILTM) makes use of templates that can be fabricated with the same patterning and etch transfer processes that are used for manufacturing phase-shifting photomasks. Several commercial mask houses now accept orders for S-FIL templates, which are generally patterned at 1X using shaped-beam pattern generators. While shaped-beam tools achieve high throughput, Gaussian-beam tools offer a significant improvement in resolution. In this study, Gaussian beam tools were used to expose both ZEP520A positive resist and HSQ negative resist at 100 kV. The targeted feature types were chosen to be representative of a range of structures that are found in semiconductor devices, and were sized to meet the anticipated requirements of future lithography nodes. These features were patterned over large areas, and proximity effect corrections were applied.

Resolution in ZEP520A was enhanced by thinning the resist to 70 nm and applying a negative bias to the critical features. Initial tests at a critical dimension of 40 nm confirmed that process latitude improved significantly when using negative bias as large as 20 nm. The methodology was applied to both 28 and 32 nm features.

To fabricate a template, pattern transfer processes including a chromium and fused silica dry etch process were employed. Imprinted features as small as 28 nm from templates made using a combination of an enhanced ZEP520A resist process and a high resolution template pattern transfer process previously described were clearly resolved. The process latitude gains from e-beam written resist features carried over directly to the imprinted features.

Further enhancements to the template fabrication process are possible by either improving the resolution of the ZEP520A or by using a high resolution HSQ negative resist. Well defined HSQ 20 nm patterns defined on a chromium-on-glass substrate were obtained. 22 nm patterns were also defined in ZEP520A resist. Additional methods for further enhancing the resolution of ZEP520A will also be discussed.

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6517-43, Session 9

Soft UV-based nanoimprint lithography for large-area imprinting applications

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UV-based Nanoimprint Lithography (UV-NIL) offers several decisive technical advantages concerning overlay alignment accuracy, simultaneous imprinting of micro- and nanostructures and tool design

due to the absence of high imprint pressures and thermal heating cycles. Thus, this technique provides low-cost solutions for R&D institutes and small businesses to compete in emerging patterning technologies. A variety of potential applications has been demonstrated using Nanoimprint Lithography coming from different application fields like semiconductor technology, photonics and biotechnology (e.g. SAW devices, vias and contact layers with dual damascene imprinting process, bragg structures, patterned media, and microfluidics) [1,2].

UV-NIL offers two approaches for patterning using either rigid quartz glass stamps (Hard UV-NIL) or soft stamps (Soft UV-NIL) for structuring of UV-sensitive resists resulting in an etching mask for the substrate to be patterned.

Due to the variation in the thickness of substrates and the rigid quartz glass stamps in Hard UV-NIL, the area patternable with one imprint step is limited to about 25x25 mm(c)˜. Therefore, in order to pattern on 300 mm wafer scale a step and repeat process must be used. In Soft UV-NIL processes elastomeric stamps (in most cases made of PDMS [3]) are used which are able to compensate for any surface roughness and curvature of substrates to be imprinted offering thereby the possibility to pattern on wafer scale within one imprint step only. This method is preferred over Hard UV-NIL for applications where a continuous pattern (1) without any stitching errors is needed, (2) relaxed specifications of the alignment accuracy may be applied and especially (3) where an increase in device size increases the functionality of the device. The main process steps in a Soft UV-NIL process are spin coating a UV-curable resist (e.g. AMONIL) onto the substrate, imprinting with the flexible stamp including optical alignment of stamp and substrate, curing of the resist by UV-exposure directly through the transparent stamp and the subsequent separation of stamp and substrate. These process steps need to be fully automated for production of small and medium sized device quantities with reproducibility at industrial standards. Imprinted features with a resolution of well below 100 nm (figure 1) have been achieved with Soft UV-NIL. The fabrication of the soft stamps is carried out with a dedicated stamp fabrication tool for getting stamps with a total thickness variation (TTV) comparable to an equivalent Si wafer (~ 15 µm TTV for 100 mm soft stamps). Our contribution will demonstrate automated equipment solutions for imprinting on substrate sizes of up to 150 mm (figure 2) in diameter. Recently achieved result demonstrating resolutions well below 100 nm will be presented.

6517-44, Session 10

Chemically amplified resists resolving 25-nm 1:1 line: space features following EUV exposure

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Abstract

Lower Line Edge/Width roughness, high resolution, and superior EUV-imaging quality, have been achieved using a novel class of chemically amplified resists. 25nm 1:1 line:space features in addition to sub-25nm overexposed lines have been patterned using standard coating and exposure procedures. Examining 1µm x 0.5µm windows of top-down SEM images revealed very promising LER and LWR values of 2.7nm and 4.3nm respectively, for 25nm features. This is the first chemically amplified resist to resolve 25nm 1:1 features indicating that diffusion blur can be overcome using the correct resist design approach.

Such a high performance was retained even at film thickness as low as 30nm. The main factor that influenced its performance was the post-exposure bake temperature; Relatively small variation affected dramatically the final resolution. The trade-off of the high resolution was the system's high-activation energy however, current investigation into faster versions exhibiting similar resolution will be highlighted. The EUV exposures were performed using Interference Lithography (EUVIL) at the Swiss Light Source. This paper will focus on the lithographic optimization of these resists for EUV lithography

6517-45, Session 10

Patterning performance of new molecular resist in EUV lithography

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At present, the development of high-quality EUV resists is the most critical issue in EUV lithography (EUVL) [1]. Considering resist materials, conventional polymeric chemically amplified (CA) resists have reached their performance limit [2]: The resolution is limited by acid diffusion, and the LER is too large due to the large molecules and compositional non-uniformity. A promising solution is molecular resists. A large number of them have been investigated in the search for a suitable one; but most have been found to exhibit the fatal problem of severe pattern collapse.

We reported the EUV patterning performance of a chemically amplified positive-tone resist based on a low-molecular-weight partially-protected polyphenol, namely, 4,4'-methylenebis [2-[di(2,5-dimehtyl-4-hydroxyphenyl)methyl]phenol (25X-MBSA-P) [3]. It exhibits a high contrast, a resolution of 30 nm at an exposure dose of 10 mJ/cm2, and a low LER of 6 nm (3σ) at an inspection length of 2000 nm. Unfortunately, it suffers from severe pattern collapse in dense fine-pitch patterns [3].

In this work, we designed and synthesized a new partially-protected polyphenol for which the position of the protected hydroxyl group in 25X-MBSA-P has no dispersion, and evaluated its EUV patterning performance. Imaging experiments were carried out with a high-numerical-aperture (NA=0.3), small-field EUV exposure tool (HINA) using coherent illumination (σ = 0.0) [4]. The illumination system consists of two flat mirrors, and also a spherical mirror that focuses the image of the EUV light source on a point at the pupil of the projection optics. The advantage of this system is that the image contrast is higher than that obtainable with partially coherent illumination. The light source was synchrotron radiation (SR) on the SBL-1 beamline of Super-ALIS at NTT [5]. An EUV mask with an 80-nm-thick TaGeN absorber and a 10-nm-thick-Cr buffer layer was fabricated to replicate dense sub-30-nm patterns [6].

This advanced CA polyphenol molecular resist does not exhibit serious pattern collapse. Moreover, it provides a resolution of less than 30 nm at an exposure dose of 12 mJ/cm2, a high aspect ratio of 2, and a low LER of 5 nm (3σ) at an inspection length of 2000 nm. This performance is equal to that of the best CA polymeric resist currently available.

The authors would like to thank Dai Nippon Printing Co., Ltd. for fabricating the masks, and Tokyo Ohka Kogyo Co., Ltd. for preparing the resists. The authors are also grateful to Mr. Murakami, Mr. T. Oshino, and Mr. K. Mashima of Nikon Corporation for useful discussions; the HINA set-3 optics were developed and provided by Nikon. This work was supported by NEDO.

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6517-46, Session 10

Metrology for EUV-resist outgassing using pressure-rise method

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The resist outgassing is a big concern in EUV lithography, since EUV lithography is conducted in vacuum environment, and hydrocarbon gas has a large impact on the degradation of EUV mirrors reflectivity. To develop a low-outgassing resist material, we have to develop a reliable method to measure the outgassing rate. ASET has constructed a new measurement tool for resist outgassing, which utilize pressure rise method, and applied this tool for typical EUV resist. Then the measured outgassing rate is converted to production tool condition by scaling the EUV irradiation intensity.

Ultrahigh vacuum technology and load-lock sample transfer system was utilized in this apparatus, then the background pressure was maintained to be 2 x 10-7 Pa, even when resist sample was set inside the chamber. Pumping speed was controlled by using a small opening between chamber and turbo molecular pump. These techniques helps to increase signal to background ratio which is major factor of precision. Pumping speed was directly determined by measuring pressure down speed using outgas itself from resist, since pumping speed depends on chemical species. Synchrotron radiation beamline of NTT Super ALIS was used as the light source. EUV light was monochromatized by using MoSi multiplayer mirror.

In the process of pumping speed analysis, we found that the pressure decay after when EUV light was stopped was not expressed in single exponential. So, more detailed analysis was applied assuming multi species composition for outgassing molecules. We found three component approximation is enough to explain the pressure decay. The pressure change was calculated using this multi-component pumping speed and then compared with the observed pressure change when EUV light is on and off. Then outgassing rate was determined by adjusting the calculated pressure change to the observed one.

This new apparatus and analysis method was applied to the model resist. This resist was originally synthesized in MIT Lincoln Lab. and supplied from SEMATECH as international round robin activity for resist outgassing. Outgassing rate was determined to be 1.5E+12 molecules/ cm2 · s (\@0.21 mW/cm2), which corresponds to the outgassing quantity of 3.9E+13 molecules/cm2 (\@5.6 x 1.5 mJ dose). This value is well agreed with the reported value[1], even though they uses a different measuring method, i.e., ex-situ GC-MS analysis.

To estimate the impact of this level outgassig rate in production era, we estimated the outgassing rate in production tool condition by scaling the irradiation intensity and overhead time. It was calculated to be 1.2E+15 molecules/cm2 · s (\@0.4 W/cm2 and 40% overhead collection). This value is 4 times larger than the requirement for hydrocarbon resist outgassing which is temporally proposed by ASML. Refinement of resist material to reduce outgassing speed is necessary but not so far to requirement.

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6517-47, Session 11

30-nm template fabrication for step and flash imprint lithography

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Step and flash imprint lithography (SFIL) is the most suited for semiconductor applications, so that high-resolution capability on SFIL templates needs to be demonstrated down to 30nm or even 20nm resolution.

SFIL templates fabrication can be started with a conventional 6025 quartz photomask blanks, using an established 50nm thick anti-reflective chromium film and 300nm thick EB resist, an established phase-shift mask-making process as well, to define features on the quartz substrates. This scheme provides us 100nm resolution capability, but is impractical for a high-resolution template such as 50nm features or below. There is no need for the hark-mask film of template blanks for SFIL to have an optical density or anti-reflective function. Then, a thin chrome film (such as 15nm thick) and a thin resist (such as 100nm thick) are available, and already been studied, and proved their resolution capability for down to 30nm features.

The purpose of this work is to investigate SFIL template fabrication method, i.e. blanks and its process development, to improve fabrication capability and quality of 30nm templates, and to examine extendibility of the scheme, blanks and its process, to make 20nm templates and beyond.

To obtain superior resolution and pattern quality, as for resist, ZEP520A process condition was examined and reviewed over soft-baking condition, developer chemistry, and develop recipe. Then, two hard-mask films were investigated in this work. The first one was a conventional thin Cr film and a thin ZEP520A to study its limit. And, resolution exam on this blanks resulted 50nm or slightly less in feature size, with facing difficulties in CD losses and pattern fidelity due to a large etching bias and micro-loading effect. The second one was a new one to investigate an alternative hard-mask film with a thinner ZEP520A, in order to study its capability in resolution and fidelity for 30nm and beyond.

A new hard-mask film, with a thinner ZEP520A, demonstrated 30nm capability in resolution and quality, extendibility for the beyond as well, in SFIL templates fabrication.

6517-48, Session 11

New requirements for the cleaning of EUV mask blanks

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Defect size has been traditionally used to determine killer defects and yield in the semiconductor technology. However, as a result of reducing critical device size and therefore reducing critical defect size, other factors besides defect size come into play. Extreme ultraviolet (EUV) mask blanks are especially sensitive to defects. For the 45 nm node, the defectivity requirement is very stringent, requiring the complete removal of particles larger than 27 nm from EUV substrate blanks.

However the definition of a 27 nm defect is not clear. So far only a one-dimensional parameter has been assigned to defect size, yet the size depends on the metrology technique used to measure it as well as the definitions used to describe it. It is common to use the diameter of a polystyrene latex (PSL) sphere with equivalent volume as the defect size. Therefore, the defect size is given in nm PSL equivalent volume diameter (PEVD). Most modeling work uses this approximation to calculate adhesion forces and the momentum required to remove a spherical particle from the surface.

Our recent results indicate that not only size but defect shape is a very important parameter for determining particle removal capability. Therefore, while two particles may have the same PEVD size, one particle may be easy to remove from the surface while the other particle is difficult to remove based only on their shapes. To account for a particles shape, we have introduced the particle form factor (PFF)-the ratio of the particle contact area to the effective momentum transfer area-as the key parameter for defect removal. In general, a particle of a specific size (PEVD) can be removed with traditional cleaning methods if the PFF <<1, but it cannot be easily removed if the PFF \>1. In the current paper, we present the result of our studies on sub-50 nm mask blank substrate defects and their removal, using the single defect traceability (SDT) method developed at SEMATECH. In this method, scanning electron microscopy (SEM) and atomic force microscopy (AFM) imaging are used to show defect shape data. Special SEM imaging and software are used to construct 3D images of the defect. The defect composition is identified using energy-dispersive spectroscopy (EDS). Our defect shape information is used to determine the relationship between defect dimensions on an EUV substrate and defect dimensions on a final multilayer-coated mask blank (Fig.1). Existing theoretical modeling is used to determine the maximum defect height and width on the EUV substrate that will lead to a printable defect on the EUV mask blank.

6517-49, Session 11

Experimental and simulation investigations of acoustic cavitation in megasonic cleaning of extreme-UV photomasks

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Extreme ultra-violet (EUV) lithography has become the technique of choice to print the ever-shrinking nanoscale features on the silicon wafer. For successful transfer of patterns on to the wafer, the EUV photomask cannot contain defects greater than 30 nm. Megasonic cleaning is a very successful cleaning technique for removal of particles on photomasks, but also causes a relatively high amount of damage to the fragile EUV photomasks. Though it is believed that acoustic cavitation is the primary

phenomenon responsible for cleaning as well as pattern damage, a fundamental picture of the acoustic cavitation mechanisms in play during megasonic cleaning has not yet emerged. In this study, we characterize the role of acoustic cavitation in megasonic cleaning by examining the effects of acoustic power densities, cleaning solution properties, solution temperature and dissolved gas content on cavitation via experiments and molecular dynamics (MD) simulations. MD is an atomistic computation technique capable of modeling atomic-level and nanoscale processes accurately making it well suited to study the effect of cavitation on nano-sized particles and patterns. Preliminary studies indicate a strong match between experimental and simulation results in their ability to predict the effect of solution temperature, acoustic power and dissolved gas content on cavitation.

6517-50, Session 11

Photonic band-gap masks to enhance resolution and depth of focus

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Reticle enhancement techniques are well known in the industry consisting of OPC corrections, Complimentary Alternating Aperture Phase Shift Masks, Attenuated PSM, subresolution features, etc. As geometries get ever smaller, issues associated with extending these technologies include but are not limited to such things as increased database size due to OPC and Electrical corrections, linewidth biasing in relation to pitch such as is necessary for AAPSM due to sidewall angles and intensity imbalance, chrome fingers or floating chrome due to undercut etches, multiple layouts necessary to create CAAPSM, and misregistration due to CAAPSM or sub-resolution features such as are used in inverse mask generation. The cost of applying these technologies is significantly impacting inspection and costs of the masks as resolution approaches 30 nm half-pitch climaxing with the very high cost of operations associated with Extreme Ultraviolet Lithography, EUVL, scanners and the reflective masks associated with EUVL.

We have come up with a Photonic Band Gap, PBG, mask making process that addresses these issues; reduces data handling and size, mask making difficulties and in general time to tape out and make the mask while generating extremely high contrast near field images demonstrating down to 80 nm equal line/space utilizing 248 nm illumination and 30 nm half pitch using 193 nm TE polarized illunination. Intensity imbalance as seen in CAAPSM can be virtually designed out of the mask making process and multiple mask exposures are not necessary. The PBG mask incorporates a relatively easy mask manufacturing approach and utilizes effective negative index of refraction response to enhance the overall resolution. Simulations and data in regards to intial results will be presented on this new mask manufacturing approach to enhance overall resolution and depth of focus.

6517-51, Session 11

Properties of EUVL masks depending on capping layer and absorber stack structures

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Extreme ultraviolet lithography (EUVL) using 13.5 nm wavelengths has become a leading next generation lithography technique planned to be used in the sub 40 nm regime. In contrast to the conventional lithography using transmissive and refractive optics system, EUVL employs reflective optics using mirrors and photomasks made with Mo/Si multilayers to produce a constructive interference of reflected EUV light. An EUVL blank mask consists of a low thermal expansion material (LTEM) substrate, Mo/Si multilayers with a capping layer, and absorber stacks. The desired circuit layout is transferred by removing the absorber in selected areas using e-beam writing and dry etching process, after which the mask can be used for imaging. In this paper, we present the results of an investigation of properties of EUVL masks depending on capping layer and absorber stack structures. All layers including Mo/Si multilayers, capping layers (Si or Ru), and absorber (TaN) stacks are deposited on either 6 inch 6025 quartz substrates or thermally oxidized Si wafers using an ion-beam sputter deposition (IBD) system. The observed reflectivities of various stack structures radiated at EUV wavelengths are in good agreements with simulations obtained using Maxwell equations and refractive indexes of each layer. Several patterned masks including Ru capping layers and TaN absorbers have been fabricated and exposed with a small-field micro exposure tool (MET) using EUV radiation at 13.5 nm wavelength. The printing performances depending on TaN absorber stack thicknesses are investigated and the implications on the selection of optimum mask structure are discussed.

6517-52, Session 11

Sub-35-nm logic device template fabrication

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Referring to the International Roadmap of Semiconductors(ITRS), UV Nano Imprint Technology is estimated to be next generation lithography which is responsible for sub-32nm technology. NNFC(National NanoFab Center) have been fabricated the qualified imprint template which is the key to succeed in UV nano imprint technology.

In this paper, we have demonstrated the Proximity Correction Method to fabricate sub-35nm half pitch (line/space, contact) template and Improved Imprinting Technology.

6517-53, Session 12

Molecular ruler nanolithography

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The selective placement and precise tailoring of the thickness of chemically self-assembled multilayers is the basis for molecular ruler nanolithography. These self-assembled multilayers, composed of alternating layers of α-ω mercaptoalkanoic acids and coordinated metal ions, are deposited on photolithographically patterned Au structures forming molecular ruler resists to fabricate tailored, lithographically defined patterns with sub-50 nm separation [1]. The first generation features created by conventional techniques are referred to as parents and the second generation features generated by the molecular ruler process are identified as daughters. The distance between the parent and daughter structures is measured out by the molecular ruler resist, which is employed as an organic sidewall spacer on the parent structure. The thickness of this molecular ruler resist can be precisely controlled by varying the numbers of multilayers and the length of the organic molecule. As a result, the line-edge resolution and roughness of structures created using this process is of the order of the thickness of the self-assembled monolayer (~ nm). In addition, this process uses parallel solution-processing at ambient temperature and pressure and hence is compatible with heavy-volume manufacturing.

The evaluation of our lithographic processes has enabled the fabrication of nanoelectrodes with yields greater than 90% [2,3]. These electrodes are being applied as testpad structures for the interrogation of the electrical properties of nanomaterials. The electrode dimensions have been scaled down to the sub-100 nm regime using e-beam lithography. Previous limitations on the relative height of the initial and secondary structures have been circumvented by the selective etching of the Au thin film. The Cr thin film left behind following this selective removal was used as an etch mask to etch nanometer-scale trenches into SiO2, for the fabrication of nanofluidic channels that are self-aligned to micron-scale features [4]. We continue to push this technology toward mainstream industrial manufacturing and these techniques will be discussed.

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6517-54, Session 12

Scissionable bile acid nanostructures for lithography

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Pixelated photoresists, i.e. resists that compartmentalize photochemistry into discrete imaging elements are an emerging design for improved resolution. A pixelated design seeks to overcome chaotic organization in complex resist formulations through application of small regular or symmetric imaging species, and/or through the application of preorganization of resist components. [1]

Another approach, backbone scission, has also emerged as a powerful method to improve resist performance. [2] In this approach, the parts of the resist structure that have undergone radiation driven chemistry are disconnected from the unaffected material. This enhances contrast and also confers an additional mechanism: structural disruption.

Bile acids have been used recently as building blocks to enable host-guest chemistry [3] and have been incorporated as additives in photoresists [4] and structural elements [5]. They as a class are fairly large (mw ~400) highly functionalized molecules possessing a hydrophobic face, alcohol groups and a carboxylic acid group.

We describe here a scissionable pixelated resist architecture based on bile acids bound by acid-sensitive tertiary ester linkages into dendrimeric arrays. This design seeks to employ structural disintegration and catalyst pre-organization in addition to solubility switching as contrast mechanisms. Preliminary EUV and ebeam studies have shown G0 and G1 materials capable of sub-micron imaging.

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6517-55, Session 12

Stretched polymer nanohairs by nanodrawing

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A simple, yet innovative, method is presented for fabricating high-aspect-ratio polymer nanohairs (aspect ratio \>20) on a solid substrate by sequential application of molding and drawing of a thin polymer film. The polymer film was prepared by spin coating on a rigid or flexible substrate, and the temperature was raised above the polymer's glass transition while in conformal contact with a poly(urethane acrylate) mold having nanocavities. Consequently, capillary forces induced deformation of the polymer melt into the void spaces of the mold and the filled nanostructure was further elongated upon removal of the mold due to tailored adhesive force at the mold/polymer interface. The optimum value of the work of adhesion at the mold/polymer interface ranged from 0.9 to 1.1 times that at the substrate/polymer interface.

6517-56, Session 12

Direct high-speed three-dimensional nanoscale thermal lithography using heated atomic-force microscope cantilevers

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Patterning materials at micrometer and nanometer length scales is a critical and enabling technology in a variety of applications. In particular, nanopatterning of polymer thin films is the basis for the vast majority of current microlithography processes used in integrated circuit manufacturing. Future scaling of such polymer patterning methods will require innovative solutions to overcome the prohibitively high tool and mask costs associated with current optical lithography methods that will prevent their use in many applications. There are opportunities to improve both the direct write lithography methods used for mask manufacturing (e.g. e-beam lithography) and the highly parallel lithography methods used for device manufacturing (e.g. EUVL). A variety of scanning probe-based methods for surface modification and patterning have been recently demonstrated including direct atomic manipulation, thermomechanical deformation, and dip pen nanolithography (DPN). Scanning probe methods are attractive in that they offer direct write capability, high resolution patterning down to potentially molecular scale resolutions, and the ability to perform in-situ metrology while writing. While these AFM based techniques are interesting, there remain several unmet needs. Perhaps most important in these needs is the problem that while sub-100 nm resolution is possible with many of these AFM methods, the writing speeds are generally very slow with typical tip writing speeds in the range 0.1-1 nm / sec. Recently, we have developed and reported a new AFM lithography technique using heated AFM cantilevers in conjunction with polymer thin films. This paper reports on the recent progress in this area where a heated atomic force microscope cantilever is used to achieve nanoscale patterning in polymer films via local thermal decomposition of polycarbonate thin film materials. Specifically, cross-linked polycarbonate thin films are shown to be an excellent writing media for this process. This new method has the advantage that the tip can be heated and cooled on microsecond time scales and thus material can be removed and patterned without need for disengagement of the tip from the polymer surface. This ability to write while the tip is constantly engaged to the surface offers significantly higher writing speeds for discontinuous patterns relative to many other scanning probe techniques such as DPN. 60 μm/sec writing speeds have been achieved for this thermal AFM writing process and results of investigations of the writing speed, writing temperature, resolution parameter space will be discussed. These high writing speeds are several orders of magnitude faster than other probe lithography techniques. For example, Figure 1 shows a line-space pattern made by thermal writing with a heated probe tip at 725 oC using a scanning speed of 6 μm/sec in a 150 nm thick cross-linked polycarbonate film. The figure shows that the polymer is cleanly decomposed by the heated probe tip, and no residue is observed around the written feature. The single line width shown in these images is approximately 200 nm at the top of the features. This resolution is mainly determined by the aspect ratio of the probe tip and the film thickness. With high aspect ratio probe tips and thinner polymer film thicknesses, significantly higher resolutions are possible. Since a polymer is used as the imaging material, tip wear is negligible using this method as compared to many other AFM lithography methods. Unlike the majority of other lithographic methods, this new method also permits the direct fabrication of three dimensional patterns. Figure 2 shows an example of a 3D pattern formed in a polycarbonate film using a single writing scan where the tip scan speed is varied over different regions of the feature to remove different amounts of material. Investigations of this 3D patterning capability will also be discussed. All of the techniques are amenable to being scaled to high throughputs by utilizing large arrays of heated cantilevers (e.g. arrays similar to those already reported for Millipede data storage applications).

6517-57, Session 12

Focused ion-beam nanopatterning for fabrications of III-nitride light emitting diodes

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Photonic device structures often require nanoscale lithography techniques for their device fabrication. The techniques are electron beam lithography and FIB pattering. Focused ion beam etching has been used as a nanolithography tool for the creation of these nanostructures without mask. We obtain nanoscale mesa patterns on InGaN/GaN light emitting diode wafer using focused ion beam and characterized. The InGaN/GaN LED wafer was grown by molecular organic vapor deposition (MOCVD). To reduce the surface damage during FIB patterning, we used a dielectric mask layer and dry etching to eliminate re-deposition of sputtering materials and Ga+ ion implantations during FIB patterning, and finally, removed mask layer with wet etching. A metal thin layer was deposited by an ion beam sputter to avoid charging effects during FIB patterning. We obtain a 2-Dimensional patterning for the fabrication of the high brightness LEDs. This FIB pattering technique can be applied to nanofabrication optoelectronic devices.

6517-58, Session 13

Rigorous model for registration error due to EUV reticle non-flatness and a proposed disposition and compensation technique

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Micro-lithographic imaging systems using wavelengths of 193 nm and above are designed to be telecentric on both sides of the projection optics. Unfortunately, EUV imaging systems will only be telecentric on the wafer side. On the object side, the reticle is illuminated by a chief ray that is not parallel to the optical axis (typically 6 degrees off-axis), resulting in a violation of the telecentricity condition. Out-of-plane-distortion (OPD) that causes points on the reticle to be out of the optimal focal plane will therefore cause magnification and registration errors.

The lack of telecentricity on the object side places a severe requirement on reticle flatness. SEMI P37 (Specification for EUV Lithography Mask Substrates) specifies a typical 50 nm peak-to-valley (PV) criteria on both the front (FS) and backside (BS). This value is 10X tighter than the 0.5-micrometer flatness typically specified for critical 193 nm exposure applications.

The films deposited on the substrate (BS coating, FS multilayer and absorber) further complicate the problem due to stress-induced bow. The resulting blank when measured in a freestanding vertical orientation will have a typical PV flatness exceeding one micrometer, even if the underlying substrate meets the P37 requirement.

The industry, at this point, has not completely agreed on how to address this problem, nor has it demonstrated a full solution. However, some potential strategies are under development.

In this paper, we suggest an explicit strategy based on the analysis of interferograms produced by application-specific metrology. This metrology, preformed before mask patterning would allow either disposition of the blank based on predicted registration performance or feed-forward correction at the mask patterning step that would compensate for the expected mis-registration.

This paper will describe the calculation and algorithms used in fitting and analyzing the interferograms. It will also summarize the results of the proposed technique using interferograms collected in collaborative work between the University of Wisconsin (UW), Intel and Sematech using a prototype metrology apparatus at UW.

6517-59, Session 13

Status and path to a final EUVL reticle protection and handling solution

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In extreme ultraviolet lithography (EUVL), the lack of a suitable material to build conventional pellicles calls for industry standardization on new techniques for reticle protection and handling throughout its lifetime. This includes reticle shipping, robotic handling, in-fab transport, storage, and uses in both atmospheric environments for metrology and vacuum environments for EUV exposure. In this paper, we review the industry's most promising reticle carrier approaches for particle-free protection, including improvements in conventional single carrier designs and new EUVL-specific carrier concepts. The new concepts that will be reviewed include a variety of forms originating from the very basic concept of a removable pellicle. An EUVL removable pellicle can simply be a protective flat face plate that shields the patterned side of the photomask from particulate contamination. Variations of a removable pellicle include adding a protective ring to the face plate that surrounds the four sidewalls or adding a backside cover to form a completely closed environment. The removable pellicle must remain with the reticle all the time, unless separation is absolutely necessary, as during EUV exposure. To minimize the out-gassing impact, removable pellicles are often made of metallic materials, such as aluminum.

We will present our evaluation results from some of the most promising EUVL reticle protection approaches. These results were obtained using the world's most sensitive mask substrate inspection capability (≤ 50nm). In particular, our discussion will focus on the two most critical stages in reticle use: shipping and vacuum pumping and venting. During vacuum pumping and venting, a reticle is exposed to pressure swings from atmospheric to several milli-torrs vacuum, or vice versa. The range of pressure changes used in our experiments is such that it represents the most severe vacuum conditions in an EUVL exposure tool. We will also discuss SEMATECH's progress in developing robotic handling testing capability for the most advanced EUV carrier options to evaluate and demonstrate complete EUVL reticle carrier and handling solutions.

Finally, we will summarize the progress of the SEMI EUVL Reticle Carrier and Load-port Standards Task Force, which SEMATECH has been helping to organize and lead. We will present our assessment of the technical challenges facing EUVL reticle handling technology and the feasibility of a single reticle handling solution for all EUVL reticle making and usage steps. In addition, we will discuss a path to a final EUV reticle protection and handling solution.

6517-60, Session 13

Performance estimation of EUV exposure optics for below 32-nm node in consideration of Mo/Si multilayer

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The EUV lithography is the most promising candidate for the next generation semiconductor exposure technology to fabricate fine patterns of 32nm and below 32nm node in half-pitch, now that ArF immersion technology is expected to cover 45 nm node these days.

EUV optics are composed only of the mirrors, and the number of mirrors varies with the target node according to the permissible aberration. For Example, six-mirror projection optics and eight-mirror projection optics are suitable for 32nm node and below 32nm node, respectively.

Each mirror is given a Mo/Si multilayer coating to raise reflectance of EUV. The reflectance is extremely sensitive to the multilayer thickness, the exposure wavelength, and the ray incidence angle. And the multilayer is designed to give a best performance at exposure wavelength of 13.5nm. Errors of thickness and optical index of the multilayer have more serious effects on the imaging performance as the number of mirrors increases. So, we are studying these effects especially on the eight-mirror projection optics in order to attain the technology of EUV lithography for below 32nm. At the conference, we are going to present the following issues numerically.

1. Image quality in consideration of the spectral width around 13.5 nm.

Not only the light of 13.5nm, the light around 13.5nm (i.e. 13~14nm) can also reach the wafer. The images vary with the wavelength because of the wavelength dispersion of multilayer coating. We simulate the image by overlapping image at each wavelength.

2. Throughput in consideration of the spectral width around 13.5nm.

The throughput used to be estimated roughly based on the etendue of radiation source without consideration of the spectral width, the throughput proved to be influenced by the spectral width sensitively. We estimate the throughput at various spectral widths.

3. Allowance of the multilayer coating errors.

The quality of irradiation at the wafer changes with errors of the multilayer coatings. The decline in intensity of the irradiation causes a decrease in the throughput, and the deformation of the spectrum causes a poor imaging performance because of the change of effective source and pupil function of projection optics. We estimate the allowance of the multilayer coating errors in view of the throughput and the imaging performances.

4. Influence of Out Of Band (OOB) radiation.

The radiation from the source contains OOB radiation such as UV in addition to EUV radiation. Resists have sensitivity to OOB radiation in general. We estimate the degradation of the imaging performances by calculating the quantity and intensity distribution of OOB radiation which reaches the wafer.

6517-61, Session 13

Image formation study of EUV holographic lithography

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Extreme Ultraviolet Lithography (EUVL) is one of the promising candidates for the next generation lithography approach toward the sub-32nm devices. It is based on the use of radiation around 13nm. The major difficulty is caused by the strong absorption of the materials at this wavelength; thus, multi-layer coated reflective optics (and masks) are normally required. Today, only few exposure tools are in existence due to the combined requirements of source, complex reflective mask, and reflective imaging optics. At the CNTech facility, an undulator is used for exposure in the EUV, using among other tools EUV Interferometric Lithography. In a previous work, we reported the first results from a novel holographic lithography technique using EUV radiation - EUV-HL. Computer generated binary holograms (CGH) were fabricated on a 100nm thick SiNH membrane with a 100nm thick Cr absorber layer to reconstruct an arbitrary pattern ("CNTECH" logo) on PMMA photoresist. The experimental setup of a transmissive EUV-HL system is shown in Fig. 1 and the recorded image on PMMA resist is shown in Fig. 2.

A CGH can be visualized as the coherent superposition of a set of phase zone plates, each corresponding to a single pixel in the object. The information required for image formation is spread out over the entire hologram; hence the image quality is less prone to mask defects. A CGH mask can be considered as a non-periodic diffraction grating. The setup of the EUV-HL system yields an optic-less system with low numerical aperture (N.A.) and has a relatively large depth of field (DOF). As an example, fresnel zone plate (FZP) of 50nm resolution, focal length 1.5mm at lambda=13nm will require a bandwidth better than 40nm to deliver the nominal resolution, over a DOF of ±260nm.

In this study, we will address in detail the questions related to the development of an accurate EUV-HL image formation system from a lithography point of view. We will show what are the optimal exposure conditions for exposing a standard resolution test pattern (as shown in Fig. 3) in the EUV. In addition, the optimization of CGH will also be performed in order to improve the image quality by adopting algorithms similar to optical proximity correction (OPC), i.e., that modify the (virtual) object to achieve the desired targeted pattern. Finally, we will consider the effect of electron-beam proximity corrections on the CGH patterning and compare with experimental results obtained at the UW EUV exposure facility.

6517-62, Session 13

EUVL mask development status at Samsung

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Extreme ultraviolet lithography (EUVL) is one of the leading candidates for the next generation lithography for device manufacturing with feature size beyond 32nm. Samsung have established the EUV mask pilot line in order to meet these requirement specifications since 2004. We developed the etching process for maximum selectivity between absorber, buffer and capping layer on the 2 kinds of mask blank type. The whole mask patterning process was executed on an advanced tool set comprising of EBM5000 variable shaped e-beam writer, developer HamaTech ASP5000, cleaning HamaTech Mask Track, and two chamber CP6000i mask etcher.

This paper will summarize the fabrication process for EUV mask and the results of the mask patterning process, absorber dry etch optimization, reflectance of multilayer, material film stress, EUV mask defect inspection, absorber defect repair, cleaning performance, and defect printability using the Micro Exposure Tool (MET).

6517-63, Session 14

Thermal management design and verification of collector optics into high-power EUV source systems

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The productivity demands of the EUV lithography beta exposure systems require considerable source power levels in order to deliver 15 W in-band power at the intermediate focus (IF). Considering the transmission budget of the debris mitigation device (DMT) and of the grazing incidence collector (GIC), this corresponds to about 200 W in-band power in 2π sr, which entails about 10-15 kW total radiated power in 2π sr. This amount of radiated power, bound to increase considerably for high volume manufacturing exposure systems, requires effective, stable, and reliable thermal management design for the entire source-DMT-collector subsystem.

In this paper, the thermal management for a multi-shell grazing incidence collector design will be reviewed together with the characteristics of the source and the debris mitigation device. The power budget assumptions will be explained and quantified.

In order to effectively remove the absorbed power from the collector's optics, several cooling circuits are integrated into the backside of the EUV mirrors. The design guidelines are to provide optical performance stability through proper optimization of geometrical layout, flow and pressure drop parameters, and interference-free design with respect to the optical path. The effectiveness of the cooling layout is ultimately validated by means of thermo-structural analysis based on finite element models (FEM), resulting in estimation of the opto-mechanical deformation performance data. This is then used to simulate the far field image stability by means of ray tracing calculation techniques. Examples of far field image RMS distortions under full power will be reviewed.

A closed-loop design methodology is implemented where the field tests of the collectors installed and operated in the source test stands under nominal EUV radiation will provide the input data for the verification phase. The thermal response of the collector-DMT subsystem is mapped via several thermocouples, at transient and steady state. This massive amount of data is effectively compared to the theoretical data based on our FEM predictions. The validation of the power budget is the primary objective of the test campaign, and is achieved by means of few fundamental measurements of cooling water's flow rate and temperature, along with power measurements, under steady state conditions. Once the power budget estimation is verified, the validation of the FEM model, based on comparisons between the theoretical and actual thermal response of the collector system, follows.

The opto-thermal performance of the EUV collection system is also tested, namely the collector transmission, far field image stability, and the DMT-collector transmission under increasing power loads.

Supporting test data, obtained independently from transmission measurement carried out in a collector reflectometer set up, will also be presented.

The presented data will demonstrate that the thermal management capability and techniques developed by Media Lario Technologies are effective and adequate for 15 W intermediate focus EUV power and are scalable to HVM application.

6517-64, Session 14

Low-cost EUV collector development: design, process, and fabrication

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Cost of ownership (COO) is an area of concern that may limit the adoption and usage of Extreme Ultraviolet Lithography (EUVL). One of the key optical components that contribute to the COO budget is the collector. The collectors being fabricated today are based on existing x-ray optic design and fabrication processes. The main contributors to collector COO are fabrication cost and lifetime. We present experimental data and rigorous optical modeling to demonstrate a roadmap for enhanced efficiency and an order of magnitude reduction in collector COO.

Current state of the art collectors are based on a Wolter type-1 design and have been adapted from x-ray telescopes. It uses a long format that is suitable for imaging distant light sources such as stars. As applied to industrial equipment and very bright nearby sources, however, a Wolter collector tends to be expensive and requires significant debris shielding and integrated cooling solutions due to the source proximity and length of the collector shells.

The design presented here is based on an elliptical collector that has been optimized for collection efficiency however this test vehicle is being used to demonstrate a low cost fabrication process that can encompass other collector designs as well. In this work a fifteen shell collector design is described. The number of shells and their design may be modified to increase the collection efficiency and to accommodate different EUV sources.

The fabrication process used here starts with a glass mandrel, which is elliptical on the inside. A seed layer is coated on the inside of the glass mandrel, which is then followed by electroplating nickel. The inside/exposed surface of the electroformed nickel is then polished to meet the figure and finish requirements for the particular shell and finally coated with Ru or a multilayer film depending on the angle of incidence of EUV light. Finally the collector shell is released from the inside surface of the mandrel.

There are several potential cost and fabrication process advantages to this process. There is flexibility in the choice of material for producing the mandrel - this allows for optimizing the cost of fabrication of the mandrel. Moreover, since the final surface and figure of the collector optic can be modified, after electroforming the optic, the mandrel, in principle does not have a limited lifetime. Finally, the mandrel provides mechanical support to the electroformed optic throughout the fabrication process, thereby reducing deformation of the optic during polishing and coating.

The optical design, optimization of collection efficiency, fabrication and characterization results is discussed in this work.

6517-65, Session 14

Advanced debris mitigation schemes and cleaning methods: collector optics lifetime extension

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Extreme ultraviolet (EUV) light sources with efficient emission at 13.5 nm are needed for next-generation lithography. A critical consideration in the development of such a source is the lifetime of collector optics. The optics are exposed to a large flux of energetic particles coming from the expansion of the pulsed-plasma, potentially leading to mirror damage due to erosion, layer mixing, and ion implantation. Frequent replacement of the mirror system detracts from the economic feasibility of EUV lithography and must be avoided. The Xtreme Commercial EUV Emission Device (XCEED) at the University of Illinois has been designed to test the performance of various EUV mirror materials during operation of a commercial EUV source, and to investigate the mechanisms behind observed losses in reflectivity over a varying number of pulses. Research efforts at the University are focused on several critical challenges facing the source-optic system. This paper will present results on a series of advanced debris mitigation schemes tested at UIUC. Pulsed foil trap experiment and mixed fuel based debris mitigation will also be presented. This paper will highlight the role of ion acceleration processes in reducing the ion energy of heavier masses. Debris spectra measurements using the calibrated ion (spherical sector electrostatic energy analyzer, ESA) and neutral energy analyzers (0-12 keV dynamic range) will be presented on the commercial XTS source operating with Sn, highlighting comparisons with Xe data showing 4-8keV energy peaks based on buffer gas fill. Ion debris is also measured from a Sn-LPP EUV source and the comparison between Sn DPP and Sn LPP ion energy spectra will be shown. RF plasma is introduced between the pinch region and debris mitigation tool. Interesting results are obtained, where the presence of RF plasma helps to sputter off the flakes deposited on nearby surface around electrodes in Z-pinch plasma - improving downstream optics lifetime. New Sn etching chemistries are investigated and the results are presented in detail. Particle removal using plasma assisted cleaning by electrostatics is investigated and encouraging results are obtained. The overall picture points towards a viable Sn DPP or LPP source-optic system for HVM conditions

6517-66, Session 14

Energetic and thermal Sn interactions and their effect on EUVL source collector mirror lifetime at high temperatures

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Exposure of collector mirrors facing the hot, dense pinch plasma in plasma-based EUV light sources remains one of the highest critical issues of source component lifetime and commercial feasibility of EUV lithography technology. Studies at Argonne have focused on understanding the underlying mechanisms that hinder collector mirror performance under Sn exposure and developing methods to mitigate them. Both Sn ion irradiation and thermal evaporation exposes candidate mirrors tested (i.e., Ru, Rh and Pd) in the experimental facility known as IMPACT (Interaction of Materials with charged Particles and Components Testing). Studies have led to an understanding of how Sn energetic ions compared to Sn thermal atoms affect three main surface properties of the collector mirror: 1) surface morphology, 2) surface structure and 3) surface chemical state. All these properties are crucial in understanding how to operate devices under HVM conditions using Sn as the main EUV radiator. This is primarily due to the correlation of how variation in these properties affects the reflectivity of photons in the EUV spectral range of interest (in-band 13.5-nm).

In this paper we primarily study Sn thermal and energetic particle exposure on collector mirrors (Ru, Pd and Rh) as a function of temperature and its effect on EUV reflectivity. This is possible by the new state-of-the-art in-situ EUV reflectometry system that measures real time relative EUV reflectivity at 15-degree incidence and 13.5-nm during Sn exposure. Sn energetic ions at 1-keV and fluxes of about 10^13 cm^-2s^-1 are used in conjunction with a moderate flux Sn evaporative source delivering Sn fluences ranging from 10^15-10^17 cm^-2. The temperature of the mirror sample is locally varied between 25 and 300 C with the chemical state of the surface simultaneously monitored using X-ray photoelectron spectroscopy, and low-energy ion scattering spectroscopy. In addition, the partial sputtering efficiency due to incoming Sn energetic ions on candidate mirror materials is also monitored in-situ and in real time using an advanced rotating QCM-DCU system (quartz crystal microbalance - dual crystal unit). The rotating QCM-DCU is sensitive to sputter rates of 0.005 nm/sec.

Complementing in-situ diagnosis, we utilize ex-situ diagnosis with: X-ray reflectivity, at-wavelength EUV reflectivity using the newly upgraded NIST-SURF facility, XRF, HSEM, and AFM. Results demonstrate the balance between energetic and thermal Sn has on the total Sn surface fraction during exposure and its effect on the structural and reflective properties of the mirror surface. Experiments and modeling will be presented as well as implications to high-volume manufacturing operation levels with Sn plasma EUV light sources.

6517-67, Session 14

Application of the Energetiq EQ-10 electrodeless Z-Pinch(tm) EUV light source in outgassing and exposure of EUV photoresist

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Formulating high sensitivity and high resolution EUV Resists is a critical issue gating the adoption of EUV lithography. The ability of resist manufacturers to quickly screen outgassing rates and sensitivity of EUV resists will facilitate faster formulation of a production-ready EUV photoresist. The high power and low cost per watt of the Energetiq EQ-10 light source enables relatively simple designs without complex optics to deliver relevant data efficiently. Because the source operates without electrodes1, a significant source of contamination is removed, further simplifying the design of exposure systems.

Data will be presented from two prototype exposure systems. The first, in operation at Osaka University, Japan2 has been used for in-band

flood exposure experiments to test resist sensitivity and develop photochemical modeling capability. The second, in operation at SUNY-Albany3, integrates exposure/sensitivity with outgassing measurements (GC/MS and RGA) and also allows direct tests of mirror contamination, at power densities near those required for Beta exposure tools.

Features of both experiments have been integrated into a commercial device. Details of this tool — the Litho Tech Japan EUVES-7000 system for resist outgassing and exposure — will be presented at this meeting4.

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6517-68, Session 14

Optimization of EUV laser and discharge devices for high-volume manufacturing

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A key challenge for Laser and Discharge Produced Plasma devices is achieving sufficient brightness with minimum debris generation to support the throughput requirements of High-Volume Manufacturing (HVM) lithography exposure tools with long lifetime. Source performance, Debris mitigation, and reflector system are critical to efficient EUV collection and component lifetime. Integrated models are developed to simulate EUV emission at high power, debris generation and transport in EUV devices, interaction with different mitigation systems, and escaping debris/mirror interaction. The models being developed includes, for example, optimization of source parameters, combination magnetic fields and gas jet parameters to significantly reduce the debris, and mirror surface conditions to enhance the reflectivity of EUV. Source optimization includes multiple laser interaction with single target for laser devices and electrode designs for discharge sources. Debris-mirror interaction modeling is benchmarked with recent experimental results of IMPACT facility. Initial simulations show that for HVM devices a combination of source optimization, innovative debris mitigation system, and understanding debris/mirror interaction is required to achieve the lifetime needed.

6517-69, Poster Session

Detection signal analysis of actinic inspection of EUV mask blanks using dark-field imaging

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Extreme ultraviolet lithography (EUVL) is a leading candidate for a device manufacturing with a half pitch of 32 nm and beyond, with the possibility of adoption in half pitch 45 nm node still remaining if economically viable. The manufacturing of defect-free mask blanks is, however, a significant challenge for the implementation of EUVL. In general, defects in a multilayer-coated mask blank are classified into two types: amplitude defects and phase defects. In EUVL mask blank, phase defects are a severe problem. As only a 2-nm-high multilayer defect at the surface of a multilayer which is a phase defect induces a significant phase change of reflected EUV light, the defect produces a dark spot image at a clear field and gives a significant printed image change. While the phase defect is a serious defect, visible or UV inspection is sensitive only to the top surface of the multilayer and it is not easy to detect such shallow defect.

Selete (Semiconductor Leading Edge Technologies, Inc.) has been working on the development of a full field actinic (at wavelength) inspection tool using dark-field imaging to inspect the phase defects of a multilayer-coated mask blank for EUVL. The concept of the method and the tool design has been transferred from MIRAI Project Phase 2 [1,2]. In the inspection tool, defects are detected as brighter spots than surrounding area because of dark-field imaging and are identified simply applying a certain level of threshold. As the brighter spot gives the higher sensitivity, it is important to study the through focus characteristics giving maximum intensity of the spot. The experimental through focus imaging data using MIRAI proof-of concept (POC) tool with a 26x Schwarzschild optics of numerical aperture (NA) of 0.2 and a back-illuminated charge-coupled-device (BI-CCD) of 13 μm pixel size shows that the best focus in which a defect signal is maximized is different between pattern types, especially hole (pit) and dot (bump), and a common focus level through various small patterns can not be secured [3]. The best focus shift between hole and dot programmed defect patterns with around 140 nm width is 6 μm whereas the depth of focus (DOF) of the defect signal defined as FWHM (Full Width Half Maximum) is only 6 μm. (Fig.1) The defect depth and height on the multilayer surface are 6.0 nm and 5.7 nm, respectively.

The through focus characteristics between various patterns are investigated by electromagnetic (EM) simulation and the results are compared with the experiments in this paper. This paper also describes the recent experimental data by the 26x Schwarzschild optics. A 1.2-nm-high, 55-67-nm-wide (FWHM) programmed dot (bump) defect is detected.

This work was supported by NEDO.

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6517-70, Poster Session

Development of EUV mask handling technology at Selete

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We, MIRAI-Selete, started a new EUV mask program in April, 2006. Development of EUV mask handling technology is one of the key areas of the program. We plan to evaluate EUV mask carriers using Lasertec M3350, a particle inspection tool with the defect sensitivity less than 50nm PSL, and Mask Protection Engineering Tool (named "MPE Tool"). M3350 is a newly developed tool based on a conventional M1350 for EUV blanks inspection. Since our M3350 has a blank flipping mechanism in it, we can inspect the front and the back surface of the blank automatically. We plan to use the M3350 for evaluating particle adders during mask shipping, storage and handling.

MPE Tool is a special tool exclusively developed for demonstration of pellicleless mask handling. It can handle masks within protective

enclosures, which Canon and Nikon have been jointly proposing, and also, can be modified to handle other type of carrier as the need arises. Figure 1 shows a schematic drawing of our MPE Tool. The MPE Tool has a robot in the air area, which transfers a naked mask or the mask-protective enclosure from RSP200 to the loadlock chamber. And a robot in vacuum area transfers it from the loadklock chamber onto the electrostatic chuck. We focus on not only particle adders on the front surface of the mask but also the back surface, because particles between the mask and the chuck affect OPD and IPD of the mask.

* This work is supported by NEDO.

6517-71, Poster Session

Impact of interface treatment with assisted ion beam on Mo-Si multilayer formation for EUVL mask blanks

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Defect-free masks are critical to the use of extreme-ultraviolet lithography (EUVL) for the high-volume manufacture of LSIs. To make low-defect-density mask blanks with Mo-Si multilayers, we have developed a sputter deposition system that can employ either ion-beam sputtering (IBS) or magnetron sputtering (MS). [1] Another essential characteristic of a Mo-Si multilayer mirror for mask blanks is a high reflectivity in the wavelength range of 12-15 nm. To determine the factors important for high reflectivity, we analyzed Mo-Si multilayers grown by IBS and MS using transmission electron microscopy (TEM), Rutherford back-scattering (RBS) measurements, and reflectivity calculations that took the interface layer between Mo and Si into account. The results showed that the interface layer (0.5-1.5 nm thick) arising from the intermixing of Mo and Si atoms during coating degrades mirror reflectivity. A comparison of Mo-Si multilayers formed by IBS and MS showed that the interface layer was 30-50% thinner for MS than for IBS. [2]

To reduce the thickness of the interface layer, we devised a new process that involves treating the surface of the Si layers with an assisted ion beam (AIB) of Ar or oxygen in combination with sputter deposition. Atomic force microscopy (AFM) measurements of the surface of two Mo-Si bilayers showed a 20% improvement in root-mean-square (RMS) roughness for Ar ion-beam treatment and no degradation for oxygen ion-beam treatment. X-ray diffraction (XRD) and TEM measurements indicated substantial differences in the Mo-Si interface after the two types of AIB treatment. Reflectivity calculations for Mo-Si multilayers were carried out, considering the effects of the competitive processes of impurity incorporation and reduction on the thickness of interface layers.

At the conference, a new coating process that involves surface treatment with an AIB will be described; and the results of XRD, TEM, and RBS analyses that show how effective our new process is will be presented.

Acknowledgement: This work was supported by the New Energy and Industrial Technology Development Organization (NEDO), Japan.

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6517-72, Poster Session

Spectrally investigated optimization for the high-optical transmission of the C-shaped nano-apertures

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The limitation of empirical wavelengths of lasers useful for optical microlithography due to the maturity of current laser technology makes the spectrally-investigated optimization very important for the design of C-shaped nano apertures, to achieve high optical transmission as well as tight focusing because the resonance behavior of apertures depends on the incident light's wavelength. The optical transmission and divergence through the nano aperture are determined by the effects of the propagation mode and evanescent mode, because its resonance conditions are given by its geometric parameters and the localized surface plasmon effect. Thus, the decaying behaviors of propagating light through nano apertures depend on their geometries and material properties as well as the wavelength of incident light.

In this report, finite difference time domain (FDTD) method is used to simulate the electromagnetic field intensities at both near field and far field in order to optimize the C-shaped nano apertures for high transmission with tight focusing. The radiated far field intensity from the aperture is strongly coupled with the propagation mode of the near field intensity. The high transmission properties of the C-shaped nano aperture show the significant enhancement of propagation mode compared to square apertures.

We fabricate the C-shaped nano apertures with FIB milling and measure the far field transmissions, which is advantageous because of its easier feasibility compared to near field measurement. Using the far field transmission measurement, we have the indication of the surface plasmon effect of C-shaped nano apertures and approve the spectral optimization of the apertures.

6517-73, Poster Session

Design of metal slits for higher harmonic fringe patterns generated with surface plasmon interference lithography

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In this paper, based on numerical study using finite difference time domain method, we design metal slits for higher harmonic fringe patterns generated with surface plasmon interference lithography. The slits are designed to generate higher harmonic fringe patterns having high intensity output, high contrast and good uniformity in sub-100 nm scale. Using permittivity of the aluminum metal film derived from Lorentz-Drude dispersion relation, we calculate the output characteristics of the fringe patterns obtained by the slit. Preliminary numerical simulations show that the peak of output intensity and the contrast depend on the thickness of a spacer layer that is placed between the slit and a photoresist layer. The peak intensity is changed periodically as the metal film thickness increases with an oscillation period of quarter of the incident light wavelength. It is found the peak of output intensity reaches its first maximum when the spacer layer thickness is 30 nm. Also the peak of output intensity is changed periodically as the slit period increases with an oscillation period of the surface plasmon wavelength. The slit width is an important parameter to affect the pattern uniformity. When the slit width is larger than a half of the surface plasmon wavelength, the pattern uniformity becomes poor. The simulation results obtained by changing the spacer thickness, the film thickness, the slit width and the period of the slit are expected to provide helpful information for the metallic plasmonic slit design. A best-fitted slit dimensions for 2nd harmonic fringe pattern are the slit period of 220 nm, slit width of 60 nm and metal film thickness of 110 nm thick. We fabricate several types of slits on aluminum film according to the calculated designs with a focused ion beam (FIB) facility. Lithography experiments using i-line Hg lamp are performed to record the near-field fringe patterns using aluminum slits and SU-8 negative photoresist.

6517-74, Poster Session

The effect of localized mask density variations on image quality in EUV lithography

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The impact of Stray Light (also sometimes called 'scattered light' or 'flare') in lithographic exposure tools is considered as one of the critical issues in optical lithography. Its effect on the EUV lithography is more significant than that on the optical lithography, because it is in proportion to 1/ * 2 as the exposure wavelength decreases down to 13.5nm. It is getting more important and difficult to reduce the level of stray light to less than 10%, which is required for the high volume manufacturing. Stray light is mainly generated by rough mirror surfaces and other reflection surfaces including mask, which are used in illumination optics and projection system. It has more impacts on

imaging performance such as reduced overall process window including exposure latitude, depth of focus, contrast, and pattern fidelity. Therefore it is important to understand the behaviour of stray light. In general, there are several methods to characterize and quantify the properties of stray light : traditional disappearing pad test, resist threshold approximation, and complex calculation by measuring roughness and wavefront errors of mirrors. However, as a result of charaterizing stray light using such kinds of methods, it is need to be applied for generation of correction model. Several techniques such as dummy pattern implementation and selective biasing are already proposed in order to reduce the effects of stray light.

EUV mask used in memory and logic devices has various kinds of patterns with localized density variations, which are determined by patterned multilayer area. Therfore, EUV mask can also be considered as one of the scattering sources of stray light. Features surrounded by different pattern densities in the mask can be affected by reflected and scattered light from that area. Image quality of features which are adjacent to high density area is degraded by stray light and its influences decrease as becoming more distant from the area. The stray light results in not only resist top loss but also process window reduction due to aerial image contrast degradation. The Most efficient way to decrease influences of stray light can be a combination of selective biasing and dummy implementation. The purpose of dummy implementation is to maintain background density as uniform as possible. Then, to apply selective biasing method after dummy implementation becomes the best method to correct stray light induced linewidth variation.

In this paper, the range which can affect image quality from high density area is investigated. The effect of EUV mask density variations on image quality is also studied in terms of process window, such as LER, depth of focus, resolution, etc., while mask density surrounding features is varied from dark field to bright field with various dummy patterns. As a result, allowable mask background density, which does not affect image quality of surrounding features and decreases effects of stray light, is suggested.

6517-75, Poster Session

Corning ULE(r) glass can meet P-37 specifications

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Corning ULE(r) glass is a binary SiO2 + TiO2 composition formed directly using a flame hydrolysis process. ULE possesses a very low thermal expansion range that can also be accurately adjusted for various applications including EUV photolithography. It is also necessary that the material is capable of meeting stringent flatness and roughness specifications if ULE is to be used for mask blanks and optics applications. For ULE, small compositional striations have been shown to affect surface quality by inducing a mid-spatial frequency (MSF) defect during polishing. Therefore, the main challenge has been to reduce MSF roughness to an acceptably low level by diminishing compositional striations present in the glass.

Recently, a combination of predictive modeling and experimentation have resulted in a process that reduces striae to the levels needed for EUV masks and optics. These models have enhanced the fundamental understanding of the glass forming process, leading to process adjustments in both oscillation patterns and heat treatment producing glass with improved striae characteristics.

ULE masks with reduced striae have been polished to MSF peak-to-valley levels of less than 8 mm, which is within 4 nm of the best surfaces for 193 nm fused silica masks. This sub-8 nm topography accounts for less than 20% of the total 50 nm flatness error budget allowable for EUVL masks. These results indicate that Corning's ULE product can meet the P-37 surface finishing specifications, and combined with CTE performance is positioned as the material of choice for EUV mask blanks.

6517-76, Poster Session

Evaluation and selection of EUVL-grade TiO2-SiO2 ultra-low-expansion glasses using the line-focus-beam ultrasonic material characterization system

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Ultra-low-expansion glasses, having a coefficient of thermal expansion (CTE) within ±5 ppb/K at the desired temperature (for example, 22±3°C), are required as the basic substrate materials suitable for photomask blanks or optical mirrors in extreme ultra-violet lithography (EUVL) systems operating in reflective optics. TiO<sub\>2</sub\>-doped SiO<sub\>2</sub\> (TiO<sub\>2</sub\>-SiO<sub\>2</sub\>) glass is one of the candidates. Its ultra-low CTE is achieved by controlling the TiO<sub\>2</sub\> concentration. In order to develop EUVL-grade ultra-low expansion glasses, it is of fundamental importance to evaluate CTE characteristics with an extremely high accuracy, and to feed back measurement results to improvement of glass production process conditions. Much effort has been paid for improvement of conventional CTE evaluation methods, achieving higher measurement resolutions of ±2 ppb/K for ±2σ (σ: standard deviation) for a direct CTE measurement using a laser interferometric dilatometer and ±0.04 ppb/K for an indirect CTE measurement of the refractive indices by the optical method. However, these methods can only measure averaged characteristics along the thickness direction of TiO<sub\>2</sub\>-SiO<sub\>2</sub\> glass substrates, involving periodic striae associated with their fabrication process conditions, so they cannot provide proper information of CTE on the specimen surface needed for the EUVL systems. <br\>

We proposed a new indirect CTE evaluation method for ultra-low expansion glasses using the line-focus-beam ultrasonic material characterization (LFB-UMC) system. Evaluation is made by measuring the phase velocities of leaky surface acoustic waves (LSAWs), excited and propagated on the water-loaded specimen surface. The great advantages of this technology include nondestructive and noncontact two-dimensional analysis of the characteristics of the specimen surface, and its extremely high sensitivity to CTE evaluation. We have developed methods of evaluating the striae configuration and parameters, standard specimens for the system calibration, and interrelationships among LSAW velocities, TiO<sub\>2</sub\> concentrations, and CTE characteristics. We also obtained the CTE resolution of ±0.3 ppb/K for ±2σ at 75 MHz.<br\>

In this paper, we established evaluation procedures for a practical size of photomasks and optical mirrors used as reflective optics in EUVL systems, based on our previous investigations. Several specimens were prepared with their surfaces parallel to the striae plane from commercial TiO<sub\>2</sub\>-SiO<sub\>2</sub\> ultra-low-expansion glass ingots (C-7972, Corning Inc., 1500 mm<sup\>φ</sup\> × 150 mm<sup\>t</sup\>) for demonstration. Homogeneities/inhomogeneities of specimens were evaluated at 225 MHz, observing LSAW velocity variations caused by striae. For an example, a maximum velocity distribution of 6.66 m/s with an averaged velocity of 3306.88 m/s was detected for a specimen (229 mm × 149 mm × 7 mm<sup\>t</sup\>). This velocity distribution corresponds to distributions of 0.40 wt% in TiO<sub\>2</sub\> concentration and 29.3 ppb/K in CTE. <br\>

Our ultrasonic method should be standardized as a new evaluation method not only for the developments of the EUVL-grade glasses and the evaluation of the production processes, but also for the quality control and selection of the production lots.

6517-77, Poster Session

Defect mitigation and reduction in EUVL mask blanks

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Fabrication of nearly defect-free mask blanks is one of the most significant challenges facing the commercialization extreme ultraviolet lithography (EUVL). Despite significant advances in our ability to clean

substrates, the incoming substrate contributes more defects than the multilayer coating process to the total number of defects on our lowest defect density mask blanks. This is because cleaning processes are ineffective against substrate pits, which dominate the substrate defect distribution. Fortunately defect mitigation methods have been developed that use a coat-and-etch process to smooth substrate pit and particle defects. We have designed and installed a process module specifically for smoothing substrate pits and particles. This process module has several new features, such as the ability to isolate the etch source during the deposition steps, and should enable planarization to be done more cleanly than what has been done before. Currently the greatest challenge for us is to demonstrate that this smoothing process can be rendered clean enough for manufacturing. We shall present results on the particles added during planarization and the composition of these particles, which is critical to identifying their origin and eliminating them.

In addition, we shall highlight recent progress in our defect reduction effort, which is primarily focused on eliminating defects that might occur during multilayer coating. We shall show the first-ever results for mask blank defects detected down to 45 nm (PSL equivalent). This defect reduction work is being performed in a separate process module that is adjacent to the process module used for defect mitigation.

6517-78, Poster Session

Low-viscosity and fast-curing polymer system for UV-based nanoimprint lithography and its processing

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One of the key major elements for the successful integration of nanoimprint lithography into industrial production processes is the availability of high-performance resist materials. In hot embossing lithography standard materials like PMMA, well-known from E-beam lithography were used, whereas in UV-based nanoimprint lithography (UV-NIL) [1] no off-the-shelf or commercial resist materials are available, so that new photocurable materials had to be developed. While a lot of publications report about various technical aspects, only few data were presented dealing with specific UV curable polymer systems for UV NIL and related material issues [2].

In this contribution we present a new low-viscosity and fast curing UV-NIL resist, which is applied by spin-coating and is designed for wafer-scale imprinting. The recipe of the UV-NIL resist is the result of a systematic investigation of numerous UV curable raw materials. The main criteria were:

• Base material properties: viscosity, wetting and film thickness uniformity had been tuned for liquid resist processing.

• Fast curing during UV-imprinting: suitable components were selected on the basis of PhotoDSC measurements.

• Cured film properties: mould release (low detachment forces) and dry etching behaviour were important criteria of the cured polymer and its potential fields of application.

The investigations resulted in the high-performance polymer system mr-UVCur A (Table), which shows fast curing (few seconds), has high plasma etch resistance and is spin-coated in the film thickness range of 150 - 450 nm. Film thicknesses in the sub 100 nm range can be achieved by diluting the resist with suitable solvents (Figure 4). Due to the low viscosity mr UVCur A exhibits very fast filling of the mould patterns, as we show in the process example (Figure 2). The resist material mr UVCur A was fully characterised concerning its UV-imprinting behaviour including investigations on (a) imprinting with hard and soft moulds, (b) UV curing dose, (c) resolution and demoulding, (d) plasma etching and selectivities to several substrates (Si, SiO2, Ti), and (e) pattern transfer processes. Sub 30 nm resolution, which is only limited by the pattern size of the mould, is demonstrated and gives evidence for the capability of fabricating high resolution patterns with the presented resist material.

This work is supported by the Bundesministerium für Bildung und Forschung (BMBF), contract number IWO50336.

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6517-79, Poster Session

Pattern transfer of multilevel interconnect structures generated by step and flash imprint lithography

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Modern integrated circuits may have up to ten levels of back end wiring to connect the silicon level devices to the package level electrical contacts. The dual damascene process for fabrication of these copper interconnects requires many difficult steps for each of the wiring levels. Each dual layer requires two demanding lithography steps as well as a host of film depositions and etch processes. Both the difficulty and number of process steps can be significantly reduced through a multilevel imprint scheme.

Step and flash imprint lithography (SFIL) is a nanomolding process, which utilizes a patterned quartz template as a master mold. The template is brought into contact with a liquid monomer, which is then polymerized through UV curing to produce a solid replica of the template pattern. Various etch processes are used to transfer the pattern into the underlying layers. Multi-level SFIL was reported as a novel approach to fabricating dual damascene copper interconnects. Fabrication and imprint processing of two-level SFIL templates and subsequent development of dual damascene electrical test structures have been demonstrated in imprint resist materials.

The fabrication of real devices requires two-level patterns to be transferred from imprint resist material into an underlying dielectric film. Reactive ion etching (RIE) is a standard process for pattern transfer of a single pattern level. On the other hand, using RIE for simultaneous transfer of two-level patterns requires special considerations. Etch selectivity strongly effects the transferred aspect ratio of the two layers, therefore the type of imprint resist material and etch recipe parameters must be optimized to obtain a desirable pattern transfer.

This paper discusses the feasibility of dual damascene pattern transfer into Applied Material's first generation low-k material, Black DiamondTM. Siloxane-based acrylates and sol-gel materials were investigated as imprint resist materials. The relative etch rates of different imprint resist formulations and Black DiamondTM were measured to determine an ideal material. The faceting of the multi-level structures is documented at varying feature dimensions. A demonstration of the dielectric transfer etch was performed and evaluated. Progress on integration of this process into a copper CMP flow at ATDF, Austin, TX will be reported.

6517-80, Poster Session

Photopatternable low-K dielectrics for imprinting lithography

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The miniaturization of integrated circuit (IC) feature sizes is the driven force for low k materials, which are required to decrease signal delay and inductive cross-talk between the interconnect lines. There are generally eight or more metal wiring levels stacked over the transistor gates in advanced IC devices. These wiring levels are imbedded in the low k dielectric material. More than 100 unit process steps are required to fabricate these complex "back end of the line" BEOL structures.

Recently, Step and Flash Imprint Lithography has shown promise as a method for greatly reducing the number of process steps required to produce the BEOl structures. The SFIL strategy is to fabricate both the

wire and the via (connector) for each wiring level in a single step. The accomplishment of this requires new, specialized, imprintable dielectric materials. Besides the low dielectric constant, these materials must (a) have high thermal stability; (b) be photopatternable; (c) have low viscosity and low vapor pressure before patterning; (d) display high mechanical properties after solidification; (e) demonstrate excellent adhesion to the barrier layer, the dielectric and to metal.

This work describes the synthesis and characterization of new functionalized POSS and Si-14 dielectrics designed for the SFIL BEOL application. The processing performance of these materials in integrated circuit fabrication will be also described.

6517-81, Poster Session

Nanoimprinting with SU-8 epoxy resists

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One of the growing needs for nanoimprint lithography is to have improved thermal and etch resistant materials with rapid throughput or short cycle times. Thermoplastic materials, while widely used require both heating and cooling process steps that dramatically add to the total process times. Additionally, lower process temperatures would be beneficial in that they reduce the effect of any differences in the coefficient of thermal expansion between polymer and substrate. One group of materials that a number of groups have been investigating are chemically amplified epoxy resists such as SU-8 photoresists. SU-8 is widely known for its excellent thermal, chemical and etch resistance as well as its wide process latitude. These products permit imprinting around 100ºC, short imprint times and short cure cycles since only a fraction of the curing needs to be completed before the mold can be removed. Newly introduced “improved” SU-8 products exhibit lower Tg’s and improved flow properties at temperatures below 100ºC.

This paper reports on the evaluation of XP SU-8 4000N for potential application in nanoimprint applications using hot UV imprint lithography. The use of this material is advantageous in that it can be imprinted, exposed and sufficiently cured at the same temperature without any temperature cycling leading to very short cycle times. After removal from the imprint mold the imprinted image can be further cured off-line to desired levels by subsequent heating without any loss of pattern fidelity.

Uncured XP SU-8 4000N has a Tg of approximately 10ºC, yet its films are sufficiently robust to be handled at temperatures from 60 to 100ºC. This resist exhibits excellent flow properties in this range, which is also the temperature range needed to post exposure bake the exposed areas and lock in the imprinted patterns. Thus, a wafer can be spin coated to provide films of less than 100nm thickness to more than 500 nm thick and subsequently baked to remove the residual coating solvent. The coated wafer is then introduced to the imprint tool and placed on a heated chuck for a few seconds, and then the imprint mold is applied. While in contact with the mold on the heated chuck, the resist is exposed through the mold then held in contact for up to a few minutes until sufficiently cured. The wafer can then be immediately removed from the imprint tool and stored until further cured in an off-line oven or on a hot plate.

We will present the results of a statistical experimental design examination of the hot plate temperature (imprint temperature), the exposure dose and the post exposure heating time. The goal of the study is to determine the optimal hot plate temperature, exposure dose and heating time. The optimal temperature is a balance between resist flow and cure rate which must also be balanced by the thermal expansion difference of the materials used. Higher temperatures give better flow and faster cure times but also lead to more thermal stress imparted into the cured film.

6517-82, Poster Session

MR-NIL 6000: new epoxy-based curing resist for efficient processing in combined thermal and UV nanoimprint lithography

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Epoxy-based resists have been used in lithography for many years. They are applied in UV, e-beam and X-ray lithography due to their high versatility with film thicknesses from < 100 nm to \> 1 mm and recently have been suggested also to be used in nanoimprint lithography (NIL) [1]. Each of these applications requires an adapted resist composition meeting the very specific demands of each type of lithography.

Here we report the new epoxy-based curing resist mr-NIL 6000 designed for thermal NIL, where the curing reaction is initiated by UV exposure and subsequently occurs in an annealing step, which corresponds to the post-exposure bake in UV lithography. Especially for the application in NIL the requirements to the resist are very different from those of radiation-based lithography. Essentially, sufficient sensitivity is important for short cycle time, whereas pattern resolution and contrast do only play a minor role. The glass transition temperature Tg of the original resist system (before curing) is decisive for the imprint temperature to be chosen. An epoxy resin with low Tg was designed allowing imprinting at moderate temperature. The imprint temperature on its part roughly determines Tg of the cured resist and, hence, affects the temperature of the mould release and also the thermal stability of the imprints. Thus, an imprint at too low temperatures will result in insufficient thermal stability of the imprinted patterns.

The aim of the investigations was to elaborate the optimum processing conditions for the epoxy resist and besides to obtain cycle times as short as possible. The presented results refer to an imprint process, where the imprinted resist is exposed by UV light and the curing reaction occurs immediately in the machine.

UV-coupled differential scanning calorimetry (Photo DSC) was applied to assist the screening of the resist composition and above all to help establishing the most suitable conditions for the particular process steps as the prebake conditions and the imprint step itself including exposure dose variations and finally the temperature of the mould release.

Besides, flow tests were carried out with the imprinted and cured resist patterns at different temperatures by means of AFM measurements. They gave a rough estimate of the respective degree of curing and revealed the imprinting conditions necessary for achieving sufficient thermal stability that is required for an isothermal imprint process as well as in following processes, e.g. in metallisation or etching processes.

An optimum imprint temperature of 100 °C - 120 °C, preferably 120 °C, was determined. The flow tests showed that the imprinted patterns exhibit good dimensional stability at 120 °C under these conditions. This allows releasing the mould at the imprint temperature and running an isothermal process this way. The curing reaction in the mould during imprinting enables excellent pattern transfer fidelity and a high aspect ratio of the imprinted features. A short cycle time could be achieved so that the resist is well suitable for industrial applications.

6517-83, Poster Session

Structure and stability characterizations of anti-adhesion self-assembled monolayers formed by vapor deposition for NIL use

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Anti-sticking efficiency of the stamps remains a key issue in Nanoimprint Lithography. The anti-adhesion properties of commonly used Si- or SiO2-based stamps can be improved by binding fluorinated chlorosilanes covalently to the surface. During the formation of the SAM, SiCl3 groups react with adsorbed water present on the substrate surface to form silanols, which then condensate first with neighbours and then with the hydroxyl groups on the substrate. This leads to a covalently bounded film to the substrate by Si-O-Si bonds. Two techniques are used for the formation of this self-assembled monolayer: liquid phase deposition or vapour phase deposition. For NIL use, although the liquid phase is largely used with regard to its ease, results won’t be as good as vapour process in term of release agents formed.

The most important factor to obtain a good anti-adhesion in this kind of coating is the number of fluorine atoms per surface area which has to be as high as possible and in particular CF3 groups which naturally present a lower critical surface tension compared to CF2. The problem

is then that during the SAM formation, a deviation from the idealized layer is observed which leads to an increased presence of CF2 group on the surface and then to a less effective anti-adhesion layer.

We will present here the study of vapour deposition of the F13-TCS molecule for the formation of an anti-adhesive layer for both thermal and UV-NIL processes. Stamps used for these processes are respectively silicon and quartz substrates and both are compared. Several deposition procedures are investigated and characterized. First depositions present promising results with surface tensions as low as 12mN/m on both silicon and quartz.

The structural morphology of the formed SAM is now particularly under observation. The morphology of the layer is analysed by the mean of FTIR measurements using an ATR technique. The quantitative study of the spectra will allow us to determinate the angle of inclination of the molecules and then to estimate the density of the layer. This technique, combined to static and dynamic contact angles, ellipsometry and AFM measurements will allow us to have a good idea of the structure of the grafted layer and its ability to present good anti-adhesion properties.

The stability of this formed layer during NIL processes is another important issue and will be tested. Thermal and pressure stabilities of the anti-adhesive layer will be study, first separately and then combined, for hot embossing NIL use. Same study with flash UV and printing, first separately and then combined, will be done for UV-NIL process. The degradation of the SAM due to these different parameters will be analysed using the same tools as previously mentioned.

6517-84, Poster Session

Template flatness issue for UV curing nanoimprint lithography

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UV curing NanoImprint Lithography (UV-NIL) is seen as a promising Next Generation Lithography (NGL) because of its high throughput, high resolution and alignment capabilities. However, contrary to the commonly used lithographic techniques which use 4X or 5X masks, nanoscale features required by the increasingly scaling down trend in microelectronic domain need to be directly patterned in quartz templates. That is why the template fabrication processes for UV-NIL have been widely investigated especially for high resolution electron beam lithography and the subsequent dry etching step that has to be performed. The template flatness specifications as well as its impact on the uniformity and quality of the imprinting features hasn't been reported yet, though. This is what we propose to study via different template fabrication processes.

One of the few common points between the UV-NIL tool suppliers is the requirement of thick fused silica templates (typically, few millimetres). However, the etching step in such a substrate is particularly difficult because of the insulating properties of the fused silica. This implies that one needs to have specific etching tools available only within industrial mask shops.

We have developed an alternative technique that consists of patterning and etching thin fused silica substrates that are then cut at the template size and assembled with a dummy template, which has been preliminary diced and micromachined according to the tool supplier requirements. Thus, the difficult etching step into a thick insulator substrate is avoided. We have then used two techniques to assemble the thin fused silica piece to the dummy template: the first one consists of gluing it, and the other one is the wafer bonding process.

The gluing process is carried out manually with a UV curable glue spread on the template surface and irradiated for 15 seconds with wide spectra UV lamp. On the other hand, the wafer bonding process is performed in a specific mini bonder once the surfaces that will be in contact are subjected to a hydrophilization treatment. In order to strengthen the hydrogen bonds created during the pre-bonding step, the stack composed of the thin fused silica die on the dummy thick quartz holder is annealed at 200°C for 2 hours.

The flatness of the dummy template as well as the one characteristic of the assembled pairs is then evaluated with a Fizeau interferometer. As expected, the curing step of the glue is shown to induce stresses that bend the thin fused silica piece while the template assembled by the wafer bonding technique produces much flatter stamps.

The different templates were then tested for UV-NIL patterning using an EVG NIL Stepper. It was shown that a rather thick resist needs to be span on the substrate in order to imprint over the whole active area when using the glued stamps (to compensate their unflatness), while thin resists can be used for flatter templates. We will then investigate the impact of the template flatness on the resist residual layer uniformity.

6517-86, Poster Session

Imprint solutions, costs, and returns of patterning LED's

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High resolution patterning of LED's has shown the potential to significantly increase the light output. There are 3 different imprint strategies being proposed to manufacture these devices. These imprint solutions and all the support equipment for cleaning, coating, and etching form an imprint cell. This paper will compare the imprint cell solutions and provide a highly condensed review of the literature on patterning impact on LED performance. The net result is an assessment of the costs of patterning in LEDs's and the potential returns to the manufacturer.

Imprint is probably the only patterning technology that can deliver sub 100 nm features at a low enough cost to be of interest to the LED manufacturers. Patterning fine features on LED wafers must be able to deal with rough, non flat wafers. The competing imprint solutions rely on either;

1) flexing the wafer or

2) flexing the template

3) or making the surface of the template compliant,

The published data on wafer non- flatness, and the compliance of the different solutions will be compared.

The literature and vendor data for the available solutions for all the operations in the imprint call operations are analyzed and compared to form a "buyers guide" to imprint on LED's.

Finally the processing cost of adding patterning to an LED is shown to be less than $10 a wafer. The potential cost scenarios of the different imprint techniques will be compared.

The return to manufacturers, of patterning on LED's, involves increasing the light output by improving either light creation or extraction. Patterning the LED with photonic crystal (PC) structures has been shown to control the shape and power of the output beam. This shape control makes them very useful for illumination applications such as projection displays where spot size is critical. The increase in power is an advantage in all lighting applications.

Patterning is also used to create webs of conductors to spread current uniformly through large devices. Large devices tend to be more efficient because the patterned area must be as long as the decay length of the modes (\> 250 μm). Large die help by reducing number of packages per installation, at the expense of increased heat dissipation.

Finally the quality of the GaN material itself can be improved by patterning the growth substrate and then using lateral overgrowth epitaxy.

6517-87, Poster Session

Whole wafer imprint patterning using step and flash imprint lithography: a manufacturing solution for sub-100-nm patterning

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Imprint lithography has been shown to be an effective technique for the replication of nano-scale features1. When the imprint material is a UV crosslinkable liquid, it is possible to perform the patterning process at room temperature and ambient pressure, which enables good pattern

fidelity, short processing times, and reduced process defectivity2. Imprinting whole wafers using drop on demand dispense techniques offers improved throughput and nanopatterning over wafer topography in excess of 10 μm. Template fabrication of arbitrary whole wafer patterns offers unique challenges for 1x feature fabrication. The resolution and pattern area of the imprint approach is strictly dependent on the ability to create a 1X master template. This paper will provide a detailed description of whole wafer templates, imprint materials and processes, and etch processes that have been employed to create a whole wafer archetype process through hard mask patterning. Particular attention will be given to high volume manufacturing focused on whole wafer template fabrication, throughput and pattern fidelity.

Step and Flash Imprint Lithography (S-FILTM) makes use of templates that can be fabricated with the same patterning and etch transfer processes that are used for manufacturing phase-shifting photomasks. In the case of whole wafer templates the master die pattern is fabricated using conventional techniques. The working template carries the full wafer die pattern imprinted by step and repeat using the master. (Figure 1) The SFIL/R process is used for patterning the working template4. The structure, pattern fidelity and critical dimension uniformity of the master and working templates will be discussed. Figure 2 is an SEM micrograph of imprinted features from a working template.

The working templates are used to imprint wafers in the 2" through 4" range in the Molecular Imprint whole wafer imprint tool (Figure 3). UV curable resist materials are drop wise dispensed on the wafer, brought in contact with the template and cured. The mean residual layer of 90 nm half pitch pillars, used to make holes in this reverse tone process, is < 35 nm with a cross wafer range of < 10 nm (Figure 4). Wafer throughput of \> 40 wafers per hour on thermal oxide coated silicon and sapphire wafers has been demonstrated. One of the major advantages of the whole wafer imprint process is that the template conforms to the wafer surface, allowing arbitrary pattern generation (Figure 5) of sub-100 nm features over wafer topography in excess of 10 μm. This is in contrast to sub-100 nm optical imaging by DUV steppers where the depth of focus prevents imaging of such features over wafers with such a high degree of nanotopography.

In a number of applications substrate etching requires aggressive etch chemistries and thus hard mask etch processes have been developed. The SFIL/R resist layers demonstrate good selectivity to SiN and SiO2 hard mask etch processes (Figure 6). Imprint and subsequent hard mask patterning results will be described with specific focus on residual layer performance, imprint pattern fidelity, and feature critical dimension through hard mask patterning. A summary of the process flow and equipment requirements for whole wafer imprint pattern generation will be given.

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6517-88, Poster Session

Exposure characteristics of character projection-type low-energy electron-beam direct writing system

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In order to break through a technological trade-off of high throughput with CP exposure versus mask-less in the single beam EBDW strategy, we have introduced a standardized CP aperture method that makes it possible to reduce the number of EB shots without frequently aperture making and a low energy EB exposure with a benefit of proximity effect free.

According to this concept, a low energy EB of less than 5keV has a potential to expose character patterns without inter- and intra- proximity effect correction in combination with variably shaped beam (VSB) exposure.

This is an advantage of low energy EB in comparison with the high energy EB.

We confirmed the proximity effect in low-energy EBDW with the CP exposure by changing the number of holes in the one CP shot.

In the EBIS, the maximum size of a CP shot is 5 micrometer-square.

140nm 1:1 hole pattern in the maximum size of the CP shot includes up to 18x18 hole array.

In the examinations of CP exposure, 1:1 hole patterns were exposed by various sizes of CP shots, only one hole, 3x3, 5x5, ..., and 18x18 hole arrays without any modulation of exposure dose.

The sizes of hole patterns were measured from an edge to the center of exposed region.

From the results of measurements, the sizes of hole patterns were slightly varied, but the effect of the size of CP shot might not be confirmed.

Although the optimum dose for each size of the CP shot was varied because of coulomb effect by the beam current of a shaped CP shot, the optimum dose for each CP shot can be controlled by referring its size of CP shot.

We also confirmed the proximity effect by other examinations, for example, material and structure dependence under the resist layer of substrate.

It is found that the low energy EBDW is useful for exposure of practical patterns of logic devices by the CP exposure with higher throughput, because the proximity effect is so small that complicated corrections due to the adjacent pattern and structure of substrate under exposure layer are not necessary.

In this paper, we show the characteristics for exposure of low-energy EBDW.

6517-89, Poster Session

Data processing system in EB direct writing to obtain photolithography friendly resist patterns

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System-on-a-chip and ASIC devices are low volumes, wide variety, and short product-life cycles. Moreover, before mass production, low volume production is needed to manufacture engineering samples, prototype LSIs, or to verify the function of chip on silicon. The total cost to produce low-volume parts is now dominated by mask costs since masks costs cannot be amortized over a large number of shipped products. Maskless lithography (ML2) is the most effective method is solving this cost problem. For instance, using electron beam (EB) direct writing technology to low volume parts production can amortize the total mask costs.

However, it is a problem that the shape of resist patterns differs from the difference between the source of light and the method of photolithography and EB lithography [Fig. 1]. In using an exposure technology different from mass production, it is caused a different physical phenomenon in the lithography process, and it forms different images. In order to improve the difference, it is necessary to change the following process conditions and parameters. Otherwise, there are influences in the characteristic and the yield of LSIs.

There is a clear need to reduce the negative implications of difference of the shape of resist patterns caused by using different lithography technology. We have developed a data processing system which makes the EB exposure data to obtain the same shape as the shape of resist patterns by photolithography.

The data processing system consists of two parts [Fig. 2]. One makes a design data library for EB exposure. Another one is replaced the design data for manufacturing purposes with pertinent data to this design data library for EB exposure, and the replaced design data for EB exposure is converted into EB exposure data.

In the former process, it is executed whenever a design rule is defined. First, it converts the design data of IC parts (i.e. SRAM cell, UNIT cell, I/O, Via hole, metal wire etc.) into each exposure data. Second, it

calculates the shape of resist patterns on a wafer of these exposure data by each lithography simulation. After that, it takes the difference data of each shape obtained from those simulations, and it corrects the original design data by using the difference data. Lastly, it registers as a design data library for EB exposure. In the latter process, it is executed whenever the design data for manufacturing purposes is input.

By this system, we have been able to obtain shape equal to photolithography in using EB lithography [Fig. 3]. As for this EB exposure data, an increase in the number of shots is suppressed to the minimum by using the cell projection method.

6517-90, Poster Session

Recent progress of a character projection-type low-energy electron-beam direct writing system

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We have developed a character projection (CP)-type low energy electron beam (EB) direct writing system (EBDW) called EBIS (Electron Beam Integrated System). In order to break through this technological impasse of high throughput via CP versus mask-less in the single beam EBDW strategy, we have introduced a standardized CP aperture method that makes it possible to reduce the number of EB shots without frequently aperture making and a low energy EB exposure with a benefit of proximity effect free.

The features of introduced equipment engineering expertise to realize our low energy EBDW with CP are as follows. (1) The data conversion system involves a standardized CP aperture making function. (2)A compact EB column equipped with monolithic deflectors and lenses was developed to resolve less than 100 nm L/S patterns at 5keV. (3)A voltage contrast imaging method using a micro channel plate was introduced for the buried mark detection. (4)A platform including a full 300mm wafer stroke air guided XY-stage and a naked wafer transportation system, was newly designed for the EBIS system.

We have been working to verify the fundamental performances. Through the experimental verification of the system, the capability of 100nm-hp resolution has basically been verified. This paper describes the current status of our EBIS system.

6517-91, Poster Session

Shot noise effect on LER and throughput in LEEPL systems

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LEEPL (Low Energy Electron-beam Proximity Projection Lithography) uses low energy of electrons of 2KV.[1] In such an low energy , electrons are known to behave quite differently in the resist to high energy electrons such as in 50 KV. Their energy loss rate is very high and they deposit almost all energy within the resist whose thickness is less than 100nm and thus the resist shows very high sensitivity. Under these condition it has been concerned that the statistical variation of electrons known as " shot noise" may deteriorate LER (Line Edge Roughness) and CD of the image patterns. On the other hand the experimental observations made by LEEPL tools and observations by others [2] have shown LER (3 sigma value) of the resist after development is much smaller than a simple consideration of the shot noise variation due the primary electrons alone represented by 3 / square root of N ,where N is the number of the incident primary electrons. In order to estimate quantitatively how much smaller the effective LER , we introduce a " reduction factor: f " which is the ratio of the shot noise component of the observed LER against 3* square root of N/ N: the shot noise factor due to the primary electrons. The value of " f " was estimated as 0.38 from three independent methods, namely two from experimental results and one from Kotera's computer simulation [3]. This translates that the minimum number of the incident primaries per CD square is 588 electrons and the required dose for 100 nm line pattern is 0.94μC/cm2. These values are approximately two times larger than the experimental values obtained in [2] and significantly smaller than the values predicted by [4] The above analysis can be extended to taking account of the effect of acid diffusion in the case of CAR resist. Following Kotera's simulation data [3], one can obtain, for an example, the value of diffusion dependent " f " as 0.25 at the acid diffusion length of 20 nm and the corresponding minimum number of the incident primaries per CD square as 254 electrons.

As consequence of this analysis, we will discuss the shot noise-limited-throughput and -CoO of LEEPL systems for 65, 45, and 32 nm device node applications in comparison with other lithography systems.

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6517-92, Poster Session

CD budget analysis on hole pattern in EUVL

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Extreme Ultra Violet Lithography (EUVL) is a promising candidate for a next-generation lithography because of the excellent resolution for hp 32 nm technology node and beyond. In order to manage CD error factors and to construct production available EUVL technology, CD error budget analysis is very important. 3-D mask structure effect should be considered in CD budget analysis of EUVL because it distorts a near field image as shown in Fig. 1. Therefore, we focus on a hole pattern that is considered very sensitive in 3-D effect, because it is surrounded by absorber walls. In this paper, we introduce simulation study of our CD budget analysis of hole pattern that has not been introduced sufficiently on pattern layout dependence. Moreover we think that the relationship between printability and blur function that is composed of each blur effect in exposure tool should be studied.

Our CD budget analysis is done as follows. At first, we investigate 3-D mask effect and its influence on the printability, using MEEF depending on pattern layout. Secondly, we investigate blur effect caused by a multilayer surface roughness on a scanner mirror, and various statistical noise which affects proximity effect and usable depth of focus. Thirdly, the spatial distribution of experimental printability (exposure latitude) is investigated comparing to simulated printability that includes MEEF and blur effect. And spatial distribution of blur function is estimated from this comparison. Finally we budget individual CD errors factor from the view of impaction on blur functions.

In this paper we introduce the first and the second steps.

6517-93, Poster Session

Fidelity of rectangular patterns printed with 0.3-NA MET optics

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Rectangular patterns are necessary for the isolation layer and other layers of the ULSI fabrication process. In optical lithography, fine rectangular patterns tend to deform because of optical proximity effects. This requires complex correction for mask patterns. Since extreme-ultraviolet lithography (EUVL) uses a much shorter wavelength than optical lithography does, it should provide better pattern fidelity. In this study, rectangular patterns of various sizes were printed with the micro exposure tool (MET) at the Lawrence Berkeley National Lab. (LBNL), and their fidelity to the mask patterns was evaluated.

The projection optics of the MET consist of two aspherical mirrors. The magnification is 1/5, the numerical aperture (NA) is 0.3, and the incident angle of EUV light on a mask is 4 degrees. Annular illumination (Sigma= 0.3-0.8) was used for printing. EUVL masks were fabricated using mask blanks developed by ASET and a dry-etching process developed by Dai Nippon Printing. The masks consisted of a 6-inch-square (6025) glass substrate, a 40-pair Mo/Si multilayer, a 10-nm-thick Cr buffer layer, and a 65-nm-thick TaGeN absorber layer. Most of the experiments

employed MET-1K (120 nm), which is a positive-tone chemically amplified EUV resist. The rectangular patterns had dimensions of 5WxW and the spaces between the patterns had a width of W (W = 45, 50, 60, 70, 80, 90 nm).

The experimental results showed the pattern fidelity of 90-nm-node rectangular patterns to be fairly good. However, 45-nm-node patterns exhibited considerable shortening in the lengthwise direction. We used the SOLID-EUV lithography simulator (Sigma-C) to analyze the cause of the shortening. The wavefront error of the MET optics was assumed to be 0.7 nm rms (Zernike 37-fit) and the flare of the optics was assumed to be 10%. The simulation results showed little deformation of the aerial images of rectangular patterns, even for 45-nm-node patterns. Since it was difficult to explain the observed shortening in terms of the effects of wavefront error, flare, or defocus, we speculated that the shortening might be caused by acid diffusion during post-exposure baking (PEB). When we used a diffusion length of 20 nm for acid diffusion, the calculated shapes of rectangular resist patterns agreed well with the experimental results for various sizes. Thus, we concluded that acid diffusion was the main cause of line shortening in rectangular patterns printed with the MET. To mitigate the shortening, the diffusion length of the acid in the resist should be reduced by improving either the material composition of the resist or the PEB process.

We would like to thank International SEMATECH for giving us the opportunity to use the MET. We would also like to thank the CXRO group at LBNL for their assistance with the printing experiments using the MET. The EUVL masks were fabricated by Dai Nippon Printing Co. Ltd, and MET-1K resist was supplied by Rohm & Haas. This work was supported by New Energy and Industrial Technology Development Organization (NEDO).

6517-94, Poster Session

EUV exposure experiment using programmed multilayer defects for refining printability simulation

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Extreme Ultraviolet Lithography (EUVL) is one of the promising candidates among several lithography options for hp32nm node and beyond. However, fabrication and qualification of defect-free multilayer mask blanks are critical challenges for broad adoption of EUVL. With recent improvement of actinic and non-actinic mask blank inspection, their prospective sensitivities have reached the verge of the uncertainty window in which the minimum size of the printable defects is predicted to fall in hp32nm node. Therefore, it is the right time for shifting some efforts toward more accurate prediction of minimum size of printable multilayer defects both by EUV exposure experiments and associated simulation work.

One of the challenges in the prediction of multilayer defect printability is that it depends not only on the surface profile of multilayer defects but also on the morphology of the multilayer underneath. We have employed finite-element-method (FEM) based simulation to solve electromagnetic field equation with deformed multilayer. One of the advantages of this method is the decomposition of the structure into triangular or tetrahedral cells which has a high compatibility with the expression of slight changes in the shape of multilayer defects. Figure 1 shows a schematic cross sectional view of the computational domain with programmed multilayer defects partially covered by absorber patterns. This layout is based on one of the test patterns in the actual programmed defect mask (PDM) that was fabricated by HOYA Corporation, and is being used for exposure experiments. The distance between multilayer defect and the adjacent absorber line is designed to vary by sub-pitch step with gvernier-like structure. Cross sectional layer structure is designed to emulate gdecorative mode of the multilayer deposition on rectangular seed of defect at the bottom of the multilayer, and each material domain is triangulated to construct a polygon that resembles a cross-sectional TEM image.

Actual exposure experiments are carried out using the micro exposure tool (MET) in Lawrence Berkeley National Lab using the resist MET-1K. Figure 2 shows 80nm line and space patterns where one of the resist lines is printed by the mask absorber line partially overlapping the multilayer line defect underneath. The experiments demonstrated that the impacts of multilayer defects can be eliminated when they are fully covered by absorber patterns as evidenced by some of resist CD not affected by the multilayer defect fully covered by the absorber lines. Many of the resist CD were, however, significantly affected by multilayer defects nearby where the amount of CD variation was dependent on the overlapping size with absorber patterns. The change in resist CD affected by multilayer defects with various overlapping sizes were systematically measured in a dose-focus matrix. In this paper, the simulation and the experiment results are compared in terms of applicability of the simulation to predict the impact of any minute difference in multilayer morphology onto defect printability, as well as to predict the allowable minimum extrusion of the tapered defect foot out of absorbers. The implication to multilayer deposition process will also be discussed.

This work was supported by NEDO.

6517-95, Poster Session

Lithographic metrics for the determination of intrinsic resolution limits in EUV resists

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Resist resolution remains a significant issue for EUV. Strong concerns remain with the use of chemically amplified resist owing to their diffusion characteristics. Currently EUV resist development is primarily focused on large-scale screening efforts in an attempt to identify platforms showing promise in a variety of areas with resolution arguably being the parameter of highest importance at this time. The characterization of the intrinsic resolution limit of resists, however, is not a trivial issue due to practical complications such as pattern collapse and top-loss. Note that the intrinsic resist resolution limit has been claimed to be determined by the resist diffusion length and various metrics have been proposed to characterize this diffusion length as well as resist resolution. Here we investigate a variety of resolution and diffusion length metrics and study the correlation between these metrics and observed resist performance when applied to a variety of leading EUV resists. The metrics we study include iso-focal bias, line-edge-roughness correlation length, resist modulation transfer function, corner rounding, and through-dose sub-resolution contact printing.

6517-96, Poster Session

Absorption of extreme ultraviolet radiations in different photoresists

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Extreme ultraviolet (EUV) lithography is one of the promising techniques for the fabrication of semiconductor features below 30 nm. One of the key parameters that can affect photoresist performance is their absorption characteristics at EUV wavelengths. The measurement of the absorption length or absorbance is important because it causes the dose to vary through the thickness of resist which results in sloped sidewall angle. One method for measuring absorption length of a resist is by direct measurement of the transmission of EUV radiation through the resist when it is on a transparent membrane. These measurements have been performed for various resists using EUV radiation from an Energetiq EQ 10M EUV source and an AXUV EUV sensitive photodiode. A 100nm thick silicon nitride membrane is spin coated with different resists and placed in proximity of the photodiode. The thickness for the photoresist is measured using cross-section scanning electron microscope (SEM). The results will be shown comparing the absorbance for different photoresists currently used for extreme ultraviolet lithography.

6517-97, Poster Session

Analysis of relation between optical and latent image condition and line-edge roughness in EUV lithography

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It is thought that the roughness observed at resist edge (LER/LWR) appeared in a replicated pattern is a result of many complicated and

correlating factors which causes nonuniform dissolution boundary in resist. The authors has been interested in the influence of optical image to LER/LWR, extremely to the role of image slope and contrast. To clarify which (i.e., slope or contrast) is more directly affects to roughness, the lines-and-spaces (L/S) patterns were replicated by changing pattern width, illumination, dose, defocus, and resist. To change the illumination condition can give us resist patterns with various optical image slopes and contrasts. The replication was performed by EUV microexposure tool HiNA in ASET (located NTT R&D Center fs Super-Alis) and MET in SEMATECH (located Berkeley ALS). They both have NA of 0.3 which are performed by 2 coaxcial asheric mirrors with a center obscuration. The measured roughness indicated that it has strong correlation with calculated aerial image contrast regardless to pattern sizes or illumination, as shown in Fig.1.(aerial image was calculated by SOLID-EUV). So it can be recognaized that the image contrast has closer effect to roughness. To confirm it more directly, we evaluated the latent image in resist by measuring the pattern width vs. exposure dose and compared with LWR. The results for 70 nm L/S by the resist MET-1K in annular illumination are shown in Fig. 2, for HiNA and MET with the calculated aerial images. In this figure the dose in the horizontal axis is normalized with that when the measured resist pattern width was 70 mn. We found that though the ideal (calculated) image slope are similar in HiNA and MET, the evaluated latent image showed bluring and it was worse in HiNA. The LWR of HiNA was also larger than that of MET. The image blur causes degraded image slope and contrast simultaneously, so this result makes confusion in estimating which is more important in edge roughness. Another founding in Fig.2 was that the LWR shows bow shape according to the dose (in other words, to the pattern width) appearing smallest LWR when the patten width is about center in replicable dose range, although the image slope in this range is almost same. So we guess that the image slope is not the principal source within image originated roughness. On the other hand, there were experimental evidence that the values of LER at one side of L/S pattern sometimes showed significant differences with those of the other side (i.e., left edge and right edge is inconsistent). The differences between those edges were sometimes more than double in 3 sigma. The calculated image showed that under the existence of aberration in projection optics, or with an unsymmetrical pupil fill of diffracted light, aerial image of L/S pattern shows unsymmetrical edge slope. This indicates that also the image slope has a not negrigible effect on LER. In this paper we will discuss the relation between the roughness and image contrast/image slope carefully.

This work was supported by NEDO. We acknowledge International SEMATECH for giving us the opportunity to use the MET. We deeply thank the CXRO group at LBNL for their assistance with the printing experiments using the MET. MET-1K resist was supplied by Rohm & Haas.

6517-98, Poster Session

Process window study with various illuminations for EUV lithography applications

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EUV lithography has the ability to support 22 nm logic manufacturing and beyond. Similar to the DUV lithographic systems, partial coherence on EUV lithographic systems can have a big impact on process latitude for critical layers. Thus, it is important to understand the effect of partial coherence on EUV imaging systems. Knowledge gained can then be applied to verify lithography models and aid in future tool designs.

In this paper, process windows with various illumination settings are investigated. The experiments are done using the MET station at the Advance Light Source (ALS). In addition to the annular and dipole illuminations which reported in our last paper, C-quad and quad illuminations are used to explore the impact of the partial coherence on the process window. Even though the system has resolutions below 30nm dense lines, the exposures are targeted for 50 nm, and 45 nm dense features due to the resist limitation.

The experimental results are compared with I-Photo (Intel's lithography modeling tool) simulation results. Both resist based model and aerial image threshold model are used for the comparison study. The experimental results correlate well with the resist based simulation results, but the some discrepancies are observed for the aerial image threshold cases. We believe the discrepancies are due to the resist limitations. As expected, the dipole and C-quad illuminations show the largest Depth of Focus for dense lines and spaces.

6517-99, Poster Session

Characterization of low-order aberrations in the SEMATECH North MET tool

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Previous papers have reported on print-based methods developed to measure the aberrations in the Berkeley EUV microfield exposure tool (MET). The data showed that the tool has larger aberrations than those measured during interferometry (both visible and EUV) performed before the optic was integrated into the tool. The same analysis has been performed on the SEMATECH North MET to measure the low-order aberrations.

As with the Berkeley tool, quantitative measurement of cross-field astigmatism has revealed elevated levels of astigmatism in the SEMATECH North tool. Additionally, we present quantitative measurements of field tilt and curvature, coma, and spherical error. Pending the availability of new data, we also investigate the effect of system temperature on aberrations.

6517-100, Poster Session

EUV lithographic flare and MTF measurements on Intel micro-exposure tool

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Flare and modulation transfer function (MTF) as a function of feature size and pitch in horizontal (H) and vertical (V) directions have been measured on Intel's Extreme Ultra-Violet (EUV) Micro-Exposure Tool (MET) with a high sensitivity photo resist. The high sensitivity photo resist does not have cross-link at the high doses required to measure Flare and MTF. The predicted value for intrinsic flare from Mid-Spatial Frequency Roughness (MSFR) of mirror surfaces is 3.5% at 0.5 um feature size. And the measured flare in the H direction is 7.7% and is almost same the flare in the V direction. In this paper we report the measurement results of Flare and MTF on MET as a function of feature size in both H and V directions .

We observe higher contrast at smaller pitches for the H features. The predicted trend of the MTF Vs pitch using the measured wavefront error is closer to the H features. This confirms our earlier observation that the imaging of vertical features on the Intel MET is not as good as the horizontal features.

6517-101, Poster Session

Characteristics and prevention of pattern collapse in EUV lithography

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As the integration of semiconductor process goes large and complex, the line width of a pattern has been reduced continuously. In this study, we investigated the pattern collapse with resolution under 32 nm printed by extreme ultra-violet lithography (EUVL). Pattern collapse means that pattern is bend, break, and tear of the resist, and affects in production and yield rate of semiconductor. To search for pattern collapse characteristics of EUVL, we compared the height of the resist and the space width. We predicted the pattern collapse with the calculation about external force and allowable stress that pattern receives. EUV resist has smaller adhesive strength and etching tolerance than currently available DUV and ArF resists, and has confirmed that the pattern collapse happens more easily. Also, we searched alternative ways and conditions that can prevent or minimize the pattern collapse for EUVL.

6517-102, Poster Session

Extreme ultraviolet interference lithography with incoherent light

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In order to address the crucial problem of high-resolution low line-edge roughness resist for extreme ultraviolet (EUV) lithography, researches require significant levels of access to high-resolution EUV exposure tools. The prohibitively high cost of such tools, even microfield tools, has greatly limited this availability and arguably hindered progress in the area of EUV resists. To address this problem, we propose the development of a new interference lithography tool capable of working with standalone incoherent EUV sources.

Although EUV interference lithography tools do currently exist, presently used designs require illumination with a high degree of spatial and/or temporal coherence. This, in practice, limits current systems to being implemented at synchrotron facilities greatly limiting the accessibility of such systems. Here we describe an EUV interference lithography system capable of overcoming the coherence limitations, allowing standalone high-power broad sources to be used without the need for excessive spatial or temporal filtering. Such a system provides promising pathway for the commercialization of EUV interference lithography tools.

6517-103, Poster Session

A short-pulsed laser cleaning system for EUVL tool

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Traditional methods of reticle protection, such as using a pellicle, cannot be applied to EUVL tool. There is a possibility that some particles in the vacuum chamber adhere to the surface of a retilce. In order to resolve this critical issue, in situ cleaning methods of particles on a reticle need to be developed. As an in situ method, we propose a short-pulsed laser cleaning system. This technique consists of a perfect dry process, and will have easier and wider application than conventional techniques. In order to confirm whether it can be used inside the EUVL tool or not, we have to verify experimentally that it is possible to remove particles in vacuum without any damage to a Mo/Si multilayer. In the present study, both Ru-capped and Si-capped Mo/Si multilayer mirrors have been used. As organic contaminant particles, monodisperse fluorescent PSL spheres are deposited on the mirrors by using an atomizer. As a short-pulsed laser, a Q-switched YAG Laser (wavelength: 266~1064 nm, pulse width: ~7 ns) is used. These experiments have been conducted in atmosphere or in vacuum. As a result, at the pressure on the order of 10^-3 Pa, a removal rate of organic particles (size: 100 nm) on the surface of multilayer mirrors is about 100 %. The laser irradiation conditions are that the laser wave length is 266 nm, the laser fluence is approximately 20 mJ/cm2, and the numbers of pulse is 400. In the above conditions, it is not found that there is any particular damage on the surface of multilayer mirrors. In addition to these results, an interesting phenomenon, which it has been easer to remove particles in vacuum than in atmosphere, has been found. As inorganic contaminant particles, 500 nm SiO2 particles and 500 nm Ni particles are deposited on a bare-Si wafer by using a powder dispersion generator. The removal rate is below 10 % at the laser fluence around 100 mj/cm^2 and 100 pulses in atmosphere. In vacuum, however, the removal rate increases up to about 50 %. These experimental results are considered that drag force exerted on a particle by surrounding gas molecules is neglected because a gas at the pressure on the order of 10^-3 Pa is in free molecule regime (Knudsen number \> 10), where these particles can easily leave the Si surface.

6517-104, Poster Session

Mo/Si multilayers with enhanced capping layers

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The lifetime of Mo/Si multilayer-coated projection optics is one of the outstanding issues on the road of commercialization of extreme-ultraviolet lithography (EUVL). A serious problem of Mo/Si multilayers capped by silicon is the considerable reflectivity degradation due to carbonization and oxidation of the silicon surface layer under exposure by EUV radiation.

In this study, we focus on titanium dioxide (TiO2) and ruthenium dioxide (RuO2) as promising capping layer materials for EUVL multilayer coatings. The multilayer designs as well as the deposition parameters of the Mo/Si systems with different capping layers were optimized in terms of maximum peak reflectivity at the wavelength of 13.5 nm and long-term radiation stability. Optimized TiO2 capped Mo/Si multilayer mirrors with an initial reflectivity of 67 % presented a reflectivity drop of 0.6 % after an irradiation dose of 760J/mm2. The reflectivity drop was explained by partial oxidation of silicon sublayer. No reflectivity loss after similar irradiation dose was found for RuO2 capped Mo/Si multilayer mirrors having initial peak reflectivity of 66 %.

Finally, the reflective properties and long-term radiation stabilities of Mo/Si coatings with TiO2, RuO2, Ru and C capping layers were compared. The major results of the comparative study, out of band (OOB) reflectivity, and photo-catalytic behaviour will be presented and discussed in this paper.

6517-106, Poster Session

Polarization dependence of multilayer reflectance in the EUV spectral range

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The development of EUV lithography is critically based on the availability of suitable metrology equipment. The EUV reflectometry facility of the Physikalisch-Technische Bundesanstalt (PTB) at the electron storage ring BESSY II is designed for at-wavelength metrology of full-size EUVL optics with a maximum weight of 50 kg and a diameter of up to 550 mm. For peak reflectance, a total relative uncertainty of 0.14% is achieved with a reproducibility of 0.07 %. The long-term reproducibility of the wavelength is 0.008 % and the short-term repeatability below 10-5. To provide the necessary data for the transfer of these high-accuracy measurements which use linearly polarized radiation to EUV optical components under working conditions, PTB has upgraded the EUV reflectometer for measurements at up to 20° angle of incidence in P polarization. We will discuss representative polarization dependencies obtained at model multilayer coatings. It will be shown that a detailed model of the multilayer stack is needed in order to correctly predict the angle- and polarization dependence of the multilayer reflectance. The exact knowledge of these dependencies is a prerequisite for the design of advanced high-NA EUV optical systems.

6517-107, Poster Session

Carbon deposition on multilayer mirrors by extreme ultra-violet ray irradiation

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Extreme ultraviolet (EUV) lithography tools are under development. Organic gases exist in the tool in spite of a vacuum. They cause carbon depositions on the multi-layer mirrors in the tool by EUV irradiation. It leads to reflectance degradations of the mirrors. This degradation is still one of critical issues of the tool development. We set up an ultra high vacuum experimental chamber at the synchrotron radiation facility SuperALIS SBL2 (Atsugi, Japan). The background pressure is 5.0x10-7Pa. It is possible to inject organic gas into the experimental chamber and measure reflectance of a mirror sample in-situ with EUV irradiation. We researched the dependences on organic gas species, organic gas pressure and EUV light intensity in the carbon deposition in order to understand this reaction.

EUV light was irradiated on a (Si/Mo) multi-layer mirror sample injecting organic gas like buthane (an aliphatic hydrocarbon, C4H10), buthanol (an aliphatic alcohol, C4H10O), methyl propionate (an aliphatic ester, C4H8O2), hexane (an aliphatic hydrocarbon, C6H14), perfluoro octane (an aliphatic fluorocarbon, C8F18), decane (an aliphatic hydrocarbon, C10H22), decanol (an aliphatic alcohol, C10H22O), methyl nonanoate (an aliphatic ester, C10H20O2), diethyl benzene (an aromatic hydrocarbon, C10H14), dimethyl phthalate (an aromatic ester, C10H10O4) and hexadecane (an aliphatic hydrocarbon, C16H34). Each organic gas pressure was adjusted to 1.0x10-5Pa and each gas injection was monitored by Quadrupole mass spectrometer. EUV doses were ~180J/mm2. These irradiations showed reflectance changes of mirror samples. Reflectances went up slightly and down. They were predictable for thin carbon depositions. To estimate the amounts of deposited carbons, mirror sample surfaces were measured by x-ray photoelectron spectroscopy. It was revealed that organic gases with heavier molecule weight or higher boiling temperature cause faster carbon depositions. At lower organic gas pressure, carbon deposition rates decreased. Carbon deposition rates increase linearly with organic gas pressure. Dependence on EUV light intensity was estimated from comparisons between a EUV beam profile and carbon distributions on irradiated samples. Carbon deposition rates increased rapidly, but became saturated at higher EUV light intensity.

Three reactions, an adsorption (the reaction rate constant: k1), a desorption (k-1) and a carbon deposition by EUV irradiation (k2), are taken into account to understand these behaviors of the carbon deposition. According to this model, it is reasonable that heavier organic gases and higher organic gas pressure cause faster carbon depositions. They seem to adsorb on the mirror surface easily and be fixed on it after EUV irradiation. Carbon deposition rates depend on EUV light intensity following 1-exp(-k2*EUV light intensity*time). In our experimental condition, k2 factors seem to be almost constant among organic gas species. k1 factor is the most important among the three reactions. Total carbon deposition rate is affected strongly by the adsorption.

This work was performed under the management of Extreme Ultraviolet Lithography System Development Association in the Ministry of Economy Trade and Industry program supported by New Energy and Industrial Technology Development Organization in Japan.

6517-108, Poster Session

Effect of deposition, sputtering, and evaporation of lithium debris buildup on EUV optics

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One of the critical issues within extreme ultraviolet (EUV) lithography is mirror lifetime and the degradation due to debris from the EUV pinch. This work models and experimentally measures the mitigation of Li debris from collecting on the surface of EUV optics through combined use of a He secondary plasma with plasma densities from 1010 to 1012 cm-3, evaporation from optic materials at elevated temperatures, and preferential sputtering off of the optic material. Profilometry, AFM, and SEM results show the ability to keep the EUV optic in an as received state while being exposed to EUV like debris. This expands the current knowledge base in understanding lithium interactions with a He plasma and optic surfaces. Previously, it has been demonstrated that the application of a secondary plasma source around the surface of mirror optics contaminated with low-energy sputtered material was able to remove a significant fraction of lithium and contaminant material is removed. This work expands the experimental matrix to investigate Li removal off of the surface of mirror optic materials as a function several competing variables. These variables include He plasma temperature, density, flux, and incident energy on the mirror optic as well as the temperature of the surface. An analytical model has been developed to help explain the prior measurements of lithium diffusion in mirror optic materials that will lend itself towards accurate prediction in various other mirror optic materials. The foundation of this model will include atomistic simulation empirical evidence from ongoing experiments, and theoretical arguments. This work improves the current state of the art knowledge in lithium-optic material interactions, experimentally test mitigation and renewal of optic materials, and develop a relevant model for the predictive capabilities of the mirror optics while expanding the knowledge base of lithium transport and interaction.

6517-109, Poster Session

Processes on Ruthenium surfaces related to degradation of EUV mirrors

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Our objectives are (a) to characterize the composition and stability of O-covered Ru surfaces that simulate surfaces of Ru-capped multilayer mirrors, under exposure to different background gases (hydrogen, water) and to radiation, and (b) to make secondary electron yield (SEY) measurements for clean Ru and O- and C-dosed Ru, using 13.5 nm radiation at Brookhaven's National Synchrotron Light Source.

It is generally believed that irradiation of Ru-capped mirrors in EUV exposure tools leads to Ru oxidation, due to radiation-induced surface chemistry in the inevitable background pressure of H2O. To examine the effects of electron irradiation on the accumulation of O on an initially-clean Ru(10-10) surface, we have bombarded the surface with 100 eV electrons while exposing it to D2O vapor from a molecular beam doser. Isotopically-labeled D2O was used to minimize crosstalk with background hydrogen. Measurements were made for a range of D2O pressures, from 10-8 to 10-6 Torr, and for the temperature range 150-300 K. We found that electron bombardment of clean Ru in background D2O vapor leads to substantial O chemisorption at high pressure (10-6 Torr) and low temperature (~200 K). Radiation-induced accumulation of chemisorbed O on Ru at 300 K in the presence of D2O vapor is a slow process, and accumulation of O on Ru-capped mirrors at 300 K may be correspondingly slow. This is qualitatively consistent with the predictions made in [1] concerning the very short lifetimes of adsorbed water on Ru at 300 K, and with calculations of H2O dissociation rates on Ru [2].

We compare the effects of atomic and molecular hydrogen (at hydrogen pressure up to 1x10-6 Torr) on the removal of chemisorbed O from the Ru(10-10) surface. Atomic H is shown to be very effective in removing O at 300 K, but molecular H2 is much less effective. The data suggest that H reacts directly with adsorbed O to make OH, and a second H atom reacts with OH to make H2O, which desorbs at 300 K.

The Secondary Electron Yield (SEY) of Ru-capped multilayer mirrors is an important parameter that greatly influences radiation-induced surface chemistry. The SEY of Ru(0001) was measured under ultrahigh vacuum conditions at beamline U4A of the National Synchrotron Light Source (NSLS) at Brookhaven National Laboratory. Absolute values of SEY were based on measurements using a calibrated silicon photodiode. The SEY (0.020) corresponding to the energy of EUV photons (92 eV) is near the MINIMUM value of SEY for Ru. This may be a factor that influences the effectiveness of Ru as a capping layer: dissociation of adsorbed gases caused by EUV-produced low-energy secondary electrons may be less effective on Ru than on other surfaces where the SEY is higher.

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6517-110, Poster Session

EUVL optics substrate recovery process: reflectivity and surface roughness

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Multilayer coating technology for Extreme UV lithography and the manufacture of optics substrates for these coatings is rapidly progressing. However, the development and optimization of the deposition processes of the thin-film coatings needs experiments on accurately prepared (surface figure, surface roughness) aspherical substrates. A possibility to recycle the usually costly substrates without damaging them would be very desirable. Substrate recovery layers (SRL) at the interface between the Mo/Si multilayer and the substrate have been proposed [1], but some removal procedures investigated

(wet-chemical etching, plasma etching or reactive ion etching) proved to affect the substrate surface and to increase its roughness. By consequence, the reflectivity decreases.

We have used an organic material as an SRL, and successfully removed the multilayer by using an organic solvent, a process which did not lead to damage of the substrate surface. In addition, we found that the reproducibility of the coating process, expressed as a variation of the coating centroid wavelength (CTW) value, did not diminish. Identical reflectivity, within 0.5%, and CTW values, within 2 pm, of multilayers deposited on recovered substrates have been measured. The SRL process was applied on different substrate types (Si, quartz, glass) with diameters up to 50 mm. We present results on the substrate recovery process, with special attention to the effect of the SRL on surface roughness and reflectivity measured at 13.5 nm.

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6517-111, Poster Session

Long-time durability of Ru capping layer for EUVL projection optics by introducing ethanol

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Ru-capped Mo/Si multilayers (MLs) are a promising candidate to be used for EUVL projection optics (PO) mirrors. It has been shown that reflectance degradation due to oxidation occurred during EUV irradiation in an atmosphere where water vapor of 1.3e-5 Pa was introduced into a clean vacuum. On the other hand, it has been observed that oxidation was suppressed in an atmosphere with high hydrocarbon content. Therefore, long time durability of Ru capping layer for oxidation by introducing ethanol into clean vacuum was investigated in this study.

The ultimate vacuum pressure of an experimental chamber was 2e-7 Pa. Water vapor was introduced up to 1.3e-5 Pa in EUV irradiation. Ethanol was additionally introduced up to 2.5e-6 Pa. Synchrotron radiation (SR) selecting EUV was used for irradiation by using a long undulator (LU) at NewSUBARU. The central irradiation power was 145-170 mW/mm2. Dose dependence of reflectance change was measured until the EUV dose of 6000 J/mm2. An EUV mean power of 0.18 mW/mm2 for PO mirrors was proposed by S. Bajt et al. for the maximum of plasma EUV source. Therefore, 6000 J/mm2 was equivalent to about 1 year of maximum mean power in actual tools.

Reflectance changes at different irradiation power densities of 145-170, 73-85, and 13-15 mW/mm2 measured using distribution of beam intensity are shown in Fig. 1. The reflectance changes quickly increased 1% first and decreased to initial value. After that, reflectance was kept at initial value until final dose. Reflectance changes taken at different irradiation power were synchronized. Therefore, we think that dose dependence of reflectance change was little dependent on EUV power density because reflectance change may be interpreted by a systematic error. The reflectance degradation was suppressed by introducing ethanol in any case.

We would like to discuss about difference between plasma and SR EUV sources. We think that ethanol molecules on a mirror surface block oxidation, which is generated from water molecules arriving and remaining on the mirror surface, during EUV irradiation. Incident power plays important role in this situation. Therefore, a comparison between incident powers of plasma and SR sources has been performed. In the case of plasma source, the repetition frequency may be 10 kHz, the pulse duration be 10 ns and the ratio of exposure time in whole operation time, which includes alignment, stage overhead, etc, be 1/4. In this case, the mean power of 0.18 mW/mm2 equals the incident power of 7.2 W/mm2. In the case of LU, the repetition frequency was 500 MHz and the pulse duration was 33 ps. The mean power of 145-170 mW/mm2 of LU equaled the incident power of 8.8-10 W/mm2. Therefore, the measurement using LU properly imitated that of actual tools. In other words, an acceleration test was performed according to the ratio of mean powers of LU. In conclusion, it was found that introducing ethanol can suppress reflectance degradation, which occurred from oxidation, at least for 1 year in actual tools.

This work was performed as a research program of METI, Japan, and managed by NEDO.

6517-112, Poster Session

High-accuracy EUV reflectometer

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Developers and users of EUV-optics need precise tools for the characterization of their products. Often a measurement accuracy of 0.1% or better is desired to detect and study slow-acting aging effect or contamination by organic contaminants.

To achieve a measurement accuracy of 0.1% a EUV-source is required which provides an excellent long-time stability, namely power stability, spatial stability and spectral stability. Naturally, it should be free of debris.

A EUV-source particularly suitable for this task is an advanced electron-based microfocus EUV-tube. This EUV source provides an output of up to 300 μW at 13.5 nm. Reflectometers benefit from the excellent long-time stability of tool.

We design and set up different reflectometers using EUV-tubes for the precise characterisation of EUV-optics, such as debris samples, filters, multilayer mirrors, grazing incidence optics and masks. Reflectivity measurements from grazing incidence to nearly normal incidence as well as transmission studies were realised at a precision of down to 0.1%.

The reflectometers are computer-controlled and allow varying and scanning all important parameters online. The concepts of the reflectometers are discussed and recent results are presented.

The devices can be purchased from the Laser Zentrum Hannover e.V.

6517-113, Poster Session

Development of optical component for EUV phase-shift microscope

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Extreme ultraviolet lithography (EUVL) technology has been paid attention as a next generation lithography technology. In the technology, defect-free mask is one of the critical issues. And, moreover, due to the existence of the multilayer, the phase defect in it's multilayer has induced the other inspection problems. Several research groups have been developed the phase-defect inspection technology since 2004 year. One of the disadvantage of these systems is that the verification of the height of the phase defect has to be followed using thickness measurement systems, like AFM, after it's inspection and the measurable pattern size is limited due to the AFM's spatial resolution.

In our research group, a EUV phase-shift microscope has been developed for an actinic mask inspection to help to making defect-free multilayer mask. This microscope consists of Schwarzchild optics and X-ray zooming tube. And To get the quantitative phase information of the phase defect a Mirau interferometer was installed in it. To realize the Mirau interferometer, we have developed the x-ray beam splitter, which is critical component in the Mirau interferometer in the research. The beam splitter divides beams divided into two parts, transmission and reflection parts. The reflected beam goes to the reference mirror and it can be a reference beam. Once again by the beam splitter two beams, reference beam and beam coming from sample after transmission at the beam splitter, can be combine to make an interference image.

In this report, we describe the production condition of beam splitter of the membranous structure and present obtained the result of the beam splitter with 10 MPa tensile stress.

6517-116, Poster Session

Fabrication of fine pitch gratings by holography, electron-beam lithography, and nano-imprint lithography

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Fine pitch gratings (200 nm -240 nm) are required for many technologies such as optical filters, semiconductor lasers and sensors for bio-medical devices. Various lithographic techniques are commercially available for fabricating gratings and depend on the type of grating required, cost and volume of manufacture. High resolution projection steppers common to silicon device manufacturing are capable, but have a prohibitive cost of ownership for much smaller volume manufacturing of photonic devices. The remaining techniques are holography, electron beam lithography and nano-imprint lithography.

In this paper we compare methods for manufacturing fine pitch gratings using holography, electron beam lithography and nano-imprint lithography. Holography has traditionally been used as a cost effective method for providing fine pitch periodic perturbations using a UV laser, beam splitter and angled mirrors to produce the grating interference pattern. It is fast and can be easily applied to a sample of large area but is limited to uniform gratings with the same pitch and no phase jumps (figure 1). Electron beam lithography offers additional flexibility over holography, for example, in the fabrication of gratings which require incremental changes in period (chirped), and phase shifted gratings such as for certain types of distributed feedback laser where spectral mode control of the device is required (figure 2). Although electron beam lithography is much more flexible, the serial exposure makes throughput much lower for densely packed devices, and the patterning cost per wafer much higher. Nano-imprint lithography is a novel printing technique and rapidly expanding technology which is being seen as a cost effective alternative for higher throughput. Nano-imprinting requires a template which is first patterned using electron beam lithography. The template can be used many times (for multiple fields per wafer and on multiple wafers) to imprint the gratings (figure 3) and therefore maintains the advantages of electron beam lithography while providing a higher throughput.

We have conducted a series of experiments to study and characterize lithographic processes used to fabricate fine pitch gratings. For each technique we look at the critical factors influencing grating resolution, pitch accuracy and control of duty cycle.

6517-117, Poster Session

Three-dimensional x-ray lithography using a silicon mask with inclined absorbers

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We are developing a mask for an X-ray lithography that applies the silicon on insulator (SOI) wafer and the MEMS technology. We have already succeeded in fabrication of the X-ray mask with vertical X-rays absorber by the Bosch process. On the other hand, silicon can be diagonally etched by optimizing the etching condition in a taper reactive-ion-etching (RIE) technique. We thought X-ray absorbers of an X-ray mask were processed to three-dimensional shape, and a gray mask for an X-ray lithography was fabricated by using the taper RIE technique. An X-ray mask was fabricated by the MEMS technology according to the following procedures. A SOI wafer which the SiO2 film in the thickness of 1 um is placed between Si of thickness 30 um and 525 um was prepared. After patterning by photolithography, a deep-RIE etching system was used. Si was etched in SF6/C4F8/O2 mixed gas at the pressure of 9.5 Pa. Next, a window was patterned by the photolithography on the back side of the wafer, and the back side Si in the thickness of 525 um was etched using same etcher. The SiO2 layer was etched by buffered HF. At the last, the photoresist was removed by organic solvents and O2 plasma ashing. The X-ray absorber of a normal X-ray mask has vertical sidewalls. However, sidewalls of an X-ray gray mask were inclined at the angle of 61 degrees. Especially, the cross-sectional shape of X-ray absorber is a triangle for the line width 20 um. In the taper RIE, the pressure control in the process chamber was very important to control the inclined angle of the Si structure?fs sidewall. This mask and a resist were fixed in gapless on the exposure stage of BL-4 in the synchrotron radiation facility TERAS of AIST with which the He gas of 1 atm was filled. The operation energy of TERAS was 750 MeV and the maximum storage ring current was 250 mA. X-rays generated from the bending magnet penetrated the Be window of 50 um thickness and the X-ray mask, and were irradiated to a PMMA resist of 1 mm thickness. The total dose energy was 150 mAh and development was performed at the room temperature for 16 h using a GG developer. We experimented on the X-ray lithography by using each silicon X-ray mask, and cross-sectional shape of PMMA resist structures were observed by SEM. When the normal X-ray mask was used, resist structures were vertical. However, sidewalls in the upper part of the PMMA resist structure were inclined and rounded when the X-ray gray mask was used. Especially, the shape of the PMMA resist structure of the line width 20 um was able to be processed to shape like the target. Thus, the effectiveness of the gray mask that adjusted the thickness of absorber was confirmed even by the X-ray lithography. We succeeded without the scanning and the rotation of the exposure stage in fabrication of such three-dimensional resist structures by only one X-ray exposure.

6517-118, Poster Session

Photon sieve array x-ray maskless nanolithography

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It is difficult to use a traditional refractive lens to focus X-rays, because of the strong absorption of solid materials in this spectral region. However, photon sieve, which is a novel diffractive optical element consisting of a large number of precisely positioned holes distributed over a flat surface, can be used to the focusing and imaging of X-rays. Photon sieve compared with traditional Fresnel zone plate can suppress sidelobes and thus increase space resolution as well as decrease the limit of lithography technology. Photon sieve can be integrated as a part of MOEMS to improve the efficiency and lower the cost. This new kind of MOEMS can be widely applied to martial, industrial, civilian and other fields. The development of photon sieve technology can benefit the studies on X-rays diagnose technology, photon crystal device, nanoelectronic device, etc. Photon Sieve Array X-ray Maskless Nanolithography (PSAXMNL) presented in this paper is a novel approach to providing low-cost, improved resolution and highly flexible lithography. PSAXMNL will be promising in research, development, design verification, mask making tool for direct writing and applications of nano-patterning. It employs an array of photon sieves as diffractive optical lenses to focus incident collimated X-ray into an array of spots on a substrate coated resist. The X-ray incident on each photon sieve is modulated by means of an upstream spatial light multiplexer, while the substrate is scanned underneath. Hence patterns of arbitrary geometry are written in a dot matrix fashion. Since a large number of focused X-ray beams are writing simultaneously, PSAMNL can achieve practical writing speeds. Standard semiconductor processing tools, such as laser-beam direct writing lithography, e-beam lithography, X-ray lithography and electroplating, can be employed in the processes to fabricate photon sieve array. High-numerical-aperture photon sieve array can be reliably fabricated with planar fabrication processes. Focal characteristics are ensured uniform across the array by these processes. We numerically analyzed the feasibility of PSAXMNL and its potential for the fabrication of novel devices. The related contents include the Discrete Fast Fourier Transform algorithm for the diffracted field of single photon sieve according to Fresnel-Kirchhoff diffraction theory, such as point spread function, and the approaches to enhancement resolution, such as the suppression of sidelobes, the suppression of higher order foci, the construction of a specific focal spot shape, the equivalent pupil function theory, the diffraction efficiency and the physical limit of the resolution. Apodization was investigated as a means of enhancing resolution in PSAXMNL. The results of apodization simulation by means of MATLAB were shown that PSAXMNL is capable of high-quality lithography at high resolution. However, photon sieves array is diffractive optics elements modulating amplitude and thus suffers from dispersion and low diffraction

efficiency. We are exploring two useful solutions to overcome these defects in the next research. On one hand, diffractive and refractive lens combination may be employed to compensate focusing or imaging quality for the dispersion. On the other hand, phase photon sieve array technology and surface plasmon polaritons technology may be used to improve the diffraction efficiency.

6517-119, Poster Session

Micro-scale magneto-polymer boomerangs fabricated using soft lithography

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Polymeric particles containing magnetite have been used for years in many different applications including, but not limited to, separations, magnetic resonance imaging, hyperthermia treatment, and drug delivery. Until now, such composite particles have been synthesized using techniques such as emulsion polymerization, liposomal encapsulation, and self-assembled monolayer processes. A novel approach utilizing soft lithography was used here that greatly increases control over the final composition and structure of the particle. This technique employs a perfluorinated polyether (PFPE) elastomer in an imprint lithography process, known as Particle Replication In Non-wetting Templates (PRINT). During this process, a master template, patterned SU-8 photoresist on a silicon wafer, was used to pattern the PFPE mold. The PFPE mold dictated the ultimate shape and size of the particle. A monomer solution containing a dispersion of magnetite was evenly distributed over the patterned PFPE surface. Once cured photochemically, isolated particles can be harvested using a sacrificial adhesive layer.

In this work, a crosslinked network of polyethylene glycol (PEG) methacrylate (MW 1000 g/mol) and PEG trimethacrylate (MW 428 g/mol) containing 15 wt% aqueous ferrofluid was photochemically cured within the cavities of a PFPE mold that was patterned in the shape of boomerangs 10 microns long and 4 microns wide. Magnetic materials were trapped in desired locations of the PRINT boomerang particles by applying a strong magnetic field using a rare earth magnet. After applying the field samples were cure photochemically. Four different samples were prepared in which magnetite was trapped in various locations throughout the particles. When a magnetic field was applied to a viscous solution, the particles were observed to move with magnetite side of the particle pointing in the direction of the applied field. Particles were characterized by microtome TEM, x-ray powder diffraction, SEM, and 3DFM microscopy.

6517-120, Poster Session

Simulating particle deposition rates during evaporation-driven self assembly

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Evaporation driven self-assembly (EDSA) of nanoparticles suspended in a drying solution is a key component in a number of applications. For example, the EDSA process is useful for directed selfassembly in maskless lithography, but EDSA is not well suited for applications where a uniform deposition of particles is required. As such, the ability to predict when and how evaporation driven flows will occur is a powerful tool for any fabrication process involving evaporation. When self-assembly is desired, the location and size of the fabricated nanostructures can be controlled by using the evaporation rate, the fluid properties, and the surface energy and geometry of the substrate (see Fig. 1). For example, non-uniform evaporation from the meniscus surface or lithographically defined features on the substrate can be used to control the pinning of the receding contact line in order to create ordered arrays of particles of arbitrary configuration at very small scales [1,2]. As EDSA is highly parallel it has the potential for high throughput. Well ordered arrays of nanoparticles may serve many different areas in the semiconductor industry, from information storage structures to semiconductor based light pathways for optical computing. Therefore, it is important to understand and model the governing physics behind the transport and assembly mechanisms. In general, EDSA processes can be broken into behaviors that occur in two regimes. At the macro-scale, the process is driven by the bulk transport of particles to the lithographically defined features. Particle organization and deposition occur at the micro- and nano-scale. The macro-scale process is driven by the fluid velocity that is generated by the evaporation from the surface of the solution and the process is governed by continuum fluid dynamics. Computational fluid dynamics (CFD) models of this process were developed in order to investigate the macro-scale processes that lead to directed selfassembly. These CFD models focus on the first phase of the process, which is responsible for the transport and concentration of nanoparticles at the lithographically defined features (see Fig. 2). An experimental technique was developed that allows for direct observation of bulk particle transport during self-assembly. This technique was successfully used to observe the self-assembly that occurs during the evaporation of a colloidal droplet (see Fig. 3), a process which has been well documented and is commonly referred to as the “coffee stain” phenomenon [3]. The first phase of the undirected self-assembly that leads to the formation of a high particle concentration ring was modeled using the developed CFD methodology and compared to experimental observation. The details of the evaporation driven flows that lead to the formation of the ring were adequately predicted using the CFD model. The modeling methodology developed in this work provides a powerful tool to understand evaporation driven self-assembly nanostructure fabrication.

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6517-121, Poster Session

Microfocus EUV tube for at-wavelength reflectometry

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The precise characterization, optimization, and quality control of multilayer mirrors, masks, and other optical components for EUV lithography is a critical issue on the way towards the realization of EUV lithography. Usually, the characterization of EUV optics is carried out at synchrotron facilities which is a very expensive and time consuming procedure. Therefore, compact, inexpensive, and easy-to-use tools and systems for a fast and reliable in-house at-wavelength reflecitivity control are needed.

In this presentation we will provide an update on our commercial compact microfocus EUV source for in-house at-wavelength metrology. This source, called EUV tube, is based on electron-induced characteristic emission from solid targets. The EUV tube is debris-free, has excellent long-term temporal and spatial stability, and very low running costs. All source parameters are computer-controlled and the source size can be adjusted down to 10 µm. Recent improvements on EUV power scaling will be presented. Different applications in the field of at-wavelength metrology will be highlighted. New results on EUV reflectometry of multilayer mirrors and grazing incidence optics will be demonstrated and compared with measurements obtained at synchrotron facilities and with plasma-based sources.

6517-122, Poster Session

CO2 laser and Sn-droplet target development for EUVL

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The development status of the two key technologies developed at EUVA for a HVM Laser Produced Plasma EUV light source will be presented in detail, i.e. the high-power RF-excited CO2 laser and the

Sn droplet target. Special emphasis is given on the target optimization for given laser parameters, e.g. repetition rate.

This work was supported by the New Energy and Industrial Technology Development Organization (NEDO), Japan.

6517-123, Poster Session

Characterization of various Sn targets with respect to debris and fast ion generation

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Sn is currently the target material of choice in the EUV community due to its high conversion efficiency. However, its main drawback is the generated debris that severely limits the lifetime of EUV (and other optical) components. Mass limitation of the Sn target is therefore necessary but not sufficient because the generated plasma has to be completely ionized in order to successfully apply magnetic mitigation.

Several Sn targets with different size and shape have been investigated with respect to the generated fast ions and debris using Faraday cups and quartz crystal microbalances. In addition, a magnetic field with a maximum field strength of 1.4T at the target position has been used to measure the mitigation. The laser used for these experiments was a TEA-CO2 laser.

This work was supported by the New Energy and Industrial Technology Development Organization (NEDO), Japan.

6517-124, Poster Session

Small field exposure tool (SFET) light source

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A small field exposure tool (SFET) has been built in Japan under the guidance of EUVA and Canon Inc. The light source of SFET has been developed at the EUVA Hiratsuka R&D center. The drive laser is a short-pulse, high-power KrF laser, developed by Gigaphoton Inc. and Komatsu Ltd., and the source target is a xenon jet. The light source and its characteristic performance will be presented in detail.

This work was supported by the New Energy and Industrial Technology Development Organization (NEDO), Japan.

6517-125, Poster Session

Debris characteristics from a colloidal microjet target containing tin dioxide nano-particles

S. Kubodera, S. Suetake, Y. Senba, A. Hosotani, Y. Takahashi, Univ. of Miyazaki (Japan); T. Higashiguchi, Utsunomiya Univ. (Japan)

We are developing a low-debris laser-produced plasma extreme ultraviolet (EUV) source by use of a colloidal microjet target, which contained low-concentration (6 wt%) tin-dioxide nanoparticles. The low concentration nature of the target reduced the absolute amount of debris, and we found out that the use of nano-particles regulated the condensation of particles and significantly decreased debris whose size was larger than microns. On the other hand, the low tin concentration, i.e. the low number of EUV emitters, was compensated and the conversion efficiency (CE) was improved by introducing double pulses of two Nd:YAG lasers operated at 532 and 1064 nm as a result of controlling of the micro-plasma characteristics. The EUV CE reached its maximum of 1.2% at the delay time of approximately 100 ns with the main laser intensiy of 2 x 1011 Wcm-2. The CE value was comparable to that of a tin bulk target, which, however, produced a significant amount of neutral debris. The use of low concentration nano-particles in a microjet target with a diameter of 50 microns decreased the neutral debris emission from a target, which was monitored by a silicon witness plate placed at several distances apart from the target in a vacuum chamber. The witness plate was analyzed by use of XPS. The XPS signals of tin atoms showed that the signal intensity increased linearly with the increase of the laser shot numbers. The signal intensity as a function of the distance from the microjet target was inversely proportional to the square of the distance. Both signal behaviors were easily understandable. An electrostatic energy analyzer (ESA) separated the tin and oxygen ions with an ion energy larger than 0.5 keV. We observed significant decrease of singly-ionized tin and oxygen ion signals when the double laser puses were used. The most probable energy of the singly-ionized tin ions also decreased from 9 to 3 keV. The oxygen ion energy was below the detection limit of the ESA. This decrease of the ion energy was attributed to the interaction between an expanding low-density pre-plasma and a main laser pulse. The decrease of the tin ion energy around 3 keV encouraged us using a magnetic field for ion mitigation.

6517-126, Poster Session

A model of a distributed EUV source for next-generation lithography tools

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The need for a highly scalable, low debris and long lifetime source of Extreme Ultraviolet (EUV) radiation has been well established in the previous years of this conference. Presented here is the basic concept of the STARFIRE distributed EUV radiation source which emits little to no debris, while at the same time achieving conversion efficiencies that can be optimized to approach the theoretical physical limit of ~1.6% of EUV from Xe in a 2% band centered at 13.5nm into 2π ster-radians. Modeling results will be presented that have been based on a variety of techniques including advanced magneto hydrodynamics calculations that utilize Prism Computational Science's HELIOS-CR, Particle-in-Cell simulations using OOPIC Pro, and finally ab initio calculations which encompass such aspects of optimized EUV collector geometry and circuit models. This array of simulations was used together to study the variation of parameters and of different aspects of the STARFIRE EUV source. The results of this parameter study suggest the optimum control conditions that will allow the STARFIRE EUV source to produce an array of high brightness and high stability EUV images to be used in a High Volume Manufacturing (HVM) tool.

6517-127, Poster Session

EUV and debris emission from laser-irradiated pure-tin droplet

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Tin droplet scheme is proposed to supply minimum mass target for EUV light source based on laser-produced plasmas. In the previous experiments with tin-droplet, tin-compound is contained in solvent, however solvent may be another source of EUV mirror contamination. We are performing the first demonstration of EUV generation from Nd:YAG laser-irradiated "pure-tin" droplet, which has been developed in University of Hyogo. For proving principle of droplet scheme, two issues should be addressed; (i) EUV conversion efficiency comparable to that from planar or jet targets, (ii) mitigation of debris generation compared to that from planar or jet targets. EUV-calorimeter calibrated with E-mon, Faraday cup charge collector, Thomson parabola ion analyzer. wetness plates are used for measuring EUV energy, ion debris, tin-deposition, respectively. This work is performed under the auspices of Leading Project promoted by MEXT (Japanese Ministry of Education, Culture, Sports, Science and Technology).

6517-128, Poster Session

Experimental results of an addressable xenon microdischarge EUV-source array for HVM lithography

B. E. Jurczyk, R. A. Stubbers, J. L. Rovey, M. D. Coventry, Starfire Industries LLC

The joint specification projected in-band EUV power requirements at the intermediate focus will rise beyond 185W 2%-bw to maintain the necessary 80-100WPH throughput for economic viability. New

improvements in photon efficiency and mask illumination are needed to reduce reflections and power demand, as well as improving source spatial uniformity.

In 2006, Starfire presented a novel approach to the EUV source-optic architecture using a high-brightness light source array for direct integration within the illumination optical system. Spatial uniformity and Kohler illumination across the entrance pupil is achieved by dividing the incident light into discrete bundles on a fly's eye mirror. These light bundles form a secondary source image plane that is projected onto the pupil of the projection optics. This configuration allows electronic adjustment of partial coherence and depth of focus for improved lithographic contrast and resolving capability. By distributing total EUV power across discrete units, thermal and particle loadings become manageable without the need for exotic materials or cooling schemes, and sources of contaminating debris are reduced.

Experimental data from a 5x5 xenon-fed microdischarge source array is presented, demonstrating repetition rate and source addressability for illumination patterning and grayscaling capability. In addition, experimental data from xenon-based sources will be presented with a suite of plasma and optical diagnostic instruments, including conversion efficiency, spectral purity and debris generation. Projections for scaling to HVM conditions will also be presented.

6517-129, Poster Session

XUV spectroscopy of mass-limited Sn-doped laser micro-plasmas

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Efficient 13.5 nm emission from high repetition rate, mass-limited tin-doped droplet laser plasma source scheme was proposed by UCF for extreme ultraviolet lithography (EUVL), utilizing Mo/Si multilayer mirror(MLM) reflective optics. Tin content limited to what is required for high conversion, small droplet diameter, and complete ionization of the target with laser irradiation, leads to reduced debris production required for preserving source lifetime. Conversion efficiency of 2.25% was obtained with this target, recently[1]. Effective, low cost mitigation schemes that can be integrated with realtive ease into the source configuration have also been demonstrated[2]. Detailed characterization of the flux at the collector mirrors was completed. We assess the spectral purity in terms of the energy of emission in the entire region and compare to the inband energy for this tin-doped droplet laser plasma source. This will complete the characterization of radiation from the tin-doped droplet plasmas for EUVL.

A combined experimental and theoretical program is employed in order to measure and interpret emission spectra from laser plasmas. The unresolved transition array (UTA) of tin observed in spectral measurements at 13.0 nm is identified as resulting from large numbers of transitions produced by Sn(7+) - Sn(12+) ions at plasma temperatures of approximately 30 eV. Measurements as well as calculations show that 30 eV can be produced with laser irradiance intensity near 10e11 W/cm2. Term structure calculations of 4dw electron configurations for these ions have been completed, with strongest lines producing transitions into 13.0 nm region coming from 4d(n)-4p(5) 4d(n+1) and 4d(n)-4p(n-1) 4f(1) [3].

Mo/Si MLMs produce highest reflectivity at 13.5 nm, but it is also highly reflective in the region from \>50 nm - 400 nm. Spectral purity is a requirement for a viable EUV source, since this out-of-band radiation (\> 50 nm) will cause flare, affecting the image fidelity at the wafer. IR radiation pose possible threats to first collector mirror due to heating. Thus detailed metrology measurements of the broadband emission from this source is needed. Characterizations of this emission in the off-band EUV has been completed [4]. Preliminary measurements of visible and IR regions indicate levels within the required limits for the tin-doped droplet plasma. Calibrated high resolution spectral data obtained using flat-field spectrometer in the XUV and UV region from this source will be presented. Assessment of energy of emission in this region and comparison to the inband power will be made for the tin-doped droplet laser plasma source in this region. All measurements will be conducted at optimum plasma temperature for 13.5 nm emission from tin. Comparison of the spectral characteristics to theoretical emission spectrum obtained for the same experimental conditions will be presented.

1.C-S Koay. PhD thesis: Radiation Studies of the Tin-doped microscopic Droplet Laser Plasma Light Source Specific to EUV Lithography. University of Central Florida, 2006.

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6517-130, Poster Session

High-power/high-repetition-rate laser-produced tin-doped micro-plasma source for EUVL

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There has been considerable improvement in EUV technology over the last few years resulting in the development of micro-exposure tools (for metrology, resist development or similar). However, significant technological challenges remain on the journey towards developing a high volume manufacturing tool. One of the main challenges that still is needs to be to developed is an EUV-source capable of providing in-band powers in excess of 115 W at the intermediate focus.

In this work, considerable progress achieved in developing a high-repetition rate/high-power EUV-source based on the mass-limited Sn-doped droplet target concept, is presented. Sn-doped fluid injected into vacuum at 25 m/s is producing equidistant 35 micron spheres. Therefore, the small source size allows large collection angles while easily meeting the maximum etendue requirements.

Furthermore, the mass-limited target concept is applied with only as many radiating species in the micro-target as we need to obtain high conversion efficiencies [1], while keeping debris and out of band radiation at a minimum. This is highly advantageous in ccomparison to discharge-plasmas, where the tin-consumption and consequently debris-issues are by far more challenging. To avoid collector mirror degradation from debris and to guarantee long collector mirror lifetimes, several independent mitigation schemes are used in combination. Measurements taken with a low-repetition rate laser with solid tin were very promising and proved the feasibility of our approach [2]. Additional results regarding debris measurements with high-power/high repetition rate lasers on our droplet target will be presented.

We already have shown continuous long-term operation (30 kHz) and stability of the target delivery system elsewhere [3]. Deploying a 3D-machine vision computer-controlled positioning system, the position of the droplet is continually adjusted in respect to the incident laser. Using this 3D-imaging feedback system, excellent position stability was demonstrated over a time span of several days. Furthermore, because of operation at high repetition rates, the source is capable of providing high dose control which is desired for EUVL.

Results from experiments performed with a high-power (1 kW)/high repetition-rate (3-4 kHz) Q-switched Nd:YAG laser and a high power fiber laser (200W) synchronized with our droplet delivery system will be presented. A flat-field spectrograph is used to record time-integrated EUV spectra at an angle of 26° degrees measured relative to the incident laser. For absolute energy measurements a precision EUV energy-meter was developed and cross-calibrated with the EUV energy-meter flying circus II. To ensure absolute equal radiation conditions for spectral acquisition and absolute energy measurements, both instruments are mounted at the same relative angle compared to the incident laser.

A calibrated EUV-photodiode at the intermediate focus is used to determine the EUV-power.

To compare the status of our source concept with discharge sources, we use an array of multilayer-mirrors at realistic plasma-mirror distance to collect EUV light in the intermediate focus. Also, we can deduce the in-band power at the intermediate focus with the angular dependence of the measured in-band emission and known reflectivity of a full-size (2pi) Si/Mo multilayer mirror.

We expect to report the achievement of significant power milestones with a high-repetition rate Nd:YAG laser as well as a high power fiber laser.

1. “High conversion efficiency microscopic tin-doped droplet target laser-plasma source for EUVL”, Chiew-Seng Koay, Simi A. George, Kazutoshi Takenoshita, Robert Bernath, Etsuo Fujiwara, Martin C. Richardson, Vivek Bakshi, Proceedings of SPIE, volume 5751, 2005.

2. “Debris mitigation for high-NA laser plasma EUV sources”, Tobias Schmid, Kazutoshi Takenoshita, Chiew-Seng Koay, Simi George, Somsak Teerawattansook, Martin Richardson, SPIE Microlithography, 2006

3. “The LPL tin-doped micro-droplet laser-plasma EUV source”, Martin C. Richardson, EUV Source Workshop 2006, Vancouver, Canada

6517-131, Poster Session

Laser-produced plasma source system development

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This paper describes the development of laser produced plasma (LPP) technology as an EUV source for advanced scanner lithography applications in high volume manufacturing. EUV lithography is expected to succeed 193nm immersion technology for critical layer patterning below 32nm in 2009. The paper describes the development status of subsystems most critical to the performance to meet joint scanner manufacturer requirements and semiconductor industry standards for reliability and economic targets for cost of ownership.

The intensity and power of the drive laser are critical parameters in the development of extreme ultraviolet LPP lithography sources. The conversion efficiency (CE) of laser light into EUV light is strongly dependent on the intensity of the laser at the interaction point of the laser and the target material. The total EUV light generated then scales directly with the total power incident of the laser. In this poster, we report the progress on the development of a short pulse, high power CO2 laser for EUV applications.

The lifetime of the collector mirror is a critical parameter in the development of extreme ultra-violet LPP lithography sources. Deposition of target material and contaminants as well as sputtering and implantation of incident particles can reduce the reflectivity of the mirror coating substantially over time during exposure even though debris mitigation schemes are being employed. We report on progress during exposure measurements and test experiments with a 320mm diameter ellipsoidal collector mirror using a high-repetition-rate laser-produced plasma EUV light source.

Droplet generation is a key element of the Laser Produced Plasma Extreme Ultra-Violet (LPP EUV) source being developed at Cymer Inc. for EUV Lithography applications. The main purpose of this device is to deliver small quantities of liquid target material (droplets) to the focused spot of a high power pulsed laser. The EUV light in such configuration is obtained as a result of creating highly ionized plasma from the material of the droplets. Liquid tin or lithium are examples of materials that can be used as target materials due to the relatively high conversion efficiency of the pump laser energy into EUV emission in these metals. In this paper we discuss the most recent results obtained with the droplet generator and describe the requirements and technical challenges related to successful implementation of this device.

Additionally, developmental status of other critical subsystems for LPP EUV sources may be reported.

6517-132, Poster Session

Gibbsian segregating alloys: a potential solution to minimize collector degradation

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A critical issue for EUVL is the minimization of collector degradation from intense plasma erosion and debris deposition. Collector optic reflectivity and lifetime is heavily dependent on surface chemistry interactions between fuels and various mirror materials in addition to high-energy ion and neutral particle erosion effects. An innovative Gibbsian segregation (GS) concept has been developed for being a self-healing collector optic. A Mo-Au GS alloy has been developed on silicon using a DC dual-magnetron co-sputtering system in order for enhanced surface roughness properties, erosion resistance, and self-healing characteristics to improve collector lifetime. A thin Au segregated layer is maintained through segregation during exposure, even though overall erosion is taking place. When looking at pre- and post- exposure analysis of a GS Mo-0.56%Au alloy at 20o grazing incidence and 28 cm away from the plasma pinch after 2.2 million shots from a SnCl4-fueled DPP, it was seen that the while the surface roughness went from 1.8 to 7.9 + 0.5 nm, there were actually islands formed on the surface with surrounding areas to be very smooth. These islands were from contamination in the system and not from the ion impact damage as the bulk concentration of Au in Mo-Au alloy is ~ 0.56%, while ~ 40% Au was found at the film surface even after being eroded by ~ 20 nm. This illustrates that Au is segregating to the surface faster than it is being eroded. The reflective material Mo underneath the segregated layer was protected by this sacrificial layer. This phenomenon is useful in the design of a collector optics surface and provides insight into plasma-facing optics lifetime as high volume manufacturing tool conditions are approached. The two dominant driving forces, thermal and ion flux gradient are focused in this work. Both theoretical and experimental efforts were undertaken in this study to prove the effectiveness of the GS alloy used as EUV collection optics, and the underlying physics behind it with respect to the segregation diffusion, surface balance, and erosion will be investigated both qualitatively and quantitatively. Xe fuel will be used in the future EUV exposures to investigate the GS performance in order to avoid the contamination issue of Sn-fueled EUV source. This work developed a theoretical model to predict erosion and the GS process during EUV exposure in a DPP environment.

6517-133, Poster Session

Debris mitigation techniques for a Sn- and Xe-fueled EUV-light source

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An extreme ultraviolet light (EUV) source is investigated at the University of Illinois to characterize debris ejection and evaluate the efficacy of various mitigation techniques. This work is intended to determine best methods for enhancing the lifetime of optical components inside the vacuum system of a commercial lithography tool. The source used is an XTREME Technologies XTS 13-35 capable of producing 35W of EUV light from a z-pinch plasma by utilizing either Sn or Xe fuels. As the plasma compresses, high energy photons in the extreme ultraviolet range are released. In an exposure tool, this EUV light would be collected using highly specialized mirror optics and routed for use in nanolithography. This light emission is accompanied by the ejection of electrons and multiply charged ions which can significantly damage the nearby mirror surfaces through erosion and deposition mechanisms. Gaseous metal fuels like Sn also present the complication of surface condensation which can have an equal or greater effect on the overall reflectivity of the optical array. Characterization of the ejecta is performed with an electrostatic spherical sector energy analyzer (ESA) that identifies ion species by energy-to-charge ratio using ion time of flight (ITOF) analysis. For characterization of neutrally charged species, a microchannel plate is placed in direct line-of-sight with the source and a high voltage electric field is used to divert ions and electrons from impact. These two methods are used to quickly evaluate various experimental debris mitigation schemes by monitoring the output

intensity of the ion and neutral ejecta. Sample exposures and witness plates are used to explore the effect of debris mitigation on optics lifetime. An RF plasma is placed between the pinch and the collector area to explore the possibility of improved ion mitigation through coulomb-enhanced scattering. Interesting results are obtained which could actually help to remove the flaking from near electrode areas and also a reduction in the main ion signal is noticed. A pulsed foil trap is introduced to explore the prospect of further advanced ion diversion through pulsed, high-voltage electric fields. These techniques are evaluated both independently and in conjunction for xenon and tin fuels. Comparisons are also made between the general debris spectra of Sn- and Xe- fueled pinch plasmas. Both spectra show that singly- and doubly-charged fuel ions are the dominant species, with Xe+ and Sn+ peak measured fluxes of 4100±398 and 7600±737 ions/eV•cm2•pinch, respectively, though Xe+ ions are seen in a greater abundance at higher energies. The Xe+2 and Sn+2 spectra differ, however. While they share a similar shape, the latter is observed at an approximately 200 times reduced magnitude.

6517-134, Poster Session

Comparison of optical performances of alternative grazing incidence collector designs for EUV lithography

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One of the main drivers for the optical design of collectors for Extreme Ultra-Violet (EUV) lithography for high volume manufacturing tools is the requirement of increasing the solid angle collection efficiency and the optical transmission of the optics in order to comply with the more recent specification of 180 W set for the in-band radiation at 13.5 nm at the intermediate focus [1]. In addition, the improvement of the collector efficiency has benefits in relaxing the requirement for the power emitted by the source, in reducing the thermal load on the collector itself and increasing its lifetime.

At present, the collector optical configuration of choice, in particular for Discharge-Produced Plasma (DPP) sources, is based on grazing incidence type I Wolter design [2]. For lithographic applications, the design needs to be optimized to match the source and illuminator specifications while assuring manufacturability and maximizing optical performances in terms of collection efficiency and far field intensity uniformity.

In the type I Wolter design, each ray experiences two reflections, and consequently the overall reflectivity is given by the product of the reflectivity of each of the two reflections. It is easy to show that the overall reflectivity is maximised when the two grazing incidence angles, and thus the reflectivity of the two reflections, are equal [3], at least for the kind of dependence of reflectivity on the grazing incidence angle of commonly used coating materials, like Ruthenium. This condition can not be satisfied for all rays in a type I Wolter design. Indeed, for each mirror, the two grazing incidence angles can be made equal for one ray at most. A new design has recently been proposed [4] for grazing incidence collectors, in which the above condition on the two reflection angles is satisfied for all rays collected by each mirror and the collection efficiency is of the order of 20%, or more, greater than what is achievable with type I Wolter collectors.

In addition, a second new design for grazing incidence collectors is currently under investigation with the aim of increasing the flexibility with which the optical design can be tailored to the boundary conditions set by the source, the debris mitigation tool, and the illuminator. The increased number of degrees of freedom also allows an improvement of the collection efficiency of the order of 5-10% with respect to type I Wolter design.

The new design concepts will be presented in details and discussed and their optical performance in terms of collection efficiency and far field intensity distribution will be compared to those obtained with a type I Wolter collectors.

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6517-135, Poster Session

Optimization of 13.5-nm conversion efficiencies from laser-produced tin plasmas for EUV lithography

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Tin-based laser-produced plasmas (LPPs) are attractive candidates as extreme ultraviolet (EUV) light sources for EUV lithography. The accurate simulation of the dynamics and spectral properties of plasmas created in EUVL radiation source experiments plays a crucial role in analyzing and interpreting experimental measurements, and in optimizing the 13.5 nm radiation from the plasma source. Using a suite of radiation-hydrodynamics, plasma spectroscopy, and atomic physics codes, we are developing new techniques for producing high conversion efficiency tin-based LPP sources at several laser wavelengths.

In our studies, we employ 1-D and 2-D radiation-hydrodynamics codes to simulate the dynamic evolution of LPPs. The results of radiation-hydrodynamics simulations can be post-processed using SPECT3D to generate images and spectra that can be compared directly with experimental measurements. Both the radiation-hydrodynamics and spectral codes utilize atomic physics databases based on a suite of well-tested atomic structure codes. Previous simulation results for Li and Sn LPPs have been shown to be in very good agreement with experimental measurements [1].

In addition to the above, we have set up optimization algorithms that allow a broad range of parameter space (e.g., laser intensities and pulse shapes) to be very efficiently searched. We will discuss the major features of these simulation tools, and present example results of simulations of tin-based EUV radiation sources.

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6517-136, Poster Session

Characterization of the Tin-doped droplet laser plasma EUVL sources for HVM

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EUVL sources are required to satisfy the stepper manufacturers’ specifications on source power, source lifetime, source ettendue, power stability and source spectral purity.

We have previously reported many characteristics of tin-doped droplet target for EUVL source, such as the high conversion efficiency (CE) [1], the small out-of-band radiation [2], and the limited ion emission [3]. We address and demonstrate in this paper the primary issues associated with long-term high power EUV sources for high volume manufacturing (HVM) using tin-doped droplet target.

The tin target is shown to produce the highest CE for interaction with one micron laser irradiation wavelength where commercial laser systems with this wavelength output can be applied. High power EUV generation is demonstrated using high repetition rate (HRR) laser system synchronized with target delivery which is stabilized with advanced feedback schemes. We have currently two options for the HRR laser, diode pumped solid state laser (DPSSL) and diode pumped fiber laser (DPFL). The HRR laser can be temporally and spatially multiplexed so that it is possible to generate even higher EUV power.

The tin-doped droplet target is capable of being driven up to the same or higher frequency to match any laser repetition rate. The EUV power stability, therefore, the dose stability is higher than that of the minimum frequency specified by the source requirements.

We can tolerate the penalty of operating at high frequencies, which is the increased amount of tin ion emission. The tin-doped droplet target is a mass-limited target [4] with all of the tin atoms are ionized and contributing to the useful EUV radiation. Any tin ions generated during irradiation is captured by effective ion mitigation schemes, [5] before they reach the first collector mirror. We have conducted the mirror lifetime estimation scaling with the ion kinetic energy distributions at the mirror distance and have calculated surface sputtering yield of Si and Mo. The estimated mirror lifetime is within the requirements even at increased operation frequencies when the ion mitigation schemes that we have developed are applied.

We also present the radiation characteristics of the tin-doped droplet plasmas in terms of the spectral purity. Only a limited number of photons from the out-of-band radiation emission from the tin-doped droplet EUVL source propagate through the stepper optics to wafer and beyond. The source size is about 100 microns in diameter [6] which is well below the source etendue limit. Therefore, tin-doped droplet target is shown to satisfy all of the source requirements.

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6517-137, Poster Session

LPP EUV source by minimum mass tin targets

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Minimum mass target is a key technology to protect the collection mirror from contamination problem in the EUV source by a laser-produced tin plasma. We have measured EUV emission and ion energy spectra for the low density foam targets of tin-oxide with different initial mass density and the tin-layer coated targets with different coating thickness. With reducing the initial mass density and the coating thickness (the number of tin atoms) it was found that the maximum ion enrgy emitted from plasma decreases drastically while keeping EUV intensity. From these results, mimimum number of tin atoms required for high power EUV source target was evaluated.

We have been developing several kinds of novel targets with minimum mass, such as punch-out-target, tin droplet target and tin-coated droplet target. In the punch-out target, a thin tin layer is overcoated on a substrate transparent for a laser pulse. A puncher laser illuminates the tin layer from the substrate side to push out the tin layer. The intensity of puncher laser is so weak that the punched out tin layer is still in solid, but flies at a velocity of ~ 1 km/s. The flying target is heated by a drive laser to generate EUV emission. The feasibility experiments of punch-out target have been performed, and rather high conversion efficiency and drastic reduction in ion number and ion energy, compared with those from solid tin targets, were demonstrated. Experimental results on tin droplet target will be also presented.

This work was performed under the auspices of Leading Project promoted by MEXT, Japan.

6517-138, Poster Session

A mass-limited Sn target irradiated by dual laser pulses for an EUVL source

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One of the most critical issues in development of extreme ultraviolet lithography (EUVL) is to develop a powerful, clean, long life-time, and efficient EUV light source. Laser-produced Sn plasma shows the highest conversion efficiency (CE) from laser to in-band (2% bandwidth) 13.5 nm EUV light. However, in order to apply Sn material to high volume manufacture (HVM), debris becomes a critical issue. Various kinds of targets with low concentration of Sn have been widely investigated to mitigate the debris related with the Sn plasma, including Sn-doped water droplet, Sn-doped foam, and low density SnO2 etc. However, these targets introduce extra O, H, and C particles, which are also critical for collector optics used in EUVL source.

We present the efforts to mitigate debris from laser-produced Sn plasma by introducing a low energy pre-pulse while keeping high CE. The basic idea is to separate the processes of the generations of the plasma and the 13.5 nm EUV light. A low energy pre-pulse is introduced to generate a pre-plume, another pumping pulse heats up the pre-plume to the favorite temperature for efficient 13.5 nm EUV light. Much lower ion energy and nearly the same CE were simultaneously observed from the plasma driven by a dual-pulse as compared with that driven by a single pulse.

Thin Sn coating was investigated as a mass-limited target. A typical result obtained with a 30 nm Sn film is shown in Fig.1. It is seen that higher ion energy always accompanied with mass-limited target is efficiently controlled under 100eV by introducing a low energy pre-pulse using. While almost the same CE was obtained as compared with that obtained with a single pulse and a massive target. It is also noted that less gas is required to mitigate ions with lower energy when dual pulses are used.

These researches enable an efficient, clean, and high-speed mass-limited target supply based on pure Sn for HVM EUVL source. Its scheme will be discussed.

Fig.1 Time of flight of ions from laser-produced Sn-plasma irradiated by a single or dual pulses in ambient Ar gas with various pressures.

Conference 6518: Metrology, Inspection, and Process Control for Microlithography XXI

Monday-Thursday 26 February-1 March 2007

Part of Proceedings of SPIE Vol. 6518 Metrology, Inspection, and Process Control for Microlithography XXI

6518-01, Session 1

Metrology challenges of double exposure/double patterning

W. H. Arnold, ASML Netherlands B.V.

No abstract available

6518-02, Session 2

Process monitor gratings

T. A. Brunner, IBM Thomas J. Watson Research Ctr.; C. P. Ausschnitt, IBM Microelectronics Div.

Despite the best efforts of lithography design-for-manufacturing to maximize the process window of chip features, process windows shrink with decreasing nominal dimensions. Controlling the manufacturing process within these shrinking windows requires monitor structures designed to maximize both sensitivity and robustness. In particular, monitor structures must exhibit a large, measurable response to dose and focus changes over the entire range of dose and defocus that comprise the chip-feature process window.

We describe an approach to the design and implementation of process monitor grating (PMG) structures tailored to lithography and measurement capability. In the design we use sub-resolution assist features (SRAFs) to degrade the lithographic imaging (for enhanced dose and focus sensitivity), and to maximize both the grating pitch and the printed dimensions of the grating elements (for enhanced robustness and measurability). The specific SRAF dimensions are uniquely determined by the lithographic capability and the desired grating duty cycle.

We apply the scatterometric measurement of PMGs to the characterization and on-product control of 65nm and 45nm manufacturing processes.

6518-03, Session 2

Lithography equipment control using scatterometry metrology and semi-physical modeling

K. R. Lensing, J. P. Cain, A. Prabhu, A. Vaid, R. Chong, B. Singh, Advanced Micro Devices, Inc.; E. M. Apelgren, Spansion Inc.

As semiconductor device technology migrates to the 65-nm node and beyond, process windows for lithography steps are shrinking below equipment tolerances. At previous technology nodes, the depth-of-focus (DOF) for critical patterning layers was large enough to assume that focus variation would not have a significant impact on output quality metrics. As this assumption breaks down, new methodologies are needed to control focus. On the equipment side, traditional techniques for periodic calibration of machine focus are proving incapable of addressing subtle variations that occur on product at small geometries. On product, run-to-run APC control of critical dimensions (CD) using exposure dose alone relies on the underlying assumption that focus deviations will not significantly impact the assumed linear relationship between dose and CD. To address these emerging problems, Advanced Micro Devices (AMD) and Spansion have developed a methodology to calculate critical dose and focus parameters using scatterometry metrology and semi-physical CD models. The system takes advantage of the accurate sidewall profile metrology produced by scatterometry to provide the required focus sensitivity to detect subtle equipment variations before they negatively impact yield. The technique uses production film stacks and design-rule line spacing to ensure that the results are applicable to current products. The present implementation allows each lithography cell to be periodically characterized to ensure that dose and focus settings are optimized for production runs. By measuring in a variety of locations across the reticle field in both horizontal and vertical orientations, the results can be expanded beyond a simple machine focus calibration to include a more detailed characterization of the lithography equipment. Future work will involve extending this methodology to in-line product control. By monitoring and correcting for focus deviations on a run-to-run basis, DOF requirements can be relaxed to support improvements in resolution.

The focus control solution developed by AMD requires accurate, precise and reliable top and bottom CD data to adequately differentiate dose and focus variation. To that end, scatterometry metrology is being used rather than scanning electron microscopy (SEM). The top-down nature of CD-SEM renders it incapable of producing accurate sidewall information, especially at current geometries where critical resist lines are often densely nested and extremely vertical.

To build the process model, scatterometry data is generated for each field of a focus-exposure matrix (FEM) wafer, and the resulting top and bottom CD data is used to fit the parameters to a CD series expansion (Equation 1) to form two independent model expressions relating CD to dose and focus. The series expansion in equation 1 was originally published by Mack et al and is derived from the physics of a generalized optical system. Of critical importance to the quality of the modeled solution is the correct assignment of model orders (m and n) for a given system.

Once models for top and bottom CD have been created and optimized, those models can be inverted to solve for the effective dose and focus of subsequent runs, given new top and bottom CD values. The independent top and bottom CD expressions enable a “2 equation, 2 unknown” system that can be solved numerically or analytically. The quality of the inversion results are highly correlated to the degree of focus observability present in the system, and our results will show how CD response to focus changes can be modulated through the film stack and pattern density of the test vehicle.

The dose and focus output of the model inversion can obviously be used for effective machine focus calibration, but the real power of this technique lies in developing a measurement strategy to calculate reticle tilt, astigmatism and spherical aberration. Extensive wafer mapping can also be used to detect focus “hot spots,” dose and focus uniformity problems, and wafer edge effects.

6518-05, Session 2

Characterization of hyper-NA lithography focus control using scatterometry

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This paper discusses the use of scatterometry to characterize focus control for hyper-NA lithography. As optical lithography is being used to manufacture ever shrinking devices, not only has the numerical aperture of the lens increased but the k1 factor is pushed closer to 0.25, which is its theoretical limit for a single exposure image. As a result, the control of scanner parameters such as focus and dose uniformity is becoming more and more critical for maintaining viable process latitude. This can only be achieved with sensitive and reliable metrology as input to automated process controls.

A variety of techniques based on phase shift technology have been traditionally used to monitor scanner focus [1-3]. Recently scatterometry has offered significant promise as an alternate technique to monitor both focus and dose [4]. In this study, we perform a careful comparison of normal incidence spectral scatterometry to other accepted methods for focus characterization and monitoring, such as

Phase-shift Focus Monitoring (PSFM) and Phase-grating Focus Monitoring (PGFM). We discuss the operating principles of these techniques and compare the sensitivity and repeatability of scatterometry-based focus monitoring to PSFM and PGFM. In addition, the variation observed in characterizing intra-field and across-wafer behavior of a hyper-NA scanner is described when using these different techniques. Finally, the measured focus control performance is evaluated against the best achievable performance of the scanner based on its internal metrology and scanning algorithms.

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6518-06, Session 2

Focus, dose controls, and its application in lithography

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and Takahiro Matsumoto Nanotechnology & Advanced System Research Laboratories, Canon Inc., 23-10 Kiyohara-Kogyo-Danchi, Utsunomiya-shi, Tochigi, 321-3298, Japan Two of the most important process parameters for controlling the lithographic process are the focus and exposure dose. Both affect the circuit pattern in a non-trivial way. For in-line control of the volume production of lithography, A new method as known as the focus and dose line navigator (FDLN) has been developed to estimate the focus and dose deviations from the data of several different kinds of metrology tools. And a new signal processing based on an inverse problem theory for focus sensor of semiconductor exposure tool has also been developed. This methodology involves two steps: First, build the library as supervised data using FDLN result and focus signal. The library means relational equation between the focus error value and focus signal. Second, using this library, signal processing is done on actual process wafers. By using this technology, the focus detection system can be achieved with a high accuracy and robust against varies semiconductor process wafers.

6518-131, Session 2

A comparison of focus monitoring techniques

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In this paper we compare three focus monitoring techniques, Back Side Chrome (BSC) and two ASML proprietary techniques, LVT and FOCAL. Whereas the first technique provides intra-wafer and intra-field information at the same time, the latter two only provide intra-wafer and intra-field information respectively.

For monitoring purposes, an off-line measured focus technique, in our case BSC, is preferred as it does not require readout time on the scanner itself. However it is important to know the difference between information obtained in this way and the information provided by the self metrology techniques (LVT and FOCAL) used to set up the exposure tool itself. From through-batch results and short term monitoring data, we try to correlate the trends between the information obtained from each technique. This is complicated by the different sequence and timing used in each technique and the influence of that will be illustrated by real monitoring data of an XT:1250Di with i2 configuration.

6518-07, Session 3

Statistical optimization of sampling plan and its relation to OPC model accuracy

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Currently, the accuracy of an Optical Proximity Correction (OPC) model is typically judged by a final fitting result, for example, the root-mean-squared edge placement error. Although an eigenvalue cut-off method has been a popular choice and been widely used to prevent over fitting the wafer data, there is no ultimate way to evaluate whether the OPC model has reached the fundamental limitations of the calibration data. On the other hand, although the intrafield and interfield variations of wafer have been observed for a long time, the methodology to set up wafer sampling plan for OPC model calibration has been conventionally based on the assumption that the CD errors can be approximated as being random and normally distributed, and can therefore be fully defined by a 3σ variation and a mean. As lithography proceeds to the 45 nm node and beyond, the total error budget decreases dramatically. As a consequence, the wafer sampling plan has become larger and larger, in order to satisfy final accuracy requirement of the data. However, due to the existence of systematic components in the wafer data variation, simply increasing the number of measurements on the same structure not only results in wasting a large percent of SEM machine time, but also may not reach the true accuracy which is needed by that technology.

In this paper, we seek a systematic strategy for creation of a wafer sampling plan and to determine the relationship between this plan and the OPC model accuracy. We start our study with the traditional error components analysis of wafer data. From this, we introduce our methodology of calculating the effective sampling size based on each pattern and its error component, as shown in Figure 1. As can be seen, with different contributions from each individual error component, the effective sampling size can vary from about 5 to 12, depending on the structure and the distribution of the error. Also, if the location and number of fields, chips, and wafers are not carefully considered in the sampling plan, up to 50% of the SEM time is potentially wasted. With all the error components separated, the confidence of the estimated mean can be calculated and, hence, an error bar can be added to each mean of the wafer data. This error bar is then used to determine which patterns are overfit and which patterns require an improved fit, as shown in Figure 2. In this paper, we will present a method of providing an optimized and economical solution for wafer sampling. With this calculated error bar, the ultimate metric for OPC model accuracy will also be discussed.

6518-08, Session 3

Automatic setup of in-line critical dimension (CD) monitoring and OPC calibration recipes in a foundry environment

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As feature dimensions in an IC shrink, Optical Proximity Correction (OPC) become relatively more complex (1). As a result, there is a dramatic increase in the usage of OPC, with thousands of measurement locations needed on the test wafer to calibrate the OPC model. Hundreds of locations are then typically measured for OPC verification before 'hot spots' are checked on product wafers.

In this paper, we study the feasibility of using Applied Materials OPC Check software to perform not only the above mentioned OPC function, but to also set up in line critical dimension scanning electron microscope (CDSEM) recipes for both litho and etch processes monitoring. OPC Check can automatically create CDSEM measurement recipes based on CAD design data (2). The main advantages of having recipes setup done through OPC Check as compared to performing recipe creation on the CDSEM tool itself are the reduction in CD-SEM tool usage and more importantly, the availability of the recipes before the first wafer is being processed in lithography resulting in a faster of cycle time for new devices.

To facilitate our objective, a new feature was implemented in the design to provide a universal global alignment (GA) feature under both optical and SEM view. The global alignment serves two functions: to minimize device-to-device and layer-to-layer optical variation, and to synchronize design (CAD) and wafer coordinate systems. With this universal alignment feature available across all production layers of interest, we can fully automate recipe creation process from design to production.

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6518-09, Session 3

Quantification of two-dimensional structures generalized for OPC model verification

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Model based optical proximity correction (OPC) today has become a necessity in advanced lithography for 65nm and 45nm design rules in order to achieve production-worthy pattern fidelity. While the model parameters used for OPC can be calibrated and determined by using a limited set of test structures, it is important to note that presently the selection of the test structures suitable for OPC model calibration has been mostly guided by experience and physical intuition. To date, there is no known quantification methodology to ensure the model parameters, as calibrated from a limited set of test structures that can reliably apply OPC without any ambiguity for all of the full-chip patterns.

Doubts often arise from this ambiguity as to whether or not any given mask pattern undergoing OPC is safely “covered” by the model parameters. Since the current mask making cost is high and the design data-to-mask cycle time is long, semiconductor manufacturing demands that the post-OPC mask data to have no errors, or at least no catastrophic errors induced by OPC treatment, such as bridging or short, etc.

Although there are some design for manufacturing (DFM) verification tools use a calibrated model to locate possible trouble locations on the OPC treated mask data, the very fundamental yet perilous assumption in such tools is that the model can be applied universally. In reality, a “calibrated” model can only be reliably applied to those of two-dimensional pattern structures that are lithographically resembled to the test structures used for the model calibration. Without a methodology to quantify a set of generalized two-dimensional structures suitable for OPC model calibration, one can not define OPC “safe” mask patterns.

There is certainly an increasing urgency to call for a methodology to quantify the two-dimensional structures. With such quantification, a “safe zone” of 2D structures can be defined unambiguously, which greatly enhances the reliability of OPC process. In addition, several critical quantities have been proposed to characterize an OPC model so that model assessment can be laid on more quantitative foundation from a statistical point of view. In this report, we demonstrate the working feasibility of our OPC qualification model.

6518-10, Session 3

Setting MRC rules for OPC: balancing inspection capabilities, defect sensitivity, and OPC

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One of the challenges associated with shrinking design dimensions, and advanced RET techniques is finding photomask inspection settings which achieve sufficient defect sensitivity, while supporting aggressive OPC geometries. In the newest technology nodes, cutting-edge mask inspection tools have trouble differentiating between mask defects and features intentionally drawn by designers and modified by OPC software. There are many techniques that can be employed to address this problem, and one of the primary tools is “desensing” the inspection tool. This is a process by which the tool does not stop or flag errors on the smallest features in the die-to-data comparison which allows the tool to handle some small dimensions and features generated by OPC, but at the expense of potentially missing some real defects. There have been many studies done on defect printability, in an attempt to understand what size of defect is potentially harmful, and below which threshold, defects can be safely ignored. Once the needed defect sensitivity is understood, mask manufacturers can characterize their inspection capabilities and then define rules to set constraints in OPC software. As long as the OPC providers do not create features that violate these rules, the mask manufacturer can theoretically inspect the masks, and guarantee a very high likelihood that they will be able to find all defects larger than a fixed size. This approach has been sufficient in the past, but with current OPC demands, this approach to setting defect specifications and mask rules is proving to be problematic.

In this paper, we examine the problems associated with constraining Models-based OPC with mask rules. We give examples of rules associated with the KLA 576 tool at a 90nm pixel-size inspection setting, and specific 45nm layouts which will receive sub-optimal OPC treatment with these rules. We then take the defect specification typically used for this mask layer, and use Monte Carlo simulation methods to place minimum sized simulated defects in various locations in close proximity to these sensitive layouts. We then compare simulations of the optimal OPC, the optimal OPC with the defects, and the sub-optimal OPC. We then use knowledge about the frequency of small defects to compare the risks associated with small mask defects to the risks associated with sub-optimal OPC. This experiment demonstrates that there are some instances where mask rules based on inspection capabilities and defect sensitivity alone can be problematic, and that OPC requirements need to be taken into account when choosing a defect specification and an inspection strategy. We conclude by proposing a strategy for balancing these requirements in a practical manner.

6518-11, Session 3

Methodology to set-up accurate OPC model using optical CD metrology and atomic force microscopy

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For the 90nm node and beyond, smaller Critical Dimension(CD) control budget is required and the ways to control good CD uniformity are needed. Moreover Optical Proximity Correction(OPC) for the sub-90nm node demands more accurate wafer CD data in order to improve accuracy of OPC model. Scanning Electron Microscope (SEM) is the typical method for measuring CD until ArF process. However SEM can give serious attack such as shrinkage of Photo Resist(PR) by burning of weak chemical structure of ArF PR due to high energy electron beam. In fact about 5nm CD narrowing occur when we measure CD by using CD-SEM in ArF photo process. Optical CD Metrology(OCD) and Atomic Force Microscopy(AFM) has been considered to the method for measuring CD without attack of organic materials. Also the OCD and AFM measurement system have the merits of speed, easiness and accurate data. For model-based OPC, the model is generated using CD data of test patterns transferred onto the wafer. In this study we discuss to generate accurate OPC model using OCD and AFM measurement system.

6518-12, Session 3

SEM-contour-based OPC model calibration through the process window

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As design rules shrink, there is an unavoidable increase in the complexity of OPC/RET schemes required to enable design printability. These complex OPC/RET schemes increase the mask complexity and production cost, and can introduce errors that limit yield. The most

common errors are found in OPC design itself, and in the resulting patterning robustness across the process window. Two factors in the OPC design process that contribute to these errors are a) that 2D structures used in the design are not used in OPC model calibration and b) that the OPC model calibration is done at the nominal process settings and not across the entire focus-exposure window. In order to overcome the challenge of designing OPC/RET schemes for manufacturability at the 65nm node and below, the tools used in the OPC generation flow must be tightly coordinated. SEM-contour based OPC model calibration has arisen as a powerful approach to deliver robust and accurate OPC models since every pixel now adds information for input into the model, substantially increasing the parameter space coverage. This work compares two alternative methods for calibrating OPC models. The first method uses a traditional industry flow for making CD measurements on target structures at nominal process conditions. The second method uses 2D contour profiles extracted automatically by the CD-SEM over varying focus and exposure conditions. OPC models were developed for aggressive dipole and quadrupole illumination conditions (193nm wavelength, NA=0.85, k1<0.35, att:PSM) used in 65nm- and 45nm-node patterning. Results are shown for variable weighting of the different process conditions, feature types, and even distinct feature components. The resulting models can be used for post-OPC verification and process-aware OPC. Additionally this work addresses the issues of automating the contour extraction and calibration process, reducing the data collection burden with improved calibration cycle time.

6518-13, Session 4

Meeting overlay requirements for future technology nodes with in-die overlay metrology

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As a consequence of the shrinking sizes of the integrated circuit structures the overlay budget shrinks as well. Overlay is traditionally measured with relatively large test structures which were located in the scribe line of the exposure field in the four corners. Although the performance of the overlay metrology tools improved significantly over time it is questionable if this traditional method of overlay control will be sufficient for future technology nodes. For advanced lithography techniques like double exposure or double patterning in-die overlay is critical and it is important to know how much of the total overlay budget is consumed by in-die components.

We reported earlier [1] that small overlay targets were included directly inside the die area and good performance was achieved. This new methodology opens the possibility for a wide range of investigations. This provides insight into processes which were less important in the past or not accessible for metrology. The present work provides real data, instead of estimates, for the differences between the scribe line and in-die overlay. The influence of scanner-induced distortions (tool to tool differences) and illumination settings on in-die overlay is shown.

Furthermore the registration error of the reticles (Fig.1) is correlated to overlay residuals (Fig.2). The similarity of the patterns can be seen visually. The influence of the pellicle on mask and wafer overlay is studied.

Furthermore, placement errors due to lens aberrations for design-rule-like pattern were measured and compared to simulated results. An excellent correlation was achieved.

Finally, the individual contributors to in-die-overlay are discussed in the context of other overlay contributors and are compared with the available overlay budget. It will be shown that new overlay correction schemes which take advantage of the additional in-die overlay information need to be considered for production.

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6518-14, Session 4

Zero-order imaging of device-sized overlay targets using scatterfield microscopy

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The tolerances required for overlay measurement beyond the 65 nm node will necessitate the use of device-sized targets. One candidate for such a target is comprised of arrays of lines with widths matching the critical dimension of the device. The characteristics of this target would additionally be representative of the actual features of interest printed on the wafers. However, conventional imaging of these targets is problematic as the arrays are much denser than the Rayleigh resolution criterion. We have previously demonstrated using arrayed targets with 50 nm critical dimension and 270 nm pitch that a single array reflects only the zero-order component from its interior while its edges reflect higher order light.[1] This zero-order and edge response can be used to determine the relative position of similar co-located targets, yielding overlay measurements through what is called zero-order imaging. We investigate this imaging mode using a newly constructed scatterfield microscope, essentially a combination of scatterometry and bright field optical microscopy.[2] By coupling engineered illumination to the characteristics of the target, we demonstrate not only the applicability of zero-order imaging to overlay metrology, but also the extensibility of this imaging to linewidth metrology as well. Quantitative values derived from comparisons to theoretical modeling will be presented.

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6518-15, Session 4

Blossom overlay metrology implementation

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Improved overlay capability and sampling to control advanced lithography has accelerated the need for compact, multi-layer overlay metrology. Previous publications [Ausschnitt, et. al. and Binns, et. al.] have described our approach, called Blossom, which minimizes the size of the overlay marks associated with each layer while maximizing the density of marks within the overlay metrology tool’s field of view (FOV).

Here we describe our progress in introducing this approach to 65nm manufacturing and 45nm development. Iterations of recipe build software accompanied by rigorous performance evaluations have converged on an implementation path. Target layout options have been explored to accommodate the needs of scribe-line, within-chip, double-exposure, multiple reference layer, stitched field and alternating phase shift measurement. We present our latest precision, TIS, and tool matching results toward on-product qualification.

6518-16, Session 4

The application of SMASH alignment system for 65-55-nm logic devices

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65-55nm Logic-Devices require high performance of not only the resolution, of but also the overlay accuracy (Mean+3sigmas<20-30nm). Thus, here, overlay performance of several layers in our advanced devices is investigated with using Immersion-exposure-tool. We used the new alignment system called SMASH which is a recently developed phase grating alignment sensor installed in ASML’s immersion-exposure-tool. SMASH supports flexible mark design in terms of size and pitch of the grating so that it can comply for our design

requirement. SMASH has much smaller alignment beam size of ~ 40μm for it.

New mark design for our 65-55nm process will be investigated so as to obtain higher alignment accuracy than that of current marks. The alignment performance becomes more accurate proportionally to data density of the mark and it depends on the diffraction angle and efficiency from the mark. Thus, to obtain acceptable alignment accuracy with smaller mark, it should be designed such as diffraction efficiency is maximized within the required boundary condition in the pitch [diffraction angle] and segmentation of the mark.

In this paper, several new smaller marks are designed and evaluated. The evaluation shows that comparable performance could be obtained in the new design mark as in SMASH original marks. Finally, we select one from the new smaller marks and apply it to our 65-55nm process, especially, to the five process modules (Gate-to-Active, Contact-to-Gate, Metal1-to-Contact, Via1-to-Metal1, Metal2-to-Via1), and performance within 20nm (Mean+3sigmas) are typically obtained. The overlay accuracy needed for our 65-55nm Logic-Devices is successfully achieved with immersion-exposure-tool. SMASH* (SMart Alignment Sensor Hybrid) : the name of alignment system using with phase grating alignment sensor

6518-17, Session 4

Overlay metrology tool calibration

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In a previous publication, we introduced Blossom, a multi-layer overlay mark [Ausschnitt, et al. 2006]. Through further testing carried out since that publication, Blossom has been shown to meet the requirements on current design rules [Morningstar, et al. 2007], while giving some unique benefits. However, as future design rules shrink, efforts must be made now to ensure the extensibility of the Blossom technology.

Previous work has shown that the precision component of Total Measurement Uncertainty (TMU) can be reduced by using extra redundancy in the target design, to achieve performance beyond that of a conventional box-in-box measurement. However, improvements to any one contributor to TMU would not be sufficient for future design rules; therefore we have also to consider Tool Induced Shift (TIS) variability and tool to tool matching.

In this paper, we introduce a calibration artifact, based on the Blossom technology. The calibration artifact is both compact, and produced by standard lithography process, so it can be placed in a production scribe line if required, reducing the need for special sets of calibration wafers compared to other possible calibration methodologies. Calibration is currently with respect to the exposure tool / process / mask, which is arguably more pertinent to good yield, and less expensive, than calibration to an external standard; externally calibrated artifacts would be straightforward to manufacture if needed.

By using this artifact, we can map out remaining optical distortions within an overlay tool, to a precision significantly better than the operational tool precision, in a way that directly relates to overlay performance. The effect of process-induced mark uncertainties on calibration can be reduced by performing measurements on a large number of targets; by taking multiple measurements of each target we can also use the artifact to evaluate the current levels of process induced mark uncertainty. The former result leads to an improvement method for TIS and matching capability. We describe the artifact and its usage, and present results from a group of operational overlay tools.

We show how the use of this information also provides further insight into the layout optimizations discussed previously [Binns et al. 2006]. It provides the current limits of measurement precision and mark fidelity with respect to target redundancy, enabling us to use a predictive cost-benefit term in the optimization. Finally, examining the bulk behaviour of a fleet of overlay tools, allows us to examine how future mark layouts can also contribute to minimizing TMU rather than just precision.

6518-105, Session 4

Improved overlay control through automated high-order compensation

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As Moore's Law drives CD smaller and smaller, overlay budget is shrinking rapidly. Furthermore, the cost of advanced lithography tools prohibits usage of latest and greatest scanner on non-critical layers, resulting in different layers being exposed with different tools; a practice commonly known as 'mix and match.' Since each tool has its unique signature, mix and match becomes the source of high order overlay errors. Scanner alignment performance can be twice as bad in mix and match, compared to single tool overlay operation. In a production environment where scanners from different vendors are mixed, errors will be even more significant. Mix and match may also be applied to a single scanner when multiple illumination modes are used to expose critical levels. This is because different illuminations will have different impact to scanner aberration fingerprint. The semiconductor technology roadmap has reached a point where such errors are no longer negligible. Mix and match overlay errors consist of scanner stage grid component, scanner field distortion component, and process induced wafer distortion. Scanner components are somewhat systematic, so they can be characterized on non product wafers using a dedicated reticle. Since these components are known to drift over time it becomes necessary to monitor them periodically.e per scanner, per illumination. Even with the same scanner pair, if combination of scan direction is different, the signature could change. Therefore, collection of baseline data and its management can be difficult. On the other hand, process impact is believed to be coming from the heat stress caused by the high temperature processes such as RTA and/or etch. Since this component fluctuates randomly, mix and match control should include metrology and correction based on production lots. In this paper, we outline a methodology for automating characterization of mix and match errors, and a control system scheme for real time correction.

6518-19, Session 5

Monte Carlo modeling of secondary electron imaging in three dimensions

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Secondary electron (SE) images from a scanning electron microscope (SEM) are the starting point for much of semiconductor industry dimensional metrology. Roadmap-specified accuracy for measurements is now comparable to or smaller than instruments' spatial resolution. Under this circumstance, achieving the required measurement accuracy for many kinds of measurements (critical dimension in particular) depends upon the ability to model the instrument/sample interaction. This has been successfully demonstrated using a model-based library technique, in which model results are interpolated to match measurements. At NIST the model results are provided by MONSEL, a Monte Carlo program that simulates the full SE cascade using Mott elastic cross sections with SE production via Möller and plasmon processes.

However, sample shapes in MONSEL are limited to a few parameterized classes, for example, lines with translationally invariant trapezoidal cross sections, parameterized by width, height, spacing, corner radius, etc. More complex or inherently 3-dimensional shapes, e.g., lines with a round or complicated footing, lines in which edge or sidewall roughness is important, the rounded corner at the end of a line, or a rounded via, are also important in semiconductor applications, but simulations of these were not available.

NISTMonte, a public domain Java Monte Carlo code developed for x-ray microanalysis, had the required capability to model 3-d shapes, but no modeling of secondary electrons. Accordingly, we have written a "MONSEL package" for NISTMonte. In the process, we have improved the modeling of electron barrier penetration (at surfaces or boundaries between materials) and improved the modeling of materials, including

semiconductors, for which the electron density of states peaks several electron volts below the Fermi level. We will report comparisons of the new 3-d model to the older model for sample shapes accessible to both, and show examples of results from shapes accessible only to the new code.

6518-20, Session 5

Evaluation of CD-SEM measurement uncertainty using secondary electron simulation with charging effect

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CD measurement accuracy becomes more important with shrinkage of pattern size. Generally, the improvement in measurement precision, such as reproducibility, was an important subject for CD measurement. However, the improvement in measurement accuracy, such as actual pattern dimension, has become important for more accurate CD control in recent years. Some measurement techniques for accuracy are examined (TMU: Total Measurement Uncertainty). In case of a very thin line pattern, the pattern edge on both side overlaps with one profile, and the conventional CD measurement can not be measured in sufficient accuracy. Thus, in order to measure the pattern CD with high accuracy, it is important to grasp correctly the physical phenomenon generated by electron beam irradiation. Until now, many analyses of the electron beam irradiation using a secondary electron simulation are reported. And CD measurement technique of presuming an actual cross-sectional form from top-down images by combining the secondary electron simulation and the actual CD-SEM image is considered (MBL: Model Based Library). However, in the case of an insulator, it is necessary to take an charge phenomenon into consideration. The phenomenon of electron beam irradiation cannot be correctly simulated without charge effect, and CD measurement accuracy gets worth using MBL. Although many charge effect by electron beam irradiation are reported until now, the influence of charge on the measured CD is seldom reported.

Then, we developed the secondary electron simulation in consideration of charging effect, and analyzed various SEM images [Figure 1]. And the CD measurement uncertainty using CD-SEM was verified using the secondary electron simulation with charging effect. As CD measurement influenced by charge, we took notice of CD measurement of the bottom of a hole pattern. When measuring the bottom CD of the hole pattern, the insulator surface becomes positive charging by irradiating the large area before CD measurement. The secondary electron generated from the bottom of the hole pattern is pulled out to a detector. Also in the pattern form which has a perpendicular taper angle, the CD-SEM image is observed like a forward tapered shape [Figure.2]. This is because an incidence electron is deflected by the positive charging of insulator surface. The amount of electron beam deflection is computed using the secondary electron simulation. As a result, it becomes possible to measure the actual bottom CD with high accuracy by combining CD-SEM images and results of the secondary electron simulation.

Thus, we will report the analysis results of basic charging effects on several SEM images and the influence of charging effect on the measurement result of CD-SEM, particularly for the bottom CD of the hole pattern.

6518-21, Session 5

Characterization of photo-resist dimension at virgin state and line sliming effect using in-line CDSEM

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CDSEM is widely used as the primary in-line tool to characterize dimensions of photo resist patterns defined by the lithography process. The interaction between the accelerated electrons and the resist molecules may reduce the resist feature size, giving rise to the line sliming effect, particularly for 193nm resists. As a result, the reported feature size by the CDSEM reflects the post-slimmed state. Although AFM does not cause line sliming effect, it suffers from low throughput and tip dependencies. Without a resist chemistry being developed that eliminates these slimming effect, there is a growing need for an in-line characterization technique to measurement resist at the virgin state.

This paper reports the work of a new method that characterizes the resist feature at virgin state using the in-line CDSEM. It is based on novel macro designs. The feature size at the virgin state and the line sliming effect are investigated. The result reported by the new method is consistent with AFM, suggesting it is technically equivalent. Using of this method does not require any change in wafer process or CDSEM tooling. This work would improve process feed back to litho and feed forward to etch, thus boosts fab yield and productivity.

6518-22, Session 5

Carbon nanotube metrology in a CD SEM

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In the Nantero NRAM process, a carbon nanotube film is patterned using conventional photolithography and etch techniques. CD SEM metrology of the printed resist image is straightforward, as the resist pattern can be imaged clearly. However, challenges arise when SEM inspecting an etched nanotube pattern. This is because of the small dimensions of the nanotubes, and hence the thinness of the nanotube film. The nanotubes barely interact with the electron beam. Under conventional SEM inspection, a nanotube pattern is nearly invisible. Using high magnification, high levels of integration, and great care, a nanotube pattern can be imaged, but this is slow and does not facilitate easy characterization or automated metrology.

In order to facilitate nanotube pattern characterization, test structures have been developed which use passive voltage contrast to cause electron emission from the nanotube pattern and from associated conducting structures. These enable manual inspection of the nanotubes, along with automated pattern recognition and automated CD measurement. The voltage contrast is achieved by connecting the nanotubes to a remote charge-sink outside the image field. The voltage contrast occurs with no extra electrical connection to the wafer, and without special SEM components or beam adjustment.

The voltage contrast is used in two general ways: 1. Nanotubes are clearly imaged, enabling inspection, CD measurement, coat-quality characterization, etc. 2. Indicator structures in associated process layers light up when contacted by nanotubes, enabling measurements of line-end shortening; etch bias; overlay; etc.

Various structures have been developed, including: 1. CD cell for manual and automated CD measurement. 2. Vernier structures for characterization of overlay, line-end shortening and etch-bias. 3. Serpentine structure for characterization of nanotube coat quality using conduction length.

6518-23, Session 5

Physical matching versus CD matching for CD SEM

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CD-SEMs fleet matching is a widely discussed subject and various approaches and procedures to determine it were described in the literature.

The different approaches for matching are all based on statistical treatment of regular CD measurements that are performed on dedicated test structures. The test structures are a limited finite set of features, thus the matching results should be treated as valid only for the specific defined set of test features. The credibility of the matching should be in question for different layers and specifically production layers. Since matching is crucial for reliable process monitoring by a fleet of CD-SEMs, the current matching approaches (such as TMU) must be extended so that the matching will be only tool dependent and reproducible on all layers regardless their specific material or topographic characteristics.

In this work the term “Physical Matching” is introduced and a new matching procedures based on physical parameters is described.

This approach extends the conventional matching methods to enable significant improvement of the matching between CD-SEM tools in production environment.

To study and demonstrate the physical matching, we focus on the limited parameters set - the image brightness, contrast and SNR. We

test the sensitivity of CD measurements to changes in these parameters both on test structures and on production layers. We show that while on the test structures the sensitivity is low and reasonable change of the image brightness, contrast or SNR have small effect, on production layers this is not the case and different CD tools that slightly differ in those parameters might be mistakenly considered as matched. The advantage of the physical matching approach for case study is demonstrated. The improved matching procedures are based on a new target that is used to measure the above image parameters directly. This way it is possible to characterize correctly the physical state of the measurement tool and guarantee the same image characteristics which in turn guarantee improved matching on all layers. In the framework of the proposed matching approach a proper determination of the minimal set of physical parameters that is needed to guarantee CD-SEM tools stability and matching should be included.

6518-24, Session 6

Developing the new ADC algorithm that enables to identify the defect source

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1. Introduction

As SoC product life is getting shorter, faster yield ramp becomes the key for all of the device manufacturers. On the other hand, a number of new materials such as Copper for wiring or low-k materials for inter-layer dielectric as well as the new structures are applied to the latest manufacturing process. These changes make it difficult to rapidly improve yield. The conventional ADC (Automated Defect Classification) capture the defect feature based on its size and shape, but cannot identify the process that generates defects. The ultimate goal of ADC is to identify the defect source to reduce the time required for yield improvement. To overcome the disadvantage of the conventional ADC, the new algorithm that makes it possible to identify the defect source is examined. The purpose of this study is to propose the new ADC algorithm and to verify its efficiency through its application to the latest product.

2. Conventional ADC and its disadvantage

Figure 2-1 shows the typical example of the defect classification result by means of the conventional ADC algorithm. Although defects are classified based on either their shape or size, the defect source cannot be identified by this method.

3. New ADC algorithm

Figure 3-1 shows the new ADC algorithm. Since the pattern defect causes serious yield loss after copper dual damascene process introduced, this study focuses on the classification of the pattern defects. The shape of defective pattern gives the useful information to identify the defect source. For example, if a particle exists either in the CVD film or on it, the particle induces the defocus trouble of the resist pattern on the film. In this case, the defective pattern shows the pencil shape. Correspondingly, the relationship between the shape of the pattern and the process step in which defects happen is carefully examined for the typical defects (Trench photo defect, PR bubble, film particle) that cause pattern short. To classify the defects, 2 parameters, pattern size (width) d and the length of the defective pattern x, are taken into account in this study, as shown in Figure 3.2. The new algorithm discriminates from the shape of the defective pattern expressed by the parameters d and x.

4. Efficiency Verification of the New Algorithm

The developed new algorithm is applied to the high volume production line to verify its efficiency. The typical defects in the metallization process (shown in Figure 4-1) are classified using the new algorithm. Figure 4-2 shows the result of the classification. According to the chart, the new algorithm is verified to be capable of classifying the defects and of identifying the defect source (due to photo resist, particles in the CVD film, etc.) with the certain criteria led by d/x.

5. Conclusions

We proposed the new ADC algorithm that enables identifying the defect source more efficient. The proposed algorithm was verified to be efficient through the practical example in the high volume production line, and helpful on in-line excursion prevention.

6518-25, Session 6

Developing μADI methodology for new litho process monitoring strategies

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With the introduction of sub 100nm DR and especially 193nm photolithography the development of new monitoring strategies became necessary due to new material, tool and process challenges. The authors believe that μADI is a big step forward for photolithography defect monitoring as well as for integrated process learning.

Resist quality and handling became essential for the whole process. The new 193nm resists revealed an inherent defectivity, which could be solely attributed to the quality of the resist. This defectivity is originated by very small resist inhomogenities and leads to tiny bridging and stringer defects, which can affect yield critically. On top of that, also the entire lithography process, i.e. handling and scanning, became more critical, as process windows are decreasing to levels of common positioning accuracy and layer thicknesses.

On the one hand more sensitivity is needed for being able to control the resist quality more tightly. The high resolution bright-field patterned wafer inspection methodology provided a lot of improvements over the last years but is capable to fulfill the requirements on test wafers only. On the other hand there is a demand for a monitoring strategy, which is using product wafers and thus able to understand the interaction of material, structure, topography and shrinking process window. Test wafer monitoring is only able to provide an isolated snap shot of a specific work-step without further interaction. This integrated monitoring strategy requires a high resolution based sensitivity and superior noise suppression capabilities - lithography layers e.g. can show a lot of non-yield relevant etch mask defects, which are very hard to suppress with common techniques.

This work introduces a novel after lithography monitoring strategy, which is based on a dark-field defect inspection technique on product wafers. Wafers can be scanned after development with a close to bright-field inspection like resolution at superior noise suppression. This enables lithography defect detection down to single line short level. Thus, completely new inspections approaches for tool and line monitoring can be developed, sample plans can be optimized and time to results and appropriate corrective actions can be significantly shortened.

6518-26, Session 6

Studies on EUV mask storage and contamination problem by EUV reflectometer and optical measurement tool

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As the demands for throughput and critical dimension (CD) control for EUV manufacturing increase, so do the demands on protecting the mask surfaces from contaminations, carbon contamination or oxidation. Degradation of reflectivity will be the critical issue associated with optical components including the patterned masks, handling, transport, and storage. We have studied the handling and storage with patterned masks, as well as carbon contamination removal in conventional experimental setup

This paper reports the results for these evaluations, which is one of challenges in EUV technology to maintain the characteristics of patterned mask. Contamination rate, oxidation rate with patterned mask and at-wavelength peak reflectance were focused.

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6518-27, Session 6

Immersion lithography defectivity analysis at DUV

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Significant effort has been directed in recent years towards the realization of immersion lithography at 193nm wavelength. Immersion lithography is likely a key enabling technology for the production of critical layers for 45nm and 32nm design rule (DR) devices. In spite of the significant progress in immersion lithography technology, process induced defects remain a critical issue. The benefits of the optical resolution and depth of focus, made possible by immersion lithography, are well understood. However, the implementation of immersion lithography could be limited by increased defect density which reduces production yield. Understanding the effect of the immersion lithography process parameters on wafer defect formation and defect density, together with the ability to monitor, control and minimize the defect density down to acceptable levels is necessary for successful introduction of immersion lithography for production of advanced DR's.

In this paper, we present experimental results of immersion lithography defectivity analysis, focused on topcoat layer thickness parameters and resist bake temperatures. Test wafers were exposed on the ASML 1150i-* -immersion scanner, and defect inspection was performed using a DUV inspection tool (Applied Materials, UVisionTM), Defect material analysis and focused ion beam (FIB) cross sectioning was performed for different defects. The analysis revealed defect-types that were not previously reported as detected using visible or UV wavelengths. Higher detection sensitivity was demonstrated through detection of small defects at the DUV wavelength not detected at the visible wavelength, indicating on the potential sensitivity benefits of DUV inspection for this layer. The analysis indicates that certain types of defects are associated with different topcoat layer thickness and with different resist bake temperatures. We expect that similar type of analysis to be performed at DUV wavelengths would enable optimization of immersion lithography processes, thus enabling the qualification of immersion processes for volume production.

6518-28, Session 6

Innovative inspection metrology for wafer edge defectivity in immersion lithography

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In semiconductor manufacturing, control of the process at the wafer edge is a key parameter in determining the total number of yielding die on a wafer. Edge of wafer issues include non-uniformities in process steps such as deposition, lithography, and etch, and potential particle defects from the edge of the wafer, since it is in mechanical contact with various equipment and transport materials. In dry lithography, the process control on the edge is understood quite well, and various edge bead removal (EBR) processes currently exist to ensure the resist and wafer edge are sufficiently clean to pass through the scanner and subsequent process steps. Immersion lithography however changes this situation significantly. Now during exposure, the wafer edge is temporarily in contact with water from the immersion hood, and particles can then be transported back and forth from the wafer edge area to the scanner wafer stage. Materiel in the EBR region can also potentially be damaged by the dynamic physical force of the immersion hood movement.

In this paper, we have investigated the impact of immersion lithography on wafer edge defectivity. In the past, such work has been limited to inspection of the flat top part of the wafer edge due to the inspection challenges at the curved wafer edge and lack of a comprehensive defect inspection solution. This made it very difficult to detect and control defects on the non-flat part of the wafer edge. This study utilized a new, automated edge inspection system from KLA-Tencor. This system provides full wafer edge imaging (top, side, bottom) using laser-based optics with multi-sensor detection including scatter and reflected light for inspection of edge defects. The defects of interest are then classified with Automated Defect Classification (ADC) software. Using this technology, evidence of the wafer edge defect impact from the immersion hood will be shown, as is illustrated in the Figure below. Moreover, results of this methodology will be used for process optimization towards EBR defect control and compared to other conventional inspection techniques.

This kind of metrology and process optimization is important to understand the mechanisms of EBR related immersion defects and to achieve a sufficient die yield level, when these processes are introduced in semiconductor manufacturing.

6518-29, Session 7

A comprehensive study on the limits of optical critical dimension metrology

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This paper is a comprehensive summary and analysis of a study on the limits of optical critical dimension (OCD) metrology. The presentation will focus on two primary elements: 1) the comparison, stability, and validity of industry models and 2) a comprehensive analysis of SEMATECH-chosen process stacks to evaluate the ultimate sensitivity and limits of OCD.

The first material presented will be the evaluation of models at NIST and currently in use by the industry. This was accomplished by establishing a modeling baseline using the NIST exact Maxwell equation integral equation solver and the NIST-developed rigorous coupled waveguide model. Optical responses from electromagnetic scattering simulations using the NIST models and results from two industry models were compared for a standard target set and process stack as well as a more thorough comparison of scattering results for a range of target geometries, wavelength, and incident illumination angles. The four models evaluated show good agreement over a range of targets and geometries for zero order specular reflection as well as higher order diffraction. The models perform well as long as an appropriate grid size or number of orders are chosen. The finite models were also successfully compared to the infinite grating models.

Next, the paper will cover an evaluation and comparison of optical CD limits using different optical scatterometry methods. The fundamental optical limits evaluated were with respect to the sensitivity to changes in 2D/3D profiles (width, height, and side wall angle) for SEMATECH-selected process stacks. The optical response and sensitivity to these process stacks was also simulated in the presence of noise intended to represent a typical industry tool. The investigation involved a comparison and evaluation of angular scatterometry versus spectroscopic scatterometry, and includes polarization dependence and analysis as well. The investigation will also include sensitivity analysis based on recent developments using scatterfield microscopy (1). The effects due to material inhomogeneity from process variation or line edge and line width roughness were not treated here.

A number of process stacks and geometries representing semiconductor manufacturing nodes from the 45 nm node to the 18 nm node were simulated using the different measurement modalities including angle-resolved scatterometry and spectrally-resolved scatterometry, measuring various combinations of intensity and polarization. It is apparent in the results that large differences are observed between those methods that rely upon unpolarized and single polarization measurements.

Using the multi-parameter fits and assuming that the sensitivity of scatterometry must meet the criterion that the 3σ uncertainty in the bottom dimension must be less than 2% of the linewidth, specular scatterometry solutions are shown to exist for all but the isolated lines at 18 nm node. Scatterometry does not have sufficient sensitivity for isolated and semi-isolated lines at the 18 nm node unless the measurement uses wavelengths as short as 200 nm or 150 nm and scans over large angle ranges. Alternative optical measurement solutions are presented for this range of target parameters.

This study laid the groundwork for performing more detailed and, in many cases, more realistic simulations and interpretation of the results. One of the limitations of this study was its lack of a realistic noise model.

The OCD limits are presented here in a way to allow the determination

of ultimate tool performance under those conditions stated. The data do give direct input to the limits and sensitivities using specular scatterometry techniques currently in use by the semiconductor industry. These results point toward improvements the industry can make to improve measurement performance and meet the future ITRS roadmap requirements.

6518-30, Session 7

Detailed analysis of capability and limitations of CD scatterometry measurements for 65- and 45-nm nodes

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Control of critical dimension (CD) of 65 and beyond nodes is hot issue now. As soon as feature size reduces it becomes difficult to measure CD precisely. A lot of factors can influence on accuracy of measurement. Scatterometry method is applicable for both production and development purpose, and can be used for in-situ or ex-situ control.

In this work we study influence of CD non-uniformity and sidewall angle as well as influence of parameters of measurement system on precision of result. TE, TM and unpolarized light with different angle of incidence on grating structure is considered to find the best conditions for CD measurements of 65 and 45 nm nodes. Rigorous coupled-wave analysis (RCWA) is used for theoretical spectra calculation and least square method for results extraction. Reflected spectrum from structures containing non-uniform or uniform CDs with variation of sidewall angle is compared with the set of theoretical spectra, and CD value with layer thickness is extracted in the same way as in the real experiment. It is shown that CD non-uniformity and sidewall angle can be estimated through comparison of results obtained with different polarization state of light. Best choice of polarization, angle of light incidence, range of wavelength for spectrum measurement and parameters of library for spectrum analysis is obtained in order to provide precise and fast scatterometry measurement for 65 and 45nm nodes mask structures.

6518-31, Session 7

Real-time profile shape reconstruction using dynamic scatterometry

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In-line process control in microelectronic manufacturing requires real-time and non-invasive monitoring techniques. For example, scatterometry uses the ellipsometric signature (i.e., Stokes coefficients vs. wavelengths) of light scattered by periodic structures to follow the shape of a grating in real time during etch processing.

Traditionally, the direct problem of defining the shape and computing the signature is dealt with using Modal Method by Fourier Expansion. However, the inverse problem cannot be solved as easily. Different classes of algorithms have been introduced (evolutionary, simplex), but the method of library searching is more commonly used in industry. For the latter, a signature library is built-up using different combinations of profile parameters (CD, height, sidewall slope, etc.) and the experimental signature is compared with the library for the best match.

Although generating the library requires a lot of computation time, solving the inverse problem can be made very fast because pattern matching is reduced to a simple numerical database search. Unfortunately, this technique becomes difficult and inexact when scatterometry data is limited in wavelength resolution (i.e., data is acquired at only a few wavelengths due to speed requirements in real-time process control situations). Specifically, the library method fails because several database patterns can be matched to the experimental data.

In this work, we present a method for real-time reconstruction of grating shape variations using dynamic scatterometry data. Since it is not possible to solve the inverse problem for each time step, our idea is based on the following: a fully defined signature is measured at t = 0 before processing and subsequent partial signatures are used to intelligently refine the library search using Tikhonov time-regularization. In this method, the best library match is selected using appropriate weighting of both the proximity to the measured data and the smoothness of shape variation over time. Mathematically, a time-related term (based on previous history) is used to couple each time t Tikhonov minimization problem; in this way, harsh shape variations are avoided - allowing smooth and realistic, real-time pattern reconstruction. This time-related term couples one given time t equation with previous profile candidates that fall within a certain history window. Clearly, the most accurate pattern reconstruction for time t occurs when using the entire scatterometry history. However, computing resources are limited in a real-time control application; as such, processing time must be decreased using optimized minimization and library-search routines.

This approach has been implemented in the present work as a general C++ architecture dedicated to scatterometry. The system integrates multiprocessing (shared memory) capability for high-speed signature generation and the use of the Graphic Processing Unit (GPU, video card processor) as a numerical database accelerator for the library-based inverse problem. Due to the inherent vector architecture of the GPU, the entire library search operation can be made in only a few clock cycles.

The talk will deal with pattern recognition software development and focus on a comparison of real (AFM topography) and inferred (scatterometry time-based regularization) profiles evaluated at different stages of etching.

6518-32, Session 7

Mueller polarimetry in the back focal plane

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Conical diffraction geometry is receiving increasing interest for scatterometry. In contrast with teh ordinary planar diffraction geometry, the grating lines are not perpendicular to the incidence plane, which increases the amount of information provided by intensity and/or polarimetric measurements. For the practically interesting case of small period gratings, the data collected at a single wavelength but various polar and azimuthal angles can be even more relevant then those obtained at fixed angles and variable wavelengths. In this respect, the Optical Fourier Transform method, where the back focal plane of a large numerical aperture opitcal system is imaged on a CCD is particularly interesting, as it allows complete measurements over a wide 2D angular range simultaneously, without any moving parts.

In this communication, we will present our first results with a complete Mueller polarimeter based on this approach for the characterization of isotropic as well as grating samples. The advantages and shortcomings of complete polarimetry with respect to reflectometry will be discussed

6518-34, Session 7

Modeling the effect of line and trench profile variation on scatterometry measurements

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The modeling used to interpret scatterometry measurements usually assumes the profiles are periodic. We investigate the effects that variations in profile have on specular reflectance and polarization from a grating consisting of parallel lines or trenches. We model the effects of variations by calculating the reflectance of a superstructure, in which the profiles are randomly modulated about their nominal profile. We investigate, as an example, a nominal grating consisting of 100 nm silicon lines having a vertical sidewall angle, a pitch of 200 nm, and a height of 100 nm probed with a wavelength of 532 nm. We vary the edge positions, the edge profiles, the line heights, and the trench depths and find that the Stokes reflectance can be modified from its nominal value by a relatively large amount, especially in the case of line-width variations. We find that the reflected field can be approximated by the mean field reflected by a distribution of periodic gratings and that the field does not represent the field from the average profile. When fitting results to more than one modeled parameter, the changes that are observed can be enough to shift the deduced parameter in some cases by more than the rms variation of that parameter. The diffuse reflectance (the non-specular diffraction efficiency) is found to increase

with the variance of the fluctuations. The implications of these findings will be discussed.

6518-194, Session 7

Realizing design-based metrology

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Being able to rapidly introduce a product into production, ramp the production volume and maintain high yields is essential for a semiconductor manufacturing company to stay competitive. The integration of in-line manufacturing data with design is an enabler for achieving this goal. This integration will allow learning to occur at an earlier point in the product introduction thus reducing time for product qualification which will allow for a faster production ramp. In addition, this early learning will enable more rapid yield fixes thus reducing time to achieve high yields. Ultimately these two factors could increase profits by $100M or more, depending on production mix.

There are several approaches to the problem of assessing the impact of pattern fidelity and other anomalies on device functioning. Current state of the art is to make statistical assessments. For complex manufacturing due to the long learning times and small incremental improvements associated with statistical result generation, the probability approaches are no longer adequate to achieve and maintain technology leadership. The inherent technical barrier that the statistical approach has is that it is dependent on large sample volumes. In current complex manufacturing, the cost of obtaining a large enough sample is cost prohibitive and may not be able to be obtained at all due to the trend towards smaller volume production runs. The goal of this effort is to create the foundation to make a deterministic assessment on device functionality (yield) from each individual anomaly.

The best approach to achieve this goal is to fuse the existing manufacturing data, numeric data and image data, to design in order to facilitate and formulate an integrated multi-source assessment. This integration of manufacturing data with design can be accomplished but requires the augmentation of the image data for location, size, and basic measurement extraction. This paper specifically targets a solution to the image processing technical barriers that have deterred industry investment in a deterministic solution. An approach has been developed to address these barriers via an image-to-design based software analysis engine. This hardware-independent, software-based approach provides the ability to rapidly compare, in high volume, multiple images to the design database, providing vectorized polygons extracted from the images which can be analyzed versus the original design intent using area and dimensional techniques.

6518-35, Session 8

TEM calibration methods for critical-dimension standards

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One of the key challenges in critical dimension (CD) metrology is finding suitable calibration standards. Over the last few years there has been some interest in using features measured with transmission electron microscope (TEM) as primary standards for linewidth measurements. This is because some modes of TEM can produce atomic lattice images that are traceable to the SI (Système International d'Unites or International System of Units) definition of length. As interest in using calibration samples that are closer to the length scales being measured increases, so will the use of these TEM techniques.

An area where lattice spacing images produced by TEM has been used as a primary standards is in critical dimension atomic force microscopes (CD-AFM), where they are used for tip width calibration. Two modes of TEM that produce crystal lattice images are high resolution transmission electron microscope (HR-TEM) and annular dark field TEM (ADF-TEM). HR-TEM produces lattice images by interference patterns of the diffracted and transmitted beams rather than the actual atomic columns, while ADF-TEM produces direct images of the crystal lattice. The difference in how both of these techniques work could cause subtle variations in how feature edges are defined.

In this paper we present results from width samples measured using HR-TEM and ADF-TEM. We examine the level of uncertainty that can be obtained when each TEM technique is used for this type of analysis. Next we compare the results with measurements taken from the same location by two different CD-AFMs. Figure 1 shows schematic diagrams of the measurement principle for CD-AFM, HR-TEM and ADF-TEM.

Both of the CD-AFM instruments used for this work have been calibrated using a single crystal critical dimension reference material (SCCDRM). These standards were developed by NIST and SEMATECH and used HR-TEM for traceable width calibration. Consequently, the present work and the prior SCCDRM work provide a mutual cross-check on the traceability of the width calibration.

6518-36, Session 8

Image simulation and surface reconstruction of undercut features in atomic force microscopy

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The atomic force microscope (AFM) provides an important tool for dimensional measurement of topographic features at atomic resolution. Conventional AFMs, due to their cone-like probe shape and the unidirectional feedback systems, have their images restricted to shapes (called "umbras") characterized by a single height at each lateral position. Reentrant, or even nearly vertical, parts of specimens are not imaged accurately.

For a number of years now, probes with lateral protrusions and feedback systems with bi-directional servo control have been incorporated into the newer AFM instruments. These instruments, which are capable of imaging undercut features, have found applications as reference metrology tools at SEMATECH and in a number of fabs. Despite such hardware progress, the underling algorithms for AFM image analysis have not been able to match such progress for the following reasons:

• Even though methods are available for tip-specimen interaction modeling for conventional AFMs, they are not directly applicable to re-entrant surfaces. This is because current algorithms are based on grayscale morphology. They assume an umbra-like specimen shape.

• Simple offset of AFM CD measurement by the probe width, although applicable to sidewall measurement, does not produce accurate characterization of structural dimensions, particularly when sidewalls are sloped.

An approach based on slope-matching and erosion has recently been introduced in [1] to address this issue. However, its implementation is limited to 2D and its morphological implementation is limited to removing points on the outer boundary of the surface.

In this paper, new mathematical morphology software for AFM image simulation and surface reconstruction, applicable for complex 3D structures with under-cut features, is introduced. The developed approach is based on a representation of 3D objects in which the usual rectangular array of pixels (single height) is replaced by an array of "dexels." Unlike a pixel, a dexel element may have multiple heights in each column. This allows the under-cut features to be represented in the dexel form. We have developed algorithms for dilation and erosion of dexels. These permit image simulation and surface reconstruction for 3-d objects of arbitrary shape.

The validity of the developed dilation and erosion algorithms is demonstrated for structures with and without undercut features. Through the comparison between the new dexel-based software and existing grayscale morphology software, we demonstrate the consistency between the software for structures without under-cut features. Through examples of dilation and erosion operations on a set of known 3D surface shapes, we illustrate the usefulness of the dexel-based software for objects with under-cut surfaces.

The application of the software to linewidth measurement based on both synthetic and actual AFM data is also presented.

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6518-37, Session 8

Statistical approach utilizing nonlinear regression for CD error prediction

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In various critical dimension (CD) control techniques in the field of lithography such as optical proximity correction (OPC) and advanced process control (APC), we need to create models of relationship between CD error and various error sources. A key for successful result of the CD control is whether we can make good model that can predict CD error prior to actual wafer processing. In general, the each model is derived from a physical-based function. However, the sources of CD error are so numerous and the interaction among them is so complicated that it is difficult to build a sufficient robust physical-based model. In such cases, a statistical based model such as regression model is often tried to be used. Although a statistical approach cannot avoid uncertainty, robustness is expected once an effective model is constructed.

We have made an attempt to create CD error model by use of statistical nonlinear regression. An approach of neural network is attractive to describe a nonlinear relationship between inputs and outputs. In this paper, we show the application of the neural network approach to the prediction of CD error induced by proximity effect. In addition to the intensity of aerial image, mask layout information including pattern density, which is difficult to treat by a conventional lithography simulation based on a lumped parameter, were used as the input parameters. As a result, the neural network approach provided higher prediction accuracy than a conventional lithography simulator. We also report the application of the nonlinear regression approach to the analysis of CD error in manufacturing line. In a state-of-the-art semiconductor manufacturing line, we can easily sample large amount of the state information of exposure tool via Equipment Engineering System (EES). By utilizing EES, the regression successfully extracted a hidden correlation between CD error and some error sources.

6518-38, Session 8

X-ray reflectivity and scattering for pattern shape metrology

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Recently we demonstrated that specular X-ray reflectivity (SXR), when complimented by critical dimension-small angle X-ray scattering (CD-SAXS), can be a powerful methodology to quantify the complete cross section of nanoscale pattern.1,2 The SXR data from parallel line-space patterns, with a pitch of approximately 200 nm, was fit with a multilayer recursive model based on the solutions to a one-dimensional Schrödinger equation. These fits provide electron density (proportional to mass density) of the patterned film as a function of height. From the electron density profile, one can deduce the line-to-space ratio variations as a function of pattern height. If the pitch of the patterns is known via CD-SAXS, the absolute pattern cross-section can be defined. The reason why this technique works is that the coherence length of the X-ray source, which defines the length scales over which the density from SXR is averaged, was larger than the characteristic dimensions of the nanostructures being patterned. For the line-space patterns previously studied, the effective density of the patterned region was equal to the density of the fully dense material reduced by the appropriate volume fraction defined by the line-to-space (dense-to-open) ratio. This is referred to as the effective medium approximation (EMA). The focus of this presentation is to explore the limits of applicability for the EMA, and thus the limits of SXR as an effective pattern shape metrology. Our study is extended to parallel-space grating patterns with periodicities ranging from 200 nm to 16 μm. SXR measurements are made with the incident X-ray beam both perpendicular and parallel direction of the grating. For periodicities less than 900 nm, the perpendicular and parallel measurements yield comparable SXR curves. For periodicities 900 nm and greater, the parallel measurements yield very complicated SXR curves, inconsistent with the EMA. For the perpendicular orientation periodicities all the way out to 16 μm were consistent with the EMA. From this we can conclude that the lateral coherence length (in the width direction of the beam) of our X-ray source is on the order of 900 nm. In the longitudinal direction (in the incident beam direction) it is apparently larger than 16 μm. Knowing these dimensions will place limits on the use of SXR as a pattern shape metrology.

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6518-39, Session 8

Accuracy in optical image modeling

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Wafer exposure process simulation and optical photomask feature metrology both rely on optical image modeling for accurate results. To gauge the accuracy of an imaging model one might compare the model results with an actual image. Modeling results, however, depend on several input parameters describing the object and imaging system, such as wavelength, illumination and objective NA's, magnification, focus, etc. for the optical system, and topography, complex index of refraction n and k, etc. for the object. Errors in these parameter values can lead to significant differences between the actual image and the modeled image. In addition, feature width must now be added to the parameter list. Because of these parametric uncertainties, one would hope and expect the models to be far more accurate than such a comparison might indicate.

One can also compare different imaging models with each other. While the parameter nominal values should be chosen to represent real objects and instruments, they will be identical for both models and contribute no uncertainty to the conclusions. Although not a complete answer to the question of modeling accuracy, differences in model results can at least set a lower limit to the modeling uncertainty.

There are some additional factors which can contribute to image modeling inaccuracy. Since analytic solutions are unavailable in the vast majority of realistic cases, numerical solutions are used. This introduces some computational parameters like grid size, how many terms to carry in an infinite series, how many discrete illumination plane waves to calculate, etc. There is always a tradeoff here between accuracy and computation speed. These parameters can be set by trial and error, but since a model may not always converge nicely as a parameter is advanced, it is difficult to evaluate the magnitude of the errors arising from the computational parameters.

Two very different optical imaging models were used in this study. Both solve Maxwell's equations numerically for the illumination and boundary conditions describing photomask exposure. The Integral Equation model solves for the image of a single isolated object and the Modal Waveguide Model solves for an infinite array of identical objects using the differential form of Maxwell's equations. Both were used to model a range of quasi-isolated photomask linewidths and spacewidths, and the image differences were quantified by calculating the apparent feature width differences in a measuring microscope. The results are expressed as nanometers of difference over a range of feature sizes.

Admittedly not a complete or satisfactory answer to the question of image modeling accuracy, such a differential comparison at least places a meaningful number on modeling differences and sets a lower limit on modeling accuracy.

Conference 6518: Metrology, Inspection, and Process Control for Microlithography XXI

6518-40, Session 8

Single crystal critical dimension reference materials (SCCDRM): process optimization for the next-generation of standards

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Critical dimension atomic force microscopes (CD-AFMs) are rapidly gaining acceptance in semiconductor manufacturing metrology. These instruments offer non-destructive three dimensional imaging of structures and can provide a valuable complement to CD-SEM and optical metrology. Accurate CD-AFM metrology, however, is critically dependent upon calibration of the tip width.

The NIST response to this need was the development of single crystal critical dimension reference materials (SCCDRMs). [1-3] In 2004, a new generation of SCCDRMs was released to the Member Companies of SEMATECH - a result of the fruitful partnership between the organizations. These specimens, which are fabricated using a lattice plane selective etch on (110) silicon, exhibit near vertical sidewalls and high uniformity can be used to calibrate CD-AFM tip width to a 1 nm standard uncertainty.

Following the 2004 release, NIST began work on the “next generation” of SCCDRM standards. A major goal of this thrust was to improve upon the SCCDRM characteristics that impact user-friendliness: the linewidth uniformity and cleanliness. Toward this end, an experiment was designed to further optimize the process conditions. This experiment employed a model with six two-level factors. These factors were:

1. Pre-thinning of the oxide hard mask before silicon patterning,

2. Concentration of KOH and etch duration used for patterning,

3. Use of ultrasonic agitation during patterning,

4. Use of ultrasonic agitation during cleaning of chips with iso-propyl alcohol,

5. Duration of cleaning with iso-propyl alcohol, and

6. Use of acetone or oxygen plasma to remove carbon deposits from SEM inspection.

The last factor in this experiment was recently completed. A preliminary analysis of our results shows great promise for further improvement of the SCCDRM process. Among other observations, we found that the minimum linewidth and linewidth uniformity were primarily sensitive to different factors - and can thus be independently tuned to meet our future goals. These results are summarized in figures 1 and 2.

Presently, we are planning a new refining experiment to further optimize the important factors that we have identified. Our strategic goal is develop a NIST Standard Reference Material (SRM) based on our SCCDRM technology. We are considering both a chip-based (as in the 2004 release) and a monolithic 200 mm wafer implementation for this standard. The measurement focus is expected to be on isolated lines that are most suitable for CD-AFM calibration, but we are also exploring application of this technology to grating standards for scatterometry.

6518-41, Session 9

Comparison and uncertainties of standards for CD-AFM width calibration

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Since the advent of commercial CD-AFM technology in the 90s, these tools have enjoyed growing acceptance in semiconductor manufacturing both for process development and to support in-line CD metrology. The most common application of CD-AFMs has been to support CD-SEM metrology as a reference for tool matching or as a non-destructive alternative to TEM and SEM cross sections.

Although the scale calibration uncertainties that dominate CD-AFM pitch measurements also apply to width measurements, these are not typically the most significant terms for deep submicrometer linewidth measurements. Instead, the most challenging source of uncertainty in width measurements is the calibration of the tip width and shape. [1, 2]

The interaction of a CD-AFM tip with the imaged surface is complex, but for many purposes a highly simplified and two-dimensional model can be useful. In this basic model, the effect of the tip is represented as a simple additive offset which must be subtracted from the apparent width to obtain an accurate measurement. The uncertainty in the value of the tip width to subtract is sometimes referred to as the zeroth order tip width uncertainty. [2,3]

The finer details of the tip-sample interaction, pertaining to things like flare radius, feature sidewall angle, feature corner radius, and the three-dimensional nature of both the tip and sample are thought of as being higher-order tip effects. While higher order effects can be important in the measurement of less uniform structures such as photoresist lines, these effects are often negligible for measurement of relatively uniform structures - particularly those with near-vertical sidewalls. Such structures are thus useful as CD-AFM tip width calibration standards.

For many years, CD-AFM users typically developed in-house reference standards for tip width calibration - often based on SEM or TEM cross sections. But the uncertainty of such standards was often large or unknown. Tip characterizer samples - which used a sharp ridge to calibrate the tip width - are commercially available. However, scanning such samples can result in tip damage, and the uncertainty of tip calibrations based on this method is limited to about 5 nm.

In 2004, both NIST and VLSI Standards responded to this need for more accurate CD-AFM tip calibration. VLSI Standards introduced the NanoCD(tm) series of width standards. [4] These specimens are fabricated using a technique that involves deposition of alternating layers of silicon and oxide, followed by a cross section and oxide etch.

At about the same time, NIST released single crystal dimension reference materials (SCCDRMs) to the Member Companies of SEMATECH - a result of the fruitful partnership between the organizations. [5,6] These specimens, which are fabricated using a lattice plane selective etch on (110) silicon, exhibit near vertical sidewalls and high uniformity can be used to calibrate CD-AFM tip width to a 1 nm standard uncertainty.

Using instruments at both NIST and SEMATECH, we are performing a detailed comparison of these two standards and an assessing the relative uncertainties associated with their use. We will also intend to compare the uniformity, navigation, and ease of use for both standards.

6518-42, Session 9

An investigation of atomic force microscopy to measure spacer and dual-stress liner profiles

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Channel strain engineering has recently replaced gate oxide scaling as a means to improve device performance. Dual stress liner (DSL) is a common approach used by several chip manufacturers today to gain a substantial speed increase at the same power levels, compared with same transistors without strain engineering, and entails depositing a tensile nitride on NMOS and a compressive nitride on PMOS regions. Spacer engineering is also important because it is critical for the dopant profiles and for device contacts.

Variation of spacer and DSL profiles around the gate leads to a broader device speed distribution lot-to-lot, within lot, and within wafer at the 90nm node and beyond. Reducing this variation and therefore improving Circuit Limited Yield (CLY) is of significant value, and cannot be done without valid metrology. Specifically, it is important to determine the thicknesses of oxide and nitride spacers, and the dual stress liners, as well as Si recess and nitride pulldown post nitride spacer patterning. Because of the complicated profile of the features at hand, xSEM is traditionally used for this purpose, but is destructive, slow, and provides a very limited sample of data.

We have demonstrated the ability to perform these measurements on a CD-AFM by imaging the resulting topography at subsequent steps. It is obvious that in a manufacturing environment, one desires the fastest and least expensive solution that fulfills the basic requirements. Within the confines of the CD-AFM, this implies choosing the appropriate scan mode/tip combination. Thus, we will also be reporting the results of

evaluating several tip types under several scan modes for the aforementioned applications.

Additionally, there's a big difference between a manually operated tool and a manufacturable solution, and we intend to determine whether a true inline solution is possible. This paper will be reporting upon an evaluation of an inline application of a CD-AFM for the purpose of APC feedback for spacer and dual stress liner patterning.

6518-43, Session 9

Use of carbon nanotube probes in a critical-dimension atomic force microscope

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Ever increasing miniaturization of semiconductor chips demands the advancement of critical dimension (CD) AFM technology, where the creation and employment of ideal probes like carbon nanotubes (CNTs) are of primary concern. As we reported in previous presentations, the precise control of CNT orientation, length, and end modification allows us to implement ball-ended and bent tips for CD-AFM [1]. Such CNT tips have actually been employed in a commercial CD-AFM, Dektak* SXM AFM at NIST. Generally, slender CNT easily bends under lateral stress, and likely adheres to the adjacent vertical sidewall when the tip and the sidewall are in parallel. Measurement artifacts arise in various ways depending on the tip type, tip geometry, pattern feature under scan, and scan parameters, prompting optimization of tips for practical purposes. This presentation includes our research results about, first, the general interaction between nanotube tips and surface features (and the resulting CD AFM system response), second, the optimization of nanotube tips for CD-AFM, third, CD-AFM images obtained with the optimized tips, and finally the limited optimization of scan parameters which is not under our full control.

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*Certain commercial equipment, instruments, or materials are identified in this abstract to foster understanding. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the materials or equipment identified are necessarily the best available for the purpose.

6518-44, Session 9

Profiles of buried and surface relief gratings determined by spectroscopic scatteometry and atomic force microscopy

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A series of surface relief gratings with ultra narrow line width from 15 nm to 150 nm and written by state-of-the-art e-beam lithography has been investigated. Two methods were used to determine the profile: (1) scatteometry and (2) a well calibrated atomic force microscope. In order to allow the AFM to track all parts of the grating profile the grating is investigated under different tilt angles. Further one buried multilayer grating with period of approximately 570 nm has been investigated using scatterometry. The measured quantities of the profile include the sidewall angle of approximately 90°, the groove height from 50 nm to 150 nm, and the filling degree from 10 % to 40 %. The two methods, which respond to very different material properties, give consistent results and demonstrate that scatteometry can be used to determine the topology of both buried and surface relief low aspect ratio gratings.

6518-45, Session 9

In-line AFM characterization of STI profile at the 65-nm node with advanced carbon probes

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At the 65nm node and beyond, the ability to control the step height between active area and isolation oxide in the shallow trench isolation (STI) module of a process flow is of paramount importance to improve die yield and device performance. During definition of the STI module, variations in process parameters lead to the formation of a divot at the interface between isolation and active area which, as dimensions scale down, also become of detrimental impact to final device performance. In recent years, the Atomic Force Microscope (AFM) has been proposed as a metrology solution to characterize step height and divot. Incidentally, the minimum size of these recesses can be as low as about 20 to 40 nm in width and 30 to 40 nm in depth, hence the actual AFM tip's apex radius and length cannot be considered anymore as ideal.

In this paper, we report results of STI profile measurements done with a commercially available VX340 AFM system from Veeco Instruments, using advanced dense carbon tips. Dense carbon is a material with a much higher Young's modulus than silicon, which minimizes low tip degradation. The dense carbon tips used in this study feature an apex radius of as low as 2nm, which is significantly smaller than the typical width and depth of the STI divot. Superior reproducibility, accuracy and longer tip lifetime compared to regular focused ion beam milled probes has been achieved. This paper describes also the differences in terms of accuracy and reproducibility of divot depth measurement between an algorithm based on the histogram analysis of data point population, and a new measurement algorithm based on analysis of profile shape. The measurement reproducibility was estimated to be better than 1.5 nm (3sigma), and the tip lifetime greater than 1300 engages. The AFM data has been compared with TEM cross-sections to determine the accuracy of the measurements and to show the correlation between the two techniques.

6518-46, Session 10

Impact of thin film metrology on the lithographic performance of 193-nm bottom antireflective coatings

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At 65nm device generations and below, requirements for bottom antireflection coating (BARC) performance are extremely stringent. Reflectivities as low as 0.1% and even lower are often required. BARC thickness and complex refractive index values must be highly optimized for the specific resist, film stack, and even for the feature size and lithographic imaging parameters being used. Implicit in the optimization procedure is the assumption that the optical properties of the BARC have been measured to sufficient accuracy so that the uncertainty in the measurement of these BARC properties will not have a significant impact in the lithographic performance of the resulting optimized BARC.

In this paper, we will perform a theoretical analysis of the BARC optimization process with respect to the propagation of BARC n&k measurement errors. For several realistic cases, specifications on the measurement accuracy of these optical parameters will be derived and the lithographic consequences of BARC metrology errors will be explored. Typical experimental BARC measurement uncertainties will be shown and compared to these accuracy requirements. Approaches to improving the measurement of BARC thickness and n&k will be suggested.

6518-47, Session 10

Dielectric-thickness dependence of damage induced by electron-beam irradiation of MNOS gate pattern

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Inspection or measurement methods using an electron beam will become essential for device production processes in the near future. For example, CD-SEM is currently the main in-line method for critical dimension (CD) measurement of gate structures. In addition, the SEM inspection method has the capability to detect electrical defects and patterning issues, which at present may be optically invisible[1]. However, electron irradiation of a device pattern can damage or affect device performance. To develop damage-free methods for in-line inspection using an electron beam, mechanisms that induce damage should first be analyzed. In the previous paper, we analyzed the damage of MOS capacitors induced by SEM inspection [2]. We found that higher-energy electron beams, whose electron range was larger than the thickness of the gate electrode, created traps at the interface between the Si substrate and the gate dielectric.

In this study, we analyzed the damage of MNOS capacitors with various gate dielectric thicknesses. There is a higher possibility that SiON gate dielectrics could leak or the threshold voltage (Vth) may shift more easily due to the nitridation of the gate dielectric. The effects of the dielectric thickness on irradiation damage were also studied.

We prepared capacitor test elementary groups (TEGs) for a MOS and MNOS (for high-performance CMOS). The thicknesses of the gate dielectrics were changed from 2.45 - 10.0 nm. Before and after irradiation of the electron beam, high-frequency and quasi-static C-V characteristics were measured to determine the flat-band voltage (Vfb), and the density of created traps. Leakage currents were also determined from I-V characteristics.

According to these experimental results, we found that there is no remarkable difference between MOS and MNOS capacitors. We also found that the induced damage strongly depends on the thickness of the gate dielectric. Damage was induced when a higher-energy electron beam, whose electron range was larger than the thickness of the gate electrode, was irradiated. The electron dose was 10 times higher than that under the typical inspection condition in these experiments. When the electron beam was irradiated on the MOS capacitor, whose gate dielectric thickness was 10.0 nm, the Vfb shifted due to the created traps. On the other hand, when the electron beam was scanned over the MOS or MNOS capacitor, whose gate dielectric thickness was 4.0 nm, the Vfb shifted less than 5 mV. However, the leakage current was 10-7 A/cm2 at a Vg of 3.0 V. When the electron beam was scanned over the MNOS capacitor, whose SiON dielectric thickness was 2.45 nm, the leakage current was not increased. This may be because the electron-scattering probability is much smaller in the 2.45-nm-thick dielectric. In addition, even if the electrons are scattered thereby creating electron-hole pairs in the gate dielectric, the created electrons and holes can pass through the gate dielectric by direct tunneling. Accordingly, the electron beam energy should be lower, so the electron range is smaller than the thickness of the gate electrode, which enables damage-free inspection when the gate dielectric thickness was 4.0 nm and thicker.

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6518-48, Session 10

OPC model data collection for 45-nm technology node using automatic CD-SEM offline recipe creation

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ABSTRACT

Optical and Process Correction in the 45nm node is requiring an ever higher level of characterization. The greater complexity drives a need for automation of the metrology process allowing more efficient, accurate and effective use of the engineering resources and metrology tool time in the fab, helping to satisfy what seems an insatiable appetite for data by lithographers and modelers charged with development of 45nm and 32nm processes. The scope of the work referenced here is a 45nm design cycle “full-loop automation”, starting with gds formatted target design layout and ending with the necessary feedback of one and two dimensional printed wafer metrology.

In this paper the authors consider the key elements of software, algorithmic framework and CDSEM functionality necessary to automate CDSEM recipe creation. We evaluate specific problems with the methodology of the former art, “on-tool on-wafer” recipe construction, and discuss how the implementation of the design based recipe generation improves upon the overall metrology process. Individual target-by-target construction, use of a one pattern recognition template fits all approach, a blind navigation to the desired measurement feature, lengthy sessions on tool to construct recipes and limited ability to determine measurement quality in the resultant data set are each discussed as to how the state of the art design based (DBM) approach outperforms the former methodology.

The offline created recipes have shown pattern recognition success rates of up to xx% and measurement success rates of up to yy% for line/space as well as for 2D Minimum/Maximum measurements without manual assists during measurement.

The overall results of using design based “wafer less” recipe construction show marked improvement in a number of key areas by which the metrology is gauged.

6518-49, Session 10

Optical line-width measurement below 50 nm

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In a recent publication1, we have demonstrated optical line width measurement in the range of 50nm, with a precision better than 2nm. The line width is less than 1/50th of the diameter of the point spread function of the optical system used for the experiment, and is well beyond the conventional resolution limit of the optical system. The measurement is performed by using an ultrastable optical interferometer together with artificial neural networks. The optical system provides extremely stable signal of high signal to noise ratio, and the artificial neural network is used to extract information from the signal that are of interest to the measurement. Currently the system uses an objective lens with a numerical aperture of 0.3, and a HeNe laser (wavelength = 632.8nm). By increasing the NA of the objective to near unity, and by using a laser of shorter wavelength, 10 nm measurements are well within the ability of the technique. We will present results obtained on a number of different samples.

Our current research is concentrated on extending the application areas of the technique, so that it can be used to measure samples of more general types. In order to measure a sample which we do not have prior knowledge, it is crucial that the output signals from the optical system is classified properly. A successful classification of the signal is similar to gaining a priori knowledge of the sample, and will greatly reduce the difficulty associated with measuring very small dimensions. In this talk, we will discuss several methods that are potentially capable of performing such classification. These methods include artificial neural networks, principal component analysis and projection pursuit. We will show the methodology of the measurement process, which consists of five main steps: 1) profiling of the sample using the optical interferometer; 2) classification of the optical signals; 3) dividing the signals to appropriate range; 4) applying necessary signal conditioning algorithms to the signal; and 5) measure relevant parameters using the ANNs. We will discuss the possibility of using the measured parameters of the key components of the sample to reconstruct the sample profile, with details much smaller than that can be obtained directly from the optical system. Results obtained from both experiment and computer simulation will be used to illustrate the abilities of the various methods.

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Conference 6518: Metrology, Inspection, and Process Control for Microlithography XXI

6518-50, Session 10

Metrology challenges for advanced lithography techniques

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Traditionally CD SEM has been positioned as a local critical dimension measurement and analysis technique. New emerging lithography techniques motivate CD SEM to face challenges such as overlay error measurements.

For the sub 40 nm nodes, several new litho techniques are developed that implies multiple lithographic and process steps. Seamless integration of litho and processing for optimal CD and registration performance requires specific CD and/or overlay metrology. Areas of development are situated at CD measurement algorithms and correlation after develop and etch. Naturally, such litho process has furthermore the consequence that overlay needs to be measured with unprecedented accuracy and on resolution.

Unique overlay target design in combination with innovative CD SEM measurement techniques will be described in this article. Fundamental and application specific metrology challenges and solutions will be highlighted.

6518-51, Session 11

Transition from precise to accurate critical dimension metrology

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A radically new methodology has been implemented to evaluate quality of 65 nm technology critical dimension (CD) metrology and its readiness for production. Elements of the methodology were used in a previously reported scatterometry evaluation study [1]. At every critical process level precision, bias, linearity and the total measurement uncertainty (TMU) were evaluated for metrology fleet over extended periods of time using the technology representative set of samples. The samples with variations fully covering and often exceeding process space were pre-calibrated using CD AFM. Precision of the CD AFM measurements was determined for every analyzed process level based on repeated measurements conducted over several days. The NIST traceable standards were used to verify CD AFM line CD and scale calibrations. Therefore, for the first time the NIST traceability has been established for CD metrology at every critical process level for the entire technology. The data indicates an overall healthy status of the 65 nm CD metrology. Sub-nanometer accuracy has been established for gate CD metrology. The thorough CD metrology characterization and specifically absolute CD calibration were instrumental in seamless technology transfer from 200 mm to 300 mm FAB.

The qualification of CD metrology has also revealed several problems. Most of the problems are well-known from the previous studies and should be addressed soon. CD scanning electron microscopy (SEM) has a systematic problem with bias of CD measurements. The problem is common for several front-end and back-end of line process levels. For most process levels TMU of CD SEM is noticeably affected by sample modification inflicted by electron irradiation (shrinkage, charging, buildups, etc.). This is causing difficulty, especially in the case of fleet TMU evaluation. An improved data collection methodology should be devised to minimize the impact of sample modification on fleet TMU measurements.

The reported progress in semiconductor industrial CD metrology became possible after a recent breakthrough in line CD standard technology [2,3], recognition of CD AFM as a valuable instrument for CD traceability [4,5] and development of the concept and mathematical tools for TMU analysis [6,7].

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6518-52, Session 11

Device metrology with high-performance scanning ion beams

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Scanning ion microscopes (SIM) employing high performance ion sources and optics have been proposed as a replacement for the conventional CD-SEM in device metrology. The rationale for this major change of emphasis is that the e-beam columns used for metrology are compromised in performance because of their need to balance a number of competing requirements. For example the desire to minimize resist shrinkage and damage, and to maximize edge definition, is met by operating at low beam energies, but this choice reduces the brightness of the electron source and inevitably degrades the electron-optical performance because of chromatic aberration and diffraction limiting effects.

A SIM potentially offers both higher performance, a greater variety of imaging options, and a more effective optimization of operating conditions. In the ALIS system, the He+ ion beam produces a secondary electron (iSE) signal which is an order of magnitude higher than the eSE signal from an electron beam at the same energy, and the iSE yield continues to rise with increasing energy. Further, raising the incident ion energy E0 does not degrade spatial resolution because the range varies only slowly with E0, ion backscattering is limited and falling, and the beam remains predominantly forward rather than laterally scattered. In addition chromatic aberration in the ion optics is minimized and the ion source brightness is increased. Both signal generation and instrument performance are therefore optimized under the same operating conditions permitting sub-nm resolution to be achieved at beam energies of 20-30keV.

Because the range of He+ ions for beam energies below about 100keV is comparable with the mean free path for ion generated secondary electrons (iSE) then the behavior of the iSE yield as a function of surface orientation to the beam differs substantially from that observed in the e-beam generated SE signal (eSE). The iSE signal is also more sensitive to surface chemistry and to the crystallographic state and orientation of the sample, and any charging induced by the ion beam is always positive in nature. As a result of these factors the form of iSE line profiles across a feature is rather different to the corresponding eSE profile and new algorithms for metrology will be required. A first approach to simulating iSE profiles based on an extension of the Bethe-Salow model of eSE production has been developed to meet this need.

An intriguing alternative possibility is to use Rutherford backscattered (RBS) ions for imaging. This is possible because at low and medium energies the He+ ion beam has a relatively high (~5-10%) backscatter yield even from low atomic number targets such as silicon. The RBS ions have a very limited escape depth, giving excellent edge definition, and are immune to the effects of surface charging. RBS and iSE profiles thus provide complementary data for a more complete analysis of device metrology.

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6518-53, Session 11

Beyond measurement uncertainty: improving the productivity of metrology tools

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A key responsibility of a metrology engineer is to reduce measurement uncertainty. While important, decreasing measurement uncertainty is only one of many tasks the metrology engineer needs to address. Continually improving the productivity of the metrology toolset is another responsibility that requires the appropriate skills and analysis tools to address the key issues efficiently. Often, limitations in recipe build experience, inadequate calibrations and monitoring of the fleet and toolset limitations, cause many productivity issues that directly affect the cycle-time and the efficient use of engineering resources. This paper explores the analysis tools needed to improve productivity. Examples of analysis tools used at IBM will be shown along with how they have lead to improved productivity of the fleet. Further, future requirements will be discussed catered towards standardizing the critical information needed from suppliers for building universal analysis tools to allow improvements in productivity to be realized by all.

6518-54, Session 11

Realizing value-added metrology

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The conventional premise that metrology is a “non-value-added necessary evil” is a misleading one, which must be viewed as obsolete thinking. Many metrology applications are key enablers to traditionally labeled “value-added” processing steps in lithography and etch, such that they can be considered integral parts of the processes.

Various key trends in modern, state-of-the-art processing such as optical proximity correction (OPC), design formanufacturability (DFM), and advanced process control (APC) are based, at their hearts, on the assumption of fine-tuned metrology, in terms of uncertainty and accuracy. These trends are vehicles where metrology thus has large opportunities to create value through the engineering of tight and targetable process distributions. Such achieved distributions make possible predictability in speed-sorts and in other parameters, which results in high-end product. The necessary quality metrology is strongly influenced by not only the choice of equipment, but also the quality application of these tools in a production environment. The ultimate value-added by metrology is a result of quality tools run by a quality metrology team using quality practices.

This paper will explore the relationships among present and future trends and challenges in metrology, including equipment, key applications, and metrology deployment in the manufacturing flow. Of key importance are metrology personnel, with their expertise, practices, and metrics in achieving and maintaining the required level of metrology performance, including where precision, matching,, and accuracy fit into these considerations. The value of metrology will be demonstrated to have shifted to “key enabler of large revenues,” debunking the out-of-date premise of metrology being “non-value-added.” Most of the examples used will be from critical dimension (CD) metrology, but examples from overlay, films and defect metrology will also be sought.

6518-56, Session 11

Enabling immersion lithography and double patterning for memory devices

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Most semiconductor manufacturers expect 193nm immersion lithography to remain the dominant patterning technology through the 32nm technology node. Conventional immersion lithography, however, is unlikely to take the industry to 32nm half-pitch. Various double patterning techniques have been proposed to address this limitation. These solutions will combine design for manufacturability (DFM) and advanced process control (APC) strategies to achieve desired yield. Each strategy requires feeding forward design and process context and feeding back process metrics. In this work, we discuss interim solutions for control of immersion lithography and double patterning lithography (DPL) with the objective of enabling these technologies at 32nm half-pitch. Although most examples relate to memory manufacturing, many are applicable to logic as well.

Practical interim solutions have been developed to support the CD and overlay control required for immersion lithography, double-patterning (Figure 1), and spacer-etch alternatives for patterning at 32nm half-pitch.

• Intra-field grating-based overlay metrology has been shown to cut overlay model residuals by more than 50%, so that 3nm overlay control targets are achievable from a measurement perspective. Embedded, in-die, micro-grating targets may be necessary to provide the localized metrology required in double patterning strategies (Figure 2).

• 3D CD metrology based on spectroscopic ellipsometry has been extended to measure multiple shape and profile parameters simultaneously, enabling rapid feedback of focus, exposure, and critical dimension information to the litho cell. Segmented grating patterns down to 30nm have been monitored successfully (Figure 3).

• 2D CD metrology based on spectroscopic ellipsometry has been extended to provide accurate feed-forward and feedback to the etch module, enabling critical APC adjustments required for spacer-etch alternatives to double patterning lithography. Ultra-thin spacers have been measured down to dimensions of 4nm (Figure 4).

• Virtual metrology using lithographic simulators, calibrated with feedback from metrology tools, is becoming a highly beneficial technology for rapid qualification of immersion lithography tools. In our examples, we show how advanced simulators take into account the effects of hyper-NA, TE polarization, and mask topography.

When implemented on state-of-the-art metrology tools, these solutions can provide accurate process metrics to enable immersion lithography and double patterning at 32nm half-pitch. Moreover, if they can reduce the qualification time and increase the yield of $50M lithography cells, standard factory economic models suggest benefits in the tens of millions of dollars per factory per year.

6518-138, Session 11

Improved dimension and shape metrology with versatile atomic force microscopy

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Accurate, precise, and rapid three dimensional characterization of patterning processes in integrated circuit development and manufacturing is critical for volume production with high yield, top quality, fast cycle time, and low cost. As process tolerances and circuit geometries shrink with each technology node, the precision, accuracy, and capability requirements for dimension and profile metrology intensify. The present work adopts the scanning probe based technology, 3D atomic force microscopy (AFM), to address current and next-generation critical dimension (CD) metrology needs for device features at a variety of process steps. Fast, direct, and non-destructive 3D profile characterization of patterning processes is a primary benefit of CD AFM metrology. Vertical height/depth, lateral line/trench width, sidewall shape profile, and surface topography can be measured at sub-nanometer resolution. Instead of traditional contact and tapping scan modes, the CD AFM utilizes a deep trench (DT) mode for narrow and deep trenches, and a CD mode for linewidth and sidewall profiling. The 3D capability enables one tool for many applications where conventional scanning electron microscopy (SEM), scatterometry, and stylus profiler tools fall short: Gate etch/resist linewidth and sidewall cross-section profile, etch depth for high aspect ratio via, copper trench fencing detection, STI etch depth/polish recess, 3D analysis for FINFET and ITFET multi-gate devices, pitch/CD/sidewall angle (SWA) verification for scatterometry targets, post-CMP contact dome/dishing, and surface roughness for SiGe and tungsten films. AFM measurements are NIST traceable and insensitive to bias induced from target proximity,

materials, and density. The measurement is precise, and more accurate than CD SEM. It takes approximately one minute for AFM to capture full 3D data in all x/y/z axes, rather than hours for TEM. The tiny AFM probe can scan nondestructively anywhere in-circuit or scribe without sample preparation or vacuum. The AFM is an efficient tool for rapid process improvement/development, and is a complementary addition to the dimension metrology family.

6518-57, Session 12

Correlation length and the problem of line-width roughness

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Although Line Edge or Line Width Roughness (LER and LWR) is considered as one of the main obstacles in the further advancement of lithography to sub-65nm dimensions, crucial issues concerning it, such as its effects on device operation, its measurement and characterization and its material and process origins, remain open and under intensive investigation.

As regards the LWR characterization issue, the simple solution of employing the standard deviation of the line widths Rq (or σ) has been shown to be inadequate since it ignores the dependence of Rq on the evaluation interval L (the line length included in the measurement area)[1]. To overcome this difficulty, it has been proposed to measure Rq at sufficiently large L (\>2μm) where, in most cases, the dependence on L almost disappears[2]. However, LWR concerns us due to its degradation effects on the operation of transistor gates whose widths correspond to resist line lengths much lower than the above L. Thus, we need a way of relating the Rq at large L to its behaviour at lower L. This can be done either by calculating the whole Rq(L) curve or, more economically, by a three parameter model describing the main features of this curve (see Fig.1). The model includes apart from Rq at very large L, the correlation length ξ and the roughness exponent α. The correlation length ξ is associated with the line length above which no correlations exist among line widths and Rq saturates at almost a constant value, while the roughness exponent α quantifies how wiggle the line is and determines how fast the Rq(L) curve lowers as L decreases.

In this work, we focus our attention on the correlation length and its implications to the three open LWR issues referred in the beginning. The first issue is whether Rq suffices for capturing all the effects of LWR on transistor characteristics such as the off currents and the threshold voltage deviations. Extending our previous work[3], we show that lines or gates with identical Rq at large L but different correlation lengths exhibit different effects on transistor performance (see Fig.2). In general, lines with lower ξ generate gates with more reliable operation. This effect is connected to the interrelation of LWR and CD variation and the crucial role of ξ on it.

The second issue regards the definition and measurement of ξ. This can be done through either the correlation functions (autocorrelation or height-height correlation) or the Rq(L) curve. We compare the values of ξ extracted by these methods and focus on the statistical reliability of their measurements by calculating the standard deviation of measured values over a large number of line samples.

Finally, we shortly comment on the effects of resist properties and process conditions on the correlation length with particular emphasis on the size of polymer molecules and the acid diffusion length.

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6518-59, Session 12

Characterization of line-edge roughness in Cu/low-k interconnect pattern

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Scaling of MOSFETs is making the influences of line-edge roughness (LER) on semiconductor device performance a serious problem. LER of gate patters are intensively studied because size of the pattern is smallest in MOSFETs. Although LER of interconnect patterns was not attracted much attention, recently, it was pointed out that it might cause increase of resistivity [1, 2] and degradation of time-dependent dielectric breakdown (TDDB) immunity [3, 4]. As it has already been reported, LERs in resists, SiO2, and poly-Si have symmetric shape against the ideal edge line (denoted as symmetric LER, hereafter) [5]. In addition to symmetric LER, wedge-shaped LER which is due to the protruding metal into inter-metal dielectric (IMD) was observed in low-k pattern [3, 4]. Such LER (denoted as wedge-shaped LER hereafter) gives larger impact on TDDB reliability than the symmetric LER even if they have same LER value (3sigma). This is because the electric field concentrates at the tip of the wedge. Therefore new metrics other than the conventional 3sigma for the characterization of LER of interconnect patterns which can detect the wedge-shaped LER are required. Moreover, surface porosity of a line trench sidewall makes LER of Cu/low-k interconnects large when porous low-k materials are used as IMD.

In this study, we investigated the LER of actual Cu/low-k interconnect patterns in detail and found that we could evaluate the wedge-shaped LER of interconnects using skew in LER histogram.

The results show the line edges of ArF resist and low-k patterns extracted from the images of critical dimension scanning microscope (CD-SEM). In contrast to the resist pattern, wedges protruding into the low-k line are observed in the low-k pattern. In order to evaluate the wedge quantitatively, deviation of the line-edge position from the ideal edge point was measured at n points (denoted as delta-xi, where i=1, 2, ... n). The histograms of delta-xi (i.e., LER histograms) are calculated. Wedge LER causes a long tail at the right side of the histogram, while symmetric LER results in symmetric histogram. The symmetry is evaluated by calculating skewness of the histogram. Skewness of zero and positive value correspond to symmetric and wedge-shaped LER, respectively (negative value indicates low-k material spikes out to the space area). We have measured the skewness of twenty-four edges and calculated the average. The obtained average skewness values of ArF resist and low-k histograms are -0.13 and 0.67, respectively. Namely, the LER in the ArF resist pattern is almost symmetric while the low-k pattern has the wedges. Furthermore, auto-correlation function was calculated, and it was found that the width of the wedge was 50 to 80 nm.

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6518-60, Session 12

Impact of acid diffusion length on resist LER and LWR measured by CD-AFM and CD-SEM

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The improvement of devices performances is due to many factors such as new architectures, new materials and better lithography resolution. Resist chemical components play a key role in the final performance of a specific resist. In addition to resist characteristics such as : resolution, etching selectivity, the final resist LER and LWR becomes a critical issue because it can degrade resolution and linewidth accuracy [1] and causes fluctuations of transistors performances [2-8]. LER, LWR is currently calculated with top-view SEM images [9-10]. LER and LWR in chemically amplified photoresists can be partially controlled by acid diffusion length during the post-exposure bake. Acid diffusion length related to photoacid generator size has an impact on LER [11-12].

In this paper we propose to compare two different techniques CD-AFM and CD-SEM in order to study the impact of various acid diffusion lengths on LER and LWR. The first results show different trends depending on the technique used, as shown in figure 1 which compares

the measured LER from CD-SEM versus CD-AFM for the same exposure on the same wafer. Therefore, CD-SEM could immediately have a non negligible impact on near term new resist manufacturing and lithography and etching processes development. Finally we propose strengths and weaknesses of each technique.

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6518-61, Session 12

Advanced edge roughness measurement application for mask metrology

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Mask Manufacturers are continuously asked to supply reticles with tighter CD (Critical Dimension) specifications, such as CD uniformity (CDU) and mean-to-target. To meet this on-going trend the industry is in a quest for higher resolution metrology tools, which, in-turn, drives the use of SEM metrology into standard mask manufacturing process. As dimensions of integrated circuit features reduce, the negative effects of roughness of the features due to litho and etch process on CDU and mean-to-target CD become more pronounced, since there is no corresponding reduction of roughness with dimension reduction.

As a result of the increased problems, metrics that quantify roughness of specific sections of an integrated circuit have been developed; for example, line edge roughness (LER) and line width roughness (LWR) measuring the roughness of a linear edge and of the CD values along the edge, respectively.

This paper continues previous efforts on the analysis of LER on wafer and reticle level [1, 2] to the field of mask metrology. In order to better understand the types of roughness as well as the impact of the CD-SEM roughness measurement capabilities on the control of the mask process, the sensitivity and accuracy of the roughness analysis were qualified by comparing the measured mask roughness to the design for a dedicated LER test mask. Additionally, the precision of LER measurements was determined.

All measurements were performed on an Applied Materials RETicleSEM system using the built-in algorithms to extract the LER values.

For a better understanding of the impact of the generated mask roughness on the final printed wafer also aerial image simulations both of the original CAD design and of the Mask SEM contours were carried out to estimate the CAD to Mask transfer effects.

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6518-114, Session 12

The coming of age of tilt CD-SEM

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The need for 3-D metrology is becoming more urgent to address critical gaps in metrology for both lithographic and etch processes. Current ArF lithography often results in resist lines with re-entrant profiles or t-topping, as do many etch processes. Also, recent advancements in gate process technology also raise challenges to traditional top-down metrology. One such example is the FinFET, which is truly a 3-D device with 3-D metrology needs.

The ability to measure the bottom width of a profile is crucial for process control. Recently, tilt-beam critical dimension-scanning electron microscopy (CD-SEM) applications have been developed to measure bottom CD of such features, using the tilted-view to "see" the bottom, avoiding the feature's larger top. This is an important achievement, as the bottom of a profile is the main feature of interest in many processes.

Estimation of sidewall angle is also quite important. For several years, tilt-beam CD-SEM has been an available technology for this measurement, with limited adoption by the litho-metrology community. However, in this paper we will explore another method to use the tilt feature to measure average sidewall angle, based on edgewidth measurement and the assumption of basic trapezoidal profile and known height, and combined with the multiple-feature sampling of MacroCD. While it will not provide exact profile shape, this technique can be quite useful in providing average profile information and will definitely exhibit good throughput. Samples used will be photoresist and etched FinFET structures to measure bottom CD and sidewall angles. An evaluation will be done that shows the uncertainty of the measurement of bottom CD and sidewall angle, with accuracy being considered through a correlation to a CD-atomic force microscopy (AFM) reference measurement system. Conclusions will show preliminary findings of the readiness of tilt-beam CD-SEM for measuring profile and, by extension, the status of measuring 3D structures such as FinFETs, and using CD-SEM as a direct control of lithographic tooling for t-topped resist profiles.

6518-195, Session 12

Line-edge roughness and cross sectional characterization of sub-50-nm structures using CD-SAXS

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Critical dimension small angle x-ray scattering (CD-SAXS) is a measurement platform with the potential capability of quantifying the average cross section profile and line edge roughness in patterns ranging from (10 to 500) nm in width with sub-nm precision. CD-SAXS measures the diffraction of a collimated X-ray beam with sub-Angstrom wavelength from a periodic pattern such as those found in optical scatterometry targets to determine pattern cross section. The capability of CD-SAXS for line-edge roughness (LER) characterization is tested through the measurement of patterns with sub-50 nm linewidths fabricated with EUV lithography and designed with roughness with controlled amplitude and frequency. For these patterns, CD-SAXS provides high precision data on cross section dimensions, including sidewall angle, CD, and pitch, while also providing the amplitude of line edge roughness. In limited cases, both the amplitude and the

frequency of line edge and line width roughness are obtained. Ongoing efforts to compare CD-SAXS measurements of pattern cross section with optical critical dimension (OCD) and top-down scanning electron microscopy (SEM) will be discussed. Comparisons of line edge and line width roughness measurements will also be discussed between CD-SAXS and SEM.

6518-63, Session 13

Scatterometry on pelliclized masks: an option for wafer fabs

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Optical scatterometry-based CD and profile metrology is now widely used in wafer fabs for lithography, etch, and CMP applications. This acceptance of a new metrology method occurred despite the abundance of well-established CD-SEM and AFM methods. It was driven by the desire to make measurements faster and with a lower cost of ownership. Over the last year, scatterometry has also been introduced in advanced mask shops for mask measurements. Binary and phase shift masks have been successfully measured at all desired points during mask production before the pellicle is mounted. There is a significant benefit to measuring masks with the pellicle in place. From the wafer fab's perspective, through-pellicle metrology could verify mask effects on the same features that are characterized on wafer. On-site mask verification would enable quality control and trouble-shooting without returning the mask to a mask house. Another potential application is monitoring changes to mask films once the mask has been delivered to the fab (haze, oxide growth, etc.). Similar opportunities apply to the mask metrologist receiving line returns from a wafer fab. The ability to make line-return measurements without risking defect introduction is clearly attractive. This paper will evaluate the feasibility of collecting scatterometry data on pelliclized masks. We explore the effects of several different pellicle types on scatterometry measurements made with broadband light in the range of 320-780 nm. The complexity introduced by the pellicles' optical behavior will be studied.

6518-64, Session 13

Development of advanced mask inspection optics with transmitted and reflected light image acquisition

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The lithography potential of an ArF (193nm) laser exposure tool with high numerical aperture (NA) will expand its lithography potential to 65nm node production and even beyond. Consequently, a mask inspection system with a wavelength nearly equal to 193nm is required so as to detect defects of the masks using resolution enhancement technology (RET). Wavelength consistency between exposure tool and mask inspection tool is strongly required in the field of mask fabrication to obtain high defect inspection sensitivity. A novel high-resolution mask inspection platform using DUV wavelength has been reported, which works at 198.5nm. The wavelength is close to the wavelength of ArF exposure tool.

To balance competing goals for inspection speed and defect detection sensitivity, we have developed a novel high-resolution mask inspection optics to form magnified mask pattern images by collecting illumination light transmitted through the mask and reflected from the mask simultaneously. Moreover, the focusing sensor using reflection illumination light (198.5nm) has been developed, in order to detect both of transmitted and reflected pattern images in-focus. The focusing sensor has the advantageous feature that focusing error caused by repeated small size pattern on the mask is eliminated, limited illumination light source power is effectively utilized and detecting the focusing point with the same wavelength as mask pattern imaging.

Figure 1 shows a schematic diagram of the newly designed split field illumination image acquisition optics and focusing sensor optics. In this system, the laser beam in the illumination optics is split into two beams to enter the transmission illuminator and the reflection illuminator. The beam for the reflection illuminator is merged again at the bottom side of the objective imaging lens and works as the reflection illumination. The illumination area on the mask is split into two rectangular areas: one is the transmission illumination region and the other is the reflection illumination area.

The XY stage scans the mask so the mask as to capture the transmitted and reflected mask image respectively. Imaging beams from the mask are separated by split mirror at the imaging plane and delivered to TDI (Time Delay Integration) sensor. Two TDI sensors are used for detecting transmitted light and reflected images simultaneously.

To detect the transmitted and reflected light image acquisition simultaneously, illumination interaction may cause image deterioration. Low aberration transmittance illumination optics and focusing function are effective to avoid the illumination leak.

Figure 2 shows the defect pattern images of 94nm defect patterns with transmitted and reflected lights using the 198.5nm optical system. As the defect size reduced to 94nm, only the reflected illumination optics can detect the defect signal. For the other type of defects, transmitted illumination has good sensitivity, so the transmitted and reflected image acquisition has complementary advantages for improving defect detection sensitivity.

Figure 3 shows the focusing offset error, which is influenced by the repeated small size pattern on the mask. Only 0.04 um offset occurs on the mask of 0.2um L/S pattern, and this value is within the objective lens focus depth.

6518-65, Session 13

Real-time monitoring of reticle etch process tool to investigate and predict critical-dimension performance

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As mask pattern feature sizes shrink the need for tighter control of factors affecting critical dimensions increases at all steps in the mask manufacturing process. To support this requirement Intel Mask Operations is expanding its process equipment monitoring capability. We intend to better understand the factors affecting the process and increase our ability to predict substrate health and critical dimension performance.

This paper describes the methodology by which we are able to predict the contribution of the dry etch process equipment to overall critical dimension performance. We describe the architecture used to collect process related information from sources both internal and external to the process equipment. In addition we discuss the method used to assess the significance of each parameter and to construct the statistical model used to generate the predictions. It will further discuss the methodology used to turn this model in to a functioning real time prediction of critical dimension performance. We will discuss how this prediction can be used to drive improvements and provide early detection for process excursion.

6518-66, Session 13

CAD-based line/space mix-up prevention for reticle metrology

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Critical dimension metrology is a key factor in semiconductor manufacturing, that helps keep a process stable. The measured CD is used for Statistical Process Control (SPC), in which a process is kept within its specification limits of the design, and within its defined control limits to maintain stability.

The metrology tool has to provide long term measurement stability, while keeping high sensitivity to process variations. Especially for mask metrology, a 100% success rate of all measurements to be performed is essential because only one misprocessed structure would result in

scrapping and reprocessing the mask. Further, the number of measurements typically performed on a reticle is significantly higher than on a wafer. Therefore, it is not possible to create CD-SEM recipes online on the metrology tool, but automated recipe generation from CAD design is needed.

One of the key factors to ensure long term measurement stability is the ability to measure always the correct feature at the correct location. This demand requires high measurement placement accuracy from the metrology tool. As the industry goes toward the 45 nm technology node, navigation accuracy of metrology tools gets more an more critical, especially for the case of 1:1 line space pattern structure in a deep array typical for DRAM masks.

In this case the standard SEM Pattern Recognition (PR) anchor reference cannot provide a good solution, because it can confuse between the line and the space resulting in high percentages of confused measurements of a line instead of a space and vice versa. This is especially true for SEM recipes automatically created from the CAD design, because in this case a synthetic pattern recognition target is created and no SEM based pattern recognition target is used. Therefore, a possible different contrast between lines and spaces on a mask cannot be utilized for distinguishing lines from spaces.

A unique solution was developed to allow measuring 1:1 line/space structures correctly.

The provided algorithmic solution is based on the analysis of the SEM waveform profiles, and a smart identification of its characteristics. Based on this information, distinction between line and space can be achieved.

The solution allows fully automated CAD based offline recipe creation with a high success rate of distinction between lines and spaces for 1:1 pitch cases without the necessity of editing recipes on the tool in advance of performing the measurements.

6518-67, Session 13

Aspects and new developments on edge angle and edge profile metrology at PTB

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Measurement and control of edge profiles and edge angles is increasingly important in microlithography. Especially for critical dimension metrology a sophisticated multi-dimensional shape metrology is mandatory. Different type of dimensional metrology instrumentation is in use today for edge profile and edge angle measurement. While destructive cross section SEM measurements often serves as reference, AFM and optical scatterometry systems are commonly used for day-to-day or in-line control. Due to the limitations of these metrology systems (AFM: slow, scatterometry: only integral measurements of periodic structures), the evaluation and modelling of top down SEM images is increasingly considered, too.

At the PTB both SEM and AFM as well as optical scatterometry are applied for edge angle and/or edge profile metrology, supported by optical transmission microscopy.

For AFM-based edge angle measurements either an AFM with a tilted tip in step mode or ultra-sharp tips are used. In addition we currently develop a measurement system combining both a vertical and a horizontal step mode, which will allow us to measure edge profiles and angles even for undercut edges. The measurement ap-proach and the status of the system will be presented.

At the PTB we have realised a new DUV hybrid scatterometer for measurements over the full range of 6025 masks which combines essential elements of a reflecto-meter, an ellipsometer, and a diffractometer. As radiation source a frequency multi-plied Ti:Sa laser system is applied. It provides four wavelength ranges (fundamental: 772-840 nm, SHG: 386-420 nm, THG: 257-280 nm, FHG: 193-210 nm). Using the fourth harmonic allows at-wavelength metrology of state of the art photolithography masks. In addition to scatterometric measurements this set-up allows to measure the complete Müller-matrix including transmission, polarisation and depolarisation. This new set-up will be presented in detail. Furthermore first scatterometric measure-ments of grating structures on chrome on glass (CoG) masks and the corresponding analysis procedures to deduce the grating topography will be shown.

Finally we study the possibilities of evaluating high resolution top down SEM images to determine edge angles. Different types of edge operators have been developed at PTB which allow to evaluate very precisely top and bottom edge positions. The po-tential of edge angle evaluation using these new analysis procedures will be dis-cussed.

We present an overview of the PTB measurement capability with an emphasis on newly developed metrology methods and systems. The current measurement capabilities of the different systems will be compared and discussed.

6518-68, Session 13

Study of polarization and rigorous effects on phase shifting masks through simulations and in-die phase measurements

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As lithography mask process moves toward 45nm and 32nm node, phase control is becoming more important than ever. Both attenuated and alternating PSMs (Phase Shift Masks) need precise control of phase as a function of both pitch and target sizes. However conventional interferometer-based phase shift measurements are limited to large CD targets and requires custom designed target in order to function properly, which limits phase measurement.

Imaging simulations, both, in a rigorous and a Kirchhoff regime, show the dependency of the phase in the image plane of a microlithography exposure tool on numerical aperture, polarization, and on the so-called balancing of the mask for features close to the size of the used wavelength. For these feature sizes, the image phase does not coincide with the etch depth equivalent phase calculated from the nominal depth and optical constants of the shifter material. Additionally, for PSMs generating phase jumps deviating from 180°, the resulting phase in the image plane of a microlithography exposure tool depends on the transmitted diffraction orders through the aperture of the imaging system.

Consequently Zeiss, in collaboration with Intel, has started the development of a laterally resolving Phase Metrology Tool (Phame(tm)) for in-die phase measurements.

In this paper we present this optical metrology tool capable of phase measurement on individual line/spaces down to 120nm half pitch. Alternating PSM, Attenuated PSM, Cr-less masks were measured on various target sizes and simulations were performed to further demonstrate the capability and implication of this new method to measure the scanner relevant phase in-die, taking into account NA, polarization, and rigorous effects.

6518-69, Session 14

Advances in process overlay: alignment solutions for future technology nodes

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Semiconductor industry has an increasing demand for improvement of the total lithographic overlay performance. To improve the level of on-product overlay control the number of alignment measurements increases. For direct-alignment (also called layer-to-layer alignment) also more mask levels need to be measured. Accordingly, the alignment mark size needs to become smaller, to fit more marks into the scribelane. For an in-direct alignment scheme, e.g. a scheme that aligns to another layer than the layer to which overlay is being measured, alignment mark stacking can provide solutions.

Simultaneously there is a requirement to reduce the alignment mark sub-segmentations without compromising the alignment and overlay performance. Smaller features within alignment marks can prevent processing issues like erosion, dishing and contamination. However,

when the sub-segmentation size within an alignment mark becomes comparable to the critical dimension, and thus smaller than the illuminating wavelength, wire-grid polarization effects start to occur. Polarization effects are a challenge for optical alignment systems to maintain mark detectability. Nevertheless, this paper shows how to actually utilize those effects in order to obtain enhanced alignment and overlay performance to support future technology nodes.

Finally, another challenge to be met for new semiconductor product technologies is the ability to align through semi-opaque materials, like for instance new hard-mask materials. Enhancement of alignment signal strength can be reached by adapting to new alignment marks that generate a higher alignment signal. This paper provides a description of an integral alignment solution that meets with these emerging customer application requirements. Complying with these requirements will significantly enhance the flexibility in production strategies while maintaining or improving the alignment and overlay performance.

6518-70, Session 14

Algorithm for lithography advanced process control system for high-mix low-volume products

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Lithography advanced process control systems (APC) have been developed, introduced into LSI production lines, and are playing a major role in improving CD and overlay (OL) variation, and productivity. Lithography APC has worked quite well for continuously processed product lots because of the wealth of historical data that can be used to predict the trend in the lots. However the bigger the increase in the number of small-volume products, the lower the productivity and controllability of CD and OL become. Productivity goes down due to the increase in overheads in changing masks and the increase in the rework rate caused by the uncertainty of APC prediction for the first lot of a new product. In general, to predict the optimum exposure dose and alignment offset for a product lot by lithography APC, the trends of CD and OL in the product lot must be known. For a new product lot, however, there is no trend. Poor prediction forces a send-ahead, or results in a reworking of the product lot. Both deteriorate productivity. This productivity-related problem is becoming more serious, especially in a fully-automated line. To overcome this difficulty, we have developed a suitable algorithm for lithography APC. The algorithm consists of an analysis of the attributes of the product and data processing of the process control parameters based on similarity in attributes. We have confirmed that this new algorithm is quite effective in improving productivity.

6518-71, Session 14

Advanced process control with design-based metrology

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K1 factor for development and mass-production of memory devices has been decreased down to below 0.30 in recent years. Process technology has responsed with extreme resolution enhancement technologies(RET) and more complex OPC technologies. ArF immersion lithography is expected to remain the major patterning technology through under 35 nm node, where the degree of process difficulties and the sensitivity to process variations are to grow even higher.

Design for manufacturability(DFM) can help to lower the degree of process difficulites and advanced process control(APC) can help to reduce the process variations.

DFM and APC require much information from wafer side such as hot spot inspection results and total CDU measurements at the lot, wafer and field.

In this work, we discuss new design based metrology which can compare SEM image with CAD data and measure the whole CD deviations from the original layouts in a full die. It can provide the whole CD distribution diagram of various transistors as well as cell layout. So, it is possible to analyze the root cause of the CD distribution of some specific transistors or cell layout, such as mask CDU, lens aberrations or etch process variation and so on.

6518-72, Session 14

Investigation of optimized wafer sampling with multiple integrated metrology modules within photolithography equipment

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Micron Technology, Inc. explores the challenges of defining specific sampling scenarios for the user of multiple integrated metrology modules within a photolithography track. With the introduction of integrated metrology into the photolithography track, the user is faced with the challenge of determining the type of data collection required to adequately monitor the photolithography tools and the manufacturing process. Photolithography tracks have a Metrology Block, capable of integrating three metrology modules into the standard wafer flow. Taking into account the complexity of multiple metrology modules and varying across-wafer sampling plans per metrology module, the user must optimize the module wafer sampling to obtain their desired goals. The user must also understand the complexity of the track handling systems to deliver wafers to each module. Track systems typically process wafers sequentially through each module to ensure consistent processing. In these systems the first wafer must process through a module before the next wafer and the first wafer must return to the cassette before the second wafer. Integrating metrology modules within this type of system can reduce throughput and limit flexible wafer selections. The user must also have the capability to select specific wafer sampling to each integrated metrology module. This case study explores optimizing wafer sampling plans and identifies limitations with the complexity of multiple integrated modules, for maximum metrology throughput without impact to the productivity of processing wafers through the photolithography cell.

6518-73, Session 14

Advanced lithography parameters extraction by using scatterometry system

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As the advanced IC device process shrinks to below sub-micron dimensions (65nm, 45 nm and beyond), the overall CD error budget becomes more and more challenging. The impact of other lithography process parameters other than exposure energy and defocus on final CD results cannot be ignored any more.

In this paper we continue the development of an advanced control system, which can be used to detect, classify and correct up to 5 lithography parameters. Sets of focus exposure matrix (FEM) models are first set up with different DOE process conditions split. And photoresist profiles of specially designed scatterometry CD mark are then fitted to models (Neural Network Model or standard polynomial model). Based on these calibrated models, not only exposure and defocus but also PEB, Lens aberration, etc. can be estimated. This approach utilizes information of resist CD, height, sidewall and feature dependent bias to classify different lithography parameters and therefore can give more accurate estimation of lithography parameters like energy, focus, PEB, spherical aberration and coma aberration. And the new approach does not need phase shift mask or other specially designed mark and can be used by most of mass production Fabs and used for process monitoring and matching on inline production wafer.

6518-74, Session 15

A methodology to evaluate critical-dimension uniformity control for sub-32-nm technology

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Critical dimension (CD) control is one of the key requirements for manufacturing integrated circuits. For the 32 nm node, the 2005 International Technology Roadmap for Semiconductor (ITRS)1 specifies a resist requirement for gate resolution and gate CD control (3sigma) of 1.3 nm, and a total gate length variation (3sigma) of 1.56 nm.

Manufacturable solutions to meet these specifications are currently not known.

CD uniformity control becomes more and more statistically limited with the continuous aggressive scaling of transistor gate width. In the limit where line edges are self-affine, correlation length and fractal dimension are two parameters that affect the roughness contribution from a given spatial frequency in addition to the line edge roughness (LER). In this paper, we will present a fundamental study of the effect of these factors on CD variation.

Usually power spectral density (PSD) (which is a function of roughness,) correlation length , and fractal dimension are used to simulate the line edges2,3. Corresponding experimental line edges can be extracted from SEM images of real transistors. In our simulation, for each gate width, over 10 thousand line edges are generated with PSD for specified LER, Lc, and fractal dimension. We have learned that CD variation not only depends on the LER, but also on Lc. The larger Lc, the more CD variation across the chip will be. The relationship between CD variation and Lc could become exponential as the gate width scales comparably to Lc. If LER and Lc can be regarded as independent parameters, then there are two ways to reduce the CD variation: One is to reduce LER, the other is to reduce Lc.

We will present the simulation method and results in detail. Resist exposure, PEB and development models will be used to discuss how the lithographic process may influence Lc, thus providing insight on CD uniformity control.

6518-75, Session 15

Predicting electrical measurements by applying scatterometry to complex spacer structures

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Scatterometry has for years demonstrated its ability to accurately measure simpler structures, such as those found in the Shallow Trench Isolation (STI) and gate modules. Demonstrations of scatterometry's ability to accurately measure more complex structures have been considerably fewer. This is understandable, as scatterometry modeling has progressed from the capability of measuring simpler structures several years ago to the capability of measuring very complex ones only very recently. While scatterometry suppliers are exerting a pushing force for more complex structures, IC manufacturers are exerting a pulling force, demanding ever more complex capabilities to enable the monitoring and control of ever more sophisticated structures. Validation of these scatterometry measurements remains as important as ever. Many methods exist to independently validate scatterometry measurements, but perhaps the most useful of these methods comes from electrical testers. Spacers make up one category of complex structures that scatterometry is now addressing. They are important because of the influence they have on multiple device characteristics. Thus, being able to predict device performance by measuring spacer structures in-line can lead to improved device performance and yield. Here we present the application of scatterometry to a complex spacer structure that is dominated by a nitride film. We correlate the scatterometry measurements to those from XSEM. Such measurements include the pulldown of the spacer from the top of the gate, the thickness of the spacer film, and the width of the spacer at the bottom. We also correlate various scatterometry measurements to electrical measurements of relevant parameters, such as gate resistivity. Results show that the scatterometry measurements correlate well to both XSEM and electrical measurements, thus demonstrating that scatterometry can be a reliable measurement technique for improving spacer controls and reducing the mean time to detect (MTTD) profile abnormalities. Because of this, the scatterometry measurements can be used as a predictor of electrical performance significantly before the electrical test occurs.

This paper describes measurements applied to both NFET (figure 1) and PFET (figure 2) structures. These 90 nm node structures are significantly different from each other because the PFET contains an extra oxide film over the nitride spacer that further complicates the measurement. Complexity arises not only from the multiple spacers and the SOI substrate, but also the implants of the gate and SOI. Despite the structural differences, we found that both FETs correlate well to electrical test measurements of gate resistivity and overlap capacitance. Furthermore, electrical measurements at multiple places in the process route were found to correlate to the scatterometry measurements.

6518-76, Session 15

Characterization of bending CD errors induced by resist trimming in 65-nm node and beyound

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Resist trimming is a technique that is often utilized in order to close the gap between line widths which can be repeatedly printed with currently available lithography tools and the desired transistor gate length. For the 65-nm node the resist line width delivered at pattern is between 60 to 70 nm while the final transistor gate length is usually targeted between 35 to 45 nm. The 15 to 25 nm CD (critical dimension) difference can be bridged by resist trimming. Due to the stringent gate CD budget, the resist trimming process ideally should have the following characteristics: i) no deterioration in CD uniformity; ii) no damage in pattern fidelity; iii) controllable CD trim rate with good linearity; iv) no degradation in LER (line edge roughness) or LWR (line width roughness).

Unfortunately, a realistic resist trimming process is never perfect. In particular, resist consumption and the resultant internal stress build-up during resist trimming can lead to resist line bending. The effect of the bending resist lines is a higher post-etch CD and significantly degraded local CD uniformity. The bending CD error is defined as the difference between the post-etch CD and the design CD due to resist bending after trimming.

In this paper, the following aspects of resist bending CD errors have been investigated: i) the relationship between bending CD errors and transistor layout; ii) the relationship between the bending CD errors and different 193 nm photoresists; and iii) the relationship between bending CD errors and the photo process parameters, such as resist CD target, resist thickness and different post-develop thermal bakes.

At the end of this paper, the presentation will be focused on how to reduce the bending CD errors. Based on available data, we will show that bending CD errors can be significantly decreased by minimizing the resist thickness or curing the resist pattern with a plasma treatment before trimming. Instead of resist trimming, BARC trimming and hard-mask trimming are also discussed.

6518-78, Session 15

Characterization of capacitive 3D deep-trench mask open structures using scatterometry

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Semiconductor manufacturing yield improvement demands tight process control using high precision, accurate, and high throughput metrology solutions. Spectroscopic Critical Dimension (SCD) metrology is successfully employed for characterization of a large number of electronic device structures in different development environments and production modules. The non-invasive technique is utilized to simultaneously characterize CD, sidewall angle, trench depth and film thickness. Furthermore, properties of buried layers can be characterized if interactions with the films are detected upon reflection of the incident light. Hence, thick transparent and semi transparent stacks, which may prove difficult to fully characterize using conventional CD-SEM and CD-AFM techniques, are routinely modeled and measured by SCD. Furthermore, electron microscopy cross-sectional imaging is useful for the characterization of most 2D structures; however, this imaging provides limited accuracy when characterizing elliptical 3D structures such as the Deep Trench Mask Open (DTMO) structure studied here. This structure consists of a dielectric film stack containing etched holes that have aspect ratios approaching 10 (Fig. 1). What makes this application challenging for scatterometry is not only its 3D shape, but also the presence of a double periodicity along one axis, creating a unit

cell containing two holes. Here we report on details of the characterization of wafers containing both lithography-induced and etch-induced variations. Accuracy investigations involve the use of Total Measurement Uncertainty (TMU) analysis, while utilizing a CD-AFM as a reference measurement system. Results show that the scatterometry measurements correlate well with the reference measurements. The DTMO structure consists of a thick Boron silicate glass (BSG), Si3N4, thermal oxide on silicon substrate. The etch time is chosen so that a silicon over etch region is created. Figure 2 shows the SCD MCD short and long axes results for one of the wafers in a notch right position. It is noted that measurements were done in both notch down and notch right wafer orientations. Larger sensitivity to critical parameters was found at the notch right position where the plane of incidence is normal to the short axis.

6518-79, Session 15

A novel CD-SEM approach to challenges in metrology accuracy

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The continuing trend of lithography capabilities to produce ever smaller features raises the relevance of the accuracy of the printed feature. Traditional metrology performance metrics focused mainly on precision are not sufficient anymore without a clear statement on the actual accuracy of the critical dimension measured. A study shows differences of up to 20nm between metrology tools of different kind or vendors. In this paper a novel approach to CD SEM metrology is introduced, that is focused on achieving adequate accuracy in addition to the traditional precision requirements. The methodology, denoted as “True CD” is correlated with complementary metrology techniques across litho and etches processes to validate the accuracy of the suggested approach.

6518-18, Poster Session

Dynamic sampling for advanced overlay process control

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Overlay metrology and control have been critical for successful advanced microlithography for many years, and are taking on an even more important role as time goes on. Due to throughput constraints it is necessary to sample only a small subset of overlay metrology marks, and typical sample plans are static over time. Standard production monitoring and control involves measuring sufficient samples to calculate up to 6 linear correctables. As design rules shrink and processing becomes more complex, however, it is necessary to consider higher order modeled terms for control, fault detection, and disposition. This in turn, requires a higher level of sampling. Due to throughput concerns, however, we consider this only on an exception basis based on automated trigger mechanisms. The result is real-time dynamic sampling, resulting in improved scanner control and lithographic cost of ownership. This study addresses the motivation and initial results for dynamic sampling and their application to higher order modeling.

6518-33, Poster Session

Application of perturbation methods in optical scatterometry

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Optical scattering techniques can provide rapid, non-destructive measurements of nanometer-scale structures for micro-fabrication process control. In general, these techniques compare measured optical characteristics of a sample to results generated from a theoretical model. These models can be computationally expensive, especially when used with iterative methods to obtain solution to the inverse problem. However, the structures of interest are normally restricted to small changes from some nominal structure.

A similar problem is encountered when designing photonic crystal devices. Photonic crystals are periodic index variations used to engineer the dispersion of optical materials. Planar photonic crystals can be fabricated using conventional microlithography techniques and can be similar to two-dimensional (2D) arrays of contact holes. Integrated optical devices such as waveguides, splitters, and resonant cavities can be created by introducing controlled defects into these arrays. Since analytic solutions for the optimal design of a particular photonic crystal device may not be possible, it is often necessary to solve for the dispersion curves of several closely related configurations to find the best result. Several investigators have applied perturbation theories from quantum mechanics to quickly generate new solutions from previously calculated dispersion curves. Perturbation theories have also been used to efficiently calculate the effects of defects, disorder, and side-wall roughness on the performance of photonic crystals.

In this paper, we apply perturbation techniques to scatterometry. The effect of small changes in the profile of a nominal test structure on the scattered field can be modeled by set of point sources. The distribution of these sources is a function of the fields in the nominal structure as well as the changes to the profile. This relationship can be expanded in a polynomial form. Often, only the first term of this polynomial is necessary for an acceptably accurate solution, making the calculation much simpler. The fields due to these point sources can be added to the nominal solution to obtain a new solution for the perturbed system. In general, this is less computationally expensive than calculating a completely new solution for each small change to the profile.

We use this technique to calculate the changes in the scatterometry signal due to side wall roughness. We investigate both linear gratings and two-dimensional arrays of holes. We also briefly discuss some of the unique challenges and opportunities for using optical scatterometry to measure the properties of photonic crystals.

6518-58, Poster Session

AFM characterization of resins for 193-nm photolithography

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The 2001 “International Technology Roadmap for Semiconductors” (ITRS), which defines the specifications and objectives to be reached for the next generation components for the microelectronic industry, introduced for the first time a new criterion the “Line Edge Roughness (LER)” of the photolithography patterns. These patterns are produced with the help of photosensitive resins, a key processing step in the semiconductor manufacturing. The best microlithography resins allow today LER of the order of 5 to 7 nm.

This microlithography pattern roughness limits the possibility to control accurately the length of the transistor gate increasing, thus, it’s leaking currents.

The aim of this research is to understand the physico-chemical mechanisms inducing the LER and optimize the synthesis and formulation of the photosensitive resins in order to reach acceptable values for this new criterion.

In order to achieve this goal, an interferometric lithography setup with 193 nm irradiation wavelength was built. The phase masks that were used make it possible to write grating with fringe spacing varying from 100 nm to 500 nm. This irradiation platform constitutes our reference irradiation set-up with which the resins can be compared. The patterned resins were characterized using Atomic Force Microscopy. Several modes were compared like contact, resonant and pulsed force mode. The interest of AFM measurement is to allow, in addition of the topographic characterization, to give access to information on the photoinduced modification of the resin.

We particularly focused on the roughness obtained on the written lines. In particular, we analyzed the effect of the resin composition, photonic parameters and curing aspects on the geometry of the patterns.

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6518-62, Poster Session

SEM metrology for advanced lithographies

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For many years, lithographic resolution has been the main obstacle for keeping the pace of transistor densification to meet Moore's Law. The industry standard lithographic wavelength has evolved many times, from g-line to i-line, deep ultraviolet (DUV) based on KrF, and 193nm based on ArF. At each of these steps, new photoresist materials have been used. For the 45nm node and beyond, new lithography techniques are being considered, including immersion ArF lithography and extreme ultraviolet (EUV) lithography. As in the past, these techniques will use new types of photoresists with the capability of printing 45nm node (and beyond) feature widths and pitches.

This paper will show results of an evaluation of the critical dimension-scanning electron microscopy (CD-SEM)-based metrology capabilities and limitations for the 193nm immersion and EUV lithography techniques that are suggested in the International Technology Roadmap for Semiconductors. In this study, we will print wafers with these emerging technologies and try to evaluate the performance of SEM-based metrology on these features. We will conclude with preliminary findings on the readiness of SEM metrology for these new challenges.

6518-77, Poster Session

Across-wafer CD uniformity control through lithography and etch process: experimental verification

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Across wafer gate critical dimension (CD) uniformity, which impacts chip-to-chip performance vis-à-vis speed and power, has become increasingly stringent at the 90nm technology node and beyond. In order to improve across-wafer CD uniformity through the litho and etch sequence, we proposed [1] tuning across-wafer PEB temperature profile to compensate for various upstream and downstream systematic spatial CD perturbations. Our previous simulation, modeling and preliminary experimental work [1] demonstrated the promise of this approach. Due to the portability and fidelity of temperature-to-offset model of PEB bake plate, we used this model in conjunction with the resist CD PEB sensitivity to optimize the PEB bake plate settings to reduce the post-etch CD variation.

This paper presents the experimental results for the final experiment, which consists of a characterization experiment and a verification experiment. The characterization experiment for the lithography and etch process extracted baseline signatures of post-develop (DI)CD, post-etch (FI)CD and plasma etch bias. Two PEB hot plates were used, with each plate used on half of the wafers, and this aimed at examining PEB plate matching on DICD & FICD. The characterization experiment was repeated one week later to capture possible drift of DICD, FICD and etch bias signatures. Systematic spatial signatures are seen in FICD, DICD, etch bias, and the signatures are approximately stable across one lot and from week to week. The strong statistical correlation of baseline signatures between wafers across one lot and from week to week also demonstrated the stability of baseline FICD, DICD and etch bias. This validates the legitimacy of our choice to treat the baseline DICD, FICD and etch bias signatures as systematic, stable and observable disturbances.

Using a two-week-averaged baseline FICD and etch bias signatures as well as the extracted resist PEB sensitivity, the temperature profile of the PEB plate adjustment was calculated using the proposed approach, and verification wafers were patterned to verify the efficacy of proposed post-etch CDU control approach. The measured optimal FICD had around 1nm less in variation than the baseline FICD, amounting to an approximately 40% decrease. Considering that more than 6 months time lag between the characterization experiment and the FI CDU control verification experiment, the achieved FI CDU improvement is truly promising. The FI CDU control results were also verified by examining the across-wafer PEB profile change and the tuned across-wafer DICD map. PEB profile change strongly correlates with DICD/FICD change, and the tuned DICD map strongly correlates with etch bias signature, which also validates the efficacy of the proposed control approach. Additional CDU improvement could be achieved if integrated metrology is available to shorten the time lag between the baseline characterization and PEB profile adjustment. The error budget analysis will evaluate the impact of the model limitations on the final CD control performance.

Reference:

[1].Q. Zhang, P. Friedberg, C. Tang, B. Singh, K. Poolla and C. Spanos, "Across-wafer CD Uniformity Enhancement through Control of Multi-zone PEB Profiles", Proc. Of SPIE, Vol. 5375, 2004.

6518-80, Poster Session

Image analysis of alignment and overlay marks with compound structure

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Decreasing of node size significantly increases requirement to overlay precision. Complex structure of target demands using of compound structures of overlay mark, which usually contain features with acute sidewall angles, coated by several layers. In this paper the possibility and limitations of image-based overlay with compound structures with overlay mark and coating layers are analyzed in detail. Dependence of overlay signal shape on overlay offset is considered. Structures with asymmetric sidewall angle, non-uniform thicknesses of layers and curved shape of layer borders are examined. Influence of thickness variation, difference between left and right sidewall angles of asymmetric shape and curvature of layer borders are investigated. For the simulation of such complex structures of overlay marks, our in-house simulator based on rigorous coupled-wave analysis (RCWA) module is used. Maximum allowed values of these parameters are studied in order to determine the limitations of image-based overlay.

6518-81, Poster Session

Methodical approach to improve defect detection sensitivity on lithography process using DUV inspection system

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Adoption of immersion technology to enhance the resolution of current wavelength gives rise to large concerns about defect controllability on lithography process. Along with aggressive design rule shrinkage k1 factor of lithography process is close to below 0.3 and this low k1 factor process results in very tight process window. Therefore requirements of sensitive defect detection on lithography step are grown with the adoption of new concept and low k1 regime processing.

On optical wafer inspection the signal of defect is closely related with wavelength regardless of its perspectives - Bright field and Dark field. Defect signal through bright field is enhanced through higher resolution imaging where the resolution is proportional to λ/NA. On the other hand defect signal through dark field is governed by famous Rayleigh equation which also requires shorter wavelength to get high defect signal.

In this paper we would like to report significant improvement of defect detection sensitivity on lithography process inspection through step by step trace of the defect formation and shape. Throughout the process flows till final etch and cleaning process from lithography the SEM non-visible defects or buried defects on lithography step are turned into line open or line thinning which are killer defects and has low defect signal on cleaning step.

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6518-82, Poster Session

Etch process monitoring by electron-beam wafer inspection

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Electron beam inspection (EBI) of wafers has been widely shown to be a powerful tool for random defectivity on wafers, particularly for sub-surface electrical defects that cannot be seen by optical tools. Some types of systematic defects, such as subtle under- or over-etch of contacts, can be difficult to catch using traditional die-die or cell-cell comparison because all contacts may be similarly affected. In this paper we investigated methods for catching systematic process defects using EBI.

We used a design of experiment where different dies on the wafer were etched using a total of 4 different etch parameters. The dies were selected by using multiple resist coat, pattern, and etch steps at a single contact layer. A total of 3 wafers were given the same process treatment. Following the etch steps, one wafer continued through the fabrication process to final test , one wafer was inspected using an eS31 electron beam wafer inspection tool, while the third wafer was held in reserve. The initial inspection did not show any significant difference in defectivity between the dies, although final bit test did show pseudo-systematic defectivity depending on etch process condition. The wafer was then inspected on an eS32 tool using a special e-beam preconditioning step to enhance the contrast of subtle under-etched contacts. In this case, we were able to pick out a defectivity corresponding the etch condition of each die. The in-process defectivity found by the electron beam inspection tool matched well with the end-of-line bit failure map.

In summary, subtle systematic etch process variations were detected by varying the etch process parameters across a single wafer, and tuning the electron beam inspection sensitivity to maximize contrast for subtle etch variations. Such techniques can be a powerful tool for optimization of etch process recipes to minimize wafer electrical defectivity.

6518-83, Poster Session

Immersion-induced defects SEM-based library for fast baseline improvement and excursion monitoring

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Immersion lithography offers great benefit for 65nm and below processes but at the same time posses a great challenge. Along with hyper NA values, which increase the scanner resolution, a new type of imaging process related defects emerged. New defects emerged related to water, top coating, resist and BARC. A Root cause analysis of the so-called wet defects (immersion) versus the so-called dry defects (non immersion) becomes crucial for defect reduction program. Manual and eventually automated classification can be used to analyze the data and monitor base lines. Furthermore, a robust automatic Defect Classification (ADC) increases productivity and decreases the wafer cycle time.

This article outlines a methodological approach for wet and dry defect classification, based on signatures analysis and rule based ADC, enabling generation of an immersion induced defect library for fast base line improvement and excursion monitoring. The article is written in collaboration with ASML using Applied Material SEMVision G3 automated defect analysis tool.

6518-84, Poster Session

Classification of backside defects using wafer ADC with spatial pattern recognition

A. P. Carlson, Rudolph Technologies, Inc.

Defects on the front and back surfaces wafers during processing can be either tool or process-induced. Tool-induced scratches, process-induced contamination, or residues on the back of wafers, often have a unique signature, such as a repeatable scratch caused by wafer handling equipment, or a chuck imprint on the backside of a wafer.

Automatic Defect Classification (ADC) is the process of categorizing defects found by inspection equipment into one of several defect classes. Spatial Pattern Recognition (SPR) is a method of comparing defect patterns at the wafer level with known defect signatures stored in a library that is created from process data. These defect signatures can represent systematic issues with process tools, handling equipment, or the process itself.

This paper describes the steps of an inspection method for identifying wafers with both known and new spatial pattern signatures. By reporting frequency of each signature category, process partitioning can efficiently trace the source of these problems. In addition, new defect signatures can be automatically learned and added to the library. This method allows for migration to an increasingly automated method to monitor process and tool-related excursions, classify defects, determine root causes, and take corrective action, while reducing the amount of human interaction required.

6518-85, Poster Session

Novel technology of automatic macro inspection for 32-nm node and best focus detection

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We had developed Novel Inspection Technology (1) for the next generation automatic macro inspection. With this technology, CD and LWR variation were detected as the polarization fluctuation, and converted into the image gray level.

To know the future possibility of this technology, it is very important to verify the detection sensitivity on the next and further generation wafers. We analyzed the detection sensitivity on down to hp 32nm patterns by the vector simulation tool.

On the other hand, we evaluated this technology with hp 55nm production wafers, and found that this technology enables to detect 10% line width variation as a defect. The test result was consistent with the prior simulation result. This fact not only proved the capability of this technology on hp 55nm process, but also suggests the effectivity on hp 32nm process.

This technology is also useful for Best Focus Search. Up to now, Best Focus Search has been done by an SEM, and it takes a long time. With this technology, it enables to reduce the time drastically. This technology, the polarization fluctuation becomes maximum in best focus. Best Focus Search is available by applying this feature. The time to search the best focus is to be Sixtieth compared with an SEM.

(1) T. Omori, K. Fukazawa, T. Mikami, K. Yoshino, Y. Yamazaki, “Novel inspection technology for half pitch 55nm and below”,

Metrology, Inspection, and Process Control for Microlithography XIX , Proc. SPIE Vol.5752, pp174-182, 2005

6518-86, Poster Session

Results from a new die-to-database reticle inspection system

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A new die-to-database high-resolution reticle defect inspection system has been developed for the 45nm and below logic nodes and the comparable memory nodes. These nodes will use predominantly 193nm immersion lithography although EUV may also be used. Many different

reticles types may be used for these nodes including: COG, simple tri-tone, complex tri-tone, high transmission, dark field alternating, enhancer, CPL, and EUV. Finally, aggressive model based OPC is typically used which includes many small structures such as jogs, serifs, and SRAF (sub-resolution assist features), with accompanying very small gaps between adjacent structures. The architecture and performance of the new inspection system is described. This new system is designed to inspect the aforementioned reticle types in die-to-database mode. Die-to-database inspection results are shown on standard programmed defect test reticles, as well as advanced 45nm and 32nm node reticles from industry sources; results show high sensitivity and low false detections being achieved. Direct comparisons with prior inspection systems show measurable sensitivity improvement and a reduction in false detections.

6518-87, Poster Session

Optimization of wafer fab contamination inspection methodology for sub-65-nm node reticles

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Contamination inspection can be divided into two distinct operating cases, 1) mask shop out going quality control / wafer fab incoming quality assurance and 2) wafer fab reticle re-qualification within the litho cell. In the first case, 100% defect capture rates at a specified defect size, has been and continues to be the objective of the implemented methodologies. In the second case, the objective is to detect changes in reticle quality resulting from issues such as progressive defects (i.e. crystal growth) during production use that could impact integrated circuit performance and yield.

This paper focuses on the differences between the two operating cases and the implications on inspection system hardware implementation. System tradeoffs and resulting performance are discussed.

6518-88, Poster Session

Inspection sensitivity improvement through optimization of lobe blocking on high-end memory devices

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As cell size of advanced memory is reaching to around 50nm hence the size of defect is required to be detected is less than 30nm. In the array area the best combination of the inspection tool that can be achieved the maximum sensitivity through optics based is short wavelength, small pixel and dark field perspectives when the noise from pattern can be blocked. To block the pattern noise efficiently and having enough defect signal to detector laser illumination is better approach than broadband lamp where lobe formation and light intensity is problematic.

UVisionTM 3D channel was evaluated on array area of advanced memory design rules. Below 100nm node design rule few pixels 3D channel can successfully suppress the Customized Light Collection (CLC) lobe which is a collective reflection light from array pattern.

In this paper we would like to report significant improvement of defect detection sensitivity with higher throughput that is up to 3 to 6 times faster than conventional bright field imaging inspection. In addition to this to enhance the defect signal customized CLC lobe block was developed to maximized the defect collection angle and showed improvements on defect detection. Because of CLC lobe suppression's inverse relationship with device design rule the results show that the smaller design rule is the better sensitive result.

6518-89, Poster Session

Use of automated EBR metrology inspection to optimize the edge bead process

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Accurate placement of the edge exclusion region is critical to maintaining edge die yield. Variation in film overlay in the edge exclusion region can lead to yield-limiting defects. Edge Bead Removal (EBR) metrology or Wafer Edge Exclusion (WEE) metrology describes a topside surface measurement of the wafer edge exclusion region relative to the wafer center and the wafer edge. This measurement is typically made at several points along the wafer's edge and often ranges between 0mm and 6 mm in width. In photolithography, EBR metrology data can be used to determine the repeatability of wafer alignment and the accuracy of EBR dispensing nozzles on the coat track.

In addition to EBR/WEE metrology, wafer edge inspection provides an indirect method to control the EBR process by detecting jaggedness of the EBR profile, scalloping, splashing, and other EBR line defects. Improper EBR can also create residuals on other edge surfaces that can lead to cross-contamination of wafers and handling equipment.

This paper describes a combined EBR/WEE metrology and wafer edge inspection method that can quickly detect EBR-related defects and characterize the quality of the EBR process. This data reveals the relationship between EBR-related defects and the quality of the EBR process, and can be used to make necessary adjustments to the coat track - and as a basis for wafer rework decisions. Proper tuning and monitoring of the EBR/WEE process allows for the eventual elimination of an entire class of EBR-related defects, thus significantly increasing edge die yield.

6518-90, Poster Session

High-throughput polarization imaging for defocus and dose inspection for production wafers

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Advanced 193nm lithography processes create a unique challenge for integrated device manufacturers (IDMs). As IDMs move towards more complicated, smaller line widths, the probability of manufacturing defects occurring increases. IDMs have traditionally utilized automated macro inspection tools to detect these process defects. However, these Macro tools have usually been designed to detect either large defocus-type defects or smaller particle-type defects, but not optimized to find defects at both ends of the size and contrast spectrum.

Rudolph approached the problem by integrating a unique polarization-imaging configuration, which greatly enhances detection of defocus-type defects without sacrificing the existing capability to detect other types of macro defects.

The improved inspection system demonstrated high sensitivity on detecting defocus-type defects, on multiple devices and processes, at high throughput. Results will be presented for a variety of processes down to 50nm line widths.

6518-91, Poster Session

Real-time spatial control of photoresist development rate

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Critical dimension (CD) is one the most critical variable in the lithography process with the most direct impact on the device speed and performance of integrated circuit. One exciting new challenge for process control is the development of control and optimization strategies that compensate for the non-uniform processing in one step (process) with that in another. An effective controller could work to resolve several integration problems, possibly speeding development time. The development rate can have an impact on the CD uniformity from wafer-to-wafer and within-wafer. Non-uniformity in the time to reach endpoint is the result of non-uniformity in film thickness, exposure dosage and resist chemical compound. This can in turn lead to non-uniformity in the linewidth. Conventional approach to control this process include monitoring the end-point of the develop process and adjust the development time or concentration from wafer-to-wafer or run-to-run. This paper presents an innovative approach to control the spatial uniformity in photoresist development rate in real-time by monitoring the photoresist thickness across the substrate.

In all the experiments carried out, commercial DUV resist SL4000 was spin-coated at 1500 rpm on a 4-inch wafer; soft baked at 100degC for 60 seconds and was subsequently exposed for 0.9 seconds. The developer solution used is CD-26, also from Shipley Inc. The wafer was then placed on a programmable bakeplate. The bakeplate consists of an array of independently controlled resistive heating elements with embedded resistance temperature devices (RTDs). This provides flexibility to influence the develop process through temperature manipulation of the bakeplate. The zones of the bakeplate can be configured easily depending on the application. A droplet of developer was then dropped on the site where film thickness was monitored using a spectrometer system. The spectrometry system comprises of a broadband light source, a spectrometer, and a bifurcated fiber optics reflection probe. The reflectance signals were then acquired by a computer.

To demonstrate the control strategy, the decreasing film thickness at two sites are being monitored and controlled to track a reference thickness profile as shown in Figure 1. The thickness profile can be generated using nonlinear curve fitting of the reflectance signals based on reflectance equation. With in-situ measurements, the temperature profile of the bakeplate is controlled in real time by manipulating the heater power distribution using conventional proportional-integral (PI) control algorithm. For our research, we not only use the in-situ resist thickness measurement to detect the endpoint of the develop process but also improve the resist development end-point uniformity from wafer-to-wafer. Figure 2 shows a typical conventional development process. Notice that the development rate is not uniform. In Figure 3, the proposed experimental setup is conducted, the resist thickness at two sites are monitored, noticed that the end-point at the two sites are the same. We have experimentally obtained a repeatable consistency in the time to reach endpoint given a reference develop profile, from wafer-to-wafer. An error of less than 5% in the time to reach endpoint has been achieved.

6518-92, Poster Session

A general predictive method to analyze spatial distribution of process variables

Y. Chen, VIGMA Nanoelectronics

As the minimum feature size of semiconductor devices is scaled down to 22nm (half-pitch) node, the CD variations have approached the maximum tolerable limit of +/-10% of the mean values. Even though there are some fundamental physical and chemical processes responsible for the observed variations, their interaction is so complex that a deterministic predictive model that can take all the relevant mechanisms into account is extremely difficult if not impossible. Nevertheless, the awareness of statistical characteristics of process variations is important for circuit/device designers to model the circuit/device behavior and estimate the process yield. Therefore, probabilistic methods based on multivariate statistics need to be incorporated especially when the devices continue to shrink down such that CD variations become comparable to its averaged values.

Principle component analysis (PCA) and canonical correlation analysis (CCA) are two important multivariate statistical techniques widely used in social sciences, biology, geophysics, meteorology, to name a few. In this paper, we introduce a PCA & CCA-based predictive method that can estimate a set of variable Y, e.g., discrete spatial distribution of a process variable on a field, based on a preceding observation of one or several different but correlated type of data set X.

The predictive procedure can be demonstrated with a CD distribution within a die as an example. Let us assume that we have collected resist CD values at I locations and substrate CD values (post-etch with a time delay Tau) at J locations within the same die, and totally N die samples have been measured. It should be kept in mind that the predictor data set does not need to be only one kind, e.g., resist CD as we shall use later. Rather it can be combined with many different types of process data such as bake temperature and dose variation distribution. Data vector X (x1, x2,..., xI) and Y (y1, y2,...,yJ) are concatenated together to calculate the (I+J) x (I+J) covariance matrix [C]. A CCA transforms above original raw data into sets of new variables, often called canonical variates, Wm and Zm, where subscript m=1, 2,..., minimum (I , J). Each pair of Wm and Zm is weighted linear combination of elements of the variation data vectors X' (x1', x2',..., xI') and Y' (y1', y2',...,yJ'), and the weighting coefficient for each element is ai (i=1,..., I) and bj. (j=1,..., J) respectively. Here, prime means the variation value with mean subtracted. The constructed pair of canonical variates Wm and Zm has decreasing correlation as m increases, and they are orthogonal to or uncorrelated with each other when their subscripts are different (e.g., W1 and Z2 are uncorrelated). In other words, based on previously collected raw data, two projection matrixes [A] and [B] can be constructed to project the variation data vectors (with the mean values subtracted) onto the corresponding canonical vectors. Moreover, simple linear regressions will relate the predictor canonical variate to the predictand variate.

Given a newly measured data vector (e.g., resist CD) on one die at a preceding time t, the projection matrix can be used to calculate the preceding canonical variates, which will then be used to calculate the delayed canonical variates with linear regressions. The delayed vector of Y (e.g., post-etch substrate CD) to be predicted can be synthesized from the delayed canonical variates with the projection matrix. Usually, when the sample sizes N is not much larger than the site number (which is often the case in semiconductor processing), we need to use the so-called principle components of raw data for above analysis. Principle component analysis (PCA) is also a multivariate statistical technique which finds orthogonal elements of raw data. That is, formed by a linear combination of the original elements, each PCA element is uncorrelated with each other and the leading elements contain most of the information of the original data. We shall demonstrate the proposed method with a set of real-time data from IC industry.

6518-93, Poster Session

Advanced process control for hyper-NA lithography based on CD-SEM measurement

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In the next generation advanced lithography, optical system with numerical aperture (NA) of 1.0 or larger is realized using immersion lithography and that with NA of 1.3 or larger, which is referred as Hyper NA, is realized with the use of high refractive index liquid. However, there are problems such as unfavorable polarization in the optical path of exposure tool and extremely shallow focus depth. In particular, the focus depth closely relates to the allowable exposure error range and greatly influences the critical dimension and the shape of photo resist patterns. For process engineers, the evaluation of such influences is required in optimizing process condition and selection of suitable material. A method used generally for examining the process reaction defines Process Window (PW) from Focus Exposure Matrix (FEM). Due to very shallow focus depth, accurate PW evaluation using the conventional method will become difficult in next generation lithography, that is to say, in the Hyper NA generation. If PW evaluation is not accurate, it is possible for process optimization and material selection to be incorrect. In order to prevent such problem, it is necessary to use patterns with dimensions that resemble the actual patterns for FEM measurements in addition to along with conventional line and space patterns. In other words, PW analysis using Hot Spot, which is a site very sensitive to process variation, is necessary. This means that in the next generation lithography measurement, local measurements by CD-SEM must be combined with global tendency measurement across a wafer by OCD.

MPPC (Multiple Parameters Profile Characterization) method (1) is a technology that numerically measures the change in the resist pattern shape Using MPPC, this research aims to increase the accuracy of PW against the conventional method that uses only the critical dimension (CD) measurement at the bottom position of the resist shape (bottom CD: BCD). Further more, improvements in measurement reproducibility of PW is aimed by combining MPPC with ACD (Averaged CD) method, which is a method that measures and averages a number of patterns in an image to improve measurement reproducibility. MPPC is a function that quantifies a cross sectional profile into a number of indices lists from the secondary electron profile measured by CD-SEM. The MPPC indices define terms such as PCD, TCD, TRD, and BFT. By using the

averaged value of MPPC indices with conventional BCD or the averaged measurements of Hot-Spot pattern with line and space patterns, it is possible to visually represent PW of a higher practicality and measurement reproducibility.

In this paper, PW evaluation with high reproducibility by CD-SEM for next generation lithography with Hyper-NA will be presented. Potential capability of CD-SEM and MPPC for future measurement technology will be discussed.

6518-94, Poster Session

Application of integrated scatterometry (iODP) to detect and quantify resist profile changes due to resist batch changes in a production environment

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Due to decreasing critical dimension (CD) tolerances and lithographic process windows for increasingly smaller geometries, it is becoming critical that the smallest deviations in the lithographic process be detected in real time and corrected immediately to ensure minimal impact on product yield, rework, and cycle time.

One cause of process deviation is a resist batch change. Some effects of resist batch changes are well understood and controlled, such as the slight CD variations that can be corrected with a change in exposure energy via a feedback system. Another effect can be an unexpected change in the resist profile, which is normally not detectable with a top-down CD-SEM measurement and can produce an unpredictable etch delta. In processes where the normal resist profile is re-entrant this can lead to an out of control post-etch CD and ultimately to yield loss. Using the Tokyo Electron Clean Track(tm) integrated scatterometery solution (iODP), the change in resist sidewall angle can be detected during a resist batch change.

This paper will quantify the magnitude of the change in sidewall angle for an ARF resist, explain how iODP allowed additional controls to be placed on incoming resist, and discuss cost savings made possible as a result of this work.

6518-95, Poster Session

Litho cell control using MPX

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Due to an ever shrinking DOF budget optimal lithographic process control involves a closely coupled combination of test wafer and product wafer characterization as well as internal focus control methods. It has been shown in previous work that MPX (Monitor Photo Excursion) optical technology for line-end-shortening metrology of focus and dose provides a reliable and low cost product monitor solution. In this work we apply MPX technology to litho cell monitor and control on test wafers. Focus-exposure matrix (FEM) wafers are measured and analyzed automatically on a routine basis. Process window parameters are tracked over time by scanner, including spatial analysis of results across the scanner field such as tilt and curvature. These MPX results will be compared to CD SEM and internal scanner focus control methods for correlation and accuracy. Improvements in litho cell control are also discussed.

6518-96, Poster Session

Data sharing system for lithography APC

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Advanced process control (APC) systems have become a must for introduction into the critical process stages of semiconductor production lines. Usually APC servers are installed in every factory and are independent of each other. We frequently need to ship production lots or experimental lots in process to another factory in order to raise or balance productivity, or to process the lot using specific equipment. In such cases, it is important to share historical data on the product between factories in order to carry out lithography APC precisely. To solve this problem we have developed two new types of inter-APC data-sharing systems for lithography APC systems. The first sharing system is for sharing data on the processing history, and the other is for sharing mask data. The mask data sharing system consists of one mask information data server and one lithography APC server. Mask information described in a common format is obtained via a wide area network (WAN) from the mask vender and stored in the mask information data server. This information is periodically transferred to the database on one specific lithography APC server. This lithography APC server periodically delivers the mask information to every other lithography APC server. The system that shares the data on the processing history consists of a function for delivering the processing history data. In shipping a product lot to another factory, product-related data on the processing history is delivered by the lithography APC server from the shipping site. Mask information and data on the processing history are used to predict the optimum exposure dose and alignment offset for the product. Development of this data-sharing system for lithography APC has enabled us to build a precise process control system for moving product lots between factories.

6518-97, Poster Session

CD measurement in flash memory using substrate current technology

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The most relevant phenomenon of this past decade in the field of semiconductor memories has been the explosive growth of the flash memory market, driven by cellular phones and other types of electronic portable equipment. The demand for accurate measurement of CD and electrical characteristics such as capacitance and resistance of flash memory is increasing as the size of the flash memory is getting smaller.

One of the difficult points for the measurement is the high aspect ratio of contact hole structure. It is difficult to measure the CD or shape of hole bottom with conventional CD SEM which is using secondary electron (SE) detector because the escape ratio of SE from high aspect ration contact hole is very low (<10 %). EB-SCOPE technology has been developed as one approach to solving this challenge. It offers a wide range of applications in monitoring semiconductor processes such as inspection of high aspect ratio contact and via holes. We can measure CD of floating and control gate by substrate current (SC) measurement method.

When we scanned e-beam to the surface of floating gate and control gate of flash memory, we got a SC profile which is totally different from the SE signal of CD SEM. In our system SC value is positive if electrons flow to substrate and minus vice versa. SC value show constant value when e-beam scan oxide region before touch the bottom of floating.

When e-beam starts to irradiate to floating gate, SEs emitted from the surface of floating gate and so positive charges (holes) generated around the surface of the floating gate and incident electrons are accumulated in below area of floating gate, the positive mirror charges are generated at the substrate by this polarization. So current is increasing at the first stage of e-beam irradiation to the floating gate.

As scanning is going on, the holes and electrons located in each area start to combine by electric filed between them and the net charges become positive and they are dominant finally in the floating gate because the SE yield is over 1 at low incident energy (~ 1 kV). The mirror charges at the substrate turn into negative charges and then when the voltage between and floating gate and substrate reaches to 10 V, the F-N (Fowler-Nordheim) current generated and electrons at the substrate flow to floating gate through oxide film. The current is decreased and the turns into negative finally. When the e-beam passes from the floating gate, the amount of FN current is decreased and then the current is going to zero point. The SC signal at irradiation of e-beam to control gate is lower than that of floating gate because the configuration of control gate and floating gate is the same as serial connection of two capacitors and then the total capacitance is lower.

We can know surface state of floating gate by as well as the bottom CD of flash memory fro this information.

We will suggest also the possibility of the measurement of the

capacitance and resistance of flash memory by measuring the slope of the signal and the time constant. From this analysis, we can know the electric characteristics as well as bottom CD without e-test after all process finishes. This technique can contribute yield enhancement in flash memory manufacturing process.

6518-99, Poster Session

Overlay metrology for dark hard mask process: simulation and experiment study

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As design rule shrinks in semiconductor devices, photoresist thickness is getting to thinner. Since photoresist is too thin as a pattern transfer mask, dark hard mask process is developed and being widely used. Dark hard mask subsequently serves as a pattern transfer mask for under lying films. Although the dark hard mask provides excellent etch resistance property, it is hard to make a good alignment since the extinction coefficient k of the hard mask is too high. As a result, the image quality of alignment and overlay marks under hard mask is significantly degraded.

In this paper, simulation and experimental study results are reported to solve this problem. For simulation part, an in-house simulator, which is based on rigorous coupled wave analysis and Fourier optics method of high NA imaging, is used. According to the simulation and experiment study, image quality of alignment and overlay marks can be optimized by choosing the thickness of hard mask and sub-film carefully for a given process condition. In addition, it is important to keep the specification of film thickness uniformity within a certain limit. Simulation results are confirmed by experiment using the state of art Flash memory process in Samsung R&D facility. Detailed simulation and experiment results are presented.

6518-100, Poster Session

In-chip overlay metrology of 45-nm and 55-nm process wafers

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The feasibility of measuring overlay using small (between 1x1μm and 3x3μm total size) targets has been demonstrated , . The symmetry of the image of isolated test features changes with overlay offset. The targets are small enough to be positioned within active areas of the device, and total measurement uncertainty (TMU) is sufficient to allow these targets to be used in characterizing overlay variations in the active device. In this paper we describe application of these targets to production wafers at 45nm and 55nm design rules.

In-chip targets were placed inside the device area of test wafers for a 45nm production process. Overlay was measured at two process steps - Poly to STI and Contact to Poly. The targets were placed at 120μm intervals along a horizontal line completely through the device area, and at the same spacing along a vertical line. Standard bar-in-bar targets were placed in the active area wherever possible. Measurements were made in multiple fields and from multiple wafers using an unmodified Nanometrics Caliper élan overlay tool. We will describe analysis of the data to reveal the systematic variation of overlay within the field by removing random and grid-scale effects, with results such as are shown in figures 1 and 2. Similar effects have been seen on all the layers tested.

Both the bar-in-bar and the in-chip target data show changes in overlay that cannot be explained by the linear or quadratic models of in-field scanner behavior that are normally used to link scribe-line overlay measurements to predictions of in-field overlay variation for the purposes of process control. The overlay variations are in the 0-10nm range, which means that, according to the 2005 ITRS, they account for nearly 100% of the overlay budget for a 45nm process.

Measurement of in-die overlay is made possible by the use of these very small targets. In order to allow characterization of overlay change within product die, not only must the targets be as small as possible but also they must be capable of packing as densely as possible into surrounding patterns. A space is necessary between the target and the surrounding device pattern but we will show that this need be no more than 1μm on each side. As a result the total device area required for each target is no lager than 5x5μm. We will report results obtained from even smaller targets.

The greater sampling density possible with the new in-chip targets makes the pattern of overlay variation much clearer than is possible with the large bar-in-bar targets. It would in any case not be possible to use the larger targets inside real product die. The data shows that overlay shifts discontinuously at the boundaries of large-scale pattern changes. This effect cannot be described by any model where overlay variations are purely a mathematical function of position, and in process control at this node it will become necessary to use characterization of overlay by measurement instead of models

6518-101, Poster Session

Evaluation of novel overlay targets for thin film head application

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Overlay control becomes more crucial for wafer processing in thin film head (TFH) industry, in order to achieve higher up to terabyte data storage capacity. High topographic feature and large transparent spacing between measured two overlay layers are unique challenges for TFH overlay measurement. It is important to know if overlay target does represent the true overlay and its effect to overlay control. In this work, three overlay targets, Box-in-Box (BiB), Frame-in-Frame (FiF) and KLA-Tencor Advanced Imaging Metrology (AIM), were evaluated under different process conditions. The key performance study of the overlay targets included: overlay precision and Tool-Induced-Shift (TIS) variability; effect of photo resist thickness from 200nm to ~5mm; effect of transparent dielectric spacing up to ~5mm between two overlay layers; overlay mark fidelity (OMF) from array test; analysis of stepper correctable parameters and their residuals. Tool matching is another important factor for overall overlay tool capability. We also compared matching response by different overlay targets.

6518-102, Poster Session

Through-focus technique for overlay metrology

A. Liu, Y. Ku, Industrial Technology Research Institute (Taiwan); N. P. Smith, Nanometrics Inc. (Taiwan)

Optical overlay metrology is thought to face the challenges in precision improvement with edge-determination based algorithm because the design rule is gradually decreasing in advanced semiconductor process. We develop a novel algorithm for determining the overlay error of grating structures with an optical bright-field imaging tool. It is a continuous developing work of the through-focus method that has been studied in our previous work for enhancing overlay tool performance to measure pitch and CD. By evaluating the intensity variation of the different acquired images through the analysis of the optical images obtained at different defocus positions, the analysis curves of the focus measure versus the overlay error experimentally demonstrate the nanometer sensitivity with the overlay of the grating structure.

When plenty of images of different target pattern captured with image sensor at different amounts of defocus position, the image intensity variation in each image can be calculated by focus criteria. We have evaluated several focus metrics for the image analysis of bright-field microscopy, including gradient energy, standard deviation, contrast, Laplacian, and etc. In our application, the standard deviation is the best metric of the image within the grating area because it discriminates the side lobe local maximum more sharply that is a key phenomenon in our algorithm application.

Four groups of 800 nm pitch overlay target patterns with fixed CD of 100, 200, 300 and 400 nm were designed and fabricated. The overlay offset with two layer grating structure was varied from 0 to 400 nm by 4 nm increment with keeping all other dimensions constant. The target pattern size is designed as 25 mm. The line-width of these test targets were verified with CD-SEM. The traditional BIB target with the same

varying overlay offsets were also designed and fabricated as a measurement comparison of the overlay of grating structure.

All experimental data were acquired by using an automated commercial overlay metrology tool with 0.3 condenser lens NA, 0.5 objective lens NA, and illumination centered at 550nm with 50nm FWHM. A series of defocus images were acquired by the CCD camera while the positioning stage are moved along the optical axis path and then saved as the image files for image analysis. Each image file is 512 x 512 8-bit gray scale image. The defocus positions were adjusted from -4 mm to +4 mm offset relative to the best focus position with the increment of 0.25 mm.

Empirical models were developed to fit the experiment results of image intensity variation versus overlay error. The experimental data show that the variations of the focus measure has nano-scale sensitivity to the overlay of the grating structure, so that it can be used to determine the overlay error by implementing the algorithm. Thus, the through-focus method has potential application in overlay metrology for the process control in future semiconductor manufacturing.

6518-103, Poster Session

Improvement of front-end process overlay in 60-nm DRAM

Y. Hwang, W. Ma, Hynix Semiconductor Inc. (South Korea)

ArF immersion lithography and RETs(Resolution Enhancement Technology) are the most promising technology for sub 60nm patterning. As device has shrunk, overlay accuracy has become more important by small overlap margin between layers. Overlay performance of immersion process is affected by thermal effect due to water evaporation so it can be worse than dry process and CD variation in DPT(Double Patterning Technology) process is affected by overlay performance. So improvement of overlay accuracy became hot issue in realization of future lithography technology, especially immersion process and double patterning process. Current status of the art lithography tool shows 10 ~ 12nm(3sigma) overlay control in front-end process, but this overlay performance is merely not sufficient for future technology.

In this paper, we investigated the causes of overlay variation and tried to improve overlay accuracy in front-end process of 60nm DRAM device. Therefore the results in this study can be implemented to new technology such as immersion and double patterning. First, overlay residual error factor is classified into two types, one is the equipment error factor and the other is process error factor. Major factor of equipment error can be divided into SCMV(Single Chuck Mean Variation) by stage accuracy variation, chuck to chuck mean and correction factor variation by using twin chuck etc. And major factor of process error can be divided into alignment signal variation by chuck defocus (stage particle by contamination), increase of overlay residual by material deposition, alignment key height variation by etch loading effect, overlay vernier attack by CMP(Chemical Mechanical Polishing) process etc. We analyzed causes of these overlay error factor and we applied new system and process to improve these overlay error factor.

In conclusion, we could understand what overlay error is come from and how to improve overlay accuracy in 60nm device, and we could get good overlay performance with using new alignment system and process optimization.

6518-104, Poster Session

Hardware materials and parameters optimization for improvement of immersion overlay

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Though immersion lithography is on the verge of starting mass-production, demerit in overlay controllability by immersion is thought as one of last huddle for that. The first issue in immersion tool has not been matured compared to dry tool. As design rule is getting smaller, overlay specification is also changing the same way. But immersion tool is not ready to meet this tighter overlay specification. The second issue is regarding the material that we use in immersion: top coat and water. Process details of material are needs to be verified thoroughly about how each parameter affect on alignment and overlay respectively. In this paper, we made an experiment about machine parameter split and investigate top coat effect on overlay. To improve overlay performance of immersion, we analyzed machine parameters: scan-speed, settling time, UPW(Ultra Pure Water) flow, air-shower pressure etc. And we made an experiment how the effect of top coat is appeared on overlay through simulation and experiment. In the experiments, we used ASML 1400i & 1700i scanner. Resolution improvement of immersion tool has been proved by lots of papers, but it is need to be verified of overlay controllability that getting tighter. Continuously we believe that most efforts are to be focused on overlay control issue

6518-106, Poster Session

In-die overlay metrology performance study for 45-nm design rules and beyond

Y. Avrahamov, M. E. Adel, P. Izikson, KLA-Tencor Corp. (Israel)

Layer to layer alignment in optical lithography is controlled by feedback of scanner correctibles provided by analysis of in-line overlay metrology data from product wafers. There is mounting evidence that the “high order” field dependence, i.e. the components which contribute to residuals in a linear model of the overlay across the scanner field will likely need to be measured in production scenarios at the 45 and 32 nm half pitch nodes. This is in particular true in double pitch patterning scenarios where the high order reticle feature placement error contribution to the in-die overlay is doubled. Production monitoring of in-die overlay must be achieved without compromise of metrology performance in order to enable sample plans with viable cost of ownership models. In this publication we will show new results of in-die metrology, which indicate that performance comparable with standard scribeline metrology required for the 45 nm node is achievable with significantly reduced target size. The capability roadmap of the Archer tool family will be discussed, including specific features which are required for production worthy in-die metrology to be enabled.

6518-107, Poster Session

Say good-bye to DOF: statistical process window analysis with inline lithographic process variations

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In this paper we present one application of our new Advanced Lithography Parameters Extraction (ALPE) system in the lithography process window analysis.

Compared with traditional DOF/EL based process window analysis or Monte Carlo approaches with pre-assumed process variations, our new approach uses real-life process variations (exposure, focus, and even PEB temperature, etc. if needed) collected by the new ALPE system. Different from pre-assumed process variations and independently measured process variations, all these process variations are directly correlated with inline CD variations, so we call them real-life process variations. Based on these real-life process variations, the estimation of final CD uniformity will be more accurate and objective.

6518-108, Poster Session

Use in-line AFM as LWR verification tool in 45-nm process development

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Because the critical dimension shrink to fit advanced process generation requirement, line width roughness (LWR) became more and more important.

As design rules for semiconductor devices shrink, the Line Width Roughness approaches the CD of the line itself. This leads to poor device performance or even device failure. Thus, an accurate process monitor for LWR is required.

CD-SEM measurements for LWR require a reference to verify the

accuracy. TEM has traditionally played this role. However, it's destructive nature, the errors induced by sample preparation, the limited data output and long turn around time make routine TEM measurements undesirable.

CD-AFM is non-destructive technique that is able to generate highly accurate 3 dimensional profiles of a sample surface over tens of microns in the X and Y directions with sub-nanometer resolution.

In this paper we present results that show strong correlation between CD-SEM, TEM and inline CD-AFM based on measurements of an OPC grating. Based on these results, the CD-AFM has successfully replaced the TEM as the reference tool of choice for 45nm R&D process generation.

To improve this situation, we success to adopt in-line X3D AFM to replace FA TEM method as the verify tool in 45nm generation process R&D stage.

The 50nm CD tip was used for this test, one through pitch grating pattern is designed for this OPC model test. In the mean time, we collect non-OPC and OPC data at the same time, the AFM results showed strong enough correlation among CDSEM, TEM and in-line AFM.

6518-109, Poster Session

Die-to-database verification tool for detecting CD errors, which are caused by OPC features, by using mass gate measurement and layout information

T. Kitamura, NanoGeometry Research Inc. (Japan)

In the SPIE conference in 2005, the Die-to-Database Verification Tool NGR2100 system, which enables detection of repeated defects on a SoC (System on Chip) device, has been introduced. Further, it has been mentioned that CD (Critical Dimension) uniformity among a shot or a wafer is measured by the NGR2100 system with a huge number of CD's. Furthermore, in the SPIE in 2006, FEM (Focus Exposure Matrix) analysis by using the NGR2100 has been discussed. Besides these applications, the NGR2100 system has many other applications, e.g. Process Window Qualification or the like. As one of applications, the NGR2100 system also enables detection of CD errors, which are caused by OPC (Optical Proximity Correction) features, on a memory device by using mass gate measurement and layout information. The key features of the application include high-resolution and high-speed secondary electron acquisition capability, a scan generator to acquire images of a large field of view, proprietary electron optics to eliminate field distortion over the wide scan field, automatic gates extraction function from a polycrystalline layer and an active layer of a layout data, and analysis of a gate widths for each gate classification.

CD errors, which are caused by OPC features, on a memory device are detected by the following procedure:

1. An image of gates to-be-verified is acquired at 100 M pixel/sec sampling rate.

2. A reference geometry corresponding to the image to-be-verified is generated from layout data by polygon ORing, clipping, and width correction. The reference geometry is represented by lines comprising of a line segment or a curve, and is compared with the image to-be-verified. Gates in a memory device are extracted by using the Boolean AND operation on polygons in a polycrystalline layer of a layout data and polygons in an active layer of the layout data. The gates are classified by directions, widths (CD), and lengths.

3. Edges are detected from the image to-be-verified by using a conventional edge detector.

4. Fast matching between the detected edges of image to-be-verified and the lines or curves of the reference geometry is performed.

5. Gate widths are measured from the image to-be-verified by using line profiles existing in the extracted gates.

6. A gate width distribution for each gate classification is obtained from the measured gate widths.

7. Gates which do not belong to the normal distribution are recognized as gates having CD errors caused by OPC. Even if gates have same directions, widths (CD), and lengths, the gates may have different OPC features. Therefore, the gate width distribution may include the various normal distributions.

8. The recognized CD errors are used for feedback to OPC features in order to improve a process window.

The procedure for over 3000,000 gates is performed in two hours, while a CD-SEM (Critical Dimension Scanning Electron Microscope) requires 21 days for the same procedure.

In some cases, peripheral circuits of a memory device have same feature, however gate width distribution of the circuits are different depending on positions. Further, there has been a tendency for gates having short lengths to have large widths.

Consequently, the Die-to-Database Verification Tool NGR2100 will also contribute to quicker TAT for memory devices, and make higher yield by improving a process window.

6518-110, Poster Session

Dynamic thermal dose management of the PEB step for dense-iso variation control

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For years lithographers have benefited from controlling the thermal dose during steady state PEB processing. Multi-zone hot plates have been developed to take advantage of the ability to tune CD by the PEB step. One of the remaining problems is the disparity of chemicals in the resist available to isolated versus dense features.

It has been shown that the transient ramp up phase of the PEB step can be engineered to minimize the variation of dense to iso CD. One key to this is highly accurate, highly responsive metrology with enough time granularity to capture the transient response phase. Such a measurement system is described in detail, with emphasis on how to utilize it to tune dense-iso CD variation via PEB transient dose engineering.

6518-111, Poster Session

Metrology setup to analyze systematic CD variation using scanning electron microscopy and scatterometry in sub-90-nm technology

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Control of Critical Dimension (CD) variation is extreme important in semiconductor manufacturing processes. To achieve excellent CD control, the nature of CD variation must be well understood. Recently, CD shrinkage of ArF photoresist is reported in case of using Critical Dimension Scanning Electron Microscopy (CDSEM) to measure CD in sub-90 nm lithography. This shrinkage would be one of main error factors of CD variation in ArF lithography if we do not apply any special solution, since the shrinkage of CD after lithography makes can not recover before etching process. It can be induce off-targeted CD by changing CD after lithography. Therefore, we need a new measuring strategy in ArF lithography to overcome the CD shrinkage and understand nature of CD variation. Due to nature of mechanism of the scatterometry, it is becoming more and more important as a inline metrology in ArF lithography. In this paper, we suggest a method to find an optimum sampling plan which gives better understanding for systematic CD variation when we use CDSEM and scatterometry. Finally, we will show excellent solution to achieve improved CD controllability by scatterometry.

6518-112, Poster Session

Major trends in extending CD-SEM utility

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Requirements for increasingly integrated metrology solutions continue to drive applications that incorporate process characterization tools, as well as the ability to improve metrology production capability and cycle time, with a single application. All of the most critical device layers

today, along with even non-critical layers, now require optical proximity correction (OPC), which must be rigorously modeled and calibrated as part of process development and extensively verified once new product reticles are released, using critical dimension-scanning electron microscopy (CD-SEM) tools. Automatic setup of complex recipes is one of the major trends in CD-SEM applications, which is adding much value to CD-SEM metrology. In addition, as integrated circuit dimensions continue to shrink, local linewidth variation influences the statistical confidence of a measured CD's representation of the process. A feature, called "AverageCD" measures multiple targets within the field of view (FOV). "AverageCD" allows not only measurements of a single data point representing one discrete feature, but sampling of the mean and variance of the process. These two applications, automatic recipe creation and "AverageCD," are combined in the second version of the DesignGauge software, which is available for the latest generation Hitachi S-9380II CD-SEMs DesignGauge V2 is not only capable of offline recipe creation and CD-SEM control, but also has the ability for direct transfer of design-based recipes into standard CD-SEM recipes. These recipes can be used for OPC model-building and verification as with previous DesignGauge applications, but the software also provides the option for design template-based recipe setup for production layer recipes. This ability yields much needed improvement to production tool utilization, as production recipes can thus be written offline for new products, improving first silicon cycle time, reducing engineering time required to generate recipes, and improving CD-SEM utilization. Another benefit of the application is an improvement in recipe robustness over conventional direct-image-based pattern recognition. This work will show an extensive evaluation of DesignGauge V2, including rigorous tests of navigation, pattern recognition success rates, SEM image placement, throughput of recipe creation, and recipe execution. The impact of "AverageCD" will also be evaluated.

[1] "Automated CD-SEM Recipe Creation-A New Paradigm in CD-SEM Utilization." B. Bunday , W. Lipscomb, J. Allgair (ISMI), K. Yang, S. Koshihara, H. Morokuma, L. Page, and A. Danilevsky (Hitachi High Technologies). 6152-1B, SPIE Microlithography 2006.

6518-115, Poster Session

Stochastic simulation of material and process effects on the patterning of complex layouts with e-beam and EUV lithography

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Future device generations will have to perform alterations in the layout based on process information to improve the overall profitability of the product. Given the increasing cost of IC fabrication, patterning simulation of the layout prior to tapeout should be carried out in order to facilitate the IC designers with more accurate data. Those data could be used for further layout optimization.

With these problems in mind, a home made stochastic lithography simulator, along with a EUV and an e-beam exposure-pattern-convolution module are integrated in order to result in a complete lithography simulator to account for high resolution layouts. The application of stochastic modeling techniques is preferred in the length scales probed with this simulator because all microscopic phenomena can be considered, through appropriate assignment of occurrence probabilities. This way it is also easier to incorporate new phenomena in the framework.

The first module of the simulation process is a 3-D Monte Carlo simulation of the electron transport for the particular resist-substrate system (i.e. scattering properties of materials, beam energy). The results of the point beam Monte Carlo simulation are convoluted with the beam diameter and the particular layout of interest. Along a corresponding line of work simulation of EUV exposure and secondary electron blur is performed.

The energy deposition from either e-beam or EUV simulation is used as input, along with the layout (CIF or GDSII format) of interest, for the calculation of the final energy deposition over the area under study. In this module the exposure strategy and experimental parameters (exposure dose, beam step size, etc.) are taken into account. At this level the energy deposition as a 3-D matrix over the area of interest is available. This energy deposition matrix is normalized and accounts for the photoacid generator (PAG) ionization probability. The rest of the simulation, e.g. reaction-diffusion and resist deprotection, and resist development, and etching, follow next. The effect of sidewall etching on the edges of the top down image is considered isotropic. The rough edges of the top down image constitute a boundary, whose evolution during etching yields by solving the Eikonal equation numerically using the fast marching method.

Currently 2-dimensional top-down simulations could be performed efficiently. The layout can be simple lines/spaces or even a complex single-layer layout of shapes which could be introduced into the simulation as a CIF file. The most CPU time consuming processes are the calculation of the energy deposition on the layout and the polymer chain distribution in the lattice.

The whole process could be useful in the validation of design rules taking into account line-edge roughness (LER) and for simulating the layout before actual fabrication for design inconsistencies. The effects of exposure, material and processes on layouts will be presented in this work using the above simulation approach. Particular examples of LER effects on complex layouts will be investigated.

In the current work the whole simulation process will be applied on the mask levels of an inverter layout and the metrology of critical dimensions and line-width roughness on the p and n-type transistors will be correlated with the exposure, resist material and processing parameters of the mask layers.

6518-116, Poster Session

Macro CD contact ellipticity measurements for lithography tool qualification

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Contact hole integrity is an important metric for IC manufacturers, which is reflected in tight ellipticity control as part of lithography tool qualifications

Current ellipticity measurement methodology is very sensitive to random process variations of the contact hole shapes. Determining systematic ellipticity poses a challenge on qualification productivity, as acquiring more data for statistical validity leads to unacceptably long measurement times. The introduction of MacroCD Vector measurement enables a single shot large sampling of contact holes, including vector calculation and averaging of all individual contact ellipticity results within the MacroCD measurement array.

Based on these enhanced measurement features, it is shown that contact hole ellipticity can be determined with much higher accuracy while local, mostly process induced, variations can be characterized simultaneously. This opens possibilities to study correlation between ellipticity and possible root-causes in the litho-chain.

6518-117, Poster Session

Sub-nanometer CD- SEM matching

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Minimizing metrology tool deltas through improved matching techniques is a constant pursuit. CD-SEM matching results of sub-nanometer were demonstrated between two tools, far superior to the vendor specifications. Details and methods are discussed, including FOV Factor matching, automated SEM tuning, new qual sampling plans (termed 5x5x5), and a 1st difference monitoring plan for tool drift. The results from these efforts will be reviewed, spanning beyond a year of data and including tip changes.

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6518-118, Poster Session

Visible light angular scatterometry for nanolithography

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Scatterometry1 is one optical measurement technique that has been explored extensively for semiconductor sub-micrometer and nanometer dimensional metrology. The technique refers to the measurements of reflected power upon the interaction of an incident beam with some periodic surface (grating). The characteristics of the diffractive surface affect directly the acquired measurements. Therefore it is possible to resolve some information about the grating line profile and dimensions from the measurements, which is referred to as the inverse scatterometry problem.

As technology is continuously pushing lithographic processes to sub-nanometer precision2, we address the feasibility of resolving with satisfying accuracies sub-100 nanometer line width (CD) dimensions as well as other important line profile features (depth and slope angle) using scatterometric measurements and low-cost visible wavelengths. For this purpose, angular reflectance measurements are considered using red wavelength incident beam (HeNe laser) at 632.8 nm. Both TE and TM polarized light are investigated where the electric field oscillates parallel or normal to the grating lines respectively. An iterative linearized solution model (linear regression) that has been established previously3 is employed here to retrieve the various line profile parameters based on the rigorous coupled wave approximation (RCWA).

The case where the pitch (period) is smaller than the wavelength is specifically addressed where only the specular order is reflected for the majority of incident angles (except maybe large incident angles). In this case, the interaction of electromagnetic waves in the visible wavelengths at the surface is closer to the Fresnel reflection at a uniform (flat) boundary than the optical diffraction at a periodic boundary. The periodic surface thus acts as a flat boundary with some effective optical index that is dependent on the structure geometry. In more accurate terms, the grating interacts with the incident beam as a flat surface with an effective index value determined by the pitch and line profile dimensions as well as the refractive index of the grating material. The variations in the value of the line profile parameters thus alter the Fresnel-like response for reflection. Consequently, these variations in the Fresnel-like reflectance curve could be used to detect slight changes in the effective index along the plane of incidence, or alternatively to detect slight changes in the profile parameters given sufficient measurement sensitivities.

Numerical simulations as well as experimental studies are demonstrated to propose low-cost feasible implementation for metrology in small nanotechnology research lab environments. Experimental results are based on sub-100 nm grating lines fabricated using both nanoimprint and electron beam lithography.

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6518-119, Poster Session

Robust sub-50-nm CD control by a fast-goniometric scatterometry technique

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Sub-50 nm half pitch critical dimensions metrology of resist lines on BARC by a fast goniometric scatterometry technique in the visible range has been investigated. The goniometric optical instrumentation allows illumination and reflection of patterned objects from almost all angles of view (-80°/80° polar angles, and 0°-360° azimuthal angles). As a consequence, this tomography-like technique ensures a robust lines profiles reconstruction. The performances in the case of sub-50 nm half pitch lines are demonstrated and compared to UV-VIS ellipsometry. Although the goniometer's illumination wavelength is far larger than the ellipsometer's ones, a better precision and robustness are achieved by fast-goniometry in the case of non-ideal shapes. Computational issues are also discussed.

6518-120, Poster Session

Accurate and reliable optical CD of MuGFET down to 10nm

P. J. Leray, G. F. Lorusso, S. Y. Cheng, N. Collaert, M. Jurczak, IMEC (Belgium); S. S. Shirke, M. Tortonese, VLSI Standards, Inc.

As the device's critical dimension (CD) decreases, it approaches the limits of standard metrology techniques and measuring features smaller than 20 nm represents a serious challenge. Within the framework of the 32 nm program at IMEC, a reliable and accurate approach to small feature metrology is required. We describe here a methodology aimed to measure features down to 10nm by means of scatterometry. The results are compared to calibrated CDSEM measurements [ ]. The active fin of a Multi Gate Field Effect Transistors (MuGFET) were measured across wafer and across batch. Scribe to cell correlation, wafer fingerprint, 3D profile, oxide thickness were investigated, In particular, 3D profile information was compared to TEM. Our approach produced very consistent results from all measurement techniques, and it is now fully integrated in the IMEC production line to monitor the FinFET platform.

6518-121, Poster Session

OCD metrology by floating n/k

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Recently, the introduction of OCD, i.e., scatterometry-based Optical CD measurement, has aroused much interest. Using OCD, critical dimensions of the 45-nm node can be measured with high accuracy and repeatability, even though the employed wavelengths are of the order of the visible light.

Compared with the scanning electron microscope (SEM), OCD provides practically nondestructive measurement of the resist CD. More, since only signals scattered to a specific angle are collected, OCD measurement is essentially impervious to line-edge roughness. Thus, it is especially suitable for process monitoring/control, despite that only patterns of large grating can be measured. Further, since the OCD hardware can be made very compact, it can be placed inside the track to realize integrated metrology (IM), for providing advanced process control (APC) with nearly real-time response, which is beneficial to the lithographic process with a very small process window. Further more, since not only the CD but the entire resist profile is measured, the APC can be made better by including defocus monitoring in addition to dosage.

However, the drawback of OCD is that the CD is evaluated indirectly, i.e., entirely based on resist profile reconstruction by simulation. The accuracy of the obtained resist CD/profile relies on the accuracy of the simulation. Since the computation loading of OCD is heavy, to shorten the computation time to make OCD practical as IM, to our knowledge, many OCD vendors simulate the resist profile by assuming the fixed refractive index/extinction coefficient (n/k) of the substrate. This is the case for organic bottom anti-reflection coating (BARC). However, for inorganic BARC of tunable n/k, the stability of n/k depends on the control of film deposition process, which can never be made perfect.

This paper reports investigation of the error committed for such assumption by referring to the actual n/k variation of production wafers. It also reports an efficient methodology for OCD modeling to handle such within-wafer n/k variation.

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6518-123, Poster Session

In-die critical dimension metrology using beam profile ellipsometry and reflectometry

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As device size continues to shrink and device design rules change, it is becoming clear that process metrology measurements on the traditional thin film and grating test pads in die streets are not providing the level of correlation to device structure necessary for optimal process control. In addition, the determination of local uniformity within a die is also becoming more important. Therefore, the need to perform high resolution measurements (with high throughput) directly within the die or cell area itself is growing, and poses new challenges for metrology. The micron-scale spot size for the beam profile reflectometry (BPR) and ellipsometry (BPE) technologies available on the Opti-probe has proven its worth for fast and very stable measurements of thin films. Here we report on the novel use of BPR and BPE for in-die measurements of several representative structures, and show that they are very fast and stable, and that high-resolution multi-parameter measurements of structures are possible, exceeding the capability of standard optical metrology solutions, while meeting current and next generation metrology requirements for precision and stability.

As an example, Figures 1a,b shows contour plots of the mid-CD measurement within a 100 x 120 micron test pad for a poly/gate application, using the SE result from a TWI RT/CD analysis (a), as compared to the BPE signal (b) (the measurement area itself is 60 microns). As one can see, the correspondence between the two results is clear. Additional results coupling the BPR signals to BPE for multi-parameter measurements are also presented. Overall, the 3 * stability for CD determined from the BPR and BPE signals for the applications presented is typically <0.25 nm.

6518-126, Poster Session

Mask global CD uniformity enhancement by removing local CD variation on mask

Y. Choi, M. Kim, O. Han, Hynix Semiconductor Inc. (South Korea)

As required CD uniformity on mask is less than 3nm for 50nm device, it is a challenge for mask engineer to overcome this limit. Usually total CD uniformity is composed with 3 kinds of uniformity, global CD uniformity which is dependent on FEC (fogging effect correction), develop and etch process, Local CD uniformity which is belong to E-beam process, and CD measurement error. To enhance the global CD uniformity, the repeatable CD measurement without local CD variation is important. In this paper, the source of local CD variation on mask will be evaluated, and to enhance the global CD uniformity, group CD measurement will be introduced and a result of process optimization with group CD will be presented .

This mask optimization process will be done for 50nm DRAM device.

6518-128, Poster Session

Achievement of sub-nm reproducibility for length measurements over 300 mm using the PTB´s nanometer comparator

R. G. J. Koening, J. Flügge, H. Bosse, Physikalisch-Technische Bundesanstalt (Germany)

The possible introduction of double or multiple exposure techniques drastically increase the overlay and registration metrology requirements in advanced lithography, as already indi-cated in the 2005 ITRS roadmap. Reference metrology tools have to be further developed to follow these specifications. The PTB as a national metrology institute is responsible for the dissemination of the length unit to industry. Since more than 15 years the PTB has offered length and coordinate calibrations to mask industry using its modified LMS 2020 mask comparator. In addition to this, the PTB is involved in the technical surveillance of the measure-ment laboratory at Vistec in Jena, which offers calibrations of length and coordinates on masks using an LMS IPRO and is accredited within the German calibration service (DKD).

In addition, the PTB has, in cooperation with partners from industry, developed a new 1D reference length comparator, the Nanometer Comparator. The dimensional measurements performed with the Nanometer Comparator are directly traceable through the use of an iodine-stabilised, frequency doubled Nd:YAG-laser as radiation source for the vacuum interferome-ter system, which is completely operated in vacuum. In order to minimize its non-linearity, the Jamin-type heterodyne interferometer uses only one polarization, spatially separated beams and roof mirrors as reflectors. The air bearings of the sample carriage are equipped with additional piezoelectric transducers so that the remaining angular deviations, which are caused by the motion and are measured by vacuum angle interferometers, can be corrected as well. Furthermore, most of the other known systematic uncertainty sources were either com-pletely eliminated or their standard uncertainty contribution was kept in the order 0.1 nm through the design- and construction phase of the Nanometer Comparator.

The Nanometer Comparator successfully participated in the latest international line scale comparison “Nano3” [1]. Measurements of a LIP 382 high resolution encoder system were used recently to characterize and validate the performance of the Nanometer Comparator. A reproducibility (2 s) of 0.6 nm over a range of 280 mm was achieved and it could be shown that the interferometer non-linearity remains below 0.1 nm. Furthermore, an international length comparison with two other industrial 1D vacuum comparators using this encoder as a transfer standard was carried out successfully. A maximum difference of only 5.5 nm, which is in the order of 2x10-8 and in agreement with the quoted measurement uncertainties, was obtained.

Lately intensive investigations and optimizations have been performed to reduce the measurement uncertainty contribution of the structure localization by means of the optical microscopes. The Nanometer Comparator is equipped with a slit and a CCD microscope. It is now possible to calibrate line scales of the “Nano3 design” [1] with an expanded measure-ment uncertainty (2s) below 5 nm.

[1] H. Bosse, W. Häßler-Grohnde, J. Flügge, R. Köning, Final report on CCL-S3 supplemen-tary line scale comparison Nano3, Metrologia 40 (Technical Supplement 2003) 04002

6518-129, Poster Session

Aera193i: aerial imaging mask inspection for immersion lithography

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At wavelength Aerial imaging has been proven to be a powerful tool in the inspection of photomasks at 78 and 65nm and this capability is provided on the Applied Materials Aera193 system. In order to meet the needs of the lithographic community it has been necessary to extend the performance envelope of the Aera193 to facilitate the inspection of sub 65nm photomasks hyper-NA immersion 193nm lithography. This has been accomplished through the use of increased illumination and projection NA and new advanced pupil shapes. Preliminary inspections and review images showing good results on 55nm design node advanced masks designed for NA up to 1.4 and sigma up to 0.96 are presented in this paper and show significant detection of protrusions and intrusions, transmission defects at 193nm, corner defects, isolated pinholes and pindots, proximity glass/phase defects, local CD defects, edge placement defects, proximity pinholes and pindots on immersion masks. This new capability is embodied in the Aera193i and can also be provided on earlier generation Aera193 systems as a field upgrade.

6518-130, Poster Session

Critical dimension measurements on phase-shift masks with reproducibility below 2 nanometers using an optical pattern placement metrology tool

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A useful extension of the optical mask pattern placement metrology is the measurement of critical dimensions, exploiting the outstanding mechanical resolution and stability of a corresponding mask metrology

machine. In particular the CD measurement on phase-shift masks (PSMs) poses a challenge on the optical measurement method. The paper presents the computational modelling of the corresponding measurement setup with respect to illumination beam path (reflection, transmission), PSM properties, and measurement optics for an edge detection method. Variables have been the illumination intensity, the focus variation of the edge position, and the critical dimension of the pattern. Based on the modelling outcome the alignment and the illumination have been improved and verification measurements have been performed on various machines of the type VISTEC LMS IPRO 3. The paper presents the setup, the modelling and the comparison to the practical measurement results., showing the achievement of the envisaged 2-nm reproducibility.

6518-132, Poster Session

LWR metrology for imprinted nanowires at 17-nm 1⁄2 pitch

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In the fabrication of nanowire crossbar circuits by nanoimprinting, we share the goal in reducing the Line Edge Roughness (LER) to lower the electrical resistance. While we have successfully patterned 17 nm 1⁄2 pitch Pt nanowires , we have also found the resistance of the wires to be too high to be explained by the simple scaling. Our attempt to perform LER metrology with a “state-of-the-art” CD SEM on the sample yielded results that do not appear reliable because of the high level of noise in the images (Fig. 1 A & B). We therefore subjected the samples to alternative metrology.

For our nanoimprint mold, which is made of etched Si, was imaged with our High-Resolution SEM (FEI-Sirian, Fig. 1C) and the LER information was extracted from the image with Summit image analysis software. For our imprinted Pt nanowires, we subjected them to Transmission Electron Microscopy (TEM) analysis (Fig. 1D) and extracted the LER information from the images with standard edge detection software. The results differ significantly from those from the CD-SEM. Because the higher quality of these images, we believe these results are more reliable than those from the CD SEM.

Table: Comparison of LER measured by CD-SEM, TEM, and HR SEM

Sample CD-SEM TEM HR SEM

Mold (Si) 2.5 nm - 1.5 nm

Pt wires on Qz 4.1 nm 3.4 nm -

Our results indicate that current CD metrology is inadequate even for measuring LER of ~3 nm, which is needed for the 57 nm node for Y2008. Moreover, the TEM results illustrate the importance of grain size’s influence on the LER. It is clear that better metrology for imaging the material structure will be needed as the line width shrinks to <30 nm.

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Table: Comparison of LWR measured by CD-SEM, TEM, and HR SEM.

Sample CD-SEM TEM HR SEM.

Mold (Si) 3.5 nm - 2.0 nm.

Pt wires on Qz 4.0 nm 3.5 nm - .

Our results indicate that current CD metrology is inadequate even for measuring LWR of ~3 nm, which is needed for the 57 nm node for Y2008. Moreover, the TEM results illustrate the importance of grain size’s influence on the LWR. It is clear that better metrology for imaging the material structure will be needed as the line width shrinks to <30 nm.

6518-133, Poster Session

Novel CD-SEM calibration reference consisting of 100-nm pitch grating and positional identification mark

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We have developed a novel reference grating fabricated by EB cell projection lithography and silicon dry etching, instead of conventional 240-nm pitch reference grating fabricated by laser-interferometer lithography and anisotropic chemical wet etching. Based on these results, we developed a 100-nm pitch grating reference for CD-SEM calibration. According to evaluation by CD-SEM, high-contrast secondary electron signals and uniform grating patterns within 3 nm in 3 sigma were obtained due to eliminate proximity effect of EB exposure. The reference has array of 100-nm grating cells in the x and y directions. Each cell consists of a 100-nm grating unit and the X-Y coordinate number in array and an addressing mark for CD-SEM to identify calibration position. These positional identification marks achieve accurate calibration managed by specification of the location of the grating and the number of calibrations. The accurate pitch size of the reference grating can be calibrated by optical diffraction angle measurement method using DUV laser.

6518-134, Poster Session

Advanced CD-AFM probe tip-shape characterization for metrology accuracy and throughput

H. Liu, J. R. Osborne, M. Osborn, G. A. Dahlen, Veeco Metrology LLC

As semiconductor and data storage industries apply Critical Dimension Atomic Force Microscopy (CD-AFM) for their metrology needs in research and production, (1) measurement accuracy/repeatability and (2) measurement throughput are the major criteria for acceptance. However, these two requirements are usually contradictory for a metrology instrument. For example, a scatterometer can take a snapshot of a wafer in seconds, but such indirect CD measurements are biased by the availability of library models and uncertainty of computer simulations. Transmission Electron Microscopy (TEM) provides an atomic-scale resolution that is traceable back to the lattice structure of atoms, yet the cross-section data is highly localized and can take days or weeks to acquire.

In the case of CD-AFM, since the scanning probe physically interacts with the structure of interest at a close proximity, the determination of sample morphology comes from direct measurements. Therefore, the measurement uncertainty can be attributed to: (1) AFM probe tip shapes and (2) system control and scan algorithms. For the former, past efforts have been mainly focused on improving metrology accuracy and repeatability by reducing the dimensional uncertainty of a tip shape. This approach includes characterizing the probe tip shape periodically. Inevitably, such tip shape calibration procedure takes time (approximately 5 min) and burdens production throughput.

In this paper, we introduce several new methods for AFM probe tip shape characterization with different designs of tip shape characterizers. The new tip shape characterizers were designed to address the limitation of current structures. First, a single silicon overhang structure with wear-resistant coatings was used as the characterizer for both tip width and tip shape profile. Tip-to-tip scan repeatability data (0.7 nm 3 Sigma) and measurement statistics suggest an improvement over present state-of-the-art practice. Tip shape profiles of several high aspect ratio (20:1 to 25:1), low lateral stiffness probes were successfully characterized with this method. Furthermore, the use of single characterizer provides an opportunity to shorten tool calibration time, and consequently, increase measurement throughput.

In addition, a characterizer prototype based on nanostructures is proposed for CD-AFM. When scanning probe geometry shrinks with semiconductor technology nodes, it has become a challenge to characterize a probe with a few tens of nanometer of width with a micrometer-size characterizer. Using a comparable or smaller size of characterizer for a small (20 to 50 nm) AFM probe not only reduces the dimensional uncertainty, but also expands the 2-D profiling capability of current tip shape characterization.

We will discuss limitations of current tip shape profiling techniques, proof-of-concept experiments for new characterizers, implementation of new tip shape characterization methods, and approaches to increasing measurement throughput.

6518-135, Poster Session

Validation of CD-AFM image reconstruction using TEM as the reference metrology system

G. A. Dahlen, L. Mininni, M. Osborn, H. Liu, J. R. Osborne, Veeco Metrology LLC

With each successive ITRS node, increased emphasis is placed on measurement precision and accuracy, while structures concurrently become more 3-dimensional. Subjected to these constraints, Critical Dimension Atomic Force microscopy (CD-AFM) has exhibited an expanding role in reference metrology for the semiconductor and data storage industries. Recent standards developed by NIST and VLSI, in conjunction with on-going CD AFM development, has enabled single nanometer uncertainties for width measurements. However, for current semiconductor morphologies, 1-dimensional "tip width compensation" for AFM probe shape effects is inadequate and retains residual tip shape artifacts in the AFM image, which in turn, lead to measurement bias. To remove the image "dilation" that occurs due to the tip shape (in all regions contacted by the tip), the tip shape must be fully characterized and extracted from the image in an "erosion" process.

Our prior work has focused primarily on the details of the tip characterization and algorithms used in the image reconstruction process. The present paper investigates validation of CD AFM image reconstruction using Transmission Electron Microscopy as the Reference Metrology System (RMS). To have meaningful results, an assessment must be made using a broad range of tip shapes and challenging sample morphologies. To address this, we have selected three samples: the VLSI NanoCD for the its characterized upper-corner radii and two "process stressed artifacts" provided by IBM1,2. The first IBM artifact consists of a "notched", over-etched polysilicon gate, shown in Figures 1 and 2. The second is a non-reentrant, under-etched polysilicon sample with "radiused" foot section. The tips selected for the study are conventional CD AFM probes, recently developed "trident" probes from Team Nanotec, and carbon nanotube probes from Daiken/Sumitomo Corporation.

Sources of measurement error for the reconstructed images can be attributed to three sources: 1.) the measurement system, 2.) the reconstructed tip shape, and 3.) the image reconstruction algorithm. The sources of error are not de-coupled. Hence, non-destructive TEM measurements are obtained of the tip apex region in the study. Finally, the data collection strategy for the IBM samples required careful prescreening of the TEM sample site in order to account for line width variation (LWV).

[1] M. Sendelbach and C. Archie, "Scatterometry measurement precision and accuracy below 70 nm", Proceedings of SPIE, Vol. 5038, pp. 224-238, 2003

[2] The authors wish to express their appreciation to Bill Banke, Chas Archie and Matthew Sendelbach for providing the polysilicon samples used in this study.

6518-137, Poster Session

An advanced AFM sensor: its profile accuracy and low-probe-wear property for high-aspect ratio patterns

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Design rule shrinkage and the wider adoption of new device structures such as STI, copper damascene interconnects, and deep trench structures have increased the necessity of in-line process monitoring of step heights and profiles of device structures. For monitoring active device patterns, not test patterns as in OCD, AFM is the only non-destructive 3D monitoring tool. The barriers to using AFM in-line monitoring are its slow throughput and the accuracy degradation associated with probe tip wear and spike noises caused by unwanted oscillation on the steep slopes of high-aspect-ratio patterns.

Our proprietary AFM scanning method, Step-in mode, is the method best suited to measuring high-aspect-ratio pattern profiles. Because the probe is not dragged on the sample surface as in conventional AFM, the profile trace fidelity across steep slopes is excellent. Because the probe does not oscillate and hit the sample at a high frequency as in AC scanning mode, this mode is free from unwanted spurious noises on steep sample slopes 1) 2). To fully take advantage of the above properties, we have developed an AFM sensor optimized for in-line use, which produces accurate profile data at high speeds and incurs little probe tip wear. The control scheme we have developed for the AFM sensor, which we call "Smart Step-in", elaborately analyses the contact force signal, enabling efficient probe tip scanning and a low and stable contact force 3).

With a developed AFM sensor that realizes this concept, we have conducted an intensive evaluation on the effect of low and stable contact force scan down to 1 nN. Probes with silicon tips, HDC (High Density Carbon) tips and CNT (Carbon Nanotube) tips have been used for the evaluation. The experiment proves that low contact force enhances the measured profile fidelity by preventing probe tip slip on steep slopes (Fig. 1). Dynamics simulation on these phenomena has also been conducted, which shows a good match to the experimental result.

The low contact force scan also realizes extremely little probe tip wear, which is essential to assure high measurement repeatability. Step-in mode inherently causes little probe tip wear thanks to the minimal number of tip-sample touch. This good property has been enhanced by the low contact force scan. Evaluation results on probe wear will be also presented.

This paper partially belongs to "Nanometer-Scale Optical High Density Disk Storage System" project which OITDA contracted with The New Energy and Industrial Technology Development Organization (NEDO) in 1998 based on funds provided from the Ministry of Economy, Trade and Industry (METI) of Japan, and partially belongs to "Terabyte optical storage technology" project which OITDA contracted with The Ministry of Economy Trade and Industry of Japan (METI) in 2002 and contracted with The New Energy and Industrial Technology Development Organization (NEDO) since 2003 based on funds provided from METI.

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2. Takafumi Morimoto, Toru Shinaki, Yukio Kembo, and Sumio Hosaka, "New atomic force microscope method for critical dimension metrology", Proc. SPIE 5038, 636-643 (2003).

3. Masahiro Watanabe, Shuichi Baba and Toshihiko Nakata, Toru Kurenuma, Hiroshi Kuroda and Takenori Hiroki, "An Advanced AFM sensor for High-Aspect Ratio Pattern Profile In-line Measurement", Proc. SPIE 6152, 797-806 (2005).

6518-139, Poster Session

A new in-line AFM metrology tool best suitable for LSI manufacturing in the 45-nm node and beyond

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Every new semiconductor technology node provides further miniaturization and higher performance, thus increasing requirement to higher performance of metrology tools.

AFM has superior space resolution to other metrology tools and has already become an indispensable in-line tool in the current LSI manufacturing. In-line AFM is now essential for pre-CMP, post-CMP, post-etch topography measurement and other inspections in which stylus surface profilers have been used.

AFM has also started to be used for critical dimension (CD) measurement recently. CD-AFM technique using a special flared probe has been proposed to apply AFM to CD and sidewall roughness measurement. AFM is a powerful non-destructive tool for the calibration

of other CD metrology tools such as CD-SEM and OCD.

However, there are still several issues to be improved to apply AFM for in-line use including CD metrology to the 45-nm node and beyond. Reproducibility issue caused by probe tip wear may be considered to be fatal. Probe size limitation and its relatively slow throughput are other serious issues.

To overcome these issues against AFM for in-line metrology, we have developed a new in-line AFM best suitable for LSI inspection in the 45-nm node and beyond. We have also developed several types of carbon-nanotube (CNT) probes specially designed for our AFM. Our new AFM features advanced Step-in mode [1,2] and high-throughput wafer processing. In Step-in mode, a probe tip approaches, contacts to a sample surface, escapes from the surface, and moves to a new measurement position. Sure and gentle probe tip contact of Step-in mode realizes not only precise measurements of high-aspect-ratio pattern samples, but also minimum tip wear.

In this paper, we will demonstrate the advantage of our new in-line AFM. Especially, we will emphasize on the benefit of the combination of Step-in mode and the CNT probe. Figure 1 shows the measurement results of a photoresist line-and-space sample (70 nm line-width / 280 nm line-pitch). The measurement was performed using Step-in mode of 1-nN contact force, and the CNT probe whose diameter is 20 nm. Though the images contain no sidewall information because of the top-down AFM measurement, detailed topography of the top of the patterns can be clearly observed.

Figure 2 shows average profiles along the line with the contact force as a parameter (note that no tip shape deconvolution was performed). Because the contact force of more than 5 nN causes deformation of photoresist, suppressing the contact force is important for the measurement of photoresist samples.

In this paper, we will also mention long-term measurement stability of our AFM. Thanks to Step-in mode and the CNT probe, our new in-line AFM realizes precise measurement and excellent reproducibility over a large number of wafer processing for the LSI manufacturing of 45-nm node and beyond.

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6518-140, Poster Session

Magnification calibration standards for sub-100-nm metrology

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As we approach the 65nm technological node, transistor gates with dimensions of the order of 40nm are being manufactured. As the device performance is directly related to the dimensions of the gate, critical dimension (CD) control becomes an important part of the fabrication process. Characterization of these small feature size, generally referred to as Metrology, is an indispensable ingredient of the semiconductor manufacturing processes. Metrology relies not only on the precision, but also the accuracy of commercially used metrology tools like the high performance CD-SEM. To facilitate the measurement of the CD-SEM performance, an easy access to standard reference artifact traceable to international specifications is an added advantage. Considerable literature is available for CD-SEM performance, which relies on in-house artifacts or general test objects. The absence of commercially available artifacts hinders performance evaluation of different CD-SEM. The objective of this abstract is to introduce the fabrication and characterization of artifacts for the sub-100nm metrology, which can be made available in wafer form at low cost.

In this work, artifacts have been designed and fabricated for precise magnification calibration of the CD-SEM. The designing of the artifacts takes into account the proximity effect, a problem associated with the e-beam exposure, to produce dense grid type structure in the sub-100nm region. The structures are fabricated using the e-beam lithography tool, operated at 50KeV. The artifacts have been fabricated on a thin layer of negative resist HSQ spun on silicon substrate. Subsequent development in 0.26N TMAH gives a structure on silicon wafer, thereby eliminating contamination issues. The artifacts have 100nm pitch, with linewidth of the order of 40nm.

The analysis of the SEM image for resolution, astigmatism correction is carried out using the SMART macro (Joy et al 2000; Joy 2002) designed for the SCION Image program. Furthermore, characterization of the artifacts for line pitch determination is carried out using standard software such as “Measure” (Spectel Corp.) which provides an absolute calibration of the image pixel size that can then be used to measure other features. Line pitch determination carried out by the threshold method and the regression to baseline method gives out values close to 100nm, in accordance to designed values. The low values for the line edge roughness (LER) further facilitates precise linewidth metrology. Line pitch determination using optical metrology tools and the inbuilt laser interferometer in the electron beam lithography tool are being evaluated for precise measurements.

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6518-141, Poster Session

CD-AFM scan algorithm enhancements

L. Mininni, Veeco Metrology LLC; J. Foucher, Lab. d’Electronique de Technologie de l’Information (France); M. Osborn, Veeco Metrology LLC

Improving device performance and yield is one of the primary goals of microelectronic research and development. In order to attain this goal, process engineers are focusing on the integration of new materials and the development of new device architectures. For production process control, the two main techniques to monitor device dimensions are CD-SEM and Scatterometry. Despite the excellent repeatability of these techniques, SEM and Scatterometry often suffer from unacceptably large measurement uncertainty, particularly when applied to newly developed device technologies. A consequence of these metrology limitations is a delay in the transition of new process technologies into production.

CD-AFM is a versatile metrology technique, which is capable of providing consistent, precise measurements for a wide range of sample types and geometries. In this paper we present recent enhancements in the CD-AFM scan algorithm, which we have demonstrated to improve CD measurement accuracy, resolution and precision, while increasing Tip lifetime and scan speed for advanced CD-AFM Tips. An example of sidewall noise reduction is shown in figure 1, and a 40% improvement in Bottom CD measurement repeatability is shown in figure 2.

6518-142, Poster Session

Plasma-assisted cleaning by electrostatics (PACE)

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The need for a non-contact contamination removal technique has been exhibited by various companies. While an EUV compatible pellicle is being researched, contamination will become an ongoing problem to overcome. Some techniques that are being considered for contamination removal include the use of shockwaves which are potentially damaging, as well as rolling contamination off of a surface. Depending on feature size, rolling or moving of contamination horizontally across a surface is limited as there is a strong possibility that the contamination will get trapped in between features. Plasma-Assisted Cleaning by Electrostatics (PACE) is a non-contact removal method that utilizes charge imbalances to remove particles perpendicular to the surface. A positive bias is applied to the top of the sample for conducting samples or to the substrate behind an insulating sample. This positive bias draws in net electrons from the plasma to the entire surface. The contamination charges negatively and the

positive bias is removed and switched with a negative bias. The combination of substrate/particle charge imbalance as well as electric field effects from the plasma sheath provide for the removal mechanism. Surface damage has been avoided by staying below the sputtering threshold for the surface materials of the samples. Recent tests on 2.5 nm ruthenium on Si/Quartz using the PACE technique coupled with Atomic Force Microscopy data has shown no roughening of the surface and approximately 90% removal efficiency of contamination. In addition, Auger Electron Spectroscopy scans show no removal of the 2.5 nm ruthenium capping layer. Removal results for 30 nm to 220 nm PSL particles as well as select other contamination materials on samples comparable with EUV masks in addition to damage assessments will be presented.

6518-143, Poster Session

Optical characterization of high-aspect-ratio of microstructures

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In the present research we have fabricated and investigated two kinds of surface relief gratings (phase diffraction gratings), formed with standard photolithography combined with the plasma-etching and reactive ion etching (RIE). Diffraction efficiency of diffraction gratings (originally produced in silicon and quartz glass substrates) was measured experimentally and estimated using linear dimensions of gratings defined by atomic force microscopy (AFM) and scanning electron microscopy (SEM). The main experimental results were compared with the computer simulations where the standard software ("PCGrate 2000MLT" and "GSolver") were employed to calculate diffraction efficiency of different period of diffraction gratings for the different wavelengths of visible light. Comparing two evaluation methods: direct (scanning probe microscopy) and indirect (diffraction efficiency) we have demonstrated feasibility of optical methods in control of geometrical dimensions of gratings at the microscopic range. These methods enabled us to control and produce diffraction gratings for the different optical applications, like dispersive elements in spectroscopes, beam splitters or micro-fluidic devices.

6518-144, Poster Session

Contrarian approach to and ultimate solution for 193-nm reticle haze

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Despite ample phenomenological evidence of reticle haze in IC manufacturing fabs, the mechanism of reticle haze formation is not well understood. Many attempts to control the reticle haze formations are driven by trial-and-error approach and results are frequently contradicting and confusing.

Authors apply extensive expertise of airborne molecular contamination (AMC) measurement and control and DUV optics protection to developing a potential solution to the issue of 193 nm reticle haze.

The authors outline the common mechanism of the reticle haze formation and show that chemical modification of the reticle surface during mask manufacturing procedure is largely responsible for mask reticle susceptibility to AMC and surface molecular contamination (SMC). A proposed mechanism well explains available experimental and phenomenological data and the differences seen in chemical compositions of the haze particles observed at different fabs.

Authors proposed the single elegant solution for controlling multiple types of haze. Effectiveness of this solution is demonstrated through the field data obtained from production fabs.

6518-145, Poster Session

Thermal imaging of a lithography cell, including exposure tool, using a self-contained instrumented wafer

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Interesting results were obtained by looking at the lithography cell from the perspective of a wafer. The wafer viewpoint was achieved by instrumenting the substrate of a 200mm production wafer with an embedded network of extremely thin electronics and an array of 53 thermal sensors, and then covering the array with a thin film or half thickness silicon wafer. This instrumented wafer had resist applied, was developed, spun in the resist application module, soft and hard baked and exposed in a 248nm tool.

Each separate step was fingerprinted, as well as the behavior of the entire line in an integrated run. This is the first known full thermal process emulation of the lithography cell.

Effects of exposure dose on wafer temperature were measured, in varieties of dose, in single shot mode, and in a normal shot pattern.

Thermal response of the wafer was much higher than expected, and meaningful data were acquired.

6518-146, Poster Session

Optimization of lithography process to improve image deformation of contact hole sub-90-nm technology node

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In resolution limited lithography process, the image deformation is getting severer. This is very important area where we need to fully understand and improved since the image deformation is directly giving poor CD control effect. Especially, contact hole image will be more sensitive since it has lower k1 factor that line and spaced pattern. This image deformation of contact hole can give some severe electrical fail due to not opened contact. In our case, we observed some critical failure mode of diagonal induced by abnormal contact hole shape of rough edge.

In this paper, we investigate how deformed contact hole image impacted on degradation of device performance in electrical properties and yield and how we can improve it. To quantitatively analyze image deformation of contact hole, we recommend new measurement method first. This new measurement gives exact image deformation amount at different experimental conditions.

Finally, we will show how experimental conditions such as soft bake temperature, post expose bake temperature, hardening bake temperature, illumination condition and mask bias change image deformation of contact hole.

6518-147, Poster Session

Pore-filling dynamics for nano-imprint lithography

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The escalating cost for Next Generation Lithography (NGL) tools, driven by the need for complex sources and optics, has propelled many research groups to explore alternate forms of imprint lithography. Step and flash imprint lithography (SFIL) has emerged as a low cost, high throughput alternative to conventional photolithography for producing high aspect-ratio and high resolution patterns.

SFIL is a low pressure molding process that transfers the topography of a rigid transparent template using a low-viscosity, UV-curable organosilicon solution. The solution is photopolymerized by exposure to UV radiation through the backside of the template, leaving an inverse replica of the relief structure. Complete filling of features is thereby essential for nanoimprint process to faithfully replicate the desired features. Previous work of Reddy et al. provided insight on gas entrapment within pores, due to the pinning of upper contact line of fluid-air interface at sharp corners.

This paper presents work focused on diffusion of entrapped gas through an etch barrier. A rigorous model has been developed using finite difference numerical techniques and the Landau transformation for moving boundary conditions. The filling process is studied parametrically for a variety of feature sizes, aspect ratios and pattern densities. Surface energy analysis has been investigated for various cases to identify limits for the highest achievable aspect ratios. The pinning effect, described by Reddy, has been documented experimentally and efforts to develop analytical model are in progress. Multi etch-depth templates, ranging from 100nm to few microns, were fabricated using electron beam lithography for the present study.

6518-148, Poster Session

Resolution enhancement technique using oxidation process with nitride hardmask process

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In lithography process, resolution enhancement technique (RET) which makes us use same lithographic equipments and materials is one of most important area to enhance development speed of device. The studies for RET have widely been done and the examples of RET are modified illumination, phase shifted mask and double exposure. The most studies have been done in lithography area. We think that area of RET study is not only lithography but also overall patterning including etching process.

In this paper, we develop new RET which is using oxidation process of silicone. When we use nitride hard mask process and CMP with this oxidation process, we observed to achieve small resolution. Also we investigate process capability of this new process in terms of CD control, defect and so on.

6518-150, Poster Session

Process development to improve subresolution size of hole shape in ArF lithography for flash devices

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As the resolution requirement downing 90 nm beyond, hole pattern is one of the most challenging features to print in the semiconductor manufacturing process. Especially, when hole patterns have dense array of holes as they are consisted of several columns with single row, there can be serious distorted form from desired patterns such as oval hole shape and bridge between holes. It is due to nature of diffraction which is interaction of diffracted light from near holes. Overlap margin reduction by hole shape change as oval shape is very harmful in sub-90nm photolithography process which has very narrow overlay margin. To increase overlap margin, it is necessary to solve these phenomenon. Optical Proximity Correction (OPC) has been used for overcoming oval hole shape. Through the result of OPC modeling and simulation, we could get optimized mask bias of hole. Sometimes, good experimental data will be help for this modeling and OPC process. From these OPC simulation and experimental data, most compatible rule based OPC process could be developed. In this paper, we suggest the method of improving oval hole shape by using OPC simulation and making rule base OPC process from experimental data.

6518-152, Poster Session

Capacitive sensor for optical measurement and monitoring

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Abstract: The ultimate aim of the work described here is to explore Nano-technology. The initial target, as described in this paper, has been to implement a Nano-precision capacitive displacement sensor, modularized circuitry, and measurement range from ±5μm~±25μm, resolution better than 5nm, precision better than 10nm, linearity better than 5‰, stability better than 20nm/h can be achieved.

According to the demands of “phase modulation monitoring and dynamic compensation” project of SGII-9, high precision adjustment devices are adopted to realize the phase dynamic compensation of optical waves; Adjustment precision is better than 20nm, we developed a Nano-precision capacitive displacement sensor to monitor adjustment process. Measurement circuitry is based on the principle of ideal parallel capacitor, sensor probe and measured object surface compose a two-plate sensor, according to the principle of arithmetic measurement circuitry, when sine wave excitation current with constant frequency passes through capacitor, the amplitude of output potential is proportional to the gap between two plates.

Fig. 1 Schematic diagram of measurement circuitry

The schematic diagram of the measurement circuitry is shown in Figure 1, the amplitude and frequency stability of sine wave excitation circuitry are strictly required, improved quartz oscillator circuitry is proposed to meet the demands; in order to eliminate the disadvantage factor of parasitic capacitance, imperfection equipotential circuitry are presented, compared with conventional complete equipotential screening technology, imperfection equipotential circuitry is simpler and easy to integrated; Improved main amplifier composes of two-stage operational amplifier and has high input impedance; the action of zeroing circuit is to supply suitable operating point for the instrument; Stability of regulated power supply influenced the performance of sensor directly, the p-p amplitude of ripple voltage of ordinary regulated power supply is more than 10mvp-p, we adopt DC-AC-DC secondary regulated voltage technology, 24V direct current is turned into high-frequency square wave current by applying PWM push-pull circuit, following with ordinary rectification, filter, voltage-stabilizing, double isolated separately regulated power supply with p-p amplitude of ripple voltage better than 0.2mv are achieved;

6518-153, Poster Session

Purge micro-environment with ionized air to reduce chances of ESD damages to reticles/wafers

H. Wang, Y. Liu, Entegris, Inc.

Electrostatic charge on reticles/wafers and the surfaces of the microenvironment (RSP, FOUP, SMIF pod, etc) they are stored in can potentially damage the features on them. Purging of the microenvironments using pure N2 or XCDA has been utilized by many fabs to help mitigate AMC contamination on reticles/wafers. We have been experimenting ionizing the purge gas to bring an additional benefit of neutralizing electrostatic charges with purge gas. Experimental results have shown substantial reduction of charges on reticles/wafers, and the internal surfaces of the microenvironments.

6518-154, Poster Session

Monitoring airborne molecular contamination: a quantitative and qualitative comparison of real-time and grab-sampling techniques

A. M. Shupp, Particle Measuring Systems, Inc.

Monitoring and controlling AMC (Airborne Molecular Contamination) has become essential in DUV (deep ultraviolet) photolithography for both optimizing yields and protecting tool optics. A variety of technologies have been employed for both real-time and grab-sample monitoring. While real-time monitoring has the advantage of quickly identifying “spikes” and upset conditions, 2 - 24 hour plus grab-sampling allows for extremely low detection limits by concentrating the mass of the target contaminant over a period of time. Employing a combination of both monitoring techniques affords the highest degree of control, lowest detection limits, and the most detailed data possible in terms of speciation. Currently, there is concern in industry regarding the accuracy and “agreement” between real-time and grab-sampling methods. This study utilizes side by side comparisons of a variety of real-time monitors operating in parallel with both impingers and sorbent tubes to measure NIST traceable gas standards. By measuring in parallel, a truly valid comparison is made between methods while verifying the results against a certified standard.

Conference 6518: Metrology, Inspection, and Process Control for Microlithography XXI

6518-155, Poster Session

Improved optics life with continuous parts per trillion contamination analysis and control

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Optics components used in lithography and inspection/metrology equipment are constantly pushing the limits of both lens stack materials and coatings. Lenses, windows, reticles and mirrors are all susceptible to irreversible photo contamination even if “parts per trillion” (PPT) levels of acid, base, refractory and organic compounds in the surrounding purge environment interact with the equipment high energy light sources. Replacement of these optical components is cost prohibitive, so a practical solution must be found that can provide the needed PPT purity of facility supplies, such as Optics purge gases, along with the continuous quality record to document the history for future diagnostics analysis.

Real time continuous measurement of these contaminants at PPT levels is not practical for the manufacturing area: the equipment capable of measuring PPT level gas phase photo sensitive contamination is expensive and requires a laboratory environment with qualified staff.

Offline analysis techniques offer the required detection limits of analysis, but cannot answer the goal of a continuous, historical record proving that the gas supply has always stayed in specification - a record showing that the optics have never been exposed to the critical impurities.

Both equipment manufacturers and users are faced with this challenge to deliver and document facility gases with sub PPT levels of contamination. This paper provides a completely new and unique concept for contamination control of Optics purge gas with an integral system reporting for continuous analysis of the delivered compressed gas quality at PPT detection levels. Field data from multiple locations in the USA, Europe and Asia will be shown to support the new AMC control and assessment philosophy.

6518-156, Poster Session

Optimizing surface finishing processes

M. W. Quillen, Eastman Chemical Co.; J. Moore, DAETEC; P. L. Holbrook, Eastman Chemical Co.

As the semiconductor industry continues to implement the ITRS node targets that go beyond 45nm [1], the need for improved cleanliness between repeated process steps continues to grow. Wafer cleaning challenges cover many applications such as Cu/low-K integration, where trade-offs must be made between dielectric damage and residue by plasma etching and CMP or moisture uptake by aqueous cleaning products [2-5]. Some surface sensitive processes use the Marangoni tool design [6] where a conventional solvent such as IPA, combines with water to provide improved physical properties such as reduced contact angle and surface tension. This paper introduces the use of alternative solvents and their mixtures compared to pure IPA in removing ionics, moisture, and particles using immersion bench-chemistry models of various processes. A novel Eastman proprietary solvent has been observed to provide improvement in ionic and moisture capture as compared to conventional IPA (Fig. 1). These benefits may be improved relative to pure IPA, simply by the addition of various additives. Some physical properties of the mixtures were found to be relatively unchanged even as measured performance improved (Fig. 2). Benefits of particle removal were identified, however, the values were found to be method dependent using various deposition approaches. A description of the solvent systems, modeling, analytical equipment, and method capability will be presented.

6518-157, Poster Session

New filter media development for effective control of trimethysilanol and related low-molecular weight silicon containing organic species in the photobay ambient

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Tremendous efforts are being made in the industry to eliminate yield-reducing contaminants from air used for semiconductor processing tools. There is growing concern within OEMs that low molecular weight silanes and siloxanes (LMWS), for instance, Trimethylsilanol (TMS), can be a potential pre-cursor of photochemical formation SiOx deposits on the surfaces of optical elements. Impossible to remove via UV/ozone or physical cleaning, these deposits are causing loss of transmission, a decrease in uniformity, de-tuning of antireflective coatings and eventually, reduction of throughput that could result in costly lens replacement.

The authors present results of extensive studies on unique chemical behavior of LMWSs and associated challenge of their analytical determination, effective control and air chemistry in general. In their paper, the authors describe a new approach to creation of a TMS gaseous source for filter media development and comprehensive practical guidance on reliable analysis of target compounds. In the course of their research, the authors discovered that filtering a diverse mixture of airborne molecular contaminants (AMCs) in the fab is not without complication - a breakdown of certain LMWS’s takes place within hybrid adsorption media, forming various by-products which may propagate through the filter’s array much faster than parental compound.

The authors of this research and paper propose a unique engineering solution to the challenge of controlling LMWS’s - a solution that shows a significant advantage over currently existing approaches.

6518-158, Poster Session

Noncontacting electrostatic voltmeter for wafer potential monitoring

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With reduced half-pitch line widths, the International Technology Roadmap for Semiconductors (ITRS) forecasts increasing number of issues with electrostatic discharge (ESD) related phenomena and the need for improved wafer electrostatic charge control in semiconductor wafer processing. This means that wafer metrology should encompass charge measurements as a routine operation. Additionally, with the increasing complexity of wafer processing, in-line measurements, including surface voltage and charge detection and analysis, are becoming more important. One of the instruments utilized in such measurements is a non-contacting electrostatic voltmeter (ESVM). In this paper the authors would like to introduce a new design of the ESVM probe which allows for the measurement of surface voltages with DC stability and millivolt sensitivity. The construction of the probe utilizes a gold plated sensor that is mounted on a vibrating tuning fork which is electromechanically excited by a piezoelectric driver.

6518-159, Poster Session

Optimized molecular contamination monitoring for lithography

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A new approach to monitoring molecular contamination in lithography is presented. Recent technical advances have made it feasible to perform continuous real-time monitoring with significant advances in sensitivity and stability while minimizing sample tubing effects. These improvements are realized by using a small, low-cost monitor that is dedicated to monitoring a single location. Previously, it has been cost prohibitive to conduct continuous monitoring of molecular contamination on a large scale.

Conventional molecular contamination monitoring systems employ a multi-point air sampling system connected to an analyzer. This monitoring approach has evolved into normal practice, driven by the need to monitor a large number of locations at the lowest reasonable cost.

The biggest drawbacks of the conventional monitoring approach are small quantity of measurements per day at each location, effects of long sample tubing lengths, analyzer response and clear down times when adjacent sample point concentrations differ greatly, and minimal ability to perform sample averaging to increase sensitivity. For example, a sixty point sampling system with a 10 minute sample cycle will take 600 minutes or 10 hours to sample all locations. Each location will be monitored for 10 minutes every 10 hours, leaving each location

unmonitored for the remaining 9 hours and 50 minutes.

A dedicated, point-of-use monitor offers the following advantages over a conventional multipoint sampling system: continuous monitoring, no missed contamination events, sample tubing lengths reduced from 20 - 30 meters to 2 - 3 meters, and 5 - 10x better sensitivity. Reducing the sample tubing lengths minimizes interactions between the contamination molecules and the tubing surface.

Improvements in sensitivity and stability are realized through the dedicated monitor approach to molecular contamination monitoring. Because the monitor is continuously sampling the same environment, sample averaging can be used in a highly effective manner to reduce the detection limit. In one application, for example, the limit of detection for one minute samples is 120 ppt and the limit of detection for a 60 minute rolling average is 8.2 ppt. This is particularly useful in chemically filtered environments where the concentrations are usually low and stable. An automated monitoring software package can simultaneously plot individual one minute data points and a long-term running average. The one minute samples are used to immediately detect the onset of a contamination event while the long term running average is used to monitor background contamination at the lowest levels.

6518-160, Poster Session

The novel advanced process control to eliminate AlCu-PVD induced overlay shift

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The wafer induced overlay shift caused by metal film deposition is becoming an important concern with ever tighten overlay tolerances. Various overlay mark designs have been studied to protect from the effects of AlCu-PVD (Physical-Vapor Deposition) induced overlay shift [1], but it seems not so effective. APC (Advanced Process Control) is another method to manage the AlCu-PVD induced overlay shift, however, several process factors should be considered for ensuring overlay registration accuracy [2], which makes the APC algorithm complex and the APC model setup costly.

In this study, a new approach has been demonstrated to effectively eliminate the AlCu-PVD induced overlay shift. Since the metal sputtering process usually causes the surface of scribe-lane overlay metrology targets to physically shift, the true metal-to-contact registration behavior can be measured only before metal-deposition or after metal-etch step. With measuring the metal-to-contact layer registration before the metal deposition and feeding forward the values for metal-to-contact overlay compensation at the real metal photo step, the metal-induced shift can be optimally managed. The post metal-etch vector maps of metal-to-contact overlay errors of two different algorithms were compared in Figures 1(a) and 1(b), the shorter vector length of feed-forward compensation approach demonstrates its outperformance to conventional compensation algorithm, done in ADI (After Develop Inspect) step, in metal-induced overlay shift control. Besides, several sets of overlay metrology targets have been compared on the process effects of contact-etch and contact-WCMP (Tungsten Chemical-Mechanical Polishing). Figure 2 compares the overlay residual analysis by KLASS between wide-trench overlay mark and narrow-trench overlay mark, as the consequence, the wider trench key used at contact layer for overlay measurement is the most susceptible to the process variations, resulting in a larger overlay residual than that of narrower trench key. The feed-forward compensation algorithm in combination with narrow-trench overlay mark has demonstrated its effectiveness on managing the AlCu-PVD induced overlay shift as well as reducing the process noises.

6518-161, Poster Session

Low-pressure drop filtration of airborne molecular organic contaminants using open-channel networks

A. J. Dallas, J. D. Joriman, L. Ding, Donaldson Co., Inc.

Airborne molecular contamination (AMC) continues to play a very decisive role in the performance of many microelectronic devices and manufacturing processes. Besides airborne acids and bases, airborne organic contaminants such as 1-methyl-2-pyrrolidinone (NMP), hexamethyldisiloxane (HMDSO) and condensables are of primary concern in these applications. Currently, the state of the filtration industry is such that optimum filter life and removal efficiency for organics is offered by granular carbon filter beds. However, the attributes that make packed beds of activated carbon extremely efficient also impart issues related to elevated filter weight and pressure drop. Most of the lower pressure drop AMC filters currently offered are quite expensive and are simply pleated combinations of various adsorptive and reactive media. On the other hand, low pressure drop filters, such as those designed as open-channel networks (OCN's), offer good filter life and removal efficiency with the additional benefits of significant reductions in overall filter weight and pressure drop. Equally important for many applications, the OCN filters can reconstruct the airflow so as to enhance the operation of a tool or process. For tool mount assemblies and full fan unit filters this can result in reduced fan and blower speeds, which subsequently can provide reduced vibration and energy costs. Additionally, these low pressure drop designs can provide a cost effective way of effectively removing AMC in full fab (or HVAC) filtration applications without significantly affecting air-handling requirements. Herein, we will present a new generation of low pressure drop OCN filters designed for the removal of airborne organics in a wide range of applications.

6518-162, Poster Session

Novel method of under etch defect detection for contact layer-based Si substrate using optic wafer inspection tools

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As the design rules of semiconductor devices have decreased, the detection of critical killer defect has became more important. One of killer defect is under etch defect caused by insufficient contact etch. Although very low throughput only e-beam wafer inspection tool has used for monitoring tools of under etch defect because optic wafer inspection don't have enough signal to detect that on contact layer. In this study, novel method is suggested for detection of under etch defect using optic wafer inspection tool had high throughput and repeatability.

6518-163, Poster Session

CD-bias evaluation and reduction in CD-SEM linewidth measurements

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We experimentally evaluated the bias in linewidth measurements that are taken using a critical dimension scanning electron microscope (CD-SEM). Using the results of this evaluation, a bias reduction technique was developed.

CD-SEM is a powerful metrological tool for use in the development and manufacture of semiconductor devices. However, the electron scattering in a sample's structure causes the measurement bias to vary with changes in the pattern shape, such as a change in the sidewall angle. The secondary electron signal has blooms at the edge of the pattern and the edge detection algorithms assign the edge positions in the blooms in CD-SEMs. The edge detection algorithms used in current CD-SEMs are affected by variations in the blooms that cause linewidth measurement bias depending on the pattern shape. However, the pattern shape is usually not known. This measurement bias is greater than the international technology roadmap for semiconductors (ITRS) requirement, but it is difficult to eliminate the errors without using the pattern shape information.

In this study, CD-SEM measurement bias was evaluated by comparing cross-sectional CD measurements and/or critical dimension atomic force microscope (CD-AFM) measurements. Cross-section scanning microscopy (X-SEM) and scanning transmission electron microscopy (STEM) were used as cross-sectional CD measurement techniques. To evaluate the dependence of sample geometry on CD measurement

bias, gate line patterns with various line widths and sidewall angles were produced. The sidewall angle variation was achieved using etching under different conditions. CD-SEM and CD-AFM measurements, and then cross-sectional CD measurements, were taken.

A key challenge for the effective use of cross-sectional measurements is the development of an efficient sampling strategy, needed for the practical use of X-SEMs and STEMs, to take into account the effects of line edge roughness. In this study, statistically efficient cross-sectional sampling was decided on the basis of a line edge roughness evaluation made using CD-SEM and CD-AFM measurements. CD-AFM results were used to confirm the uniformity of sidewall profile along a line with edge roughness. The cross-sectional edge assignment algorithms for X-SEM and STEM images were determined by making simulation studies. CD-AFM measurement results were also used to validate Monte Carlo simulation of SEM/STEM images. We identified the advantages and disadvantages of three reference measurement techniques (CD-AFM, X-SEM and STEM) for very small structures for use in future devices.

To develop a bias correction algorithm, we investigated the relationship between pattern shape and secondary electron signal profile and confirmed that the CD bias caused by sidewall shape variation was consistent with our simulation results. On the basis of the experiments and the simulation analysis, we developed a bias correction technique for CD-SEMs. The technique estimates sidewall shape using the secondary electron signal, and corrects CD bias depending on the estimated sidewall shape. We compared conventional algorithms using this technique.

6518-164, Poster Session

Ellipsometric studies of the absorption of liquid by photoresist

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In situ spectroscopic ellipsometry, deep UV ellipsometry, and imaging ellipsometry were employed to study the absorption of liquid by photoresist(PR) used for 193 nm immersion lithography. When 125 nm thick PR was soaked in water over a period of \>30 minutes, ~5% increase in thickness was observed. From the analysis of ellipsometric spectra covering from near infrared to deep UV, we could estimates less than 2 vol.% uptake of water by PR after completion of soaking. This resulted in very small decrease in refractive index of PR(~0.4%). When imaging ellipsometry was used, the absorption of water by PR in much shorter periods could be detectible. In imaging ellipsometry, the microscopic images of (Δ, Ψ) in small area are obtained thanks to two dimensional multi-channel detection systems such as CCD. Using imaging ellipsometer, we could observe the interaction of PR with water even upon 1 s of contact. Also, we found that the water absorption or interaction was not uniform over surface. More studies are required for the implication of this observation. Obviously, imaging ellipsometry is a good technique to inspect water mark in immersion lithography. We also repeated similar experiments for high index liquid (JSR HIL-001) but to find negligible change by imaging ellipsometry.

6518-165, Poster Session

Advanced defect definition method using design data

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As Moore's Law indicates, pattern feature sizes have become smaller and smaller, increasing the need for more critical metrology and inspection methodologies in integrated circuit fabrication. Critical methodologies are especially required in the inspection area where more critical defect definition methods are needed for the accurate evaluation of inspection tools.

In traditional defect definition, we use only normal CD measurement results with manual measurement methods. These one dimensional definition methods gives only defect size information which is not enough information to do accurate evaluation. In addition, there is a lot of measurement uncertainty such as human errors, measurement errors, and systematic errors which are included in the data of manual measurement methods. Because of these mentioned issues, evaluation results will differ from person to person and other environmental influences.

On this paper, the defects will be defined not only with one dimensional measurements but instead with two dimensional measurements using such functions as Gap measurement and EPE (Edge Placement Error) measurement in DesignGauge using Design Data. For example, misplacement defects in which a pattern is shifted on the wafer as shown in figure 1; traditional one dimension measurement methods can not detect this type of defect. However, with DesignGauge, misplacement defects can easily be detected if the Design Data is used as in figure 2. EPE measurement method which is one of the advanced features of DesignGauge will very accurately define misplacement defects.

As the trends to smaller feature sizes in integrated circuit fabrication continues, various defects should be controlled and measured with advanced defect definition methods using Design Data.

6518-166, Poster Session

Image quality improvement in inspection optics using double integrator illumination

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As minimum feature size continuously shrinking, the performance of the pattern inspection systems with high numerical aperture is required to obtain the high-fidelity pattern images on the mask or the wafer. The complexity of the mask pattern, for example, has been rapidly increasing, because the pattern exposure systems have been performing under conditions of low-k1 factor. This mask pattern feature complexity leads to the mask inspection optics difficulties.

The most annoying problem disturbing the high-fidelity pattern images in the mask defect inspection systems is the existence of virtual images in imaging optics. The mask pattern is focused on an image acquisition sensor in the mask defect inspection system. The focused image pattern on the sensor includes two images, one is true image, and the other is virtual image. The virtual images are generated by the Köhler's illumination with the integrator (Figure 1(a)). This virtual image is theoretically derived from the periodicity of the integrator.

The improvement of image quality introduces higher defect detection sensitivity into the mask defect inspection system. To reduce virtual images, the double integrator method is applied to the illumination optics. By adopting the double integrator illumination method, virtual images disappear in the imaging field (Figure 1(b)). And due to the power density drop of bright spots, the resistance of lenses for working environments can be dramatically reduced at the stop position of objective imaging lens.

This paper reports the effects of the image quality improvement in the mask defect inspection system. The simulation results are shown when this method is applied to the advanced mask defect inspection system.

6518-167, Poster Session

The study of ADI (after develop inspection) by e-beam

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It has been reported by ITRS that generation with the technology node of hp45nm has to assure reduction of minimum 22nm sized defects. In consideration of that, it is thought that conventional defect inspection equipment using optical systems that are mainly used at present is incapable of detecting such 40nm defects. We previously reported that the detection of minor defects in a space on the resist pattern wafer is possible by using electron beam. In general, however, the amount of current for the defect inspection equipment with electron beam is over 1000 times that for CD-SEM, and it is concerned that the electron beam can damage the photoresist. Thus, we have examined the damaging behavior of electron beam regarding the material and structure of the resist by AFM, TOF-SIMS and FT-IR..

As a result, we have found out the mechanism of resist deformation and decomposition due to electron beam. We hereto also report that we could suppress the damage to ArF resist by defect inspection with electron beam to the extent equivalent to or less than that caused by CD-SEM.

6518-168, Poster Session

Three-dimensional anisotropic semiconductor grooves measurement simulations (scatterometry) using unconditionally stable FDTD for calculation time shortening

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At present, the scatterometry analysis is developed for the shape measurement in two-dimensional period line division made for the inspection. In the 3D analysis, the enormous calculation times were problems. In the last paper on Microlithography in 2004-2006, the 3D-FDTD analysis of the arbitrary shapes for vertical and oblique incidence was completed. The sub-grid and alternating-direction-implicit (ADI) methods are used for the time shortening analysis. The sub-grid method is carried out by the adoption to change the cell dimension into the 1/3 small lattice in the multilayer thin film parts. Then, the calculation speeds using the sub-grids become about 3 times faster than those of no sub-grids. Using ADI-FDTD algorithm, we show that it is possible to speed up the calculation time to one tenth. In this paper, we established numerical calculation techniques for the three-dimensional arbitrary cross section measurement equipment production by oblique incident light waves. Analytical models are periodic or isolated grooves, and also isotropic or anisotropic grooves. The light sources are plane waves and Gaussian beams. We use unconditionally stable (US) FDTD (Finite Difference Time Domain) method. In addition, we study the anisotropic mediums. The cell size of FDTD method must be small enough (<tenth part of wavelength) and the time-step size must satisfy Courant stability condition. If the time-step size is not within this bound, the FDTD scheme will become unstable. As a result, the FDTD method may require a large number of iterations. In this paper, the US-FDTD method based on the Crank-Nicolson scheme is proposed. The US-FDTD is an implicit method. It needs the matrix calculation. The matrix is simply solved in the tridiagonal matrix. In this method, the field components are defined at only two time steps. Compared to the ADI-FDTD method analyzed in the last year, the US-FDTD method has two advantages. (1) The left-hand and right-hand sides of the original updating equations are balanced (in respect to the time steps). (2) Only a single iteration that requires less number of updating equations is needed for the field development. The ADI-method required 4 time steps compared to 1 time step with the FDTD technique. Then, the numerical performance of the proposed US-FDTD method over the ADI-FDTD algorithm is demonstrated. It is possible to increase the time steps to 20. So, the new faster calculation time is one twentieth. Then, we analyze the FDTD method for the uniaxial anisotropy medium using the anisotropic PML (Perfectly Matching Layer). When we consider anisotropic conductive films, anisotropic etching for the silicon, liquid crystals and so on, the anisotropy analysis is needed. Then, the scattering characteristic from anisotropic medium is calculated. In this case, we use the Gaussian beam for no periodic and isolated grooves. Analyzing widths of the FDTD are required even in the vertical incidence over six times the spot size. Then, the scattering characteristics are examined using the spot size 0.2-1.0 microns and are also examined and scanned parallel by the beam for each shape grooves on the surface.

6518-169, Poster Session

Metrology of replicated diffractive optics with Mueller polarimetry in conical diffraction

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The micro- and nanostructures replicated from the mold into a metallized foil are widely used in the fabrication of security hologram labels for the identity documents, brand protection, etc. In the hot embossing replication technology the nickel shim is typically used to mold the sheets of formable material in order to obtain diffractive optical structures.

The replication tool itself is a result of electroplating of the nickel on the original surface of “master” diffraction gratings defined by the chosen optical design. The surface relief of the structure is quite complicated and the fabrication of “master” gratings can be very expensive. The metrology of this step of the replication process is a key factor to achieve low cost per replica. Optical techniques proved to be a good choice for the control of the grating dimensions and the shape of the profile, as they are fast and non-destructive.

We used novel spectroscopic Mueller polarimeter[1] to study the “master” gratings, made with electron beam lithography and wet etching in the polymethyl methacrylate layer, spin-coated on the chromium-covered glass substrate. Spectroscopic Mueller matrix coefficients of the special metrological test patterns, representing 1D sub-micron diffraction gratings, were acquired at the fixed angle of incidence of 55° at the different azimuthal angles. In conical diffraction the Mueller matrices of the diffraction gratings do not contain zero submatrices, consequently more extensive sets of experimental data can be obtained. The Mueller matrix coefficients of the same “negative” structures of the nickel replica were also measured. Experimental spectra were fitted with a RCWA code with symmetrical trapezoidal model of the grating profile.

Our approach significantly reduces the parameter correlations observed with standard spectroscopic ellipsometry in planar diffraction[2]. The calculated “optimal” values of the diffraction gratings parameters were in a good agreement with the results of AFM measurements for both “master” and replica gratings. The calculated profiles of the gratings for both samples are found to be complementary (Fig.1), given the specifics of electroplating process.

While the AFM measurements contain information on local topology of the sample surface, which can vary somewhat within the test pattern, the Mueller polarimetry provides the averaged values of the features size, which essentially define the visual quality of the resulting hologram. We showed that the Mueller polarimetry, as a fast and non-contact optical characterization technique, can be used for the verification of “master” gratings before molding tool fabrication step and for the on-line analysis of the final product.

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6518-170, Poster Session

Influence of wafer warpage on photoresist film thickness and extinction coefficient measurements

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Photoresist thickness and extinction coefficient are two important parameters in the microelectronics processing, and these two parameters can be estimated using simple setup of reflectrometry as shown in Figure 1. The literature consists of a number of different techniques for in-situ monitoring of photoresist properties in microlithography process including the use of in-situ ellipsometry, contact angle measurements, in-situ ultrasonic sensors, in-situ multi-wavelength reflection interferometers. The abovementioned monitoring methods work under the assumption that the inspected wafer is flat. Wafer warpage is common in microelectronics processing. Warpage can affect device performance, reliability and linewidth or critical dimension (CD) control in various microlithographic patterning steps. Warped wafers also affect the various baking steps in the microlithography sequence due to nonuniform air-gaps between the wafer and the hotplate. In this work, the influence of wafer warpage on photoresist properties is investigated. In particular, the photoresist extinction coefficient and photoresist thickness is of interest and can be extracted from a typical reflectance signal using different wavelength range as shown in Figure 2.

The experimental setup is shown in Figure 1. The sensor probe from reflectometer is positioned above the flat wafer or warped wafer with a distance of 5 mm normally pointing to the center to acquire the reflected light intensity. The whole sensor comprises a broadband light source (LS-1), fiber optics reflection probe (R200), and a spectrometer from Ocean Optics. The reflection probe consisting of a bundle of 7 optical fibers (6 illumination fibers around 1 read fiber) is positioned above the wafer to monitor the resist properties in real-time. The light from the broadband light source is focused on the resist through one end of the probe and the reflected light is guided back to the spectrometer through the other end. The reflectance signal collected by the spectrometer is transmitted to the computer, from which the resist properties including the resist thickness, extinction coefficient can be estimated via conventional optimization techniques.

In the studies, the photoresist used are Shipley 1813 (g-line resist) and SL4000 (DUV resist) from Shipley. The Shipley 1813 resist is spin-coated at 1000 rpm for wafer A, and 2000 rpm for wafer B. SL4000 resist is coated at 1000 rpm on wafer C. Experimental results are tabulated in Tables 1 and 2. We note that the estimation of resist thickness is relatively independent of the degree of wafer warpage as shown in Table 1. For the estimation of the resist extinction coefficient, the percentage deviation can be as high as 20%. It is thus important to compensate for the estimated resist extinction coefficient due wafer warpage. Based on the reflectance signals, the degree of wafer warpage can also be detected. These information can then be used for compensating or calibration of the estimated photoresist extinction coefficient. Table 2 also shows the calibrated extinction coefficient which is close to the actual extinction coefficient.

6518-171, Poster Session

Angular scatterometer for line-width roughness measurement

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The development of the semiconductor industry has created the need for reliable CD (critical dimension) and line width roughness metrology. According to the report of the semiconductor technology by ITRS 2005, the measurement solution of the line width roughness for the CD below 80nm is unknown. However the critical dimension for semiconductor devices shrinks to few tens of nanometers, the line width roughness becomes a critical issue because it degrades resolution and line width measurement accuracy. The roughness of gate width will influence the property of Vth (threshold voltage) and Ioff (leakage current) directly, and hence it causes fluctuations of transistors performances.

One kind of the measurement tool for the LWR (line width roughness) is AFM (Atomic Force Microscope), it can take a 3-D measurement over features in nanometer resolution. However AFM is limited by its measuring throughput for in-line process control. Another method for the LWR measurement is top-down CD-SEM. However it undesirably destroys what it measures when measuring multiple sites on a wafer. Also it does not take into account the sidewall variation along the height of the line structure. Thus it is difficult to obtain complete structure information of line width roughness using CD-SEM.

In this paper we propose angular scatterometry as a means to measure the line width roughness on photo resist structure. We establish a methodology to investigate LWR and CD using matching techniques. The grating sample is illuminated at fixed wavelength (633nm, HeNe laser) with a large angular aperture both in incidence thda and azimuth phi. A preliminary scatterometry model considering full range of varying phi and thda which was assumed that perfect CD printing without any LWR is built to fit the signature obtained from actual CD measurement with certain LWR. For comparison, the difference in the signatures indicates CD measurement error which is caused by LWR contribution. We further developed a calibration curve as a function of LWR based on the statistical quantity of the roughness variation. From the preliminary results indicate that scatterometry can indeed be the tool of choice to extract LWR and CD information in production with the resolution is about 3nm~5nm.

6518-172, Poster Session

Global and local SEM charging measurement using energy filter

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Wafer charging constitutes a long standing problem for CD-SEM metrology. As design rules continue shrinking, measurement errors caused by charging effects become more significant. Wafer charging can be generally divided into two categories: global and local. Global charging means that the wafer is charged during earlier process steps. These wafers are typically non-uniformly charged, where maximum magnitude of the charge might reach few hundreds Volts. Local charging is defined as the charge accumulation in insulating samples due to electron beam irradiation. The sign and magnitude of the local charging depends on the irradiation conditions and on the surface material properties.

Both local and global charges will be measured. The amplitude and typical variation length of global charge will be characterized across the wafer using few wafers. The behavior of local charge versus the scanned FOV and primary beam energy will be measured and analyzed.

6518-173, Poster Session

Contact leakage and open monitoring with an advanced e-beam inspection system

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Electron beam (e-beam) defect inspection becomes more important at 65nm and 45nm. Most application is extraction mode for P+/N-well contact open and N+/P-well contact leakage from piping defect. In this study , we found the optimized condition with retarding mode to detect N+/P-well contact open and P+/N-well contact leakage. This application can inspect more effective contact at same inspection time. Besides , we can detect P+/N-well leakage defect caused from un-optimized etch process. Finally we found the optimized contact process condition to eliminate contact open and leakage. E-beam inspection results strongly correlate with die yield. Electron beam (e-beam) defect inspection with retarding mode is a good inline monitor tool.

6518-174, Poster Session

New simple approach for modeling and on-line identification of piezoelectric stack actuator

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The problem of high-precision implementation and on-line identification of SPM's scanner model is studied in order to scanning small size sample/features using scanning probe microscopes (SPM), such as the image or measurement for linewidth on semiconductor chip less than 100nm.

A simple mathematical model is proposed to precisely describe the characteristics of hysteresis and creep, which can be used in the analysis and design of real-time controlling systems.

One of fundamental components of SPM is scanner, which most utilizes piezoelectric ceramic actuators to generate a scan movement between probe and sample. Piezoelectric stack actuators are monolithic and have many advantages such like excellent resolution, no sliding or rolling parts, no mechanical friction or backlash and high thermal stability and so on. So they are best suited as drivers in nano-positioning systems. But unfortunately piezoelectric ceramic is known to exhibit strong hysteresis and creep between the input voltages and the output displacements in the uncompensated open-loop operation. The hysteresis and creep can reduce the positioning precision of scanner and even produce a distortion in scanning images, which are intolerable for the high-precision imaging and measurement using SPM, and these effects must be eliminated.

The feedback control has widely used to compensate nonlinear of piezoelectric stack actuator (PESA). As has been said before, PESA has nearly infinitesimal resolution in theory. However, it is considerably difficult and impractical to fabricate the displacement sensors with so

high resolution, particularly for high bandwidth applications. But in any closed loop projects the control accuracy can never be better than the resolution of the measurement sensor. Thereby in feedback case, the high resolution of PESA may be deteriorated due to the noise of sensors in the system. That is to say, the feedback control is not suitable to the application of high resolution SPM scan. Obviously this effect is absent in the open loop case, so higher resolution of SPM scan can be gained in this case.

For open loop control piezoelectric stack actuator, different models have been proposed to describe the characteristics of hysteresis and creep of piezoelectric stack actuators. For example, Preisach model which approximates the hysteresis with a set of relay operators, can achieve 2~5% precision on longer range. Despite of these advantages, the large set of relays that is necessary for higher accuracy makes it difficult to implement and identify online. In addition, the error which is introduced by the model parameter and interpolation can have an impact on the positioning precision of SPM's scanner. At the same time, in the viewpoint of control systems, studies only on the actuators are not enough. When an actuation system is integrated with complicated particular SPM's scanner, such as flexure-based parallel kinematics mechanism, because of various mechanical variations, errors resultant from the fabrication and the interaction between actuators and mechanism, each SPM's scanner can contribute the uniqueness and complicacy of the dynamics characteristics. We believe that it's preferable to study the complicated phenomena such as hysteresis and creep based on physical experimental results. Also, the combined systems of actuation and mechanics are practically much more useful for the design of control systems. And when they are identified online, they are probably much more accurate.

To get the nano-scale resolution using SPM, open control scheme based on system model can be considered. So the hysteresis and creep model of piezoelectric actuators is presented in this paper.

Both in the experimental and theoretical analysis show that PESA's voltage-displacement hysteresis loop present all-right repeatability in the excitation signal of changeless peak-to-peak value and frequency, which correspond to control signal for horizontal direction of SPM's scanner. So in this paper two fitting multinomials are respectively approximated the growth and drop curve of hysteresis loop. Because of the hysteresis is asymmetrical and nonlocal memory, the model parameters need be gained in the same stimulated conditions as the actual scanning course. In this paper the online identifier is presented: one pre-scanning periods is increased before actual scanning, coefficients of multinomial are identified in this period, thus the hysteresis model is established, which is coincident with the hysteresis curve in the actual scanning course.

Generally it has been known that the creep curve has a logarithmic shape for time. But the parameters of model are not easy to get. Moreover the problem such as different properties of each scanner and PESA's aging etc result in changes of model parameters. Therefore the relative creep model and method for identifying parameters is presented.

In addition to the hysteresis and creep of piezoelectric stack actuator, behaviors of flexure-based parallel kinematics mechanism also are included to this model. Furthermore, because of simple and little computation cost of model these models are easy to use in an open-loop control scheme, which has a higher resolution than closed-loop operation for scanning small scans/sample features.

Model formulation is validated by comparing results of numerical simulations to experimental data, which demonstrate the validity of the method. Finally validation is followed by a discussion of model implications for purposes of actuator control.

6518-175, Poster Session

Understanding of CD change effect by rework process induced in sub-65-nm and its optimization to minimize

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The CD control tolerance is getting smaller when technology node for semiconductor is approaching to small design rule. In general, to achieve better CD control, we try to minimize lithography error sources such as track, scanner, mask, metrology and so on. We have not been interested in rework process effect which is one of process steps in lithography. In lithography, rework process is very important step since it makes wafers take lithography process again. We assume that we use same expose condition to get same CD between before rework and after rework since process conditions were still same. However, we observed that CD was changed after rework even if we used same process conditions.

We did experiment to understand the causes of this phenomenon. Our experimental results explain rework process is the root causes for CD change. Also we observed that the amount of CD change is not negligible. Therefore, in this paper, we will investigate its mechanism and method to optimize rework process for sub - 65 nm.

6518-176, Poster Session

Study on micro-bubble defect induced by RRC coating

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RRC (Reducing resist consumption) coating is widely used to reduce photo resist consumption. By using solvent to pre-wet the wafer surface, photo resist can be coated on wafer easier than normal coating method. But it also can be the source of defects. In this study, we found that RRC solvent will induce micro-bubble and cause defects. Different methods had been tried to solve this kind of micro-bubble defects. Results showed that micro-bubble defects can be found when the wafer is static during RRC solvent dispense. And the defect map was a ring shape. The diameter of the rings depended on the RRC solvent dispense amount. Non micro-bubble defect was found, if wafer was spinning during RRC solvent dispense.

6518-178, Poster Session

Characterization of resist thinning and profile changes using scatterometry

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Scatterometry is emerging as a prominent metrology technique for lithography. Not only does scatterometry produce line profile information such as sidewall angle and height along with line width, but the speed and nondestructive nature of scatterometry accommodates in-line process applications. Scatterometry systems employ reflectometry or ellipsometry to acquire spectra resulting from the interaction of the input radiation and a symmetrical grating array. The systems may use fixed wavelengths or a range of wavelengths. The output spectral data is dependent on the material and physical properties of the grating array and surrounding (subsurface, film stack) material layers. Typical scatterometry draws on mathematically modeled spectra from known optical and physical parameters such as the grating pitch and the index of refraction and absorption coefficient functions of the film stack materials. The optical properties of the materials in the film stack are of particular interest and critical to scatterometry. Material vendors typically supply constants associated with the optical dispersion models of resists and anti-reflective coatings used in lithography. These constants are most often based on a Cauchy model for optical dispersion, a very simple model. However, the optical properties of the photoresist or other coatings may not fit well to a Cauchy model or they may change during process baking, exposure or just from aging. To make an accurate scatterometry model for patterned photoresist, the material characteristics must also be modeled. Using these parameters, an accurate picture of the lithographic materials can be generated. These methods can be applied to both dry and immersion lithography.

As immersion lithography gains a foothold in the manufacturing line, many initial processes will use standard dry photoresist with the application of an immersion topcoat to protect the final lens element of the lithography tool, and to reduce defects formed from substances leaching out of the photoresist. Although the goal for an immersion topcoat it to be neutral to the resist process in terms of profiles, process windows, and CD control, many topcoats are not completely benign. Topcoat induced resist thinning is a common but unwelcome attribute.

In this paper we discuss the use of scatterometry to characterize topcoat induced thinning, and use this technique to evaluate several commercially available products. We will also demonstrate the ability of scatterometry to accurately determine resist profile changes as a result of focal changes, topcoat interactions, and airborne contamination. Measurement stability results are also shown, and correlation to CD-SEM and cross-section SEM are provided as a reference metrology.

6518-179, Poster Session

Contamination removal from collector optics and masks: an essential step for next-generation lithography

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The cleanliness of surfaces, whether they are the collector optics or the EUV reticles themselves, is an important aspect for the implementation and advancement of EUV technology. The focus of this paper will be towards finding a potential solution for two equally important problems facing EUV lithography: the removal of tin debris from collector optics as well as the removal of particle contamination from EUV masks. In a Sn EUV source, Sn debris leads to the degradation of the collector optics. Thus, the cleaning of collector optics contaminated with Sn debris is essential for successful lithography and to minimize the cost of ownership of an EUV tool. The cleaning technique used in the present work uses reactive ion etching, where the halide ions, eg. Cl2 can chemically react with Sn to form volatile products that can be easily removed. Results on the selectivity of Sn over SiO2 and Ru are obtained and are very promising towards the cleaning of Sn off of EUV compatible collector mirror surfaces. A simulated collector geometry was constructed and experiments were performed to clean Sn coated samples placed at different locations on the collector. The result allows us to understand the physical processes and helps us to perform a realistic modeling based on the geometry of collector shells. Equally important is the removal of contamination from the EUV reticles. While an EUV compatible pellicle is being researched, cleaning of masks in EUV lithography will be an important aspect to improve wafer throughput as well as to again reduce the cost of ownership. A novel process for removing contamination from EUV reticles is a non-contact/ dry cleaning technique called Plasma-Assisted Cleaning by Electrostatics (PACE). PACE is a technique that utilizes charge imbalances to remove particles perpendicular to the surface. The particles are charged using a weak local plasma, then the plasma sheath potential is suddenly modified which magnifies the electric field in the sheath region and propels the negatively charged contamination from the surface. Current results for the cleaning 30 nm - 220 nm polystyrene latex simulated contamination yield 90 % removal efficiency with no damage to the surface of the sample. Results showing the removal of nanometer scale contamination from EUV simulated materials will be presented as well as the damage assessment and mitigation.

6518-180, Poster Session

Measurement and experimentation of pellicle's life time on photomask

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The minimum feature size of the semiconductor device will be smaller and smaller because of the increasing demand for the high integration of the device. According to recently proposed roadmap, ArF immersion lithography will be used for 65 nm to 45 nm technology nodes. In exposure process, the pellicle's adhesives on the mask is becoming the serious matter and problem in semiconductor industry. Various material contribute to photomask and pellicle formation including : chemical residuals from mask cleaning, out-gassing from pellicle glue/materials, and contaminants from the scanner ambient. Pellicle's life time is important to exposure process and is affected by exposure intensity.

In this research, we consider the life time of pellicle by intensity and position of exposure. We used 193 nm (ArF) excimer laser and measured pellicle's adhesive strength on the mask and pellicle life time. [fig. 1] We investigated binary intensity mask with 193 nm ArF lithography for pellicle's life time study by changing the transmittance and exposure intensity.

6518-181, Poster Session

A new SEM CD operator verified against Monte Carlo simulations

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Scanning Electron Microscopy (SEM) is a standard method for Critical Dimension (CD) metrology of nanostructures, combining high resolution imaging with short image acquisition time. However, due to the complex process of image formation SEM images require careful interpretation and appropriate algorithms for CD evaluation.

Monte Carlo simulation programs are useful tools to investigate SEM image formation as well as to create synthetical SEM images of nanostructures for testing CD evaluation algorithms.

A new algorithm for SEM CD evaluation of trapezoidal line structures is presented. It is based on the physical modeling of SEM image formation and allows the assignment of top and bottom structural edge positions to the SEM signal. Extensive series of Monte Carlo simulation were used to derive basic functions which describe SEM image profiles for line structures. This set of piecewise continuous functions is convoluted with the electron probe intensity profile. The resulting function is fitted to the measured signal profile by a least squares algorithm. The fit returns both top and bottom edge positions as well as the electron probe diameter.

The algorithm is verified against different Monte Carlo simulation programs using different physical models of elastic and inelastic electron scattering and secondary electron generation and transport. The effect of the physical modeling on the evaluated critical dimension is discussed and the absolute CD deviation of the algorithm is determined for different sets of structural parameters like edge slope angle, material, and electron probe diameter.

6518-182, Poster Session

Characterization and adjustment of high-performance objectives for DUV applications

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Aside from steppers also inspection systems in the semiconductor industry require DUV imaging optics with very high optical requirements.

A test and adjustments set-up based on the Shack-Hartmann wave front sensor for objectives and telescopes is presented. It allows primarily to characterize the image quality of systems under test for both finite as well as infinite object and image distances.

From the wave front the modulation transfer function, point spread function or encircled energy data can be derived. Also, other data such as magnifications, focal lengths and even distortion with micrometer accuracy can be obtained with the test bench.

The test system consists of a spherical waves generator, the sensor including adapting optics and the mechanical motion system. It is highly motorized and all essential functions are computer controlled. The available wavelengths currently range from 193nm to NIR.

Example results for various systems will be presented.

6518-183, Poster Session

Phame(tm): a novel phase metrology tool of Zeiss for in-die phase measurements under scanner relevant optical settings

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Meeting the demands of the lithography mask manufacturing industry moving toward 45nm and 32nm node for in-die phase metrology on

phase shifting masks, Zeiss is currently developing an optical phase measurement tool (Phame(tm)), providing the capability of extending process control from large CD test features to in-die phase shifting features with high spatial resolution.

In collaboration with Intel, the necessity of designing this optical metrology tool according to the optical setup of a lithographic exposure tool (scanner) has been researched to be fundamental for the acquisition of phase information generated from features the size of the used wavelength. Main cause is the dependence of the image phase of a scanner on polarization and the angle of incidence of the illumination light due to rigorous effects, and on the imaging NA of the scanner due to the loss of phase information in the imaging pupil.

The resulting scanner phase in the image plane only coincides with the etch-depth equivalent phase for large test features, exceeding the size of the in-die feature by an order of magnitude.

In this paper we introduce the Phame(tm) phase metrology tool, using a 193nm light source with the optical capability of phase measurement at scanner NA up to the equivalent of a NA1.6 immersion scanner, under varying, scanner relevant angle of incidence for EAPSMs and CPLs, and with the possibility of polarizing the illuminating light. New options for phase shifting mask process control on in-die features will be outlined with first measurement results.

6518-184, Poster Session

Nonlinear methods for overlay control

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Overlay requirements for DRAM devices are decreasing faster than anticipated. With current methods overlay becomes ever harder to control and therefore novel techniques are needed. This paper will present an alignment based method to address this issue. The use and impact of several non-linear alignment models will be presented. Issues here include the number of alignment marks to use and how to distribute them over the wafer in order to minimize the throughput impact while at the same time providing maximum wafer coverage. Integrating this method into a R2R environment strongly depends on the stability of the process. Advantages and disadvantages of the method will be presented as well as experimental results. Finally some comments will be given on the need and feasibility of wafer by wafer corrections.

6518-185, Poster Session

Leveraging LER to minimize linewidth measurement uncertainty in a calibration exercise

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National Institute of Standards and Technology, Gaithersburg, MD 20899. ABSTRACT. Many semiconductor metrologists are aware 1, 2 that the contribution of Line Edge Roughness (LER), and thus Linewidth Variation (LWV), can be a significant contributor to measurement uncertainty budget. More generally, the impact of measurand variation and proper sampling is becoming a major player in nearly every area of semiconductor measurement 3. This paper describes a simple technique of using the LER of a linewidth as a fingerprint to uniquely characterize the measurement target in such a way to make the LER contribution negligible in a linewidth calibration exercise. The Single Crystal Critical Dimension Reference Material (SCCDRM) 4 was the calibration artifact used to calibrate a CDAFM. The SCCDRM contains 6 different linewidths varying from 100 nm to 270 nm. The paper shows in detail the overlay of the CDAFM linewidth data with that of the data used to calibrate the SCCDRM for each linewidth. An example of this overlay is shown in Figure 1. With the aid of this linewidth fingerprinting, Mandel regression is used to assess the quality of correlation of the CDAFM to that of the NIST-derived calibration data. As a final assessment, a NIST uncertainty budget analysis is presented as a conclusion of the calibration exercise. Absolute accuracy of less than 2 nm with a k=3 coverage factor was achieved. Keywords: linewidth, calibration, LER, uncertainty, metrology, LWR, CDAFM, SCCDRM, NIST. 1 Dixson, R. et al, “CDAFM reference metrology at NIST and SEMATECH,” Proc. SPIE Vol. 5752, Metrology Inspection, and Process Control for Microlithography XIX, Richard M. Silver, Ed., 2005, Pp. 324-336. 2 Villarrubia, J. et al, “Scanning electron microscope analog of scatterometry,” Proc. SPIE Vol. 4689, Metrology Inspection, and Process Control for Microlithography XVI, Daniel J. Herr, Ed., 2002, Pp. 304-312. 3 Mayer, J. et al, “New apparent beam artifact and measurement methodology for CDSEM resolution monitoring,” Proc. SPIE Vol. 5038, Metrology Inspection, and Process Control for Microlithography XVII, Daniel J. Herr, Ed., 2003. 4 Dixson, R. et al, “Traceable atomic force microscope dimensional metrology at NIST, Proc. SPIE Vol. 6152, Metrology Inspection, and Process Control for Microlithography XX, Chas N. Archie, Ed., 2006.

6518-186, Poster Session

A new AFM tip design which provides higher sidewall resolution (LER and CD) and better tip wear

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Improving device’s performances is one of the primary goals of microelectronic R&D. Technological steps such as lithography, gate and interconnect etching need excellent CD metrology repeatability in order to maintain production yield. However, in R&D we have reached such small dimensions with typical transistor gate length below 30nm that the accuracy of CD metrology is becoming mandatory in addition to precision otherwise final processes will not be sufficiently reliable.

In this paper we present a recent improvement in the CD-AFM tip design and tip material type, which we have demonstrated to improve sidewall resolution (Bottom CD and LER) and tip wear. Therefore, the accuracy and precision of the CD-AFM technique is immediately impacted.

6518-187, Poster Session

Köhler illumination analysis for high-resolution optical metrology using 193-nm light

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One primary mechanism for extending optical overlay and CD (critical dimension) metrology to sub-micrometer targets employs shorter wavelength of light sources and higher numerical aperture. In addition the techniques for improving both illumination and imaging systems are becoming important as target sizes decrease so that accurate preparation of illumination is becoming more critical for high-resolution optical metrology applications such as linewidth and overlay measurements. Some enhancements and analysis in optical metrology were reported by modifying Köhler illumination which is used widely in the modern microscopy [1-4].

In order to characterize the Köhler illumination, we proposed Köhler factors defining Köhler factor 1 as homogeneity in the spatial field intensity (KF1), Köhler factor 2 as homogeneity in angular intensity (KF2), and Köhler factor 3 as homogeneity in wavefront (KF3), and the field aperture pattern transfer method which analyzes the intensity distribution of the illuminating light in the defocused field plane by placing a patterned aperture in the field stop position [5].

Now we have designed an optical system for high resolution optical metrology using ArF excimer laser of a wavelength of 193 nm to have the capability of analyzing the Köhler factors for shorter target sizes. Illuminating and imaging paths were designed based on a catadioptric objective lens of 0.75 numerical aperture and 8 mm working distance, DUV CCD camera of 14 x 14 μm2 pixel size, and DUV synthetic quartz fiber for delivering the beam going out from the light source separated from the optical table, considering the fluency of light energy. Fig. 1 shows the estimated minimum light energy fluency which was designed by the energy sensitivity of the CCD camera.

In this study the characteristics of Köhler illumination were investigated by using the field aperture pattern transfer method with respect to systematic variations such as the shape of the source, the intensity distribution asymmetry at the conjugate back focal plane, the displacements of elements along and off the optical axis, and the wavefront of the angular illuminating beams. We also studied methods resulting in near collimating beams upon the field plane to investigate the

effect of angular components of the illumination.

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6518-188, Poster Session

Critical dimension: MEMS road map

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MEMS applications are getting more and more important in areas such as accelerometers, mechanical devices, biotechnology, optics, communications, and RF to name a few. The MEMS dimensions are getting smaller and processes are facing new challenges in term of critical dimension measurements. This paper will examine the needs and challenges MEMS processes are facing in term of critical dimension measurements. An automated optical CD tool with the advantages of non-destructive methods, high throughput and precision is a good approach to answer these new measurements requirements.

6518-189, Poster Session

Enabling gate etch process development using scatterometry

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Within the past few years, scatterometers have been embraced for many in-line measurement and disposition applications in the semiconductor industry. Yet, there remains some hesitation to fully rely on scatterometry for advanced process development, and instead to depend on CDSEMs and traditional failure analysis imaging methods (cross-section, TEM, FIB) to provide CD as well as profile information. This paper investigates whether scatterometry can be used as a suitable tool to supplement and sometimes replace XSEM metrology, and is an extension of the work from M. Sendelbach et. al. entitled "Improving STI etch process development by replacing XSEM metrology with scatterometry" from the 2005 SPIE Microlithography conference. A very large number of cross-sections were completed on the scatterometry grating targets as well as in-line disposition targets (figure 1) and compared to optical measurements of the gratings with the purpose of decisively answering this question. The targets used for this work were etched 65nm node NFET gate structures (figure 2). Measurements from cross-sections and scatterometry were processed to understand the top CD, middle CD, bottom CD, and sidewall angle; profile characteristics such as footing and/or notching were also evaluated.

The investigation led to some interesting results, such as the existence of significant variation within a grating. In fact, there was enough variation to indicate that one or a few cross-sections may not represent the actual process or the 'average' state of an array of lines, making XSEM metrology a poor quantitative method when used for process development. Scatterometry measurements of top, middle, and bottom CDs show excellent correlation to cross-section results (figures 4 and 5) of both the grating and disposition targets. The profile characteristics correlation results require a more in depth study, as further discussed in this paper.

6518-190, Poster Session

Extending high-speed optical metrology less than 20-nm resolution with stimulated emission depletion-stimulated anti-Stokes Raman spectroscopic imaging (sted-STARS)

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Optical metrology has been the workhorse for high speed, high resolution metrology of semiconductor metrology. However, as feature sizes fall below 50nm optical metrology has become more difficult. Presently averaging model based techniques such as scatterometry are gaining popularity for overlay and critical dimension analysis even thought there results are strongly dependent on the assumptions of the scattering models. Here we present a new molecular imaging modality based upon the combination of Stimulated Emission Depletion (STED) imaging, Quantum vibrational state population control and stimulated Anti-Stokes Raman Scattering called (sted-STARS) can be used to directly image molecular transitions in various semiconductor materials with better than 20 nm resolution at high speed. This is the first suggestion to merge two previously independent recent microscopy developments; the use of short laser pulses to perform Anti-Stokes Raman Spectroscopy and STED microscopy image resolution enhancement techniques previously only used for deep sub-wavelength imaging in fluorescent microscopy. STED techniques overlay two images of the same feature, but at different wavelengths and different phase distributions in the focal spot of the beam. One image is diffraction limited Gaussian, while the second image is phase modulated in the Fourier plane to produce an annular or railroad track shaped image at a longer wavelength that stimulates excited states in the surround region of the annulus back to the ground state vibrational manifold. The result of this exposure process is to narrow the width of the feature image. The more intense the surround excitation, the narrower the image feature Like ordinary Raman spectroscopy sted-STARS may operate as an electronically resonant for enhanced sensitivity or as a non-resonant imaging technique. Scanning, high resolution deep sub-wavelength sted-STARS imaging systems will have many applications in semiconductor manufacturing metrology. Resist latent images, overlay between layers, and strained Silicon at the gate level may be measured. It is possible to consider that all Raman active thin molecular films, such as SiO2, SiN, and low k dielectrics, may be characterized with <20 nm resolution for gate level diagnostics. In the future sted-STARS may become the imaging technique of choice for metrology on nano-scale molecular devices based upon materials such as carbon nanotubes and silicon nanowires.

6518-191, Poster Session

ArF pellicle degradation mechanism for resolving CD variation

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In ArF lithography era, the high resolution pattern embodiment becomes more practicable but it is actuality that photo-induced defect is accelerated by ArF laser's high energy by the counter-presentation. Specially, defect called as haze that is known inorganic crystal has characteristic that grow fast being influenced to high energy. This photo-induced defect exerts effect that reduces photomask lifetime and high impact on productivity negatively.

Recently, extensive studies that are willing to seek for countermeasure about haze have been performed through various researches with especially photomask cleaning process improvement. However, because a PSM mask is still weak to haze, a binary mask is preferred in ArF lithography. But, a new problem was happened after binary mask introduction. The center to edge CD variation in a lithography shot is appeared and in progress of exposure process, CD variation difference is gradually grown. And finally, CD variation difference grown considerably causes defect in wafer level. It can be inferred that the transmittance of reticle is closely related to CD variation because the center to edge transmittance of the reticle where CD variation is detected has some differences. However, the close examination searching mechanism about pellicle degradation that is expected to directly give influence in reticle transmittance change has not been

achieved. Therefore, this study focuses on identifying the pellicle degradation mechanism directly influencing on the reticle transmittance change so as to solve the ArF mask CD variation problem hereafter.

Pellicle is a thin organic film that is consisted of the element C, F, O bond. Because C, F, O single bond energy are smaller than ArF laser energy, the atomic bindings of several shape that compose the pellicle curtain can be expected to be expired by ArF laser. Pellicle degradation experiment using ArF laser acceleration exposure equipment was conducted to certify that the most atomic bonding composing ArF pellicle can be dissociated. In the experiment result, it is confirmed that the fluorine is outgassed from the pellicle. Analyzing the pellicle in mass production experiencing CD variation, it is verified that the pellicle transmittance was fallen on the whole pellicle. Also, the pellicle thickness became thinner physically that proved that the pellicle transmittance decline is caused by the dissociation of the atomic bonding in pellicle. In conclusion, carbon or fluorine outgassed from the pellicle by ArF laser high energy is adsorbed in reticle pattern side to reduce the transmittance of the reticle and at last CD variation is generated. In order to diminish the CD variation impact, the following action must be accomplished, that are the ArF laser damage minimization, the degree of purity of pellicle maximization and the absorption of outgassed component in reticle pattern minimization.

6518-192, Poster Session

Effect and procedures of post-exposure bake temperature optimization on the CD uniformity in a mass production environment

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Controlling a very tight CD budget in Photolithography is one of the challenges of the next technology nodes. The Post Exposure Bake (PEB) process is known as one of the main Litho contributors to CD non-uniformity for processes using resists with moderate or high PEB sensitivity. However, to achieve a tight CD uniformity plate to plate (PtP) and within plate (WiP) - the current temperature calibration procedures of PEB plates will not be sufficient enough to fulfil the requirements for future technology nodes.

Other influences than the static temperature of the plates contribute to CD as well. This is shown in the present paper by comparing the temperature of the PEB plates to wafer CD.

Coater / developer software was developed that utilizes a mathematical model based on scatterometry CD data and PEB sensitivity of the resist - allows an accurate PtP and WiP CD uniformity adjustment. Compared to the conventional time consuming temperature calibration procedures the CD Optimizer can improve the CD uniformity significantly - and it saves lots of productive time.

This method already has been confirmed by using bare Si wafers [1]. We will show for the first time the effect of the CD optimization on the CD uniformity of production wafer in a high volume memory FAB. We did analyse CD mass production data obtained from inline scatterometry measurements before and after optimization of the PEB plates. We can also show that it is possible to use inline mass production data for the PEB temperature optimization directly.

[1] ArF scanner performance improvement by using track integrated CD optimization

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6518-193, Poster Session

Qualification and analysis of scatterometry measurements of polysilicon gate profiles in a 90-nm logic process

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Scatterometry data were acquired on test wafers patterned on full-loop production routes, with etched polysilicon profiles intentionally skewed across wide CD and profile shape ranges, bracketing the process center, with nominal 70 nm linewidths. Scatterometry profiles were benchmarked by overlay on discrete cross-section SEM images. Polysilicon linewidth and profile shape correlations were established across wide process skews to both average top-down SEM and End-of-line Electrical Test (E-Test) data by global non-linear fits across hundreds of individual profiles. Sub-Angstrom scale matching of bottom CDs, at $P/T < 0.02$, was demonstrated between two production metrology tools in our fab by long-term precision measurements. Scatterometry measurements were made with commercial Rotating-Compensator Spectroscopic Ellipsometers (RCSEs), with regression performed on four independent spectral components of 0-th order diffracted signals from grating test structures. Profile regression and analysis were based on both real-time parallel computations, and on pre-computed databases. First-order analyses of profile parameter error propagation, correlations, and sensitivities were made using computed databases and measured spectral covariance matrices for the four signal components. Calculations of measurement uncertainties for polysilicon linewidths agreed with long-tem cross-tool 0.1 Angstrom 1-precision measurements.

6518-196, Poster Session

Mask CD control (CDC) with ultrafast laser for improving mask CDU using AIMS as the CD metrology data source

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CD uniformity control by ultrafast laser system writing inside the bulk of photomasks has previously been shown to be an effective method for local CD control (CDC) (1).

Intra-field CD variations correction has also been shown to be implemented effectively in mask-shops and fabs based on CDC SEM (2, 3) and OCD as the CD data source. Using wafer CD data allows correction of all wafer field CD contributors at once, but does not allow correcting for mask CD signature alone. In case of a mask shop attempting to improve CDU of the mask regardless of a particular exposure tool, it is a better practice to use mask CD data by itself as the CD data source.

As an alternative to the use of wafer CD data, which contains both mask and exposure tool CD signatures which may be difficult to separate, we propose to use an areal imaging system (AIMS Fab 193) as the CD data source for the CDC process.

CDU maps and data analysis with an AIMS tool was performed on test masks. The CDU map was converted into a laser patterning attenuation map which was written with the laser into the photomask bulk in the form of shading elements. The shading elements correlated in density to the required attenuation level in each zone of the mask. The effectiveness of the CDC treated mask was then verified using the same AIMS capability, and improved intra-field CD-Uniformity was confirmed.

The CDC process implementation requires an exact correction factor (CDC Ratio) for the relevant lithography process. The CDC Ratio is effectively the ratio of CD to transmission attenuation.

It was shown in this investigation, that by applying the correct CDC Ratios, an AIMS tool could characterize effectively the full process of mask CD uniformity improvement done by an ultra-fast pulsed laser CDC tool.

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6518-197, Poster Session

Verification of CHARIOT Monte Carlo software used for modeling of CD-SEM and defect inspection

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Simulation and optimization of the performance of e-beam systems such as CD-SEM and defect inspections is possible using accurate Monte Carlo modeling. CHARIOT software uses advanced physical models to simulate electron scattering in targets, electron trajectories, and signal formation in SEM. It was used to predict CD-SEM images in linewidth measurements; variable errors subject to beam and pattern parameters were found on the top of systematic errors;1 this is why the cross-correlation of SEMs is a big issue. Calibration of CD-SEMs and other e-beam systems is possible, however, the software has to be verified. In this work, we present experimental verification of CHARIOT using new and published experimental data.

The most important parameter is coefficient of secondary emission for various materials in a wide range of electron energies. The secondary emission was calculated and compared to a database.2 Measurements provided by researchers for over decades at various conditions of surface quality and vacuum resulted in a significant spread of results. New measurements were carried out for materials used in microelectronics. To assure the absence of contaminations, ion beam cleaning of the surface was provided immediately before the measurement; high vacuum was used. The results of simulation and experiment showed reasonable agreement for materials used: Si, SiO2, Al, W, and Cu.

Electron penetration through thin films is an important factor. CHARIOT is able to simulate transmission coefficients, and moreover, electron spectra of the transmitted electrons. Simulated spectra for electrons transmitted through gold films of various thicknesses were compared to experimental data. It was found that CHARIOT advanced model predicts the spectra really well, while simpler Monte Carlo models based on Bethe-Rutherford models are way off.

Examples of simulation for CD-SEM are presented along with experimental results. Edge of a line and linewidth was measured and simulated; results were compared and discussed.

Simulation of linewidth measurement errors was demonstrated in CD-SEM. In defect inspection, beam diameter was identified to be able to catch defects of specific size.

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6518-198, Poster Session

Operator independent measurement of beam size using BEAMETR technique

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Monitoring and tuning the beam size is critical for any electron-beam system. The performance of defect inspection systems, electron beam lithography (EBL) systems and scanning electron microscopes (SEM) depends greatly on beam size. Knife edge method usually used for beam size measurement is time consuming and inaccurate; the results are operator dependent. Analytical methods based on Fourier transform analysis were developed;1 which showed that the measurement can be done in a more precise way. Still, an operator had to determine the beam size out of the spectral data, which can involve an operator dependent error.

In this paper, a technique is described to determine beam size and shape automatically using a simple procedure. BEAMETR is a product involving software and a specially designed pattern. In the developed method, the pattern is scanned using an e-beam. A spectra of the signal is analyzed; beam size is automatically determined using a software program. While being a quite complex in both fabrication and analysis, the technique is really easy for end user.

Results of design, fabrication, and analysis of the beam calibration test pattern are presented. A specially designed and fabricated test pattern is used. The design includes optimization of the pattern with regards to its spectral characteristics, as well as a targeted range of beam diameters and deflection system characteristics.

The analysis uses an advanced model solving an ill-posed mathematical problem. The math works with patterns and SEM images that may involve fabrication inaccuracies and distortions. The software includes an image recognition module, in order to determine a specified portion of a test pattern, which is used for spectral analysis. Noise reduction technique and contrast enhancement are also used. The model allows one to examine the edges of signal spectra that are important when beam size is small. This technique enables automatic measurement of beams one order smaller than the minimum feature size of a test pattern.

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Conference 6519: Advances in Resist Materials and Processing Technology XXIV

Conv. Ctr. Hall 3

Monday-Wednesday 26-28 February 2007

Part of Proceedings of SPIE Vol. 6519 Advances in Resist Materials and Processing Technology XXIV

6519-01, Session 1

Identifying the materials limits of chemically amplified photoresists

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The development of new lithography approaches and materials to fabricate ever smaller feature sizes is the key enabler and driver for the continued performance increases of integrated circuits. Although the current leading technology, chemically amplified photoresists, is amazingly capable of fabricating sub-100 nm features, there are numerous technical hurdles facing the fabrication of sub-50 nm features with sufficient resolution and reproducibility. The development of photoresist materials for use at these nanometer length scales requires new measurement methods to better understand the physical phenomena that may limit their future success.

In collaboration with industry, we have developed and applied unique high-resolution metrology tools such as x-ray and neutron reflectivity (XR, NR), small angle neutron scattering (SANS), and near edge x-ray absorption fine structure (NEXAFS) to address fundamental questions facing chemically amplified photoresist materials from the formation of the latent image to its development. I will highlight aspects of our work including: 1) the direct measurement of the reaction-diffusion front with nanometer resolution from ideal line-edges to probe image blur and roughness from photoacid diffusion 2) measuring the three-dimensional “shape” of the reaction-diffusion path induced by a diffusing photoacid 3) identification and measurement of a “residual swelling fraction” during the development process and its potential impact on photoresist resolution. Insights from these studies may provide potential guidelines and opportunities for the further extension of chemically amplified photoresist technology into the future.

6519-02, Session 1

Emerging resist materials

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How far can we extend optical patterning? At the November 1992 Semiconductor Technology Workshop, the demise of optical patterning was projected to occur in 2001, after the 180 nm technology node. This corresponded to nine years or three technology nodes, n+3, out from the then current 500 nm technology node, n. The 1994 and 1997 National Technology Roadmaps for Semiconductors (NTRS) conveyed similar messages, that optical lithography would end after the 130 nm and 100 nm generations, respectively, or n+3 nodes out from the current technology nodes. The 1999 and 2003 International Technology Roadmaps for Semiconductors (ITRS) also predicted lithography’s end n+3 technology nodes out from the current 180 nm and 90 nm nodes, respectively. The 2003 and 2006 ITRS potential solutions roadmaps for exposure tool technologies suggested that optical lithography would not be viable beyond the 32 nm and 22 nm nodes, respectively. Only the 2001 update of the ITRS conveyed a more near term, n+2, transition to a non-optical lithography technology, after the 65 nm node.

During this period, considerable attention was focused on the exposure tool and mask infrastructure. The cost of bringing each exposure tool technology to market is on the order of one billion dollars. The corresponding development of a robust mask fabrication infrastructure is within an order of magnitude of the exposure tool costs. Conversely, during this same period, relatively modest investments were made in imaging materials, such as photo resists.

Today, line edge roughness (LER) and line width roughness (LWR) increasingly challenge our ability to achieve uniform electrical properties in the deep nanometer transistor domain. Additionally, the discussion about the interdependence between LER and dopant nano-roughness and their impact on device properties is just beginning to happen.

This talk will consider the limitations of current families of resists and suggest evolutionary imaging material opportunities that may satisfy projected patterning materials requirements, including LER, long range dimensional control, resolution, and functionality. The materials science needed to develop new generations of robust imaging materials for future information processing technologies represents a relatively unexplored and untapped frontier. This research are exhibits the potential for keeping the demise of optical patterning n+3 generations away from current technology, for nodes to come.

6519-03, Session 2

Fluoro-alcohol materials with tailored interfacial properties for immersion lithography

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Immersion lithography has placed a number of additional performance criteria on already stressed resist materials. Much work over the past few years has shown that controlling the water-resist interface is critical to enabling high scan rates (i.e. throughput) while minimizing film pulling and PAG extractions (i.e. defectivity). Protective topcoat polymers were developed to control the aforementioned interfacial properties and emerged as key enablers 193 nm immersion lithography. Achieving the delicate balance between the low surface energies required for high water contact angles (generally achieved via the incorporation of fluorinated groups) and the base solubility required for topcoat removal is challenging. More recently, additional strategies using fluoropolymer materials to control the water-resist interface have been developed to afford topcoat-free resist systems. In our explorations of fluoroalcohol-based topcoat materials, we have discovered a number of structure-property relationships which can be taken advantage of to tailor the interfacial properties of these fluorinated materials. This talk will address the effect of structure on immersion specific properties such as water contact angle, aqueous base contact angle, and dissolution rate.

6519-04, Session 2

Development of non-topcoat resist polymers for 193-nm immersion lithography

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193-nm immersion lithography is considered as the most practical candidate for the next-generation lithography and actively developed toward mass production for 65nm node device and beyond because it is obtain larger depth of focus(DOF) and higher resolution at a hyper numeric aperture(NA) lens design than 1.0. In this technology, it fills between the lens of the exposure tool and resist film on the wafer with the water. To prevent leaching of resist components from the resist layer into water, the use of top-coat on resist film is most useful method. On the other hand, non-topcoat resist processes would be preferable solution for 193-nm immersion lithography into mass production. These simplified process go without separate coating and baking step for topcoat material and thereby reduce cost of ownership and fewer sources for defects.

Furthermore, in case when some topcoat is applied, the defect may increase than without topcoat because of presence of an intermixing layer between topcoat and resist[1].

The challenge of non-topcoat resist is both low leaching level and high resist performance. In this study, we have tried to develop non-topcoat resist polymers for immersion lithography.

Some practical issues still exist in 193nm lithography. For example, such as immersion specific defects are recognized as one of the major

issue. The typical defect is the circular “water mark” defects, which is immersion specific and critical. It is considered that water droplet left on the topcoat/resists film surface after scanning exposure induce “water mark” defects as one of mechanism for that. In recent studies, the water mark defects depend on the hydrophobicity of film surface (topcoat/resist) have been reported[1,2,3,4]. Therefore, in order to prevent watermark defect, the materials that have higher hydrophobicity have been required as topcoat /resists.

At first, we focus on finding out new structure lead to higher hydrophobicity and developed several new materials which have highly fluorinated cyclic structure. We have tried to synthesize new resist material by two approaches. The one is co-polymerization of new hydrophobic unit with some acrylate which compose conventional resist materials. The other is simply blend of additive including new hydrophobic unit into such as conventional resist resin. The method which control the hydrophobicity of film surface by additive have been published already[5,6]. In both approaches, we successfully obtained new resist polymer which showed higher hydrophobicity and good resist performance. Especially, in latter approach, we found that blending a small amount of additive having hydrophobic unit significantly improve the hydrophobicity of the resist surface without reducing of original resist performance. We considered that additive readily came up to top of the surface after baking because it include fluorine different from base resist polymer . (Fig.1)

In addition, it was considered that additive doesn’t affect the lithographic performance of base resist polymer as it dissolves in developer after exposure and behaves like resist polymer.

The hydrophobicity of film surface was evaluated in the contact angle of water droplet at the dynamic state, the sliding and receding angels. These parameter were considered to have good correlation to wafer stage scan speed capability and immersion defect reduction.

We can easily control hydrophobicity of resist surface, receding angle from 70 to 90 degree, by varying a quantum of hydrophobic unit (Fig.2). We have also performed evaluation of lithographic performance of resist blended our hydrophobic additive, whose receding angle is 95degree ,using Two Beam Interferometeric Exposure(Fig.3). Evaluation results of hydrophobicity, leaching and resist performance of these new materials will be presented.

6519-05, Session 2

Progress of topcoat less resist for immersion lithography

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193nm immersion lithography will be coming to establish at high volume manufacturing process in the near future, because it is able to achieve higher resolution and large DOF with hyper NA that means more than 1 numerical aperture(1-4). At initial phase, top coat process will be used to prevent defect and contamination. But most of chip makers prefer to avoid the use of top coat in view of “cost of ownership” due to concerns of additional cost on top coat. Therefore top coat less resist is required. But top coat less resist process has several issues to be solved for being productive. In this report, we will discuss about topcoat less resist criteria and our experiments and results to solve issues.

The first one is hydrophobicity of resist surface. Higher hydrophobicity of surface is needed to prevent water penetration and water droplets issues. In previous investigation, we successfully found effective additive to obtain higher hydrophobicity indicated as higher receding angle(5). In addition, Hydrophobicity can be controlled with loading ratio of additives. But we also found recently that too high hydrophobicity of surface may cause defects, such as re-precipitation type. In this report, we will discuss about the relation of hydrophobicity and defects, our material approach for defect reduction and defect evaluation results with using Nikon S609B (NA 1.07). In that time we will clarify defect types and focus on re-precipitaion type and immersion specific defect type.

Besides water uptakes of acid and amine from resist film, known as leaching, is also key factor of top coat less resist process for immersion lithography. Reduction of leaching amount is definitely needed for top coat less resist to be applicable to high volume manufacturing. Regarding to leaching, resist components and water penetration are key factors. We confirmed that hydrophobicity is also relative to reduction of leaching amount. We will discuss about our approach for less leaching amount.

Furthermore lithography performance required for 45nm node and below is quite high. We will present the evaluation results that will be exposed by Nikon S609B (NA 1.07).

6519-06, Session 2

Building an immersion topcoat from the ground up: materials perspective

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Over a period of last several years 193 nm Immersion lithography from a remote and unlikely possibility gradually became a reality in many fabrication facilities across the globe and solid candidate for high volume manufacturing for the next generation technology node. It is being widely understood in the industry that top-coatless resist approach is a desirable final stage of the immersion process development. However creating low-defect high performance top-coatless resist materials requires deep understanding of the fundamental material properties of the top layer, responsible for leaching suppression and immersion fluid meniscus stability, thus enabling high speed low-defect scanning.

While a lot of progress has been made in implementing specific top coat materials into the process flow, clear understanding effects of the top coat properties on the lithographic conditions and printing capability is still lacking. This paper will discuss top coat materials design, properties and functional characteristics in application to both commercially available top coat materials and novel fluoroalcohol polymer-based immersion top coat.

We have used our fluoroalcohol based-series formulations as a test vehicle for establishing correlations between top coat performance and its physical and chemical properties including hydrophobicity, molecular weight/dispersity etc. Effects of polymer-solvent interactions on the contact angle and performance of the top coat material are also explored, providing valuable understanding transferable to design of new generation top coats and top-coatless materials. Our resultant new formulations demonstrated excellent lithographic performance, profiles and low leaching levels with metal level resist and high receding contact angles, comparable to the commercial top coat materials.

Continuing discussion to commercially-available top coats - we will highlight specifics of using current commercial top coat materials from JSR Micro - including lithographic performance and defectivity testing, and describe current status of top coat implementation at IBM 300 mm. Areas of improvement of the top coat properties and performance required for new generation immersion tooling are identified, outlining pathway for future work in realm of water-based immersion. Reliable performance of various TCX-series top coat materials across range of resist polymer platforms and process conditions is demonstrated, confirming its critical role in enabling immersion lithography for high volume manufacturing for 45 nm technology node.

6519-07, Session 2

Novel materials design for immersion lithography

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The technology of 193nm immersion lithography progresses rapidly toward half-pitch 45nm generation device manufacturing. In immersion lithography there are several intrinsic issues to be overcome. The biggest challenge in materials development is how to avoid the watermark defects and photo-acid generator (PAG) leaching with the satisfactory lithographic performance. The most of approaches is an introduction of cover coating materials (top coat) onto the resist film. Recently we have established the non-top coat resist system improved by the utilizing of the novel two kinds of materials, that is surface modified polymer and less-leaching PAG. Surface-modified polymer

behaves as the builded-top coat which delocalizes at resist surface and changes drastically the surface hydrophobicity to diminish completely the watermark defects. Less-leaching PAG can respond to thermal stimulus, which decomposes by heating and changes the acid diffusion to reduce the line-edge roughness (LWR). Herein we would like to discuss the concept of novel PAG and surface-modified polymers.

6519-08, Session 3

Novel high-index resists for 193-nm immersion lithography and beyond

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The extension of optical lithography beyond the 32 nm-node will involve technologies beyond standard aqueous 193 nm lithography. As second and third-generation immersion fluids are introduced, renewed focus will be placed on the properties of the resist, including the refractive index. Modelling work reported in previous meetings has shown that substantial gains in depth of focus and exposure latitude will result from use of resists having RI values approaching 2.0.[1] In addition the use of fluids not based on water will permit increased flexibility in terms of resist chemistry. In this presentation we will present a broad approach to the synthesis of high-RI polymeric resists, with the aim to achieve sufficient flexibility to meet all envisaged needs of 193i and 193i+ lithographies.

Our design approach has relied on development of QSPR (Quantitative Structure-Property Relations) models of the refractive index of candidate structures to be incorporated into the resist polymers. We present here a comprehensive QSPR model for calculation of RI at 193 nm, and will comment on the limitations of such a model for materials which have strong absorption bands in this spectral region. In addition we calculate the absorption spectra of candidate structures, both to limit absorption at the critical wavelength, but also to identify structures which absorb around 180 nm and which may therefore display so-called anomalous dispersion. It is well known that at the leading edge of strong absorption bands the refractive index increases markedly. In several instances we have attempted to exploit this gain in RI without sacrificing the low absorbance of the polymer.

Two principal synthetic pathways were explored, namely methacrylate chemistry with functional side chains, and Michael addition polymerization. Other synthetic options are being explored and will be discussed. A range of methacrylate monomers with sulfur-containing leaving groups were prepared and the properties of their homopolymers and copolymers with other methacrylates examined in detail. It was found that RI of up to 1.86 could be achieved with this route; the ultimate refractive index is limited by the level of sulfur that could be incorporates into the functional side chains. Therefore sulfur has been incorporated into the polymeric main chain through the Michael addition reaction, and sulfur contents of up to 33 wt. % being achieved. Examples of images obtained using resists formulated using several of these polymers will be presented.

Alternatives methacrylate structures designed to absorb around 180 nm are also described; in particular this part of the program emphasises the importance of calculation of optical properties prior to embarking on a synthetic property. We have prepared monomers and respective homo- and co-polymers with side chains containing thiophene or thiazoline units. Finally in a parallel program we are preparing materials based on modified polyphosphazenes as candidate resist polymers.

The broad approach described here has been designed to respond to the needs not only of 193 aqueous immersion but also to the requirements of 193i+ lithography. It is therefore expected that the resists chemistry is sufficiently flexible to be applicable to the still-undefined requirements of fluids beyond water. We therefore discuss in this presentation the design criteria used to develop such flexible materials.

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6519-09, Session 3

Experimental observations of high-index liquid interaction with resist

S. V. Postnikov, Infineon Technologies AG (Germany); M. Ercken, P. Foubert, R. Gronheid, E. Hendrickx, C. Jehoul, B. Kim, F. Van Roey, J. Versluijs, N. Vandenbroeck, P. Willems, IMEC (Belgium)

Immersion liquids with refractive index equal or greater than 1.65 will be essential to print the 32nm node in a single patterning approach. The new immersion liquid will have to meet different requirements from resist process perspective. For this purpose, IMEC is evaluating a methodology for testing interaction of the high index liquids (HIL) with the resist films.

The methodology is based on several experiments. Dry exposure on an ASML PAS5500/1100 scanner is carried out in combination with a pre- and post-exposure soak with the liquid. These wafers are analyzed using scatterometry. The impact of the liquid on the profile performance of the resist (CD, sidewall angle and profile height) gives an indication of the resist-liquid interaction. A procedure is also developed for measurements of dynamic leaching of the resist components into HIL by mass spectrometry. As a first test towards defectivity in high index liquids, HIL droplets will be dispensed in a controlled way onto the resist surface. The residues of the dried HIL droplet will be analyzed with respect to their morphology by KLA-TENCOR HRP220 profilometry. Another important parameter for liquid containment and defectivity is the contact angle. HIL contact angle measurements are performed via three different approaches: static droplet on stationary surface, droplet on a tilting surface, see Figure1, and captive droplet. Finally, the ASML immersion interference printer (IIP) is used to study the HIL impact on lithographic performance based on exposure latitude values and resist profile. The majority of the IIP imaging will focus on the 72nm pitch in order to make a direct comparison of imaging performance between HIL and water. The ultimate performance will be checked at 64nm pitch, which is possible with HIL only, see Figure 2.

This presentation will summarize test results for the second generation (n=1.65) high index liquids.

6519-10, Session 3

High-refractive index materials design for ArF immersion lithography

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ArF immersion lithography has been accepted as the most promising candidate for 45 nm node (hp65 nm). Instead of water as 1st Generation Fluid, the higher refractive index fluid is expected to provide a potential extension of ArF lithography to hp38 nm or below. So far, a number of novel ArF immersion high-refractive-index fluids (HIFs) as 2nd Generation Fluid have been reported. The optical properties for some of the organic HIF candidates, such as refractive indices (\>1.6) and transparency (\>98%/mm), are very promising. Successful imaging of hp32 nm L/S and hp30 nm L/S has also been demonstrated by two-beam interferometric exposure tools. However, despite of the remarkable advances in recent HIF researches, there are still a lot of issues for realizing ArF HIF immersion lithography, since the recycling system of HIF have not been developed yet. Besides, to manufacture hp32 nm device, the higher refractive index materials (n \> 1.75) such as the final lens element, immersion fluid and resist are needed.

In this paper, we will address such problems by reporting our updated results on research of JSR HILs, which are the current candidates of immersion fluids for the next generation ArF immersion lithography. We will focus on the following issues. In addition, top-coat material design for JSR HILs will be described. The higher contact angle of HIL on a top-coat is required to get a higher scan speed. In general, the contact angle and the refractive index are trade-off relationship in current top-coat materials. We will also explain our novel top-coat material design concept.

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6519-11, Session 3

Adapting immersion exposure to mass production by adopting a cluster of novel resist-coating/developing and immersion-exposure equipment

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The scaling down of pattern dimensions in lithography continues as the level of integration in semiconductor devices rises. Against this background, 193-nm immersion lithography technology is capable of even finer dimensions without changing the infrastructure technology of state-of-the-art 193-nm dry lithography. It is consequently showing much promise as a technology for next-generation mass production and is entering a stage of full-scale development toward this end.

At the same time, the fact that 193-nm immersion lithography fills the space between the projection system and silicon wafer with a fluid raises several concerns. In particular, the immersion of resist film in de-ionized water during exposure can lead to the penetration of moisture into the film and the leaching of resist components into the water, as well as the formation of residual moisture affecting post-processing. Here, the use of a protective film is considered to be helpful in preventing effects caused by the direct immersion of resist in de-ionized water, but even this measure has not been able to completely solve the above problems.

To overcome this dilemma and achieve true mass production by immersion lithography, it is essential that exposure equipment, materials, and coating/developing equipment each be optimized once the characteristic behavior of 193-nm immersion lithography technology has been ascertained.

For this reason, we previously investigated the effect of immersion exposure on the lithography process, examined the coating performance of protective film and development-process behavior, and performed a comparison with dry lithography. In doing so, we isolated the problems that had to be solved in 193-nm immersion lithography technology with an eye to mass production.

Specifically, we determined the generation mechanisms of wafer marks and air bubbles that become trapped during immersion exposure, which are characteristic problems of immersion lithography, and uncovered the factors behind development defects. We then found means of solving these problems through the appropriate application of coating/developing technologies and exposure-processing technologies based on new concepts. We also showed that immersion lithography based on these technologies could achieve the same level of performance as the existing dry exposure process, and that it could be applied to mass production by satisfying the need for critical-dimension control both on the wafer surface and during continuous wafer processing.

This paper reports the results obtained by the above studies on 193-nm immersion lithography technology and describes the effectiveness of novel coating/developing technologies and exposure-processing technologies in solving the problems characteristic of immersion lithography.

6519-12, Session 3

Immersion defectivity control by optimizing immersion materials and processes

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Because ArF immersion lithography can print IC features down to 45nm node or below, the required resist resolution must also be reduced than conventional dry resist. Intensive resist development to meet this requirement is now underway by resist vendors. Even if the pattern size was shrunk, the defectivity performance must be kept as the same level or even better than conventional dry resists. There are a lot of challenges. Resists capable of both good lithographic and defectivity performance is strongly needed. To fined out such ideal resist, screening test was done by a dedicated immersion cluster comprised of a volume production immersion exposure tool named S609B having NA of 1.07, resist coater-developer LITHIUS i+ (TEL). Defectivity is evaluated down to 55 nm half pitch which is the target size of S609B. Contact hole resists are also evaluated.

Topcoat process is a main stream for the initial stage of immersion process. Because the topcoat is the interface to water, topcoat character governs immersion defectivity. However, it is also affects resist lithographic performance. Intermixing in between them may cause such change. Both defectivity and lithographic performance are evaluated at various resist and topcoat combinations.

Topcoat-less resist process is attractive candidate for second stage of immersion lithography. Because topcoat-less process is simpler, it has a room to be able to reduce process related defects including particle, pinhole, blister and non-uniformity of topcoat. On the other hand, topcoat-less resist require not only good lithographic performance, but also high hydrophobicity and low leaching level, because the resist itself contacts with water. Topcoat-less resist having various hydrophobicity and leaching level is evaluated both lithographic performance and defectivity.

Immersion materials including topcoat, resist and BARC can be a potential source of tool contamination. Edge peeling and resultant particle generation is a great concern on immersion resist process. Bad materials or not well optimized process conditions must be screened out before immersion exposure to prevent tool contamination. We have developed off-line scan test bench equipped immersion nozzle and simple scanning stage. Particles in recovered water are measurable by particle counter. Using this test bench, particle level at various materials at various process conditions, especially edge treatment condition can be measured, so that bad materials or problematic process conditions can be figured out before the actual usage. Correlation between offline measurement and actual defectivity performance is analyzed.

If the particle level is increased in the immersion exposure tool, it is very important to know the source of particle contamination. By our research, FT-IR and TOF-SIMS are very effective analysis method to determine the particle's material or composition.

By these immersion material and process research we could successfully reduced defect level in immersion lithography.

6519-13, Session 3

Measurement and evaluation of water uptake by resists, topcoats and stacks, and correlation with watermark defects

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With immersion lithography approaching the insertion in production, watermarks remain as one of the main concerns for immersion specific defects. They require special attention because of their size and associated high kill-ratio, and their increasing occurrence at higher scan speeds. IMEC has been working to understand the underlying mechanism of why remaining water droplets cause these defects. One material parameter that appears to correlate with the tendency to form watermark defects is water uptake(1). Moreover, the effectiveness of a rinse as a mitigation strategy against watermarks is directly correlating to the water uptake (2).

In this work, Ellipsometric Porosimetry (EP) is used to measure the water uptake tendencies of materials and stacks, and investigate what parameters are affecting it. In EP, a controlled water vapor is used to induce condensation of water inside the material. This process is monitored using Spectroscopic Ellipsometry (SE) which gives information on the change in refractive index and the thickness of the layer. A methodology is developed to quantify the total water uptake by a single layer and a layer in a stack. The influence of process parameters, presence of a top coat, PAG and quencher loading, illumination, etc. on water uptake by the resist is evaluated.

The results of this investigation can be used to guide material development and to optimize processing with respect to watermark sensitivity. This way, the watermark defectivity problem could possibly be controlled even if water is left on the wafer surface.

(1) M. Kocsis, to be presented at the Immersion Symposium (Kyoto), october 2006

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6519-14, Session 4

High-performance 193-nm photoresists based on fluorosulfonamide

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The combination of high numerical aperture (NA) imaging and reticle enhancement techniques (RETs) has extended 193nm lithography into the 45nm node and possibly beyond. In order to fulfill the tight pitch and small critical dimension requirements of these future technology nodes, the performance of 193nm resist materials has to further improve. In this paper, a high performance 193nm photoresist system based on fluorosulfonamide is designed and developed. The fluorosulfonamide group has good transparency at 193nm. Compared to the commonly used hexafluoroalcohol (HFA) group, the trifluoromethyl sulfonamide functionality has a lower pKa value and contains less fluorine atoms. As a result of these differences, polymers containing the trifluoromethyl sulfonamide functionality have shown improved dissolution properties and better etch resistance than their HFA counterparts. Resists based on the fluorosulfonamide-containing polymers have demonstrated superior litho performance for both line and trench levels under the 45nm node exposure conditions. It is also found that the incorporation of the acidic fluorosulfonamide into the polymer structure could substantially reduce the PEB sensitivity of high activation energy protecting group (e.g., methyladamentyl group) based methacrylate resists. The structure, property and litho performance of the fluorosulfonamide resist system are reported.

6519-15, Session 4

Novel diamantane polymer platform for enhanced etch resistance

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Diamantanes are the next higher homologs of adamantane in the lower diamondoid family. The lower diamondoids have recently become available at economically feasible prices because they were found to be present in certain oil feed stocks in substantial quantities. Due to their low Ohnishi number and ISP, such molecules are expected to enhance dry etch stability when incorporated into polymers for resist applications. Starting from the diamantane parent, diamantane homologs of the adamantane monomers used in 193nm resists can generally be made by similar chemical steps as used for adamantane derivatization. We have successfully made the following monomers (see structures below) and have synthesized a number of copolymers with various lactone monomers. This paper will present the polymerization results, the unexpected solubility properties of the resulting polymers in resist solvents, the lithographic performance of select polymers, and the etch resistance improvement of the diamantane-containing polymers.

6519-16, Session 4

Hybrid optical: electron-beam resists

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Future lithography will most likely encompass not just a single technology, but combinations of several approaches being developed today. Versions of optical, EUV, and e-beam lithography will be implemented in different organizations, sometimes side-by-side. The specifics of such a mix-and-match approach will be determined by a variety of considerations: the geometries to be printed, the number of wafers per mask level (for optical and EUV), process latitude, throughput, yield, and so on. This more eclectic approach to lithography would greatly benefit from mix-and-match patterning with optics and electrons. However, combining optical and e-beam exposures on the same wafer-level would require the use of high-performance hybrid resists, which perform equally well with leading edge optical lithography and with e-beam exposure. Chemically amplified resists are, of course, widely used at 193 and 248 nm, and some chemically amplified resists have been employed with e-beams as well. However, hybrid lithography would require a common window of chemical composition, formulation, and processing of resists used in the two exposure modalities.

We report here on experimental results aimed at optimizing the processing conditions in 193-nm exposure and with 50-kV electron beams, with the aim of obtaining simultaneous high-resolution performance at both. The resist was a dilution of the Rohm and Haas EPICTM 2340 193-nm chemically amplified photoresist. Several processing conditions were varied, including post apply bake and post exposure bake, the use of an antireflection layer designed for 193-nm use, and resist thickness. The 193-nm exposures were performed with an interference system, and the e-beam exposures were carried out with a scanning Gaussian beam (5 nm probe size) operating at 50 kV. Dense patterns of lines and spaces were obtained with the e-beam down to 45-nm half pitch (Figure 1). For reference, non-chemically amplified resists were also exposed with the e-beam. The highest resolution of dense patterns in 55-nm-thick PMMA was 25 nm. We note that the absolute value of the resolution depends also on parameters, such as the aerial image contrast, which are not related to the resist. However, the difference in resolution between the two resists under similar exposure conditions may be indicative of the role of acid diffusion.

In this paper we will present results of separate exposures with 193 nm and with e-beams on different wafers, as well as patterning with the two systems on the same resist-coated wafers. Although these are preliminary results, they clearly indicate that high-resolution hybrid optical/e-beam resists are feasible using commercially available resist platforms.

6519-19, Session 4

Photo-deprotection resist based on photodegradation of o-nitrobenzyl phenol ether for near-field lithography

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We have used an i-line sensitive chemically amplified resist (CAR) specially prepared for near-field lithography (NFL) that utilizes the i-line light of a mercury lamp. In terms of line edge roughness, i-line CAR patterns showed superior performance to those of commercially available novolak type i-line resists. However, its LER was still as large as 13 nm (3 sigma) on the pattern, which is not sufficient for the specification required for half-pitch (hp) 22 nm node.

It is widely known that the acid diffusion during post-exposure bake (PEB) in CARs is one of the causes for the poor LER and limits the lithographic resolution to hp 20~30 nm. In order to obtain finer resist patterns than that of CARs, we invented positive-tone resist system based on photodegradation of o-nitrobenzyl (NB) phenol ether, which was named PDR-NB. The PDR-NB consists of single component; polyphenol compound partially protected by NB. The photo-deprotection reaction of NB ether and ester is known in the field of biochemistry and has been applied to the caged compounds, the drug delivery system and so on. The reaction is completed during the exposure process and needs no PEB. Hence, PDR-NB never encounters the problem originated from the acid diffusion that happens in CARs.

Polyhydroxystyrene, whose 38% of hydroxy groups were protected by NB (NBP-38), was synthesized by the coupling reaction of polyhydroxystyrene (Mw = 4,100, Mw/Mn = 1.1) with 4,5-dimethoxy-2-nitrobenzyl bromide in the presence of an equal amount of sodium hydride. For the sensitivity to the i-line light, dimethoxy substituted NB compound was used. The resist solution was formulated by dissolving NBP-38 into propylene glycol monomethyl ether acetate (PGMEA).

The absorption spectrum of NBP-38 film was measured using a spectroscopic ellipsometer. NBP-38 film had a reasonable amount of absorbance below 438 nm and its lambda-max was at 350 nm, hence

was confirmed to be applicable to our i-line NFL.

We carried out NFL exposure experiments with the tri-layer resist process using both NBP-38 and i-line CAR as top-layer resists of 20 nm thick. Although NBP-38 needed larger exposure dose (~5 times) than that required for i-line CAR, the hp 45 nm NBP-38 pattern was resolved clearly. In contrast, that of CAR did not at all though the same near-field photomask was used.

The 20 nm thick NBP-38 pattern discussed above was successfully transferred into the 100 nm thick bottom-layer resist by the two RIE process steps. These results demonstrated that our PDR-NB exhibits low LER and enables us to obtain high-resolution features.

6519-73, Session 4

Evaluation of immersion lithography process for 55-nm node logic device

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Immersion lithography has the superior advantages that show larger process window compared it with the same exposure condition by the conventional dry exposure system. Therefore development as most importance means of the micro pattern fabrication below 65nm-node devices, which require high NA exposure, is strongly promoted and is already entering a mass production application stage.

We have been developing of ArF immersion lithography process (1). Further progress to apply for mass production, it is necessary to achieve high scan speed exposure for high throughput, and avoids the degradation of lithographic performance which possibly caused by leaching (PAG etc.) from a resist contaminations. Therefore we chose a process with using a topcoat process. A cost becomes high in use of a topcoat, but the reason is because it was difficult to be consistent lithographic performance and leaching by using the topcoat-free resists which we obtained at present.

About a mass production, one of the problems left unfinished is reduction of a pattern defect of immersion induced defects.

We evaluated several resists and top coat materials and combination of both materials. As a result, we clarified a combination with ArF resist for dry exposure and optimized developer-soluble topcoat material could decrease immersion induced defects with high scan speed exposure. Furthermore, we could minimize a defect of immersion induced defects using special immersion-optimized processing.

In this paper, we report that immersion defect reduced lithography process for 55nm-node logic devices with high quality resist patterns. Details and further discussion results will be presented at the conference.

(1)T. Kodama, T. Nakata, M. Fujimoto, M. Yamana, 3rd International Symposium on Immersion Lithography, [PO-10], 2006

6519-20, Session 5

Enhancing photoresist performance with an adhesion promoting photo-acid generator

R. P. Meagley, S. Sharma, Lawrence Berkeley National Lab.

Concentration gradients of photoacid generator through the thickness of the photoresist film can profoundly affect the material's performance. [1] To engineer the acid concentration through resist thickness, we have developed a new type of resist adhesion promoting layer that incorporates photo acid generator chemistry. These adhesion promoting photo acid generators, called as a class "APPAG", enhance acid concentration at interface between the resist and the substrate. We will provide an overview on the preparation and characterization of two siloxane based APPAG materials along with a performance comparison of commercial DUV, EUV and E-beam photoresists on APPAG.

Nonaflate analog (APPAG 6) with shorter acid diffusion length was found to have a mild impact on 250nm node DUV lithography. However the triflate analog (APPAG 9), owing to the larger acid diffusion length, was shown to provide a greater influence. APPAG 9 was found to give nearly a 50% improvement in depth of focus (Figure 1). [2]

For EUV lithography, APPAG 6 will be shown to substantially improve performance envelope for 100nm dense lines and spaces and at reduced post exposure bake (PEB) temperatures. This indicates that this approach can be used to gain margin at reduced PEB which is desirable to minimize thermally driven diffusion effects. When used in conjunction with e-beam lithography, a similar effect is also seen where only half of the exposure dose was required to print equivalent features. Thus the materials represent an important new approach to extending photoresist performance margins.

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6519-21, Session 5

Second-generation radiation sensitive developable bottom antireflective coatings (DBARC) and implant resists approaches for 193-nm lithography

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We will discuss our approach towards a second generation radiation sensitive developable barc (DBARCs) (Scheme 1) for 193 nm. We will show imaging results (1:1 L/S features down to 150 nm) for some first generation implant resist material based upon a fluorinated resins and also show relative implant resistance of these first generation fluorinated resists towards As implantation (15 KeV at 5x1015 dose with 20 x 10-4 amp). Also, discussed will be a second generation of Implant resists based on a non-fluorinated resins. Surprisingly, we found that the non-fluorinated materials gave better implant resistance (~2-3 X1011 atoms/cm2) despite the higher atomic number of fluorine compared to hydrogen in the fluorinated implant materials (~2-5X1012 atoms/cm2). Table 1 details the relative arsenic stopping power of different resists having a film thickness of 1700A . Resist A and B in this table are fluorinated implant resist materials. Finally, we will give an update on the lithographic performance of this second generation of implant resists.

6519-22, Session 5

Spin-on trilayer approaches to high-NA 193-nm lithography

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New challenges face ArF bottom antireflection coatings (BARCs) with the implementation of high NA lithography and the concurrent increased use of spin-on hard masks. To achieve superior reflectivity control with high NA there must be at least 2 semi-transparent ARC layers beneath the resist to effectively suppress reflectivity through a full range of incident angles. To achieve successful pattern transfer, these 2 layers, in conjunction with the organic resist, can adopt an alternating elemental composition in order to amplify vertical resolution. This will circumvent the inherent low etch resistance of ArF resist and the decreasing film thicknesses which accompany increasing NA. Thus, incorporating hard mask properties and antireflection properties in the same two layer system facilitate the pattern transfer process as a whole rather than just enhancing lithography. As with any material expected to exhibit multiple roles there is a delicate balance between optimizing the chemistry for any one particular property since it may conflict with its other roles. We will discuss some of these conflicts and present materials we devised which balance these conflicts. We will also present simulations aimed at finding the best film thicknesses and optical indices for a trilayer stack determined simultaneously for high NA and how the simulation algorithms were devised. We will present the etch rate data, lithography and out-gassing property of silicon and high

carbon content BARC materials designed to met the demands of high NA lithography.

6519-24, Session 5

Silicon-based antireflective spin-on hardmask materials with improved storage stability for 193-nm lithography

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As the feature sizes of integrated circuits shrink, thinner photoresist coating should be used in order to avoid high aspect ratio which can cause pattern collapse. Especially for 193 nm lithography, photoresist coating is too thin to work as a mask for subsequent etching step. One of the solutions to this problem is using hardmasks which have good etch selectivity to adjacent layers. In this paper, silicon-based anti-reflective spin-on hardmasks are described. One of the major problems of silicon based polymers in the hardmask compositions is poor storage stability because silanol group is reactive enough to condense each other, which can instigate molecular weight increase to yield gel-type particles. Our hardmask materials have improved storage stability because active silanol groups are partially protected. Also this protected silanol groups can take part in crosslinking reaction during bake process without additional deprotection step. Although this strategy could encounter intermixing problems with other layers, we can produce silicon-based hardmasks without any deleterious effects. These hardmasks show anti-reflective properties and great etch selectivity to both photoresists and organic hardmasks. Characterization, storage stability and lithographic performance of this material are described in detail.

6519-25, Session 5

Novel developers for the positive tone EUV photoresists

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While much work has been done in the design of photoresist for EUV lithography, these materials have typically been optimized for so called “standard developer” i.e., 2.38% tetra methyl ammonium hydroxide. However we felt that it would be reasonable to consider specifically the developer as opposed to the resist design. Indeed it has been suggested that the polarity and cation size in developer are important positive tone resist performance. [1]

We therefore examined the effects of several aqueous systems on EUV lithography of two reference resists incorporating either containing tetra methyl ammonium hydroxide or a larger more hydrophobic ionic base. This was done in order to perturb the wetting, ionization, gellation and emulsification kinetics of the system. It is our hypothesis that a base that could wet and penetrate faster into partially deprotected resist could result in a faster photospeed, and thus make more margin available for resist design; for example a slower system incorporating higher quencher loadings could be accommodated.

Additionally, we sought to probe the effects of solvent polarity with varying amounts of non-aqueous solvent additive. [2] By reorganization of the nascent solvent shell with the nonaqueous additives, we sought to perturb the development kinetics and thus change the resist’s performance envelope by accelerating photospeed and potentially increasing contrast. This approach has been applied to non chemically amplified resist to good effect. [3, 4]

In both of the two positive EUV photoresists evaluated with the prototype developers we found that the performance was profoundly impacted by these two probes (i.e. solvent polarity and cation hydrophobicity). Also, both of the resists were found to perform quite differently across the screen of prototype developers, each showing a different pattern of sensitivity relative to standard developer. Both resists were able to be accelerated in photospeed, and impact to photospeed and other performance parameters will be discussed.

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6519-122, Session 5

Material design of Si-contained hard mask and carbon bottom layer for multilayer stack application

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Immersion lithography is the most promising candidate toward 45nm hp process, and also the first generation of immersion lithography, which is more than 1.0 NA and less than 1.3 NA is about to be applied for the high volume manufacturing. In parallel with immersion lithography introduction, multi layer stack application is being tried to apply for the manufacturing process since reflection control from the substrate would be an issue with current single layer stack. Multi-layer stack application is composed more than 3 layers for the lithography process, one is carbon bottom layer on the substrate, second is Si contained hard mask and third is resist. Multi-layer stack application can control reflection from the substrate with hyper NA(more than 1.0 numerical aperture) , also it can help etching resistance on thin film resist application. Therefore, multi-layer stack is necessary for the next advanced technology node with hyper NA immersion. Our material criteria of multi-stack are spin-on and drain compatible type with resist and BARC because of the easiness of implementation. The Si contained material for hard mask would be the most important role to establish multi-layer process.

Spin-on Si contained hard mask is mainly required characteristics that are reflection control from substrate at hyper NA, good resist matching and etching resistance that needs high Si content. Generally speaking, there is a serious trade off between Si content and resist matching. For example, high Si content of the hard mask would show bad resist matching, footing or under cut resist profile. On the other hand, low Si content of the hard mask would show good resist matching, but it might not have an enough etching resistance. (Fig.-1)

In this report, we will discuss our concept and approach for good resist matching (no footing or under cutting issue) without reduction of Si content of the hard mask. We will introduce a universal hard mask stack with more than 30wt% Si content ratio. Pattern transfer ability focus on LWR change during etching process will be discussed as well. We estimate that the composition of base polymer and film density in carbon bottom layer is relative to LWR after dry etching. We will introduce a carbon bottom layer without LWR change during etching steps.

6519-26, Session 6

The application of high-refractive index photoresist for 32-nm device level imaging

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The lithography prognosticator of the early 1980’s declared the end of optics for sub-0.5um imaging. However, significant improvements in optics, photoresist and mask technology continued through the mercury lamp lines (436, 405 & 365nm) and into laser bands of 248nm and to 193nm. As each wavelength matured, innovative optical solutions and further improvements in photoresist technology have demonstrated that extending imaging resolution is possible thus further reducing k1. Several authors have recently discussed manufacturing imaging solutions for sub-0.3k1 and the integration challenges.

The Semiconductor industry continues to mature. The imaging solution will be the most cost effective. Lithography and more importantly “imaging solutions” are driven by economics. The technology might be extremely innovative and “fun”, however, if it’s too expensive it may never see the light of scanner. The industry continues to focus on process tricks and creative science to solve problems in the most cost effective manner. There are many examples of this such as new rinses to reduce pattern collapse1, surface conditioning for LER reduction2,

new materials to assist in shrinking contact holes3 and surface treatment of ArF photoresist materials to reduce or minimize slimming4.

Recently exposure tool manufacturers have announced development of NA's \>1 for delivery in the 2006 timeframe for ArF systems. These developments will enable 65nm 1⁄2 pitch and most likely 45nm 1⁄2 pitch imaging with water immersion ArF. There has been speculation that NA's of greater than 1.3 are possible which could also enable the 32nm node.

This paper will focus on the process capability and requirement for ultra-high NA's that are near the limitation of the immersion fluid. Data will be presented demonstrating the impact of higher refractive index systems on the further extension of ArF Immersion. Device level specific test structures have been used for the four main critical levels along with advanced RET's to further explore improvements in critical imaging levels along with dominant mask effects.

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6519-27, Session 6

Performance of chemically amplified resists at half-pitch of 45 nm and below

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Chemically-amplified (CA) photo-resist has the advantage of high photo-sensitivity. The fact that one photon creates hundreds to thousands developer-soluble units makes this kind of resist extremely attractive to the lithography process. CA resist was introduced to litho production processes starting from 248nm wavelength and has been widely used since then. It is still the preferred choice for hyper-NA 193nm immersion and EUV lithography.

CA resist has an intrinsic weakness due to acid diffusion. In order to activate the de-protection process, the resist needs to be baked at elevated temperature after exposure (PEB). The high temperature enhances the acid diffusion and blurs the aerial image contrast. Theoretical analysis predicted that the acid diffusion eventually will prevent further resolution improvement. The key litho performance parameters of the CA resist - line-edge roughness (LER), photo-speed, and resolution of the CA resist - are inter-dependent; one can not be improved without sacrificing the performance of the others.

Patterns with half-pitch of 45nm and below can currently be successfully printed with the CA resists either by a hyper-NA (NA=1.3) 193nm immersion tool or a EUV MET tool. This paper will present the most recent litho performance results of CA resists exposed with the 1.3NA 193nm immersion tool and 0.3NA EUV MET tool, focusing on the resolution limit, LER, and photo-speed. We will give a comparison on the state-of-the-art CA resist performance at the edge of resolution of immersion and EUV lithography. It consists of the following parts:

1. CA resist performance at 45nm half-pitch and below with the hyper-NA (NA=1.3) 193i exposure;

2. CA resist performance at 45nm half-pitch and below with the EUV exposure;

3. Power spectrum analysis of the LER and intrinsic contribution from the CA resists;

4. Interaction of photo-speed, LER and resolution; and possible ways towards high resolution.

Although the 193i and EUV exposures have totally different optics, an overlap of the resolution capability is clearly observed around 45nm half-pitches with the CA resists. The ITRS insertion point of EUV is the 32nm half-pitch node, comparing the different CA resists at a common node provides insight into the resolution limitations of the different approaches. We intend to show how the chemically-amplified resist contributes to these two lithographic approaches around the half-pitch node of 45nm and below.

6519-28, Session 6

Evaluation of ArF lithography for 45-nm logic-node implant layers

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Scaling of designs to the 45nm node presents challenges for KrF lithography. While KrF is sufficient for a majority of the non-critical front-end-of-line (FEOL) levels, the requirements for the most demanding implant layers may drive either DUV with resolution enhancement techniques or ArF solutions. We describe the challenges of ArF lithography for implant layers, and demonstrate possible technical approaches derived during process evaluation.

Conventional reflectivity control techniques include using dry bottom anti-reflection coatings (BARCs) or top anti-reflection coatings (TARCs). The use of BARC as in conventional ArF processes is not feasible in the case of implant levels for technical reasons, and likely has an economic aspect as well. The BARC-open etch can result in a change in feature dimensions, resist thickness loss, and other undesired outcomes.

Alternative ways of controlling reflectivity-related effects such as standing waves and CD-swing must therefore be employed.

ArF resists for use with TARC are typically formulated with dye in order to suppress standing waves caused by light reflection from the substrate. Application of TARC additionally minimizes reflectivity at the resist surface. Optimizing the resist profile is challenging due to the many parameters involved: resist thickness and dye loading, TARC properties, and the optical properties of the substrate. Index-matched TARC was compared to a TARC that was not specifically optimized for ArF lithography, and may provide some performance benefits. Developer-soluble BARCs (dBARCs) offer the advantages of dry BARC with respect to reflection control, but allow dissolution in aqueous base developer. This eliminates the need and complications of BARC-open etch steps. New dBARC materials are photosensitive to facilitate dissolution of the exposed regions in order to provide superior profile control. For these early ArF resist/ dBARC combinations, there appears to be a dependence of performance on resist/dBARC matching. For the best combination of materials the lithographic performance turns out to be comparable to or better than the aforementioned approach.

The adhesion performance of ArF resists on the various substrates encountered in these FEOL levels is different from that of KrF resists. Some resists adhered weakly to various substrates, and a substrate-specific dependence was observed. To date, no substrate dependencies have been found when using a dBARC system.

Example ArF and KrF resists were processed with the same implant conditions to assess the stability during the implant- process.

6519-29, Session 6

Characterization of photo-acid redeposition in 193-nm photoresists

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Several investigators have demonstrated the importance of photoacid evaporation and redeposition during post-exposure bake (PEB) of chemically amplified photoresists. Cheng et al.1 characterized dissolution rate nonuniformities and showed that experimental results can be reconciled with resist process models incorporating photoacid evaporation. Shiobara et al.2 examined resist profile dependences on pattern density and showed that resist top profiles are consistent with evaporation as well as 're-sticking' of photoacid. Ma and Cerrina3 demonstrated that experimentally observed photoacid depletion effects can be simulated using electron-beam dose deposition and dissolution percolation models, and that photoacid depletion influences both resist profile and line-edge roughness.

Recently, Brunner et al.4 proposed that photoacid evaporation and redeposition during PEB may be a root cause of a long-range proximity

effect that mimics optical flare behavior. This 'chemical flare' process results in anomalous profile changes and linewidth variations over millimeter length scales, and is particularly undesirable in regards to development of optical proximity correction methods.

In order to further clarify the process underlying chemical flare, we have conducted TOF-SIMS surface profiling of a selection of commercial photoresists. To characterize surface composition changes by TOF-SIMS, resists were processed to the PEB step, then treated with a non-invasive staining method in order to detect photoacid concentrations at the resist surface. A photoresist that displays lithographically relevant chemical flare effects shows long-range (hundreds of microns) photoacid migration from exposed features. (See Figure 1.) Additionally, the surface of the photoresist shows blocking group depletion in unexposed regions that is directly correlated with redeposited photoacid: as one would expect, chemical amplification occurs wherever photoacid is present, regardless of its spatial origin. Photoresists that do not display chemical flare effects either do not show these long-range surface compositional changes, or show them only to a very small degree.

We will present these findings in detail, as well as additional characterization of the chemical and transport processes occurring during chemical flare, and preliminary models of the process. We will also provide an assessment of the consequences of this phenomenon, both for lithography development and photoresist design.

6519-30, Session 6

A novel plasma-assisted shrink process to enlarge process windows of narrow trenches and contacts for 45-nm node applications and beyond

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Limited process windows limit the scaling of critical IC features such as holes (contact, via) and trenches (required for interconnects and double patterning applications). To overcome this problem, contacts or trenches can be oversized during the exposure, followed by the application of a shrink technique. Various shrink techniques are proposed already, each with advantages and drawbacks [Ref. 1].

We propose a novel shrink process, based on plasma-assisted polymer deposition: a polymer is grown on the photoresist top and sidewalls by alternating deposition and etch steps, reducing the dimension of litho pattern in a controlled way. Hence small patterns can be defined with wide latitudes. Moreover, a thinner resist can be used during the litho step, increasing process windows even more. This new technology can be interfaced with existing etch platforms hence allowing for an 'in situ' approach.

The proposed approach is generic, applicable to both trenches and contacts, hence the feasibility was demonstrated for both.

Trenches.

Figure 1 shows typical examples of CD shrink on a line-space pattern. Trenches down to 80nm (160nm pitch and iso) are patterned in 220nm resist, using a 0.75NA scanner (dipole and annular illumination, 193nm dry litho). Flat wafers with a stack of SiC, 150nm SIOC:H low-k dielectric and a capping oxide are used. Trenches are shrunk down to ~40nm after etch of the whole stack, with very good CD control, related to the large process windows. After full Cu metallization, the wafers were sent for electrical measurements demonstrating excellent yield hence very good across wafer uniformity, down to the 40nm trenches (See Fig. 2).

Contacts.

A typical example are contacts patterned down to 150nm CD, in 400nm thick resist, on planar oxide wafers and wafers with CMOS topography (dry ARF litho, 0.75NA). The amount of shrink is time controlled and can be realized up to at least 75nm, resulting in contact CDs down to 75nm (see Fig 3). Moreover, the longer shrink times result in less contact roughness (see Fig. 4: shrunk contacts after oxide etch). Similar results, with contacts shrunk down to 100nm, are obtained on topography wafers, where both deep contacts to active area and shallow contacts to poly are patterned (illustrated in Fig. 5). A remarkable good CD control can be achieved for these small features through a widening of the process window.

During the presentation, we will discuss various properties of this plasma-assisted shrink technique, such as: controllability of the shrink, improvement of process windows, CD uniformity, proximity effects and LER. Both dry and immersion resist will be looked at, using various NAs and illumination conditions.

Ref. 1: Jung Hwan Hah et al., JJAP, Vol. 43, No. 6B, 2004, pp.3663-3667

6519-31, Session 7

A novel method for characterizing resist performance: simultaneous optimization for sensitivity, line-width roughness, and resolution

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In this paper the use of a single parameter is proposed to judge resist performance when simultaneously optimizing for sensitivity, line width roughness (LWR) and resolution. This parameter has been determined for a series of EUV and 193nm immersion resist materials in order to determine their relative performance. Additionally, from such an analysis the general improvement in resist technology over time is obtained.

It is now widely recognized that sensitivity, LWR and resolution are fundamentally linked, mainly by shot noise statistics and acid diffusion. Resists may be tuned to meet the individual specifications for sensitivity, LWR or resolution, but this is of no practical interest when it is done at the expense of one of the other parameters. This observation can be graphically depicted in an uncertainty triangle and has been termed the 'Lithographic Uncertainty Principle'. The simultaneous optimization of resists for these three parameters has been identified as the most critical issue for the successful introduction of EUV lithography at the 2005 EUVL Symposium. However, it should be noted that the fundamental interdependency of these three parameters is a general phenomenon for optical lithography, and not a specific EUV problem. As 193nm immersion lithography pushes to 45nm half pitches and lower, these phenomena will also become of increasing interest for this technology.

When optimizing or screening resists formulations, an important question is how to objectively judge resist performance when comparing materials for these three parameters at the same time.

The relations between LWR and sensitivity, resolution and acid diffusion length and LWR and acid diffusion length have all been theoretically described. Experimentally, good quantitative agreements have been obtained between the model expressions and experiments based on a series of model resists. However, each of these descriptions only covers one side of the uncertainty triangle.

In this paper we propose to combine these theoretical descriptions, yielding a single Figure of Merit. This Figure of Merit, which is determined from sizing dose, imaging wavelength, exposure latitude, acid diffusion length, LWR and pitch allows for a direct comparison of very different resist formulations. Moreover, at a given value of this Figure of Merit (i.e. for a given resist performance) it allows to predict the optical imaging or processing requirements to meet certain resist performance specifications. For instance dose requirements for a certain LWR specification, or acid diffusion length requirements to obtain a certain exposure latitude can be predicted.

This approach has been applied to a number of resist platforms using both EUV and 193 immersion lithography. The Figure of Merit for the Lithographic Uncertainty Principle proves to be a powerful technique for both evaluation and development of future resists chemistries.

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6519-32, Session 7

The tri-lateral challenge of LER, resolution, and photospeed: sub-32-nm modeling and experiments using ArF and EUV

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We derive a simple analytical LER model based on stochastic fluctuations of photon and acid number densities. Counting statistics are applied to a region defined by the effective acid diffusion length; these statistics are then modulated by the slope of the image intensity to produce a value for LER. This model produces the familiar effect that higher doses are generally required to simultaneously improve both resolution and line edge roughness. We compare to other similar models, as well as to sub-32nm experimental data at two very different wavelengths. In the case of 193nm, there is a relative abundance of photons, while the probability (quantum efficiency) for each photon to activate a photo-acid group is low. In the case of EUV (13.5nm), there are few photons but the quantum efficiency is high. But in either case, the dose increases as feature size and LER decrease. Finally, we discuss the potential to lower LER using post-processes techniques and radically different chemical platforms. This discussion also includes the challenge of impacting the relatively long-wavelength spatial frequencies seen in experimental measurements to contribute most LER.

6519-33, Session 7

PAG segregation during exposure affecting innate material roughness

T. H. Fedynyshyn, D. K. Astolfi, A. Cabral, MIT Lincoln Lab.; J. M. Roberts, Intel Corp.

Increased understanding of fundamental resist material characteristics is needed to develop resists with improved resolution and line edge roughness. A material's characteristics will not only influence resist sensitivity and resolution, but they also may influence the critical dimension control of the lithography process through their effects on line width roughness (LWR). Critical dimension control at sub-100 nm resolution will be extremely sensitive to the fine details of the molecular structure.

We have developed an AFM-based technique to measure intrinsic material roughness (IMR) after base development. This method involves performing an interrupted development of the resist film and measuring the resulting film roughness after a certain fixed film loss. We have performed this technique on exposed resists with a fixed dose and variable develop times. We have found that similar results can be obtained by measuring the film roughness with a fixed develop time and variable dose, and thus a simple contrast curve can yield information on the innate material roughness of the exposed resists.

Experimentally, we have found that the IMR is dependent on the PAG and the polymer employed in the resist. The IMR of the resist is also strongly dependent on the bake conditions, with increasing IMR at higher bake temperatures. Several PAGs have been identified that result in significantly lower material roughness and thus the potential for significantly reduced line width roughness in resist imaging. We will also present evidence for PAG segregation during the bake steps being responsible for increased IMR in exposed resists, presumably by increasing the dissolution rate inhomogeneity on a nano-scale level. We will also show how the effects of PAG segregation can be mitigated by the choice of PAG and polymer for the resist.

The Lincoln Laboratory portion of this work was sponsored by a Cooperative Research and Development Agreements between Lincoln Laboratory and Intel Corporation. Opinion, interpretations, conclusions, and recommendations are those of the authors and are not necessarily endorsed by the United States Government.

6519-34, Session 7

A mechanistic model for line-edge roughness

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Physically-based photoresist models, such as those in PROLITH, have been very successful in describing photolithography from a continuum standpoint. These models allow engineers to accurately predict the final resist CD on the wafer and to analyze process robustness, such as calculation of focus-exposure process windows. However, as feature sizes continue to shrink, we are beginning to see yield-limiting phenomena that are due to the molecular nature of photoresist materials. One example of this is line-edge roughness (LER). LER is believed to be due to fluctuations during the exposure process (shot noise) and post-exposure bake (thermal diffusion and reaction). We present a model that explicitly takes into account the molecular nature of the photoresist during the exposure and post-exposure bake processes. We do this by writing a Master Equation that describes the probability that acid molecules are generated during exposure, and then describes the evolution of the acid, quencher, and blocking-group probability distributions during the bake process. We show how all the parameters in this model can be simply derived from the parameters in a calibrated PROLITH continuum model. Finally, we demonstrate prediction of LER from an accurately tuned PROLITH continuum model and compare the LER predictions with experimental results.

6519-35, Session 7

The characterization of photoresist for accurate simulation beyond Gaussian diffusion

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With the continued shrink of integrated circuit fabrication groundrules, the photolithography process penetrates deeper and deeper into the regime where performances are dominated by optical proximity effect. The achievement of good critical dimension (CD) control becomes more and more dependent on optical proximity correction (OPC). Current simulation capabilities involve a first principle aerial image simulation algorithm, such as the transmission cross coefficient (TCC) algorithm, and a resist model, which captures the dynamics of the chemical amplification and the developing process. In the past few years, it has been found that the key photolithographic parameters, such as, the exposure latitude (EL) and the mask error factor (MEF) for the dense features can be very accurately simulated by the algorithm in which the latent image are made by simple Gaussian diffusion of the aerial image. However, more detailed comparison between the simulation and experiment in isolated features, or two-dimensional (2D) features indicates that the current modeling algorithm is still not accurate enough. This has resulted in the fact that even advanced model based OPC may require hundreds, even a thousand experimental CD measurement points to make a confident fit between the simulation and real world data. In addition, the model made with such endeavor does not usually extend well beyond the minimum groundrule, which can cause sub-groundrule test structures to fail. Under ideal situation, as it is well known, the aerial image between the lines and spaces are symmetric. However, different resists prefers different biases. Some resists prefer underexposure while others prefer overexposure. In this study, we have studied the parameters of the photoresists other than the Gaussian acid diffusion, such as, the dissolution contrast curve and the acid loading and amplification factors. We found that the OPC behavior of the photoresists we have experimented is significantly linked to these parameters besides the Gaussian diffusion, which is the first order improvement of the simulation algorithm to the pure aerial image. In this paper, we will present our studies of several resists with varied dissolution contrasts and acid loading and amplification factors, and we will show the idea toward the derivation of a physical model to represent the effect of these parameters to the known OPC behavior.

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6519-37, Session 8

Direct measurement of the in-situ developed latent image: the residual swelling fraction

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The dissolution of partially deprotected chemically amplified photoresists is the final step in printing lithographic features. Since this process step can be tuned independently from the design of the photoresist chemistry, measurements of the dissolution behavior of photoresists may provide needed insights towards improving line-edge roughness. The residual swelling fraction (RSF) is the remaining photoresist that swells rather than dissolves in a lithographically printed feature. The latent-image shape, photoresist chemistry and composition, photoacid concentration, nanoscale deprotection morphology, and aqueous hydroxide properties contribute to the RSF. One measurement challenge is quantifying the RSF spatial extent at the line-edge. Contrast variant neutron reflectivity was developed and applied to quantify the nanometer-scale spatial distribution of resist and aqueous base developer near a developed model line edge. The magnitude of the spatial extent of the swelling measured during in situ development, rinse, and drying imply the resist profile at line-edge is dynamic on the nanometer scale. The main results regarding model 193 nm photoresists will be presented.

6519-38, Session 8

Fundamental limits to EUV photoresists: what resolution, LER, and sensitivity can be achieved?

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As the semiconductor industry continues to follow Moore's Law, the demand to print smaller features continues. Extreme ultraviolet (EUV) lithography is the leading candidate for 32nm half pitch manufacturing. Experimental results1,2 indicate that current resists lack the ability to simultaneously meet the 2005 International Roadmap for Semiconductors (ITRS) goals for Resolution, Line-edge/width roughness (LER/LWR), and Sensitivity (RLS). This RLS tradeoff has also been demonstrated through modeling work where Gallatin3 has shown that it will be very difficult to have a standard chemically amplified (CA) resist that simultaneously has low LER, low dose, and high resolution. Clearly, the fact that the three most critical resist characteristics are in opposition, raises serious questions about whether EUV resists will ultimately be capable of delivering the needed performance. Indeed, last fall EUV resist limitations were named the number one critical issue to EUV technology implementation.

In this work we present an improved LER model and use it to explore the impact of three properties: (1) Anisotropic acid diffusion. Allowing for anisotropic diffusion alters a fundamental assumption in the original model and hence alters the RLS tradeoff. We will show how the tradeoff is changed and improved. (2) Increased quantum yield. Increasing the quantum yield (≡ the number of acids generated per photon), clearly improves sensitivity. There are several ways of increasing quantum yield and each has a specific impact on the deprotection distribution and hence on LER and resolution. The RLS impact of these various methods will be compared and contrasted. (3) Secondary electrons. The EUV exposure mechanism involves secondary electrons.2 The spatial range of these electrons nominally decreases resolution, an effect which has not been accounted for in previous models. However, if these electrons can be harnessed to significantly increase quantum yield while keeping their spatial range small it may be possible to use them to improve the RLS tradeoff.

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6519-39, Session 8

Etch resistance: comparison and development of etch-rate models

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Etch resistance and post etch roughness of ArF photoresists still remain one of the main critical issues during process integration for sub-100nm technology nodes. Compared to phenyl-containing KrF polymers, methacrylate polymers commonly used for ArF lithography show weak bulk etch resistance in addition to a highly damaged surface after standard etch processes.

There are a number of etch models in the literature which attempt to describe the correlation between polymer structure and blanket etch rates. Ohnishi and Ring Parameter are the most common etch models correlating atomic and structural trends in the resist polymer and etch rates. These etch models have been tested in two ways: systematically changing the composition of a terpolymer and using polymers with different functional groups. By comparing the etch rates of this large series of polymer structures it was found that these etch models were not sufficient in describing the relationship between the atomic or structural trends in polymer with etch rates. A new etch model that describes the structure property relationship and etch rate trends has been developed. This new model shows a better correlation with the observed experimental results and was further tested with new polymer structures.

6519-40, Session 8

Dissolution behavior of resist polymers studied by Quartz-Crystal-Microbalance method II

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Development process of resists plays an important role to determine the resist performance such as resolution, line-width roughness, pattern collapse, and so on. Quartz-Crystal-Microbalance (QCM) method has been applied to obtain the detail information of dissolution behaviors.[1] QCM has the advantage to measure in-situ film thickness with highest resolution during the development. The traditional Sauerbrey equation, which assumes the proportionality of film thickness to the shift of resonance frequency, is used to analyze the QCM traces.

Another advantage of QCM method is that QCM measurement includes the film properties such as rigidity of a swelling layer during development. The four-layer model including the gel layer formed during the development has been proposed to get the quantitative information of development kinetics.[2] The transmission-line analysis of the four-layer model was used to interpret some behaviors of swelling and residues and showed that the Sauerbrey relation does not hold in some cases. [3,4] The analyses of swelling kinetics during development are very important to characterize resist materials and give the information to reduce the line-edge roughness and to improve the resolution. However there are many complicated curves of QCM measurements to be interpreted. One of the peculiar QCM data shows plural peaks in resonance frequency and impedances during the development. We applied the transmission-line analysis to the QCM data and obtain the changes of rigidity of swelling layer in addition to the thicknesses changes of dry layer and swelling layer. The formation of swelling layer causes the broad peak of resonance frequency at the beginning of development. An impedance peak follows the frequency peak. The time difference between the frequency and impedance is ca. 15 seconds when the rigidity of the swelling layer decreased to ca. 10^5 [Pa] by the absorption of developer. The second peak of impedance is related to the disappearance of the swelling layer. In this way QCM traces give the clear picture of resist development kinetics. At the conference the typical QCM traces will be elucidated by the transition-line analysis.

In addition to the QCM analysis we have improved the time resolution of QCM apparatus from 20 Hz to 1,000 Hz. This fast measurement will give the precise information on the interface between resist and substrate, fast dissolution of de-protected base-resin. At the conference the experimental data using this fast QCM measurement system will be reported.

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6519-41, Session 8

Investigation of capillary bridges growth in NIL process

S. Landis, Lab. d'Electronique de Technologie de l'Information (France)

The NanoImprint Lithography (NIL) is a promising technique for numerous applications, but industrial applications require a high control of the defects which can appear in the printed resist [-]. The objective of this paper is to demonstrate that it is possible to predict and control the formation of the defects induced by capillary forces between the fluid polymer and the mold surface. Capillary bridges appear when the gap between the mold and the polymer is small enough to induce the growth of polymer dots by capillary forces [ ] (figure 1). This growth may be also influenced by the mold deformation. This paper presents a determination of the mold/polymer distance allowing the bridge growth and a study of the defect number and evolution as a function of the temperature, polymer thickness and mold/polymer gap.

Thanks to successive etching steps, the stamp cavity depth varies from 12 to 224 nm. Therefore, we will investigate the impact of the distance between the surface of the unprinted polymer and the stamp's surface onto the capillary bridge growth in a same printing and demolding conditions.Optical images of the printed wafers have been performed (figure 1) and statistical analyses were carried out to extract their size distribution, locations, number versus the process conditions (printing temperature, resist thickness, cavity depth...).

The bridge number has been systematically measured. The number of capillary bridges is presented as a function of the cavity depth in figure 2. For each mold depth, 5 images have been analysed, and the resulting average number is reported. This statistical analysis explains how the bridge number can be lower than 1, and not an integer number. This value corresponds to the average number bridge number in 400x400 µm(c)ˇ. This means that the defect density varies from 3.10-3 to 3.10-6/µm(c)ˇ. The bridge number in a 12 nm deep cavity is not indicated since there are so many defects that they interfere and coalesce together. The result shows that the cavity depth has a very high influence on the defect number since a logarithmic scale has to be used. This decreasing behaviour is characteristic of long range forces. It can be noticed that the defect number is very small for cavity depths higher than 40 nm, and no capillary bridge appear when the polymer/mold distance is larger than 80 nm.

We have also studied the relationship between capillary bridges growth and small asperities onto stamp surface. Figure 3 represents, the probability that a capillary bridge appears n times (n ranging from 1 to 10) at the same place. We pointed out that specific points onto stamp surface are preferential sites for capillary bridge growth. Atomic Force Microscopy investigations of the stamp surface will be also presented. We will present in this paper the evolution of the defects during the filling of the holes depending on the printing conditions. This will be equivalent to an in-situ observation of the bridge evolution during the printing process.

6519-43, Session 9

Component segregation in model chemically amplified resists

J. T. Woodward, National Institute of Standards & Technology; T. H. Fedynyshyn, D. K. Astolfi, S. G. Cann, MIT Lincoln Lab.; M. J. Leeson, Intel Corp.

The development of resists capable of low line width roughness (LWR) is required to maintain the ratio of LWR to critical dimension (CD) necessary for reliable device performance. To do this requires a fundamental understanding of resist material characteristics and how they evolve during the lithography process. One potential source of LWR is component segregation. In this study we look to see if photo acid generator (PAG) segregates from the resist polymer and whether this influences surface roughness during development. We have previously used partially developed samples of model resists exposed with a series of doses to study interfacial roughness as a function of dose and resist composition.4,5 Using similarly prepared samples we have used chemical force microscopy (CFM) to measure the chemical heterogeneity of the partially developed resist interface.

Gold coated AFM tips were functionalized by incubating in a 0.1 mM solution of octadecanethiol in ethanol to form a methyl terminated self-assembled monolayer. The tip was scanned in chemical force mode, in which the tip is scanned in contact with the sample and perpendicular to the cantilever direction, to measure the chemical dependent friction between the tip and sample.

Our model resists consisted of poly(hydroxystyrene-co-styrene-co-t-butylacrylate-co-acrylic acid) (Mn = 9,000 and Mw = 15,000) and either di(t-butylphenyl)iodonium nonafluoro-1-butanesulfonate or triphenylsulfonium nonafluoro-1-butanesulfonate as a photo acid generator. All exposures were with a Canon EX-4 248-nm 0.6NA stepper.

Chemical force imaging simultaneously collects topography and chemical force data allowing the direct correlation of chemistry to surface topography. Topography data confirm our previous results showing a periodicity in the RMS surface roughness as a function of dose. Partially developed samples of exposed and unexposed polymer with PAG show strong chemical contrast indicating chemical segregation in the sample. The surface morphology and distribution of the chemical signal is different for the two PAGs. Variations in chemical force have a lateral dimension on the order of 100 nm based on autocorrelations of line sections through the chemical force image. A negative control sample of unexposed polymer with no PAG has low RMS roughness and little chemical contrast in both undeveloped and partially developed samples.

We conclude that PAG segregation is a potential contributor to long wavelength LWR and that CFM is a useful tool for probing chemical heterogeneities at resist surfaces.

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6519-44, Session 9

FTIR measurements of compositional heterogeneities

S. Kang, B. D. Vogt, W. Wu, V. M. Prabhu, D. L. VanderHart, A. B. Rao, E. K. Lin, National Institute of Standards and Technology; K. L. Turnquest, SEMATECH, Inc.

A chemically heterogeneous local structure in model photoresist polymer thin films was probed and quantified by Fourier transform infrared (FTIR) spectroscopy. This heterogeneity was formed by an in situ photoacid catalyzed deprotection reaction-diffusion process which leads to methacrylic acid (MAA)-rich comonomer domains. The carboxylic acid groups can dimerize through hydrogen bonding within these domains, a FTIR measure of the fraction of hydrogen-bonded versus free moieties can be quantitatively related to the extent of heterogeneity. A hard spherical model supports a domain-state structure, rather than a statistically uniform homogeneous state. The extent of heterogeneity was found to be controlled by the photoacid concentration and copolymer composition. The methods and concepts developed for these photoresist polymers improve the understanding of the local structure formed in photoresists, which may help quantify origins of line-edge roughness.

Conference 6519: Advances in Resist Materials and Processing Technology XXIV

6519-45, Session 9

Changes in resist glass transition temperatures due to exposure

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Increased understanding of fundamental resist material characteristics is needed to develop resists with improved resolution and line edge roughness. A material's characteristics will not only influence resist sensitivity and resolution, but they also may influence the critical dimension control of the lithography process through their effects on line width roughness (LWR). Critical dimension control at sub-100 nm resolution will be extremely sensitive to the fine details of the molecular structure.

We have developed an AFM-based technique to measure intrinsic material roughness (IMR) after base development. Employing this technique we have deconstructed the resist into component parts and have shown that PAG is a major contributor to intrinsic material roughness. It has also been shown that no difference in IMR occurs between exposed and unexposed PAG in a model resist.

When PAG is exposed and thermal polymer deprotection is allowed to occur, as is normal in acid catalyzed resists, increased levels of IMR are present. The IMR of the resist is strongly dependent on the bake conditions, with increasing IMR at higher bake temperatures. This leads to the suspicion that the resist glass transition temperature (Tg) may be responsible for the changes in the level of IMR observed with both different polymers and bake temperatures. Such an effect would be consistent with PAG segregation playing a major role in defining the film IMR.

We have measured the glass transition temperature of resists, both exposed and unexposed, and show the effect of changes in resist glass transition temperature on IMR as well as the change in resist glass transition temperature as a function of exposure dose and level of polymer deprotection. Unique and unpredicted glass transition temperatures will be presented and rationalized.

This work was sponsored by a Cooperative Research and Development Agreement between MIT Lincoln Laboratory and Intel Corporation. Opinions, interpretations, conclusions, and recommendations are those of the authors and are not necessarily endorsed by the United States Government.

6519-46, Session 9

The study and material design for the reduction of LWR

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Research and development efforts for semiconductor device manufacturing now shift to the 32nm node and below. For the patterning of such an ultra-narrow patterns (<32nm), reduction of line-width roughness (LWR) becomes a critical issue, i.e., the demand of LWR reduction reaches <3 nm (3 *). Resist material design should be essential factor for controlling LWR less than 3 nm. In this paper, we will discuss about critical issues and material design for the reduction of LWR. In addition, a new method to clarify the material origin of LWR will be also discussed. Finally, current goal of LWR beyond 32nm node device manufacturing will be described.

An understanding of acid-diffusion reaction in chemically amplified resist during the post-exposure bake (PEB) process is critical issue for the reduction of LWR. In order to achieve LWR reduction to 3 nm, suppression of extra acid diffusion is essentially required. For the purpose of suppressing acid diffusion, we developed new PAGs with bigger molecular size. Applying these materials to ArF resist, acid diffusion was successfully suppressed, and reached to 30% level of our conventional ArF resist. Relation between acid diffusion and LWR will be discussed in detail.

Another key factor is uniformity of the deprotection reaction of acid labile group in base polymer during PEB process. In order to clarify effect of the reaction uniformity on LWR, we measured surface roughness (Ra) of resist films using AFM apparatus. In our previous study, we have revealed that Ra is well correlated with LWR, and therefore can be used as a good indicator of LWR. Figure 1 shows the effects of local distribution of the deprotection reaction on the surface roughness. By suppressing reaction locality, surface roughness Ra decreased from 6.6 nm to 2.8 nm (60 % down). This result clearly indicates that uniformity of deprotection reaction is critical factor for LWR reduction. Uniformity of the deprotection reaction is quantitatively evaluated as monomer sequence distribution of polymer during PEB process. Details about quantitative analysis of monomer sequence distribution and material design for LWR reduciton will be described in this paper.

6519-48, Session 9

Impact of line-width roughness on Intel's 65-nm process devices

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Line Width Roughness (LWR) is the random variation of MOS gate length along the gate width. LWR is undesirable because it degrades drive current (Ion), increases off-current (Ioff), and causes a random variation of device currents across a die. Previously [1] it was determined that LWR did not impact Intel's 130 nm process devices. As device sizes shrink, the sensitivity to LWR increases, so the amount of LWR that can be tolerated in future generations needs to be re-assessed.

In this paper we will present the experimental results of the effects of LWR on Intel's 65 nm process.

Intel's 65nm process includes 1.2nm gate oxide, 35 nm gate lengths, 8 metal layers, and second-generation strained silicon. Gate patterning was done using Alt. PSM and LWR was intentionally induced by exposing the contact mask pattern over the gates. Higher contact exposure doses resulted in larger LWR and smaller gate CDs. Wafer splits were created with appropriate exposure dose at gate lithography to compensate for the smaller CDs arising from the double exposure. The LWR was measured after gate etch (Final Check CD) and electrical (e)-test data measured after metal patterning.

It was found that both nominal drive current and its variation degrade with increased LWR. Additionally, Ioff increased exponentially with increased LWR. In order to maintain less than 2% degradation in Ion from LWR, the 3-Sigma % LWR should be less than 10% FCCD. Thus, for future generations, LWR needs to scale as gate lengths decrease or else any potential benefits in increased drive current would be offset by large amounts of leakage.

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6519-162, Session 9

Line-edge roughness in 193-nm resists: lithographic aspects and etch transfer

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The performance characteristics of transistor gates degrade as the magnitude of line edge roughness (LER) on the gate increases. The effect becomes increasingly problematic as the critical dimension (CD) of the gate decreases. LER originates in lithographically patterned chemically amplified photoresists and is transferred to underlying substrates during etching. Major efforts to understand and minimize the magnitude of LER in patterned resist features and in patterned substrates are ongoing.1 We describe a method to determine transfer functions for line edge roughness (LER) from the photoresist pattern through the etch process into the underlying substrate. Both image fading techniques and more conventional focus-exposure matrix

methods may be employed to determine the dependence of photoresist LER on the image-log-slope (ILS) or resist-edge-log-slope (RELS) of the aerial image. Post-etch LER measurements in polysilicon are similarly correlated to the ILS used to pattern the resist. From these two relationships, a transfer function may be derived to quantify the magnitude of LER that transfers into the polysilicon under layer from the photoresist.2

A second transfer function may be derived from power spectral density analysis of LER. This approach is desirable based on observations of pronounced etch smoothing of roughness in specific spatial frequency ranges. Fast-Fourier transform noise significantly limits the utility of this approach; smoothing functions and signal averaging of large numbers of line edges may be used to partially compensate for noise effects. An alternative and superior approach is to derive transfer functions from power spectral densities generated using autoregressive algorithms.3

The utility of these methods to multiple photoresist and etch processes will be described.

6519-49, Session 10

New resists and processes for UV-imprint lithography

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UV-assisted imprint lithography has the ability to be a truly disruptive technology and critically relies on the nanometer scale control of polymer properties, interfacial bonding and deformation characteristics of polymeric materials at near molecular dimensions, for their successful performance. Nanoimprint lithography is intriguing from a cost perspective since imprint systems do not require the sophisticated optics of conventional photolithography systems which reduce the image on a mask by four times with either projection or reflection optics. Rather, imprint lithography uses polymers that harden while conforming to a physical template upon exposure to ultraviolet light or upon a thermal transition. We have developed a nano-contact molding (NCM) imprint lithographic technique for the replication of nanometer-scale features using functional crosslinked polymeric materials. The NCM process offers many advantages over other imprint lithographic processes including the ability to utilize inexpensive templates, excellent control of the chemistry of the molded polymer and the ability to perform surface transformations via the incorporation of reactive functionality into patterned crosslinked polymers.

One of the most critical material components in the imprint lithographic process is the photopolymerized resist layer; sometimes this resist layer is called the etch barrier or imaging layer. The resist polymer chemistry needs to be designed so that it provides higher etch resistance (selectivity) than the underlying layer which allows for pattern transfer. A number of assumptions have been made regarding properties required by the resist. These presumptions include: (1) low viscosity of monomer solution; (2) rapid photocuring to high conversion; (3) low separation forces between the cured photoresist and mold; (4) mechanical properties for image fidelity; and (5) high etch resistance. Most reported imprint resist systems utilize the incorporation of organosilicon compounds into the resin to facilitate etch resistance. These siloxane-based resists however suffer from several limiting factors. First, the high siloxane content results in a low modulus, rubbery film after curing. The low modulus effects pattern fidelity which results in distorted replicated features when molding at small dimensions. Secondly, most UV-assisted imprint resists rely on acrylate or methacrylate curing chemistry, which suffers from oxygen inhibition and results in partial or incomplete curing during irradiation. Finally, there are difficulties separating the cured siloxane monomers from quartz molds - especially when trying to cure high aspect ratio features - due at least in part to the poor mechanical properties of the cured siloxane acrylates. These factors combine to give imperfect pattern transfer and catastrophic contamination of the expensive quartz imprint mold.

There has been recent work aimed at reducing some of these limitations and expand the utility of UV-assisted imprint lithography. For example there have been recent reports on the use of cationically cured vinyl ether monomer as well as thiol-ene photopolymers. Our group has been investigating some of these alternative cure chemistries as well as the incorporation of non-silicon containing organometallic etch resistant monomers such as phosphazenes and titanates. We now report our latest results in the development of alternative imprint resists as well as new advances in lift-off patterning techniques in imprint lithography.

6519-50, Session 10

Impact of curing kinetics and materials properties on imprint characteristics of resists for UV-nanoimprint lithography

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The requirement that UV-curable nanoimprint resists have low viscosity places a significant constraint on the components of a successful formulation, whether it is all-organic or silicon-containing. This is a particularly important concern when polyhedral oligomeric silsesquioxane (PSS) materials are used as a platform for a nanoimprint resist as they can be quite viscous. Recent reports have shown these materials to be useful candidates for functional imprintable dielectric materials when functionalized with suitable polymerizable groups such as epoxies and acrylates.[1,2] In this study we describe an alternative resist design using methacrylate functionalized PSS with added methacrylate diluents to reduce the viscosity to an acceptable range. The diluents include ethyl hexyl methacrylate, cyclohexyl methacrylate and isobornyl methacrylate, selected to investigate the impact of Tg on the properties of the imprinted material. The choice of diluent has a significant impact on degree of cure achievable as measured by photo differential scanning calorimetry and infrared spectroscopy. We have found that of the order of 10% of the carbon-carbon double bonds is initially consumed during cure, depending strongly on diluent structure, with a much slower subsequent reaction within the stiffened gel as irradiation continues. Because the sensitizers used absorb more strongly in the deep UV than in the mid UV significant differences are found between the curing kinetics and achievable degree of cure as a function of wavelength. Results of measurements of Tg and modulus of the resists as a function of cure will be presented, along with data showing that the degree of cure significantly impacts the adhesion strength and the crack path during wafer-template debonding. Using these data and corresponding imprint patterning results we will discuss the desirable characteristics of useful diluent systems.

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6519-51, Session 10

Material design of negative-tone polyphenol resist for EUV and EB lithography

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It is difficult to meet specifications for sensitivity, resolution, and line-edge roughness (LER) simultaneously in hp32-nm technology node. Especially, LER is widely recognized as one of the most critical issue in scaling of MOS LSIs. In order to reduce LER, we have investigated molecular resists because larger molecular weight and larger molecular-weight distribution of polymer resists are major origins of LER. Thus far we showed that a chemically-amplified (CA) positive-tone molecular resist for EUV and EB lithography using a partially-protected polyphenol was effective to reduce LER [1]. We also reported a non-crosslinking negative-tone molecular resist using 3M6C-MBSA-BL synthesized from 3M6C-MBSA based on intramolecular esterification of gamma - hydroxycarboxyl acid moiety. It showed 40-nm line and space (L/ S) resolution capability at an EB dose of 72 uC/cm2 and low LER value [2]. Also the resist showed 30-nm L/S resolution using small-field EUV exposure tool (HiNA3) in ASET [3-5]. Number of the introduced gamma-hydroxycarboxyl group into a 3M6C-MBSA-BL molecule was ca. 1 on the average.

In this paper, we discuss material design of the resist to improve performance. The resist compound used in the previous paper[2] had distribution of number of the functional group from 0 to 4 in a molecule measured by HPLC. For the purpose of improvement of the resist performance, it is necessary to clarify property of the 3M6C-MBSA-BL molecules with different number of the functional group separately. Here we propose a molecular resist made of functionalized polyphenol molecules with only one functional group in a molecule. We report design and synthesis of the resist material of mono-protected 3M6C-MBSA-BL (3M6C-MBSA-BL1). The property of the material and result of evaluation of resist performance are also discussed.

Resist compound (3M6C-MBSA-BL1) with only one functional group of the gamma-hydroxycarboxyl acid per a molecule was synthesized by modified method of the way in the reference [2]. The synthesized polyphenol compound and photoacid generator (triphenylsulphonium triflate, TPS-TF) were dissolved in solvent and formed resist films. In order to evaluate the resist resolution, an electron beam (EB) exposure system (Hitachi HL-800DE, 75 kV) was used. After optimization of formulation, resist using 3M6C-MBSA-BL1 showed sub-50-nm L/S resolution at a dose of 34 uC/cm2 under a process condition of pre-baking at 100 ºC for 90 s, post baking at 90 ºC for 120 s and development in 2.38% TMAH. 3M6C-MBSA-BL1 showed higher sensitivity than former 3M6C-MBSA-BL. This result indicates effectiveness of the mono-disperse material of 3M6C-MBSA-BL1 for improvement of resist performance. Also results of EUV imaging and LER measurement of the resist using 3M6C-MBSA-BL1, property of di-functionalized mono-disperse molecule (3M6C-MBSA-BL2) and resists using it will be reported in the conference.

This work was supported by the New Energy and Industrial Technology Development Organization (NEDO).

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6519-52, Session 10

Photo-acid generator quantum efficiency and line-edge roughness behavior in novel polymer-bound PAG 193 nm and EUV photoresists

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Substantial improvements in photoresist materials design, which can provide higher photosensitivity and precise critical dimension and line edge roughness (LER or line width roughness (LWR)) control, are required to enable the application of next generation lithography technology and the production of future sub-65 nm node IC device generations. In order to achieve the desired resists sensitivities, it appears that innovative solutions to solving the resolution and line edge roughness problems in chemically amplified resists (CARs) will be required to achieve all of the desired photoresist properties. To that end, we have been investigating the properties and performance of novel CAR resists that directly incorporate photoacid generator (PAG) groups into the polymer main chain. Direct incorporation of the PAG into the polymer chain is expected to provide a number of benefits including higher PAG loadings, reduced photoacid diffusivity, better uniformity of PAG and photoacid distribution within the resist film, and reduced outgassing. To that end, a variety of CARs have been designed and studied for 193 nm and EUV lithography that include PAG units in the main chain. These materials have qualitatively been shown to provide good imaging performance with apparently reduced photoacid diffusivities, higher PAG loadings and photospeeds, reduced outgassing, and better thermal stabilities.

The polymer-bound PAG CARs have demonstrated some of the superior performance advantages as compared to traditional blended PAG CARs such as improved resolution for analogous materials. However, experimental results also showed that the photosensitivity of some of the polymer-bound PAG resists was lower than that of the analogous blended PAG resists. The structural modification and direct attachment of the PAG moiety to the polymer backbone has the potential to alter the photoreaction rates for a PAG due to the differences in both the manner in which energy absorbed in the resist can be transferred to the PAG and the manner in which absorbed energy can decay in a non-productive fashion. Since reductions in photosensitivity are not desirable, one goal of our work is to understand the structure-property relationships in these materials to provide resist design guideline for preventing such problems. As mentioned previously, another desirable outcome of incorporation of the PAG into the polymer main chain would be production of resists with reduced LER and LWR. The complex interplay between photoacid diffusion, deprotection volumes, and the polymer molecular structure and nanomorphology is believed to be one of the origins of LER and LWR. It is anticipated that by reducing photoacid diffusivity, through binding of the PAG and resulting photoacid to the polymer chain, the resulting deprotection volume produced by each photoacid should be reduced. Since higher PAG loadings are possible with the polymer-bound PAGs, it should be possible to offset the possible reduction in resist sensitivity due to this reduced acid catalytic chain length while providing a line edge due to overlap of the smaller photoacid deportection volumes. Quantification of photoacid diffusion and LER/LWR in polymer-bound PAG resists and comparisons to analogous blended-PAG materials is also a major thrust of our work.

In this work, a novel method for determining photoacid generation rate constants and PAG quantum efficiencies has been developed. This new method has been applied to the study of 193 nm and EUV chemically amplified resists based on * -butyrolactone-methacrylate(GBLMA)-co-2-ethyl-2-adamantyl-methacrylate(EAMA) and p-hydroxystyrene (HOST)-co-EAMA polymers. In these polymer resins, different PAG incorporation methods including blended PAGs, cation-bound PAGs, and anion-bound PAGs have been studied to determine the effect of the PAG incorporation method on the PAG photoreaction rate and quantum efficiency (see Figure 1 for examples of 193 nm polymer-bound PAG CARs studied in this work). The effect of the method of PAG incorporation on LER and LWR in these materials will also be reported.

6519-53, Session 10

Novel anionic photoacid generator (PAGs) monomers and photoresist polymers for sub-50-nm patterning by EUV and electron-beam lithography

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Extreme ultraviolet (EUV) lithography at a wavelength of 13.5 nm has emerged as a promising candidate to meet the upcoming resolution requirements for semiconductor device manufacturing. In addition to developing the exposure tools themselves, significant challenges remain in developing photoresist materials that possess all of the required imaging properties. At the 45 or 32 nm technology node, the sensitivity of a resist must be approximately 10 mJ/cm2 or less, and patterned features must exhibit a line edge roughness of less than 2 nm. Conventional chemically amplified photoresist formulations are complex mixtures of a protected polymer matrix and a small molecule photoacid generator (PAG). The inherent incompatibility between these two types of materials can lead to PAG phase separation, non-uniform initial PAG and photoacid distribution, as well as acid migration during the post-exposure baking (PEB) processes. To alleviate these problems, Stewart and coworkers have reported the potential use of polymeric PAGs blended with a chemically amplified resist for controlling acid diffusion and outgassing. In our work, the focus has been to go one step further and combine photoacid generating moieties directly into the photoresist polymer matrix backbone. Several systems

with both ionic and non-ionic PAGs incorporated in the main chain have been studied. The incorporation of ionic PAG units into the main chain of the hydroxystyrene and adamantyl methacrylate based polymers showed improved EUV lithographic performance, such as faster photospeed, higher stability, lower outgassing, and lower line edge roughness (LER), as compared to the analogous blended PAG resists. Here we report novel blended anionic PAGs, anionic PAG monomers, and the resulting polymers that directly incorporate these anionic PAGs into the main chain. They were prepared in moderate to good yield and characterized by NMR, elemental analysis, GPC, TGA and DSC. The thermal stability of PAG bound polymers was determined to be superior to that of their blended PAG analogs. Also, the fluorine-free polymer-bound and blended PAG polymers studied in this work exhibited higher thermal stability than fluorine-substituted polymer-bound and blended PAGs. It was found that the photoreaction rate constants and acid generating efficiencies of blended PAGs are higher than that of analogous polymer-bound PAGs. The polymer-bound PAG resists showed much higher exposure latitudes (\>10%) than analogous blended PAG resists. Also, the polymer-bound PAG samples were capable of printing higher resolution patterns, with 20 nm 1:1 line/space images being demonstrated using 100 keV electron-beam lithography. Outgassing and EUV lithography imaging performance of these materials will also be reported.

6519-54, Session 11

Fabrication of silica 3D structures from polyhedral oligomeric silsesquioxane (POSS) by multibeam interference lithography

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The concept of three-dimensional (3D) photonic crystals that possess an omnidirectional bandgap in the optical regime has stimulated extensive research on discovery of novel materials and fabrication processes. Among many 3D microfabrication methods, multibeam interference lithography (MBIL) is fast and flexible to achieve a wide range of lattices. However, most 3D structures produced by MBIL are from polymers or low-index inorganic materials (n<1.7), which do not possess complete photonic bandgap. Previously, we and other groups have investigated the fabrication of silicon photonic crystals through a double templating method using a sequential silica/silicon CVD process. Core-shell morphology is often revealed due to the difficulty to achieve complete filling during the CVD process. Here we explore the use of polyhedral oligomeric silsesquioxane (POSS) epoxides and their nanocomposites for patterning of 3D silica microstructures, which will allow for single-step templating of high index photonic crystals. We show that the fabricated POSS 3D structures can be converted to silica 3D structures at 500oC while maintaining the structure integrity. To improve the resist contrast and minimize shrinkage at 500oC, we will further discuss the optimization of resist formulation by introduction of silica nanoparticles and mixing with other types of silsesquioxane.

6519-55, Session 11

Self-aligned, self-assembled organosilicate line patterns of ~20nm half-pitch from block-copolymer mediated self assembly

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Self-assembly of block copolymers in thin films has generated enormous attention as it provides sub-lithographic patterns by very simple process with low cost. Indeed, their potential applications for several nano-fabrications have been already demonstrated: for example, electronic devices including capacitor, memory and transistor have been successfully fabricated by using an asymmetric (cylindrical morphology) diblock copolymer of polystyrene (PS) and poly(methyl methacrylate) (PMMA). The organic nature of most block copolymers studied, however, gives poor plasma etching contrast hence a layer of silicon oxide where the self-assembled block copolymer patterns are transferred is commonly used as a hard mask for underlying substrate etching. A robust, self-assembled inorganic nanostructure will be ideal to simplify the patterning process as the inorganic nanostructure as is can be used as a hard mask. In addition, the inorganic nanostructure has more potential for providing patterns of sub-10nm features with lower line edge roughness. Since the pioneering work of Kresge et al. to create ordered mesoporous silica, numerous approaches have been developed using low or high molecular weight surfactants or amphiphilic block copolymers in the synthesis of nanostructured inorganic materials. The prevalent route to mesoporous silica using amphiphilic block copolymers or surfactants is through sol-gel chemistry, which often makes it difficult to achieve continuous, high quality films on substrates by simple film formation methods such as spin casting. In this talk, we will report the formation of robust organosilicate line patterns of ~20nm half-pitch on surfaces from the self-assembled lamellar phase of a diblock copolymer of polystyrene and poly(ethylene oxide), PS-b-PEO, and an oligomeric organosilicate precursor mixtures. We could control the orientation and alignment of microdomains of this organosilicate thin film to the same degree of the thin films of organic block copolymers. By controlling the surface energy of substrates with dense organosilicate, the perpendicular orientation of lamellae to the surface was obtained. Topographic patterns of several hundreds nanometers in length scale were generated by traditional lithography and used for alignment of the line patterns from lamellar phase. Upon removing the organic component (i.e. PS-b-PEO) from thermally crosslinked organosilicate matrix, the organosilicate microdomains remain as periodic line patterns with global alignment on surfaces. This method gives a continuous, high quality coating of inorganic line pattern with sub-lithographic length scales on surface. We will report the results on pattern transfer of the self-assembled organosilicate line pattern into underlying silicon substrate using anisotropic plasma etching as well.

6519-56, Session 11

Gray-scale lithography of photosensitive polyimide and its graphitization

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Gray scale lithography GSL was implemented using an aqueous developing photosensitive polyimide, HD8820.

The positive photo resist lithography process was characterized on silicon substrates using a Karl Suss exposure system at various film thicknesses using a Gray Scale Lithography calibration mask. The GSL mask was made from a high-energy beam sensitive (HEBS) glass that is sensitive to electron beams but not to UV radiation. The test patterns are therefore first written on the Silver doped HEBS photomask using Electron Beam Lithography at varying optical densities corresponding to various gray levels. When used subsequently in a UV photo exposure tool, the original mask patterns are not affected while acting as masks of varying intensities to the UV radiation. Analytical quadratic polynomial relationships were obtained between the gray scale optical density and the film thickness. These relationships were then used to design the final product mask to yield tapered circular rings with increasing radial film thicknesses, using a 32 bit gray scale level.

The resulting tapered structures were converted to graphite at 650 C in a Nitrogen ambient to make them thermally resistant and yet adherent to the semiconductor substrates. Graphitization was performed to enable high temperature ion implantation of a dopant. Alternatively, the polyimide features could be transferred by 1:1 Reactive Ion Etching or by Ion Milling into underlying thin films of Silicon Dioxide or Silicon Nitride to be used as the implantation barriers. The graphitization, however, saves processing steps and the desired features were successfully fabricated and adhered well to the substrate.

After the graphitization, the original polyimide film thicknesses were reduced to thinner films of amorphous graphitized polymer. Rectangular test structures were fabricated with increasing film thickness varying over the entire range of optical densities. These test structure features were measured and the resulting film thickness was plotted versus the optical density to yield a polynomial regression equation. Several samples were repeated for one polyimide film thickness and subsequently graphitized. The entire process sequence was found to be repeatable to yield acceptable graphitized film thickness variation with gray scale optical density.

Fresnel microlens and optical gratings were also fabricated. The various electrical and optical graphitized test structures were characterized by SEM, AFM and Nomarski microscopy. The HD8820 has good mechanical, thermal and optical properties for applications in electronics, optics and MEMS. When converted to graphite, the polyimide features retained their shapes and adhered well to the silicon substrate.

The present application was to use the gray scale tapered graphitized polyimide at the edges of a cylindrical p+ anode as barriers to high temperature Boron ion implantation into Silicon Carbide substrates to fabricate Junction Termination Extensions with gradually decreasing p-type doping profile. Upon final design and fabrication, these power diodes and transistors are expected to withstand thousands of volts at high temperatures.

Other applications of the gray scale lithographic structures using the photosensitive polyimide include microelectronic devices, micro-optics, cantilevers, sensors, micro-fluidics, electronic packaging and MEMS.

6519-57, Session 11

A novel top surface imaging approach utilizing direct-area selective atomic layer deposition of hardmasks

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Area selective atomic layer deposition techniques (ASALDT) have recently been developed and reported by the authors. In this technique, deposition occurs only on the regions having active sites for ALD nucleation, whereas nucleation is blocked on regions where active sites are absent. In our previous studies we demonstrated that polymer films lacking hydroxyl sites (i.e. possessing no OH groups) can successfully block TiO2 ALD nucleation when titanium isopropoxide and water are used as ALD precursors. In contrast, a very conformal film of TiO2 is deposited on the surface of polymers possessing OH groups. In this paper, we report the use of this high contrast, selective growth of titania to develop a novel top surface imaging (TSI) approach. The feasibility of this approach is demonstrated using a chemically amplified resist system based on a blend of poly(tert-butylmethacrylate) and a photoacid generator. Polymer films are exposed (248 nm source) pattern-wise through a mask and after PEB, ALD active carboxylic acid (-COOH) groups are generated in the exposed regions. TiO2 is then selectively deposited only on the regions having active sites followed by dry etching using an O2 plasma to transfer the surface titania pattern through the entire thickness of the polymer film. The TiO2 layer deposited on the exposed regions act as an extremely effective etch barrier while unmasked polymer film is easily removed by the plasma to generate the desired relief patterns. A schematic representation of the process is shown in Figure 1 and examples of optical images of patterns obtained after completion of the oxygen plasma pattern transfer etch are presented in Figure 2. This TSI method offers the potential to overcome the problem of thin etch barrier thicknesses at feature edges encountered in other TSI methods (e.g. digital silylation) which result from low silicon incorporation at the feature edge. These thin barrier thicknesses in silylation approaches are generally blamed for the large line edge roughness (LER) observed in such systems. In the ALD-based TSI approach presented here, the amount of etch barrier material incorporated into the film structure does not strictly depend on the total concentration of active sites generated in the exposed polymer volume as is the case with previous TSI approaches. The nucleation of the ALD film growth depends only on the presence of active sites on the polymer film surface, and thus the amount of ALD etch barrier deposited does not depend on the total hydroxyl concentration in the volume of the polymer film but instead depends on the number of ALD growth cycles performed. Contrast curves showing etch barrier thickness versus exposure dose, which is analogous to Si incorporation versus exposure dose curves obtained in conventional TSI methods, will be presented which show the chemical contrast advantages of this new technique. Chemical contrast curves for the new ASALDT-TSI imaging approach demonstrate highly non-linear behavior that offers the promise of solving unacceptable LER problem encountered from previous TSI approaches. Examples of high resolution patterning using this new method will also be presented.

6519-58, Session 11

Novel photodefinable low-k dielectric polymers based on polybenzoxazines

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As the feature sizes in microelectronic devices continue to diminish and as devices continue to operate at higher frequencies, there continues to be a growing need for lower dielectric constant insulator materials that can be used in both device fabrication and packaging applications. Insulating polymers with low dielectric constants (low-k), such as polyimides, are certainly one important class of materials used today in both device fabrication and packaging. However, essentially all current polymer dielectrics used in microelectronics processing suffer from one or more problems that limit their utility including: (1) requiring high temperature processing (e.g. \> 300 ºC for polyimides made from poly(amic acid) precursor films), (2) possessing large coefficients of thermal expansion (CTE) that cause stress build-up during temperature cycling in device manufacturing and operation, (3) requiring separate lithographic patterning and etching to form patterned polymer layers, and (4) exhibiting undesirable water absorption or other physiochemical properties due to modifications made to the material so that they are solution processable and in some cases directly photodefinable. In particular, the ability to develop photosensitive dielectric polymer formulations that can be directly lithographically patterned substantially reduces the cost and complexity of integrating such materials. Therefore, photodefinable dielectric polymers are significantly more attractive than non-photosensitive materials that require the use of separate resist patterning and etching processes. The goal of the work described in this paper has been the development of novel low-k polymers (k<3) based on polybenzoxazine chemistries that are directly photo-definable and which overcome many of the various problems associated with current dielectric polymers.

Polybenzoxazoles have received significant attention in the microelectronics industry as a photosensitive dielectric and alternative to polyimide materials [1, 2]. Polybenzoxazoles form rings from the dehydration of an alcohol situated ortho to an amide on a phenyl ring. However, formation of the polybenoxazole ring requires relatively high temperatures (350 oC). In searching for alternative polymers that can be formulated into photosensitive compositions and which offer low dielectric constants, excellent thermal stability, and relatively low processing temperatures, a method for producing a new class of polymers referred to here as polybenzoxazines was developed. The term polybenzoxazine is traditionally used to refer to a class of thermosetting polymer resins where the actual polymer itself is the product of benzoxazine polymerizing via a thermally induced ring-opening reaction to form a phenolic-like structure via a Mannich base bridge. These polymers are not the material of interest in this work. Instead, polybenzoxazine in this work is used to refer to polymers that contain a benzoxazine ring directly in the polymer backbone. In a manner similar to that of polybenzoxazoles, the benzoxazine rings in the polymer backbone described in this work are formed by the dehydration of a hexafluoroalcohol (HFA) situated ortho to an amide on a phenyl ring.

In this paper, the use of a combination of a novel HFA-substituted diamine monomer with various acid chloride monomers to synthesize novel thermoplastic polybenzoxazine amide alcohol precursor polymers is reported. Dehydration of the hexafluoroisopropanol situated ortho to the amide on the phenyl ring in the polymer backbone forms the six membered benzoxazine ring structure rather than the five membered ring seen in polybenzoxazoles. The synthetic route used to make these precursor polymers and the resulting ring closed polymer is shown in Figure 1. The polybenzoxazine amide alcohol precursor polymers have exhibited good solubility in a variety of different solvents including methanol, THF, PGMEA, GBL, DMF and have also shown solubility in 0.26 N TMAH. This permits the simple preparation of formulations of these polymers that can be spin coated.

Of this general class of new polybenzoxazine amide alcohol precursor polymers, it will be shown that selected polymers exhibit good solubility in developer solutions and can be formulated into photosensitive compositions by addition of a DNQ inhibitor. Examples of high resolution lithographic patterning of these materials will be shown. In

contrast to polybenzoxazoles which are known to cyclize at temperatures well above 280 oC, the new polymers reported here can be cyclized at temperatures as low as 210 oC. This substantially lower thermal cyclization temperature significantly reduces problems such as thermal stress build-up during curing and also allows these materials to be used in conjunction with a wider variety of materials that can not survive the significantly higher processing temperature required with polyimides and polybenzoxazoles.

6519-59, Session 11

Patterning of biomolecules on a biocompatible nonchemically amplified resist

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Patterning of biologically active molecules such as DNA, proteins, cells, and spores on solid substrates are of great interest for their applications in biosensors, biomaterials, and tissue engineering. Spatial organization of biomolecules could be achieved through several techniques such as conventional photolithography and soft lithography. These techniques, however, have several drawbacks due to the use of toxic organic developers in the conventional photolithography and the limited size of poly(dimethyl siloxane) stamps in soft lithography. Also, photoacid generators are required for most of the commonly used chemically amplified resists (CARs), which are undesirable for the patterning of biomolecules. Recently, an alternative method of using CAR which does not require the development step was developed for patterning of cells. However, this resist material requires photoacid generator for the pattern generation, which makes the material and process not suitable for tissue engineering.

We report a simple lithographic process for the cell patterning in conjunction with a novel nonchemically amplified resist (NCAR) material. The major advantage of this process is that it does not require the addition of photoacid generator to generate patterns and thereby making the material and the process highly suitable for the immobilization of biomolecules and cells. Furthermore, the patterned resists can be used directly for the coupling of specific cell-adhesion peptides or proteins for the alignment of cells and therefore no further process of development is required after UV light exposure. Another unique feature of this process is that, unlike the CAR approach, no post-exposure bake step is required to create patterns.

The polymers used in this study have diazoketo functional groups that upon irradiation of UV light generate carboxylic groups. This chemistry has been utilized to create alternative hydrophilic/hydrophobic regions on a NCAR film. For cell patterning, a simple lithographic process (Figure 1) has been used which involves three steps; forming a thin film of the NCAR, UV light irradiation, and cell culture on the patterned substrate. Briefly, the NCAR was coated on a glass slide from a solution of the resist material in cyclohexanone and soft-baked to remove the solvent. UV light was then irradiated on selected regions to create patterns. The substrate was then subsequently placed in the cell culture medium for cell patterning. Mouse fibroblast cells were found to be preferentially aligned and proliferated on the UV light exposed regions of the NCAR film, where carboxylic groups were present. Also, this simple process has been successfully extended to the immobilization of amine modified DNA molecules on the UV light exposed regions.

6519-60, Session 12

Resist evaluation for EUV application at ASET

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Although EUV lithography has been prepared for next generation litho-technique for several years, it has lots of obstacles yet. Especially, phase defect from the mask, and immaturity in the resist should be solved as soon as possible because they are directly related to realizing patterns on the wafer. ASET has been focusing on these two problems, the mask defect control and the resist screening for EUV. In this study, we concentrate on the resist evaluation for the EUV lithography application, mainly commercial CAR (Chemically-Amplified Resist) type resist, for example, ArF resist and KrF resist.

We screened tens of resists in viewpoint of resolution, photo-speed, LWR (Line Width Roughness) and Outgassing. We used two METs (Micro-Exposure Tools), that is, HiNA in ASET and MET in Lawrence Berkeley National Lab. (LBNL) for exposure, and we used masks fabricated by DNP and ASET.

Some resist showed modulation on the wafer for 28nm-hp line and space pattern and some resist showed very high photo-speed about 5mJ/cm2. Photo-speed could be improved about 25% by controlling the amount of additives, PAG and quencher. However, the improvement in photo-speed caused the degradation in resolution, which means there is a trade-off relation between resolution and photo-speed. We tested about the effect of the molecular mass distribution (MMD) to the resolution of resist. We found out that MMD does not affect the resolution if the resolving ability of resist is no so good. And we evaluated newly-synthesized resist, which showed new possibility for EUV resist. And several experiment results lead to changing our strategy on the EUV resist development. And we encountered an unexpected problem, pattern lifting, which was solved by using bufferlayer to improve attachment between resist and wafer surface. We conclude that 40nm node devices are possible to be fabricated from the present status of resist.

The EUVL masks were fabricated by Dai Nippon Printing Co., Ltd. The HiNA set-3 projection optics were developed and provided by Nikon Corporation. This work was supported by NEDO.

6519-61, Session 12

Molecular glass photoresists containing photo-acid generator functionality: a route to a true single-molecule photoresist

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Molecular glass photoresists are a promising alternative to polymeric photoresists for use as imaging materials with improved resolution and line edge roughness for next generation lithography (NGL) including extreme ultraviolet lithography (EUVL). The types of chemically amplified resists (CARs) based on molecular glasses reported thus far have been blended materials in which a separate photoacid generator (PAG) has been formulated with an organic molecular glass compound to produce the CAR. As with traditional polymeric CARs that utilize blends including a separate PAG, the PAG in these materials can be distributed in an inhomogeneous manner in the film (e.g. due to microphase separation or tendencies of some PAGs to avoid the resist-air or resist-substrate interfaces). Such inhomogeneous distribution can only degrade the imaging performance of such materials. Also, the LER data available on blended molecular glass resists does not show as dramatic a decrease in LER as one might expect. It is hypothesized that to achieve higher resolutions and lower line edge roughness (LER) in CAR systems, even in molecular glass CARs, the diffusion length of the photoacid must be reduced. However, such reduction in photoacid diffusivity causes a decrease in the sensitivity of the resist. Significantly reduced resist sensitivity is a serious problem for future NGL methods, and thus the sensitivity of the photoresist must be maintained by means such as increasing the concentration of PAG in the resist. However, PAGs in blended polymeric and molecular glass resists typically exhibit low solubilities, thus limiting the maximum PAG concentration that can be achieved in such systems. In order to utilize the potential advantages of molecular glasses, produce photoacids with reduced diffusivities to increase resolution and lower LER, prevent inhomogeneous distribution of resist components, and provide a means to increase the concentration of PAG in the resist to maintain high sensitivity, the work reported in this paper has focused on the development of a new class of chemically amplified molecular glass resists that are composed of a single molecule which contains all of the different functionalities desired in a CAR. In other words, the molecular glass compound contains (1) a photoacid generating group, (2) protected hydroxyl or carboxylic acid sites, and (3) etch resistant structures. A progress report on this new family of imaging materials will be provided including synthetic procedures, physiochemical property characterization of the molecular glass compounds, lithography performance for both electron beam, 193nm, and EUVL,

and etch resistance data. For example, a series of single molecule chemically amplified molecular glass resists for use in EUV and e-beam lithography were synthesized and characterized based on a triphenyl sulfonium photoacid generator core. Tris(4-hydroxy-3,5-dimethylphenyl)sulfonium chloride was synthesized by Friedel-Crafts acylation of 2,6-dimethyl phenol to provide the first initial building block for these resists. Protection of the phenolic hydroxyl sites on the compound using standard chemistries such as t-boc provided the first PAG-core molecular glass resist. Various different negative counter-ions were exchanged for the chloride using metathesis procedures to produce materials which generate a variety of different photoacids of different strengths and molecular sizes. The imaging performance of this family of compounds will be discussed as one example of this general new class of photoresist materials.

6519-62, Session 12

The resist materials study for outgassing reduction and LWR improvement in EUV lithography

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EUV lithography is the one of the candidate for half-pitch 32 nm generation device manufacturing and beyond. In case of EUV lithography, it is necessary to reduce the outgassing segments from the resist during EUV exposure to avoid optics contamination. The other key issue is line width roughness (LWR) where this parameter has a trade-off relationship with both sensitivity and resolution. Our resist materials study has been focused on these four key items; outgassing reduction, sensitivity, resolution, and LWR improvement.

Our resist materials are based on acetal type chemically amplified resist performing a good EUV sensitivity and maintaining a fine resolution capability. To reduce the outgassing, we have introduced bulky acetal protection group into polymer backbone. The most of the outgassing study have been carried out at University Wisconsin using thermal adsorption GC-MS method. It was suggested that the major part of outgassing segments in our EUV resist was generated from sulfonium type the photo acid generator (PAG) during EUV irradiation. Total outgassing value from the resist was decreased into the rage of to 1 - 9 x 1012 molecules/cm2 by modifying cation group of the sulfonium salt. We are updating further outgassing study in this presentation.

In terms of sensitivity improvement, our bulky acetal chemistry has an advantage because the large size protection group can minimize protection ratio of the polyhydroxystyrene (PHS) type polymer, which enable to cleave the protection groups with the relatively low amount of the acid. That could be enhanced the deprotection efficiency of acetal group to obtain a certain dissolution rate contrast of the resist matrix. However, this is the trade-off relationship with both resolution and LWR.

A resolution capability study was demonstrated with micro exposure tool (MET). The resolution capability of newly developed EUV resist has been successfully improved by modifying resist polymer matrix. Here, the low molecular weight polymer would be one of the key to achieve 30 –35 nm resolution.

In case of LWR, AFM study told us that the surface roughness at the half exposed area was well correlated with LWR which was exposed with E-beam writer. Some of the polymer could minimize the surface roughness at half exposed area compared with our conventional type resist. By changing polymer, LWR value at 35 nm lines were measured using MET exposed 4 inch wafer. LWR value at 35 nm was 4.86 nm. Further LWR improvement is necessary for future usage.

6519-63, Session 12

An analysis of EUV-resist outgassing measurements

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Optics contamination is of great concern for EUV lithography. In efforts to protect EUV optics, all materials used in EUV vacuum exposure chambers must be screened prior to use. Photoresists are a concern since in a high volume production tool a freshly coated wafer will be introduced into the chamber approximately every minute. SEMATECH and the International EUV Initiative (IEUVI) have been working together on the outgassing specification limit for resist and on defining a common methodology for testing resists. The group also initiated a resist outgassing roundrobin test to measure samples of the same model resist. Eight different institutions participated in the testing. Samples of the same model resist was sent to all participants to measure the resist outgassing on their tools. The results show variation in the amounts of outgassing due to different methodologies and techniques used by the researchers.

The paper will discuss two methods used to collect and detect outgassing components: in situ analysis using quadrupole mass spectroscopy (QMS) and ex situ analysis using thermal desoprtion tubes for gas chromatography and mass spectroscopy analysis (GC/MS). The GC/MS method easily identifies the outgassing components, but it depends on the asorber material and cannot identify species with molecular weights less than 35 atomic mass units (AMU). QMS is useful because it can be placed in the vacuum chamber near the resist sample, but it is difficult to quantify the amount of outgassing because of the different ionization efficiencies of the species. The advantages and disadvantages of these systems will be compared.

This paper will present detailed outgassing results and suggestions for developing a common methodology for resist outgassing measurements.

6519-17, Poster Session

Development of top coat materials for ArF immersion lithography

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193-nm immersion lithography is considered as the most promising technology which is used in mass production of semiconductor devices down to the 45nm node. In recent years, this technology has progressed significantly. Last year the fundamental optical performances of lithography were confirmed experimentally by using a trial production machine.

In immersion lithography, the space between the lens and the wafer is filled with water. The impact of water on resist performance and the possibility of damage to the lens by the components eluted from the resist material are seriously concern. To prevent penetrating of water into resist material or leaching of resist components into water, the use of top-coat seemed to be useful and admissible method. Developer-soluble topcoats have been investigated as suitable candidates for its applicability to the resist developing process.

The major challenge in development of top coat material is how to avoid the water mark defect, which is immersion specific and most critical. It is considered that water droplet left on the topcoat or resist film after scanning exposure cause water mark defects as one of mechanism for that. Recently , it has been reported that there are some correlations between dynamic contact angle, sliding angle or receding angle, of water on the topcoat surface with water mark defect and scan speed of immersion exposure tool. That is, when the topcoat has high hydrophobicity, the number of water mark defect tend to be small and the topcoat surface shows resistance to high scan speed of immersion exposure tool. Furthermore, the tolerance to more than 400nm/sec scan speed would be strongly desired in the future. So, development of materials which have high hydrophobicity have been required.

We have investigated higher hydrophobic developer-soluble topcoat by combination of developer- soluble unit with higher hydrophobic unit. We have already reported a series of fluoropolymers, FUGU having acidic acidic hydroxyl group which act as dissolution unit into alkaline solution.[1] In addition, recently we have developed new series of highly fluorinated monomers which is expected to act as hydophobic unit.[2] We co-polymerized FUGU with these hydophobic monomers and evaluated them. Some of them showed good hydrophobicity keeping moderate developer solubility. However the hydrophobicity and developer-solubility are trade off, and there seems to be a limitaition to this approach.

As a result of further examination by different approach, we suceeded in breaking through this trade-off which we met at first approach. We found that higher hydrophobic developer-soluble materials were achieved by adding small amount of highly hydrophobic polymer to developer- soluble polymer, for example FUGU and in fact this type of blending polymer showed high hydrophobicity keepng high dissolution. We consider that highly fluorinated hydrophobic unit is easy to come up to the surface of topcoat and act as if barrier of topcoat. On the other hand, this topcoat becomes to be soluble into alkaline solution because developer- soluble unit lies just below this hydrophobic surface. We have obtained various kind of new type of topcoat materials whose receding angle varied from 70~100 degree. Evaluation results and properties of these materials will be presented.

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6519-64, Poster Session

Dynamic contact angles of polymer films: detailed structure/property relationships

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Surface properties of materials are an important, even vital, consideration in immersion lithography. Many investigations have shown that simple concepts in surface polarity are not entirely useful in design of high performance surfaces for immersion lithography. We have built and characterized a broad family of “hydrophobic” materials for immersion lithography. This paper will share information on the role of molecular structure on the dynamic contact angles and hysteresis of these immersion materials. A more sophisticated concept of proper design of materials for future immersion surfaces will be presented.

6519-66, Poster Session

High-refractive index fluids for second-generation 193-nm immersion lithography

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The first generation 193-nm immersion lithography with de-ionised water (D.I. water) as the immersion fluid is now placed on the major technology to produce 45-nm node semiconductor devices. D.I. water has refractive index of 1.44 and absorption coefficient equal to 0.05/cm, and can enable stepper numerical apertures (NA) over 1.3. Recently, some novel higher refractive index fluids have been reported and the evaluations of them have been discussed. These second-generation immersion fluids that have refractive indices over 1.6 would be able to achieve the NA 1.5 and the L/S patterning under 40-nm.

We have reported two fluids, ‘Delphi’ and ‘Babylon’, which have high refractive indices (1.63 and 1.64, respectively) and low absorption coefficients (0.08/cm and 0.05/cm, respectively) enough for second-generation immersion fluid. In fact, we demonstrated hp 32-nm L/S patterning using 193-nm two-beam interferometric exposure tool with ‘Delphi’ and ‘Babylon’.

In this paper, we will discuss the other properties of our immersion fluids, such as the durability for laser exposure, the interaction with other materials used for lithography and so on. These results indicate that ‘Delphi’ and ‘Babylon’ were feasible for second-generation 193-nm immersion lithography.

6519-67, Poster Session

Mechanism of immersion specific defects with high receding-angle topcoat

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ArF immersion lithography is the most advanced technology for the future device fabrication. Last year, several device makers have already started manufacturing devices experimentally using this technology1-2). Over the past several years, some issues regarding this technique, e.g. construction of the exposure tool and the of resist components into the immersion medium, has been actively discussed and improved all over the world. These devices were made using topcoat. Because it was difficult to make a photoresist which satisfied both of the prevention of elution and the high receding contact angle (RCA). Topcoat is an effective technology to relax these requirements of the photoresist. In the first stage of device fabrication with immersion lithography, topcoat will be used. In terms of this material, RCA was increased in order to prevent the defect formation by water droplet left behind after a high speed scan condition of immersion projection lens unit3). Immersion-specific defects were reduced by this approach3). However, we observed the case contrary to commonly accepted theory. When we inspected for defects by using 2 types of topcoat materials that have high RCA, one of them hardly generated any defect, whereas the other showed high defect counts. The latter topcoat showed many circular and oval shaped defects even though the RCA of the topcoat was high at 80 degrees. Moreover, we found imperfect circular and oval shaped defect in the adjacent region of each defect as shown in figure1. These types of defects would be typical characteristic in the case of the immersion water containing bubbles. In order to confirm the generation mechanism of these defects, we hypothesized that the generation of these defects depends on the dynamic contact angle and the chemical composition of the topcoat surface in the water. The high-RCA topcoat would be the trend that the water mark defects reduced but the bubble defects increase. And the surface chemical composition would be induced hydrophobicity change of the topcoat surface. At first, we measured the dynamic contact angles of the topcoat materials. A developer-soluble topcoat on methacrylate type ArF resists was used in our examination. The dynamic contact angles were measured by contact angle meter. The amount of water absorption of the topcoat film with the method of reflectmetry of polarized lights4) (Model RM-8000, Microtec Co., Ltd.) were measured. We examined pattern defect inspection with immersion scanner (S609B and EET-scanner, Nikon). The results from the experiments will be discussed in detail during the presentation.

6519-68, Poster Session

Defectivity reduction studies for ArF immersion lithography

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The use of 193 nm immersion lithography is considering a solution for future device nodes. One of the most important issues of immersion lithography is pattern defect control. Two years ago, authors evaluated the impact of water droplets on dry exposed resist films and top coat. From this study found that when water droplets dried and shrunk in size, the internal pressure became larger than the threshold for penetration of water into the film [1].

Post immersion rinse (PIR) is expected to reduce water marks by removing water droplets before drying on the immersion exposed wafer. In this study, authors tested the effect of PIR sequence as a function of shower head movement (SHM) and cover material coating type. Two types of cover materials were investigated solvent soluble type and developer soluble type.

Then we evaluated the PIR sequence on solvent soluble and developer soluble cover materials.

Figure shows the results of the particle test on wafer surface. We confirmed that defects were decreased on both films by using PIR sequence,

But we thought that the effectiveness of PIR sequence depends on the kind of cover materials.

Then we tried the inspection of pattern defects to clarify its dependence.

Authors will discuss the relationship between cover materials type and the PIR sequence as it relates to defect reduction.

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6519-69, Poster Session

Adjustment of surface property for immersion defect reduction at 65-nm node and beyond

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193nm immersion lithography has been verified that can be put into production in next node. According to the previous publications, the major challenge for immersion lithography is to reduce defectivity , which is totally different with that of dry lithography. Immersion defects, including bubbles, watermarks, micro-bridges and etc., has to reduce before applying into real production.

In this paper, 300mm wafers that were exposed on an ASML 1400i immersion scanner with a TEL Lithius track, using a resist system with a protecting developer-soluble top-coat. The key strategy for immersion defect reduction is to change the surface properties of litho materials such as contact angle, sliding angle, receding angle and etc., in which hydrophobicity of the topcoat surface have strong correlation with the immersion specific defect counts.

Finally, by changing the surface properties of the materials with adding pre-treatment step into 65nm litho processes, the immersion-induced defects are greatly reduced. In conclusion, this process can be used both at our current 65nm litho process node and beyond.

6519-70, Poster Session

Study on the reduction of defects in immersion lithography

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ArF Immersion lithography is expected to be a production-worthy technology for sub-60nm DRAM. It gives wider process window and better CD uniformity at the cost of defects and overlay accuracy. It is generally mentioned that immersion defects are generated during exposure and removed through pre-soak and post-soak process. A lot of efforts are being made towards less defect generation during exposure and more defect removal through pre-soak and post-soak process.

We have experienced a variety of immersion defects and classified them into four types: bridge defect, bubble defect, water mark defect (T-top & stain) and swelling defect. We have worked very hard to reduce each of immersion defects with 1400i and 1700i exposure system. In this paper, we investigate method to reduce each of immersion defects: bridge, bubble, water mark swelling, through our experiment.

6519-71, Poster Session

Modified polymer architecture for immersion lithography

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In the past several years, ArF immersion lithography has been developed rapidly for practical applications. ArF immersion lithography is now researched actively and developed for the purpose of implementing the 45-nm technology node. For the device designs involved immersion lithography, line with roughness (LWR) and film wettability are very important criteria to control in the point of high resolution and defectivity.

In this study, resist polymers with low polydispersity (PD) and controlled molecular structure are prepared using controlled radical polymerization techniques, such as reversible addition-fragmentation chain transfer (RAFT) polymerization. PD index of polymers showed between about 1.2 to 1.4 and in some instances, between about 1.1 to 1.2 or less.

Additionally, each polymer chains have a RAFT end group. That is, the resulting polymer contains a chain transfer agent (CTA) moiety at each terminal end of polymer backbone. It is possible that hydrophobic CTAs can be used to decrease the hydrophilicity of resist film surface in order to make immersion defect-free resists. The immersion litho evaluation results of this system will be discussed in this report.

6519-72, Poster Session

Tailoring surface properties of ArF resists thin films with functionally graded materials (FGM)

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Immersion photolithography at 193 nm for the manufacture of integrated circuits with feature size of 65 nm and 45 nm presents a great challenge. Of primary concern in immersion lithography is the understanding of the photoresist surface-liquid interface. Use of the newest generation of thin film photoresists presents a number of materials problems, including the diffusion of water into the resist film and the reaching of resist components into the immersion medium. Much effort has been made to develop the top coat that provides to serve as good protector from leaching of the resist components (PAGs, bases) into the water. However, the application of top coats may lead to complicated processes and increase the total amount of defects on the wafer. The immersion resists which are designed for use without top coatings would be a preferable solution.

Our recent research effort has been focused on new top coating-free 193nm immersion resists with regard to leaching of the resist components and lithographic performance. We have examined methacrylate-based resins that control the surface properties of ArF resists thin films by surface segregation behavior.

Surface segregation behavior and functionally gradient material (FGM) are found in polymer blends. In polymer blends, surface segregation (FGM) occurs as low surface tensions of component is preferentially enriched on the surface of samples according differences between surface tensions of components. It is thought that the appearance of surface segregation (FGM) is affected by miscibility, surface tension, density, the rate of solvent casting.

Jablonski reported that polymer blend constituents having different hydrophobicity or surface tension, the more hydrophobic or lower surface tension, the more hydrophobic or lower surface tension species would typically wet the blend film surface when heated in air. Irie reported that fluorine localized at the surface for the blended polymer, in contrast to the uniform distribution for the fluorine-incorporated polymer. The addition of the fluorine material is advantageous for altering the surface

For a better understanding of the surface properties of thin films, we have prepared the three resins (Resin A, Resin B and Resin C) that have three types fluorine containing monomers, Monomer A, Monomer B and Monomer C, respectively.

We have blended the conventional resin with Resin A, Resin B and Resin C, respectively. We evaluated contact angles and lithographic performances of the polymer blend resists. The receding contact angle of the resist that contains Resin A or Resin B is greater than that of conventional resists to go up to 70°. The lithographic performance of the resist that contains Resin C is better than that of the resist that contains Resin A or Resin B. The chemical composition of the surface of blend polymers was investigated with XPS. It was shown that there was significant segregation of the fluorine containing resins to the surface of the blend films.

In this paper we will discuss the new design for methacrylic polymer blends, material properties, resist characteristics, lithographic performance.

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6519-77, Poster Session

Transfer mechanism of defects on cover material to resist pattern in immersion lithography process and effects on etching process

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With the scaling down of the semiconductor design rule, 193-nm lithography technology is entering the 65-nm-node generation. In 65-nm and finer processes, the practical application of 193-nm immersion lithography is progressing due to its high numerical aperture (NA), which is achieved by using de-ionized water (DIW) as the medium between the lens and wafer in the exposure system. Immersion lithography, however, generates two main concerns: the penetration of moisture into resist film and the leaching of resist components into DIW as a result of immersing the resist film in DIW.

To prevent these effects from happening, the use of a cover material process has been adopted, but there have been reports that defects caused by remaining droplets on the cover material or particles can be transferred to the resist pattern and degrade resolution. Research to date has clarified the generation mechanism of defects due to water droplets, and the importance of preventing droplets from remaining is now understood. There are few research reports, however, on the generation of particles, and to reduce defects caused by the immersion process, it is essential that the mechanism behind the generation of particle-related defects on the resist pattern be clarified, and the approach on the reduce particles is needed. It is also known that particles on a resist that acts as a mask in the dry etching process can be associated with defects in etching, which makes particle control in the process steps between lithography and dry etching all the more important.

In this paper, we clarify the defect-generation mechanism on resist pattern due to particles attached on cover material and investigate the effects of such particles on the dry etching process. We also report on the defect-reduction effect achieved by removing particles from the cover material.

6519-78, Poster Session

Models for predicting the index of refraction of compounds at 193 nm

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As the semiconductor industry continues to follow Moore's Law, the demand to print smaller features continues. First generation immersion 193 nm lithography is showing improved resolution with water as the immersion liquid, allowing the NA to increase as high as 1.3.1 More recently, higher index fluids have been developed and are showing an increase in index of refraction to 1.65 (vs. water at 1.43 at 193 nm).2

Vogel and coworkers3 and more recently,4 others have developed a method for calculating molar refraction (R) using a group additivity method,4-6 when Mw and density are known. Ultimately, however, we decided not to use this method as it is difficult to calculate the density of a compound accurately enough to be useful here. More recently, quantum chemical methods have also been used to calculate index of refraction, but these methods are not readily accessable.7,8

Here, we used literature values of refractive indices (D-line 589 nm) of compounds with representative functionalities (hydrocarbons, linear compounds, cyclic compounds, sulfides, sulfoxides, sulfones, alcohols, ethers, etc.) to build an empirical model with 18 adjustable parameters. The resulting model fit the 56 points with an average accuracy of 99.6% and an R2 of 0.987 (Figure 1A).

Predicting the refractive index at 193 nm (n193) for our target molecules is much more difficult than accurately calculating the refractive index for new molecules at the D-line (nD) because only a handful of data points are available and we need to extrapolate from relatively low values of n193 to ~1.85. We evaluated published data from NIST9 and RIT10 (Table I and Figure 1B). The compounds evaluated by NIST are largely organic and the fluids studied by Bruce Smith of RIT are highly ionic aqueous solutions of salts and acids. These two sets of data have widely different slopes. While the NIST data suggest that the D-line refractive indices (nD) will need to be ~1.66 before the n193 will be 1.85, the RIT correlation is much more optimistic and predicts that nD will only need to be ~1.54 in order for the n193 to be 1.85.

6519-80, Poster Session

Outlook for potential third-generation immersion fluids

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The imminent implementation of immersion tools in the microchip production process, confirms that immersion microlithography will likely be the predominant technique for use in the microelectronic industry in the following years. In these first stages, water will be used as the basis of the immersion fluid. However, higher refractive index fluids are desired in order to obtain the maximum potential of the technique. Several groups have successfully developed second generation fluids over the past few years 1, 2, 3. Our research group has put great effort into the development of water-based second generation fluids with a refractive index above 1.6 at 193 nm. Fundamental studies of nanoparticle dispersions and crown ether-based fluids have been investigated and high refractive indices were successfully obtained. Nevertheless, high scattering in the case of the nanoparticles and high absorption (low transparency at 193 nm) in the case of crown ethers limited the use of these fluids. In terms of transparency, alkanes are known to have a low absorption in the UV range. In addition, the refractive index of the liquid alkanes varies from 1.35 to 1.53 at 589 nm. In our studies we found a linear correlation between the density and the refractive index of these types of compounds. Taking into consideration the structure of the alkanes, cyclic alkanes tend to have a higher density, and therefore, a higher refractive index. We have investigated polycycloalkanes, and in particular perhydropyrene with a refractive index of ?1.72 at 193 nm, as potential third generation fluids for immersion microlithography. Addition of solid and highly dense cycloalkanes, such as adamantane, to the perhydropyrene will likely push up in a substantial manner the refractive index of the final fluid, reaching the desired value of 1.8-1.9.

The reversible formation of a complex between the alkanes and molecular oxygen has been found as the major contribution to the absorption in the UV region. Degassing of the solutions to avoid the formation of those reversible complexes dramatically decreases the absorption to give values close to those desired at 193 nm. The presence of oxygen during exposure represents an additional problem because of the oxidation of the fluid and formation of highly absorbing photoproducts. A one step synthesis of perhydropyrene and a simple method for the purification of polycycloalkanes are presented in this work.

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6519-82, Poster Session

Behavior and effects of water penetration in 193-nm immersion lithography process materials

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The development of next-generation exposure equipment in the field of lithography is now underway as the demand increases for faster and more highly integrated semiconductor devices. At the same time, proposals are being made for lithography processes that can achieve finer pattern dimensions while using existing state-of-the-art ArF exposure equipment.

Immersion exposure technology can use a high-refraction lens by filling the space between the exposed substrate and the projections lens of the exposure equipment with a liquid having a high refractive index. At present, the development of 193-nm immersion exposure technology is proceeding at a rapid pace and approaching the realm of mass production.

However, the immersion of resist film in de-ionized water in 193-nm immersion exposure technology raises several concerns, the most worrisome being the penetration of moisture into the resist film, the leaching of resist components into the water, and the formation of residual moisture affecting post-processing. To mitigate the effects of directly immersing a resist in de-ionized water, the adoption of a protective film is considered to be beneficial, but the possibility is high that the same concerns will rise even with protective film.

It has been reported that immersion-specific defects in 193-nm immersion exposure lithography include “slimming,” “large bridge,” “swell,” “micro-bridge,” and “line pitch expansion,” while defects generated by dry lithography can be summarized as “residue,” “substrate induced,” “discoloration,” and “pattern collapse.” Nevertheless, there are still many unexplained areas on the adverse effects of water seeping into protective film or resist. It is vitally important that the mechanisms behind this water penetration be understood to reduce the occurrence of these immersion-induced defects.

In this paper, we use protective films and resist materials used in immersion lithography to analyze the penetration and diffusion of water. It is found that the water-blocking performance of protective-film materials used in immersion lithography may not be sufficient at the molecular level. We discuss the diffusion of water in protective film and its effects.

6519-83, Poster Session

Process optimization for developer soluble immersion topcoat material

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In the current immersion lithography, the use of topcoat material has been recommended. This topcoat material has successfully maximized scan speed during immersion exposure step and also prevented small molecules in the resist film from leaching [1], which resulted in turning immersion lithography into reality furthermore. On the other hand, a process with the use of the topcoat material has an impact on productivity such as throughput and the cost for chemicals, because of the increase in number of process and chemicals. Currently, topcoat material has been classified broadly into two types; “developer soluble type” and “solvent soluble type”, and the former type is becoming the favored topcoat material because it doesn’t require removal process with special chemicals, which means it has more advantages in the productivity than the latter one.

However, as far as we recognized, the amount of the topcoat to be consumed per 300mm wafer in the coating process using developer-soluble topcoat material is approximately 3.0ml to 4.0ml, which is more than tripled the average ArF resist consumption. That is, compared with dry exposure lithography, a further impact besides the increase in number of chemicals, from the viewpoint of the cost for chemicals.

To solve this issue, we commenced consideration for reduction in the cost for chemicals regarding developer-soluble topcoat material. As one motif of developer soluble topcoat material, we used TCX-041 from JSR Corporation, which is widely used in the field of current immersion lithography development to reduce the consumption of topcoat material in coating process from both the material and process sides. As a result, we succeeded in achieving the definite effects.

In this paper, the effects of reducing the consumption of topcoat material, which we achieved from our efforts, are reported. In addition, the possibility of reduction in the cost for chemicals in immersion lithography is referred, with showing the data regarding basic performance such as the surface state and leaching level of the film coated with a small amount of topcoat.

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6519-84, Poster Session

Defect transfer from immersion exposure process to post processing and defect reduction using novel immersion track system

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As a promising candidate for a lithography technology than can support the scaling down of semiconductor devices, 193-nm immersion exposure is being developed at a rapid pace and entering a stage applicable to mass production. This technology can raise the numerical aperture (NA) of the exposure equipment by filling the space between the projection lens and silicon wafer with a fluid (de-ionized water). At the same time, direct contact between the resist film and water creates a number of process risks. There are still many unclear areas and many problems to be solved with regard to defects that raise concern in 193-nm immersion lithography.

The use of de-ionized water during the exposure process in 193-nm immersion lithography technology can lead to a variety of problems. For example, the trapping of micro air bubbles can degrade resolution, and residual water droplets left on the wafer surface after immersion exposure can affect resolution in the regions under those droplets. It has also been reported that the immersion of resist film in de-ionized water during exposure can cause moisture to penetrate the resist film and resist components to dissolve in the water, and that immersion can effect critical dimensions (CD) in addition to generating defects (Fig.1) [1]. The use of a protective film here is viewed as one possible way of preventing adverse effects from the immersion of resist in water, but it has been reported that the same kinds of problems may occur even with a protective film and that other problems may be generated such as the creation of development residues due to the mixing of protective film and resist. To make 193-nm immersion lithography technology practical for mass production, it is essential that the above defect problems be solved. Importance must be attached to understanding the conditions that give rise to residual defects and their transference in the steps between lithography and the etching/washing processes.

In this paper, we use 193-nm immersion lithography equipment to examine the transference (traceability) of defects that appear in actual device manufacturing (Fig.1). It will be shown that defect transfer to the etching process can be significantly reduced by the appropriate use of defect-reduction techniques.

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6519-85, Poster Session

Effect of polymer sensitivity on immersion defectivity

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ArF immersion lithography is the most promising technology for 45nm node and possibly beyond. However, the serious issues in ArF immersion lithography for semiconductor mass production still exist. One of the main issues is immersion-specific defects, which are caused by photoresist component leaching and residual water droplets. In this paper, we investigated leaching value of PAG anion from varying the activation energy of protecting groups. Also we will discuss the influence of various activation energy of protecting groups and watermark defect by water droplet present on the resist film during PEB process.

6519-86, Poster Session

Using a DOE to reduce immersion lithography related defects

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This paper discusses the optimization of process conditions on an immersion lithography cluster tool to minimize defects. A 45nm gate

process and a 100nm contact-hole process were selected for optimization. Previous testing has shown defect counts and density are sensitive to rinsing of wafers before and after exposure. This sensitivity was dependent on the topcoat contact angle and resist-plus-topcoat porosity. This paper expands on that study in 3 ways. (1) Examining individual process steps within the pre- and post-exposure rinse processes as well as the develop process. (2) The sensitivity to delays, coat to pre-rinse, pre-rinse to exposure, exposure to post-rinse, and post rinse to develop are tested. (3) Bake time and temperature were also added to the testing to determine if the impact to the film composition would influence the number of defects. The paper focuses on the defects specific to the immersion process and distinguishes between wet versus dry type defects. Each variable was tested over a range of conditions to identify its effect on defectivity without adversely affecting CD uniformity and process performance. The largest contributors were then tested using a DOE to find the ideal condition for each resist type.

6519-87, Poster Session

Formulated surface conditioners in 50-nm immersion lithography: simultaneously reducing pattern collapse and line-width roughness

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With the introduction of immersion lithography into IC manufacturing for 45nm node, pattern collapse and line width roughness (LWR) have become critical challenges. To address these challenges, we have implemented formulated surface conditioners which are capable of solving multiple issues and easily integrated into the post-develop photolithography process.

In this paper, we assessed the impact and reported our findings using a formulated surface conditioning solution in an immersion lithography process to improve pattern collapse and LWR process windows on 300mm Si wafers having 50 nm L/S features. The non-pattern collapse and LWR process window results were then compared to wafers processed using traditional developer processing methods, a DI Water (DIW) rinse.

We report our findings using Focus Exposure Matrix (FEM) wafers having 50nm dense lines/spaces (L/S) and a 3:1 aspect ratio to determine the non-collapse and LWR process windows. An ASML XT:1700i(tm) Scanner and a 6%attPSM mask were used to pattern the FEM and LWR wafers. The wafers were then developed using an optimized developer recipe on an RF3i(tm) coater-developer track. Each wafer was analyzed and evaluated to determine and report the impact to non-pattern collapse and LWR.

Formulated surface conditioners having dual capabilities, reduced pattern collapse and LWR improvement, have demonstrated multiple ITRS Roadmap goals can be achieved and easily implemented into standard IC processing in order to meet these challenges.

6519-89, Poster Session

BARC (bottom anti-reflective coating) for immersion process

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193nm immersion Lithography will be installed at 45nm and beyond. For severe CD control, BARC (Bottom Anti-reflective Coating) have been used and this material must be used for immersion lithography.

So far, we have developed several BARCs with various advantages (fast etch rate, broad resist compatibility, high adhesion, conformal...etc). Especially in immersion process, development of BARC has to satisfy these two issues (Optical control & Defectivity) for the following reasons.

The reflectivity control at Hyper NA is not same as the lower NA, because optical pass length in the BARC is not same between at low NA and at High NA. In order to achieve the enough etch selectivity to substrate, the hard mask materials are necessary. These under layers have absorption at 193nm. As a result of simulation, target optical parameter of next BARC should be low k value (k = ~0.25) at multi BARC stack.

On the other hand, the defect issue must tend to decrease in immersion process. However, the generation of many kinds of defects is suspected in immersion process (water mark, PDD, sublimation defect...etc). Regarding the BARC, there are also several specific defects in this process. Especially, after edge shot, film peering at edge area is one of the concerns during edge shot. We researched edge peeling source and solution of this defect.

In this paper, we will discuss the detail of our BARC approach (litho performance, optical parameter, leaching, sublimation, edge peel defects and etch selectivity) and introduce new BARC for 193nm immersion lithography.

6519-90, Poster Session

Organic ArF bottom antireflective coatings for immersion lithography

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Substrate reflectivity control plays an important role in immersion lithography. Multi-layer bottom anti-reflective coatings (B.A.R.C.s) become necessary. This paper will focus on the recent development in organic ArF B.A.R.C. for immersion lithography. Single layer low k ArF B.A.R.C.s in conjuction with multilayer CVD hard mask and dual layer organic ArF B.A.R.C. application will be discussed. High NA dry and wet lithography data will be presented. We will also present the etch rate data, defect data and out-gassing property of these new B.A.R.C. materials.

6519-91, Poster Session

Multilayer BARCs for hyper-NA immersion lithography process

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Organic Bottom Anti-Reflective Coatings (BARCs) has been used in the lithography process. BARCs may play an important role to control reflections and improve swing ratios, CD variations, reflective notching, and standing waves.

In 45nm and 32nm node, application of the immersion lithography technique is not avoided to obtain the high resolution. To obtain the high resolution, numerical aperture (NA) of the optical system needs the Hyper-NA lens of 1.0 or more but come up to the problem of affections the polarized light in the Hyper-NA lens. The substrate of reflection control also will become more difficult by using single BARCs system and the thin film resist becomes the necessity and indispensable at Hyper-NA lithography. To achieve an appropriate reflection control, to suppress the CD difference to the minimum, and to prevent the pattern collapse, hard mask with the spin coating film and antireflection characteristic is needed. In order to solve these issues, we designed and developed new materials with the suitable optical parameter, square resist shape and large dry etching selectivity. These Multi-layer materials of each process are spin-coated by existing coater/track system and conventional ArF photo resist or immersion resist is available in this process.

This paper presents the detail of our new materials for Hyper NA lithography.

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6519-92, Poster Session

Process evaluation and metrology verification for next-generation immersion process

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In order to prepare for the next generation technology manufacturing, ASML and TEL are investigating the process performance of the Lithiusi+/ TWINSCAN XT:1700i lithocluster through decreasing critical dimension patterning. Process performance with regards to critical dimension uniformity and defectivity are compared at different critical dimensions in order to determine areas of concentration for equipment and process development. Specifically, defect types will be classified to generate a pareto for each technology node to see if there is any change in the defect types as critical dimensions are shrinking. Similarly, critical dimension uniformity will be compared through technology nodes to see if any budget contributions have increased sensitivities to the smaller patterning features.

6519-93, Poster Session

Novel polymeric anionic photo-acid generators (PAGs) and photoresists

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There is a rapidly approaching roadblock of critical importance in semiconductor processing technology, namely the development of advanced tools and photoresist materials for the patterning of sub-45 nm transistor features in advanced logic and memory devices. In fact, significant progress has been made in developing exposure tools. On the other hand, development of new photoresist materials that can be used with these new short wavelength exposure tools is essential. In general, a chemically amplified resists consisting of a polymer matrix with plasma etch resistance capability, is mixed with a small molecular photoacid generator (PAG) that provides the ability to produce a relief pattern in the CA resist thin film via radiation exposure. The inherent incompatibility between polymer matrix and the photoacid generator leads to problems including PAG phase separation, non-uniform initial PAG and photoacid distribution, as well as acid migration during the post-exposure baking (PEB) processes. To alleviate these problems, several systems with ionic or non-ionic PAG incorporated in the main chain have been studied recently. The incorporation of ionic PAG units into the main chain of the hydroxystyrene and adamantyl methacrylate based polymers showed improved EUV lithographic performance, such as faster photospeed and higher stability, lower outgassing, and lower line edge roughness (LER) than corresponding blend resists. Here we report novel bound and blend anionic PAGs and a series of new photoresists incorporating PAG in the main chain. The design of microstructure was based on a methacrylate polymer backbone due to minimal 193 nm absorbance: * -butyrolactone methacrylate (GBLMA) was included in the microstructure to improve adhesion, 2-ethyl-2-adamantyl-methacrylate (EAMA) was incorporated as the acid-cleavable bulky alicyclic substituent groups to improve resolution, sensitivity, and dry etch resistance. Polymeric and monomeric PAGs with or without fluorine were synthesized, and correspondingly, PAG bound polymers, PAG blend polymers were also prepared, characterized by NMR, elemental analysis, GPC, TGA and DSC, as well as exposed at 193 nm for imaging evaluations.

These novel materials provide optical transparency at 193 nm and also etch resistance. The thermostability of nonfluorine PAG bound or blend polymers were superior to that of the fluorine-substituted PAG bound or blend polymers. PAG incorporated resists, and PAG blended resists were exposed at a wavelength of 193 nm, ASML 5500/950B optical lithography system with 0.63 NA, and evaluated using SEM. The fluorine substituted PAG bound polymer and PAG blend polymer provided 110 nm (220 nm pitch) line/spaces at 11.5 mJ/cm2, 13 mJ/cm2, and 80 nm isolated features at 3 mJ/cm2, 1 mJ/cm2, respectively, which showed faster photospeed and good lithographic performance. The fluorine-free PAG bound or blend resists showed lower photospeed compared to photoresists based on fluorine substituted PAGs. Positive sub-100 nm patterns were obtained for these systems. Although the photosensitivity of the PAG blend polymer is higher than that of PAG bound polymer, yet it is anticipated that PAG incorporated into the polymer main chain may control acid diffusion compared with the PAG blend polymers. AFM images showed top and side profiles and surface and sidewell roughness of the resist patterns roughness were obtained. LER measurements will be provided.

6519-95, Poster Session

Ionic photoacid generators (PAGs) and base incorporated into main-chain of polymers for sub-50-nm patterning by EUVL

M. Wang, The Univ. of North Carolina at Charlotte; W. Yueh, J. M. Roberts, Intel Corp.; K. E. Gonsalves, The Univ. of North Carolina at Charlotte

As the semiconductor industry moves to the 32 nm node, it becomes apparent that new lithography technology will be needed. One possibility for fabricating this feature size is extreme ultraviolet (EUV) technology. New high performance resist materials will need to be developed with the advent of EUV. The sensitivity of a resist must be approximately 10 mJ/cm2 or less, and patterned features must exhibit a line edge roughness of less than 2 nm[1]. Conventional chemically amplified photoresist formulations are complex mixtures of a protected polymer matrix and a small molecule photoacid generator (PAG). The inherent incompatibility can lead to PAG phase separation, non-uniform initial PAG and photoacid distribution, as well as acid migration during the post-exposure baking (PEB) processes[2]. To alleviate these problems, several systems with ionic or non-ionic PAG incorporated in the main chain have been studied[3-5]. The incorporation of ionic PAG units into the main chain of the hydroxystyrene and adamantyl methacrylate based polymers showed improved EUV lithographic performance, such as faster photospeed and higher stability, lower outgassing, and lower line edge roughness (LER) than corresponding blend resists, base quencher was added to the formulation to control the acid diffusion and improve the line edge roughness further [5]. Here we report new polymers incorporating both PAG and base in the main chain, and PAG blend polymers. They were prepared in moderate to good yield and characterized by NMR, elemental analysis, GPC, TGA and DSC.

We investigated different PAGs (including ion PAG, anionic fluorinated and fluorine-free PAGs) and three organic bases (1-vinyl-2-pyrrolidinone, 1-vinylimidazole, 4-vinylpyridine) incorporated into the polymer main-chain. Firstly, we prepared the terpolymers composed of hydroxystyrene, adamantyl methacrylate and base, and then blend anionic fluorinated PAG to make resists, and carried out their initial imaging evaluation exposed at 254 nm UV. The results showed that the 1-vinyl-2-pyrrolidinone based terpolymer had better performance than the other two bases. We fixed the base, 1-vinyl-2-pyrrolidinone incorporated into the polymer, and changed the PAG type as well as the feed ratio to prepare a series of different composition to investigate the effect of PAG and base on the imaging performance. The PAG/Base molar ratio should be approximately 2~5. Electron beam lithography and LER will be provided

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6519-96, Poster Session

Development of nanocomposite resists with high plasma etch resistance

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Plasma etching is one of the critical process steps in manufacturing structures for micro-electronics. During the etching process, a patterned photoresist layer is the preferred etch barrier. Due to the often insufficient etch resistance of conventional resist material, the resist layer must remain thick enough to stand up a large variety of different etchants without becoming so thin that pinholes are present. One way to overcome this limitation is to develop new resist materials having high etch resistance.

We report about the development of novel nanocomposite resists that incorporate colloidal silica nanoparticles into conventional resist materials to yield thick film materials with both excellent lithographic properties and significantly increased plasma etch resistance. 10-50 wt% silica nanoparticles of 10-15 nm in size were dispersed homogeneously in a variety of standard resist resins by a simple process. The nanocomposite resists have the similar lithographic performance to the conventional resists without silica nanoparticles. The nanocomposite resists also show excellent process window capability and stability. Oxygen plasma etch and reactive ion etching (RIE) processes were used to evaluate the etch resistance of the nanocomposite resists. Compared with standard photoresists, the oxygen plasma etch rate is reduced by 38-90% when the silica content increases from 20 to 50 wt%. The etch selectivity of nanocomposite resists with 40 wt% silica is increased by 70% in deep RIE etching test

6519-97, Poster Session

Chemical composition distribution analysis of photoresist copolymers and influence on ArF lithographic performance

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Recently it is more important to develop novel photoresist polymers applicable to miniaturization of semiconductor circuit pattern. It is well known that high performance polymers is raised up by using of a novel monomer and optimizing popular factors such as molecular weight (Mw), molecular weight distribution and chemical composition ratio. But for achieving higher performance polymers, it is necessary to control more finely molecular structure of the polymers. There is an example report in which sensitivity was improved by optimizing of the end group structures of the polymer. [1]

We have focused “distribution” of polymer chemical composition ratio instead of “average composition” commonly being used in discussions on polymer designing, since it is now difficult to make up higher performance polymers by the common “average composition” discussion. Critical adsorption point-liquid chromatography (CAP-LC) method developed by Gorshokov et al [2], [3], was taken to measure the “distribution” and we acquired necessary knowledge from it.

The CAP condition can be acquired by choosing appropriate eluents and proper stationary phase. In this condition, we found that LC peaks of polymers, which have similar kind but different Mw, appeared at the same elution time. By this way, we could get useful “distribution” information of chemical composition without influence of Mw.

We could confirm that model copolymers prepared by different polymerization conditions had different “distribution” by measurement of CAP-LC in their chemical compositions. Moreover we would like to discuss the effect of different “distribution” to lithography performance such as sensitivity, gamma value and dissolution rate, and so on.

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6519-98, Poster Session

Development of single component chemically amplified resist based on dehalogenation of polymer

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In the fabrication beyond 32 nm node, the uniform distribution of acid generators in resist matrix is a serious concern. The incorporation of acid generators to polymers has attracted much attention in order to prevent the compatibility problem of acid generators with polymers. The simplest way to efficiently generate acids by ionizing radiation is the halogenation of polymers. In the previous studies, we made clear the reaction mechanisms of chemically amplified resists, in particular, halogenated polymers. In this study, we designed a single component chemically amplified resist based on the reaction mechanisms of chemically amplified resists.

Partially protected Br-PHS was used as a polymer matrix. Triphenylsulfonium-triflate (TPS-tf) was used as an acid generator. Propylene glycol monomethyl ether acetate (PGMEA) was used as a casting solvent. The wafers were primed with hexamethyldisilizane (HMDS). Resist solutions with and without acid and amine were spin-coated onto silicon substrates at 3000 rpm for 30 s to form thin films. The resist samples were exposed to 75 kV electron beam after baked at 110.0 °C for 90 s. Water-soluble conducting polymer (Showa Denko, Espacer) was also spin-coated at 2000 rpm for 60 s before exposure. After the exposure, they were baked in the temperature range of 60-130 °C for 60 s. They were immersion-developed in 0.13 N tetramethylammonium hydroxide (TMAH) solutions for 30s and rinsed in water before drying. Resist patterns were recorded with a JEOL JSM-6335F SEM.

The developed resist showed an excellent performance. With a semi-isolated condition, 50 nm lines were successfully formed without the addition of any additive such as a base quencher. When a base quencher was added into the resist, line & space patterns with 150 nm pitch and 200 nm pitch were obtained. Although the sensitivity was degraded with amine addition, 150 nm pitch patterns were delineated. We demonstrated the design of a single component chemically amplified resist for ionizing radiation, based on the reaction mechanisms which are different from those of photoresists.

6519-99, Poster Session

Novel 193-nm positive photoresist composed of ester acetal polymer without phenyl group

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An aliphatic divinyl ether compound can be prepared by the reaction of acrylpimaric acid and chloroethyl vinyl ether. Further reaction of the aliphatic divinyl ether and acrylpimaric acid give rise to a novel ester acetal polymer without phenyl group which shown good transparency at 193nm. The ester acetal polymers can be quickly decomposed at the presence of strong acid generated by PAG above 100oC and become easily soluble in dilute aqueous base. Two-component photopolymer consisting of the ester acetal polymer and PAG can be used as 193nm positive photoresists.

6519-100, Poster Session

Two-component photoresists based on acidolytic cleavage of novel ester acetal polymer

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The reaction of acrylpimaric acid and several divinyl ether compounds, including 1,3-divinyloxyethoxybenzene, 2,2-bis(4-[2-(vinyloxy)ethoxy]phenyl)propane, and 1,4-divinyloxyethoxybenzene, can take place in the presence of organic solvents to form novel ester acetal polymer. The polarity of solvents and reaction temperature have much

effects on the reaction. The ester acetal polymers can be quickly acidolyzed at the presence of strong acid generated by PAG above 100oC and become easily soluble in dilute aqueous base. Two-component positive photoresists can be formed by the ester acetal polymer and PAG and displayed excellent lithographic performance as deep UV resist .

6519-101, Poster Session

Nonchemically amplified resists for deep-UV lithography

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Chemically amplified resists utilizing acid-catalyzed reactions have been widely used as photoresists to achieve practical throughput. Despite of their high photosensitivity, chemically amplified resists suffer from serious problems such as the appearance of an anomalous insoluble skin layer and line-width shift caused by the air-borne contamination and the acid diffusion in the resist films when the post-exposure bake is delayed. These post-exposure delay problems make it difficult to fabricate fine patterns. Moreover, the photoacid generators are used almost exclusively in their monomeric forms and have limited compatibility with the polymeric photoresist material. The resulting problems include phase separation and non-uniform acid diffusion and thereby limiting the resolution. Furthermore, most of the commonly used photoacid generators contain aromatic rings in their structure and possess potential environmental hazards.

Nonchemically amplified resists have a greater potential to suppress the post-exposure delay problems, as they are not susceptible to air-borne contamination and acid diffusion. We designed and synthesized a novel diazoketo-functionalized methacrylate monomer that has cholate moiety in its structure. The cholate derivatives are particularly interested due to their excellent film formablility, transparency in DUV region, and high CF4 plasma etch resistance due to the alicyclic moieties present in its structure.

Cholic acid 3-diazo-3-ethoxycarbonyl-2-oxo-propyl ester methacrylate (CDEOPE-MA) was synthesized from Cholic acid 3-diazo-3-ethoxycarbonyl-2-oxo-propyl ester and methacryloyl chloride as shown in Scheme 1. After workup, the crude monomer was purified by column chromatography to yield 47% of CDEOPE-MA. Copolymers of CDEOPE-MA, methyl methacrylate, and γ-butyrolacton-2-yl methacrylate were synthesized by free radical polymerization. The number average molecular weight of the polymers was in the range of 8,400-13,200 g.mol-1 and the polydispersities were in the range of 2.0-2.6. The polymerization yields were 63-71 %. Weight loss of the polymers began above 100 °C. The degree of photobleaching of the polymers at 248 nm and 193 nm wavelengths were calculated from the UV absorbance spectra of the polymers before and after UV light irradiation. The polymers showed high degree of photobleaching at 248 nm and moderate degree of photobleaching at 193 nm. The initital lithographic evaluation showed the feasibility of the polymers to be used as candidates for deep UV lithography.

6519-102, Poster Session

EUV printing of contact holes for the sub-40-nm node

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Contact holes are one of the most challenging and critical layers in the DRAM manufacturing process. The first sub-40nm node will most likely require contact holes with dimensions in the sub-60nm range.

Therefore recent EUV resist screenings at one of the available EUV micro-exposure tools (ALS/Berkeley) have been extended to expose arrays of dense and semi-dense contacts with a size of 60nm and below. Besides the comparison of state-of-the-art EUV resists for contact hole printing, focus exposure matrix (FEM) data for dense and semi-dense contact holes are analyzed.

Since Line Edge Roughness (LER) is recognized as one of lithography's difficult challenges for sub-40nm nodes, an appropriate determination of LER is used to characterize the roughness behaviour of contact holes over exposure dose and focus.

Experimentally attained printing results of contact holes and simulation data are discussed in terms of today's EUV resist performance vs. ITRS roadmap requirements.

6519-103, Poster Session

Non-ionic photoacid generators for chemically amplified resists: evaluation results on the application-relevant properties

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The shrinking of device geometries for higher performance and higher memory capacity has been achieved by the development of lithography technology. For the leading-edge lithography for the fabrication of semi-conductor devices, KrF excimer-laser (248 nm) and ArF excimer-laser (193 nm) have been employed as the light source and chemically amplified (CA) resist technology has been introduced. In the CA resist technology photoacid generator (PAG) is one of the key ingredients for making desirable resist patterns. Several PAGs have been applied for CA resists, e.g., iodonium sulfonate, sulfonium sulfonate, diazomethanedisulfone, N-hydroxyimido sulfonate, nitrobenzyl sulfonate, and so on. However, there is still needs for new PAGs, which improve photospeed, thermal stability, storage stability, resolution, resist profile and/or process latitude. Especially for ArF CA resist, PAGs releasing a strong acid are required but there are few PAGs available. In addition, as an immersion technology has drawn keen attention for the next generation lithography, it is demanded to develop new PAGs compatible with immersion lithography.

We recently reported new non-ionic PAGs, 2-[2,2,3,3,4,4,5,5-octafluoro-1-(nonafluorobutylsulfonyloxyimino)-pentyl]-fluorene (ONPF) and its derivatives, which can generate strong acid by light irradiation. A series of ONPF analogues have been synthesized and the application-relevant properties, such as precise evaluation of leachate under immersion process, photospeed study with electron beam exposure tool, outgassing investigation and so on, are presented in this paper.

6519-104, Poster Session

PAG distribution and acid thermal diffusion study in ultra-thick chemically amplified resist films

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Ultra thick resist films near 100 to 150 um thickness range are gradually receiving increased demand in packaging and other resist applications. Some dry film applications are being replaced with wet ultra thick resists driven by the need to print more challenging pitch / resolution at high aspect ratios. Ultra thick resists based on conventional novolak and diazonaphthoquinone (DNQ) chemistry require high exposure doses, long development times and produce sloped profiles. This is generally attributed to their thick film absorption and their limited novolak dissolution rates. Chemically amplified (CA) technology based resists can provide significant advantages over conventional DNQ because of their high speed, fast development and steep profiles. However, the large majority of thick film positive i-g-line/broad band resist products are DNQ based.

Some efforts by resist manufacturers are directed to i-line CA thick resist development. Although CA technology has been applied widely in DUV (248nm) and 193nm, it has only been applied to relatively thin film applications, much less than 10um in thickness. Thick films introduce new challenges that were not experienced in thin film resist development. Some of these challenges are addressed in this study.

Two significant performance differences between thin and thick film resist applications discussed in this paper are: 1) the influence of residual solvent on PAG/acid diffusion and the de-blocking of the polymer, and 2) the influence of Cu substrates, frequently used in thick film applications, on PAG distribution and side wall profile compared to Si substrates.

The significant reduction in post exposure bake (PEB) temperatures

observed in thick film CA resists, compared to thin films, required to de-block the polymer, is attributed to the high solvent retention in thick films. High solvent contents in thick films is expected to enhance acid mobility, thermal diffusion range and accelerating the kinetics of the system. This has been observed with both high as well as low activation energy blocking groups such, as t-butyl esters and acetals, respectively. High activation energy resist systems require PEB temperatures above 120oC, up to 140oC for 1um resist films. Similar polymers used in thick film resist, greater than 10um in thickness, can be de-blocked efficiently below 100oC.

Dramatic changes in resist side wall profiles and footing are observed only on Cu substrates that can be correlated with PAG structures. All formulations are based on styrene/hydroxystyrene/t-butylacrylate polymer system. The observed results suggest variations in PAG distribution in thick resist films applied on Cu wafers and more uniform PAG distributions on Si substrates.

Examples of 10um thick resist profiles using different PAG structures on Cu substrates

A series of different structure PAGs examined in this study is discussed in details. Highly fluorinated PAGs produced undercut profiles, while PAGs containing low or no fluorine produced more pronounced foot. Blends of PAGs varying in their total fluorine contents produced proportional changes in resist profiles on Cu. This trend is consistent with PAG attraction or repulsion mechanism by the Cu substrate.

6519-105, Poster Session

Study of 193-nm resist degradation mechanisms under various etch chemistries

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The effectivity of 193nm photoresists as dry etch mask is becoming more and more critical as the size of integrated devices shrinks. 193nm resists are known to be much less resistant to dry etching than 248nm resists based on poly(hydroxystyrene) polymer backbone. The decrease in the resist film budget implies a better etch resistance to use single layer 193nm photoresists for the 65nm node and beyond. In spite of significant improvements made in the past decade regarding the etch resistance of photoresists, much of the fundamental chemistry and physics that could explain the behaviour of these materials has to be better understood. Such knowledge is necessary in order to propose materials and etch processes for the next technology nodes (45nm and below).

In this paper, we report our studies of the etch behaviour of different 193nm resist materials as a function of etch chemistry and etch time. In a first step, we focus our attention on the interactions between photoresists and the reactive species of a plasma during a dry etch step. Etch experiments were carried out in a DPS high density chamber. The gas chemistry in particular was changed to check the role of the plasma reactive species on the resist. O2, Cl2, CF4, HBr and Ar gas were used.

Etch rates and chemical modifications of different materials after etch were quantified by ellipsometry, Fourier Transformed Infrared Spectroscopy (FTIR), Thermo Gravimetric Analysis (TGA), Atomic Force Microscopy (AFM) and X-Ray Photoelectrons Spectroscopy (XPS). We evaluated different materials including 248nm resists and model polymer backbones (pure PHS or functionalized PHS), and 193nm model polymers (PMMA and acrylate polymers) or resist formulations. Besides the influence of resist chemistry, the influence of plasma parameters was addressed. The influence of etch time on the resist behaviour is also discussed.

6519-106, Poster Session

Development of high-performance multilayer resist process with hardening treatment

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Hyper NA ArF immersion lithography is one of the most promising technologies for the manufacturing of devices 45nm node and beyond. Developments of the novel resist system, which enables to reduce reflectivity in hyper NA region and also to transfer narrow pattern with thin imaging layer below 150nm have been required. Track compatible multi-layer resist (MLR) system consists of silicon containing ARC (Si-ARC) and spin on carbon (SOC) is one of the candidates [1], however, the etching durability of conventional MLRs are inferior to amorphous carbon hard mask (HM) by a chemical vapor deposition (CVD).

In this study, we have developed the hardening process of SOC by H2 plasma treatment to improve the etching durability of MLR. H2 plasma hardened SOC film showed drastic improvement in dry etching durability, wiggling features of MLR without H2 treatment observed after SiO2 etching totally disappeared (Fig.1). The hardening mechanism of SOC was analyzed by FT-IR with gradient shaving preparation (GSP) and Raman spectrometry. Formation of diamond like amorphous carbon about 50nm depth was observed [2] and assigned to the improvement in dry etching durability.

Simulated reflectivity at the interface between resist bottom and top surface of MLR stack with hardening are shown in Fig.2 as a function of the thickness of Si-ARC layer and numerical aperture (NA) of exposure tool. Reflectivity below 0.6% was attained with very wide ranges of Si-ARC thickness and NA. Measured refractive indices of hardened SOC film at 193nm gradually decreased from the surface to inner region and finally became the same value as the untreated SOC. This might be origin of estimated excellent reflectivity characteristics.

Lithographic performances of MLR stack with H2 plasma hardening , such as exposure latitude, depth of focus and the resist profile, will be presented in this paper.

6519-107, Poster Session

Correlation between etching and optical properties of organic films for multi-layer resist

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With interconnect scaling towards the hp 45 nm, the precise control of the critical dimension (CD) in 140-nm pitch interconnects is becoming more important. Multi-layer resist processes, such as using a tri-layer resist consisting of a top imaging resist layer, an intermediate spin-on-glass layer, and a bottom spin-on organic layer, are useful for increasing initial resist thickness to etch porous SiOC film. The problem is that the etching CD of the bottom layer is controlled by the etching conditions as well as being affected by the properties of the organic film under a given constant etching condition.

We have identified a correlation between the amount and rate of etching and various properties of organic film. In our experiment, we prepared six organic films that had different densities, hardness values, reflective indexes, and FT-IR peaks and exposed their patterned samples using electron projection lithography.

Our results showed that the amount of side etching of the bottom layer for the patterned samples depended on the etching rate of the organic films. The etching rate did not depend on density; it depended on hardness and the refractive index. The etching rate decreased with increasing hardness. It is possible that there is a correlation between hardness and the bonding energy in the organic films. The etching rate decreased with increasing refractive index in the visible wavelength spectrum (400-700 nm). Organic film has a high refractive index because it has many high-energy bonds, such as phenyl, C=O, and C-O. We found that the refractive index showed the etching characteristics of the bottom organic layer. Consequently, the etching CD of porous SiOC can be better controlled by using an organic film with appropriate properties as the photoresist.

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6519-108, Poster Session

Rework/stripping of multilayer materials for FEOL and BEOL integration using single wafer tool techniques

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As feature sizes continue to the 45nm and 32nm nodes, significant challenges will continue to arise in both front-end-of-line (FEOL) and back-end-of-line (BEOL) applications. The reduced thickness, as well as the reduced etch resistance, of the photoresist (PR) makes it nearly impossible to use the PR as both an imaging and a pattern transfer layer. This etch challenge has led device manufacturers and vendors to explore the use of multi-layer (tri-layer) stacks. Multi-layer stacks are typically comprised of a thick via-filling organic layer that will provide adequate etch resistance while etching into low-k and ultra-low-k dielectrics. A silicon-containing layer is then applied on top of the via-filling layer, which will provide imaging as well as etch resistance for the organic layer. The PR is then applied on top to complete the multi-layer stack. While many challenges present themselves in multi-layer stacks, new challenges such as rework and cleaning have arisen. As low-k and ultra-low-k dielectrics become more prevalent, traditional ashing processes for the removal of photoresist and anti-reflective coatings can cause damage to the dielectric layer due to their chemical and physical structure. While some processes have been developed to replace lost organic material during ashing and etching through silyation, alternate processes are being developed where entirely wet stripping processes can remove multi-layer stacks. One advantage of an entirely wet removal process is it can prevent damage caused by ashing or etching, and the wet stripper is developed so it does not attack the dielectric films. While an entirely wet removal process has potential advantages, it still must be proven that these processes can remove residues that are left after etch processes, sufficient removal of particles are obtained, and any material loss of the dielectric layer meets the requirements of the customer and the International Technology Roadmap for Semiconductors. Other challenges are presenting themselves as many customers would like to move from batch-type wet rework or cleaning processes to single wafer tool processes.

It is the intent of this paper to not only identify new wet cleaning materials that can be used to remove multi-layer materials by means of an entirely wet process, but also to find single wafer tool processes that produce fewer particles (defects) and cause no dielectric material loss.

6519-109, Poster Session

Spin-on organic hardmask materials in 70-nm devices

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In ArF lithography for < 90nm L/S, it seems that ACL (amorphous carbon layer) deposition becomes inevitable way because thin ArF resist itself can not provide suitable etch selectivity to sub-layers. Recently, in order to transfer image properly, ACL should be used as a hardmask, as ArF resist is used as a first imaging layer.

In ACL deposition, surface particles originated from ACL deposition are found frequently, which are problematic in mass production. Limited capacity, high cost of ownership and low process efficiency of ACL deposition also become a dilemma which can not be ignored by device makers. One of the answers to these problems is using a spin-on organic hardmask material instead of ACL deposition.

In this paper, we have developed spin-on organic hardmask materials applicable to 70nm memory devices. Applications to three different stacked processes were investigated in terms of photo property, etch property and process compatibility.

- 3 layer process (ArF PR/Si ARC/Spin-on Organic Hardmask/Substrate)

- 4 layer process (ArF PR/BARC/Si ARC/Spin-on Organic Hardmask/Substrate)

- gap fill process (ArF PR/BARC/LTO/Spin-on Organic Hardmask/Substrate)

Based on the test results described in this paper, our spin-on hardmask materials are expected to advance towards commercialization.

6519-110, Poster Session

Materials for and performance of multilayer lithography schemes

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The 45-nm node will require the use of either 193-nm multilayer scheme lithography or immersion lithography. Immersion lithography is a complex process that needs multiple reflection control layers and extremely thin resists. The use of multilayer lithography provides solutions for these issues through a minimum of a carbon-rich pattern transfer and anti-reflective layer (spin-on carbon, or SOC) and a silicon-rich anti-reflective hardmask (Si-ARC). These layers provide a high degree of reflectivity control over a variety of substrates under traditional and hyper-NA lithographic conditions. The combination of the two layers also provides a highly planarized substrate for an ultrathin resist, and provides a route to etch substrates due to the alternating nature of the organic resist, inorganic Si-ARC, and organic SOC. Furthermore, the integrity of the films when fully cured allows for the resist only to be reworked by solvent wash without any detrimental effect on lithographic performance or increase in defect levels, thus saving rework process time and reapplication of materials.

The selection of our scheme based on optical constants and the thicknesses of materials and their performance will be discussed. Lithographic performance, etch integration and capabilities, and resist rework process will also be discussed.

6519-111, Poster Session

Advanced developer-soluble gap-fill materials and applications

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In the advanced integration of semiconductor devices, the dual damascene process of creating copper interconnects is an important revolution for the back-end. Traditional lithography processes utilizing photoresists and anti-reflective coatings cannot meet the requirement of small feature size integration structure. Gap-fill materials can play a key role in the planarization of high aspect ratio vias or trenches, which helps to ensure a lithography process that results in the best profiles and critical dimension control. A thick layer of gap-fill material is coated on a high aspect ratio substrate in order to cover topography and achieve low thickness bias between dense and isolated feature areas. This step is often followed by plasma etching to remove extra gap-fill material above the substrate surface, leaving only filled vias. The plasma etch step is expensive and also is a potential source of defect generation.

Instead of using a plasma etch process, developer-soluble gap-fill materials can be etched back to the substrate surface by using a standard photoresist developer (tetramethylammonium hydroxide), which provides the advantages of reducing defects, eliminating plasma damage, simplifying the process, and decreasing the cost. By careful design of both the polymer and formulation, our developer-soluble gap-fill materials fill vias and trenches on different substrates without void formation. Also, these gap-fill materials do not exhibit swelling or peeling problems during the developer etch-back process. Dissolution rate is adjustable by customizing the material with regard to the chemical structure of the polymer and the formulation composition. The developer etch-back process can be finely controlled to achieve partial fill, full fill, or a thin layer remaining on the top surface. The bias between dense and isolated areas is significantly reduced due to the dissolution rate difference between the bulk material above the vias and the material inside of the vias. Heat transfer and other factors have been considered to explain chemical and physical changes of bulk and via materials.

Our developer-soluble gap-fill materials are spin bowl compatible. The film remaining after develop back is not soluble in solvents. The materials do not interact with BARCs or resists and are stable under BARC and resist process conditions. Both KrF and ArF lithography produce good profiles when the gap-fill materials are coated with BARC and resist.

Plasma etch property is an important process parameter in substrate printing process. Depending on substrate material, structure, and application, the required etch conditions and etch selectivity can be varied. In this paper, we report developer-soluble gap-fill materials with different etch properties, and we present etch rate data under different etch gases and etch conditions.

6519-112, Poster Session

Novel low-reflective index fluoropolymers-based top antireflective coatings (TARC) for 193-nm lithography

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Recently, implant lithography, typically having larger feature sizes which were printable with 248-nm light source in the previous node, now most require 193-nm lithography. In implant lithography, top anti reflective coatings (TARC) are commonly used to reduce CD swing. The TARC materials for used 193-nm were required more low reflective index and alternative of perfluorooctylsulfonic acid (PFOS) and perfluorooctylcalboxylic acid (PFOA). We synthesized some novel fluorinated polymers for application in 193-nm. Their fundamental properties were characterized, such as transparency at 193-nm (wavelength) and solubility in water and a standard alkaline developer. High transparency, i.e., absorbance better than 0.2 μm-1 at 193-nm wavelength, was achieved. The dissolution behaviors of them were studied by using the Quartz Crystal Microbalance (QCM) method. Several polymers dissolved in water and showed high transparency and a low refractive index by a wavelength of 193-nm. These results show that their polymers were able to apply to top anti reflective coatings (TARC). The dissolution rates of the fluoropolymers in water and a 0.262N can be controlled by optimizing counter monomers containing hexafluoroisopropanol (HFA) unit, carboxylic acid unit and so on.

6519-113, Poster Session

Effect of molecular weight and thermal cross-link rate on via filling performance in BARC and gap fill materials

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Innovative technologies are required by integrated circuit manufacturers to create smaller feature sizes on chips. According to the semiconductor roadmap, feature sizes are slated to be as small as 32 nm in 2008, sizes will be continued to decrease in the following years.

Conventional method of patterning trenches in a Via First Dual Damascene process involves filling the vias with a Dry Etch Organic gap filling materials and then applying the photoresist followed by trench lithography after coating Bottom Antireflective Coating (BARC). The biggest problem with this process is the huge fill bias observed as the via pitch and density changes across the wafer. This bias between isolated and dense via arrays is not acceptable and leads to narrow process windows and problems during subsequent trench etch processes.

It is common knowledge that the thicker you coat a gap fill material, the lower the fill bias between isolated and dense via structures. Therefore, this method of patterning trenches does show an advantage over the conventional method in terms of process latitude. The process mentioned above requires wafers, which are coated with gap fill material, to be transferred to the Etch/CMP tool for an etch back step and brought back to the photo area for BARC coating and trench lithography. This transfer process is cumbersome, reduces the wafer throughput and can also generate particles during wafer handling steps.

In this paper, the study of effect of molecular weight and thermal crosslink speed on via filling performance in BARC and gap fill materials was investigated. And,we will introduce the new BARC and gap fill material consisted of the polymers with self crosslink-reaction system. In addition of sublimate reduction data, resist profiles and 100nm via fill performance in via- first dual damascene process presented here would show clearly these materials are ready to be investigated into mass production of 45 nm node IC devices and beyond.

6519-114, Poster Session

Optimization of hardmask for dual-antireflection layers

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The continuous shrinkage of critical dimensions has driven ArF lithography to resolve very small features and ever thinner photoresist films to prevent pattern collapse and enlarge process margin. Hardmask process which is using extra layer for etching mask instead of photo resist is very effect to optimize lithography process with thin photoresist. This hardmask technology is becoming increasingly important as the demand for both the critical dimension control and sufficient thickness of etch mask needed.

We have developed a silicon based hardmask prepared by plasma-enhanced chemical vapor deposition (PECVD) process which gives very similar performance of reflection control as conventional organic anti-reflective coating (ARC) or dielectric ARC. On the other hand, conventional ARCs either organic or dielectric Conventional are very sensitivity to the substrate topology effect. In order to overcome this issue, we developed the Dual ARC (dielectric ARC + organic ARC) process which showed excellent performance of less CD variation than single ARC. In addition, this material can serve as an effective hardmask etch barrier during the plasma etch. The most advantage of Dual ARC is that we have good critical dimension uniformity (CDU) regardless of substrate thickness variation.

6519-115, Poster Session

Advances in developer-soluble antireflective coatings for 248-nm lithography

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A novel approach to developer-soluble bottom anti-reflective coatings (BARCs) for 248-nm lithography was demonstrated. The BARCs are photosensitive, dye-filled systems incorporated with a polymer binder. The films are generated by thermally crosslinking the polymer matrix, which are then photochemically decrosslinked. The BARCs are positive working in nature. The BARCs are compatible with solvents commonly used in the industry. Easy modification of the films with regard to optical properties for potential use with various substrates was also demonstrated. The BARCs exhibit anisotropic development in aqueous tetramethylammonium hydroxide (TMAH) subsequent to photoresist application, exposure and post-exposure bake. The lithographic performance of the new systems is compared to that of non-photosensitive developer-soluble BARCs.

6519-116, Poster Session

Optimization of material and process parameter for minimizing defect in implementation of MFHM process

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Silicon-containing material has recently attracted attention as new hard mask material. We have studied the applicability of MFHM (Multi-Functional Hard Mask, Si-ARC) / SOC (Spin on Carbon) materials as an alternative to the BARC/SiON/a-Carbon. We call Si-ARC as MFHM because Si-ARC material simultaneously has to have both anti-reflective property and pattern transfer property. SOC is the material of high carbon content. This process is very useful in terms of cost reduction and process simplicity compared to a-C process. Evaluation results have showed good lithographic and etch performances. However this MFHM process has showed material related specific defect. In this paper, we will introduce defect type and suggest its solution.

Conference 6519: Advances in Resist Materials and Processing Technology XXIV

6519-118, Poster Session

A novel 248-nm wet-developable BARC for trench applications

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As critical dimensions continue to shrink in lithography, new materials will be needed to meet the new demands imposed by this shrinkage. For example, new materials will be needed for implant applications. A wet-developable bottom anti-reflective coating (BARC) will be needed to maintain CD swing and improve reflectivity control. One of the major requirements of this material will be complete clear-out of trench structures. To meet these demands, a novel polyamic acid-based, 248-nm wet-developable BARC has been prepared. This material showed an excellent process window and controllable development rates. It is a highly absorbing BARC with n and k equal to 1.73 and 0.49, respectively. Lithography with this material has shown 180-nm dense profiles, and clear-out has been demonstrated for 120-nm trenches. In addition, spin-bowl compatibility, low residue, and low sublimation will be demonstrated.

6519-119, Poster Session

Wet recess gap-ill materials for an advanced dual-Damascene process

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Conventional method of patterning trenches in a Via First Dual Damascene process involves filling the vias with a BARC and then applying the photoresist followed by trench lithography. The biggest problem with this process is the huge fill bias observed as the via pitch and density changes across the wafer. This bias between isolated and dense via arrays is not acceptable and leads to narrow process windows and problems during subsequent trench etch processes. Another approach, currently being used, is to coat a thick layer of material (which does not need to have antireflective properties) but can fill vias. These via fill materials are often referred to as a gap fill materials. Gap fill materials are applied to the substrate and then recessed either by using dry etch process or CMP to the substrate. The substrate is then coated with a conventional BARC.

It is common knowledge that the thicker you coat a gap fill material, the lower the fill bias between isolated and dense via structures. The process mentioned above requires wafers, which are coated with gap fill material, to be transferred to the Etch/CMP tool for an etch back step and brought back to the photo area for BARC coating and trench lithography. This transfer process is cumbersome, reduces the wafer throughput and can also generate particles during wafer handling steps.

We released a novel approach of using a developer soluble gap fill materials before, wherein the gap fill material is coated thick enough to planarize all the topography and is then recessed (developed) using a standard 0.26N TMAH developer. Since the material recess process takes place in the same coater track, it simplifies the process and increases throughput. The wet recess materials that had been developed had not so good recess uniformity. We will discuss the performance and characterization of new wet recess gap fill materials which applies an original system. The new wet recess gap fill materials have good recess uniformity and wide process window compared with conventional materials.

6519-120, Poster Session

Spin-on organic hardmask for high-temperature application

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A new technology using amorphous carbon as a hard-mask is applied to real device production. However, amorphous carbon process has cost problem to extend its application more widely.

In this paper, we will introduce a noble material that substitutes amorphous carbon. This material has high thermal stability and low etch rate. Of course, SiON film can be deposited on this material. In addition, it is soluble to normal thinner so that EBR can be applied with normal thinner. Using this material as a etch barrier, we could get the 2,500 depth oxide contact hole of which diameter was 130nm.

6519-121, Poster Session

Low out-gassing KrF bottom antireflective coatings

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Out-gassing of bottom anti-reflective coatings (B.A.R.C.s) becomes a severe issue when more and more IC manufacturers move to 300mm track with high-precision hot plates. We have made significant progress in developing KrF B.A.R.C.s that are minimized in out-gassing. In this paper, several products will be discussed: one was aimed to match optical parameter of a typical KrF B.A.R.C.; one was designed for via filling application; and one was developed for special application on SiON/SiN substrate. We will compare the out-gassing of those new products with conventional KrF B.A.R.C.s and we will present the resist compatibility data and etch rate data as well.

6519-124, Poster Session

Novel approach of UV cross-link process to planarization for 32-45 nm advanced lithography

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Conventional method of patterning trenches in a VFTL(Via First Trench Last) Dual Damascene process involves filling the bias with a Dry Etch Organic Bottom Antireflective Coating (BARC) and then applying the photoresist followed by trench lithography. The major problem with this process is the huge bias (step height) observed as the Via pattern pitch and density changes across the wafer. The bias between isolated and dense Via arrays is not acceptable and leads to narrow process windows and problems during subsequent trench etch processes. Another approach, currently being used, is to coat a thick layer of material (which does not need to have antireflective properties) to reduce the bias between isolated Via and dense Via. However, too thick layer cause other difficulties during trench process.

Now, the new type of thin layer of material to reduce the bias is proposed. The material is referred to as UV Cross-Link Film(XUV).

The main properties of the UV Cross-Link Film are little thickness bias of isolated-Via and dense-Via pattern, void free, no intermixing with resist and BARC, and in particularly more effective barrier properties to reduce resist poisoning on a kind of Low-k materials by using the newest UV cross link process we studied in UV-Photo irradiation system.

The process for UV Cross-Link film is simple, just UV ray irradiate the film for a few seconds in same coater-developer tool. The planer property was related to some factors of materials at 23deg.C condition (liquid or solid phase), chemical interaction, Cross-Link reaction rate, UV shrinkage ratio, density, and polarity.

We propose a novel method, UV Cross-Link process to reduce the bias. And, we also study the films performance compared with the standard thermal Cross-link process using only hot plates.

6519-125, Poster Session

Overcome the challenge of CD-bias with organic bottom anti-reflective coating removal process

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Following the trend of critical dimensions (CD) shrinking image transfer process moved to deep UV illumination spectrum applications. As a result new deep UV-resists were developed to fit the demand of photolithography processing. But its sensitivity to under-layer material and parasitic reflection effect raised the necessity to apply new material

class - bottom anti-reflective coating (BARC). In its turn applied BARC caused the need to remove it in the opening of developed resist mask prior to the etching of the main material. Therefore process engineers incorporated BARC removal step before etching. This step may affect such important parameters of resist mask as profile and (CD) prior to etching of main material. Thus it is important to study BARC removal process and its impact on the final result to be able to control overall pattern transfer process.

This paper presents a review of two BARC removal processes incorporated into subhalf-micron contact etching. They are believed to represent different etching mechanisms. Accuracy of size feature transfer was taken as a primary criterion for comparison of different BARC removal processes. These processes are based on application of glow discharge in the following basic gas mixtures: CF4+O2 and CO+O2. The first process based on CF4+O2 gas mixture shows a behavior of neutral etching species model that cause a footing developing during BARC removal. Roughly this may be explained by the continuous direction spectrum of neutral active species movement. The access of active neutral species to the BARC layer is dependant upon the window mask size, resist profile and the thickness of resist layer. The second process based on CO+O2 gas mixture represents another etching mechanism - ion bombardment induced etching. On contrary to the previous partially isotropic process this one provides anisotropic etching. This is due to stimulating and activating the etching reaction by ion bombardment. Anisotropic features are achieved because of directional ion flux normally to wafer surface. This process is proved to be independent of profile and mask opening size features.

Data presented show that process based on CO+O2 gas mixture provides consistent close to zero CD bias at BARC removal step while CF4+O2 gas mixture based process causes negative CD bias with apparent dependence upon the window mask size.

Robust results of CO+O2 process allow one to consider it and its basic etching mechanism to be a mainstream of process development for different applications.

6519-126, Poster Session

Thin bilayer resists approach for 193 nm and future photolithography II

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Bilayer Si-containing resists are a technique of interest and a strong candidate to replace CVD hard mask processes for small critical dimensions(CDs). We proposed a very thin film approach of bilayer resist for future lithography, defined the requirements for the resist, and demonstrated 55nm transferred patterns with a high aspect ratio, by using a 2 beam interferometer exposure. In this paper, we have further demonstrated transferred patterns smaller than 60nm using a high NA scanner, and have demonstrated 45nm transferred patterns with a 2 beam exposure system and a 20% Si containing thin bilayer resist.

6519-127, Poster Session

Radiation sensitive developable bottom anti-reflective coating (BARC) for 193-nm lithography first generation

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The use of anti reflective coatings (ARC) in 193nm lithography is a standard production process necessary for critical dimension (CD) control and image integrity. Bottom anti reflective coatings (BARCs) require a plasma etching step to remove them. Developable-BARC (DBARC) need not be removed by plasma etching. DBARC, thus, offers an alternative solution for applications in which plasma etching is undesirable. Ion implant process is one such application in which dyed resist, top-ARC/ resist combination or radiation insensitive, constant dissolution rate-BARC (CDBARC) are used(1). Radiation sensitive DBARCs(2,3) are more tolerant to process parameters than CDBARC and can offer improved performance below 200nm CD than dyed resist or top-ARC techniques.

DBARCs should be insoluble in the casting solvent of the resist but should also be compatible with edge bead removal (EBR) solvents. It should effectively absorb 193 nm radiation while still be transparent enough to be imaged and developed. The imaged stack (resist and DBARC) should be completely removed during the normal resist development process. The challenge of designing such material was met in our 1st generation DBARC product, demonstrated in this paper. This product is applied at a thickness of 30 nm to function as a 1st minimum 193nm DBARC.

The polymer is designed to contain sufficient aromaticity for adequate BARC absorption. It also contains acid labile lactone structure for imaging. The Polymer composition is optimized to be highly hydrophilic and soluble in diacetone alcohol but insoluble in PGMEA. Therefore, the DBARC is compatible with resists using PGMEA as their casting solvent. Commonly used EBR solvents can remove the DBARC as long as the coating is still wet. The other components of the DBARC formulation, such as the photo acid generator (PAG) and base are retained in the film at their intended concentrations.

The DBARC dissolution rate in the developer was used to understand its behavior and select suitable bases. The dissolution rates of exposed DBARC films, containing different bases were measured before and after solvent soak. The changes in dissolution rate before and after soak, compared to the dissolution rate of base free DBARC were correlated to base extractions by the solvent. It was also concluded that the selected PAG was not greatly affected by the solvent soak. This investigation also revealed dramatic dissolution rate differences between the resist and DBARC together as one system and the DBARC alone. Some explanations based on modeling(4) of such systems can be offered.

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6519-128, Poster Session

Post exposure bake unit equipped with wafer shape compensation technology

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In 193nm lithography, it is well known that CDU (Critical Dimension Uniformity) within wafer is especially influenced by temperature variation during PEB (Post Exposure Bake) process. This temperature variation has been considered to be caused by the hot plate unit, improvement of temperature uniformity within hot plate itself has been focused to achieve higher CDU.

However, we have found that the impact of the wafer shape on temperature uniformity within wafer can not be ignored when the conventional PEB processing system is applied to an advanced resist technology.

There are two factors concerned with the wafer shape. First, gravity force of the wafer itself generates wafer shape bending because wafer is simply supported by a few proximity gaps on the conventional hot plate. Next, through the semiconductor manufacturing process, wafer is gradually warped due to the difference of the surface stress between silicon and deposited film layers (Ex. Si-Oxide, Si-Nitride).

Therefore the variation of the clearance between wafer backside and hot plate surface leads to non-uniform thermal conductivity within wafer during PEB processing, and eventually impacts on the CDU within wafer.

To overcome this problem concerned with wafer shape during PEB processing, we have developed the new hot plate that equipped with the wafer shape compensation technology.

This new unit consists of a hot plate, proximity gaps and vacuum seal ribs. Wafer shape is immediately compensated and fixed to flat along the hot plate surface when PEB processing starts.

As a result of evaluation, we have confirmed that this new PEB system has an advantage not only for warped wafer but also for flat (bare) wafer.

In case of the convex shaped wafer with 193nm process, as degree of wafer warping became higher, CDU within wafer became worse with the conventional hot plate, while no impact on CDU was found with the new system.

In case of the flat wafer, temperature uniformity within wafer with the new system was improved by almost 30% compared to that with the conventional hot plate, and CDU within wafer was also significantly improved, achieving 0.8nm (3sigma) against the result of conventional hot plate of 1.2nm.

6519-130, Poster Session

BCM (by-product capping mask) process to define subresolution size of floating gate in sub-90-nm flash memory

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It is necessary to make small size of flash cells for high density flash products. It is indispensable to define small space of Floating Gate (FG) in such a high density flash chips. The KrF lithography resolution limit to define a space is about 130 nm. Also, the space resolution limit of ArF lithography is about 80 nm. But we have to define a space width of less than 70 nm for the fabrication of 90 nm flash memory. Many people is using spacer process to define small space of Floating Gate. This spacer process is required very complicated process of deposition of a spacer film such as oxide or silicon nitride and etching process. So it has many issues to use in mass production even if it overcome lithography resolution limit.

In this research, using the KrF light source, we develop new type of resolution enhancement technique (RET) which is combined with controlled polymer process in etching chamber. We name it as the BCM(By-product Capping Mask) process and it replace the spacer process in a fabrication of 90 nm flash device.

The BCM process can significantly reduce process steps and process time. We understood that the reaction of polymerization was a key factor in BCM process. To optimize this BCM process we used DOE(Design Of Experiments) after setting the important factors of the polymerization reactions. We compared the results of BCM process with those of a spacer process from the view point of profiles, CD uniformity, defect densities, and surface ingredient qualities. Finally, we confirmed that the Floating Gate made by BCM process was more competitive than a spacer process.

6519-131, Poster Session

0.286k1 ArF immersion lithography for 92-nm pitch gate patterning

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Of the mask layers of DRAM, gate mask is the most difficult layer to delineate because it contains nested and isolated patterns together. DRAM chip comprises cell area with nested patterns and periphery area with isolated patterns. Size of cell patterns is 30~40nm smaller than the one of periphery patterns, so that exposure condition is set to focus cell patterns, which makes periphery patterns have poor process window.

As patterns become smaller, DRAM specification can no longer tolerate the poor periphery patterns resulting in the slow operation speed. The conventional way of improving the patterning performance of isolated patterns is to use sub-resolution assist features(SRAFs). However, its effect is not enough. More aggressive ways would be using double exposure technique(DET) or amorphous carbon trimming process at the cost of process complexity.

In this paper, we will study on how to improve the practical resolution limit of isolated patterns without any tricks like DET or trimming process. First approach is to experiment the effect of process factors including illumination pupil condition, resist thickness, post-exposure bake(PEB), post-exposure delay(PED), development time and so on. Second method is to develop the new photoresist which satisfies nested patterns and isolated patterns simultaneously. Most of commercially available photoresists were either for only nested patterns or for only isolated patterns. If photoresist holds wide process window both in nested patterns and in isolated patterns, gate patterning will be a lot easier. To make gate patterns of 92nm-pitch, 1.2NA ArF immersion scanner will be used, which corresponds to process factor (k1) of 0.286.

6519-132, Poster Session

Reducing bubbles and particles associated with photoresist packaging materials and dispense systems

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Packaging, handling and dispensing of photoresist impacts the number of particles and/or microbubbles in the liquid. These abnormalities scatter light during photo processing of microelectronics or flat panel display products and significantly degrade manufacturing yield and performance. Photoresist is typically packaged in either a glass bottle or a polymer film (e.g. PTFE). The polymer film package (NOWPak), also known as a Bag-in-a-Bottle or Bag-in-a-Can, employs a polymer bottle or stainless steel drum to provide the physical support required for the product. Particles and/or microbubbles may be introduced due to physical or environmental stresses induced during shipping and handling. Finally, the dispensing process may generate microbubbles due to the changes in pressure inherent with pumps of pressure-dispense systems. Certainly filters and reservoirs are employed to trap particles or vent gas but additional optimization is desired. A brief overview of photoresist packaging and dispensing technologies is presented toward understanding current challenges of delivering quality chemicals to the semiconductor processing tool. Further, we describe our method to ensure accurate measurement of micron and submicron particles under conditions where the particle and the liquid have similar indexes of refraction.

In this paper we describe physical mechanisms associated with particle generation and microbubble formation in photoresist associated with packaging materials. Particle generation from PTFE film-based packages and glass bottles were studied under a 3000 mile road test and a vibration table simulation of a road test. Although no significant particle generation occurred, microstructural analysis of the film revealed minor changes in the structure as measured by low-angle x-ray diffraction. The particle count and x-ray data will be discussed. We employed thermodynamic expressions, based on the Volmer-Weber model, to describe bubble nucleation and adherence or trapping at surfaces and compared contact angle measurements to a theoretical model of the system. Gas (N2) permeation through several PTFE-based polymer films was measured and compared to gas dissolution rates in glass vessels under a pressurized head-space condition, toward quantifying the impact on photoresist lifetime due to oxygen related discoloring. A model of gas incorporation at each stage of the pressure-dispense system was developed.

Particle measurements were verified by capturing the particles and analyzing them with an SEM. Particles were collected using 0.1 µm ultra high molecular weight polyethylene (UHMWPE) membrane filters and propylene glycol monomethyl ether acetate (PGMEA, a common photoresist solvent) as the liquid. We demonstrated that PGMEA was an appropriate substitute for photoresist toward measuring particle generation in packaging materials. Energy Disperse X-Ray Spectroscopy (EDS) was used to identify particle composition. The ability to accurately measure and control micron and submicron particles and bubbles in photoresist is essential in the achievement of high manufacturing yields.

6519-133, Poster Session

Resist evaluation for contact hole patterning with thermal flow process

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Resist thermal flow (reflow) is one of the techniques that can be applied with minimum lithographic process modifications, especially on contact hole layers, to relax critical dimension constraints in optical lithography. Indeed, if the resist material presents the requested characteristics in term of moderate glass transition temperature, an additional bake step after the pattern development allow decreasing contact hole CD by controlling the resist film thermal flow.

However, depending on the resist chemistry and the lithographic process (bulkiness of the grafted protecting groups, lateral chain flexibility, remaining free volume content after Soft bake...etc.) the flow rate calculated from the CD variation slope versus the flow bake temperature is more or less sharp and easy to control in a production line.

As a result, it is not always obvious to select the best resist materials with the most appropriate process parameters for thermal flow applications.

In this paper we investigate the lithographic performances of different positive tone chemically amplified resists (sensitive to 193nm or 248nm wavelengths) and the characterization methods that can be applied to the selection of resists suitable for contact hole flow processes. Some model polymers have been included into the characterization as well. Unfortunately, although several resists show interesting figures of merit on lithographic performances, often they do not lend themselves to thermal flow because they thermally degrade at or near the reflow temperature [1]. Consequently, we investigate resist thermal properties by thermal analysis (DSC and TGA tools) in order to define material requirements for a resist for thermal flow applications. In addition, flow properties are monitored using rheology analysis. The objective of the work is to understand how the temperature of the reflow bake step can be adjusted and how correlate resist characteristics with lithographic performances after reflow.

Finally, process parameter influences like contact hole size, initial shape, soft bake and post exposure bake temperatures and time have been also considered, in order to propose a 193nm resist adapted to 60 nm contact hole CD after reflow.

Reference

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6519-134, Poster Session

Pattern shrink process for sub-50-nm DRAM

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In the fabrication of sub-100nm DRAM, line and space patterning is not so difficult in comparison to contact hole patterning. Contact hole patterning is more difficult because of its lower aerial image contrast. However, as the pattern size gets smaller below 60nm, line and space patterning also became difficult thing. Direct printing using ArF dry scanner is not good enough to delineate the narrower space pattern even though resolution enhancement technique (RET) is used.

Hyper NA(\>1.0) immersion lithography is expected to play a main role in sub-50nm technology node. In this paper, we will evaluate process window for sub-50nm line & space and contact hole layer. Pattern shrink technologies such as RELACS and SAFIER were set up to give enough shrink rate(≥30nm). Process window and profile of shrink technologies will be compared to those of direct patterning using high-resolution resist. We will also present the defect inspection results after pattern shrink with 1.2NA ArF immersion scanner.

6519-135, Poster Session

Effect of novel rinsing material and surfactant treatment on the resist pattern performance

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In this study, surfactant treat method and novel rinsing material were demonstrated for multi-purpose to improve the resist pattern performance. In DOF increasing, we compared to D.I. water rinse and surfactant treatment with developer process. Table 1 shows the 115nm isolated hole had 15% increase in DoF and the hole circularity also improved. It is due to surfactant can easily to remove the contact hole bottom scum and footing, Applied the treatment for hole pattern not only increases the DoF but also reduces the blind contact risk. In LWR improving, Table 2 shows the 65nm dense line had 13% improve in LWR after surfactant treatment. It is a effective method to improve LWR and no impact with DoF and Exposure Latitude (EL).

Additionally, we have evaluated many rinsing materials for LWR and pattern collapse improvement; therefore, we have screened and developed a novel material TS98 from six chemical candidates. We have investigated application of this method to the 45nm node process, 60nm dense line, with aspect ratio=2.3; As compare to standard developer process. Table 3 shows LWR improved by 6% with novel material TS98 treatment. In addition, we also describe our studies on pattern collapse improvement; the pattern collapse problem is due to capillary force that is increased as the pattern size decrease. As a result, the novel material TS98 has lower surface tension, was effective to decrease this capillary force and increase the pattern collapse margin, the tested with 60nm dense line, the Critical Normalized Aspect Ratio (CNAR) has 15% increased compare to D.I. water. TS98 appear the effectiveness to improve the LWR and collapse.

The novel rinsing material TS98 and surfactant treatment were effective to solve LWR, pattern collapse problem and DoF increasing; In the future, we will investigate the ADI and AEI LWR relation and application of defect reduction by rinsing treatment. We believe the methods will be applicable to 45nm node and beyond.

6519-136, Poster Session

Impact of airborne NH3 and humidity against wafer-to-wafer CD variation in ArF lithography through 45-nm technology node

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As a feature size of semiconductor devices gets smaller, the aggressive requirements for critical dimension uniformity (CDU) have become a critical issue in the leading edge ArF lithography. Our CD budget analysis indicates that wafer-to-wafer (WTW) CDU improvement might be more difficult than within wafer (WIW) CDU improvement. Because the WTW CDU involves more variation factors and the impact of each variation factor has not been fully understood.

One of the important factors contributing to WTW CD variation is a process time delay, such as a post apply delay (PAD) and post expose delay (PED). It is very likely the process time delay effect is related to the environmental control in the integrated photo-cluster (ArF scanner and track system). Previous authors have shown that the most significant environmental effects were the amine in the photo-cluster environment. This paper explores the CD impact of air-borne NH3 and humidity on WTW CD variation taking account of resist formulation dependencies, such as PAG, base polymer and solvent system. From these experiments, recommendations are made for the optimal 45 nm environmental control inside the integrated photo-cluster.

6519-138, Poster Session

Proximity effect correction for the chemical shrink process of different type contact holes

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Small contact hole patterning had become the most difficult task in optical lithography as design rule of semiconductor continuously shrinks below 65nm. Conventional contact hole scheme need to avoid side-lobe and conduct complicated dense-isolated bias for resolution enhance and depth of focus (DOF) improvement. To overcome this issue, some RETs (Resolution Enhancement Techniques) by process had been investigated, like RELACS (resolution enhancement lithography assisted by chemical shrink). RELACS is one of feasible procedures which could provide enough improvement in resolution, photo-resist profile, DOF, and CD uniformity (CDU). Proximity effect is one of significant topics to evaluate chemical shrink bias of different type contacts. With regard to research of shrink bias of different size

and pitch contacts had been investigated broadly in the past. In general, the constant bias of shrinkage for difference pattern size was an assumption. However, according to our evaluative results, we had characterized the correlation about the shrink bias versus pattern size. In this paper, we will present chemical shrink bias of different size and different pitch contact holes and then we could follow this correlation rule to define general rule for proximity effect correction.

6519-140, Poster Session

Mechanism of post develop stain defect

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In regards to stains appearing on the resist pattern after developing, this study succeeded in the reduction of these stain defects by improving the develop process. Furthermore the mechanism of this stain defect was considered by analyzing components of the defect.

Since the stain defects of former generation such as i-line or KrF resist defect are known well, even now this defect is seen on the ArF resist. The appearance of this stain defect was caused by a kind of resist or pattern. Until now this defect has been resolved by improving the resist.

In this study however, we tried to resolve the stain defect by the improvement of the developing process. As this improvement was able to greatly reduce this defect with no change to the resist or pattern, it was understood this defect is much influenced by the developing process. Thus it is projected the resist surface condition during the develop process was the important key to decreasing this defect. It should be understood the number of defects was changed by the kind of resist or pattern. First we analyzed the components of the stain defect itself. Next we analyzed the change in resist surface condition by the new develop process.

As a result, it was realized this stain defect was from the developer chemical, it was considered that the developer remaining on the resist film caused the stain defect. As the resist surface condition was changed by the improved develop process, resulting in a sharp decrease in the stain defect.

6519-141, Poster Session

New ArF resist introduction for process through-put enhancement

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The equipment development and process improvement have been continuously done for through-put enhancement of mass production in semiconductor industry. The improvements of photo exposure tool and photo related material have been also progressed to correspond with this trend in litho process. Especially, the track applying to photo process is one of the main factors to affect on the through-put of wafer process. The developing time in track process has been known as a major bottle-neck point for the litho process. Recently, several types of developing nozzles are evaluated and introduced to reduce the developing time and finally shorten the patterning process time without pattern profile deformation. And the more developing units are being also applied to improve the through-put for developing process. However, these developing time and units controls induce some limitations for the through-put improvement in the respect of hardware technology and space in track.

Therefore, new resists which can reduce the process time and enhance the through-put are introduced in this paper. These resists are having less SOB and PEB process time than those of other resists. Normally, the baking times of currently used ArF resists are 90s for SOB and PEB process, respectively. At present, we are going to reduce the process time by controlling the SOB and PEB time below 60s without profile deformation and margin reduction for the below 80nm size of L/S patterns. Several PAGs and additives will be applied to control the baking time for ArF resist. The diffusion length and rates of PAG will be a key point to control the pattern formation for the less baking time condition. The top view profile and cross-sectional views of resist patterns formed by baking time less resists are checked and compared with those of currently used resists. The profile performances of resists and the compatibility between resist and substrate will be evaluated on the different types of substrate conditions. And the several properties of resist like bulk effect and contrast will be tested to check the application possibility for mass production. From these experimental results, it will be confirmed that the baking time less material can be act as a driving factor to improve the through-put of litho process.

6519-142, Poster Session

A heater plate assisted integrated bake/chill system for photoresist processing

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The lithography process is the most critical step in the fabrication of nanostructures, accounting for one-third of the costs of integrated circuit manufacturing. Thermal processing of semiconductor substrates through conductive heat transfer is common and critical in the lithography. Each thermal processing step involves baking the substrate to an elevated temperature for a given period of time, this is then usually followed by a chill step which is used to cool the wafer to an appropriate temperature for subsequent processing. Of these baking steps, the post-exposure bake step is the most sensitive to temperature variation for the current generation of chemically-amplified resists (CARs). For such CARs, the temperature of the wafer during this thermal cycle have to be controlled to a high degree of precision both spatially and temporally. A number of recent investigation also shows the importance of proper bakeplate operation on CD control. Consequently, the temperature control system for this process requires careful consideration, including the equipment design and temperature sensing techniques.

Because of its large thermal mass and sluggish dynamics, conventional hotplates are robust to large temperature fluctuations and loading effects, and demonstrate good long-term stability. These advantages however become shortcomings in terms of process control and achievable performance when tight tolerances must be maintained. Other disadvantages include uncontrolled and non-uniform temperature fluctuation during the mechanical transfer of the substrate from bake to chill plates, spatial temperature non-uniformities during the entire thermal cycle, etc. This lack of a method to conduct real-time distributed, closed-loop temperature control with conventional hotplates is a source of process error in the lithography chain. Considerable improvement has made in novel designs of these thermal systems in the literature by our collaborators and us, however a number of shortcoming still exists including excessive power consumption, cost issues in fluid-based systems, inability to conduct rapid ramp-up and down heating rates etc.

In this work, we describe a new thermal processing system developed for optimal processing of temperature sensitive photoresist so as to address the abovementioned issues. Our proposed system comprises of a heater plate for heating the substrate, coupled with an array of thermoelectric devices (TEDs) which provide real-time spatial and temporal temperature uniformity control and active cooling as shown in Figure 1. During the baking process, the various zones of TEDs will be separately and judiciously energized to maintain temperature uniformity throughout the wafer. Depending on the polarities applied to the TEDs, they can operate in either heating or cooling mode. This makes them excellent regulating devices.

The proposed system offers excellent temperature control during the entire thermal cycle, eliminates substrate movement during the baking and chilling processes, and accommodates in-situ temperature measurement for real-time control. The feasibility of the proposed approach is demonstrated via detailed simulations based on first principle heat transfer modeling. Figure 2 shows the system performance for a typical bake and chill cycle. A prototype is currently being developed to demonstrate the thermal system capability.

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6519-143, Poster Session

Molecular contamination control technologies for high-volume production phase in high-NA 193-nm lithography

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While the current standard for NA (Numerical Aperture) for the semiconductor resist process is 193 nm, use of the 193 nm immersion exposure process is growing and almost ready for application in mass production. With these finer design rules for devices, it is necessary to ensure a cleaner atmosphere around wafers by not only by reducing the ammonia concentration, as is done conventionally, but also by limiting the concentration of amines and N-methyl-2-pyrrolidone (NMP) to low levels. The cleanliness of the space around wafers depends heavily on the performance of chemical filters.

Focusing on the fact that the collection efficiency of chemical filters varies according to the coefficient of molecular diffusion of the gaseous species to be collected, we are involved in research on chemical filters that can be applied to future lithography processes. It is generally known that chemical filters can use two types of adsorbent: the “neutralization reaction type”, using the conventional reaction mechanism; and the “ion exchange type”, using a new reaction mechanism. We studied the use of a strong acid cation exchange resin as an adsorbent to provide high removal efficiency and high adsorption capacity. To take the fullest advantage of the capability of adsorbents, we have established a method of deriving a filter structure with adequate reaction efficiency by applying adsorption theory.

This paper reports high-performance chemical filters that can be applied to next-generation exposure and coating & development technologies, including liquid immersion lithography, while meeting the increasingly stringent requirements.

We evaluated the adsorption and breakthrough behavior of chemical filters under combined amine gas conditions, taking into account the fact that the actual atmosphere around wafers simultaneously contains different amines. In addition to amines, organic contaminants originated in various chemicals used in the process also exist in the atmosphere around wafers. The presence of these components cannot be ignored. We thus verified the adsorption behavior of chemical filters under combined conditions designed to correspond to an actual service environment and established a method of designing chemical filters with superior capacity to adsorb combined amines.

6519-144, Poster Session

Printing of structures less than 0,3 μm by i-line exposure using resists TDMR-AR80 and TDMR-AR95

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In the last few years there has been increasing interest in high resolution i-line resists which allow the printing of structures smaller than 0,3μm. In many applications this will help to avoid the use of DUV-steppers which are higly cost intensive in regards to price and cost of ownership.

We have evaluated the resists TDMR-AR80 und TDMR-AR95 from TOK Company in order to check their potential concerning minimum line width and focus /exposure process latitude.

TDMR-AR80 und TDMR-AR95 are regarded as dissolution contrast enhanced i-line resists. Attached OH-groups on the polymer chain lead to enhanced solubility of the exposed, and a higher insolubility of the unexposed regions in comparison to resists of former generations, thus leading to a higher contrast which enables printing of smaller structures.

We have investigated the focus/exposure process latitude of the two resists with our main focus on trench structures. The Bossung Plots of dense lines and semi-dense lines were determined. The resist profiles were characterised both by inline-SEM measurements and cross-sections. The influence of several stepper illumination modes and Off Axis Illumination (OAI) on the focus/exposure process window was investigated. Resist characterisation was additionally done by defect density measurements and theoretical litho simulation.

The implementation of the resist in production provided large amounts of data which enable the calculation of parameters related to process stability (wafer to wafer and lot to lot CD-standard deviation, Cp-, Cpk-values etc.).

Results:

The resistsTDMR-AR80 and TDMR-AR95 enable printing of trench structures less than 0.3um. For 0.3μm lines, our specification limit of 0.3μm +/- 10% was reached within a focus range from - 0.1 to 1.0 microns. OAI illumination mode enlarged the focus window by 20% in comparison to the standard illumination mode. Structures of 0.28μm and 0.26μm were printed with a focus window of 0,7μm which shows the high potential of this resist generation.

The focus/exposure window derived from the litho simulation fits well to the values observed in the experiments.

Cross-sections didn´t show any significant profile change between the focus values of -0.2μm to 0.8μm. In all cases the difference of the angles on both sides of a resist line (= Coma) was less than 4°. Defect density measurements showed excellent results. No hint of defects caused by chemical reaction of resist and developer was found.

Whereas TDMR-AR80 is designed as a resist for high reflective substrates, TDMR-AR95 should be used in combination with a BARC-resist. The reduction of any swing curve effects enables better CD-uniformity and higher resolution. Therefore, the system BARC/ TDMR-AR95 showed the best results in regards to CD-uniformity, printing of minimum size structure and high volume process stability.

6519-145, Poster Session

Various factors of the image blur in chemically amplified resist

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In the current optical lithography, the resolution is being pushed for 45 nm half-pitch node, and there is care strongly for coverage of chemically amplified resist, including immersion lithography. So far the chemical amplification has brought high performance for lithography. In future, for the ArF lithography beyond 45nm half-pith node, it will be important to control pattern size. On the other hand, because of the including of physical and/or chemical factor such as many wafer flows and chemical reaction process, the chemical amplification is attended by the resist blur. Concretely, there are various factors in the each wafer flow (Resist coating, Post bake, Exposure, PEB, Development and Rinse) to cause the resist blur. For example, it’s acid diffusion on PEB. The influence of these factors for the resist blur is a significant issue for lithography beyond 45 nm half-pitch node. Therefore the need to reduce these factors on the resist blur becomes higher in order to further extend the ArF lithography beyond 45 nm half-pith node.

In this paper, the various factors on the resist blur, which we achieved from our efforts, are reported. We commenced consideration for the various factors on the resists blur in chemical amplification in high NA ArF lithography. As high NA tool, we used the interferomentric exposure tool. As the results, we found the strongly interrelation between the various factors and the resist blur, and referred the influence of resist blur for 45 nm half-pitch node.

6519-146, Poster Session

Image tone optimization in advanced mask making for DUV lithography

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Deep-UV (DUV) lithography has been developed to define minimum feature sizes of sub-half-micron dimensions of devices semiconductor. In response to this trend, DUV mask technology has been proposed as an effective technique for considering the reduction of mask making cost, especially, in low volume designs. However, the requirement of tight CD control of the mask features in advanced devices is resulted in increasing of mask cost. In this research, we discussed two different typed image tones comparison, positive and negative tone, in DUV lithography. The choice of final mask tone needs to be selected as

function of pattern density and shape. The evaluation items to judge if the mask is good are the final CD uniformity, pattern edge quality, resolution and mask throughput. Both mask process and manufacturing throughput are affected by image tone type of positive and negative . This paper will show the procedures and results of experiment.

6519-147, Poster Session

Advanced photoresist dispense valve control technology for process control improvement, process stability

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As resist volume must decrease to make IC's more profitable, the accuracy and repeatability of dispense systems must increase. Any inconsistencies in a dispensing system can negate any savings that could potentially be acquired due to rework or even scrap. This has become a problem for older factories with pumps that are not accurate below 2.0ml per dispense. In order to help with these issues, Integrated Designs (IDI-CYBOR) has created the Digital Dispense Valve System.

This digitally controlled mechanical valve upgrade can prolong the life of a dispense pump and save a potential costly pump replacement. The digital dispense valve increases the accuracy & repeatability at lower dispense volumes and gives more repeatable suckback control than was previously available for this generation of pump systems with pneumatic valve controlling dispense and suckback. The Cpk and Process Stability can be increased greatly when compared to the previously used mechanical valves vs the new digital valves.

6519-148, Poster Session

Automatic viscosity controlled production of photoresist

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Viscosity of photoresist is an important product parameter because it determines film thickness during spin coating. Producers of photoresist, therefore, have implemented manufacturing procedures which require that fluid viscosity be measured several times during production. To ensure product quality, periodic samples are taken off-line to an analytical laboratory where viscosity is measured under controlled conditions. However, off-line measurements, interrupt production, engage valuable human resources, and fail to provide adequate process feedback. This paper describes the implementation of an automatic viscosity-controlled production process of photoresist. A unique in-line viscometer is employed that automates the process and increases throughput. With sufficient accuracy and repeatability of the measurements, it is now possible to correlate and predict film thickness with viscosity values taken during photoresist production.

6519-149, Poster Session

Adhesion effect of resist reflow process

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It is one of the difficult issues how to make sub-100 nm contact hole pattern. We have to execute another fabrication process on photolithograpy to make sub-100 nm contact hole pattern. Compared to another fabrication process, resist reflow process is a good method to obtain very high resolution contact hole without the loss of process margin. However it is not easy to predict the actual reflow result by simulation due to very complex physics and/or chemistry is involved in resist reflow process. We must know a certain chemical constant value and many fabrication variables. We made resist reflow simulation tool to predict approximate resist reflow as functions of pitch, temperature, time, array, and so on. We are able to see the simulated top view, side view and the changed hole size. We used Navier-Stokes equation for resist reflow. We had varied the reflow time, temperatue, surface tension, and 3-dimensional volume effect for old model. However the photoresist adhesion is another very important factor that was not included in the old model.

6519-150, Poster Session

Investigation of mechanism of pattern deformation on TiN substrate and O2 plasma effect without BARC

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The pattern deformation such as photoresist lifting after lithography due to not enough photoresist adhesion to substrate is become critical issue when aspect ratio is much higher than what photoresist adhesion can support. This aspect ratio is getting higher when our design rule of device requests smaller feature size in lithography process. The BARC (Bottom Antireflective Coating), which advanced lithography is using, is very good layer to improve adhesion of photoresist since they are same kind of chemical. However, BARC needs extra etching process before main etching which is step to remove substrate. Sometimes, this BARC etching step generated defects which makes yield loss. Especially, lithography step for metallization with aluminum likes without BARC process to be free from those defect. We think that adhesion of photoresist on metal substrate such as aluminum or TiN is very important to develop lithography process without BARC. The adhesion change between photoresist and metal substrate will be changed as function of how we apply pretreatments for metal substrate. The typical pretreatments before patterning are dry ash, wet cleaning and HMDS treatment.

In this paper, we study that adhesion changes as function of pretreatments and their mechanism. To understand the interaction between photoresist and substrate, we analyze surface change of wafers which prepared with several different experimental conditions using Auger Electron Spectroscopy(AES) and Dynamic Contact Angle Analyzer. The results will explain how photoresist adhesion may be changed with different pretreatment conditions and how we can optimize process condition to improve photoresist adhesion without BARC.

6519-151, Poster Session

62 μm-scribe-line 90-nm product alignment signal improvement: remove TIN HM on alignment mark

C. Chen, A. Chia, A. Chang, J. Lee, C. Chen, C. Huang, United Microelectronics Corp. (Taiwan)

As product scribe line shrunk from 110um and 80um to 62um, the alignment signal (W.Q.) apparent become weak. Many wafers occur alignment error to cause wafer scrapped. For improving 62um-scribe-line 90nm product via align to trench alignment mark signal (W.Q.), removing TIN HM on trench alignment mark can help to acquire a better alignment signal. For the sample via and trench layer, the AA capability is comparable to old alignment method. As the result, over 90% of alignment signal (W.Q.) absorbed by TIN HM layer can be verified.

In this article, the evaluation results of various mark types will be discussed. Among the alignment signal of these mark types, the best one can be chosen to use on future process, however, due to CUCMP residue issue, "half size open" and "full size open" can not be used. Therefore, "sizing + 0.25um" mark on trench mask for via alignment is suggested to use for better alignment.

6519-152, Poster Session

Accurate photoresist usage forecasting

L. C. MacDowell, IBM Corp.

Accurate photoresist usage forecasting is essential for smooth operation of semiconductor fabs, with overstocking leading to waste due to shelf life expiration and understocking potentially leading to running out of photoresist with an uplift in product demand. Most photoresists have a short shelf life, typically six months, long lead times for delivery and usage can vary significantly depending upon

semiconductor product demand. Fabs with a large number of product types with a subsequent high number of different photoresists can be challenging to project accurate usage.

Calculating monthly photoresist consumption involves more than multiplying wafer coating volume by wafer passes. Other critical factors that need to be included in the calculation are the number of photo tracks loaded with a particular photoresist, the frequency of the periodic dispense to waste to keep the delivery lines from drying, the consistency of the coating volume wafer to wafer, percent rework required and the number of process monitors run on the track.

All of these factors can be combined to accurately project photoresist usage and data will be presented from the IBM 200 mm fab located in Essex Junction, Vermont showing projected versus actual usage of both low and high volume photoresists and the usage calculation methodology.

6519-153, Poster Session

Consignment stocking of photochemicals benefits and risks

L. C. MacDowell, IBM Corp.

The IBM 200 mm logic fab located in Essex Junction, Vermont has utilized consignment stocking of photochemicals (photoresists, ARC's, polyimides and solvents) for several years with multiple suppliers which has provided benefits to both IBM and the suppliers with minimal risk. Consignment stocking is defined as the supplier providing inventory, typically a three month supply, of photochemicals to be stored in the IBM chemical warehouse and IBM then paying for the material as it is consumed by fab manufacturing. A monthly usage or pull report is sent to the supplier for invoicing. Photoresists are the most challenging chemical type for consignment stocking due to short shelf life and the need for refrigerated storage for advanced photoresists.

The benefits to IBM include delayed payment, longer term inventory supply, large chemical lot sizes which reduces QC testing and maximum shelf life due to build to order chemical lots. The supplier benefits from eliminating storage of IBM inventory, not building ahead due to build to order, reduced QC testing due to large batch sizes and accurate chemical usage reports for raw material planning. The major risk to IBM is shelf life expiration of photoresists due to product demand slowdowns and the need to maintain refrigerated storage. Accurate usage forecasting is critical for a successful photochemical consignment stocking program.

6519-36, Poster Session

Simulation of the combined effects of polymer size acid diffusion length and EUV secondary electron blur on resist line-edge roughness

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Line-edge roughness (LER) poses important obstacles for meeting the specifications suggested by ITRS related to resists. With the shrinking of dimensions and the requirements of low resist LER, even the second-order-important phenomena should be considered explicitly. Fine-tuning of lithographic materials and processes is mandatory. Lithography simulation is necessary in order to predict the effects of a large number of parameters, sometimes inter-related, on the final value of resist LER. Stochastic simulation could assist in understanding the microscopic changes in the resist material during processing. The parameters that affect LER are related to exposure, material and process, and should be examined independently in order to be optimized. In the current work, each polymer chain in the resist film is explicitly considered as self-avoiding random walk. Chains are mutually excluded, simulating the excluded volume interactions in the real film. Also, the photoacid generator (PAG) molecules are considered separately, and acid diffusion is simulated through a random walk around the acid creation position. This framework gives the ability to consider every microscopic process in the resist film in great detail. Shot noise and secondary electron blur (SEB) models for EUV exposure were incorporated in the stochastic lithography simulator. An "energy map" from EUV exposure simulation, is constructed which is normalized and used as an initiation probability for the PAG molecules. An ionization "in the vicinity" of a PAG will activate the PAG. Then acid diffusion, deprotection, ionization, development, etching and edge LER quantification can be performed. The effect of sidewall etching on the edges of the top down image is considered isotropic. The rough edges of the top down image constitute a boundary, whose evolution during etching yields by solving the Eikonal equation. Its numerical solution is accomplished by the Fast Marching method. The effects of shot noise from EUV simulation of the exposure process combined with the acid diffusion range and the polymer size of the resist, will determine the process window in terms of minimum LER. Also our aim is to give quantitatively the proportion of each of the considered parameters on the final LER value. The simulation tool will be used to predict trends in LER rather than absolute values, but the simulated LER will be compared to experimental findings wherever possible. SEB might be inappropriate for low average degree of polymerization (ADP) even if acid diffusion due to post-exposure bake has been optimized. SEB effects are additional to diffusion, i.e. excessive diffusion as well as excessive SEB deteriorates LER. The percentage participation of ADP, acid diffusion range (LD), and SEB on the final LER of the resist should be quantified. This is the purpose of the proposed work. Simple lines/spaces layout in a top-down view (2D) will be considered for the quantification of LER and examples of the application of the simulator in cases of complex layouts will also be given.

6519-47, Poster Session

Distribution control of protecting groups and its effect on LER for EUV molecular resist

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The minimum feature size for the LSI circuit geometry will reach below 20 nm in the upcoming 32 nm half pitch. In order to achieve this target, various new lithographic technologies, such as ArF immersion lithography with double patterning, Electron-Beam (EB) and Extreme UltraViolet (EUV) lithography, are now simultaneously being developed. However, line edge roughness (LER) of the fabricated resist patterns is becoming the most significant issue as the gate length is reduced [1-4]. The aim of this study is to develop a new resist, which can pattern with a molecular level accuracy.

We have reported the characteristics and LER properties of molecular resists based on low molecular weight polyphenols as a chemically amplified positive-tone EB resist [5-7]. In this article, new molecular resist based on polyphenol derivatives for EUV lithography will be reported.

We have designed and synthesized a molecular resist material, which has no distribution of the protecting groups and have evaluated its performance as a molecular resist with an EUV exposure tool. The molecular resist attained a resolution of sub-30 nm patterning. It was found that controlling the distribution of the protecting groups in a molecular resist material has a great impact on improving LER.

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Acknowledgment

This work was supported by the New Energy and Industrial Technology Development Organization (NEDO) under the management of the Key Technology Research Promotion Program.

6519-154, Poster Session

Evaluation of the 3D compositional heterogeneity effect on line-edge-roughness

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Line-edge-roughness (LER) and the relationship to resist processing and materials design is a critical problem for sub-65 nm photolithography. In this work we investigate how chemical composition fluctuations (heterogeneity) produced by the reaction-diffusion of photoacids in chemically amplified photoresists affect the resulting LER through computer simulation. A 3-dimensional microscopic picture of reaction-diffusion of individual photoacid accounts for the deprotection fluctuation formed by the post exposure bake (PEB). The resulting LER is related to both the gradient of average deprotection profile and the degree of local chemical heterogeneity. The effect of dose contrast, PEB time, diffusivity of photoacid and trapping strength on the chemical heterogeneity are evaluated and compared to neutron reflectivity measurements.

6519-155, Poster Session

Reduction of LER by controlled copolymerization in ArF lithography

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In recent years, ArF lithography requires half-pitch size (DRAM) of 45nm or below. To achieve the requirement, line edge roughness (LER) is recognized as one of the most serious problems in lithography today, because it directly degrades device characteristics and affects system performances. LER is greatly affected by lithographic processes (exposure, acid-diffusion, deprotection and development) and material properties. The effect of factors involving the lithographic processes is not small, but we think that a practicable approach to reducing LER is to control the material properties. The many researches are doing actively for the base polymer and monomer materials for ArF positive-tone resists. LER in chemically amplified resists is understood to be fluctuations in the acid catalyzed reaction that determine molecular solubility and developer percolation. A typical fluctuation size in these processes is significantly larger than the molecular size and depends on various parameters, such as acid concentration, diffusion length, molecular size, protection ratio and variation, and polymer aggregates. Yamaguchi et al. reported polymer aggregates are naturally contained in the resist films, and there is the difference between dissolution rates of inside and of outside aggregates.

In this paper, we hypothesized that reduction of LER is correlated with the improvement of the polymer uniformity. 2-methyl-2-adamantyl methacrylate, 3-hydroxyl-1-adamantyl methacrylate, and gamma-butyrolactone-2-yl methacrylate copolymer were prepared by controlled copolymerization. By the observation with AFM, we found that the uniformity of the polymer was improved. The resist samples were formulated with polymer, photo acid generator (PAG), quencher and solvent. And the resist films with 250nm thick were spin-coated on silicon substrate and soft baked. Lithography was done by two-beam interference (TBI) lithography. The magnitude of LER was measured by top-down scanning electron microscope (SEM) method and top-down AFM method. As the result of investigation of lithographic pattern, LER was affected by uniformity of copolymer. Furthermore, the result of the analysis by quarts crystal meicrobalance (QCM) method was shown that the dissolution behavior was correlated with the uniformity of copolymers.

6519-156, Poster Session

A study of process extension technologies

S. Kim, The Catholic Univ. of Korea (South Korea)

Current 193-nm optical lithography and commercially available 193-nm resists are pushed far beyond previously expected critical dimension by using process extension technologies for the resolution enhancement. It is necessary to model and analyze those process technologies to control shrinkage sizes. In this paper, four kinds of process extension technologies such as thermal treatment, polarization illumination, etch trim, and double patterning are summarized and modeled. Those simulated results have a good agreement to experimental available results. Through analytical approach, those process benefits are compared quantitatively and optical proximity correction of each process are described. To generate below 20 nm half pitch pattern, the possibility of those technologies is discussed.

6519-158, Poster Session

More developed mechanical modeling of pattern collapse simulation in 193-nm immersion lithography

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High aspect ratio resist patterns with dimensions below 50 nm often bend, break or tear. These phenomena are generically called “resist pattern collapse”. Pattern collapse is a very serious problem in fine patterning less than 50 nm critical dimension (CD), so that it decreases the yield. In order to analyze mechanically this phenomenon and create its simulator, two models have been made and compared. In this paper, various approaches with various analyses are made to understand pattern collapse[1.2]. Also, the critical aspect ratio for 50 nm node, that determines whether pattern collapse happens or not, can be calculated with these approaches. Finally, added spinning for more effective pattern collapse mechanical modelling[Fig. 1]. Also, did Simulation about pattern collapse phenomenon according to sidewall angle.

6519-160, Poster Session

The rational design of polymeric, non-CAR, EUV-resist materials by QSPR modeling

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Extreme ultra-violet (EUV) lithography, in which the irradiation is carried out with 13 nm (~ 90 eV) photons, is one of the likely candidates for next generation lithography, with the potential to permit the patterning of features below 50 nm[1]. A number of limitations in the currently available technologies, however, need to be addressed. These include the development of resist materials that have: a low adsorption cross section (i.e. high transmittance), high sensitivity and contrast to 13 nm radiation, minimal production of volatile components (i.e. outgassing) and low line-edge roughness (LER) values. Current research efforts include, for example, investigations of polymeric systems containing photoacid generators (PAG)[2], molecular glasses (with or without PAG)[3] and multilayer resists[1].

To date, however, there are no resist formulations which are capable of meeting all of the requirements above or, indeed, the target LER values. Additionally, the diffusive path-length of the PAG may be up to 50 nm, a significant size compared with the feature size (sub-50 nm) and target LER criteria of emerging lithography technologies. In this work we present preliminary results in the use of a rational design approach to guide the design and synthesis of non-chemically-amplified (non-CAR), polymeric resist materials for 13 nm, EUV lithography.

This paper focuses on the development of a qualitative structure property relationship (QSPR)[4] model to predict the rate of radiolysis of polymeric materials as a function of the chemical constituents in both the main and side chains of the polymer structure. The QSPR model was developed using data obtained from the radiolysis of a range of low molecular weight species and carried out at 1 MeV (γ irradiation) or at 70 eV (mass spectrometer electron ionisation source).

The choice of 1 MeV or 70eV irradiation as models for the EUV process was made to allow for the high-throughput determination of a large enough chemical space for the QSPR model and the ability to screen species with potentially volatile products. Moreover, correlations between the γ and electron ionisation, and EUV radiolysis of selected polymers was carried out to verify that the higher energy irradiation is a suitable model process for EUV and is further discussed in this work.

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6519-161, Poster Session

Model-based OPC for BARCless DUV process

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The BARCless DUV process doesn't use bottom anti-reflective coatings diverging from conventional process. It is well known that the role of BARC is reduced sub-layer film effect. Because BARCless process is more affected by substrate, photoresist profile between isolated line and dense line is quite different. So behavior of pattern CD without BARC is significantly different to using BARC. This can cause the fitting error. This paper reports the OPC modeling methods for BARCless process.

6519-163, Poster Session

Some nonresist component contributions to LER and LWR

T. Kudo, S. Chakrapani, G. Lin, C. Antonio, D. Parthasarathy, R. Dammel, M. Padmanaban, AZ Electronic Materials USA Corp.

Line edge roughness (LER) and line width roughness (LWR) become more important in manufacturing sub 100 nm node devices, because they are directly related to reliability and production yields of devices.We have investigated various process factors determining LER/LWR of 193 nm resists. In this paper, we report influence of mask layout (bright field/dark field), pitch dependence, substrates, film thickness, developers and optical settings on LER/LWR and the origins of line roughness are discussed.

6519-164, Poster Session

Depth-of-focus and line-width roughness (LWR) performance of novel surface conditioner solutions for immersion lithography

B. J. Lu, United Microelectronics Corp. (Taiwan)

As the lithographic technology goes beyond 45nm node, line edge roughness (LER) and line width roughness (LWR) have become critical parameters. There is a growing interest in applying surface conditioner solutions during post-develop process to reduce LER. Surface conditioners would interact with resist sidewall selectively, causing surface plastization effect and smoothing the sidewall profile. As a result, LER can be reduced significantly. In this paper, the features of 45nm lines/spaces patterned by immersion lithography were used to evaluate surface conditioners performance on LER reduction. The results showed about 10~15% LER reduction, as well as a significant improvement on the common process window for LER. No negative impact on the resist profile was observed with the new process.

In addition, etch testing was conducted to determine how much post-develop LER reduction has been retained through etch by comparing post-etch and post-develop LER for both baseline and surface conditioner processes.

6519-165, Poster Session

Effect of photo-acid generator concentration and developer strength on the patterning capabilities of a model EUV photoresist

K. Choi, Intel Corp.; V. M. Prabhu, K. A. Lavery, E. K. Lin, W. Wu, J. T. Woodward, National Institute of Standards and Technology; M. J. Leeson, H. B. Cao, G. Thompson, Intel Corp.

Current EUV photoresist materials do not yet meet performance requirements on exposure-dose sensitivity, line-width roughness, and resolution. In order to quantify how these trade-offs are related to the materials properties of the resist and processing conditions, advanced measurements and fundamental studies are required that consider EUV-resist specific problems. In this presentation, model EUV photoresists are studied to quantify the influence of photoacid generator loading and developer strength on EUV lithographically printed images. The developed line-space patterns were examined for critical dimensions and pattern density for features ranging from (40 to 120) nm. An atomic force microscopy (AFM) technique was used to examine the line-edge quality of the latent image. These results are then correlated to the developed image using varied developer concentrations and characterized by top-down SEM. Finally, these EUV lithographic imaging results would be discussed with respect to swelling and dissolution behavior using quartz crystal microbalance measurements.

6519-166, Poster Session

A study of EUV resist outgassing characteristics using a novel outgas analysis system

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Resists are one of the most critical issues in the realization of extreme ultraviolet lithography (EUVL) for use in actual semiconductor device manufacturing below the 32-nm node. This is because at present, no resist concurrently meets the requirements for resolution, sensitivity, and line width roughness (LWR). Another concern for EUV resists is outgassing at these highly energetic wavelengths under vacuum. At the estimated throughputs of high volume manufacturing (~100 wafers per hour)1 , there is a huge concern about optics contamination.

In efforts to protect EUV optics, all materials used in EUV vacuum exposure chambers must be screened prior to use. Resists are a concern since a freshly coated wafer will be introduced into the chamber approximately every minute in a high volume production tool.

We have designed a novel outgas analysis system to ensure the safety of various optical elements from the possibility of outgas contamination from the resists.

In this analysis system, a stand-alone EUV source (EQ-10MR by Energetiq technology, inc.) of comparatively high power output2 is utilized for accelerated outgassing evaluations at ultra-high vacuum conditions. Various outgas evaluation methods were also made available for use in this system. Quadropole mass spectrometry (QMS), gas chromatography - mass spectrometry (GC-MS), quartz crystal microbalance (QCM) and 'witness plate' analysis methods are utilized to accurately capture and quantify resist outgassing elements that may be released before, during and after EUV exposure.

The GC-MS evaluation set-up as shown in fig.1 is quite unique from the commonly available outgassing systems with the utilization of the 'cold-trap sampling technique'. In this outgas sampling technique; a 'trap box' is set over the resist coated wafer fragment during exposure. Using an internal cooling system, the trap box temperature is lowered to catch outgassing elements released from the resist wafer fragment. After exposure, the trap box is then transferred to a heating chamber where the outgas elements that have adhered to the trap box is heated and released to a desorption tube for GC-MS analysis. This process is performed under ultra-high vacuum conditions.

The results of the system performance evaluations will be discussed in the conference. Also, using the above mentioned evaluation methods, the analysis and definition and quantification of various resist outgassing elements and their respective release mechanisms will be reported.

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This work is partially supported by the New Energy and Industrial Technology Development Organization (NEDO).

6519-167, Poster Session

Sub-10-nm contact holes with aspect ratio over sixty formed by e-beam resist shrinkage techniques

W. G. Chen, M. Kao, M. Tsai, Industrial Technology Research Institute (Taiwan)

There are potential applications of sub-10nm contact holes with high aspect ratio in nano-electronics and nano-lithography in the near future. E-beam chain scission resist ZEP520A with 400nm thickness was studied for sub-10nm contact holes with high aspect ratio formed by CD shrinkage techniques of thermal reflow and SAFIER. CD shrinkage temperatures and repeating times were process parameters to be studied. Design parameters of initial CD and line/space ratio of contact hole with 1/3 and \>1/20 before shrinkage were also studied. PAB temperature of 70oC was used for the baking of ZEP520A. ESIZE for contact holes with 40-100nm initial CDs at 70oC PAB is 150-290μuC/cm2. CD shrinkage was processed from one to six times at most with 90 sec for each time at the shrinkage temperature. CD-SEM and cross-section SEM were used to measure the top-CDs and sidewall profiles of contact holes individually. The cross-section SEM shows that a contact hole passes through the resist to bottom with clear contrast while the CD-SEM shows a gray top-CD image for shrunk CD less than 10nm. The CD data below 20 nm could only be correctly measured by cross-section SEM. Process window of thermal reflow for the aforementioned initial CDs is 155-165oC while that of SAFIER is 150-165oC. It is evident that SAFIER effect is more significant at lower temperatures than thermal reflow effect. There is no shrinkage for both methods for temperatures below 140oC. Initial CD smaller than 100 nm becomes invisible at one time of heating for both methods at temperatures above 170oC and CD shrinkage rates of both methods decrease for more than one time of heating. Thermal reflow has a larger CD shrinkage rate than SAFIER. The dependence of shrinkage rate on initial CD size and spatial frequency is not apparent. CD ceases shrinking for further heatings as the CD reaches an ultimate CD size. The ultimate CD for a larger initial CD is also larger. The smallest shrunk CD is found to be 5.8 nm with aspect ratio over sixty for 50 nm initial designed CD. In general, CD uniformity of SAFIER is better than that of thermal reflow with more heatings. CD non-uniformity decreases with increasing contact hole size for SAFIER while the trend for thermal reflow is reversed. Both thermal reflow and SAFIER have better CD uniformity for isolated contact holes than that of semi-dense ones. More heatings for isolated contact holes using both methods also improve the CD uniformity. The contact holes shrunk by thermal reflow process generally show funnel-shape profiles while those shrunk by SAFIER process show similar profiles with wider undercut. In summary, the thermal reflow process results in better profile while the SAFIER with slower CD shrinkage rate has a better control on CD and uniformity.

6519-168, Poster Session

Study on photochemical analysis system for EUV lithography

A. Sekiguchi, Y. Kono, Y. Minami, M. Kadoi, Litho Tech Japan Co., Ltd. (Japan); T. Kozawa, S. Tagawa, Osaka Univ. (Japan); D. Gustafson, P. A. Blackborow, Energetiq Technology, Inc.

A system for photo-chemical analysis of EUV lithography processes has been developed. This system has consists of 3 units: (1) an exposure that uses the Z-Pinch (Energetiq) EUV Light source (DPP) to carry out a flood exposure, (2) a measurement system RDA [1] for the development rate of photo-resists, and (3) a simulation unit that utilizes PROLITH [2] (KLA-Tencor) to calculate the resist profiles and process latitude using the measured development rate data. With this system, preliminary evaluation of the performance of EUV lithography can be performed without any lithography tool that is capable of imaging and alignment.

Profiles for 20 nm lines are simulated for the KrF resist (TDUR manufactured by TOK) and the EB resist (ZEP-520 manufactured by Nippon Zeon), Both resist that has sensitivity at the 13.5nm wavelength.

The simulation successfully predicts the resist behavior. Thus it is confirmed that the system enables efficient evaluation of the performance of EUV lithography processes.

6519-169, Poster Session

Improved lithographic performance for EUVL-resists based on activation energy for hydroxy phenol and hydrocarbone acrylate type polymer

S. Kim, Dongjin Semichem. Co. Ltd. (South Korea)

As the feature size is smaller, it is difficult for the lithography progress to keep pace with the acceleration of design rule shrinkage and high integration of memory device.

Extreme Ultra Violet Lithography (EUVL) is the preferred solution for the 32nm node.

In this paper, we have synthesized two types of polymer. One is based on Hydroxy phenol for KrF polymer, the other is based on hydrocarbon acrylate type polymer for ArF. Also we have synthesized the various polymers for depends on activation energy.

In this experiment, we are focus on four goals.

First focus is evaluation of the resist resolution, Second is resist LER(Line Edge Roughness), Third is resist sensitivity and the forth is Out-gassing materials.

This EUVL resist showed resolution to 35nm, photo-speed of 10.2mJ/cm2.

This resist also had minimal LER, 3σ, of 3.5nm for HP40nm 1:1 line and space.

6519-170, Poster Session

Photoresist dissolution into a CO2 compatible salt and CO2 solution: rate dependence on processing conditions

A. E. Zweber, North Carolina State Univ.; M. I. Wagner, Micell Technologies, Inc.; R. G. Carbonell, North Carolina State Univ.

Image collapse and line width roughness (LWR) are two current challenges in lithography which become more pressing as the aspect ratio and spacing of critical dimensions become smaller. One method reducing both problems is the direct development of extreme ultraviolet (EUV) commercial photoresists with supercritical carbon dioxide (scCO2) and a carbon dioxide compatible salt (CCS).[1-4] The CCS, a fluorinated ammonium salt, associates with the photoresist Bronsted acid groups in the unexposed regions compelling it to dissolve in the scCO2 rich phase resulting in a negative tone development. The low surface tension of CO2 reduces image collapse, and the plasticization of the polymer infused with scCO2 reduces LWR.

A high pressure quartz crystal microbalance (QCM) has been used to study a few mechanistic features of the CCS/scCO2 development process, including effects of temperature, pressure, and density.[5] This paper will further the knowledge of the CCS/scCO2 development by addressing how using a CO2 dry before development and not applying a HMDS layer affect the photoresist removal rate and the completeness of photoresist removal.

The typical QCM experiments quantifying the removal rate of photoresist into the CCS/scCO2 phase began with a spin coated commercial EUV photoresist film baked at 110oC. In these kinetic studies, a HMDS layer between the crystal substrate and photoresist film was not applied to simplify the experiment. The film was placed into a high pressure QCM cell, and CO2 was added to the cell up to the experimental pressure. At this point, the film was dried with 400 ml of CO2 at 30 ml/min to remove any residual solvent and subsequently improve reproducibility. Then the CCS/scCO2 solution was injected displacing the CO2, and the unexposed photoresist film dissolved into the scCO2-rich phase. In a separate experiment, wafer coupons coated with a HMDS layer and the same photoresist were developed. The wafer coupons were sealed into a high pressure cell already containing the CCS, pressurized with CO2 to the experimental pressure, and then depressurized after a set amount of time.

Two differences were apparent between the QCM and the wafer coupon experiments. First, the QCM resulting photoresist removal rates were slower than the removal rates of wafer coupons. Second, atomic force microscopy (AFM) showed that particles remained on the QCM substrate after the bulk of the photoresist was removed, resulting in a different, slower removal rate regime. With CCS/scCO2 development being carried out on the wafer coupons, no particles remained on the surface. It is believed that both the CO2 dry and lack of a HMDS layer play a role in the particle formation during the QCM studies. The effect of both a HMDS layer and a CO2 dry on photoresist removal rate will be investigated for temperatures 35oC - 50oC and pressures 3500 psig - 5000 psig and analyzed for remaining particles with AFM.

(1) Wagner, M.; DeYoung, J. U.S. Pat. Ser. No. 11/088171, March 23, 2005.

(2) Wagner, M., et al. Proc. SPIE; San Jose, CA, 2006.

(3) Wagner, M., et al. Proc. SPIE; San Jose, CA, 2006.

(4) DeYoung, J., et al. Proc. SPIE; San Jose, CA, 2006.

(5) Zweber, A. E., Carbonell, R. G. Proc. SPIE; San Jose, CA, 2006.

6519-171, Poster Session

Exposure of molecular glass resist by e-beam and EUVIL

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Most current EUV resists were derived from conventional 248 and 193nm resist platforms. They have shown nice results with best resolution down to the 30nm range. However, the goal for the introduction of the EUV lithography, 22nm, appears difficult to reach. Furthermore, the minimum achievable LER is 4nm, whilst 1.2nm is required by the ITRS roadmap. The sensitivity target, that has been relaxed to 10mJ/cm2, is still rather high and current resists give their best performances for formulations requiring higher doses. It has become apparent that a new resist platform will be required to meet the ITRS requirements. One such are molecular glasses. These utilise substantially smaller molecules than typical polymeric resists, and are generally monodispersed (as opposed to the typical polymer weight distribution) which should allow smaller CD and lower LER.

The application of molecular resists to EUV lithography has not been significantly examined and initially it is necessary to show that they are capable of out-performing conventional materials. This work will show the results of exposure of several molecular glass resists by e-beam at CEA-Leti and by EUV interference lithography at the Paul Scherrer Institut.

Functionalized polycarbocycle molecular materials have been synthesized and proposed as basic components of EUV resist formulations by the Demokritos group, in collaboration with Intel researchers [1]. These molecules comprise a polycarbocycle core that provides high etch resistance and moderate absorbance at the EUV region. Similar molecules had been proposed before as etch resistance additives [2]. In addition, the other necessary functionalities, i.e. acid sensitive groups and hydrophilic groups have been incorporated to the main core. Fig.1 shows such a molecular architecture. The small size of these molecules is expected to result in low line-edge roughness (LER) (M17 in Fig. 1 has a radius of approximately 1nm).

Positive chemically amplified resist formulations with excellent film formation properties have been developed. Thermal stability even at temperatures close to 200oC and proper glass transition temperatures, i.e. higher than 50oC, allow thermal processing at temperatures from 50 to 130o C. On the other hand standard (0.26 N) TMAH developers are used.

EUV-IL exposures show 50nm (fig. 2) dense lines and 45nm dense lines but with poor patterning characteristics. Since these were the very first exposures, resolution and profile improvements are expected by modifying either the formulation or the process conditions.

A negative tone resist based on the acid catalysed crosslinking of triphenylene derivatives with epoxy functionality together with hydroxy terminated triphenylene derivatives, [3] and developed by the Uni of Birmingham group, has also been tested. The derivatives are shown in fig. 3. An ionic photoacid generator was used to sensitize the material.

[1] D. Niakoula, P. Argitis, I. Raptis, E. Gogolides, V.P. Vidali, D.R. Gautam, E. A. Couladouros, W. Yueh, J. Roberts, R. Meagley, EUVL Symposium 2005, San Diego, USA. ; MNE 2005, Vienna, Austria.

[2] E. Gogolides, P. Argitis, E. A. Couladouros, V. P. Vidali, et al, J. Vac. Sci. Technol. B 21(1), 141 (2003).

[3] A.P.G. Robinson, H.M. Zaid, F.P. Gibbons, R.E. Palmer, M. Manickam, J.A. Preece, R. Brainard, T. Zampini and K. O'Connell, Microelec. Eng., 83, 1115 (2006).

This work has been carried out in the framework of the More Moore project financed by the European Community

6519-177, Poster Session

Sub-10-nm structures written in ultra-thin HSQ resist layer, using electron-beam lithography

A. Grigorescu, M. van der Krogt, C. Hagen, P. Kruit, Technische Univ. Delft (Netherlands)

Hydrogen Silsesquioxane (HSQ) is known as a high resolution negative-tone inorganic electron beam resist. Minimum line edge roughness, high etch selectivity and the small molecular size make HSQ a very good candidate for high-resolution electron beam lithography [1,2]. All the experiments reported in the HSQ literature were made using 50-100 nm resist layers and by using the standard tetra methyl ammonium hydroxide (TMAH) based developer. We believe that thinner resist layers and a better optimisation of the development process may influence the ultimate resolution than can be achieved by using HSQ (Flowable Oxide, FOx-12 from Dow Corning) as high resolution electron beam resist. We report here electron beam exposure experiments on ultra-thin resist layers. Silicon wafers were cleaned with 100% fuming nitric acid and then baked at 200 °C for 2 min to remove residual moisture. Next, samples were spin coated with a solution of 1:5 FOx-12:MIBK, respectively 1:10 FOx-12:MIBK at a speed of 3000 rpm for 60 s. The HSQ layer was prebaked on hotplates for 40 min at 90 °C in order to get high contrast and a good reproducibility [3]. The thickness of the resulting HSQ, ranging from 10 nm to 20 nm, was measured with an ellipsometer. The wafers were exposed in a Vistec Electron Beam Pattern Generator (EBPG 5000+) at 100 kV with an aperture of 300 μm (201 pA beam current, 2 nm estimated spot size). The test patterns consisted of dots and lines with different widths that were written with different pitches and various exposures doses. The structures were all written with a fixed beam step size (the distance between two adjacent exposures) of 1.25 nm. Depending on the designed linewidth, an exposure is performed by linearly scanning the beam once (1-exel line) or by scanning n adjacent lines (n-exel line). The samples were developed by manual immersion at 20°C in TMAH developer (MF-322 from Rohm and Haas) for 60 s (for dots) or in potassium hydroxide (KOH) aqueous solution (AZ 400K from Clariant) for 15 s (for the lines). Namatsu [4] suggested that a higher contrast can be obtained by using KOH-based developer instead of conventional TMAH. Exposed substrates were then rinsed in 1:9 developer:water for 10 s, rinsed in demineralised water for another 10 s and blown dry with nitrogen. Following the development process, resist linewidth was measured and imaged using a Nova Scanning Electron Microscope. The best results are shown in the photos below. Using 100 keV electron beam lithography, we report the achievement of 6 nm dots (see Figure 1) with a pitch of 125 nm in the x direction and 100 nm in the y direction in 20 nm HSQ layer on silicon substrates. Although the pitch is relatively large, this result is important because these are the smallest dots ever written in HSQ. We also investigated the effect of a potassium hydroxide (KOH) aqueous solution developer on the ultimate resolution. The result of the first experiments in a 10 nm thick HSQ layer using a development time of 15 s is shown in Figure 2. From this figure it is seen that the linewidth is 7 nm and the pitch is 20 nm. This is the smallest pitch (20 nm) achieved to date using HSQ resist. We believe that by adjusting the development process (e.g. shorter development time, different developers) and by refining the exposures strategies, the ultimate resolution than can be achieved with HSQ, can be improved.

The next step is to write dense lines and spaces of 6 nm or smaller and isolated structures with a size smaller than 6 nm.

6519-192, Poster Session

Phenolic molecular glasses as resists for next-generation lithography

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In this contribution, we present our effort in designing new chemically amplified molecular glass resists based on bulky phenol derivatives. In contrast to traditional polymeric materials, they possess the advantages to be uniform in size and composition. Various compounds comprising rigid aromatic moieties were synthesized in our laboratories and evaluated for electron beam and Extreme UV lithography (* = 13.4 nm). Several molecular glass structures will be discussed. In particular, we introduce the use of tert-butoxycarbonyl protected 'noria-Boc' molecules (Figure 1) as promising photoresists for emerging next generation lithographic techniques. They are synthesized from the condensation reaction of resorcinol with 1,5-pentanedial.1 After protection with tert-butyl dicarbonate, this cyclic, bulky and amorphous material is characterized by a high glass transition temperature (Tg \> 120 °C) and excellent film formation properties. A post-exposure bake temperature of 140°C is necessary to ensure complete development of the exposed areas and produce sub-100 nm lines as it is shown in Figure 2. The lithographic performances of noria molecules protected with acetal and acrylate are subject to further investigations.

6519-172, Poster Session

Study on diazonaphthoquinone positive photoresist composition for LCD

Y. Zou, F. Zhou, Beijing Normal Univ. (China)

We report on a study of the diazonaphthoquinone positive photoresistcomposition for LCD. LCD is one type of flat panel display and is employedextensively in applications ranging from small-scale products, such as a phygmomanometer, to various portable electronic devices such as PDAs andnotebooks. Photoresist is the important material used for the electrode of LCD.LCD photoresist consists of photoactive compounds, binder resin and organic solvent. We first study the esterification of 3,4,5-trihydroxybenzophenone, 2, 2¡¯, 4,4¡¯-tetrahydroxybenzophenone and 1,2 - diazonaphthoquinone- 4-or- 5 ¨Csulfonyl chloride, then the conventional photoactive compounds were synthesized. The properties of the conventional photoresist composition were also studied. Ourwork focuses on exploring new type of photoactive compounds. We prepared the new phenol compounds: 7, 8-dihydroxy-4-methylcoumarin, 6, 7-dihydroxy-3, 3-diphenyl-3H-benzenefuran-2-ketone, and then reacted with 1, 2£°(c)diazonaphthoquinone-4-or-5- sulfonyl chloride, so the new photoactive compounds were obtained. The new photoactive compounds were used with PGMEA as organic solvent and the novolac resin as binder resin, then the photoresist composition wasprepared. The photoresist composition was coated on the pretreated ITO filmsand ITO glasses.After the prebake, exposure, developing, hard bake, a desired pattern was produced. The properties of photoresist composition, for example: photosensitivity, resolution and developing performance were good.

In the paper,the synthesis method of the new phenol compounds and photoactive compounds, the evaluation method of the photosensitivity, resolution and developing performance were introduced in detail; the token of esterification productions, the esterification condition, the relation of BP ratio with photosensitivity and developing performance were all discussed. The images of the photoresists from SEM and electron microscope were also offered in this paper. Finally,we have the conclusions: The 14 kinds of photoactive compounds that we have synthesized were able to applying in the LCD photoresist; the patterns of photoresist composition were good and the photosensitivity can reach to 40.5mJ.cm-2£¬the resolution can be 1õÌm.

6519-173, Poster Session

Characterization of a high-photospeed positive thick photoresist for lead-free solder electroplating

W. W. Flack, H. T. Nguyen, Ultratech, Inc.; K. Saito, K. Misumi, Tokyo Ohka Kogyo Co., Ltd. (Japan)

The introduction of lead free solder (SnAg) electroplating for advanced packaging applications has created new challenges for thick photoresist processes. Dry film laminate resist materials do not provide sufficient resolution or process control for the smaller bump diameters used with advanced design rules. The traditional positive tone DNQ-Novolak photoresists require large exposure doses and long processing times that are unacceptable for the total cost of ownership (COO) of the lithography cell in a manufacturing environment. Standard chemically amplified positive photoresists have interactions between the PAG and Cu or Cu2O at the soft bake step which makes it impossible to obtain sufficient pattern fidelity for electroplating lead free solder on copper seed layer substrates.

This study will characterize a novel positive tone, chemically amplified resist (TOK PC-0059B PM) that can be single coated up to 100 microns thick for lead free solder electroplating. The PAG in the photoresist has been formulated to prevent any interaction with Cu or Cu2O. This photoresist exhibits extremely high photospeed, excellent pattern resolution and ease of stripability after electroplating.

The lithographic performance of the thick positive resist will be optimized on 300mm wafers using a broad band, low numerical stepper. Enhanced process latitude and very high photospeeds will be demonstrated for thicknesses up to 100 microns. Cross sectional SEM analysis, process linearity, and electroplating performance are used to establish the lithographic capabilities.

6519-174, Poster Session

Performance of a 55-micron copper pillar bump process using a positive thick chemically amplified photoresist

W. W. Flack, Ultratech, Inc.; D. Crapse, Motorola, Inc.; E. S. Capsuto, Shin-EtsuMicroSi, Inc.; H. T. Nguyen, J. Buchanan, Ultratech, Inc.

As pin counts and interconnection densities increase there is growing interest in copper pillar bumps for flip chip packaging. The use of copper pillars provides the advantage of large standoff height while using smaller bump diameters with improved critical dimension control. The fabrication of copper pillar bumps requires the use of a very thick resist layer for the copper electroplating. This resist material must be capable of coating, exposing, developing, electroplating and stripping with conventional equipment and standard ancillary process chemicals. In addition, resist sensitivity and process bake and development times are critical to minimize the cost of ownership of the lithography cell. For the electroplating process the resist profile, plating durability and stripability are important considerations.

This study will characterize a novel photosensitive resist (ShinEtsu SIPR 7123) for a single coat, 55 micron thick copper process for a manufacturing environment. This resist has been formulated for enhanced photospeed, ease of stripability and has additives to eliminate the cracking often seen with very thick films. In addition, various process constraints will be studied due to strict equipment limitations for integration into an existing production line.

The lithographic performance of the thick positive resist will be optimized using a broad band, low numerical stepper. Enhanced process flexibility and productivity will be shown in regards to developer type and no wait times between process steps. Results will show excellent adhesion to copper with no surface treatment and no resist popping during exposure or post exposure bake (PEB). For increased productivity a no PEB process will also be studied. Cross sectional SEM analysis, process linearity, and plating performance are used to establish the lithographic capabilities.

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6519-176, Poster Session

The use of black pigment polyimide, DARC300, as a light absorber on an optical sensor

K. A. Gehoski, Motorola, Inc.; P. Holm, Motorola; K. Boggess, Motorola, Inc.; C. Scott, Brewer Science

In the design and fabrication of arrayed opto-electronic detection devices, it is critical to provide optical isolation between the individual array cells to prevent optical crosstalk between channels and contribution from stray light that would otherwise result in degraded signal-to-noise performance. To accomplish this, the light incident between the cells' optical apertures and around the periphery of the array must be blocked from entering the active semiconductor layers. One approach has been to use an opaque layer of metal, but this can lead to reflections and light trapping and ultimate absorption of this stray light in device active regions. Another approach is to use an absorbing material to block stray light. DARC300, a registered trademark of Brewer Science, is an optically absorbing, photo-definable polyimide designed for exactly this purpose. Presented here is a comparison between aluminum and DARC300 blocking layers, including a review of the process development and issues addressed along the way. The most prevalent issues with the DARC300 were the remnants of black pigments after develop, and the insufficiently developed features. Figure 1 depicts an SEM micrograph of a feature with sprinkles of pigment remaining. Figure 2 shows insufficient developed features. This paper will present the solutions that were used to overcome these issues. Lastly, performance of detector arrays fabricated without blocking layers and with aluminum and DARC300 blocking layers will be presented.

Conference 6520: Optical Microlithography XX

Tuesday-Friday 27 February-2 March 2007

Part of Proceedings of SPIE Vol. 6520 Optical Microlithography XX

6520-01, Session 1

Marching of the microlithography horses: electron, ion, and photon: past, present, and future

B. J. Lin, Taiwan Semiconductor Manufacturing Co., Ltd. (Taiwan)

No abstract available

6520-02, Session 1

Future directions for CMOS device technology development from a system application perspective

T. H. Ning, IBM Thomas J. Watson Research Ctr.

No abstract available

6520-03, Session 1

Optical lithography: 40 years and holding?

J. H. Bruning, Corning Tropel Corp.

No abstract available

6520-05, Session 2

Defects, overlay, and focus performance improvements with five generations of immersion exposure tools

J. Mulkens, B. Streefkerk, H. C. Jasper, S. Kruijswijk, F. de Jong, L. Levasier, M. Leenders, ASML Netherlands B.V. (Netherlands)

The history of microlithography teaches us that the full integration of new lithography technologies into volume production takes about 10 years. Immersion lithography however, is currently being brought to manufacturing in less than 5 years. The early availability of immersion exposure tools has been one of the key enablers for this fast introduction. These learning done with these early immersion exposure tools resulted in fast and gradual improvements of the immersion technology.

Since 2003 we have been developing and shipping four generations of immersion scanners with maximum NA starting from 0.75 up to 1.2. In 2007 a fifth generation tool with 1.35 NA will be shipped. Over time we have been improving the specific immersion modules in the scanners, resulting into improvements in defects, overlay and productivity. In this paper we will review the learning we did on these critical performance items. It will be discussed how improvements in water containment and improvements in immersion resist processing lowered the defect numbers to levels as required for volume manufacturing. On overlay and focus performance it will be discussed how the thermal management of immersion water and wafer can bring overlay down to numbers comparable as seen on dry exposure systems.

Data will be presented representing the performance of more than 20 immersion systems and for a variety of user conditions. An outlook for further improvements will be included.

6520-06, Session 2

Current status of high-index immersion lithography development

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High index immersion lithography is one of the candidates for next generation lithography technology following water immersion lithography. This technology may require only moderate changes of chip making processes and result in lower cost of ownership (CoO) compared with other technologies such as double processing, extreme ultra violet lithography (EUVL), nano-imprinting, and other technologies.

A feasibility study of the optical design for a microlithographic lens with high index fluid and high index lens materials has been performed. As a result of this study, 1.45-1.55NA optics, enabling resolution of 36-37 nm HP, can be achieved with 2nd generation immersion fluids, which have refractive indices of 1.6-1.65, and high index lens material based on a similar design concept to 1.3NA optics for water immersion lithography. Regarding high index lens material, several potential candidates have been reported. We can achieve 1.45NA optics with barium lithium fluoride, which has a refractive index of 1.64, and 1.55 NA optics with lutetium aluminum garnet, which has a refractive index of 2.14.

In order to achieve 32nm half pitch (HP) resolution with a k1 factor of 0.28, 1.7NA optics will be required. Therefore the target refractive index for 3rd generation immersion fluid and resist development will be 1.8 or greater, and potential candidates for high index lens material will be limited to lutetium aluminum garnet.

Several challenges remain for high index immersion lithography, however. The main challenges for microlithographic lens development are the treatment of intrinsic birefringence of the cubic crystal for high index lens materials, such as barium lithium fluoride and lutetium aluminum garnet, and quality improvement of material properties such as transmission and homogeneity. Due to intrinsic birefringence, illumination conditions including polarization arrangements and pattern orientation will be restricted. As a result, limited IC pattern layers can be generated by these optics, or, some modification to the IC pattern is required. Increase of transmission for high index lens materials is a key item to prevent thermal aberration caused by heating through exposure. This effect influences throughput. In addition, techniques to address issues other than immersion optics design, such as fluid handling in the exposure tool, need to be considered.

In this paper, the current status of material development compared with our requirements is discussed considering design feasibility and attainable NA. A risk matrix table is also reviewed.

6520-07, Session 2

Integrating immersion lithography in high-volume manufacturing for the 45-nm node

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Semiconductor manufacturers work hard to shrink critical dimensions in their device architectures and are in the midst of the 45nm node development. Generally, for the 65nm node, critical layers are processed using 193-nm scanners with numerical apertures up to 0.85 and non-immersion technology. It is clear that the capabilities and potential benefits of immersion lithography (at this wavelength and NA) need to be examined, especially as the industry turns its attention towards the 45-nm technology generation. The potential benefits of immersion lithography; increased DOF in the near term and hyper-NA imaging in the next phase, have been widely reported.

The authors previously reported on the ability to "plug and play" an all dry process into an all wet process using 0.85NA imaging systems for 65nm type devices1. Our focus continues to understand further process and tool advancements in defectivity in ArF immersion lithography as compared to dry ArF lithography.2 The defects of dry ArF immersion are the benchmark for comparison to a wet process.

In this paper, we report on the progress of development for the 45nm device level lithography with imaging systems \>1NA at the Crolles 2 Alliance1. Our continued focus is the insertion of an immersion lithography process into an established pilot manufacturing line to support 45nm process development. We will present immersion resist performance, OPC feasibility, process integration, and defectivity

comparisons. Finally, conclusions will be made as to the overall readiness of immersion to support 45nm node processing.

1. Morton et al. 2nd International Symposium on Immersion Lithography

2. Warrick et al. Proc SPIE 6154, 07

6520-08, Session 2

Performance of immersion lithography for 45-nm node CMOS and ultra-high density SRAM with 0.25μm2

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Immersion lithography is needed to shrink the design rule. The trend of design rule for 45nm-node shows that the metal half pitch is 65nm and the area of ultra-high density SARM(UHD-SRAM) is about 0.250μm^2. Especially, the immersion lithography is indispensable to resolve the contact hole patterns. The minimum pitch of hole patterns is required by 140nm for 45nm-mode. Dry lithography extends the resolution limit of hole pattern down to 160nm-pitch by using high-NA tool and high-resolution resist.

In this presentation, we will show the experimental results of the immersion lithography for 45nm-node CMOS and UHD-SRAM. By using immersion lithography, the resolution of the hole patterns is much enhanced as shown in Fig.1. Although we have adopted the alternating phase shift mask (Alt-PSM) as gate lithography due to the resolution advantage from 65nm-node, we will reexamine the advantage of the Alt-PSM regarding resolution, LER, design restriction and cost. Also, we have kept adopting the cutting layer for straight gate in the UHD-SRAM cell in order to shrink the distance of tip-to-tip.

6520-09, Session 2

Benefit of ArF immersion lithography in 55-nm logic device manufacturing

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The ArF immersion lithography has been positioned as the post ArF dry lithography for the 65nm node and below. Immersion technology has almost reached a mature status as immersion exposure tools with \>1.0NA for mass production are shipping in volume. Although immersion technology is highly beneficial for imaging it puts new challenges on the tool and process design due to the immersion water column placed in between the projection optics and the wafer surface. In this study, we will address the issues and the current status in ArF immersion technology, and also discuss pros and cons on introducing immersion technology especially with lower NA (<1.0NA) through comparison of impact on various lithographic parameters between dry and wet lithography.

The biggest concerns in ArF immersion are mainly defectivity, overlay and focus control. As for defectivity control, there are several concerns such as tool contamination and/or process defects due to leaching from resist or top coat materials, and patterned defects or resist profile degradations due to water droplets. The improved immersion hood and/or hydrophobic top coat materials and other measures have been implemented for those issues and are now under control. As for overlay and focus control, the exposure field is in direct contact with the immersion water. Water evaporation during exposure introduces temperature gradients resulting in overlay and focus control degradation. Different countermeasures have been implemented in the ASML immersion exposure tools to overcome these immersion induced effects. Current tool performance has confirmed that these countermeasures result in a significant improvement in overlay and focus control accuracy.

In case of imaging, it is well-known that the DOF is significantly improved by immersion. In recent years the use of OPC in ASIC device manufacturing has become an ever-growing burden. It is a big advantage of immersion that it can refrain from using strong RET thanks to the larger DOF. On the other hand MEEF and OPE will remain the same or even improve due to higher contrast at the edges of the process window. Furthermore, the use of polarization will improve the contrast even more, while the sensitivity for IPS (Intensity in polarization state) variation decreases significantly with respect to dry imaging.

Although it is a disadvantage in cost to use a top coat and dry resist combination in immersion, the CD control is improved because the resist-BARC thickness control margin becomes bigger as the swing curve is reduced by introducing a top coat.

6520-10, Session 3

Snell or Fresnel: the influence of material index on hyper-NA lithography

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As immersion lithography is extended to ever increasing resolution, the resulting propagation angles in the materials involved become closer to grazing than to normal incidence. The classical laws of refraction and reflection cannot be used with either assumption, however, as a collection of angles may exist across the entire range. Fresenel reflection at these angles becomes large enough that small disparities in their refractive indices at material interfaces may lead to adverse effects. As an example, when water is used at numerical apertures approaching its refractive index, imaging looses from small index mismatches to optics or photoresist, and the resulting reflection, are greater than the constraints imposed by refraction or absorption. This will limit the maximum NA value allowed by any given material to values sufficiently lower than their refractive index. We will show several examples with a variaty of fluids and materials with imaging to 25nm.

Additionally, lithographers have grown accustom to expanding the application of Snell's Law to materials with low absorption, assuming that the contribution of the imaginary component of the refractive index is negligible. This is not the case for photoresists, fluids, or glasses, which can not strictly be considered as non-absorbing media. (Photoresist of course relies on absorption for photochemistry). We have expanded Snell's Law for absorbing media, which has some very interesting consequences. We will show that the there is no limit on the numerical aperture through a material, so long as its extinction coefficient is not zero. The relationship that lithographers have been using recently where NA< min[n(glass), n(fluid), n(resist)] will be shown to be inadequate and imaging at numerical apertures up to 2.0 will be demonstrated using materials with significantly lower (real) refractive index values.

6520-11, Session 3

Hyper-NA polarized imaging of 45-nm DRAM

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Hyper NA (NA\>1) immersion lithography system made a successful debut in the field owing to the significant progresses made in immersion technology and lens design. As is well known for long time, increased NA is not always good because depth of focus reduction and poorer image construction comes straightforward from that. However, those issues engaged in hyper NA imaging seemed to be overcome simply by the support of high refractive index of water and polarized illumination. As a result, lower k1 patterning might be feasible with this hyper NA immersion system than dry tools.

In this paper, we will present experimental results on 45nm node patterning of DRAM and some technical issues of polarized illumination in hyper NA imaging.

First, practical k1 limit of 1.2NA ArF immersion system is investigated through experiment. Process window and mask error enhancement factors are compared according to the change of design rules, i.e., different k1 levels. Reasonable process window and MEEF value of around 3 are achieved in DRAM gate and isolation pattern even at 0.28 k1 regime. It was obvious that this lowered k1 was realized by the help

of polarized illumination when the results were compared with that of 60nm patterning at 0.93NA tool - corresponding k1 is 0.29 - without polarized illumination.

Then consideration about degree of polarization state must come next to the benefit of polarized illumination. Input polarization state is changed by birefringence of lens or mask materials but it is very difficult to correlate the birefringence level and critical dimension of patterns experimentally. Indirect test method was contrived to measure the effect of polarization state variation on DICD and then the allowed birefringence level is deduced numerically.

Because of increased NA, the larger angular span of diffraction spectrum is engaged in hyper NA imaging, hence the forbidden pitch and ID bias behaviors are examined with different polarization settings.

6520-12, Session 3

Pushing the boundary: low-k1 extension by polarized illumination

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The introduction of polarized illumination has enabled the extension of low-k1 processes to even smaller feature sizes. Previously, it has been demonstrated by simulations and early exposure results that properly polarized illumination leads to an increase of contrast and exposure latitude, resulting in reduced MEEF and better CD control. The gain of polarization is most pronounced in the hyper-NA regime of high-end immersion tools, but also 'dry' high-NA scanners benefit significantly from polarized illumination.

In production-worthy scanner tools, polarized lithography must be fully compatible with all requirements for a volume production tool: full throughput, overlay and focus control, flexibility and ease-of-use are essential features. This is realized by employing polarization-conserving optics, and by automated in-line metrology to optimize and control the system for any selected polarization state.

In this paper, experimental results will be shown demonstrating the gains of using polarized illumination on high- and hyper-NA exposure tools, of both dry and immersion types. The various imaging relevant parameters (process window, MEEF, EL, DOF, LER) will be addressed in relation to the use of polarization exposure conditions and compared to simulations. Finally, system control and in-line metrology will be discussed.

6520-13, Session 3

Modeling polarization for hyper-NA lithography tools and masks

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The advent of optical immersion lithography has dissolved the NA=1 barrier and is carving novel pathways for advanced semiconductor manufacturing. Nowadays hyper-NA (NA \>1) immersion lithography is considered to be a strong contender for device manufacturing at the 45nm and 32nm nodes. The use of water immersion enables a further increase in resolution and is strongly competing with the option of an early wavelength transition to EUV.

Modeling of non-paraxial lithographic imaging has steadily evolved to keep pace with the dramatic increase in NA's over the last decade. For NA's lower than about 0.6, light has been treated as an entirely scalar quantity. For the NA range 0.6<NA<0.9, vector imaging with idealized polarization has been applied, including thin film interference effects. However in this regime the reticle was still treated as a thin mask and the projection lens was considered to be scalar in nature. For the high-NA (NA\>0.9) and hyper-NA (NA\>1.0) regimes, the polarization properties of all components of the optical chain need to be addressed in detail (e.g. non-ideal source polarization distributions, polarization specific interactions with 3D mask topography, actual reticle blank birefringence, polarization aberrations of projection lenses, and polarization dependent resist film stacks).

In this paper we present a comprehensive modeling study of polarization effects from exposure tool and mask, with strong emphasis on the impact of the Jones Matrix for the projection lens, as well as source and mask polarization errors on realistic 45nm and 32nm node process levels.

The polarization properties of projection lenses can be described by so-called Jones Matrix Pupils, or Jones Matrices for short. We will discuss the theoretical properties of these Jones Matrices as well as optical metrology to measure them. Effects of the systematic and random components of Jones Matrices are studied in the context of imaging simulations on realistic process levels, in order to assess their impact on Across-Chip Line-width Variations (ACLV). We discuss the relation between the Jones Matrix and OPC-model-build in terms of the effectiveness of the matrix, kernel symmetry requirements, and run-time impact. We report on a preliminary verification on commercial OPC software that includes the Jones Matrix for OPC model-build and improved model robustness is observed (Figure 1).

For accurate modeling it is also very important to synchronize the polarization conventions of lens design codes and lithographic simulation software. Zeiss and IBM have co-developed a Jones matrix convention to provide a clear and unambiguous basis for defining vector fields in the plane-wave components of projected images. Several commercial lithography codes have now implemented Jones Pupil capability based on this convention, and all have succeeded in reproducing the imaging properties of a test lens based solely on receipt of its Jones matrix datafile.

Source polarization is usually specified by 3 physical terms (intensity, rotation & ellipticity) but lithographers sometimes prefer to use a single metric like Intensity in Preferred State (IPS), in order to simplify lithographic analysis. We have applied this approach in analyzing the impact of source polarization and mask blank birefringence (to set requirements for mask birefringence), and have verified the approach's effectiveness. Finally we also address polarization effects from the pellicle (apodization), mask topography induced polarization change, and the flare dependency on the use of polarized light.

6520-14, Session 3

Polarization-dependent proximity effects

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Optical imaging of IC critical designs is impacted by optical proximity effects originating from finite numerical aperture of projection lenses used in modern projectors. The OPE's occur because of filtering of pattern diffraction orders falling outside of the lens band pass.

The projection lenses are also subject to two sets of key phenomena impacting image formation. One set of phenomena is phase retardations of various diffraction orders reaching the image plane. The net result of such retardations are image aberrations. The lithography engineering community has been treating lens aberrations as a sum of Zernike polynomials representing wavefront aberration at the lens pupil. It constitutes scalar treatment of lens aberrations. This treatment was effective when depolarization effects in the projection lenses were negligible.

The second set of key phenomena impacting image formation is polarization transformations at the projection lens components. The net result of such phenomena is diffraction order polarization transformations. These polarization impacts can be treated by Jones polarization transformations, constituting vectorial treatment of lens aberrations. The vectorial treatment of lens aberration becomes essential for hyper-NA projection systems.

As the IC industry adopts hyper-NA imaging systems, the important question facing the photolithography community becomes: what are the ramifications of the transition from scalar to vectorial treatments of projection lenses? To answer this question, we analyze optical proximity responses of hyper-NA lens with residual, by design, aberration content. We first studied a set of OPE signatures under

scalar aberration treatment represented by conventional, Zernike polynomial series. We then generated a set of corresponding OPE signatures under vectorial, Jones aberration treatment corresponding to the initial, scalar aberration set. We compare the two sets of OPE signatures and note the image formation consequences of lens vectorization.

Development of hyper-NA scanners created a situation where conventional, scalar treatments of projection lenses do not capture the full range of phenomena impacting image formation. Analysis of hyper-NA lenses requires vectorial methodologies. We present both lens treatments and compare the scalar impacts on OPE's to their vectorial counterparts. We highlight the consequences of lens vectorization for the optical proximity effects.

6520-15, Session 3

The impact of projection lens polarization properties on lithographic process at hyper-NA

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The continuous implementation of novel technological advances in optical lithography is pushing the technology to ever smaller feature sizes. For instance it is now well recognized that the 45nm node will be realized using state-of-the-art ArF (193nm) hyper-NA immersion-lithography. Nevertheless, a substantial effort will be necessary to make imaging enhancement techniques like polarized illumination or sophisticated illumination modes routinely available for production environments.

In order to support these trends, more stringent demands are being placed on the lithographic optics. With introduction of numerical apertures \> 1 and polarized illumination, a clear description and control of polarization throughout the complete optical system is required. Although this includes the illumination unit as well as the projection lens, we limit ourselves to a treatment of the latter module. In this paper we present a comprehensive method to deduce the imaging impact of polarization properties typical for projection lenses. In extension to phase-deviations (i.e. conventional scalar wavefront) across the pupil, we explicitly treat a 2x2 complex Jones-Matrix for each point in the pupil. Although such a pupil of Jones-Matrices (short: Jones-Pupil) allows a full and accurate description of the physical imaging, it seems to lack transparency towards direct visualization of relevant imaging parameters. The presented analysis uses general lithographic assumptions and elaborates a set of fundamental rules-of-thumb, allowing an easy access to the complex information stored in a Jones-Pupil. We give methods to visualize lithographically relevant aspects of the Jones-Pupil. The impact of different types of typical Jones-Pupil errors - such as birefringence fingerprints, apodization and dichroism - under low-k1 imaging conditions is examined. The presented method allows a fast route from Jones-Pupils to the imaging performance of critical applications. This feature is crucial for lens-manufacturers in building and optimizing the best optical system, as well as for the semiconductor device manufacturer in defining the optimum lithographic process conditions.

6520-16, Session 4

Pitch doubling through dual-patterning lithography challenges in integration and litho budgets

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Rapid expansion in mobile memory devices requires lithographic patterning capability that is beyond resolution of ArF water-based immersion tools. In parallel, EUV and high-index fluid-based immersion ArF lithography are still under development and is questionable whether they will be ready to timely meet resolution needs from most aggressive memory designs. As a consequence, dual patterning to double the pitch appears to be an option calling for more and more consideration.

Extending lithography capability beyond classical resolution capability through Double Patterning has been demonstrated in earlier work. However, there are still a good number of critical aspects in DP technology that have to addressed and solved before it can become a real manufacturing solution. Dual patterning decomposition with associated processing steps could be done through a "negative" or "positive" process, where process tone is function of mask polarity. While negative and positive tone lithography processes are clearly defined, the associated patterning steps have multiple implementation options, presenting a range of different requirements, capabilities and limitations to meet resolution and control budgets. In this work, we explore various processing options with respect to their integration challenges and associated effects on scanner CDU and overlay budget. We illustrate why dual patterning lithography necessitates more than optimization of P/4 process latitudes for either positive or negative options and demonstrate the need for an integrated approach where full process complexity has direct consequences on CDU control. We contrast process options to extract budget requirements for DP lithography to build a new model that calculates CDU budget components defining a CD from its edges, which are created from separate patterning steps. The model accounts for contributions coming from outside scanner world, like reticle registration, which have a clear effect on pattern edges . Special attention is given to registration error sources captured from mask's correlated spatial distribution maps of CD and registration, which are functions of mask type and process characteristics.

We will present experimental results demonstrating process capability to double the pitch for 1D patterns, to a final k1 of 0.16, on both dry and wet lithography. Results are used to calibrate the CDU model and to extract realistic requirements for DP process budgets as function of process option. Experimental overlay results support budget prediction showing capability to meet double patterning overlay. Results increase the confidence in acceptance of double patterning solution for resolution requirements going below 0.20k1.

6520-17, Session 4

Issues and challenges of double patterning lithography in DRAM

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To achieve the patterning capability of sub-40nm, high index fluids for immersion have been developed and a lot of researches are performed in EUV sources and resists. Also, many lithography engineers are thinking of double patterning lithography as another candidate. Last year we presented the several issues in double patterning lithography for application into real flash gate layer, which mainly consist of 1-dimensional patterns. In this flash application, the layout could be successfully decomposed by either ways of positive or negative tone. So, layout decomposition method seemed to be the matter of choice and the overlay controllability and productivity seemed to be the only issues. But for the application into DRAM device, the situation changes a little. For example, because some layouts contain 2-dimensional pattern like isolation pattern, the decomposition can be restricted by small process margin and poor pattern fidelity. In this paper, we select the decomposition method for each layers of 37nm half-pitched DRAM device according to their specific pattern shapes and directions. We will present the result of each step in double patterning processes with 0.93NA 193nm system, where k1 value shows about 0.23 even with the 1.2NA system. By inspection of block edges, it will be shown how the boundaries can be formed by double patterning lithography. And we will present the results of DRAM core region by double patterning method, where the patterns are so complicated that even triple patterning is mentioned. In addition to the well known overlay issue for double patterning, etching is one of challenges in 37nm double patterning lithography. Because of high aspect ratio in etching, slight CD change in adjacent pattern results in serious pattern anomaly due to the micro loading effect.

6520-18, Session 4

Manufacturability issues with double patterning for 50-nm half-pitch single damascene applications using Relacs shrink and corresponding OPC

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In order to obtain very small features, double patterning (DP) techniques gain interest. The smallest pitch for each litho step becomes twice as large, resulting in larger process windows. Drawbacks of double patterning are sensitivity to LER and overlay errors. Furthermore, the pitch is increased, but the pattern itself remains very narrow. Hence, for resist trenches, shrink techniques are interesting, realizing narrow trenches with larger DOF and less LER. Since all shrink techniques have their own proximity properties, they will require an adjusted OPC calculation, taking into account proximity effects of both the exposure and the subsequent shrink process.

In this paper, we discuss double patterning work carried out for 50nm half pitch interconnects, using Relacs as shrink technique. Finally (after DP) 50nm trenches with 100nm pitch are required, consequently each exposure has a minimum pitch of 200nm. 25nm shrinkage is obtained by Relacs processing, hence 75nm trenches have to be defined upon exposure.

Illumination conditions.

Based on various criteria, illumination settings are optimized for the trenches with 200nm pitch. These settings result in small process windows for larger pitches, which is solved by adding optimized assist features.

Resist and Relacs processing.

To make Cu interconnects, trenches are etched in the intermetal dielectric (IMD) using a metal hard mask (MHM). The patterning is as follows: litho 1 - MHM etch 1 - litho 2 - MHM etch 2 - IMD etch. Patterning is followed by Cu plating and CMP. For both litho steps, organic BARC is used for reflection control. The second litho step is more difficult than the first one: the topography of the existing MHM patterns (result of first litho step) requires an adjusted BARC/resist process or an additional gap fill material. Moreover, resist poisoning is a serious concern (diffusion from IMD on locations where MHM is removed already), and might require the use of an additional capping layer prior to litho 2. (See Fig. 1)

Relacs processing is optimized with respect to process windows, profile, LER, bake temperature sensitivity and the influence of presence of assist features.

OPC.

Since shrink techniques will change the existing proximity effects (See Fig. 2), an adjusted OPC calculation was required. First, proximity effects caused by exposure and development are calculated ('conventional' model-based OPC). Next, the proximity effects of Relacs shrink are measured. Existing OPC-software packages do not have dedicated models for resist shrink processes. But Relacs proximity is described successfully with a model similar to etch loading effects (See Fig. 3).

Final patterning on wafers.

Moreover, final results on wafers will be discussed, with special attention for critical double patterning topics such as LER and overlay issues. Also, the 'non-conventional' OPC for Relacs shrink will be evaluated. These final conclusions will be based on SEM evaluations but also on electrical characterization of the interconnects after full Cu metallization using single damascene processing.

6520-19, Session 4

The modeling of double exposure and double patterning lithographic processes

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A variety of double exposure (DE) and double patterning (DP) lithography schemes have been proposed. These either result in a common process window which exceeds that possible using a single exposure or allow the realization of a pitch below the Rayleigh barrier (k1 = 0.25).

Whilst several demonstrations of these novel DE/DP techniques have shown proof-of-concept, little has been published documenting the robustness of such exposure schemes to natural fluctuations in process parameters.

In this work, we use simulation to benchmark the improvements in lithographic capabilities achieved by several of these schemes (resolution, process window, MEEF etc), estimate the though-put penalties incurred by the extra process steps and evaluate the sensitivities of the process to the additional degrees of process freedom, i.e. focus and dose errors on both exposures, misalignment between exposures, and second exposure topography effects in the case of double patterning cases.

6520-97, Session 4

Dark-field double-dipole lithography (DDL) for back-end processes

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The back-end metallization of a state-of-the-art CMOS process is the most critical level regarding the final density of the chip. While the gate level requires the most critical emphasis on linewidth control and critical dimension uniformity (CDU) of all lithography steps, the smallest pitch in the process is typically printed on the first metallization level. For this reason, a natural starting point for application of dipole lithography is not the gate level, which in many cases can be printed with quadrupole and other off-axis schemes, but the metal level which has pitches that are typically between 10 and 25 % smaller than the gate pitch. If the same generation tool is used for both gate and metallization levels, then a more aggressive off-axis illumination is needed for the metal level.

In this paper, we investigate the application of double dipole lithography on the first metallization level. The process windows of typical metallization layouts are studied. Using a 1.2 NA lithography system, we investigate the ability of using this lithography technique at pitches approaching 100\, nm.

6520-21, Session 5

Evaluating the performance of a 193-nm hyper-NA immersion scanner using scatterometry

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With the transition of 65nm technology to production and the development of 45nm technology, lithography has become increasingly difficult. ITRS targets for the errors on the critical dimension of microprocessor gates are below 3 nm for the 45-nm node, with a corresponding budget for the metrology errors that is significantly smaller. In addition, the increased complexity of the lithographic processes and tighter error budgets demand more accurate metrology tools for the control of lithography clusters.

In recent years scatterometry has evolved into an accurate, reliable, non-invasive and fast metrology technique. In this study, Normal Incidence Optical Critical Dimension scatterometry (NI-OCD) is used to evaluate the performance of ASML 193-nm hyper-NA immersion scanner XT:1700i. The accuracy of NI-OCD measurements is determined by correlation to CD-SEM measurements. Full-wafer CD metrology is performed to determine intra-die and across-wafer CD uniformity fingerprints. The scatterometry data is also used to characterize a contrast curve or Modulation Transfer Function (MTF) of the scanner. Finally, normal-incidence scatterometry is used to monitor the through-pitch scanner performance for multiple duty cycles.

6520-22, Session 5

Distinguishing dose, focus, and z-blur for lithography characterization and control

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For high-NA, low-k1 lithography, dose, focus and z-blur are the primary sources of variation in resist image formation. Dose is the energy transferred to the resist. Focus is the average z-position of the image plane in the resist film. Z-blur is the z-distribution of the image plane. While these are fixed conditions of the patterning process, a host of tool and process unknowns contribute to their variation in practice. The simultaneous determination of dose, defocus and z-blur proves critical to achieve and sustain patterning fidelity at 65nm and below.

A method to deconvolve dose and defocus from resist profile measurements was previously published [C.P. Ausschnitt & S.Y. Cheng, "Modeling for profile-based process-window metrology", SPIE 5378, p. 38 (2004)]. Here we extend that method to encompass the effects of z-blur as well. We derive a physical model to describe the dependence of pattern dimensions on dose, defocus and z-blur. The coefficients of our model are constants of a given lithographic process. Model inversion applied to dimensional measurements then determines effective dose, defocus and z-blur for wafers patterned with the same process.

In practice, our approach entails the measurement of proximate grating targets of differing dose and focus sensitivity. In our embodiment, the measured attribute of one target is exclusively sensitive to dose, whereas the measured attributes of a second target are distinctly sensitive to defocus and z-blur. On step-and-scan exposure tools, z-blur is varied in a controlled manner by adjusting the across slit tilt of the image plane. Thus, the response of the measured attributes can be characterized through a three-dimensional focus-exposure-tilt matrix (FETM), over which the exposure tool settings are intentionally changed. The model coefficients are determined by a fit to the measured FETM response. The model then fully defines the response for wafers processed under "fixed" dose, focus and z-blur conditions. Model inversion applied to measurements from the same targets on all such wafers enables the simultaneous determination of effective dose, defocus and z-blur at each measurement site.

6520-23, Session 5

Patterning control budgets for 45-nm and 32-nm generations incorporating lithography, design, and RET variations

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An important outcome of the 90nm and 65nm device generations was the realization that new methods for predicting and controlling patterning were required to ensure successful transfer for all design rule compliant features through the required process window. This realization lead to a strong increase in the use of CD-based and process window aware post-OPC verification in production mask tapeouts. Accurate post-OPC verification is a necessity but many patterning issues could have been detected and removed earlier in the product development lifecycle. Of course, the 45nm and 32nm device generations are only expected to further strain the ability of device manufacturers to predict process control requirements, robust patterning design rules and first-time right RET recipes. Therefore, improvements to the traditional process, OPC and design rule prediction/evaluation steps are needed.

In this paper we propose a patterning and CD control prediction methodology which incorporates not only the traditional dose, defocus and mask variation parameters but also implements RET parameter variations such as layout edge discretization, model inaccuracy, metrology error and assist feature placement. This methodology allows a more accurate prediction of process control requirements, worst case CD control layout geometries and RET subsystem accuracy/control requirements. Lithography engineers have long operated with specific (if not always fully understood) dose and focus control success requirements. To efficiently determine real worst design situations, we utilize a new methodology for quickly verifying the RET-ability of a lithography process + design rule set + OPC correction recipe based on coupling iterative layout generation with OPC testing. Our aim in this paper is to provide additional engineering rigor to the traditional experience-based OPC success requirements by looking at the total Litho + RET + metrology patterning problem and analyzing the individual component control needs.

6520-24, Session 5

Control of polarization and apodization with stratified films on photomasks and pellicles for immersion lithography

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Deviations from paraxial image models are significant at numerical apertures planned for immersion lithography. Apodization and rotation of polarization by high numerical optics are well-characterized phenomena [1]. Similar behaviors follow from intrinsic properties of photomask patterns at high spatial frequencies. Diffraction efficiencies differ from values predicted using Kirchhoff boundary conditions, and depend on polarization. Pellicles also apodize diffraction patterns because reflection losses depend on angle of incidence and polarization. These effects are large enough to influence contrast, critical dimension and depth of focus of images thru pitch. These vectorial effects may degrade image quality, or invalidate models for optical proximity correction (OPC) that do not properly comprehend them [2]. What matters for the image is the cumulative contribution of mask pattern, pellicle and optics. It may be possible to compensate the imaging errors by the coating of stratified films with appropriate thickness. The surfaces most accessible for this are those of the masks and pellicles.

Additional films on patterned mask could have at least two varieties: topcoat vs. multilayer. For topcoat, thin layer of highly transmitted film is deposited and planarized after mask features are patterned, cleaned, inspected, and repaired. For multi-layer, stratified film material is pre-deposited during mask blank preparation before resist is coated and patterned. The multi-layer film stack is then etched along with nominal mask absorber material with quality insurance of inspection/repair afterward. The film engineering on patterned mask could provide the extra degree of freedom to control the polarization of diffracted light and even enable image contrast enhancement. Likewise, additional film on pellicle with anti-reflective coating provides the knob to control the apodization effects on imaging through membrane [3].

The work reported here explores the magnitude and the control of apodization and polarization phenomena by both experiment and numerical computation. Influence of depolarization from the top coat on mask and from the anti-reflective coating on pellicle is represented by Poincaré sphere. The feasibility of the top coated composite on mask pattern and pellicle will require specification of uniformity on planarization, thickness, optical purity, defectivity and stress of the films. The tradeoffs owing to the new film introduction including integration challenge from new mask layers patterning interaction, new defect modes, additional cost and longer thruput, would need to be balanced with the advantages contributed from the additive strata vs. alternative approach such as rigorous 3D OPC.

While the ever-increasing complexity of OPC and phase shift structure on mask at planar dimension was a well-known reality, the complexity of mask strata in vertical dimension has just began.

6520-25, Session 5

Global optimization of masks to maximize process-window through focus, including film stack design to restore TM contrast at high-NA

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Our previous papers have outlined a multi-step procedure for global optimization of mask and source, using in-focus exposure latitude as the objective function. Results were included from a more sophisticated algorithm to optimize process window through focus, in which joint local optimization of both mask and source variables was alternated with global steps of optimizing the mask for fixed source and the source for fixed mask. Recently we published further details of the algorithm used for global optimization of the source; in this paper we provide further details of the mask optimization algorithm. Our method for including vector imaging gives rise to a theoretical solution for the film stack which in principle can restore TM contrast at high NA.

Even in a simplified formulation, mask optimization tends inherently to exhibit an unfavorable exponential scaling with problem size, but for small problems we can mitigate this difficulty by exploiting specialized knowledge that applies in the lithography context. For example, optimization of exposure latitude can be approximated as maximization of the edge slope between image regions whose intensities must be sufficiently distinct to print with opposite polarity. When the mask problem is cast in a correspondingly simplified form, we show that the solution space can be efficiently divided into regions that contain at most one local minimum. We recover a degree of generality by employing a less simplified objective function when we actually carry out our assessment of the local minima.

We can also exploit the quasi-binary specialization of lithographic targets when we define the solution space. Specifically, we identify potential local minima in the space formed by the dominant joint eigenvectors for minimizing average dark region intensity while maintaining average bright region intensity above threshold. By culling image-reversed joint eigenvectors that inherently degrade contrast, we typically reduce the dimensionality by more than a factor of two (exponentially shrinking problem size). Fully binary (tophat) image profiles are not an appropriate target for lithography; instead we seek to maximize edge slopes within images (near the DOF limit) that are more loosely constrained to exhibit adequate bright/dark polarity. These distinctions can be exploited by assigning a fixed proportion of the total dark region weight to the foot of image sidewalls (in a defocused plane). However, in such simplified terms a joint eigenvector formulation is incomplete - To obtain adequate solutions it is necessary to individually constrain multiple bright sample points to have intensities above threshold, resulting in multiple local minima. Nonetheless, we show that each “pocket” between these constraint quadratic forms can contain at most one local minimum, and we present an efficient point-by-point test to map out these pockets on a covering hypersphere.

The joint eigenvector formulation also provides a reasonable heuristic for quickly culling the majority of potential local minima in problems that are lithographically realistic - We show that with lithographic targets the size distribution of the minima-containing regions is extremely uneven, and that narrow regions can generally be ignored. With this and other pre-screening steps it is possible to prune the number of potential local minima by more than an order of magnitude at SRAM scale.

The above procedure represents one step in an algorithm to globally optimize a standard kind of process window, namely one that is defined against “classical” litho constraints, i.e. constraints which specify a fixed band of allowed positions for feature edges. However, during early stages of design one can define tolerances which more explicitly reflect constraints on devices, e.g. as is done with compactor codes for design migration. Compactor optimization operates on purely geometrical shapes, but the pairwise constraint form used in compaction can also provide useful flexibility in lithographic optimization, resulting in solutions whose robustness against fluctuations in dose or focus (defined by a kind of “functionality window”, rather than the usual process window) can be significantly larger than is achieved by solutions optimized under traditional (more restrictive) constraints.

Our earlier papers on mask optimization considered scalar aerial images, but under contemporary conditions the solution can be significantly influenced by vector imaging and film stack effects. Our algorithm can handle vector imaging in a general way, but it is useful to consider the special case of unpolarized illumination and a lens having radial symmetry (but arbitrary source shape). Under those conditions we show that the bilinear function which describes vector interference within the film stack can be expressed in terms of three generic radial functions. By inspection these expressions show that in principle one can recover classical scalar-like imaging conditions even at high NA by adding a reflective underlayer to restore destructive interference in TM polarized fringes. (The usual view of inherently degraded TM contrast at high NA need not apply when reflected waves contribute to the image.) Even a moderately high reflectivity can provide appreciable benefit, but the phase shift from the substrate must be controlled very accurately. In theory this can be accomplished by imaging into a very thin photosensitive layer that is spaced above the planarized reflecting film to occupy one antinode of the standing wave. With realistic materials and thicknesses there will still be phase variations in the reflected waves, whose impact on imaging can be addressed by the optimizer.

6520-26, Session 5

A solution for exposure tool optimization at the 65-nm node and beyond

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As device geometries shrink, tolerances for critical dimension and overlay control decrease. For the robust and stable manufacture of semiconductor devices at the 65nm node and beyond, both performance variability and drift in exposure tools are no longer negligible factors. To maintain the optimum performance of exposure tools, it is essential to thoroughly monitor exposure tool conditions. This data, which indicates exposure tool condition, is then fed back to a process control system within the fab.

Furthermore, because the optimum condition for each device segment is potentially different, it extremely difficult to optimize all exposure tools with a single evaluation method.

Therefore, we have developed a new system that collects and stores a large volume of data that indicates the exposure tool condition.

This paper will report on our new tool optimization method that, by using the large amount of data collected, analyzes both the performance variability and drift of exposure tools. This system provides device makers with the optimum performance of exposure tools.

6520-27, Session 6

Fast and accurate 3D mask model for full-chip OPC and verification

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As the industry continues to push 193nm lithography for 45nm node and below, the 3D mask topography-induced polarization and scattering effects become important in lithography simulations, due to the sub-wavelength nature of mask features. Unfortunately, it is quite expensive to include accurate physical electromagnetic (EM) models of these effects in full-chip simulations. This is particularly true for edge-based methods where the computing time increases as the layout complexity increases as a result of aggressive OPC. To overcome these difficulties, we have developed a new image-based method that combines rigorous EM modeling and fast image processing techniques. Its fast speed and independence of layout complexity make it practical to include physical EM effects in full-chip OPC verifications. This fast 3D mask model has been implemented on Brion’s Tachyon platform. Its accuracy has been validated against analytical and rigorous simulations (Figs. 1-2). In this paper, we will also describe the approach used in this method, its speed and its validation against experimental wafer results.

6520-28, Session 6

Process window and interlayer aware OPC for the 32-nm node

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Pushing optical microlithography towards the 32nm node requires hyper-NA immersion optics in combination with advanced illumination, polarization, and mask technologies. Novel approaches in model-based optical proximity correction (OPC) and sub-resolution assist feature

(SRAF) optimization are required to not only produce correct feature shapes at the nominal process condition but also to maintain edge placement tolerances within spec limits under process variations in order to ensure a finite process window. In addition, it is becoming increasingly important to consider multiple layers when performing correction in order to ensure electrical viability. In this paper we discuss the application of a model based process-window-aware and interlayer-aware integrated OPC system on 32nm node patterns. Process window awareness will be demonstrated for both main feature correction and SRAF optimization. In addition, interlayer-awareness will be demonstrated by correction that takes account the effects of active width on gate CD and of contact overlap with metal, gate, and active. The results show an improvement over "non-aware" OPC in gate CD control, in contact overlap, and in overall process margin.

6520-29, Session 6

Optical proximity correction in memory-device patterns using boundary layer model for 3D mask topography effect

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3D Mask-topography effect becomes critical at hyper NA regime. Although it is believed that rigorous 3D mask simulation can describe the effect accurately, the rigorous simulation is too slow to be applied to the optical proximity correction (OPC). One of promising approaches for fast OPC with the 3D mask effect is 'boundary layer model.' [1] In this model, near field image from a 3D mask feature is approximated using two layers: original and hypothetical boundary layers. Compared to the rigorous simulations and even the other 3D mask approximations, the boundary layer model is fast enough for a full-chip OPC.

This work presents a case study of OPC for a sub-50 nm node memory application using the boundary layer model with 1.2 NA ArF immersion lithographic processes. With optimized boundary layer, i.e., boundary-layer width, phase, and transmission, the boundary layer model is compared to the rigorous simulation and experimental results. We observe that the boundary layer model does improve OPC modeling to measured CD from the rigorous simulation or experiment. For example, root mean square (rms) of CD difference between the boundary layer model and experimental result is reduced to 4.33 nm, which would be 6.10 nm without the boundary layer (Figure 1). The OPC speed with the boundary layer is also confirmed to be only 2.2 times slower than the speed without boundary layer, which is reasonably acceptable.

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6520-30, Session 6

Generalized inverse lithography methods for phase-shifting mask design

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Optical proximity correction (OPC) and phase shifting masks (PSMs) are resolution enhancement techniques (RET) used extensively in the semiconductor industry to improve the resolution and pattern fidelity of optical lithography. Recently, Poonawala and Milanfar introduced a novel optimization framework for inverse lithography based on a pixel-based, continuous function formulation that is well suited for gradient-based optimization. Based on a steepest descent search, their approach is very effective for the inverse lithography problem. Their approach, however, attains masks with two-phase levels, which fail to generate adequate PSM for the synthesis of mask patterns having arbitrary Manhattan geometries. To overcome these shortcomings, this paper develops generalized gradient-based RET optimization methods to solve for the inverse lithography problem, where the search space is not constrained to a finite phase tessellation but where arbitrary search trajectories in the complex space are allowed. This generalization leads to mask patterns having unconstrained complex pixel values. Subsequent mask quantization leads to efficient design of PSMs having an arbitrary number of discrete phases. The proposed algorithms thus provide highly effective four-phase PSMs capable of generating mask patterns with arbitrary Manhattan geometries. A second contribution of the paper is the introduction of the wavelet penalty regularization framework. Inverse lithography is an ill-posed problem where numerous input patterns can lead to the same binary output pattern. Based on the wavelet transform, the wavelet penalty in ILT seeks to constrain the high-frequency energy of the mask patterns, and uses this constraint as a regularization term to bias the solution space. In effect, the wavelet penalty regularization attains solutions that have lower manufacturability complexity. Compared with total-variation regularization, traditionally employed in inverse problems, the wavelet penalty is more effective in reducing complexity in optimized mask patterns. In addition, it offers more localized flexibility than total-variation regularization. In terms of manufacturability complexity, details may be less desirable in some special areas of the mask and more tolerable in others. To this end, the wavelet penalty allows the non-uniform assignment of penalty weight coefficients across the mask. The third contribution of this paper is the development of an optimization algorithm for a double-exposure process for inverse lithography. In the event that four-phase masks are difficult to fabricate, but the goal is to still synthesize masks with arbitrary geometry, the double-exposure PSM method can be used. This approach includes a two-stage exposure process. At each stage, the PSM used is constrained to having two phases only. Our method provides the means to optimize both masks jointly. The double-exposure optimization method can lead to high fidelity output pattern reproduction with much lower pattern error than the one-exposure PSM optimization method. However, the disadvantage of this approach is that the exposure process is more complex.

6520-32, Session 7

Assessing the extendibility of chemically amplified resists through the use of MTF analysis employing 193 immersion IL, EUV IL, and e-beam lithography

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Photolithography is fast approaching dimensions at which the photoresist response limits the achievable feature size. Several methods have recently been proposed to quantify the inherent spatial resolution of photoresist films1-3. We present the results of three independent analyses of common data sets, obtained by 193 nm liquid immersion interferometric lithography using chemically amplified resists. Each analysis uses a different procedure to determine the modulation transfer function of the resist film at the spatial frequency set by the interferometric exposure. In this way we test the consistency of these different procedures for the measurement of resist resolution. The resists tested were designed around a common chemical platform, with modifications to vary the amount of image blur. The same resist system was also evaluated using EUV interferometric lithography and high resolution electron beam lithography.

References:

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6520-33, Session 7

Sources and scaling rules for LER and LWR

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The control of LER and LWR are critical to the future of lithography. We have previously shown from first principles that a significant source of

LER and LWR is a granularity in the illumination resulting from speckle or beating between the modes in the excimer laser. A second source of micro-nonuniformity is from interference in the illuminator optics. Several studies have predicted LER from granularity in the resist and from the development kinetics. The chemical amplification leads to a small number of acid molecules in the volume of the resist, an effect related to shot noise.

These granular effects are smoothed by a number of effects acting as spectral filters: multiple laser flashes, wafer scanning, diffusion of acid, transport effects in the developer, and integration through the thickness of the resist.

The total LER and LWR are the sum of these sources filtered by the smoothing effects. The LER sources and smoothing effects have different scaling rules and the LER spectra seen in the developed resist depend on image acuity and contrast, as well as on resist and development parameters. By modeling the different effects with their scaling rules and spectral filters it is possible to discriminate between different effects. A systematic and comprehensive model can be used to design experiments that can quantify the different contributions and help to propose remedies for the LER.

6520-34, Session 7

Polarization aberration analysis using Pauli-Zernike representation

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Polarized illumination is a viable technique for improving the image quality of hyper-NA lithography. On investigation of polarization effects, it is often assumed that the lens system can maintain the polarization state through optical path, which may not be the case with actual lenses. These polarization changes may cause CD variations and pattern placement errors. The extent of changes in the polarization state may vary across the pupil. In order to describe polarization variations across the pupil (polarization aberrations), we have proposed a Pauli-Zernike matrix representation.1 where is 2×2 matrix element of Jones matrix, and are Pauli spin matrices and their coefficients, respectively.

The Pauli spin matrix representation is convenient and intuitive for understanding the effects of polarization aberrations, because coefficients (a0, a1, a2, a3) of Pauli spin matrices are related to eight different and independent types of physical behavior (Table. 1). The real parts and imaginary parts of coefficients of Pauli spin matrices represent amplitude changes (dichroism or absorption) and phase changes (birefringence or retardation) of eigenvectors, respectively.2 These eight independent coefficient can be described in Zernike polynomials across the pupil, while there are often discontinuities of phase for Jones matrices.

Fig.1 shows the Fresnel effects of mask blanks in Jones matrix and Pauli spin matrix forms as a polarization aberration. It is clear that there are no phase errors (scalar aberrations) in Pauli-Zernike format but not in Jones. In this paper we'll show more examples of physical phenomena such as lens coatings and pellicles. In addition we'll show effects of CD error and pattern placement, including polarization aberration budget analysis.

6520-35, Session 7

Measurement of projection lens NA and exit pupil profile using transmission mapper (TMAP(tm))

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Introduction: The ability to measure lens performance accurately and rapidly is essential for modern day lithographic tools. In-situ metrology instruments developed by tool vendors and other companies are already in use across the industry for measurement of lens aberrations and illumination coherence [1,2,3,4]. This information is essential for matching tools in advanced technologies to ensure a consistent performance for process parameters including iso-dense bias, cross-field CD variation and depth of focus.

TMAP TM is a new technique that is capable of measuring projection lens NA absolute value along the scanner slit and the transmission variation within the exit pupil. A dose matrix is exposed with a specially designed reticle which images the exit pupil of the projection lens onto a resist coated wafer. Individual field points of the exit pupil from the developed wafer are collected from resist coated wafers with an image capture station. There images are processed with a software application and the output maps exit pupil geometry and transmission as a function of field position. The resulting output from TMAP can be input to simulation software to model the effects on process window.

A prototype instrument of TMAP was made available to Intel Ireland for experimentation on a series of 248nm and 193nm scanners spanning several generations of technology. Figure 1 shows an example of the transmission profile for a series of 248nm scanners with NA=0.68. In this case the radial profile shows a positive transmission gradient or bias towards the edge of the pupil enhancing the non-zero diffraction orders and resulting in improved image contrast. This paper will present the results of this work highlighting the different exit pupil profiles from different tool generations and also effect of mismatches within a given toolset. The impact of using different illumination conditions, varying lens NA and instrument repeatability will also be reported. In-line product data in correlation with simulation from a metal layer in a flash memory process and correlations from will highlight the significance of the transmission profile on iso-dense bias. In this instance measuring and evaluating the impact of a particular transmission profile allows the process engineer to maximise available process window by biasing the reticle dimensions for the relevant critical features. It is also proposed that TMAP is a suitable instrument for evaluating the health of a toolset as the projection lens degrades with pulsed energy from the laser and molecular contamination.

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6520-36, Session 7

Best focus determination: bridging the gap between optical and physical topography

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With decreasing CD budgets and smaller k1 values the need for perfect focus control becomes paramount. Among the individual contributors to the overall focus budget, the process (stack, design) sensitivity of the level sensor and the focus setting accuracy for the individual layers are two major contributors. Traditionally, Fab process engineers use focus-exposure matrices (FEMs) to calibrate the best focus for a given layer. In our study we discuss the limitations of this level sensor based technique, which solely relies on the optically detectable topography across the field. By exposing and measuring FEMs on multiple points in the field, and by the use of a phase grating focus monitor (PGFM), we demonstrate the systematic and random focus variation across the scanner exposure field for several layers. Critical BEoL layers in particular show considerable impact of topography, thus resulting in the across field focus variations shown. These limitations can be overcome by the use of a newly developed air-gauge focus sensor (AGILE) that is expected to be independent on any process variation. The AGILE sensor predicts and corrects level sensor process dependencies for some layers and thus accounts for the optical vs. physical topography offset. By the use of multi-point FEMs and PGFM we show that the intrafield focus range can be reduced by as much as 50%, depending on certain layer and layout characteristics. Finally, we discuss the impact of the new sensor in conjunction with the extended FEM scheme on the overall focus budget for critical layers.

6520-37, Session 7

In-situ measurement systems for realizing image performance at the 45-nm node and its effects

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The performance demands on the most recent exposure tools are requiring further improvements in imaging that impacts CD performance, such as wavefront aberrations and image field deviation, and for distortion, which affects overlay performance.

In order to demonstrate optimal performance, it is crucial to measure the image performance on the machine and compensate according to the measurement result.

The new exposure tool is equipped with an in-situ metrology system in order to achieve the most effective image performance.

We have newly developed a compact interferometric system for hyper-NA optical systems that characterizes wavefront aberrations of the projection optics. Through the combination of the new in-situ wavefront metrology system and the compensation system of projection optics, ultra-low wavefront aberration control can be realized.

A new TTR-calibration system that uses illumination light will measure image field deviation (IFD) and lens distortion with high accuracy. The use of the illumination light provides the optimum image performance in accordance with the actual exposure result.

In addition, the compensation of reticle deformation is becoming an important factor in both imaging and overlay performance. The new exposure tool also allows for measurement of reticle deformation while the reticle is loaded onto the reticle stage, thereby enabling compensation of distortion and IFD due to reticle deformation.

In this paper, we will report on the measurement performances of each of the metrology systems. We will also present the imaging performance, including IFD and distortion after compensation according to the in-situ measurement results, which will demonstrate that the new exposure tool is a production-worthy exposure system for the 45nm node.

6520-38, Session 8

Immersion defect reduction, part II: the formation mechanism and reduction of patterned defects

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Defectivity is one of the critical issues to be resolved for immersion lithography, besides overlay and throughput. Unlike the latter issues, it not only a matter of hardware engineering but also that of complex material properties. Typical immersion defects include bubbles, watermarks, particles, and particle-printing defects. Characterizing these defects is important for setting further defect-reduction strategies. Moreover, for a not well-controlled immersion system, the defect count may reach several hundreds per wafer pass. Before the SEM review, its required labor is greatly relieved if the detected defects can be accurately classified by another less time-consuming method. In the first part of this paper, we show a way to link the optical defect image to the SEM image. In addition to labor intensive, since low-energy electrons are only surface sensitive, it is very difficult to determine whether un-resolved resist patterns were caused by watermarks or obscured by fall-on particles during exposure. Our method can clearly identify the particle source and conclude that the majority of the un-resolved patterns were caused by particle obscuration during exposure but not watermarks.

The second part of this paper reports a unique method to reduce particle-printing defects. Because a majority of the un-resolved resist patterns was caused by particle printing, eliminating them can greatly reduce the total defect count. Using the method reported in another paper of this conference, we found that particles were printed by exposure of the residues left by some previous fields. Using a carefully designed exposure sequence, the average defect count has reduced from 19.7 per wafer to 4.8 per wafer(see the attached figure 1). The exposure sequence will be covered.

6520-39, Session 8

Optical error sensitivities of immersion lithography

Z. G. Chen, IBM Corp.; K. Lai, IBM Microelectronics Div.

193nm immersion lithography is marked as the main solution for 45-nm and 32-nm critical levels. Immersion system increases resolution when NA\>1 and increases depth of focus (DOF) when NA<1. Those immersion fundamental advantages have been demonstrated experimentally. The improvement of DOF enables better CD uniformity, simple mask/RET (Resolution Enhancement Technology) and less design restrictions. However we found that the imaging of the immersion system has different sensitivities to the optical errors such as reticle non-flatness, Image Plane Deviation (IPD) and laser bandwidth. The immersion sensitivities mentioned above are higher than those of dry system and the effect is even larger when higher fluid index is used. The resultant effect of these enhanced sensitivities lead to worse image plane flatness/centering on wafers and may lead to larger ACLV and machine to machine CD matching error than expected. This adverse effect of the immersion system may not be pronounced at the lower NA where DOF improvement is more significant, but it will be more noticeable at the hyper NA where the sensitivities are even higher and DOF is getting smaller.

In this paper, we demonstrate the increased sensitivity factors both mathematically and experimentally. Table 1 shows the comparison of across field focus and dose variation between the dry and immersion tool, using 2 different resist processes. We perform a detailed error component analysis to single out the immersion related factor and its impact to CD control. For this purpose we independently quantify the reticle non-flatness directly on the mask as well as different methods to measure image plane variation, such as scatterometry.

We also identify possible compensation solutions such as reticle shape correction, improved focal plane setup methodology and the incorporation of focus blur into OPC model, in order to alleviate the adverse effect of immersion in ACLV and CD stability over time and over different tool sets.

6520-40, Session 8

Contamination and particle control system in the immersion exposure tool

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Water-based immersion technology has overcome various obstacles, and is now the consensus technology candidate for the 45nm HP. The fundamental issues across many aspects of immersion lithography have been demonstrated, however defect reduction methods are still critical issues for mass production.

We have developed a new platform, specifically designed for immersion lithography. The immersion nozzle equipped on this new platform, which incorporates Canon's original Liquid Film Flow method, enables a naturally circulating water supply by using the stage movement to generate the water flow between the lens and wafer. Since the continuous movement of the wafer is essential for water flow at the lens center, we have conducted a thorough investigation of resist leaching issues. By employing the Liquid Film Flow nozzle, which allows for natural water flow, the impact on the wafer and the resist is minimized, thereby preventing generation of immersion specific defects.

This paper will report on the experimental results of the investigation into the dependency of immersion specific defects on the scan speed of the exposure tool and on the resist materials. In addition, we will show defect evaluation results from the FPA-7000AS7, Canon's first commercial immersion tool for mass production.

One of the critical issues of a mass production exposure tool is maintaining a contamination-free internal environment over the long term. At last year's SPIE, we showed that lens contamination caused by the PAG (Photo-acid-generator) of resist does not occur in the exposed area under normal immersion conditions. However, we also showed that contamination does occur in the unexposed area, which leads to particle growth. This issue could cause particles in the water, originally

accumulated at the immersion nozzle, which then results in defect problem. We fully recognize that this would become a critical issue due to subsequent production yield loss. In this paper, we will introduce our newly developed in-situ cleaning system for the immersion nozzle. We will also report on our evaluation into the dependency of the number of particles in the immersion water on the cleaning effect, the cleaning liquid and the frequency of cleaning.

6520-41, Session 8

Extending immersion lithography to the 32-nm node

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C045 technology node processes are driving the development of immersion lithography techniques and infrastructures and C032 is following in its tracks. As semiconductor development enters the arena of low leakage, high-performance devices using immersion lithography, the 32nm technology node adds more pressure of decreasing pitches and feature sizes using the most cost effective method available. The Crolles2 Alliance is in the first phases of the push for very low k1 193nm lithography for our technology development. Many resolution enhancement techniques are being explored to fill the low k1 realm; including implementation of these techniques and more aggressive integrations to support the device parameters.

However, the early development of C032-nm node along with the need for better focus and dose control algorithms, imaging of pitches to allow for the packing density will present significant challenges to photolithography even when considering super hyper-NA immersion lithography. Reflectivity variations, thin film interference through the complex film stacks, and increased sensitivity to feature size is posing a challenge for maintaining good and consistent features.

This paper discusses an analysis and early results covering the beginning development of C032-nm node with \>1NA immersion lithography. Specifically, parameters such as illumination and enhancement techniques, processing capability, application of OPC at a very low k1, process integration, mask effects, and defectivity as discussed.

6520-42, Session 8

Immersion defectivity study with volume production immersion lithography tool

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ArF immersion lithography has become accepted as the patterning solution for critical layers. Volume production of 55 nm device using immersion lithography is beginning. One of the key issues for the success of volume production immersion lithography is the control of immersion defectivity. Because the defectivity is influenced by the exposure tool, track, materials, and the wafer environment, a broad range of analysis and optimization is needed to minimize defect levels. Defect tests were performed using a dedicated immersion cluster consisting of a volume production immersion exposure tool, Nikon NSR-S609B, having NA of 1.07, and a resist coater-developer, TEL LITHIUS i+.

In order the minimize immersion defects, each aspect of the process must be optimized. The design of the nozzle structure and wafer stage of the exposure tool must be well optimized to minimize tool generated defects. Pre- and post-rinse processes have been proposed by track vendors to reduce track generated defects. Appropriate wafer edge treatment is critical to prevent edge peeling and resultant tool contamination, causing particle defects. We have developed an off-line scan test bench to measure the particle level with various materials and process conditions. Using these optimization and screening tests we successfully reduced defect levels.

For volume production, not only must defects be eliminated, but the defectivity of the process must be stable for long periods of time. We propose a simple method to check the defect level, called a scan particle check. In this check, a topcoat or resist coated wafer is simply scanned with zero dose under the immersion nozzle within the lithography tool, and then attached particles and residues on the wafer surface are measured with a defect inspection system. If the tool is contaminated, particles and residues on the wafer will be increased. Long term scan particle check results and their correlation with defectivity will be discussed.

In case of accidental tool contamination, a cleaning process should be established. Liquid cleaning is suitable because it can be easily introduced through the immersion nozzle. A surfactant type cleaning liquid was applied to the actual immersion scanner and the results will be discussed.

A broad range of optimization of tools, materials, and processes provide convincing evidence that immersion lithography is ready for volume production chip manufacturing.

6520-43, Session 9

Lossless I.C. layout compression: intra-cell, inter-cell sub-cell detection

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I.C. layout data size has increased with every new generation of technology. As the minimum feature size becomes smaller, the layout becomes denser. In addition, as the semiconductor industry moves toward sub-wavelength design, resolution enhancement techniques are applied more frequently. The increased transistor density and the increased usage of RET have led to a significant increase in layout data size. In the latest ITRS road map, a single layer of uncompressed layout presented to the pattern generator will exceed 400 Gigabytes in 2007.

In this paper, we present a technique for compressing hierarchical I.C. layout data while remaining compliant to the original format of the layout, e.g. GDSII or OASIS; this precludes the use of entropy coding techniques such as Huffman or Arithmetic coding. Instead, we achieve compression by eliminating redundancies in the representation of the geometrical data by looking for repeating groups of polygons within a cell and between multiple cells. We call the first problem intra-cell sub-cell detection and the second one inter-cell sub-cell detection. Since our techniques guarantee that the resulting layouts remain OASIS or GDSII format compliant, there is no need for a de-compressor within any of the commonly used CAD tools to view the layout.

We define the inter-cell sub-cell detection problem as follows: Given m cells, C1, C2 , ..., Cm, find the largest group of polygons, SC, that occur in n cells, with $2 \leq n \leq m$. A group of polygons, SC, is said to occur in a cell if there exists a translation that takes SC to some subgroup of polygons in a cell. This problem is NP complete as it is merely a different formulation of the Largest Common Point Set (LCP) problem, which has been shown by to be NP complete. We define the intra-cell sub-cell detection problem as follows: Given a cell, find the largest group of polygons, SC, that occurs n times within the cell. This problem is also NP complete, and can be proven by a simple reduction from the LCP problem. Since both problems are NP complete, we have developed heuristics to solve these problems. We show experimental results on actual layouts demonstrating the effectiveness of our approach.

6520-44, Session 9

Advances in compute hardware platforms for computational lithography

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As the gap between the minimum wavelength of scanners and the critical dimensions of devices has grown, the complexity of the techniques used to compensate for that gap has grown geometrically. The last six years have seen the increasing advance of computational and algorithmic complexity to compute mask patterns that retain sufficient lithographic fidelity to print and yield well enough to maintain the advances in circuit density that are the engine of the semiconductor economy. From 180nm to 45nm, we have seen the growth and application of an entirely new flow in the design and tape out of semiconductor devices. New techniques including Optical Proximity

Correction (OPC), Scattering Bars (SB), Phase Shift Masks (PSM), Lithography Rule Checking (LRC), and Inverse Mask Lithography (IML) to name but a few, constitute a significant transformation of the design. Initially applied only to the most critical portions of the most critical layers such as poly and active, they are now considered de-rigueur for almost every layer through and including the topmost metal layers. The application of these new techniques requires a brand new category of software that comprehends and simulates process behavior in order to predict distortions due to the physical process effects such as the optical characteristics of the scanner, the resist photosensitivity, the resist processing characteristics, and the characteristics of etching. The software then uses this predictive simulation capability to make adjustments to the mask pattern to compensate for the distortions. In addition to the creation of a new and complex intermediate design stage requiring an entirely new form of verification, these simulation techniques have become one of the most computationally demanding steps in the design process. Compute farms of hundreds and even thousands of CPUs are now routinely used to perform these complex transformations needed to modify the target pattern of a single layer so it will print and yield. This oral presentation will chronicle the history of these techniques from the perspective of their impact on the computing systems used to apply them, and the effect these new techniques and the compute platforms to power them have had on the costs of taping out a chip. The practical aspects of the infrastructure needed to support such extensive compute farms including power, reliability and cooling will be examined. Finally, newly emerging High Performance Computing (HPC) techniques that hold the promise of checking this unbridled growth in computational requirements will be reviewed and contrasted. Technologies such as On-Demand Compute Centers, multi-core processors, Field Programmable Gate Arrays (FPGAs), The Cell Based Engine (CBE) Processors, Digital Signal Processors (DSPs), and Graphics Chips will be examined.

6520-167, Session 9

SEM image contouring for OPC model calibration and verification

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Lithography models for leading-edge OPC and design verification must be calibrated with empirical data, and this data is traditionally collected as a one-dimensional quantification of the features acquired by a CD-SEM. Two-dimensional proximity features such as line-end, bar-to-bar, or bar-to-line are only partially characterized because of the difficulty in transferring the complete information of a SEM image into the OPC model building process. A new method of two-dimensional measurement uses the contouring of large numbers of SEM images acquired within the context of a design based metrology system to drive improvement in the quality of the final calibrated model.

Hitachi High-Technologies has continued to develop “full automated EPE measurement and contouring function” based on design layout and detected edges of SEM image. This function can measure edge placement error everywhere in a SEM image and pass the result as a design layout (GDSII) into Mentor Graphics model calibration flow. Classification of the critical design elements using tagging scripts is used to weight the critical contours in the evaluation of model fitness.

During process of placement of the detected SEM edges of into the coordinate system of the design, coordinate errors inevitably are introduced because of pattern matching errors. Also, line edge roughness in 2D features introduces noise that is large compared to the model building accuracy requirements of advanced technology nodes. This required the development of contour averaging algorithms. Contours from multiple SEM images are acquired of a feature and averaged before passing into the model calibration. This function has been incorporated into the prototype Calibre Workbench model calibration flow.

Based on these methods, experimental data is presented detailing the model accuracy of a 45nm immersion lithography process using traditional 1D calibration only, and a hybrid model calibration using SEM image contours and 1D measurement results. Error sources in the contouring are assessed and reported on including systematic and random variation in the contouring results.

6520-45, Session 10

Phase-shifted assist feature OPC for sub-45-nm node optical lithography

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Hyper numerical aperture (NA) implemented in immersion exposure system makes the semiconductor business enable to enter sub-45nm node optical lithography. Optical proximity correction utilizing SRAF has been an essential technique to control critical dimension (CD) and to enhance across pitch performance in subwavelength lithography1. Mask lithography, however, is getting more challenging with respect to patterning and processing sub-resolution assist features (SRAFs): the higher aspect ratio of mask structure, the more vulnerable. Mask manufacturing environment for DRAM and Flash becomes harsher mainly due to mask patterning problem especially pattern linearity, which causes pattern broken, inspection issue, and finally CD issue on wafer. When a pattern in relatively isolated pitches has small or large assist features, the assist features may bring unexpected CD or print on wafer. A frequency-preserving assist bar solution is the most preferred one, but it is difficult to realize for opaque assist features due to printability2. In this paper, we propose a new type assist feature dubbed “Phase-shifted Assist Bar” to improve process window and to solve the resolution constraint of mask at sub-45nm manufacturing process node. The concept of phase-shift assist bar is applying phase-shift to SRAF realized with trench structure on general mask, such as Binary and Attenuated Phase-Shifted Mask (Att.PSM). The characteristics of phase-shift assist bar are evaluated with rigorous 3D lithography simulation and analyzed through verification mask, which is containing hugely various size and placement of main and assist feature. The analysis of verification mask has been done with aerial image verification tool. This work focuses on the performance of phase-shift assist bar as a promising OPC technique for “immersion era” in terms of resolution enhancement technique, optical proximity correction, and patterning on mask.

6520-46, Session 10

The random contact hole solutions for future technology nodes

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The authors will explore the possible lithography solutions for the future technology nodes, from 90 nm down to 32 nm half-pitch (HP). The special emphasis will be on the random logic application because of the lack of a strong resolution enhancement technique (RET) for the random hole layouts. The use of illumination optimization, focus drilling can extend the projection optical lithography down to near 60 nm HP. The adoption of pitch split double exposure technique is needed to provide a robust manufacturable process window to further extend to around 50 nm HP. To further shrinking the design rule, a double patterning is need after the pitch split. The pitch split double patterning technique reaches its limit around 40 - 45 nm HP. The desire to not limit the integrated circuit (IC) design requires the lithography process k1 to be as high as possible. The random logic contact hole application is well suited for EUV lithography for 35 nm HP and below because of the high k1 process and a potential for high productivity of a mask based lithography. The pattern density of contact hole masks would not require a stringent mask defect requirement, and moreover, the EUV’s relatively higher system flare does not have a significant impact on imaging. The authors intend to use the available EUV data and simulations results to demonstrate that EUV can provide a robust process window.

6520-47, Session 10

RET application in 45-nm node and 32-nm node contact hole dry ArF lithography process development

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It is challenging to develop 45nm node contact hole using dry ArF lithography process with acceptable lithographic margin due to its small process window and large mask error enhancement factor (MEEF). No single process using conventional lithography without resolution enhancement technology (RET) application will meet DOF requirement to cover the full range of pitch from dense to isolated contact hole for 45nm node. We have developed dry ArF lithography processes for 45nm node contact hole on scanner ASML XT1400E by applying RET including off-axis illumination, SAFIER (Shrink Assist Film for Enhanced Resolution) process, EFESE (focus scan), etc.

The paper will discuss process window through pitches with optimized illumination, and where to separate pitches in case of double exposure with consideration of DOF and OPC model simulation. It will look into the effect of EFESE on DOF improvement, proximity, and MEEF at various pitches. The paper will also discuss OPC modeling strategy for 45nm node contact hole. It will analyze the effect of OPC grid size on OPC run time, file size, and edge placement error (EPE).

To extend process further to 32nm node, we demonstrated the process capability for 32nm node contact using double patterning technique. We achieved 50nm final contact CD with pitch of 100nm. Double patterning includes two litho-etch steps. The dense feature is designed into two complementary parts on two masks such that the density is reduced by half and minimum pitch is increased by at least a factor of 21/2 depending on design. After the first litho process using the 1st mask, the wafer is etched. Then another litho process using the 2nd mask is carried out and followed by a second etching process. The complete patters are formed with two litho-etch process steps.

6520-48, Session 10

Patterning with amorphous carbon spacer for expanding the resolution limit of current lithography tool

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Double Exposure & Etch Technology (DEET) is one of the main candidates for expanding the resolution limit of current lithography tool. But this technology has some bottleneck such as controlling the CD uniformity and overlay of both mask involved in the lithography process. One way to solve this problem and still maintain the resolution advantage of DET is using amorphous carbon spacer. Patterning with amorphous carbon spacer not only expands the resolution limit but also solves the problems involved with DEET. This method realizes the interconnection between the cell and peripheral region by “space spacer” instead of “line spacer” as usually used. Spacer process involves gate mask, gate etch, amorphous carbon spacer, SOG coating, and SOG etch back step sequentially. Peripheral mask is added to realize interconnection region as well as peripheral region. Finally pattern doubling is accomplished by removing of photo resist and amorphous carbon spacer with O2 plasma. With the use of spacer, it would be possible to realize the NAND flash memory gate pattern with less than 35nm feature only using 0.93NA (ArF).

6520-49, Session 10

32-nm SOC printing with double exposure techniques, regular design, inverse lithography, and 1.2 NA scanner

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Lithography entered into a new era with the introduction of the 120nm CMOS technology node and will continue in that way down to the 32nm node. Throughout these technology generations the wavelength for the critical layers has not and will not change. Only 193nm lithography will be used, pushing lithography to move closer to the theoretical limit of optical resolution . Therefore, Resolution Enhancement Techniques (RET) have been developed in order to print all shapes properly and to close the resolution gap. In parallel, starting from 65nm technology onwards, Design For Manufacturing (DFM) became a key enabler in order to shorten development cycle time. In the lithographic field, System On Chip (SOC) makers follow their own course, having different constraints, than flash or microprocessors manufacturers. Most of the SOC development effort is focused on two types of cells:

- Static RAM that are regular and use very aggressive design rules

- Logic cells that are very irregular but with slightly more relax design rules. Whereby usually the most difficult logic cell to address is the flip-flop because of its area constraints

The goal of this paper is to demonstrate the possibility, using the best available scanner technology (immersion 1.2 NA ASML /1700), to properly print these two key elements for 32nm logic technology at the same time. The first element is a 0.18µm(c)˜ SRAM and the other, a flip-flop with 32nm design rules. For the flip-flop, regular design methodology, in the frame of DFM, has been used to improve pattern fidelity at all critical levels. The feasibility of this methodology has been demonstrated on the diffusion, poly, contact and metal 1 levels, the four most critical levels.

6520-50, Session 10

Ultra-low k1 oxide contact hole formation and metal filling using resist contact hole pattern by double L&S pattern formation method

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Double line-and-space (L&S) Pattern Formation Method is one of the options to form about 0.3 k1 dense contact hole (C/H) pattern. The method is that a C/H pattern is formed by two L&S patterns that are perpendicular to each other. Because L&S patterns with off-axis illumination have large lithography latitude, the k1 factor of the C/H pattern fabricated by separate formation of the two L&S patterns can be lower than that of the C/H pattern fabricated by the conventional method. The expectation was proved to be right by experiments1). The next step to apply the Double L&S pattern Formation Method to production is whether the resist C/H pattern can be transferred to oxide and the oxide C/H pattern can be filled with metal.

Before etching, half pitch (HP) 75 nm 1:1 resist C/H pattern was formed on the bottom anti-reflective coating composed of upper spin-on glass (SOG) and lower spin-on carbon (SOC). The substrate was the oxide film, of which thickness was 500 nm. The resist process flow was as follows. The first L&S pattern was formed by an attenuated L&S mask and dipole illumination. The center position of the dipole illumination was 0.76 and the radius was 0.19 for an NA of 0.85. ArF scanner was used. After making the first L&S pattern insoluble, the second L&S pattern that was perpendicular to the first L&S pattern was formed on the first L&S pattern with the same condition.

The resist pattern was transferred to SOG film using a fluorocarbon based reactive ion etching (RIE). The SOG pattern was transferred to SOC film using an oxygen based RIE. The SOC pattern was transferred to silicon oxide film using a fluorocarbon based RIE. After SOC stripping, HP 75 nm 1:1 C/Hs made of oxide were obtained as shown in Fig.1. So the 1:1 C/H pattern made by the Double L&S Pattern Formation Method with L&S masks and dipole illumination can be used as the etching mask in the tri-level resist process and in silicon oxide etching.

The shape of the oxide C/H pattern was square in comparison with the conventional C/H pattern. The merit of the square hole is reduction of the C/H resistance in comparison with the conventional C/H pattern. On the other hand, there is the possibility of void formation after metal filling. Then, the oxide C/Hs were filled with copper by electroplating after barrier metal and seed copper sputtering. Figure 2 shows the cross-sectional reflected electron image of the C/H pattern. The cross section contains the corner of the C/H pattern as shown by the broken line in Fig.1. It was observed that the corner of the hole was filled with copper. No void was observed. So the oxide holes made by the Double L&S Formation Method were filled completely.

The resist C/H pattern formed by the Double L&S Pattern Formation Method could be used to form ultra-low k1 dense contact holes.

1) H. Nakamura et al.: JM3 4 (2005) 023005.

6520-51, Session 11

Optical mask CD calibration for hyper-high-NA 193-nm applications

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Hyper high NA mask topography effects are expected to have a major influence on the imaging properties of 193nm lithography systems for future nodes. The introduction of immersion lithography with NA\>1 expands the usage of the 193nm wavelength to nodes with critical features < 55nm (1x). The lateral dimension of smallest mask features e.g. SRAF-s, which need to be applied for these technology nodes, decrease to ~1⁄2 wavelength(4x). In order to describe the optical properties of those tiny mask features especially when polarized aggressive off-axis illumination is applied, the thin film (Kirchhoff) approximation fails totally. Therefore rigorous 3d mask simulations need to be applied. As for any other simulation, the calibration of the required input parameters, which are here especially the lateral mask dimension and 3d mask stack, is one of the most critical points.

In this paper we apply the Zeiss AIMS TM (Aerial Image Measurement System) in order to characterise the optical behaviour of critical mask features for different mask types under different illumination conditions. We compare the AIMS results with predictions of rigorous 3d mask simulations.

6520-52, Session 11

Pupil plane analysis on AIMS™ 45-193i for advanced photomasks

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For half pitch 45nm and beyond, hyper NA imaging systems and aggressive off axis illumination will be applied but it involves contrast loss due to vector effects. Vector effects can be reduced effectively by use of polarized illumination. On the other hand various problems, such as mask induced polarization, effects of mask topography and birefringence of substrates, have to be taken into account. In order to analyze the influence of mask material's characteristics, 3D topography and the degree of polarization (DoP), it had been mainly measured diffracted light using an ellipsometer but we have proposed to use the AIMS™ system for this purpose in previous work *. That was enabled by acquiring pupil plane images using the Bertrand lens in the AIMS™ system to measure selected area's diffracted light. We used off-axis MonoPole illumination in x- and y-polarization which was placed at one side of standard DiPole aperture to evaluate 0th and 1st order diffracted light intensity separately and compared the printing performance using linear polarized DiPole illumination at the same time by AIMS™ system. But DiPole illumination has a good printing performance on only one direction's pattern. So, this illumination is used for very limited pattern or combination of double mask and exposure to print for both directions. Cross-quad with azimuthally polarized illumination has been proposed to achieve good printing performance for both patterns by single mask and single exposure.

In this paper, we will use the same MonoPole illumination system as previous work but other direction's pole is also used on the illumination aperture to cover total diffraction orders of cross-quad illumination. In order to get diffracted light of 45nm half-pitch Hyper-NA e.g. NA=1.35 was applied. The AIMS™ 45-193i Alpha system was used for this evaluation.

The examinations were performed with binary and half tone PSM with half pitch 40 to 150nm on a 1x scale. We used off-axis MonoPole illumination in x- and y-polarization which was placed at x and y side of standard cross-quad aperture to evaluate 0th and 1st order diffracted light intensity separately. By the equation of "diffracted light intensity" divided by "reference intensity" we got normalized intensity for each diffraction order under different polarization illumination settings. With these we calculated the degree of polarization DoP=(TE-TM)/(TE+TM) for 0th and 1st diffraction order and compared it to simulation results.

As a result, we have confirmed good agreement between AIMS(tm) and simulations. In conclusion, the AIMS™ system is a valuable tool for both analyzing diffraction efficiency from the mask pattern and comparison to wafer printing performance. In another word, AIMS™ system can analyze mask material's characteristics.

Moreover, for other item, birefringence is thought to be critical at half-pitch 45nm imaging. Birefringence non-uniformity affect to polarization purity variation for the polarized illumination. So, we tried to measure intensity in the preferred state (IPS) value in the field of the mask and confirmed how birefringence affect to IPS degradation by measuring illumination's polarization state at the pupil plane.

Reference;

* T. Sutou et al, "Diffraction efficiency analysis on AIMS™ 45-193i for advanced photomasks", 3rd International Symposium on Immersion Lithography, Oct. 2006. (To be published)

6520-53, Session 11

The impact of the mask stack and its optical parameters on the imaging performance

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The light diffraction from small features on optical masks leads to several phenomena which can have a strong impact on the imaging performance of a mask. This includes pronounced variations of diffraction efficiencies at pitches where higher diffraction orders become evanescent (so called Wood anomalies), strong polarization dependence of diffraction efficiencies, and several other effects. In general, these phenomena strongly depend on the refractive index and the absorption of the mask materials and on the configuration of the mask absorber stack. For example, the single layer MoSi absorber, which is used in standard attenuated PSM, has been shown to exhibit an unfavorable polarization performance, especially for sub 65nm feature sizes. Dual layer absorbers were proposed to increase the degree of freedom in mask design.

In this paper, rigorous electromagnetic field (EMF) simulations of light diffraction from the mask using the waveguide method in combination with vector imaging simulation are used to explore the impact of the optical mask parameters on the diffraction and imaging performance. Resist effects are approximated by a simple threshold model which is applied to the intensity distribution inside a thin photoresist layer on an index-matched substrate. Optical mask parameters and mask stack configurations are varied over a wide range and independently from the present availability of appropriate materials. The results are evaluated in terms of diffraction efficiencies and typical lithographic performance criteria such as iso-dense bias, mask error enhancement factor (MEEF), sidelobe-printability, and overlapping process windows. Both local and global optimization techniques are used to identify optimum parameter settings. The results are compared with the performance of standard mask stacks and parameters.

6520-54, Session 11

Mask 3D effect on 45-nm imaging using attenuated PSM

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In the exposure using ArF immersion exposure tool, under the conditions in which the mask pattern pitch is smaller than several times the exposure wavelength, diffraction light distribution cannot be predicted correctly by the Kirchhoff approximation mask model, and therefore, rigorous Electromagnetic Field (EMF) analysis is required. In particular, in the dense L&S formation using oblique illumination and an attenuated phase shift mask (att-PSM), the intensity of 0th and 1st diffraction lights changes as pitch shrinks[1].

In high-density L&S formation, it is necessary to reduce a mask error enhancement factor (MEF) and to obtain sufficient exposure latitude. We consider the following two contrast control "knobs": (1) optimizing the transmittance of attenuated mask material, (2) optimizing mask bias. Figure1 shows the relation between mask bias and L&S aerial image contrast obtained using the Kirchhoff model and the EMF model. The important image characteristics are normalized image log slope (NILS)

and dose-MEF. We performed a simple optimization for exposure-defocus window of dense L&S pattern reflecting consideration of the mask EMF model for half-pitch 45nm L&S imaging using att-PSM and oblique illumination.

We carried out experiments of attenuated PSM exposure using hyper-NA exposure tools and compare the results with the 3D mask simulation. We will discuss the extent between experiment and 3D mask simulation, and practical effectiveness of the contrast control knobs.

[1]K.Sato et al, Photomask Japan 2006, 6283-122.

6520-55, Session 11

Effects of reticle birefringence on 193-nm lithography

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Unpolarized light has traditionally been used for photolithography. However, polarized light can improve contrast and exposure latitudes at high NA, especially for immersion lithography with NA of \> 1.0. As polarized light passes through a reticle, any birefringence in the reticle material can cause a change in the orientation or degree of polarization, reducing the contrast in the final resist image. This paper studies the effects of reticle birefringence on dry and immersion imaging for 193nm lithography.

The birefringence magnitude and orientation of the fast axis were mapped across several unpatterned mask blanks. These blanks cover a range of birefringence from 0 to 6nm/cm, with different orientations of the fast axis. These reticles were printed with an array of large open areas surrounded by test structures. The birefringence was measured again on the patterned reticles, and several locations were selected to cover a range of magnitudes at different orientations of the fast axis. Dry imaging at 0.93 NA and immersion imaging at 1.2 NA will be evaluated, looking at birefringence effects on dense lines and contact structures. MEEF, LER, and dose and focus latitudes will be studied on line/space patterns. Dose and focus latitudes and 2-D effects will be studied on contact patterns. Based on these results, recommendations will be made for reticle birefringence specs.

6520-56, Session 12

Early look into device level imaging with beyond water immersion

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The lithography prognosticator of the early 1980's declared the end of optics for sub-0.5um imaging. However, significant improvements in optics, photoresist and mask technology continued through the mercury lamp lines (436, 405 & 365nm) and into laser bands of 248nm and to 193nm. As each wavelength matured, innovative optical solutions and further improvements in photoresist technology have demonstrated that extending imaging resolution is possible thus further reducing k1. Several authors have recently discussed manufacturing imaging solutions for sub-0.3k1 and the integration challenges.

The Semiconductor industry continues to mature. The imaging solution will be the most cost effective. Lithography and more importantly "imaging solutions" are driven by economics. The technology might be extremely innovative and "fun", however, if it's too expensive it may never see the light of scanner. The industry continues to focus on process tricks and creative science to solve problems in the most cost effective manner. There are many examples of this such as new rinses to reduce pattern collapse1, surface conditioning for LER reduction2, new materials to assist in shrinking contact holes3 and surface treatment of ArF photoresist materials to reduce or minimize slimming4.

Recently exposure tool manufacturers have announced development of NA's \>1 for delivery in the 2006 timeframe for ArF systems. These developments will enable 65nm 1⁄2 pitch and most likely 45nm 1⁄2 pitch imaging with water immersion ArF. There has been speculation that NA's of greater than 1.3 are possible which could also enable the sub 40nm imaging.

This paper will focus on the process capability and requirement for ultra-high NA's that are near the limitation of the immersion fluid. Data will be presented demonstrating the impact of higher refractive index systems on the further extension of ArF Immersion. Calculations of the amount of DOF and EL is required per node is discussed with device level specific test structures have been used for the four main critical levels. Advanced RET's to further explore improvements in critical imaging levels along with dominant mask effects will be discussed.

1. Masuda et al. Proc. SPIE Vol. 5376, 105, Zhang et al. Proc. SPIE Vol. 5376, 103

2. Zhang et al. Proc. SPIE Vol. 5376, 101

3. Hong et al. Proc. SPIE Vol. 5376, 135

4. Cesar Garza et al. Proc. SPIE Vol. 5376, 30

6520-57, Session 12

Extending immersion lithography with high-index materials

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In this paper we report the status of our feasibility work on high index immersion. The development of high index fluids (n\>1.64) and high index glass materials (n\>1.9) is reported. Questions to be answered are related to design of high NA optics, immersion system design for fluid containment and fluid handling, and compatibility of the fluid with ArF resist processes.

On the optical design and manufacturing the challenges are related to the usage of high index glass materials like crystalline LuAG or ceramic Spinel. Progress on the material development will be reviewed.

Progress on immersion fluids development has been sustained. 2nd generation fluids have been established from multiple suppliers. For the practical utilization of 2nd generation fluids in immersion scanners we have been evaluating and testing fluid recycling concepts in combination with ArF radiation of the fluids. Results on stability of the fluid and the fluid glass interface will be reported. Measured data is provided from the testing. Fluid containment with immersion hood structures under the lens has been evaluated and tested for different scan speeds and different fluids. Experimental results on scan speed limitations will be presented.

The application part of the feasibility study includes imaging of LS structures on a 2-beam interference printer (see figure 1), fluid - resist interaction testing with pre-and post soak testing and immersion defect testing using a fluid misting setup. Results of these application related experiments will be presented and discussed. Data on the effects of droplets of the new fluids on patterned resist will be provided along with metrology data on critical feature size. The performance of chemically amplified resists is measured at aggressive feature sizes.

6520-58, Session 12

Development status of high-index lens material LuAG for ArF hyper-NA immersion systems

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The development of the next generation of optical immersion lithography tools with ultra high NA \>1.5 required a last lens element in the projection optics a refractive index of \>1.7. Only the availability of large index material in conjunction with a high refractive index immersion liquid will give the full benefit for hyper NA systems to realize feature sizes with 193nm immersion systems at 32nm technology node.

More than one year ago we proposed the novel material LuAG (Lutetium Aluminum Garnet) as the most promising candidate for this application.

In the last year we checked within a feasibility study the most critical property transmission. We could identified the critical impurities which drop the transmission at 193nm drastically.

Besides of this impurities we found several growth parameter with a

positive influence on the transmission. Considering this key factors we could improve the transmission in a first step by more than one magnitude of order within only few months, the potential for further improvement could be clearly identified.

The evaluation of the laser durability of the LuAG crystal shows very encouraging results despite of the relatively low transmission. Color centers, a chief cause for laser degradation as known from other optical material like CaF2 and BaF2 can be completely suppressed in LuAG, and explain the radiation hardness of the new material.

Based on the obtained results we work currently on demonstrator samples with reduced diameter but expected to meet final specification for 193nm lens blanks. In parallel we establish the sound basis for the upscaling of the crystal diameter to 150-200mm.

6520-59, Session 12

High-index immersion lithography with second-generation immersion fluids to enable numerical aperatures of 1.55 for cost effective 32-nm half pitches

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The semiconductor industry continues to debate the relative merits of water double patterning (easy but high cost of ownership), EUV (difficult with timing and infrastructure issues) and high index immersion lithography (single patterning optical lithography needing a high index last lens element (HILLE)) to identify which will be the most practical and cost-effective technology to follow water immersion lithography at 45 nm half pitches. With good progress on the HILLE, high index immersion with numerical apertures of 1.55 or above now seems possible. We continue our work on delivering a commercially viable high index immersion fluid. We have optimized several of our immersion fluids to meet the required specifications of refractive index and absorbance at 193 nm and are continuing to examine other property/process requirements relevant to actual use, such as fluid radiation durability, last lens element contamination and cleaning, resist interactions and profile effects, and particle contamination and prevention. These studies show that one needs to consider fluid handling issues as well as active fluid recycling in order to maintain optimum fluid properties during the lithographic process for printing sub-45 nm lines with acceptable cost of ownership. Low-absorbing third generation immersion fluids with refractive indices above 1.7 would further expand the resolution of 193 nm lithography to below 32 nm half pitch.

6520-60, Session 12

High-index fluoride materials for 193-nm immersion lithography

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In the system of immersion lithography, NA (Numerical Aperture) is limited by the smallest refractive index material among the resist, the immersion fluid, and the last lens material. Although the high index fluid (n=1.64) has been already reported, fused silica; the highest index material among reality-based candidates for the last lens material; has the refractive index of 1.57 at 193nm. It is obvious that the last lens material might be a bottleneck for the high NA immersion lithography. Some oxide materials such as magnesium oxide single crystal, spinel single crystal and ceramic spinel have been examined as a candidate for the last lens material, however, these materials have so difficult issues in VUV transmittance and other optical properties which further improvement is required to be a reality-based material. On the other hand, fluoride materials have relatively lower index than those oxide materials, however, they might show sufficient VUV transparency, laser durability, and low melting point which is favorable feature to produce the high quality large lens element. We have been investigated various binary and ternary fluoride compounds from the perspective which might show higher refractive index with cubic system. Consequently, we found out one of the fluoride compound, barium lithium fluoride (BaLiF3), which indicates the refractive index of 1.64 at 193nm, higher VUV transparency and less cleavage. We believe that this unique material has promise as the last lens material for the next generation hyper-NA immersion lithography. To meet the requirement for the last lens material, many kinds of optical properties are existed such as VUV transparency, birefringence, index homogeneity, laser durability and so on. The VUV transparency is one of the key issues for the last lens and the internal transmittance at 193nm is about 92%/cm at the moment. Furthermore, 120mm diameter crystal has been grown by using our unique Czochralski method. We will report up to dated results at the meeting.

6520-61, Session 12

Feasibility of 37-nm half-pitch with ArF high-index immersion lithography

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ArF immersion exposure systems with numerical aperture (NA) of over 1.3 are currently being developed and are expected to be used for the node up to 45-nm half-pitch. As for the next generation node, there are multiple candidates, including ArF immersion lithography with a higher NA, EUV lithography, and double exposure/pattering. These candidates have the pros and cons. For ArF immersion lithography with a higher NA, high-index glasses need to be exploited while promising high-index fluids are proposed. Since in the case of EUV there are a lot of issues on light source, resist, and so on, fundamental researches are required to realize the lithography. Finally, the double exposure/patterning has issues on pattern decomposition, throughput, and overlay.

Here, we focus on ArF immersion lithography using high-index fluid only. A refractive index of High-index fluid is typically about 1.64 1-3 and is larger than that of fused silica (~1.56). In this situation, the attainable NA is limited by the index of silica and is at most 1.5, provided that the final lens surface that is in contact with fluid is flat. An exposure system with 1.5 NA does not realize 32-nm hp node, but 37-nm hp node. In spite of this limitation, the system has the advantage of slight alterations from the current system using water as immersion fluid. From an optical point of view, it is necessary to investigate optical characteristics affected by high-index fluids and imaging performance for various patterns smaller than 45-nm hp.

High-index fluids generally have a higher absorption coefficient and a higher temperature coefficient of refractive index (dn/dT) than those of water. Consequently, the issues of thermal aberration caused by high-index fluids need to be examined. First, a simple case that a temperature of immersion fluid changes uniformly is considered. In the case that a thickness of immersion fluid is 1.0 mm, that is comparable to the current system, an index change of 1e-5 yields a focus shift of 11-nm and wave-front aberration of 5.4m * RMS. On condition that RMS of wave-front aberration is to be less than 2.0m * , an index change is tolerable up to 3.7e-6 (Figure 1). This corresponds to 0.0065 K of temperature change using -570e-6 (1/K) as a value of dn/dT. Because it is difficult to control a fluid temperature in this range, the thickness of immersion fluid needs to be reduced. Second, under the practical exposure conditions that take account of non-uniform temperature distribution of immersion fluids and the motion of a step-and-scan system, three dimensional heat analysis has been performed. As shown in Figure 2, thermal aberration in a shot may be affected by temperature distribution in the adjacent shots. We therefore have estimated the thermal aberration and have investigated various ways to mitigate the effects of the aberration.

In addition to thermal aberration, CD sensitivity to errors of mask structure for 37-nm hp will be presented. Based on these results, we will also discuss a feasibility of an ArF immersion exposure system with high-index fluid.

6520-62, Session 13

Application of full-chip optical proximity correction for sub-60-nm memory device in polarized illumination

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As the design rule shrinks to its natural limit, reduction in lithography process margin and high Critical Dimension (CD) error gives rise to use of many Resolution Enhancement Techniques (RET). Recently, one the popular RET method to solve the above problem is polarized illumination.

It is used to enhance the reduced lithography process margin and enhance CD uniformity. Polarization lithography basically uses one sided polarized light source. Therefore process margin increases for smaller design rule patterns.

In this paper, we will present the results for polarization illumination based Optical proximity Correction (OPC) for sub-60nm memory device. First, models for polarization based and non polarization based method will be compared for its model accuracy. Second, the process margin improvement for polarized and non polarized method will be compared and analyzed for poly layer of sub-60nm memory device. Finally, method for further enhancing CD error within 5% for polarized OPC model will be discussed.

6520-63, Session 13

Utilization of optical proximity effects for resist image stitching

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As alternative approaches (i.e. EUV) to pattern smaller device geometries are being explored but none has showed maturity for large volume production, 193nm ArF lithography continues to be the workhorse for semiconductor manufacturing industry. The extension of 193nm lithography heavily depends on the application of Resolution Enhancement Technologies, driving k1 factor to closer to the theoretical limit of 0.25. One effective way to drive k1 lower is the combination of dipole illumination with EPSM. However, one of the disadvantages of dipole illumination is the presence of forbidden pitches due to that the illumination conditions are only optimized for the critical pitches. One obvious solution to address this issue is the double exposure strategy. With the critical pitches are patterned using dipole illumination, the looser pitches are addressed by a less aggressive illumination condition. One concern of this double exposure strategy is that the geometries from the first exposure and the geometries from the second exposure need be seamlessly stitched together for certain device designs. This paper will discuss the utilization of optical proximity effects for image stitching. The images line/space ends are blurred from optical proximity effects. However, the non-sharpness of the image edges can be utilized for image stitches. The optimal stitching conditions, as well as registration tolerance will be studied by simulation. To verify the simulation results, a specific device geometry will be patterned using this stitch strategy. Furthermore, the process margin of this approach will be evaluated experimentally, validating its plausibility for large volume manufacturing.

6520-64, Session 13

Methods for comparative extraction of OPC response

T. E. Zavecz, TEA Systems Corp.

The optical process corrections (OPC) applied to each reticle feature must consider process window response as well as the influence of aerial image artifacts such as near-neighbor proximity and polarization. Response of the design-specific feature-image wavefront and its interaction with the imaging media will differ depending upon small iterations of each features OPC design. In essence, the complex response of aerial image interactions with the translucent wafer film stack also presents a quantifiable influence on the final design selection of the OPC structure. This contribution cannot be derived from a simple process window calculation but is a strong indicator of the designs stability to process fluctuations and must be tuned to the needs of each unique end-process.

In this study, a model-driven method of analysis of photoresist profiles is presented for several OPC designs without regard to the specific mechanics of the design itself. The design of each OPC feature is shown to be a strong contributor not only to resolution and depth-of-focus but also to the stability of final image response; that is the ability of the feature profile to stay centered within the process window with a minimum of drift and variation. Several different, 80 nm half-pitch OPC designs, yielding the same feature size and process window, are compared for their response stability to fluctuations of the process and the exposure tool perturbation signature set. The optimal process corrections on the reticle are therefore dependent upon not only the final image size at some optimal exposure point but also on the ability of the design to maintain feature size within tolerance across all perturbations of the target production process.

Models are developed that allow the extraction of the nonlinear but systematic interactions of several OPC designs with the normal fluctuations experienced across the process window plus those introduced by the toolset and film-stack variation. A method of extracting the systematic component of each feature's design-iteration is presented providing the ability to quantify the specific OPC response sensitivity to systematic changes in the process films as well as drift introduced by the tools of the exposure set. An adjunct to this method provides a quantification of the random contribution of metrology and imaging tools specific to the process, film-stack and tool set of the user.

With this approach individual feature OPC designs can be comparatively characterized to allow selection of the final reticle-design set that optimizes the size and location of the process window. In addition the comparative analysis of OPC design options allows reticle design decisions to be made that enhance the reticle imaging for stability and robustness to process perturbations. Unlike simulation techniques, this method provides a customized analysis that considers the end-process's full process window plus contributions from the unique toolset and film-stack variance. This method therefore reduces the spread of feature variation about the design target and results in higher yields of high-performance final circuits. A budget summary of the systematic perturbation inherent in a typical process is presented as part of the study.

6520-65, Session 13

ACLV driven double-patterning decomposition with extensively added printing assist features (PrAFs)

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Double exposure lithography processes offer significant yield enhancement for challenging circuit designs. Many decomposition (i.e. the process of dividing the layout design into first and second exposures) techniques are possible, but the focus of this paper is on the use of a secondary "cut" mask to trim away extraneous features left from the first exposure. This approach has the advantage of each exposure only needing to support a subset of critical features (e.g. dense lines with the first exposure, isolated spaces with the second one). The extraneous features ("printing assist features" or PrAFs) are designed to support the process window of critical features much like the role of the sub-resolution assist features (SRAFs) in conventional processes. However, the printing nature of PrAFs leads to many more design options, and hence a greater process exploration space, than for SRAFs.

A decomposition scheme using PRAFs was developed for a gate level process. A critical driver of the work was to deliver improved across chip linewith variation (ACLV) performance versus an optimized single-exposure process while providing support for a larger range of critical features. A variety of PRAF techniques were investigated, including block type features, centered assists with varying widths, and constant assist-to-feature spacing (similar to SRAF placement). The optimum solution was evaluated via through-pitch process windows, ACLV performance, and required decomposition code complexity.

6520-66, Session 13

A discussion of the regression of physical parameters for photolithographic process models

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All models currently used for Optical Proximity Correction and related Resolution Enhancement techniques are comprised of an analytical description of the modeled system with coefficients determined by data collected from the physical process. The analytical model is normally based on the Hopkin's approximation of the system because this approximation allows the reticle to be a variable in the exposure system. The analytical component of the model contains terms such as numerical aperture, partial coherence, and wavelength, all of which are

physical parameters that can be directly read from the equipment used to generate the empirical process data. Therefore, these physical parameters can be directly used in the process model and do not need to be modified.

One case example of a physical parameter is the illuminator shape. In an annular exposure system, the center of the exposure system is blocked to allow illumination by high order illumination components. The annular shape can be achieved in different manners. One scanner manufacturer uses a shape cut in a metal form to achieve an annular illumination condition while another scanner manufacturer uses a lens system to achieve the same illumination condition. Both of these systems have the same inner and outer diameters, resulting in the same annulus and therefore the same illumination technique. However, experimental data show that for the exact same settings, the annular illumination shape is detectably different. This is a first order system difference that is the result of different systems. Further differences can be found due to scanner to scanner variations in either lens shape or aperture shape. These differences create a need for physical parameters to be regressed during fitting of empirical data to the analytical model.

This paper will discuss the position of the need to regress what initially appear to be constant physical parameters during the model fitting process. The study will use equipment variability to demonstrate the range of physical constant impact upon the accuracy of a process model.

6520-67, Session 14

Latest results from the hyper-NA immersion scanners S609B and S610C

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Nikon released the world's first hyper-NA immersion scanner, theNSR-S609B with NA 1.07 at the beginning of 2006. With the highest NA lens using all-refractive optics, a flexible illumination system, and POLANO polarized illumination, the NSR-S609B is capable of manufacturing devices with better than 55 nm resolution

In addition, Nikon has announced the release of the NSR-S610C. With the world's highest NA lens (NA 1.30), the S610C can comfortably achieve 45 nm critical layer volume production with k1=0.30. Nikon's proprietary catadipotric lens design for the S610C provides the lowest flare and eliminates lens heating, resulting in stable imaging.

Because the S609B and the S610C are built on the same platform, a number of advantages can be realized. First, both the S609B and the S610C utilize a tandem stage optimized for immersion lithography. The tandem stage consists of separate exposure and calibration stages. This allows for continuous flow of immersion water, and for calibration of the exposure tool during wafer exchange. As a result, throughput of greater than 130 wph is achieved, evaporative cooling of the stage during wafer exchange is prevented, and focus drift, baseline changes, and other issues with tool stability are eliminated. In this way, the tandem stage can achieve productivity and accuracy at the same time.

In addition to the calibration functions described above, the Integrated Projection Optics Tester (iPot) mounted on the calibration stage can manage the long term performance of the projection optics. By measuring the wave front aberration, the polarization quality of POLANO, and the pupil fill, iPot supports the optimization of the imaging performance.

Nikon's polarized illumination system POLANO provides improved contrast with no loss of illumination power. This provides increased process margin for 45 nm volume production using immersion lithography.

Finally, Nikon's proprietary local fill nozzle installed on the S609B and the S610Chasbeen shown to eliminate immersion defects from bubbles, watermarks, and particles.

In this presentation, the newest data from the S609B and S610C will be presented.

6520-68, Session 14

Immersion exposure tool for the 45-nm HP mass production

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With immersion technology moving from a development phase to a mass production phase, we at Canon have developed our first commercial immersion tool, FPA-7000AS7, adopting a new concept of the 7000 platform.

The FPA-7000AS7 uses a catadioptric lens with a numerical aperture (NA) greater than 1.3 to realize 45nm node mass production. We have successfully developed a new immersion system, Liquid Film Flow method, in order to achieve a defect-free system. The Liquid Film Flow method does not disturb water movement, minimizing the impact on the wafer to create an environment free from immersion-specific defects.

The 7000 platform, common to both the FPA-7000AS7 ArF immersion tool and FPA-7000AS5 ArF Dry machine, has various functions to achieve the extremely high performance which is essential for the 45nm HP and beyond. Vibration of the projection lens caused by stage scanning has become a critical issue at the 45nm HP, and therefore must be controlled to extremely low levels in order to realize sufficient imaging performance. To achieve this, the 7000 platform employs a new vibration control body structure that completely separates the projection optics and metrology system from vibration sources, such as the reticle and wafer stages. In addition, a Two Wafer Stage system is adopted in order to achieve both high throughput performance and highly accurate focus and overlay performance. With the Two Wafer Stage system, multiple metrology measurements are performed on one stage while simultaneously exposing on the other stage. This parallel sequence improves focus and alignment accuracy by enabling focus mapping across the entire wafer with the multi-focus sensor and multiple point alignment. Moreover, the 7000 platform is equipped with several in-situ metrology systems, such as iPMI (in-situ phase measurement interferometer), TTR-calibration system. Through the usage of these in-situ metrology systems to characterize wavefront aberrations, effective light source shape and the polarization state, the 7000 platform both optimizes and automatically maintains the machine optimal condition.

In this presentation, we will show total imaging performance of FPA-7000AS7 at NA greater than 1.3 with water-immersion. Furthermore, we will present the features and performance of the 7000 platform along with simulation and experimental results.

6520-69, Session 14

Performance of a 1.35NA ArF immersion lithography system for 40-nm applications

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Water based immersion lithography is now widely recognized a key enabler for continued device shrinks beyond the limits of classical dry lithography. Since 2004, ASML has shipped multiple TWINSCAN immersion systems to IC manufacturers, which have facilitated immersion process integration and optimization. In early 2006, ASML commenced shipment of the first immersion systems for 45nm volume production, featuring an innovative in-line catadioptric lens with a numerical aperture (NA) of 1.2 and a high transmission polarized illumination system. A natural extension of this technology, the XT:1900Gi supports the continued drive for device shrinks that the semiconductor industry demands by offering 40nm half-pitch resolution. This tool features a projection lens based on the already proven in-line catadioptric lens concept but with an enhanced, industry leading NA of 1.35. In this paper, we will discuss the immersion technology challenges and solutions, and present performance data for this latest dual wafer stage TWINSCAN immersion system.

6520-70, Session 14

Exposure and compositional factors that influence polarization induced birefringence in silica glass

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Silica glass exhibits a permanent anisotropic response, referred to as polarization induced birefringence (PIB), when exposed to short wavelength, polarized light. This effect can become critical in high-NA immersion ArF lithography tools because in those instruments the polarization state of the exposure light needs to be controlled and maintained; PIB can alter the incident polarization. The magnitude of PIB in silica has been empirically correlated with the OH content of the glass. Our recent studies pertaining to PIB have focused on careful characterization of PIB, with particular emphasis on understanding all of the contributions to the measured birefringence signal and finally extracting only that signal associated with PIB. We will demonstrate that a critical contributor to the total birefringence signal is birefringence that comes from exposure beam inhomogeneities. With our 'PIB correction' we are able to show that PIB is proportional to the OH content of the glass. Further, we are also able to demonstrate that chlorine, a possible contaminant in silica manufacturing, does not significantly contribute to PIB. Our studies lead us to propose a mechanism for the evolution of PIB.

6520-71, Session 14

XLR 500i: recirculating ring ArF light source for immersion lithography

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As Argon Fluoride (ArF) lithography moves into high volume production, ArF light sources need to meet performance requirements beyond the traditional drivers of power and bandwidth. The first key requirement is a continuous decrease in Cost of Ownership (CoO) where the industry requirement is for reduction in ArF CoO in line with the historical cost reduction demonstrated for Krypton Fluoride (KrF) light sources. A second requirement is improved light source performance stability. As CD control requirements shrink, following the ITRS roadmap, all process parameters which affect CD variation need tighter control. In the case of the light source, these include improved control of bandwidth, pulse energy stability and wavelength. In particular, CD sensitivity to exposure dose has become a serious challenge for device processing and improvements to laser pulse energy stability can contribute to significantly better dose control.

To meet these performance challenges Cymer has designed a new dual chamber laser architecture. The Recirculating Ring design requires 10X less energy from the Master Oscillator (MO). This new configuration enables the MO chamber lifetime to reach that of the power amplifier chamber at around 30Bp. In addition, other optical modules in the system such as the line narrowing module experience lower light intensity, ensuring even longer optics lifetime. Furthermore, the Recirculating Ring configuration operates in much stronger saturation. MO energy instabilities are reduced by a factor of 9X when passed through the Ring. The output energy stability exhibits the characteristics of a fully saturated amplifier and pulse energy stability improvement of 1.5X is realized. This performance enables higher throughput scanner operation with enhanced dose control. The Recirculating Ring technology will be introduced on the XLR 500i, Cymer's fifth-generation dual chamber-based light source built on the production-proven XLA platform. This paper will describe the design details and performance characteristics of the new laser architecture.

6520-72, Session 15

Catadioptric projection lens system for 1.3 NA scanner

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In the history of DUV (Deep Ultra Violet) microlithographic lens design, three kinds of leaps have occurred to maintain the progress of technology of the semiconductor industry. The first step is the application of aspherical elements. This allowed us to increase NA up to around 0.9. The second innovation is water immersion. Even lower maximum ray angle on the imaging plane than dry lens can achieve NA of 1.07, thanks to the 1.44 refractive index of water, because numerical aperture (NA) is defined as product of sine of maximum ray angle on the image plane and refractive index of image space. The latest technological jump is the development of catadioptric lens systems, which is roughly defined as the combination usage of refractive element(s) and reflective element(s). The catadioptric system allows us to achieve a full field 1.3NA projection lens.

It is well known that concave mirror(s) help to simplify and provide room to increase the maximum NA of the optical system. The main advantage of using the mirror is easier control of the Petzval condition, which is the necessary condition to get a flat image plane. In the case of dioptric systems, the combination of strong negative power lenses and large diameter positive lenses is used to satisfy the Petzval condition. This is why the dioptric lens system has a glamorous shape which consists of large bulge(s) and slim waist(s). However, this glamorous shape is not so attractive for aberration control and compact dimension design. On the contrary, the catadioptric system has a rather smaller diameter and not so glamorous appearance because of the great contribution to improvement of the Petzval condition of the positive power concave mirror. This shape gives the designer room to increase the NA with better aberration control in the optical design.

In addition to Petzval condition control, chromatic aberration control is another advantage of the catadioptric system. Our catadioptric lens design is optimized to minimize the chromatic aberrations for both axial and lateral color. Furthermore, the concave mirror location close to the pupil is suitable to compensate uniform astigmatism, which may be generated due to some strong RET (Resolution Enhancement Technology) imaging conditions. This astigmatism control is achieved by deforming the mirror surface like the adaptive optics for VLT (Very Large Telescope).

The challenge in optical design for catadioptric systems is how to separate up beams to the concave mirror and down beams from the concave mirror. Though there are various ways to separate the beams, only off-axis field type lenses are suitable for the most advanced DUV projection lenses. That is, the exposure field must be offset from the optical axis.

As a result, we have selected a multi-axis lens configuration to obtain the advantages of the catadioptric design most effectively.

We have also applied some dedicated catadioptric technology for realizing the lens in the manufacturing process such as alignment techniques for multiple barrels in the multi-axis configuration, aberration analysis technology for off axis imaging field, etc.

In this paper, the completed final lens performance of our 1.3NA catadioptric system will be also reviewed.

6520-73, Session 15

New projection optics and aberration control system for the 45-nm node

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Mass production at the 45 nm node is demanding projection lenses with higher NA and lower lens aberrations.

We have developed two types of ArF projection lenses: one for dry exposure tools and another for immersion exposure machines. Both lenses are installed on the news exposure tool platform, specifically developed for 45 nm massmass production and beyond.

The projection lens for dry exposure is dioptric type with NA 0.93, while the NA\>1.3 projection lens for immersion exposure requires catadioptric type. Both lenses feature super-high NA, ultra-low aberrations and polarization control, to achieve the highest imaging performance. In addition, these lenses are equipped with a flexible and highly accurate aberration compensation system that enables 45nm node mass production.

In this paper we will present some measurement results of wavefront aberration, image field deviation and distortion of these lenses, which are appropriate for 45nm node lithography. Additionally, we will discuss

polarization performance of projection lens which must be considered in Hyper-NA optics.

Along with these basic performance, one of the most important issues concerning exposure equipment is the stabilization of aberrations during machine operation.

The new exposure tools have an automatic aberration control system, which integrates some aberration measurement units and compensators. A software installed in the tool automatically determines the optimum lens conditions, and the best image imaging performance is always ensured. The tool platform is equipped with an in-situ metrology system that enables measurement of various performances characteristics, including local flare, all without the usage of resist and at high speeds. The lenses possess multiple compensation units that adjust aberrations with high degrees of freedom. All terms of 3rd order (C5 to C9) and several higher order aberrations are tunable in these lenses.

Some of these compensation units realize real-time aberration control synchronized to the scanning motion. These units have an high-speed response with high placement accuracy within a few nanometers. This control system can correct issues associated caused by with exposure heat load and reticle deformation. The imaging performance is guaranteed even after production ramp- up as well.

In this paper we will provide a detailed explanation of the aberration control system and present actual performance results.

6520-74, Session 15

Integration of a new alignment sensor for advanced technology nodes

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In this paper we present alignment and overlay results of the advanced technology nodes. These results were obtained on specially generated wafers as well as on regular manufacturing-type wafers. For this purpose, a new alignment sensor was integrated in lithography tools of a mass manufacturing facility. This sensor was especially designed for mark layout flexibility, as well as to improve upon the performance of the alignment sensors currently in use. Further areas of sensor improvements can be found in the addition of illumination wavelengths for improved alignment robustness, in reduction of required alignment target size and in improved sensor stability.

Using various overlay indicators and optimization methodologies, the best performing alignment marks and strategies were selected. Alignment and overlay results will be shown, using the applicable alignment mark subsets. We will report on alignment parameters such as mark signal strength, mark fit quality and wafer alignment grid residuals. Long-term stability data, alignment process robustness data as well as joint Toshiba-ASML application opportunities will be discussed.

6520-75, Session 15

Ultra-narrowed injection lock laser light source for higher NA ArF immersion lithography tool

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The 193-nm lithography has moved to the mass production phase and its target node is shifting from 65 nm to 45 nm. And the ArF-immersion technology is even spotlighted as the enabling technology for below 45nm node. We have already released an injection lock ArF excimer laser with high power and high repetition rate GT60A (60W, 6000Hz, 10mJ, 0.5pm/ E95%) to ArF immersion market in Q1 2006.

In the technology below 45nm node, a light source will be required narrower spectrum and the high average laser power.

The GT61A ArF laser light source of the ultra line narrowed spectrum which meets the demand of hyper NA (NA \> 1.3) immersion tool is introduced. The GT61A aimed at improving a spectrum performance from value E95% 0.5pm of GT60A. The spectrum performance 0.3pm or less was achieved by developing an ultra line narrowing module newly.

Moreover, in 45nm node, since it corresponded to indispensable OPC (optical proximity correction) and a narrower process window, improved stabilization of spectrum performances was performed by bandwidth control technology. Newly designed Bandwidth Control Module (BCM) includes high accuracy measurement module which support the narrower bandwidth range and active bandwidth control module. It also contributes to the reduction of the tool to tool differences of the spectrum for every light source.

In the technology for below 45nm node, the high average laser power is required for high throughput demand of the double exposure or the double patterning. So we are developing 90W laser light source. We will report the performance of 90W operation.

6520-77, Session 15

Demonstration of sub-45-nm features using azimuthal polarization on the 1.3NA exitech immersion microstepper

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The practical extendibility of immersion lithography to the 45nm node is being investigated on a 1.30NA immersion projection microstepper. Preliminary implementation of various aperture designs and polarization configurations have been used to demonstrate imaging beyond the 90nm pitch. Optical proximity correction (OPC) and other resolution enhancement technique (RET) strategies coupled with resist stack optimization of dual-layer bottom anti-reflective coating (BARC) systems offer a growing platform of materials and illumination configurations for the 45nm node. In this demonstration of a RET strategy, linear-polarized light is selectively rotated at the coherence aperture to simultaneously image sub-90nm pitch features along the x and y axes within the same field. SEM images demonstrate the capability of the immersion micro-exposure tool (iMET) to support dual-orientation imaging with resolution down to the 84nm pitch.

6520-78, Poster Session

Optical performance enhancement technique for 45-nm node with binary mask

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In order to realize 45-nm node lithography, strong resolution enhancement technology (RET) will be needed. And the resolution of binary mask becomes as much of the phase shift mask (PSM) when its size is smaller than 45-nm node [1]. In this paper, we present a way to improve the resolution of conventional binary mask. The improvement is proven by 3D rigorous simulation and experiment. When the structure which has patterned binary mask conformally deposited with transparent oxide film, the oxide film has relief depth between etched and unetched Cr layer. This structure makes intensity of first order diffraction increased while that of 0th order decreased due to the topographic effect [2]. As the application of this structure, we can enhance normalizes image log slope (NILS) over binary mask. Simulation of 45-nm node on the variation of NILS depending on duty ratio and the thickness of oxide shows that more than about 10% increase of NILS compared to the binary mask. In addition, the result of experiment of 80-nm node DRAM gate layer shows about 12 % increase of NILS over binary mask. This effect is maximized when the oxide thickness is between 1000 Å and 2000Å. Considering the aspect ratio occurring as it gets thicker, about 1000Å seems the most appropriate for the real device application.

6520-79, Poster Session

Size tolerance of subresolution assist features for sub-50-nm node device

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For sub-100 nm node devices, insertion of sub-resolution assist features (SRAFs) between main features and off-axis illumination is being used to improve process window and resolution. SRAF insertion application started on a gate-poly layer spread to other critical layers. As the device is scaled down, the SRAF size decreases drastically and the distance between main features and SRAF is reduced. However, it is a burden for a mask manufacturer to fabricate SRAF patterns because mean-to-target (MTT) of SRAF is much larger than that of main feature. Below 50 nm node design, the large MTT of SRAF makes it difficult to generate desired SRAF patterns. In addition, SRAFs have the large size variation. The size variation of SRAFs on a mask leads to increase the printability of SRAFs and restrict a SRAF generation rule for acquiring process margin. Especially, on a critical gate-poly layer, this is one of the critical issues.

In this study, the size tolerance of SRAFs for sub-50 nm node device is discussed. Below 50 nm node design, mask topography effects can not be neglected because exposure wavelength is similar to a mask pitch from main feature to SRAF or SRAF to SRAF. It is investigated that the size variations of SRAF affect its printability with decreasing device node based on a rigorous electromagnetic field simulation. This size tolerance of SRAFs can be one of the specifications for sub-50 nm mask production.

6520-80, Poster Session

A method for generating assist-features in full-chip scale and its application to contact layers of sub-70-nm DRAM devices

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This paper introduces our in-house tool for automatic generation of assist-features in a full-chip scale, and demonstrates its application to real devices.

ArF is still used as a main light source for lithography of critical layers due to failure or delay of development of alternative light sources. Hence the resolution enhancement is mainly depends on increasing the NA of the projection lens or on decreasing the k1 value. The process margins, especially DOF, play a more important role in both the approaches than ever.

It has been well-known that properly designed assist-features can give significant improvement in the process margin of lithography, but the designing the assist-features is generally not a simple task. If the pattern area is very small, or if the patterns are well isolated so that the proximity effect can be safely ignored, then it is not very difficult to design assist-features. Actually there are several methods which are readily applicable to these simpler cases. However it becomes quite challenging if the pattern area is not very small, or the patterns are not isolated.

Our main products generally have large pattern areas which easily occupy most of the available imaging field of today's scanner, 26mm x 33mm, and the patterns are not isolated even in core and peripherals. Hence most of the known approaches cannot applied to our main products. Furthermore, k1 factors are becoming lower in every generation of our devices so that the proximity effect cannot be safely ignored anymore, hence a conventional rule-based approach to the assist-feature generation are not as applicable as it were.

A new method for design of assist features and an in-house tool to support this method have been developed internally. This method is a model-based and can cover the full pattern area of our main devices in a reasonable computation time due to its algorithm. This method has been combined with the model OPC procedure to give efficient procedure of assist-feature generation and OPC of main features. This method carefully and automatically control the assist features not to print on the wafer, with full consideration of the proximity effects. The minimum size of patterns and spaces are also automatically controlled not to violate the mask manufacturability conditions, which have been given by our in-house mask shop. This method has been successfully tested on a sub-70nm DRAM device in a full-chip scale.

6520-82, Poster Session

Process window optimization of CPL mask for beyond 45-nm lithography

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Chromeless Phase Lithography (CPL) has been used in sub-wavelength lithography resolution enhancement techniques (RET). As the device line width gets smaller toward 45nm technology and beyond, CPL process window optimization plays an important role to extend the limit of current optical lithography. In this study, 4 major areas of process window optimization are performed. Firstly, CPL data handling optimization and three-zone layout splitting are studied. Mask data are split into pure phase, zebra and pure chrome type based on the feature size. At the resolution limit, pure phase mask data type is used because the MEEF is low. Zebra mask data type will be used for feature size that are bigger than 75nm, while pure chrome feature is applied for feature sizes that are bigger than 180nm. Secondly, OAI and customize illumination optimization is studied. The 2D overlap region of the diffraction order within the entrance pupil is analysed. The investigation shows that process window can be improved through background noise reduction and illumination optimization. Thirdly, polarization impact on high NA application is studied. Simulation results have shown DOF can be improved by 50% through the effect of polarization. Lastly, CPL mask quartz depth optimization is studied. The investigation shows 180 degrees phase is not optimized for 193nm lithography. The effective phase for 193nm CPL is at 205 deg. With the above process window optimization, CPL demonstrates reasonable good process window on wafer printing. DOF with more than 0.3um on 65nm line with 160nm pitch has been achieved with using CPL under 0.85NA.

6520-83, Poster Session

SRAF placement and sizing using inverse lithography technology

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The use of sub-resolution assist features (SRAFs) is a necessary and effective technique to mitigate the proximity effects resulting from low-k1 imaging with aggressive illumination schemes. This paper investigates the application of one implementation of Inverse Lithography Technology (ILT) to determine ideal SRAF solutions. In contrast to traditional rule-based methods in which SRAF placement and size are typically predetermined and frozen in place, unmodified during OPC, ILT allows for the simultaneous placement and sizing of SRAFs during target inversion to maximize image quality while also maintaining margin against sidelobe printing. Furthermore, ILT enables SRAF placement for random as well as periodic patterns. In this paper, SRAF placement using this approach is studied through simulations and comparison with an analytical center-of-gravity approach proposed by Manakli et al. The computed mask and the corresponding silicon data from 45nm contact layer wafers are shown to illustrate effectiveness of ILT-generated SRAF features.

6520-84, Poster Session

Optimal SRAF placement for process window enhancement in 65-nm/45-nm technology

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The existence of pitch range with depth of focus below a sustainable

limit is a well known factor in lithography. Such 'forbidden pitch' range limits designers' ability to pack more functionality in a logic chip. There are ways to increase the process window of such pitch regions, e.g. 1) move to an immersion tool, 2) tweak the illumination conditions or 3) use an optimal Sub Resolution Assist Feature (SRAF) strategy. While the tool option is an expensive proposition, the illumination conditions are often dictated by other features such as SRAMs in 65nm/45nm logic technology. Once the illumination condition and the tool selection are fixed, a careful placement of SRAFs can be used to boost process window across the pitch range. However the standard SRAF strategy that has been followed historically is not enough to boost the process window of these 'forbidden pitches' sufficiently to allow sustainable manufacturing. With shrinking technology node, placement of SRAF is becoming rather difficult due to space limitations between concerned features and mask house's ability to manufacture mask with small assist features and smaller aspect ratios. In many cases the number of SRAF that can be inserted between main features in a symmetrical way is not enough to boost the process window.

The SRAM rules are largely developed based on printability and process window improvement for given space range between adjacent critical features and the placement of the SRAFs has traditionally been symmetrical about the main feature. In an intermediate pitch range, for example, placement of 2 SRAFs lead to their printing while 1 SRAF located at the center of the space between the critical features is not enough to increase the process window of 'forbidden pitches'. We have shown that one way to increase the overall process window is to move one SRAF closer to one main feature, while avoiding printing. In an array of critical lines, for example, each critical feature can have one SRAF closer to and one SRAF away, thus maintaining a continuity of SRAF coverage for each critical feature. Such a strategy allows one to avoid SRAF printing while increasing the depth of focus. We also describe how such asymmetrical placement of SRAF can be very beneficial in layouts where a critical feature is adjacent to non critical features. In this case also, SRAFs can be placed closer to the critical feature and away from the non critical features. The placement of these will depend on the tolerance needed for both critical and non critical lines. While critical lines have lower tolerance and hence needs more SRAF coverage for process window improvement, the non crictial features have relaxed tolerance and therefore can live with less SRAF coverage. In this paper we demonstrate how wafer data confirm process window boost from such asymmetrical placement of SRAFs in gate layer for 65nm. We show how to determine the optimal placement of SRAF in such cases. We finally recommend some rules that can be used for 45nm node based on such results.

6520-85, Poster Session

Intensity weighed focus drilling exposure for maximizing process window of sub-100-nm contact by simulation

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In our previous study [1], we introduced the method of intensity weighting over various image planes for FLEX (Focus Latitude Enhancement eXposure) process. By higher energy weighting on the best focus image for the triple focal plane exposure, it demonstrated higher contrast over wide focus range than conventional FLEX, accordingly achieved the best performance on DoF (Depth of Focus), exposure latitude, proximity and CD uniformity. However, this technique limits the production capability by the increased number of images.

Thanks for all the technology developments on RET (Resolution Enhancement Technology) with tool functionality, which is related to focus drilling method in scanner system. Hence there have been several papers addressed the focus drilling technique with high frequency illumination source recently, the focus drilling technique enables to have more continual image planes over focus range on advanced scan and repeat system while scanning the image with single uniformity energy level over various focus range [2-3].

In this paper, the approach combining focus drilling and intensity weighting was first introduced to strengthen the potential of process. As can be seen in figure 1, the focus drilling and intensity weighting achieved higher EL (Exposure Latitude) and DoF than the conventional FLEX at the same focus range. Since the hardware resource for focus drilling and intensity weighting is not available in our study, we will only demonstrate the combined technical concepts over following items through commercial simulation tool of Prolith Ver. 9.31.

1) Optimum focus range comparison between illumination sources by wavelength (KrF & ArF).

2) Quantify the level of depth of focus enlargement and the lost in exposure latitude.

3) The advantage of combination of focus drilling and intensity weighting on focus range.

6520-86, Poster Session

Process margin improvement using custom transmission EAPSM reticles

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Low k1 lithography poses a number of challenges to the process development engineer. Though polarization and immersion lithography will allow us to create processes at lower k1 than previous paradigms allowed, the lithographer will quickly be looking for RET's to push to the ultra-low k1 regime, or to extend older generation tools and avoid the aforementioned expensive options. Reticle transmission is a useful RET that can enable a low k1 process by increasing image contrast. With work performed in conjunction with our MP Mask facility, we have been able to develop custom-transmission EAPSM reticles. Reticle transmission optimization can be carried out through simulation. Optimum transmission varies depending on optical parameters and feature size. Moreover, when working with 2D patterns, reticle transmission can be optimized for weaker features, without sacrificing image contrast on primary features.

Process improvement by optimizing reticle transmission will be explored for a variety of device types using both 248nm and 193nm lithography. Simulation, custom-transmission reticle fabrication, and empirical wafer results will be presented.

6520-88, Poster Session

Verification of high-transmittance PSM with polarization at 193-nm high-NA system

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High-transmittance phase shift mask (HTPSM) and high numerical aperture (NA) imaging with polarized illumination had been proposed as one of the solutions of the 65nm technology node and beyond. Aerial image simulations and experimental exposure results confirmed the advantages of the polarized illumination for high NA imaging had been introduced.

However, influence of transmission rate of the PSM status upon imaging performance had not yet been fully investigated. We had studied the influence of different transmission rate PSM with polarized illumination upon imaging performance including depth of focus (DOF), exposure latitude (EL) and line edge roughness (LER).We will present simulation of normalized intensity log slope (NILS) vs. mask transmission rate for the through pitch line space patterns and compare with experimental data.

In this paper, masks of various transmission rates from 6%~30% have been designed. The print images had been investigated for with and without polarized illuminations of 193nm high NA tool. According to the experimental and simulation results, the high transmission rate mask could enhance resolution for 50nm node and beyond.

6520-20, Poster Session

A litho-only solution to double patterning

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This paper describes a new double patterning technique, avoiding etches in between the lithography steps, thus simplifying the double patterning process flow.

Double patterning has gained importance during the past few years. Immersion lithography with double patterning has become one of the candidates to bring us to the next node. The other possibilities to keep up with the ITRS-roadmap are immersion lithography with higher index fluids and EUV lithography. Whereas the latter two need structural changes in infrastructure, immersion lithography with double patterning makes use of the existing infrastructure. Taking this into account, immersion lithography with double patterning becomes a serious candidate to reach the 45 nm node. This technology may even bring us to the 32 nm node.

Most of the currently known double patterning techniques have relatively complex process flows, which keep them from being used in production. One of the complicating factors is the use of etch steps in between the lithography steps. This etch step is necessary to transfer the pattern of the first resist layer to an underlying hardmask before a second exposure can be done. Another complicating element, arising in several known double patterning techniques, is the translation of overlay error in CD-error. This translation occurs when a feature is printed in two exposures, i.e. not features but the spaces between them are patterned, patterning the left and right edge of a feature in different exposures.

We propose an innovative method of double patterning that does not include transfer etch in between the lithography steps. This will simplify the double patterning process. Furthermore, each feature is patterned completely in one exposure, for which CD-value is not affected by overlay error. In the paper the feasibility of the new method is presented, including data on CD-uniformity, line edge roughness and process latitude.

6520-89, Poster Session

Novel lithographic technique for differential exposure of distinct patterns on the same mask

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For most advanced NOR/NAND devices(from 90nm technology node and below) it is particularly critical to optimize lithography process both for very dense patterns (lines and spaces, contacts array) and isolated one (circuitry/source contacts) present on the same layout: resolution requirements make the illumination mode mainly studied and dedicated for dense array pattern; on the other side a non optimized illumination mode for isolated pattern could lead to a drastic reduction of overall process window, defined as the intersection between process window of every kind of pattern present on the mask.

In order to overcome this issue, isolated and dense patterns could be split up on different masks: unfortunately this option is general not possible or not advantageous because of tight overlap specification or process reasons.

In this paper we propose to separate the isolated and dense pattern printing, not by using different reticles but by exposing each kind of pattern, present on the same mask, during two distinct, specifically optimized and successive steps: this could be done by exploiting different best focus/dose condition set up for each exposure step.

For this purpose we thought that a 90 degree alternated phase shift mask (Alt-PSM) could be a solution: in fact, in this kind of reticle, the aerial image intensity coming from 0 degree phase is shifted in best focus position compared to 90 degree ones, allowing a differential exposure of this two kind of pattern.

In this paper, performance of this new technique for lines /spaces and contacts patterns down to 50nm technology node is illustrated both in terms of optical simulation and in terms of experimental verification: the latter was possible thanks to a specific resist choice and optimization and the availability of a dedicated test mask.

6520-90, Poster Session

A study of double exposure process design with balanced performance parameters for line/space applications

J. Zhu, P. Wu, Q. Wu, H. Ding, X. Li, C. Sun, Shanghai Hua Hong NEC Electronics Co., Ltd. (China)

As the semiconductor fabrication groundrule has reached the 32 nm node, in general there are three available approaches for the photolithography solution, the double exposure with 1.35 NA immersion, the high refractive index immersion, and the extremely ultra violet (EUV) lithography. Among the three, the easiest approach seems to be the double exposure method at an effective numerical aperture (NA) of 1.35. However, there are still challenges in the design and optimization of the process, such as, the use of appropriate illumination condition, the choice of a good photoresist, and the design of an optical proximity correction (OPC) strategy. Besides these considerations, there is still the question as whether we really need the double etch process. In our study, we have used a 248 nm exposure tool and a well chosen photoresist to study the photo performance parameters in the merge of two photo exposures. At a numerical aperture (NA) around 0.7, the minimum groundrule we can achieve is the one for a 75 nm logic process with minimum pitch around 220 nm. One approach will be that the features with pitches wider than 440 nm are completed in a single exposure, which includes various isolated lines and spaces, line and space ends, two-dimensional structures, etc. This strategy essentially puts the single exposure pattern under the 0.18 μm logic like pitches where mild conventional illumination can produce a balanced performance. Under typical illumination conditions, the photolithographic process under 0.18 μm like ground rule is well understood and the optical proximity correction is not complicated. The remaining issues are in the dense pitches, where the double exposure kicks in. We have demonstrated that the double exposure with single development can achieve a process window large enough for a 75 nm logic like process and the OPC behavior such as line through pitch is manageable although OPC correction strategy may require substantial improvement to accommodate two individual exposures. In the paper, we will demonstrate the result of our study of the basic photolithographic performance indicators, such as the exposure latitude (EL), the depth of focus (DOF), the CD through pitch and the mask error factor (MEF) for the optimized process. And we will discuss the choice of photoresists for this special application. It seems that a photoresist with a balanced performance for both the line and space is necessary to realize a good double exposure process. In this paper, we will also present our simulation result to explore the limit of such approach.

6520-91, Poster Session

The improvement of photolithographic fidelity of two-dimensional structures through double exposure method

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With the semiconductor fabrication groundrule approaching the 32 nm node, double exposure method with 1.35 NA immersion seems to be the primary candidate due to its relative easiness to implement when compared to the other two competitors, the high refractive index immersion and the 13.4 nm extremely ultraviolet (EUV) lithography. However, the splitting of one mask into two is not a trivial task. Besides, there is still a lot of work in the optimization of the two exposure conditions, which includes the selection of the best splitting pitch, the optimization of the illumination conditions, the choice of a good photoresist, and the finding of best splitting method for two-dimensional (2D) features with aggressive pattern density. In this paper, we would like to discuss about the best splitting method for several typical 2D structures, such as opposing line (or space) end shortening, both in isolated environment and sandwiched within dense environment, T-like structures with narrow gaps, the H like structures, etc. From our recent experimental studies, we have learnt that, for line and space photolithography, the optimized illumination condition for dense printing and good CD through pitch variation may have substantial partial coherence, i.e., the sigma value is very close to 0.5. When compared to the single exposure processes, which will typically use more annular condition, a sigma of 0.5 can generate larger mask error factor (MEF) for isolated features. This will put more pressure on the precision of the already challenging optical proximity correction (OPC) because the doubly exposed patterns and singly exposed patterns follow two different models. Therefore, it will be very helpful if we can make the 2D structures more lithographically friendly through the use of double exposure method though the initial motivation for double exposure is to split dense features into relatively more isolated ones to improve process window. In our study, we find that the extra degrees of freedom in the double exposure method we have can be

utilized to repair some intrinsic printing deficiency, such as, line end shortening and some corner rounding. In this paper, we will analyze each typical 2D structure and, for each splitting method of the typical 2D features we study, we will discuss its capabilities in realizing good process windows, the MEF, and OPC correction easiness.

6520-92, Poster Session

Double patterning with multilayer hard mask shrinkage for sub-0.25 k1 lithography

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In order to reduce the overall size of device features, continuing development in the low k1 lithography process is essential for achieving the feature reduction. Although ArF immersion lithography has extended the feature size scaling to 45nm node, investigation of low k1 lithography process is still important for either ArF dry or wet lithography. Double patterning is one procedure pushing down the k1 limit below 0.25. It combines the multilayer hard mask application and resist shrinkage process to get the feature size reducing to quarter pitch of the illumination limit. In recent spin-on hard mask studies, silicon containing bottom antireflective coatings (BARC) have been developed to combine the function of reflective control and great etching selectivity to the photoresist. Trilayer resist including the photoresist, silicon containing BARC and planarizing organic underlay can improve the reflectivity by optical index tuning of dual hard mask layer effectively and reduce photoresist thickness to avoid the pattern collapse with small features. In our study, we found some interesting characteristics of trilayer resist which could be used for double patterning technology and made the low k1 process more feasible. This procedure we investigated can make the feature size of half pitch reduce to 37nm and beyond at 0.92NA under ArF dry lithography. Among the resolution enhancement for ArF dry illumination, double patterning scheme, overlay controllability and pattern transfer process by reactive ion etching (RIE) will be discussed in this paper.

6520-93, Poster Session

Sub-k1 = 0.25 lithography with double patterning technique for 45-nm technology node flash memory devices at λ = 193nm

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An enormous pressure is currently put on Resolution Enhancement Techniques to meet the deadline for the development of high density memory devices. The prevailing conviction is to consider water immersion lithography as the choice for manufacturing 45nm technology node devices. Even if a huge effort to face immersion specific issues has been done (on defectivity, micro-bubbles, contamination, overlay control, hyper NA imaging), a technology solution to image the desired features and densities must be available till now in order to anticipate all the steps involved in the process integration before the complete assessment of the immersion infrastructure.

Moreover, the forecasted solutions for 32nm and 22nm technology nodes remain uncertain, strongly depending on current and near future development of high index fluids for immersion lithography and EUV availability. These temporal lacks of technology options are forcing scanner suppliers and IC manufacturer to include also double exposure in the group of viable choices for future development.

Double patterning (double exposure and double etch) is surely a fascinating solution for overcoming the physical resolution limit of k1 = 0.25 of imaging systems. Various papers in these last two years demonstrated an increasing interest in the exploration of such kind of technique to extend as much as possible ArF dry exposure tools. Though the concept of this technique is simple and well known, there are various technical issues which must be solved before moving to a real implementation in the manufacturing phase.

In this paper we want to present the experimental results of the application of double patterning to the definition of a 45nm technology node Flash memory device, reaching a k1 ~ 0.20 using 193nm dry lithography. Flash memory design introduces imaging critical points in several levels: active, contacts, and first metallization. For each of these layers, a dedicated study of double exposure has been performed in order to develop a combined litho-etch process to pattern the requested features density. Different issues will be reported, related to process choices (hard mask, resist compatibility), overlay performances, OPC and layout decomposition. Experimental process windows of dedicated test masks with lines and spaces and contact holes are shown. A deep study on overlay performance and possible optimizations has been performed and will be reported.

Finally, we will demonstrate that double exposure technique can be used to anticipate process integration of critical lithography steps for high density memory devices at 45nm technology node.

6520-94, Poster Session

Extending DUV lithography to 10-nm resolution with the combination of photoresist quantum state control and stimulated emission depletion imaging techniques

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It has been assumed that 193nm immersion lithography is incapable of being extended below the 32 nm process node. Here it is suggested that by using a combination of Vibrational quantum state control, Stimulated Emission Depletion (STED) imaging, and multiple micro-stepped exposures, without development between exposures, DUV lithography may be extended to print features smaller than 10nm with a 1:1 pitch. This is the first suggestion for the merger two the previously independent recent photochemical developments; the use of short laser pulses to control the reaction trajectory of photochemical reactions and STED microscopy image resolution enhancement techniques previously only used for deep sub-wavelength imaging in fluorescent microscopy. Quantum state control uses picosecond duration optical pulses to modulate a photochemical pathway while a photochemical intermediate is still in the initial vibrational excited state. STED techniques overlay two images of the same feature, but at different wavelengths and different phase distributions in the focal spot of the beam. One image is a diffraction limited Gaussian, while the second image is phase modulated in the Fourier plane to produce an annular or railroad track shaped image at a longer wavelength that stimulates excited states in the surround region of the annulus back to the ground state vibrational manifold. The result of this exposure process is to narrow the width of the latent photoresist image. The more intense the surround excitation, the narrower the latent image feature. The combination of these processes combined with micro-stepping between exposures enables the printing of dense features after post-exposure back. We will present photoresist and exposure system design requirements in order to accomplish the merger of these technologies. Beyond the fact that 193nm quantum state controlled STED DUV lithography may be used for the 32nm, 22nm, 16nm, 12nm and 8 nm process nodes, this approach should provides a number of additional benefits including:

1. Double, triple and quadruple micro-stepped exposures without resist development between steps, providing a minimal impact on wafer throughput compared to other multiple exposure techniques.

2. The mask features are not required to be reduced in size as the printed features shrink, therefore today's photomask technology and reticle feature size need not to be changed as printed features shrink, saving tremendous photomask and mask patterning equipment development costs.

3. Scanners based on this technology could be built in 3-5 years from today.

6520-95, Poster Session

Double exposure using 193-nm negative tone photoresist

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Double exposure techniques are one of the promising methods for extending lithographic patterning into the low k1 regime [1]. For frequency-doubling using double exposure methods (Fig. 1), the generation of narrow trenches as a first exposure step is thought to be simplest [2]. Conventional

implementation of this approach uses a positive resist in combination with a dark field mask, and suffers from a small process window as shown in Fig. 2 [3].

In this paper, we demonstrate effective k1=0.25 patterning with improved process window. A negative resist (TOK N023) in combination with a bright field mask was used to give a larger process window in generating a double exposure compared to a positive resist and a dark-field mask combination. The final dense line/space pattern is generated using consecutive half-pitch shifted 3:1 line/space exposures.

We will discuss several aspects of this process. First, the advantage of using a negative resist over a positive resist is shown via a series of simulations. Second, empirical results for generating narrow trenches are presented, including Bossung curve, exposure latitude vs. depth of focus, and line-edge roughness analysis results. Finally, we will report on the etch transfer of frequency-doubled patterns through a silicon-nitride hard mask. In summary, the realization of a double exposure scheme using a negative tone resist to give a large process window is demonstrated.

6520-96, Poster Session

The feasible study of splitting pitch technology on 45-nm contact patterning with 0.93 NA

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As semiconductor process technology moves to smaller generation (65nm and beyond), the contact pattern printing becomes the most difficult challenge on lithography field. The reason comes from smaller feature size and pitch on contact/via pattern printing that is similar to 2D (2 dimension) patterning. For contact and via patterns, they need better image contrast than line/space patterns on pattern printing. Hence, contact/via printing needs higher k1 value than others.

In 65nm generation experience, the k1 is ~0.44 on 0.85 NA exposure tool. Larger NA exposure tool is expensive and developed slower than the motivation of generation. Hence, the process is difficult to achieve by obtaining lager NA exposure tool. The k1 request of 45nm (logic) contact pattering (CD: 70nm / pitch: 140nm) is ~0.34 on 0.93 NA exposure tool that is available currently. RET (resolution enhancement technology) is necessary to be achieve the difficult process goal. Splitting pitch technology is a RET approach to solving 45nm contact pattering.

In this paper, we use 2P1E (2 photo exposure and 1 etching) approach to meet our process requirements. The original layout is split to dense pitch patterns and semi-iso to iso patterns parts by software. Utilizing strong OAI (off-axis-illumination) on dense pattern part and weak OAI on semi-iso to iso pattern part can obtain better process results.

6520-98, Poster Session

A study of process window capabilities for two-dimensional structures under double exposure condition

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As the semiconductor fabrication groundrule has moved toward the 32 nm node, the industry has reached consensus that among the three candidate approaches, the double exposure with 1.35 NA immersion, the high refractive index immersion, and the extremely ultra violet (EUV) lithography, the easiest approach seems to be the double exposure method at an effective numerical aperture (NA) of 1.35. However, there are still a lot of challenges in the design and optimization of the process, such as, the choice of appropriate illumination condition, the choice of a good photoresist, and the design of an optical proximity correction (OPC) strategy for both the singly and doubly exposed patterns. Besides these considerations, there is still the question as whether we really need the double etch process. In this paper, we will focus on the finding a suitable methodology in the printing of two-dimensional (2D) structures under the double exposure and single development scheme since it is the easiest and there is virtually no overlay concern. The double exposure will also mitigate the coherence requirement. Since in the single exposure scheme, the process window for the dense features will prefer large partial coherence while the isolated features need the opposite, in the double exposure scheme, the dense process window can be produced with mild partial coherence. In the study, we have used a 248 nm exposure tool and a well chosen photoresist to study the photo performance parameters in the merge of two photo exposures. At a numerical aperture (NA) around 0.7, the minimum groundrule we can achieve is similar to the one for a 75 nm logic like process with minimum pitch around 220 nm. In the experiment, the single exposure structures are limited to pitches wider than 440 nm. Although the 440 nm pitch is not difficult, the critical dimension of 110 nm is quite challenging, which can cause large line end shortening and other 2D exposure defects. In this paper, we will first present a study on several of 2D structures, such as, the opposing line and space ends, the T like line end structures, the corner rounding structures, etc and the limit on the critical dimension (CD) these structures have that can be completed with one exposure with enough process window, i.e., exposure latitude (EL), depth of focus (DOF), and mask error factor (MEF). Besides, we will also demonstrate our study on the feasibility of double exposure for typical 2D structures especially when their external separation reaches the limit of the capability of the single exposure. In addition, we will compare the experimental data with simulation results and will provide our recommendations on the quality of the photoresists.

6520-99, Poster Session

New double exposure technique without alternating phase-shift mask

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Nano-processing technology has accelerated as the technology node has advanced. Three major technologies have been developed in the field of photolithography, exposure wavelength shortening, high numerical aperture (NA) and resolution enhancement technique (RET). For 45-nm logic device fabrication, ArF immersion systems which have over 1.0 NA, will be used certainly. In addition, double exposure technique using alternating phase shift mask (Alt-PSM) will be adopted for gate layer of high performance logic devices. This double exposure technique had been used from 180-nm high-end logic device production. First exposure is used as trim mask which contains gate electrode and wire. And the part which required severe line width control such as gate electrode is exposed by Alt-PSM as second exposure. In this method, it has advantage that fine resist profile is obtained on wafer with extensive process margin. However, this double exposure technique is very expensive because of alt-PSM cost. Its fabrication process is complicated and it requires very long process. In addition, it has the restriction of alt-PSM 3-D structure, eaves under Cr, considering wave-guide-effect. And it means that alt-PSM nano-processing becomes more difficult.

This time, the authors have developed new double exposure technique without alt-PSM. The first mask is exposed in the same way of normal double exposure technique and second mask is used Cr mask or attenuated phase shift mask (Att-PSM) not using Alt-PSM. Dipole illumination is adopted at second exposure. It is expected that high quality image is gained with dipole illumination without Alt-PSM. It is thought that this new double exposure method is effective for random logic which has various pitch patterns by the optimization of illumination condition and pattern placement.

In this paper, the authors will discuss the following three topics;

1. Basic Concept of New Double Exposure Technique
2. Process Margin
3. DFM Proposal

From simulation and experimental results, it is found that new double exposure technique is possible to make exposure ability equal to or higher than normal double exposure technique using Alt-PSM. In addition, it will be able to form fine patterns with low mask cost using DFM technique, that severe controlled pattern is placed at uni-axis.

6520-100, Poster Session

ILT and double exposure: materials, mask-making and mask-to-mask alignment considerations

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Multiple path exists to provide lithography solutions pursuant to Moore's Law for next 3-5 generations of technology, yet each of those path inevitably leads to solutions eventually requiring patterning at k1<0.30 and below. It was shown [1] that dual patterning allows one to reach patterning with effective k1 as low as 0.16.

Work to be presented is focused on analyzing the use of various dual patterning techniques enabled by the use of hypothetic materials with properties that allow for the violation of the linear superposition of intensities from the two exposures. Use and possible optimization of contrast enhancement layers (CEL) and two-photon absorption resists in conjunction with ILT is considered in some details. CEL is a photobleachable material coated on top of the resist that was actively explored in the 1980s to increase the useful resolution capability of scanners for single exposure lithography [2]. Double exposure lithography using CEL is feasible if the material has reversible bleaching property. Double patterning typically requires printing 3:1 grating which have very poor aerial image. A possible use of CEL for improving the aerial image contrast for the above case will be explored in more detail. The other material under consideration is two-photon absorption resist which responds to the square of the intensity. They have also been shown to double the resolution capability of optical projection lithography [3].

In this article, we will discuss mutual material/ILT/design-rule constraints for the above media and their sensitivity to alignment and mask making errors. Work intent is to identify key relationship between the considered out-of-sight out-of-mind materials, constraints they put on mask design, and possible design rules, such that the composite latent image in the resist (prior to the final development), closely follows the design intent. Given our focus on uncovering key relations between parameters of interest, important but mathematically cumbersome thick mask and partial coherence effects are not considered, which we hope have little impact on our conclusions.

[1] Double line shrink lithography at k1 = 0.16, C. Noelscher, M. Heller, B. Habets, M. Markert, U. Scheler, and P. Moll, Microelectronic Engineering, vol 83, 730-733, 2006.

[2] Comparison of Proximity Effects in Contrast Enhancement Layer and Bilayer Resist Process. E. Ong, B. Singh, R. Ferguson, and A. Neureuther, Journal of Vacuum Science and Technology B, vol. 5, 443-448, 1987.

[3] Optical Projection Lithography at Half the Rayleigh Resolution Limit by Two-Photon Exposure, E. Yablonovitch and R. Vrijen, Optical Engineering, vol. 32, 334-338, 1999.

6520-101, Poster Session

Development and characterization of a 300-mm dual-side alignment stepper

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A number of new packaging technologies are driving the demand for high performance dual side alignment on 300mm lithography systems. Advanced system in package (SiP) techniques will require through silicon vias to allow very high density vertical interchip wiring of multiple device stacks. These through silicon vias need to be freely placed in the devices which creates a requirement for tight registration of the front to back side alignment. In the MEMS area, wafer level packaging is being used for applications where the device must interact with the outside environment without restrictions from the packaging. An example is image sensor chips where the active area of the device is on the topside and the electrical interconnects are on the backside. This application requires dual side alignment on a bonded silicon glass sandwich structure.

To support these packaging applications a new lithography stepper capable of dual side alignment on 300mm wafers has been developed. This stepper employs an innovative and flexible system for front to back side alignment to support a wide range of packaging applications. This paper discusses the design and integration of the alignment system on a broad band, low numerical aperture stepper. Experimental target capture for both SiP and CMOS image sensor applications is shown. Dual side overlay performance data on multiple wafers and lots is reviewed.

6520-102, Poster Session

Characterization of absorptance losses and wavefront deformation in DUV optics

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In order to improve the efficiency of optical components for DUV microlithography, metrology tools for comprehensive characterization of absorptance in coated and uncoated fused silica and calcium fluoride at 193nm were developed. Absolute absorption data are determined by high-resolution laser calorimetry, providing strongly enhanced accuracy as compared to transmissive measurements. The technique allows evaluation of both single- and two-photon absorption coefficients by monitoring the fluence dependence of the losses. It also accomplishes fast monitoring of degradation phenomena, e.g. laser-induced color center formation. Moreover, a separation of surface and bulk absorptance can be achieved by using samples of different thickness. A strong influence of the polishing grade on the surface absorptance was observed. In case of thin samples (d < 6mm) the surface contribution clearly dominates the overall absorption losses, even at optimum surface finish. The results are discussed in terms of a simple model for the absorption mechanisms in wide band-gap materials based on their electronic band structure.

For an assessment of the optical quality of DUV optics, a high-sensitivity wavefront analyzer system based on the Hartmann-Shack principle is employed. The device accomplishes precise on-line monitoring of wavefront deformations of a collimated test beam transmitted through the laser-irradiated site of a sample. Due to the achieved sub-nm resolution, it can be used as an alternative to interferometric measurements for ´at wavelength´ testing of optics, e.g. for on-line registration of compaction or thermal lensing effects in fused silica.

6520-103, Poster Session

Flare effect of different shape of illumination apertures in 193-nm optical lithography system

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Flare has been important variable to achieve good CD control in the resolution limited lithography area such as sub-90 nm node. Early works on flare have focused on long-range DC and local flare, with an attention on how to measure flare and how flare impact on CD control within theoretical model for ideal situation. As pattern size decreases below 100 nm, however, short-range flare has become more important because short-range effects begin to appear prominently beyond that technology node. It was also pointed out that process conditions such as photo resist thickness, substrate film stacks, and even some times photo masks can be important variables for short-range flare, too. Recently, the impacts of process variables on flare have been studied both on the conditions at wafer level and at the illumination level. In particular, we have shown in our previous paper that the illumination conditions such as coherence factor and illumination aperture shapes also give impact on short-range flare. [Y.-J. Yun, et al., Optical Microlithography XIX, Proc. of SPIE Vol. 6154, 615435 (2006).] We have found that the amount of short-range flare depends on the outer radius of the illumination aperture but not on the inner radius of annular illumination apertures. The short-range flare, the additional portion of the diffraction image to the ideal one, increases as the source size increases but it has not been clarified why the inner radius of the annular illumination apertures does not affect the amount of the short-range flare.

In this presentation, we will prove detailed relation between illumination aperture shapes and the short range flare by exploring its impact with number of off-axis illumination apertures including multi-pole illumination apertures, in addition to our previous data on partially coherent conventional and simple annular illumination apertures. We utilize the 193-nm scan-and-step exposure tool and evaluate the short-range flare

by measuring CD on the 100 nm line surrounded by clear window having various open ratios. The extended data on various off-axis illumination apertures will clarify the impact of illumination aperture shape on the short-range flare. In conclusion, we will suggest how the process error due to the short-range flare can be minimized in the sub-90 nm or beyond technology node. We also present how much the increasing flare raises CD fluctuation and reduces overlapping process window in real process quantitatively.

6520-104, Poster Session

Silicon verification of flare model and application to real chip for long-range proximity correction

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Optical proximity correction (OPC) plays a vital role in the lithography process for critical dimension (CD) control. With the shrinking of the design rule, CD becomes more sensitive to lithography process. As a result, the task for OPC becomes more challenging.

Flare, or stray light, is an added incoherent background intensity that will detract from lithography system performance, CD control and process latitude. The impact of flare on lithographic imaging and its correction through OPC has been the subject of increased investigation.

In this paper, point spread function (PSF) of flare is got based on the real lithography system performance and the flare value across the full chip is obtained through flare model which considering the pattern density through the chip. By collecting wafer silicon data with CD SEM, flare model is verified and the flare impacts on the across chip line width variation (ACLV) are showed. With the existence of flare, CD difference between different areas of the cell could be found because of local pattern densities variation. As CD varies by a comparatively wider range than optical proximity range, it could not be corrected by existing OPC model. In the paper, applications for long range proximity correction to real chip are discussed in detail.

6520-105, Poster Session

Thermal aberration control for low-k1 lithography

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Low k1 lithography such as RET (Resolution Enhancement Technology) with off-axis illumination and PSM (Phase Shift Mask) has been applied for more than the decade to catch up with the trend of Moore's law. Aberration level of the projection lens has been drastically improved for these years because high lens performance is the key for realization of low-k1 lithography. At least, lens performance at idling condition is now unbelievably small.

However, this is not the case for actual projection lens under use. Once the tool stated to use in the product line, considerable amount of exposure light supplied to the lens and the aberration started to be changed until saturated condition, which is called thermal aberration. It may not be issue, if the aberration change is negligible for the imaging performance of the patterns. But the current situation of microlithography below can not allow us to ignore the aberration changes.

- Exposure energy per unit time is being increased to maximize productivity

- Off axis illumination condition such as dipole illumination or PSM with very small sigma condition concentrate power of light to small region on the pupil

- Allowable aberration level is still being reduced due to non-enough process window for leading edge technology node

Through we have lens aberration controller by lens elements positioning, controllable aberrations are only low order components and not enough for full compensation of the thermal aberrations.

We have developed methodology to overcome this issue. One scheme is process dedicated aberration control by the conventional aberration controller. Conventional aberration controller adjusting low order aberrations due to exposure and leaves the large amount of higher order aberrations. Contrary, a new scheme balances the low order and high order aberrations to minimize impact to the target pattern.

The other technique is aberration control system using infra-red irradiations. This system can compensate uniform astigmatism, which is generated by asymmetric setting of illumination light sources like dipole illuminations.

Theses two techniques allow us to increase the productivity without pattern imaging performance degradation due to the thermal aberrations. These schemes are rather necessary system for the current and next generation very low k1 lithography with very high throughput.

6520-106, Poster Session

Quasi-telecentricity: the effects of unbalanced multipole illumination

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Telecentricity has long been recognized as an important property of lithography-tool optics. "Shift" telecentricity error, an angular misalignment of the illuminator and projection lens, manifests itself as an unwanted translation of the aerial image through focus. At best focus, no effect is visible. Generally, acceptance tests measure directly the translation through focus, although it is also possible, using pupil-imaging techniques, to observe the error directly, by measuring offset of the pupil fill with respect to the projection lens NA. Even with a perfectly aligned system (i.e. a perfectly centered pupil fill), it is still possible to induce a translation through focus. This arises especially in multipole pupil fill patterns (dipole, quadrupole, etc.) which have one pole brighter than the others. We refer to this effect as "quasi-telecentricity." With the tight pitches and extreme polar illumination patterns coming into increasing use, this effect will become more important in the next few years. We have calculated the size of the effect and placed limits on the illumination patterns that can be used for this type of printing.

6520-107, Poster Session

Novel high-throughput micro-optical beam shapers reduce the complexity of macro-optics in hyper-NA illumination systems

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Uniform illumination of the mask is a key factor for the lithography process. The requirements of Immersion Lithography make illumination systems even more complex e.g. by adding additional parameters like polarization and improved throughput. Arrays of refractive microoptics are the ideal solution for high transmission homogenising elements since several tool generations. These arrays can provide very steep intensity profiles (top hat and other profiles), enable lossless polarization control and do not suffer from zero order losses like diffractive elements.

Usually refractive microlens arrays are used with macrooptical field lenses in order to illuminate a field very uniformly or with a customized intensity distribution. High numerical apertures create the necessity for aspherical surfaces which leads to significantly higher lens cost especially for the macrooptics. In this paper we present novel microoptical homogenizers which create extremely uniform intensity distributions for high numerical apertures without any field lens or at least only with spherical field lenses. Especially multi-pole off-axis illumination can be improved with less optical components. An important prerequisite for these special types of homogenizers is that LIMO can produce free form surfaces on monolithic arrays larger than 200 mm with high precision and reproducibility. Every lens can be design individually and can also be shaped asymmetrically.

We will present surface test methods and the final UV tests, guaranteeing the performance for the applications. Example data gained with these tests will be shown with regard to: meeting the design parameters, reproducibility over one wafer and reproducibility in large lots.

Monolithic elements based on crossed cylindrical lenses provide a fill factor close to 100%. Simulations and measurements prove that microoptic arrays can be produced which provide a uniformity of the homogenized laser light of significantly better than 1% P-V at numerical apertures above 0.35.

Refractive microoptic arrays do not change the polarization state of the transmitted light which is an important prerequisite in immersion exposure tools. LIMO homogenizer sets are manufactured from fused silica and Calcium fluoride thus they are suitable for all DUV wavelengths at highest laser fluxes.

6520-108, Poster Session

Advanced polarizer for 193-nm immersion lithography

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State-of-the art advanced 193 nm lithography solutions - both dry and immersion- are based on the use of polarized light. Because every optical element in the beam path does influence the polarization status it is important to manipulate the incoming laser light in a manner guaranteeing stable polarization properties. We have developed a simple thin film polarizer which shows more than 97% transmission of p-polarized light at polarization aspect ratios in excess of 1:100. At the same time, insertion losses for s-polarized light are less than 2 %. Even higher polarization ratios (up to 1:300) with slightly reduced transmission of p-polarized light can be reached with changed layer design. The polarizers as developed are completely stable against 193 nm laser fluencies of several tens of mJ/cm2. The thin film polarizers were also used to qualify laser based measurement equipment for measurement of extinction ratios up to 1:10000 at 193 nm.

6520-109, Poster Session

A solid state 193-nm laser with high-spatial coherence for sub-30-nm interferometric immersion lithography

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Immersion lithography using available 193 nm optics and laser sources provides an attractive near-term path to reducing the printable feature sizes of integrated circuits by using a high-index fluid to reduce the wavelength at the wafer, rather than using light with higher photon energy and shorter vacuum wavelength. This approach requires the development and characterization of high-performance fluids, photoresists, overlayers, and high-index optics. Interferometric immersion lithography (IIL) allows for rapid testing of these components now, before the general availability of full-blown immersion lithographic tools.

A critical component in an IIL engineering test-stand is a suitable 193 nm light source. In contrast to the excimer laser sources used in standard lithographic exposure tools, which by design have low spatial and temporal coherence to minimize interference artifacts, IIL requires both very high spatial- and temporal-coherence to allow uniform high-contrast intensity fringes to illuminate a wafer surface over relatively large areas (~ several mm2 per exposure site). In addition, the laser should have high power stability and be sufficiently robust to allow extended periods of operation with little maintenance or operator intervention.

We have developed an all solid-state laser operating at 193 nm that satisfies these requirements for incorporation in a high performance IIL test-bed. The source emits ~10 ns long pulses at 5 kHz, producing an average output power in excess of 15 mW with low pulse-to-pulse fluctuations. The beam has a fundamental Gaussian profile and a bandwidth of ~3 cm-1, giving a coherence length of ~3mm. The system consists of an intracavity-doubled, q-switched Nd:YAG laser that provides ~13 W of 532 nm light. The green light is split into two beams, one of which is doubled to 266 nm, while the other is used to pump an OPO tuned by crystal temperature and narrowed by a Bragg-grating output coupler to emit 710.4 nm light. The red and 266 nm beams are mixed in a final BBO crystal to produce 193 nm sum-frequency light. Particular care was taken with the choices of materials, cleaning procedures and packaging to protect the optics and crystals from the damage that can easily occur with the intense, relatively small diameter beams that are used in the system. Mechanical stability is also a primary concern, and the system incorporates features designed to ensure stability and give “no-tweak” operation.

6520-110, Poster Session

New investigations regarding the prevention of depolarization of ArF excimer laser irradiation by CaF2 laser optics

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Crystalline calcium fluoride is one of the key materials for 193nm lithography and is used for laser optics, beam delivery system optics and stepper/scanner illumination optics. In comparison to fused silica it shows a much higher laser durability. However, even in pure calcium fluoride the irradiation by ArF excimer laser (193nm) can cause transmission loss and depolarization. Short time and long time tests of radiation induced changes of optical properties of CaF2 were carried out. Within short time tests initial and radiation induced absorption as well as the measurement of laser induced fluorescence and the measurement of laser induced depolarization are adequate methods for characterization of the material under ArF laser irradiation. Previous investigations were done by Burnett to prevent depolarization caused by spatial dispersion. Nevertheless an important challenge is the prevention of depolarization of the polarized laser beam by CaF2 laser optics caused by a temperature gradient. The dependence of depolarization on the direction of temperature gradient in comparison to the direction of the laser beam and the orientation of the CaF2 crystal was investigated. In the present work different paths to prevent or mitigate the depolarization by CaF2 due to a temperature gradient are discussed resulting in a special chance to mitigate depolarization by a laser window.

6520-111, Poster Session

Reliable high-power injection locked 6kHz 60W laser for ArF immersion lithography

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Reliable high power 193nm ArF light source is desired for the successive growth of ArF -immersion technology for 45nm node generation.

In 2006, Gigaphoton released GT60A, high power injection locked 6kHz 60W laser system, to meet the demands of semiconductor markets.

In this paper, we will report high durability performance and key technologies for reliable mass production GT60A laser system.

6520-112, Poster Session

Increased availability of lithography light sources using advanced gas management

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Increasing throughput demands on leading edge scanners are requiring greatly improved light source availability. This translates directly to minimizing downtime and maximizing productive time, as defined in the SEMI E10 standard. Focused efforts to achieve these goals are ongoing and have already yielded significant improvements on production light sources.

One positive contributor to improving productive time is the minimization of the light source stoppage for Halogen gas replenishment. Cymer XLA and 7000 series lasers employ one or more Halogen gas filled chambers as the gain medium. As the light source operates, the Halogen gas is depleted and contaminants accumulate, so the gas must be periodically replenished.

This can be a partial replenishment while the light source continues to operate, called an inject, that is subject to constraints to ensure the light properties remain within specifications. Alternatively, it may be a full replenishment, called a refill, where all of the chamber gas is replaced while the laser is not firing. Refills are to be minimized because of the large disruption they introduce to both the light source and scanner operation.

This paper describes availability improvements of Cymer XLA and 7000 series light sources by using advanced gas management schemes to minimize gas replenishment impact to productive time.

Tighter process control requirements and a deeper understanding of light source dynamics have led to the development of higher performance Halogen gas control algorithms which have enabled longer light source operation before the system requires a refill, and have simultaneously improved the light properties.

Using a variety of derived signals and novel algorithms we are now able to predict the end of a gas life and dynamically determine when a refill will be required. Based upon a lithography user's pulse utilization patterns this may enable longer gas lifetime between refills, rather than relying on a simple and conservative refill schedule. Recent experiments have demonstrated significantly longer gas lives using the gas lifetime predictor coupled with the standard gas control algorithm.

Recent augmented gas control algorithms have demonstrated multiple times extension of gas life through advanced gas replenishment methods and higher performance estimators. Coupling the latest gas algorithm developments with the gas lifetime predictor will provide the next quantum step forward in the evolution of gas management.

Along with these improvements to gas management, major efforts in light source fault reduction, module lifetime extension and optimization of module replacement, will provide significantly increased combined light source\scanner availability.

6520-113, Poster Session

Designing a metrology wafer for the immersion lithography exposure

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Immersion lithography takes advantage of a small water volume between the resist and the lens in order to reduce NA shift distortions. However, the evaporative cooling of the water causes significant shifts in local temperatures, which can result in overlay errors. This overlay shift is correctable if it can be predicted by a measurement system. Prior wafer based measurement systems focused primarily on PEB tool architectures, placing sensitive receivers on the top surface of a wafer, and broduced highly accurate representations of the process environment. The challenge of implementing these systems in immersion exposure tools is threefold - water seal quality, planarity, and additional height. To address these challenges, a thin, planar architecture is used. The electronics and sensors are embedded in a milled out substrate rather than affixed to the surface. Then, a thin top cover seals the system. Highly accurate calibration techniques add the sensitivity required to detect fine differences of thermal response to the immersion exposure process.

6520-114, Poster Session

A study of overlay mark robustness and enhanced alignment techniques for alignment improvement on metal layers of sub-100-nm technology

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At the cutting-edge lithographic node, overlay budgets are expected to tighten (Refer to Table 1 for ITRS overlay requirements). In order to maintain tighter overlay specifications, the conventional method of correcting linear alignment errors, through feedback of scanner correctables from overlay metrology data of product wafers, need to be enhanced. There are 3 contributors to linear alignment errors. These 3 factors are tool-induced-shift (TIS), wafer-induced-shift (WIS) and the interaction between tool and process. It is therefore necessary to improve alignment accuracy from both the process and the tool aspects.

Aberrations in the optics of the alignment scope, poor uniformity of scope illumination and telecentricity are contributors of TIS (Refer to Figure 1). They result in position shift, which in turn translates to wafer scaling signature. Change in alignment mark topography during actual wafer processing causes WIS. Metal deposition and chemical mechanical polishing (CMP) are major contributors of WIS. CMP, which is the process to planarize metal and define metal layer thickness, induces dishing and erosion of alignment marks. These damages occur due to material property differences between dielectrics and metal, under mechanical and chemical stresses (Refer to Figure 2 for illustrations of dishing and erosion). Sputtering which is a technique for metal deposition also results in film thickness variations. The sputtering process involves bombardment of a target (the coating material) by energetic ions. This bombardment ejects atoms of the target material, which then float and condense on the substrate. The angle at which the atoms strike the substrate can cause asymmetrical deposition within the topography (Refer to Figure 3 for a schematic of sputtering). Such noises introduced by these processes indicate strong wafer level rotation and scale signatures.

This paper introduces methods for improvement of alignment performance at CMP layers. A study on mark reflectivity was done. A number of various alignment mark designs were evaluated. The most robust mark to CMP process will be illustrated. The concept of the 'Alignment Parameter Optimizer', which is a function of Enhanced Advanced Global Alignment (EAGA), to select the best alignment illumination mode for each mark and the best sample shots for alignment within the wafer, taking throughput into consideration, will be discussed. A New Alignment Algorithm that is able to compensate for asymmetric alignment marks will also be presented in this paper. Finally, alignment data from a mass-production fab, with the implementation of the above-mentioned concepts will be illustrated.

6520-115, Poster Session

The optimization of zero-spaced microlens for 2.2 μm and 1.7 μm

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In CMOS image sensor, microlens arrays are generally used as light propagation carrier onto Photo diode to increase collection efficiency and reduce optical cross-talk. Today, the trend of CMOS technology is to reduce the pixel size for increase the integration density and improvement the resolution.

Microlens is typically formed by photo resist patterning and thermal reflowing, and the space between photo resist is necessary to avoid the microlenses merging during thermal reflow process. As a shrink of microlenses sizes, microlens becomes more and more difficult to manufacture without merging microlenses. However, the key of light loss free microlens fabrication is still zero-space between microlenses.

In this paper, we report the selection of the optimum shape of microlens by the dead space and the curvature and the improvements of critical dimension and thickness uniformities. Also the results of the application of zero-spaced spherical microlens in 2.2um and 1.7um pixel CMOS image sensor device are reported comparing with classical shape microlens.

6520-197, Poster Session

Laser durability studies of high-index immersion fluids: fluid degradation and optics contamination effects

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An extension of water-based immersion lithography involves replacing water with a higher index transparent oil. It has been found previously

for water-based immersion studies that ppm-levels of organic contaminants in water can lead to optics contamination.1 Understandably, potential lens contamination is a major concern for an all-organic immersion fluid. We have constructed an experimental system for controlled irradiation of high index fluids, including capabilities for in-situ cleaning of potential deposits. Our in-situ metrology includes laser-based transmission, spectrophotometry and spectroscopic ellipsometry. We present results of laser-irradiation of several high index immersion fluid candidates. Using properly developed exposure metrics, we discuss implications for fluid lifetimes in an immersion system, with and without recirculation. Using our in-situ metrology, we are able to decouple bulk fluid degradation from window photocontamination for several fluids. We find a significant variation in optics contamination rate depending on the fluid tested (see Figure 1). Even the slowest observed contamination rates would require some remediation strategies to remove the built-up deposit from the final element surface. We will present our analysis of window deposits and the results of in-situ cleaning studies aimed at removing such deposits during fluid exposure.

6520-116, Poster Session

Illumination optimization with actual information of exposure tool and resist process

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An advanced exposure tool has become able to control various functions such as lens aberration, illumination shape, wavelength, and so on. Also as process nodes proceed, the k1 factor is being decreased. Under such circumstance it is crucial to set the exposure tool functions adequately. Since it is almost impossible to do it manually, a solution tool for optimizing exposure tool function is in demand. As conventional optimization ways of illumination there have been a grid pixel-based one, a parametric one, and an arch bounded pixel based one. The common disadvantage is that they output a solution within their defined group and the solution does not necessarily correspond to the actual illumination shape of exposure tool. There occurs several nm deviation of OPE between an illumination shape derived by conventional ways and an actual one. To overcome this problem we have developed a new method. In this method all illumination shapes that a scanner provides are stored in a database, and the function expressing them is formed, and with the function a best illumination is searched. As a result the exact illumination solution that a scanner provides can be found.

We also combined the optimization of illumination and aberration. Aberration is controlled in the same way as a lens aberration controlling system build in a scanner. Besides a laser spectral of E95 is used to match a printed pattern to a target pattern. Though the impact of E95 on optical imaging depends on the lens design, this system includes it and simulates accurately. So we can optimize the scanner functions as if we control the actual scanner, which leads to more accurate optimization solution.

Regarding the simulation during optimization we evaluated whether an optical simulation is enough or a resist simulation is necessary on several cases. As a resist simulation we adopted a variable threshold resist model. A resist model is usually created under an exposure condition, but exposure conditions must be varied during optimization. So we evaluated how much different exposure conditions a resist model created under an exposure condition is effective to.

We evaluated the impact of OPC used during iteration of optimization on the result. This includes selection of optical or resist model. It was found that OPC specification and the resist model should be carefully chosen according to the optimization target.

Finally we show several effective examples of optimization by our new method.

6520-117, Poster Session

Impact of illumination performance on hyper-NA imaging for 45-nm node

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In the 45nm mass production age through a hyper-NA immersion tool, we are facing the challenges of shrinking geometries with the strict control of OPC. In particular, increasing importance is placed on the illuminator performance, and the polarized illumination has become an indispensable technology. Keys to the improved imaging are both the optimization of polarization states and the precise control of light source shapes. It is essential to define the light source shapes numerically with high precision, and to measure and control it directly on the tool.

This paper reports the optimization procedure of the polarization parameters, and the practical method to find the appropriate effective light source parameters for OPC matching. Furthermore, we introduce the actual results from our newly developed \>NA 1.30 immersion tool, FPA-7000AS7.

The first part of this paper describes the polarization parameters for optimization. It is well known that the larger the NA of the projection optics, the more prominent the optical contrast difference between the two polarization images. In order to attain the high contrast and resolution, the ratio of S-polarized light needs to be increased.

We investigated image degradation caused by the birefringence of the projection optics under various illumination conditions, and found the phase difference between P- and S-polarized lights of an illuminator affects the imaging performance. For instance, the phase difference results in a maximum 6% change of the total Ratio of Polarization (RoP) when a projection optics has 8nm retardation. We need to take the polarization phase effects into consideration as well as RoP for illuminators in the hyper-NA immersion lithography.

The second part discusses the optimization technology of the effective light source, identifying the significant parameters of effective light source in the OPC matching process. OPC matching by adjusting effective light sources is quite popular today. The conventional method is to perform OPE calculations for various shapes of effective light sources and to choose the result closest to the desired IC patterns with a large process window.

We have established a new method for OPC matching that does not require these complex calculations. This handy method uses newly defined parameters calculated directly from the effective light source shape. The parameters are also in accordance with OPE, and achieve high accuracy.

The third part of the paper is the actual data of the topics aforementioned with the discussion of metrology. FPA-7000AS7 has functions to measure polarization and effective light source shape with its on-board measurement systems.

We also report the optimization results with the in-situ adjustment system of polarization and effective light source. Additionally, we will discuss the accelerated miniaturization and the improvement of OPC matching required on a hyper-NA immersion tool.

6520-118, Poster Session

Visualizing the impact of the illumination distribution upon imaging, and applying the insights gained

S. D. Slonaker, Nikon Precision Inc.

A method has been developed for mapping and analyzing the impact of each local region of the illumination distribution (i.e. “illumination source point”). The method makes directly visible the imaging impact/result for each one of those local regions. In this way, the entire available illumination region can then be broken down generally into regions of “good light” and “bad light” for each pattern under consideration. It is possible to then further subdivide the impact of each source point/local region into ‘categories of impact’ that can be each then independently evaluated (e.g. contrast/intensity modulation, Normalized Image Log Slope, CD range through a fixed focus region, CD change due to a given dose change, aberration sensitivity, etc.).

By applying the method and analyzing the full superset of all available source points for all mask patterns being considered, the optimization of the illumination distribution becomes a straightforward matter of finding the best combination of source points to deliver whatever is described as the target of the optimization.

An example of the application of the method will be provided and discussed, with highlights on key learning steps arising from this case study that might be applicable more generally. One example of the 'visualization' of the imaging impact as a function of illuminator source position is shown below.

Figure 1:

Map of aerial image intensity (shown as countrous) as a function of position within illumination distribution, This example from the case of Lens NA=1.04 and a pattern pitch of 120 nm.

6520-120, Poster Session

Optimal solutions for the illuminator and final lens pupil coupled distributions beyond the axial symmetry

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Since last decade many efforts in optical lithography are devoted to the improvement of various system components both in order to enhance the optical resolution and to decrease the printing error. Most popular Köhler's partially coherent imaging system has the following optical components: the illuminator, the final lens pupil and the reticle itself. The last component is pattern dependent and its optimization is coupled with the proximity correction. First two components are mostly determining the system (machine) performance since they are pattern independent. We have developed the general (i.e. nonparametric) optimization method allowing us to optimize self-consistently the system performance. Main finding was that the self-consistency of the illuminator distribution and the spatially inhomogeneous final lens polarizing pupil is very essential to make synergetic effect at the optimization.

Axially symmetrical solutions allows during one exposure to print with the same quality the objects of any orientation. However, the system performance can be further improved if the printing of specifically oriented objects is only required. The improvement can be achieved by breaking the axial symmetry of the spatial distributions of both the illuminator and the final lens pupil. Instead a definite axial symmetry should only be kept. An important example is the stepper, where printing of the lines of one orientation (in one exposure) is only required. The corresponding spatial distributions should be even (respectively the orientation) in this case. Another example is the printing of both X and Y oriented lines at once, where both the illuminator and the pupil distributions should be even in both X and Y directions. Finally we have to mention the case of the illuminator with finite number of the mutually incoherent illuminator pixels. Such an illuminator is easier in both manufacture and the optical alignment. The illuminator pixels can be oriented in a grid with breaks the required symmetry. For example, a square pixel grid does not allow to print both XY lines (i.e. the lines with 45 degrees orientation) and X/Y lines at the same quality even when the axial symmetry of the illuminator intensity is used. Thus, the compensating violation of the axial symmetry is required.

In the article we present mathematically best possible combinations of the spatial distributions of the illuminator and the final lens pupil for the cases above. We also compare the cases of polarizing and non-polarizing pupils of the final lens.

6520-122, Poster Session

Sensitivity of hyper-NA immersion lithography to illuminator imperfections

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For hyper-NA immersion scanners, the impact of minor imperfections of the optical system becomes more and more pronounced. This leads to ever higher requirements of optical system design, manufactory and tuning. The imperfection of illuminator intensity profile is one of these factors. In this paper, we present the investigations of the lithography sensitivity to the illuminator imperfections. First, we created a series illuminator shapes with gradual changes in the center-shift, intensity imbalance, geometric ellipticity and intensity ellipticity.. Then we imported these generated illuminators into litho simulation software. Simulations were carried out for 40nm horizontal and vertical dense lines for the case of a 1.35NA immersion scanner. A azimuthal polarized source was assumed and a double-BARC photoresist model was included in the simulations. In the first part, ideal top-hat illuminator shapes were used in the simulation. The resist CD and the pattern shift of H&V line through focus were calculated for Dipole, C-quad and annular illuminations. The results are presented in terms of sensitivity to the illuminator imperfections, e.g. CD/imperfection or shift/focus/imperfection. In the second part, we present an analytic model which can describe more details of the realistic illuminator profiles. With this model, smoothed illuminator profiles can be generated for any defined sigma and illumination shape, and the slope of the profile in both radial and angular directions can also be characterized. Compared to the top-hat illuminators, simulation results of the realistic illuminators demonstrated a significant improvement of lithography performance prediction. This study provides, on one hand, a useful prediction of lithography sensitivity to the illuminator imperfections, and on the other hand, a valuable reference of the specification of scanner illuminations.

6520-123, Poster Session

The calibration of process window model for 55-nm node

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In previous OPC model calibrations, most of the work was focused on how to calibrate a model for the best process conditions. With process tolerance decreasing in coming NGL (Next Generation Lithography), it is increasingly important to be able to predict pattern behavior through process window. Due to a low k1 factor that leads to a smaller process window, the use of process window models is required for both optical proximity correction (OPC) and Lithography Rule Check (LRC) applications to insure silicon success.

In this paper, we examine multiple approaches for the measurement of test patterns to achieve a successfully calibrated process window model. Basically, two sampling methodologies will be employed. At first multiple data sets will be taken with a few amount of measurements. The data sets will span the entire process window with a fine granularity in focus and dose. The second approach will use only very few process conditions and for each condition a large number of data points are measured. The resulting model calibrations will be verified and judged using additional measurement data to demonstrate the quality of the process window models.

6520-124, Poster Session

Contour-based data extraction for model calibration

T. H. Wu, United Microelectronics Corp. (Taiwan)

Scanning Electron Microscope tools enable the visual inspection for the structures printed on silicon wafers in a micro lithographical process. Several software algorithms and tools have been developed to enable the automation of using these images in the RET development flow. In this paper we leverage the capabilities to address some problems in model building and hot spot analysis.

The model calibration process, in the RET flow, is one of the most critical steps towards building an accurate OPC recipe. Accurate models can precisely catch the process lithographical behavior and help RET engineers build the proper recipes to obtain high yield. For years, calibration of OPC models has been based on symmetrical structures only. This limitation is due to the fact that metrology tools usually provide Critical dimension data and not Edge Placement Error data, however model calibration can directly use EPE data for calibration. This is a drawback in the modeling process as in real designs, it is more likely to encounter asymmetrical structures as well as complex 2D structures that can not easily be made symmetrical, especially when we talk about technology nodes for 65nm and beyond,

the models will be either interpolating or extrapolating to calculate the EPE for these structures due to their absence in the calibration test patterns.

Hot spots are places where the structures have high tendency to fail with process variations. Conventionally, to identify these structures, simulations for different process conditions are made. These process window simulations consume a lot of runtime as the simulations are done for a number of combinations of different process conditions. This method is also dependant on process window model capabilities, which is usually not of the highest priority during model build. The accuracy of models in nominal conditions usually comes first.

We present an approach to extract EPE information from test structures' wafer images, and directly use them in the calibration of a 55nm and below poly process. Model accuracy is then compared to the conventional method of calibration using symmetrical data only. The paper also illustrates the ability of the new flow to extract more accurate measurement out of wafer data that are more immune to errors compared to the conventional method. Extracted contours are further manipulated to extract process variability bands based on process window wafer images. These extracted contours are used to identify structures that make hot spots and degrade chip yield.

6520-125, Poster Session

Distributed model calibration using Levenberg-Marquardt algorithm

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For minimizing the prediction error of a multivariate model, the industry standard is Levenberg-Marquardt algorithm. We describe a distributed computing technique that is natural to the algorithm, and easy to implement in a cluster of computers. When the number of parameters increase dramatically as we push forward to the next node of hyper-NA, immersion era of lithography, our technique will achieve nearly constant calibration time, simply by scaling up the computing environment.

6520-126, Poster Session

Analytical approach to high-NA images

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Since 193 nm ArF lithography is the practical wavelength, the high and hyper numerical aperture technologies prolong and start its lithography ending for further improvement of the resolution. Application of polarization illumination leads to the 25 % increase of depth of focus and exposure latitude. Polarization simulation becomes a key technology for its control and application. In this paper, polarization of numerical aperture is modeled into aerial and resist images by using improved scalar and vector models. Those simulated results have a good agreement to experimental available results.

In terms of small half pitch nodes, polarized effects are described into aerial and resist images. Optical proximity correction of polarized effects is performed. The potential to extend its lithography below 20 nm half pitch node is discussed.

6520-127, Poster Session

Modeling and performance metrics for longitudinal chromatic aberrations, focus-drilling, and Z-noise: exploring excimer laser pulse spectra

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The combined impact of longitudinal chromatic aberrations, focus-drilling, and Z-noise on several lithographic performance metrics is described. After review, we investigate an improved method for simulating the lithographic behavior of longitudinal chromatic aberrations stemming from the finite bandwidth of excimer laser pulse-spectra [Kroyan, SPIE v4000, Brunner, SPIE v6154] using PROLITH. Additionally, we explore two methods for modeling the lithographic improvements related to focus-drilling and new functionality for modeling the effects of Z-noise. Our case studies involve re-investigating the RELAX [Lalovic, v5754] process and providing a framework for accurate lithographic simulation using machine specific, pulse-spectral data, modified Lorentzian, and Gaussian models. After presentation and analysis, we discuss potential applications including methods for improving focus budgets and improved mask design.

6520-131, Poster Session

Dr.LiTHO: a development and research lithography simulator

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This paper introduces Dr.LiTHO, a research and development oriented lithography simulation environment developed at Fraunhofer IISB. Lithography simulation has been a field of activity at Fraunhofer for almost twenty years now. Numerous programs, libraries, and models have been developed. With the change of computer science techniques and paradigms, also the structure, and often even the programming language, of these modules has changed drastically over the years. Old FORTRAN programs co-exist with modern object-oriented C++ libraries. The handling of these pieces of software differs significantly. This fact impairs not only the usability of the simulation environment, but also renders combining different programs impossible, or at least extremely difficult.

Designing an integrative and easy-to-use environment is a very complex task, which in general cannot be done by modelers. Although there are so-called middleware approaches available, such as Microsoft's .NET or the open-source solution Eclipse, which support application programmers in integrating existing modules, most of these environments themselves impose a significant complexity on the development process. Furthermore, most of these frameworks are confined to certain computer platforms, complicating portable development (e.g., in order to use high-performance computing facilities). Instead, we propose a light-weight approach to a lithography simulation environment: The use of a scripting (batch) language as an integration platform. Out of the great variety of different scripting languages, Python proved superior in many ways: It exhibits a good-natured learning-curve, it is efficient, available on virtually any platform, and provides sophisticated integration mechanisms for existing programs. Moreover, Python becomes increasingly popular. Organizations like IBM, Nasa, Google, Industrial Light Magic, Yahoo, and many more are now using Python for various tasks. In addition to the beneficial language properties of Python, it autonomously manages library loading and consistent data representation. In this paper, we will describe the steps, required to provide Python bindings for existing programs and to finally generate an integrated simulation environment. In addition, we will give a short introduction into selected software design demands associated with the development of such a framework. We will especially focus on testing and (both technical and user-oriented) documentation issues.

Simulations with Dr.LiTHO have to be pre-defined in text files. These files (scripts) contain not only all parameter settings but also the simulation flow, providing maximum flexibility. In addition to relatively simple batch jobs, repetitive tasks can be pooled in libraries. And as Python is a full-blown programming language, users can add virtually any functionality. In this paper, we will demonstrate that this property is especially useful in the scope of simulation studies or optimization tasks, that often require masses of evaluations. Furthermore, we will give a short overview of the numerous existing Python packages. Especially in the field of numerical computations and visualization, these packages provide a powerful alternative to traditional libraries or programs. Several examples demonstrate the feasibility and productiveness of integrating Python packages into custom Dr.LiTHO scripts.

6520-132, Poster Session

Lithographic characterization of evanescent-wave imaging systems

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Solid immersion lithography has been proposed as a successor to liquid immersion lithography as a single exposure option for the 32 nm node . Current demonstrations have been limited to interferometric imaging. We model the solid immersion lithography process rigorously, including the evanescent wave phenomena, in a commercial lithography simulator. After verifying the experimental cases currently documented, we explore the use of solid immersion lithography for a more general optical projection system. The lithographic process space is explored for conditions such as process window, resist thickness, gap width, and gap material. Vector imaging, followed by full resist kinetics and development, is performed for all calculations. Mask error factor, CD through pitch, and other issues significant to lithography are explored.

6520-133, Poster Session

32-nm OPC design rule evaluation through virtual patterning

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Lithography simulation has proven to be a technical enabler to shorten development cycle and provide direction even before next generation tools and processes are available. At the early stages of research, only small critical areas are of concern and, for simple research, OPC decoration is sufficient. A physics based lithography model provides the accuracy that is independent of process variations. The model helps narrow the choices of lithography tool settings and OPC strategies. In this study, new OPC software, built on PROLITHTM simulation engine, is used to evaluate various OPC algorithms. Design clips for 32nm type layouts are input into the software. Different OPC decorations including line biasing, serifs and assist features are investigated. A matrix of different NA, illumination and OPC clips are evaluated through the software optimization sequences. Best process conditions are identified based on optimal process window for a given set of random layouts. Simulation results of resist profile, process windows and comparison to wafer images are shown. Coupling OPC as a function of illumination setting into the simulation package allows one to map the source space for random layouts at a faster rate then what has been done in the past. This allows much more efficient design rule determination for the process engineer.

6520-134, Poster Session

Heuristics for truncating the number of optical kernels in Hopkins image calculations for model-based OPC treatment

C. D. Zuniga, ASML MaskTools Inc.

In the application of model-based optical proximity correction (OPC) to a full chip layout, lithography simulators require fast imaging algorithms to quickly obtain the critical dimensions or CDs of the printed features. Model accuracy is frequently traded-off for speed in order to shorten the time-to-market of a chip. The sum-of-coherent systems approximation, or SOCs, represents the current standard for fast image computation. This approximation decomposes the TCC function in the Hopkins imaging equation into a sum of products of its eigenfunctions, or kernels, via singular value decomposition. The partially-coherent optical imaging system is then represented as a sum of images formed by coherently illuminated optical systems with transfer functions corresponding to the kernels of the TCC. The eigenvalues usually decay quickly, depending on the properties of the optical system. Current models will typically use the first few dominant kernels since each additional kernel adds to the computational time. However, there is no general guideline that indicates where to cut off the series in order to obtain the necessary accuracy. In this paper, we propose a generally applicable heuristic for choosing the number of kernels.

We describe a few heuristics that show how to truncate the number of kernels that are included in a lithography model calibration, resulting in a more efficient model for OPC treatment. The heuristics are based on various eigenvalue measures such as the energy or the degree of coherence and express the CD error as a function of these measures. The heuristics then show the number of kernels needed for a given accuracy.

In order to obtain the heuristics, we tested many optical systems and mask patterns. We used two base references to obtain the CD errors: 1) a case obtained with a very large number of kernels, and 2) a case obtained using the Abbe formulation of image calculation. We used high-NA vector and thin-film models of different optical systems for current 193nm technology and calculated their TCCs and TCC kernels. Using a different number of kernels, we then calculated images of various attenuated, phase-shifting mask patterns with values of k1 in the range of 0.43 to 0.28. We primarily used 1-D CD's through pitch patterns with 90nm, 65nm, and 45nm line widths. To obtain the CDs, we used a simple threshold model and adjusted that threshold to print a target pitch. Figure 1, for example, shows how the CD error decreases as the number of kernels increases for a dipole illuminator. The figure shows that there is little improvement in accuracy in using more than eighteen kernels, corresponding to 95% of the eigenvalue energy. Using just eighteen kernels rather than the full series of thousands of kernels then results in greater computational efficiency while maintaining good image calculation accuracy. Finally, we tested the heuristics for determining the appropriate number of optical kernels in the Hopkins image calculations against a previously calibrated model that used real CD measurements.

6520-136, Poster Session

Topography induced defocus with a scanning exposure system

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With every new generation of optical lithography we push towards lower k1 factors and often trade off depth-of-focus for resolution. This requires an ever more accurate alignment of the resist film surface with the image plane. Components of variance can be grouped into spacial and temporal variation of the image plane, errors of the leveling metrology, mechanical error in wafer positioning during the exposure and systematic defocus errors induced by wafer topography.

Our case study tries to gauge experimentally the defocus component induced by a step in the exposure field substrate, with the edge of the step aligned parallel to the scanning slit. Such steps frequently occur at the boarder of different chiplets or process monitors within one exposure field. A common assumption is that a step-and-scan imaging system can correct for the majority of such topography, since the wafer is dynamically leveled under the static image plane as it is scanned.

Even in an ideal exposure case, one should expect an initially sharp image plane to be blurred in the vicinity of the step, similar to focus drilling. Further, one might expect leveling residuals due to mechanical ringing or optical interference of the leveling system.

In order to study such a case in it's pure form, we use wafer with 26mm by 26mm large recesses etched to a depth of 100, 200 and 300nm. We expose a pattern of equivalent size on top of it, however, with a 13mm offset in scan direction.

Test features spread within the image on a pitch of 2mm allow us to characterize defocus conditions and effective focus blur as a function of proximity to the step.

Our results shows that the range of defocus ringing approaches about 65% of the actual step height and thus contributes significantly to the overall focusing variance.

Planned experiments explore the scan-dependency of the observed defcos, the loss of imaging fidelity due to focus drilling around the step and the influence of thin films on leveling accuracy.

6520-138, Poster Session

Study of iso-dense bias (IDB) sensitivity to laser spectral shape at the 45-nm node

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ArF lithography is becoming more demanding as it moves into High Volume Production. Since low-k1 lithography methods are being used more extensively, CD control requirements are becoming more difficult to meet. A major contribution to improved CD control is image contrast management for optimum optical performance. Laser light source performance, particularly spectral bandwidth, commonly characterized by E95% is one of the factors that can affect CD and Iso-Dense Bias (IDB). In order to efficiently monitor and set IDB tolerance, E95% metrology functionality and CD sensitivity data are required. Furthermore, the E95% set point should be determined for various scanner and process parameters.

The CD sensitivity to bandwidth for a variety of feature sizes typical for 45nm node Immersion Lithography processes, including through pitch behavior, were measured and the results will be discussed. In addition, the feasibility of E95% control to change the IDB will be discussed.

6520-139, Poster Session

Precise measurement of process bias and its relation to MEEF

T. E. Zavecz, TEA Systems Corp.

Process Bias is traditionally defined as a manufactured offset of the mask features that induces a photoresist image size to more closely match the nominal or desired circuit design size. The metric is often calculated as the difference between the size of the image on the wafer and the mask with image reduction taken into consideration.

Optical process corrections (OPC) in the mask design must consider not only the bias but also the influence of aerial image artifacts such as near-neighbor proximity, polarization and birefringence. The interactions are further complicated by the wavefront's interaction with the imaging media and optical interactions with the translucent film stack on the wafer. With the increased frequency of resolution enhancement (RET) artifacts on the mask, the concept of bias as a simple scalar becomes less clear.

In this study bias is shown to exhibit the anticipated systematic response to all of the static exposure conditions of the process as well as the range of fluctuations within the process window introduced by production signatures.

A model is developed that allows the Bias response to be measured for each mask feature-design that characterizes not only the behavior at optimum exposure but also each features stability across process and imaging perturbation sources. The model is then extrapolated to define the relationship between Bias Response and the Mask Error Enhancement Function (MEEF).

The bias models are next applied to profile metrology gathered from fixed and matrix exposure data. Bias is shown to exhibit the anticipated variation to normal process fluctuations but with additional systematic response signatures. Fine-structure perturbations in the bias are extracted and their source is shown to be linked to the imaging toolset and includes not only full-field response to lens aberrations but a sensitivity to other less obvious conditions such as scan direction and the underlying film-stack. A full analysis of the levels of each component to critical feature size variation is presented.

The analysis then turns to methods of determining OPC design-specific variation of bias response to exposure-dose and focus variation. Vertical feature edge orientation in comparison with horizontal structure bias response as well as dense-packed feature designs to isolated performance are examined. These characteristics are found to not only exhibit bias differences but to respond non-linearly to exposure and imaging conditions in a manner that can be yield-optimized by the proper selection of OPC design.

The design of the OPC feature is shown to be a strong contributor not only to resolution and depth-of-focus but also to the robustness of image response and its ability to stay centered within the process window. Proper selection of different OPC designs while yielding the same process window can therefore be further selected to enhance the stability of the process, reduce overall critical feature variation and increase yields for not only functional but high performance product.

6520-140, Poster Session

Assessment of trade-off between resist resolution and sensitivity for optimization of hyper-NA immersion lithography

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The chemical amplification provides high sensitivity of photoresists by using photoacid catalysts that are generated by irradiation for latent image formation. However, in 45-nm half pitch node and beyond, the diffusion length of the photoacid is becoming comparable to the pattern size. Therefore, it is concerned that the ultimate resolution of optical lithography may be limited by the photoacid diffusion.

We have previously presented a study on the influence of resist blur, i.e., the contrast degradation of latent image caused by the photoacid diffusion, in hyper-NA ArF immersion lithography by using an interferometric exposure tool. We have obtained experimental results that the resist blur is consistent with Gaussian blur model. Even in case of a high resolution photoresist whose diffusion length of the photoacid is approximately 11 nm in sigma, we have found that the resist blur due to the photoacid diffusion is in fact a significant issue for 45-nm half pitch node and beyond. It is expected that the resist resolution can be enhanced by reducing the diffusion length of the photoacid. On the other hand, the reduction of the diffusion length will likely cause a decrease in the sensitivity of the photoresist due to the trade-off between the resist resolution and the resist sensitivity.

In this paper, we experimentally investigate the trade-off between the resist resolution and the resist sensitivity by using various photoresists with different diffusion lengths of the photoacid. In addition, we discuss how to realize the total optimization of exposure tools and photoresists to achieve ultimate resolution in hyper-NA ArF immersion lithography. Finally, while the focus of our paper is on ArF immersion lithography, our findings are also relevant to EUV lithography.

6520-141, Poster Session

Understanding the impact of rigorous mask effects in the presence of resist models

M. C. Lam, K. Adam, Mentor Graphics Corp.

Rigorous mask effects are a well known phenomenon that have grown in importance from the aggressive use of RET to allow 193nm wavelength light to print increasingly smaller features. Despite being well known, their impact on lithography as well as the answers to the underlying question of "Do I need to worry about rigorous mask effects, and if so, when?" are not as clear. Heuristic (empirical) approaches to help compensate for mask effects, like a constant biasing of feature edges, have been proposed. These approaches are desirable since their application is simple and straightforward. Contrasting these approaches are more complex solutions that require significant modeling capability, like Domain Decomposition Methods (DDM). While more complex, these approaches offer a systematic solution to mask effects since they are derived from electromagnetic theory. Complicating the issue is that the optics/electromagnetics of the litho system are not the only factors that determine feature size, since empirical process models have a significant impact on observed feature sizes. A final complication for modeling mask effects is the need to balance the speed and accuracy of such models so they can be integrated into the OPC framework.

This paper investigates the use of DDM as a tool for understanding and predicting rigorous mask effects in the presence of empirical process models, and compares these results with full rigorous simulations as well as Kirchoff simulations to assess the impact of rigorous mask effects. It is shown that even a Constant Threshold Resist (CTR) model

can effectively compensate for mask effects at a single plane of focus, however, it is only when through focus behavior is observed, that the true impact of mask effects can be ascertained. The focal behavior of a feature can show dramatic differences in observed CD when mask effects are not modeled properly, leading to unknown process variation and a changed process window. Knowledge that current empirical process models "push" mask effects to other focal positions has strong implications for the future of OPC and OPC verification, as it will become increasingly important to have process window models that accurately predict feature behavior across a host of process conditions. The simple biasing strategy is shown to work fairly well at compensating, but not fully mitigating, mask effects through focus on features with high image slopes. However, the biasing strategy can fail at areas of aggressive lithography where poor image slope is obtained. Investigations will also determine the smallest feature size that DDM can accurately model and the results of a full model calibration with DDM will be presented and compared with a full model calibration without DDM.

6520-142, Poster Session

Transistor-based electrical test structures for lithography and process characterization

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A 65nm, NMOS only, multi-student collaborative testchip has been designed to characterize lithographic and pattern transfer related sources of variation. The testchip has over 10,000 individually probable transistors with hundreds of different contexts and proximities, dozens of different design strategies, and six different contributing students (Figure 1). Since every structure is electrically probable on an automatic probe station, massive amounts of statistically significant data can be analyzed and significant sources of variation can be characterized.

Different electrical test structures are designed to be sensitive to misalignment, Line Edge Roughness (LER), corner rounding on active and poly, etch effects, defocus, dose, and other aberrations. LER, for example, can be characterized by looking at transistors with different widths and printing gates that have poor or good Image Log Slope (ILS) (Figure 3), which has been shown to correlate well with LER . Since corners are hard to print and harder to print consistently, a set of test structures looks at the effects of corner rounding with an array of structures that range from violating min spacing rules and having significant corner rounding to having sufficient amount of space to produce a very rectangular transistor. Also, image quality and gate length variation is a strong function of pitch, so 5 line arrays have been fashioned into transistors in series with pitches varying from 180nm to 1um pitches with a 20nm step. If defocus, misalignment, dose offsets, and other aberrations can have predictable effects on the different structures, then it will be possible to diagnose the variation and understand the main contributors.

The multi-student testchip has been taped out on two donated shuttle style high performance attenuated phase shift masks at Toppan Photomask and is being manufactured at Cypress semiconductor on their baseline 65nm process flow. The standard CMOS process was modified to produce NMOS only devices as well as "enhanced NMOS transistors" that have a much stronger correlation between gate length and threshold voltage . All wafers will be exposed on an ASML 1250 193nm scanner that allows to program errors such as misalignment, defocus, and dose as well as varying the amount of aberrations in the lens. Test structure response to lithographic nonidealities was characterized using the Parametric Yield Simulator in terms of gate length, leakage, and drive current variation2. Resist images and poly images from CD-SEM will be correlated with simulation results. Electrical four point probe measurements will be used to characterize systematic across field and across wafer variation and electrical leakage current measurements will be used to characterize proximity dependent and random variation. We anticipate to characterize the main source of variation on this 65nm process flow from extensive electrical measurements that will be correlated with pattern dependent responses that were characterized using the Parametric Yield Simulator.

6520-143, Poster Session

Use of starburst patterns in optical lithography

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We propose to use a starburst pattern as a powerfull diagnostic tool in optical lithography. A starburst pattern of constant line/pitch ratio versus radius can be used as a quick diagnostic tool for various off-axis illumination techniques, in particular those that have non-isotropic illumination shapes. Because such a starburst features a multitude of pitches at a multitude of angles, a large area of the pupil is sampled. Carefull analysis of the image of the starburst gives information on the kind of illumination that is used, the relative dose for a particular pitch, the resolution limit for all angles, and can be used to find the best focus position. We perform an analysis of the characteristic regions of a starburst image for a given illumination and interpret the images accordingly.

In addition two dipole illumination schemes are compared to demonstrate the trade off in resolution in one direction for the other. Also the mask transmission impact on through angle resolution is reviewed. Aerial image simulations of the starburst patterns are analyzed and compared to the experimental results.

6520-144, Poster Session

Challenging to meet 1-nm iso-dense bias (IDB) by controlling laser spectrum

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According to ITRS Roadmap, the requirement of Gate CD Control defined 2.6nm at 65nm HP. One of the CD Errors is contributed by Iso-Dense Bias (IDB) which could be more challenging to meet. Assuming 40%of CD errors are dominated by IDB, IDB should tolerate less than 1nm. General speaking, majority of IDB are due to : first, aberration related, flare, and Sigma fluctuation by exposure tool, second, Photo Resist characteristics change as realized. But, Band Width (BW) characteristic by Laser source is another contribution because ArF exposure tool is getting popular these days.

Hence, Laser Bandwidth (BW) is ideally monochromatic which is not affected by chromatic aberration change. The reality is that the BW has been showing the Gaussian shape of spectral and has some width. 95% Integral area of this spectral shape calls E95% which is now measurable and is developed by Cymer.

This paper will discuss about the sensitivities of Litho Processes against E95% as mentioned as below and optimum value of E95% in order to meet 1nm of IDB.

-IDB vs. E95%

-CD at through pitch vs. E95%

-Process Latitude vs. E95%

-DOF

-EL

-Pattern shortening vs. E95%

6520-145, Poster Session

Impact of mask error on OPC for 45-nm node

O. Park, Infineon Technologies North America

As lithography, pushes to smaller and smaller features under the guidance of Moore's Law, patterned features smaller than the wavelength of light must be routinely manufactured. Lithographic yield in this domain is directly improved with the application of OPC (Optical and Process Correction) to the pattern data. Such corrections generally assume that the mask can reproduce these features exactly. The Mask Error Enhancement Factor (MEEF) serves to amplify mask errors, and can reduce the benefits of OPC in some circumstances. A concept of the globalized MEEF is introduced by considering fitting with measured and simulated. In general, global-bias type of OPC model may work well in applications where solution to the EPE calculation is intractable. The range of global bias value that we calculated can estimate the

accuracy of this approach. Further studies are required to fully understand and characterize 'localized bias' to cover different type of design instead of global bias approach. In this paper, we present the characterization of the MEEF for 45nm technology attenuated phase shift mask to figure out how to measure the mask errors relative to design and try to figure out new ways to reduce model sensitivity to mask deviations for metal level.

6520-147, Poster Session

Taking image quality factor into the OPC model tuning flow

C. Wang, Q. Liu, Semiconductor Manufacturing International Corp. (China); L. Zhang, Mentor Graphics Corp. (China)

All OPC model builders are in search of a physically realistic model that is adequately calibrated and contains the information that can be used for process predictions and analysis of a given process. But there still are some unknown physics in the process and wafer data sets are not perfect. Most cases even using the average values of different empirical data sets will still take inaccurate measurements into the model fitting process, which makes the fitting process more time consuming and also may cause losing convergence and stability.

The Image quality is one of the most worrisome obstacles faced by next-generation lithography. Nowadays, considerable effort is devoted to enhance the contrast, as well as understanding its impact on devices. It is a persistent problem for 193nm micro-lithography and will carry us for at least three generations, culminating with immersion lithography.

This work is to weight different wafer data points with a weighting function. The weighting function is dependent on the Normal intensity log slope (NILS), which can reflect the image quality. Using this approach, we can filter wrong information of the process and make the OPC model more accurate.

CalibreWorkbench is the platform we used in this study, which has been proven to have an excellent performance on 0.13µm, 90nm and 65nm production and development models setup. Leveraging its automatic optical-tuning function, we practiced the best weighting approach to achieve the most efficient and convergent tuning flow.

6520-148, Poster Session

Effects of laser bandwidth on iso-dense bias and line-end shortening at the 65-nm/45-nm node

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Control of Isolated and Dense line Bias (IDB) and Line End Shortening (LES) in a lithographic process has become increasingly important, particularly for the 65-nm and 45-nm nodes. The IDB depends on many factors, for example, focus, lens aberrations, partial coherence and laser spectral bandwidth.

The impact to IDB and LES from the change of laser bandwidth has been studied. Both ArF dry and immersion scanner have been investigated on typical 65-nm and 45-nm structures. A sensitive spectrometer was connected to lithography laser, allowing careful measurements of both FWHM and E95 parameters of the laser spectral profile. The spectral bandwidth was adjusted over a larger range than normally experienced value during wafer exposures by carefully varying the laser operating conditions to provide controlled changes in bandwidth while maintaining all other laser performance parameters within specification. The results of measurements made using the high accuracy on-board etalon spectrometer were compared to off-line measurements using a reference grating spectrometer.

Measurements of both line width and LES on several 65-nm and 45-nm product layers were made and correlated with laser bandwidth to determine the sensitivity of IDB and LES to bandwidth variation. The sensitivity to both E95 and FWHM measures of bandwidth was assessed.

6520-149, Poster Session

On the quality of measured optical aberration coefficients using phase wheel monitor

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In-situ aberration measurement requires indirect methods that reconstruct the phase of a wavefront from the measured images. Phase wheel monitor allows such in-situ measurement of aberrations in photolithography systems. The projection lens aberrations may be obtained with high accuracy from images of phase wheels targets printed in resist. Resulting features are mathematically analyzed to extract information about the aberrations in optics. We use a detection algorithm and multi-domain modeling to process resist images and determine the image deviation from the ideal shape, which in turn allow the amount of aberration introduced by the optical system to be quantified.

This paper provides a complete analysis of the number of tests performed on state-of-the-art full field exposure systems. Experimental results are shown and performance is correlated to interferometric lens data as well as independent lithographic imaging tests.

6520-150, Poster Session

A comparative study for mask defect tolerance on phase and transmission for dry and immersion 193-nm lithography

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Application of immersion lithography has extended the lifetime of 193nm lithography. It has enabled numerical aperture (NA) of greater than 1.0 and allows rooms for improvement in resolution as well as depth of focus. Imaging behaviors of immersion system will determine the extent of resolution enhancement technique (RET) required. A comparative study of imaging performance of 193-nm dry and immersion lithography for printing a CD of 45nm and below is done through simulation software LithocruiserTM version 2.0. Calibrated resist model is used in the simulations to achieve better predictability of the actual performance. Features under study include one dimensional (1D) lines and space and two dimensional (2D) contact holes array. The performance enhancement provided by immersion system for printing both 1D and 2D features is evaluated from the depth of focus, exposure latitude, images contrast and process windows available. Effect of variation of illumination setup on printing is studied and feasible configurations will be proposed for printing features of different pitch and alignment. Mask defect tolerance on phase and transmission for both dry and immersion system is studied to establish an acceptable level of disposition for mask defects on Phase Shift mask. Mask defects under study include defects on edge, on MoSi and between tight spaces.

6520-151, Poster Session

Understanding the causes of horizontal-vertical (H-V) bias in optical lithography, part II

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CD control requirements have entered the remarkable regime of single digit nanometers. As such, previously negligible sources of CD variation are becoming of primary concern. One example of a CD variation that has typically been thought of as a second order problem is the horizontal-vertical (H-V) feature bias, the difference in the CD between horizontally and vertically oriented features. This paper, a continuation of previous work, will continue to examine in detail several causes of H-V bias primarily as a function of asymmetry in more complicated multi-pole source shapes.

6520-153, Poster Session

OPC-free on-grid fine random hole pattern formation utilizing double resist patterning with double RETs

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A novel method for on-grid fine random hole pattern formation is developed based on optical image calculations. 90nm random hole on 200 nm base pitch grid can be formed with DOF of over 0.30 μm at KrF exposure under NA=0.82. Moreover, this method is not needed troublesome OPC.

In our previous work [1], some of the authors have developed a novel RET such that a fine random dark point image can be generated by application of high-transmission Atten-PSM and a specific modified illumination. In that work, fine random hole pattern formation has been demonstrated with negative-tone resist under KrF exposure. Unfortunately, in current days, industry cannot find any negative-tone resist with sufficient performance for ArF exposure. Hence, the previously proposed method for fine random hole cannot be realized at the most advanced lithography. At this situation, the authors consider an application of this superior RET to plugging of unnecessary holes in pre-determined high dense fine holes.

Image calculations are carried out at KrF wavelength for the convenience of experimental proof of the concept and mask fabrication. As process step, first, dense hole pattern will be formed in the first resist film. In this process step, high-resolution positive-tone resist and cross-pole illumination will be employed. By application of cross-pole illumination, dense hole pattern is well imaged with large focus and exposure latitude. At optical conditions of l=248nm, NA=0.82, DOF of larger than 0.30 um can be obtained for 200 nm pitch dense holes with 90 nm diameter from calculated optical image. After development of the first resist, resist hardening should be carried out so as not to cause resist mixing at second resist process. One of proven processes for the hardening is Ar ion implantation, while some other processes such as EB cure or DUV cure are considered as possible candidates.

Then, second lithography process will be carried out on the first resist film with dense hole pattern. In this process, as described in the previous work, high-transmission Atten-PSM and cross-pole illumination are employed to form random dark spot image. Mask pattern consists of on-grid random holes, which are laid out at some parts of dense holes to be plugged. Figure shows a typical mask pattern and optical image formed with the mask. The hole size on this mask is not needed to be changed by surrounding patterns. A unique size mask pattern can form dark spot with high process latitude. Moreover, resist bridge formation between neighboring plugs can be acceptable, because of no negative effect. As can be seen in the left figure, shape and size of dark spot image is not uniform. But minimum intensity at the spot shows enough small to rest resist after development, at a exposure dose enough to remove the second resist for excavating buried holes in the first resist film. Accordingly, OPC is not needed in this method. By application of this dark spot image to a high-resolution positive-tone resist, resist plugs will be formed at undesired holes in the first resist film.

As mentioned above, while calculation study is carried out with KrF exposure, this method is mainly aimed to apply for ArF exposure. Because image formation is scalable with wavelength, this method is effective in ArF lithography. In ArF regime, random on-grid hole with 130 nm pitch and 60nm size can be achieved by this method with currently available hyper NA immersion exposure tool. The patterning performance may meet requirement for 45 nm generation devices.

6520-155, Poster Session

Virtual OPC for hyper-NA lithography

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Traditional OPC modeling uses the measured critical dimension (CD) data for various patterns at a specific exposure condition. Virtual OPC is a new OPC sequence, in which full physical simulation data to the resist image is used for OPC modeling instead of measured CD data. The measured CD data may have errors caused by metrology tools and SEM shrinkage. Virtual OPC doesn't have to consider those errors, as long as the simulation results are accurate.

Simulation accuracy is the key factor for the success of virtual OPC. For the accurate simulation, the accuracy of simulation algorithm is essential before everything else. In addition, the same exposure condition as fab. conditions - NA, aberration parameter, flare, illumination shape, resist parameters etc.- should be used in the simulation of sample data for modeling. Accurate 3D mask simulation is also required for sub 50 nm devices using hyper NA lithography. In this study, the accuracy of optical image simulation is compared with commercial simulation tools. However, the effect of scanner parameters such as NA, lens aberration, flare, real illumination shape was studied by many researchers. Thus, these parameters are not considered in this study. The Weiss model is widely used as a resist development model because this model provides easy and fast method for resist parameter extraction. However, the current Weiss model shows a limitation on accurate iso-focal point, so a modified Weiss model is suggested. For 3D mask simulation, accurate algorithm and mask material's parameters should be guaranteed. Since the verification of 3D mask simulation algorithm is not a simple problem, commercial simulation tools are compared only in terms of aerial image with 3D mask simulation.

Preliminary simulation results present refractive index of mask materials affects to iso-dense bias and horizontal-vertical bias in the case of dipole illumination with polarization. Accurate simulation data can be obtained by previously described efforts. Finally, virtual OPC is applied to sub 50 nm flash memory device. Detailed virtual OPC application results to sub 50 nm devices are presented.

6520-156, Poster Session

Mask-friendly OPC correction for higher throughput and lower mask costs

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The noticeable mask data size increase in the last couple of years has grabbed the attention of all the IC industry. This increase is negatively affecting the throughput and masks costs [1]. Mask Data Preparation (MDP) is also beginning to consume pronounceable share in the cycle time consumption [2]. All this is making it harder and harder to have an efficient number of small testing and production cycle for each node before achieving maturity. One major factor for the explosion of the mask data sizes is the necessary Optical Proximity Correction (OPC) phase, where millions and millions of small jogs are created to achieve the design fidelity [3].

In this work, different approaches are studied to reduce the number of unnecessary jogs in the output of the Model-Based OPC (MBOPC) operation. This is achieved by merging back the small jogs that don't contribute largely to the correction. This merging is used at non-critical regions (i.e. excluding gates and High-MEEF areas). Different criteria are used to judge when to merge the fragments, from which are the jog size of the OPC output, or the severity of the aerial image ripples (ringing) at the edges before and after OPC. The merger of the correction fragments is done within the OPC iterations so its effect is accounted for in the last few OPC iterations. An additional advantage of this approach is the reduction of the false inspection alarms that are well known to occur in regions of very small notches and jogs due to the inspection tool problems in distinguishing between fine OPC corrections and mask defects. The Results are showing a pronounceable reduction in the estimated mask production shot count number while the effective Edge Placement Error (EPE) due to this correction is almost unnoticeable.

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6520-157, Poster Session

Methods and factors for OPC run-time optimization

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With the increasing complexity of design and shrinking of technology nodes, optical proximity correction has become an integral part of IC fabrication. Pattern fidelity is the base line for any accurate OPC model. Calibrated process models are used to make iterative pattern adjustments over a fragmented design to align simulated images and the target layout. More and more advanced modeling techniques are deployed for accurate prediction of complicated 1D and 2D simulations. As such, more aggressive layout situations must be taken into consideration for different process and OPC aspects such as optimization of process window, contrast, MEEF, EPE convergence, and many more. However, along with different process optimizations the mask complexity increases and the OPC run-time is also adversely affected. Often, it has been noticed that the OPC model accuracy is restricted by long OPC run-times. The variation in OPC run-time could be due to many factors, namely number of finitely sized segments, multiple iterations, EPE convergence, multiple process conditions, grid size, step size, sitelength, model complexity, etc.

Integration of fast and accurate analysis is needed while addressing the growing complexity of OPC solutions. We present here different approaches for OPC run-time improvement. A methodology is prepared to investigate best practices in OPC modeling. Additionally, proper selection of fragmentation, simulation sitelength, and number of iterations can be modified to achieve significant improvement in computation speed. The variation in run-time is assessed for different approaches listed above with an emphasis on OPC accuracy. Statistical analysis is used to measure Image parameters and EPE for various experiments, and the output is the measurement and plotting of accuracy vs. run-time. This paper will present those results and suggest best practices for OPC run-time improvement that can be incorporated as a part of an OPC model building and OPC qualification flow.

6520-158, Poster Session

Golden curve method for reticle and OPC signature stability control of optimized lithography in advanced high-MEEF applications under DFM flows

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Model based optical proximity correction (OPC) and phase shift masks (PSM) are common, enabling technology for advanced lithography at high numerical aperture. In the high resolution regime it is typical for the mask signature sensitivity to be amplified by a high mask error enhancement factor (MEEF)1. Recently, much work and development has gone into the characterization and reduction of design related low contrast “hot spots”. All of these factors are crucial to the first time success of designs as part of a disciplined design for manufacturing (DFM) flow2.

However, there is a significant risk to the above resolution enhancement techniques (RET) and DFM infrastructure if the reticle supply shows fluctuations in the complex signature components for new or revised designs. Typically, the way that OPC models are developed is by printing a reticle with representative patterns, including reticle signature errors (linearity, proximity, fidelity). Since the OPC model must be developed quickly, the normal variation in the reticle signature over time from reticle to reticle is not introduced into the OPC model to test for robustness. Moreover, the most advanced wafer lithography development is done on the earliest available reticles which may have only limited statistics on variation from mask fabrication tools and process effects3.

This paper introduces a new methodology for characterizing, quantifying, and controlling reticle signature components in order to limit the lithographic impact of reticle variation that could jeopardize all of the OPC model building and design verification of the DFM flow. We have implemented a “golden curve” method with refined reduction statistics to provide metrics that will sustain reticle stability, even at the leading edge of advanced process development. Hence, the golden curve forms a key characterization component in the overall RET and DFM strategy that is essential for 65nm and below applications.

6520-159, Poster Session

Mask enhancement using an evanescent wave effect

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State of the art lithography is continually driven to resolve smaller features, driving k1 values increasingly lower. In order to image these difficult features with reliable fidelity, engineers must increasingly use Resolution Enhancement Techniques, or RETs. One such technique that is proposed in this paper uses small, sub-wavelength grooves that are placed in close proximity to a main feature.

These sub-wavelength grooves create evanescent fields which are bound to the surface between the absorber and the mask substrate, decaying exponentially in lateral directions. In this work, we demonstrate the ability to use such Evanescent Wave Assist Features (EWAFs) to enhance the propagating near and far field energy within openings (such as slits and contacts).

A mathematical model is examined which describes the effect of the sub-wavelength features. The model is compared to the results of simulations using Finite Difference Time Domain (FDTD) models. Several cases of absorber material, feature type, spacing, and illumination will be presented.

6520-160, Poster Session

The gate CD uniformity improvement by the layout retarget with refer to the litho process

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As the minimum pitch size becomes smaller, the gate-poly critical dimension uniformity (CDU) is a critical parameter for the device performance and an important indicator of the OPC capability. From the photolithographic point of view, the root causes of increasing CDU is due to corner rounding effects, ripples, misalignment between the gate-poly and active layers.

The corner rounding effect of the gate-poly region on the active can be severe for the sub L50 device because the space between the active layer and the gate-poly layer becomes narrow. Although this effect can be handled during the OPC or in the design house, the OPC is to improve the gate-poly CDU in this paper. Ripple phenomena is captured using the pixel based simulation on an OPC tool and minimized to improve the CDU. Additionally if misalignment exists in the minimum space between the active layer and gate-poly layer during the photo process, this corner rounding effect can be more serious, so this misalignment accounted to reduce the corner rounding effect on the gate-ply CDU.

The method which can be used to improve gate-poly CDU is defined as “Litho Process-aware OPC for the Gate-Poly CDU improvement” in this paper.

An active layer is sized about 10nm to consider the misalignment in the photo process prior to an OPC correction. The evaluation points’ step size was adjusted to 20nm in the gate region for the pixel based OPC, which was determined by sizing the active layer to 10nm and critical points are searched with the EPE monitoring of several evaluation points during the OPC operation. With this cost function, a field poly is retargeted to solve the corner rounding effect and ripple effect as long as there are no contact overlap margin problem and no pinching issue during the OPC correction.

As a result of retargeting to accommodate, a corner rounding and ripple effects and misalignment correction led to an improved gate-poly CDU for a sub-50nm device

6520-161, Poster Session

Toward standard process models for OPC

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We present calibration and simulation results of applying Compact Model 1 (CM1) and Variable Etch Bias (VEB) models to OPC and OPC verifications. We discuss model formulations, study calibration techniques, and compare model predictions to the resist and etch critical dimension measurements. We discuss advantages of using these models as standard pattern transfer models during chip-scale process simulations.

6520-162, Poster Session

Modular process modeling for OPC

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Driven by rising requirements of current and future technology nodes the effort for OPC modeling is increasing steadily. On the one hand, OPC modeling accuracy needs to be improved to meet tighter specifications; on the other hand application of OPC is being expanded to more and more levels. Moreover, additional process window models are required for DfM applications, like layout simulation during the early development phase. This development comes along with huge measurement efforts of several thousands of measurements for a single level. At the same time efforts are spent to increase the model accuracy by including more realistic assumptions of the scanners and steppers and the process steps to the model, like thin film stack in combination with vector models, explicit etch models, 3D mask effects, measured illumination sources etc.

Different approaches are pursued in order to cope with the challenge of keeping efforts for OPC manageable. Much energy is spent on automation of the OPC modeling loop, including generation of OPC test masks, generation of SEM recipes, OPC measurements and subsequent OPC model building.

Another approach is to aim for modular OPC modeling, describing mask, optics, resist and etch processes separately. OPC models often have to be re-calibrated as the process is adjusted and optimized. By exchanging single modules of a modular OPC model, a fast reaction on process changes during process development is possible. At the same time efforts can be reduced, since only single modular process steps have to be re-characterized as input for OPC modeling.

Commercially available OPC tools capable for full chip runs commonly make use of a semi-empirical model, which is in a non-modular way describing the complete process including mask, optics, resist and possibly etch. Runtime requirements prevent here an exact physical modeling, and a compromise between accuracy and runtime has to be accepted. However, when modeling the complete process by one single OPC process model, the single process steps are coupled among each other in an unphysical way. Model variables are used for describing process steps they are not meant to account for. This counteracts the modular approach, and the ability of the OPC model to extrapolate beyond the calibrated range is only limited. Even reliable interpolation needs to be ensured by dense sampling of input OPC measurements, thereby preventing to run into possible instabilities of the OPC models.

The goal of our work is to investigate to what extent a commercially available OPC tool can be applied for modeling of single process steps as separate modules. For an advanced gate level process we analyze the modeling accuracy when combining models for each process step - optics, resist and etch - for differing single processes to a model describing the total process.

Knowledge of achievable accuracy limits when using an OPC model for the total process composed by modules describing single process steps is prerequisite to specify application ranges of modular OPC models. Based on the results valuable conclusions for optimization of OPC modeling efforts are possible.

6520-163, Poster Session

Predictive post-OPC contact and via printability metric and validation

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Yield is one of the most important factors for massive chip production. As the process variations increase in modern technologies, there is a high possibility that a via could fail because of the the complete or partial via. Focus and dose variations are the two most important process variations. In order to enable designers make better design decision, fast via printability metric under lithography process variations should be needed. Predicting the post-OPC printability without doing real OPC was difficult. In this paper, we develop a predictive pre-OPC lithography metric for the post-OPC critical dimension (CD) errors of vias taking advantage of the via shape pattern simplicity. We validate the accuracy of the metric against post-OPC data.

6520-165, Poster Session

Analysis of pattern density on process proximity compensation

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Extremely tight ACLV (across-chip line-width variation) control of the gate level has been required to meet the performance goal of advanced flash memory. Even though the CD (critical dimension) after photo process can be tightly controlled by lithographic MPPC (model-based process proximity correction), etch loading effect usually causes the variation of the final CD hence the ECD (post-etched CD) is more important for device performance than the CD after photo process. Some studies [1-3] have considered etch proximity correction, and the Tandem PPC (process proximity correction) [1] is much easier to be implemented because it corrects the optical and etch proximity effects independently in a multi-step fashion. Since the etch proximity correction rule decides the control accuracy of the final CD in multi-step PPC, the test pattern design and CD data gathering method are crucial to extract a rule as accurate as possible.

Figure 1 shows the test structure design in this study, the test vehicle was designed with 4 different mask transmittances and simulated the gate level pattern in memory block of real chip. And the test patterns inside the different transmission areas were split with various space widths (S2) and various dummy pattern blocks (W1) to the measured pattern. Through the combination of different transmission areas in the test mask and suitable wafer map design, various chip-level pattern densities of 40% to 70% and wafer-level pattern densities of 35% to 65% can be achieved to extract the more accurate data for optical and etch proximity corrections. The results displayed in Figure 2 reveals that the lines at memory block edge area are the most subject to the photo proximity and etch loading effects, the DCD (photo CD) decreased as the space width between two memory blocks increases but the etched bias behaves a reverse manner. But the wafer-level pattern density affects the etch loading effect significantly, as shown in Figure 3, the etched bias increases as wafer level pattern density increases. Apart from our main concern of PPC, the flare effect is the subsidiary behavior observed to affect the DCD as local coverage changes. After the key contributors to the PPE were identified and accurate data has been extracted from the memory block like patterns, the photo and etch proximity effects can be modeled as function of memory block separation, local pattern density as well as wafer-level pattern density. Finally, the respective photo and etch proximity through model-based PPC and rule-based PPC were applied in a multi-step flow to products, which could be different in local pattern density and wafer-level pattern density due to the different memory densities.

6520-166, Poster Session

Advanced new OPC method to improve OPC accuracy for sub-90-nm technology

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OPC has become an indispensable tool used in deep sub-wavelength lithograph process enabling highly accurate CD (Critical Dimension) control as design rule shrinks.

Rule based OPC was widely acceptable in the past, however it has recently turned toward model OPC according to the decreasing pattern size. Model based correction was first applied to the optical proximity phenomenon because the image of sub-wavelength pattern is distorted severely during the optical image transformation. In addition, more tight CD control required to compensate the process induced error effects from etch or other process as well optical image can be achieved.

In this paper, we propose advanced new OPC method to obtain better accuracy on the final target for sub-90nm technology. This advanced method converts measured CD data into final CD target by using an equation. We compared the results from the data converting method, suggested in this paper, with those from post-lithography (DI) and post-etch (FI) OPC model step by step. Finally we confirmed that advanced new OPC method gives better accuracy than that from conventional DI and FI OPC model.

6520-168, Poster Session

Improving the model robustness for OPC by extracting relevant test patterns for calibration

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Recently, photolithography process is facing many difficulties in patterning the circuit adequately, mainly due to the rapid decrease of the k1 factor. The limitation of numerical aperture (NA) causes the distortion of printed patterns, such as corner rounding, line end shortening, and the different bias between isolated and dense figures. The optical proximity effect correction (OPC) is the most popular method to solve this problem. Especially, we should apply the model-based OPC to the critical layers as the circuit patterns get smaller and more complex. The success of model-based OPC largely depends on the quality of the model, which describes the physics in the resist under a specific optical condition. A “good” model should have both the low fitting error and the full chip coverage. Efforts to lower the fitting error can lead to the degradation of physical meaning, and this would result in insufficient coverage of the model. To settle this concern, we should extract test patterns for model calibration that cover all the aerial image properties of full chip geometry. The variation of the model space during iterations of correction process should also be considered. In this paper, we will present test pattern selection strategy based on the model space analysis over the full chip geometry and the correction process, which is verified by the comparison of wafer and simulated results by the model based on the proposed method.

6520-169, Poster Session

Two-dimensional dry-etch modeling using local density approach for 65-nm node and beyond

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Model-based OPC allows high accuracy pattern transfer in resist regarding to rule-based approach. During the OPC step, the dimensions of the patterns targeted by the lithographers are linked to the etch process which is following. A re-targeting step is thus needed to anticipate the etch-biasing on patterns edges. Rule-based approach is currently used to pre-compensate patterns dimensions and complex rules are needed to account for complex 2D designs. However, a rule-based approach is very limited and, with each successive generation, it hardly manages to compensate all the etch effects. Thus, a model-based correction becomes more and more indispensable to achieve high accuracy pattern transfer in silicium.

In this paper, we introduced a model-based approach to compensate etch effects. The model aims to simulate the micro-loading effects during the dry-etch process. This approach is based on the evaluation of the local density of patterns and allows calibration on 1D or 2D patterns, as well as on symmetrical or asymmetrical patterns. This model-based correction is then implemented in the OPC flow for the re-targeting. In this paper, the detailed methodology will be given from the calibration step to the correction flow. Comparison between model simulations and wafer measurements will be given for the poly layer at the 65 nm node.

6520-170, Poster Session

Rapid search of the optimum placement of assist feature to improve the aerial image gradient in iso-line structure

J. Li, Q. Yan, L. S. Melvin III, Synopsys, Inc.

In modern photolithography, the dose latitude, Normalized Image Log Slope (NILS), and hence the image quality are closely related to the gradient of the aerial image intensity at the evaluation point. The placement of sub-resolution assist feature (SRAF) in the isolated lines helps improve the aerial image quality by increasing the gradient. Traditionally, it is simple and straightforward to calculate the effect of the SRAF placement on the gradient at a certain evaluation point. The gradients before and after the SRAF placement are computed separately. The difference between these two gradients manifests the magnitude of the effect. However, this simple methodology is only convenient when the location of the SRAF placement is known and it is not adaptable for searching for the optimum placement as many of the placements need to be evaluated.

In this report, an innovative and rapid solution is presented. Derived from Hopkin’s equation, the aerial image intensity is the sum of the squared electrical fields of the coherent imaging systems, which are the integration of the mask transmission function and the eigenvectors of the transmission cross coefficient (Tcc). The gradient of the aerials image intensity can be then expressed as twice the sum of the product of the electrical field and its derivative. When the assist features are added to the main feature, it can be treated as small perturbation to the main feature. This approximation simplifies the computation of the effect of assist feature on the aerial image gradient by neglecting the high order term in the aerial image gradient equation.

The effect of SRAF placement on the gradient can approximated by two terms, the first of which is the product of electrical field of the main feature and the electrical field derivative of the assist feature, and the second of which is the product of the electrical filed derivative of the main feature and the electrical field of the assist feature. In iso-line structure, this method allows one to calculate the change of the aerial image gradient caused by SRAFs placed at any desired locations and no iteration is needed. The equations for the aerial image gradient and the change due to the mask perturbation can be found in the attached file. The detailed results will be reviewed in the full paper.

6520-171, Poster Session

Implementation of pixel-based OPC considered process variation with process window model

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Below the 65nm node, the process window of lithography process becomes narrower due to low k1 factors. In order to enlarge the process window, various RET strategies such as OAI, alt-PSM would be utilized. It is also an effective suggestion to restrict some pattern types capable of inducing systematic defects when the application of RET is limited on account of its insufficient maturity or its expensiveness. Current OPC also provides a solution to improve process window. While

hybrid-OPC uses rule and model to improve process window on selected regions but its method is unsuitable for the logic devices having many random types of pattern or specific layer which require an accurate CD control. However, process window OPC, the correction of mask patterns by considering process variation such as off-dose and defocus should be expected to enhance the process window with minimal changes on the targeted design size. In order to precisely predict weak or hot spot patterns by simulation as process variation, process window model that is calibrated by sample data measured at not only best condition but also off-dose and defocus process conditions is also necessary.

In our study, process window OPC was performed using pixel-based correction instead of fragmentation based correction. Pixel based OPC can effectively compensate mask patterns to remove weak or hot spot patterns determined by process window model corresponding with real process variation. The results are demonstrated with a sub-50nm node metal layer potentially having many lithographic hot spots such as pattern bridging, collapse, line end shortening and contact overlap deficiency. The considerable reduction of the number of lithographical hot spots compared to that of nominal OPC implies effectiveness of process window OPC. The feasibility of process window OPC is also presented by distribution of process variation band after ORC.

6520-172, Poster Session

A feasible model-based OPC algorithm using Jacobian matrix of intensity distribution functions

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OPC algorithms usually can be divided into two steps: dissection step and edge moving step. In dissection step, edges in layout are broken into small edge segments, an evaluation point and an offset direction are chosen for each edge segment. In edge moving step, an offset along the offset direction of each edge segment is calculated to minimize edge placement error (EPE). In normal OPC algorithm, the edge segments are moved one by one. In another word, it does not consider cross interaction between edge segments. Offsets calculated in this way are not precise results. Iterations of recalculating offsets are required to get accurate results. However, this kind of OPC algorithm does not always lead to a convergent result, especially when PSM or complex illumination schemes are used.

Cobb and Granik have introduced a model-based OPC algorithm using the MEEF matrix, which takes cross interaction of edges into account ('Model-based OPC using the MEEF Matrix', SPIE Vol. 4889 p1281-p1292). Examples in their paper show advantages of the so-called matrix-OPC algorithm. However, to calculate EPE values and MEEF matrix coefficients needs to search image edge along offset direction, which includes several times of point intensity evaluation. In this paper we introduce a new kind of matrix OPC algorithm which needs less calculation.

The primary goal of model-based OPC is to minimize EPE at evaluation points by moving mask edges. An equivalent problem is to make the optical intensity at evaluation point as close to the threshold of resist as possible. Suppose I(x, y; s1, s2, ..., sn) represents the intensity distribution function on wafer, which is also a function of edge offsets s1, s2, ..., sn. Based on the equivalent problem, when EPE are zero at each evaluation point (x1, y1), (x2, y2), ..., (xn, yn), we have these equations:

I(x1, y1; s1, s2, ..., sn) - THRESHOLD = 0

I(x2, y2; s1, s2, ..., sn) - THRESHOLD = 0

I(xn, yn; s1, s2, ..., sn) - THRESHOLD = 0

The least square solution (s1, s2, ..., sn) of the nonlinear equations above is the best estimation of offsets. Newton method can be used to solve these equations. More sophisticated methods such as Levenberg-Marquardt algorithm can give better numerical performance and global convergence.

Jacobian matrix of the nonlinear equations are needed to solve the equations. Usually the calculation of Jacobian matrix needs lots of computation. However, if the optical model is based on convolution kernels, it can be speeded up. m_ij in the Jacobian matrix can be calculated as below:

m_ij = SUM (2 * lambda_k * f_ki * df_kij)

in which:

f_ki = Phi_k CONV Mask_i

df_kij = Phi_k CONV dMask_ij

Mask_i is all polygons near evaluation point (xi, yi). dMask_ij is a small perturbation rectangle near edge segment j, the value of df_kij can be calculated quite fast using lookup table method.

The Jacobian matrix is a sparse matrix. It is quite important to use a sparse linear equations solving algorithm in each Newton iteration step to make the matrix-OPC algorithm has a feasible speed for real application.

To avoid that the Jacobian Matrix is too large to solve, we should cut the whole layout into small areas with a surrounding band, then perform correction one by one or in parallel.

Experiments show that the new algorithm can achieve the aim of accurate EPE control and global convergence of iteration. Currently the correction speed using this new algorithm is 4-5 time slower than the normal algorithm. But we think that the gap can be narrowed by algorithm optimization and computation parallelization.

6520-173, Poster Session

Geometrical description of the microloading effect in silicon trench structures

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Standard Model Based OPC is based on resist and after etch CD measurements. In the case of non-linear photo-etch bias due to the etch microloading effect, two-dimensional configuration can be wrongly corrected by the OPC model and hence lead to possible Si bridging. This paper reports a geometrical model for the determination of potential bridging in silicon trench structures that depends on the proximity of neighboring features. The model shows a possibility to detect and correct the post OPC data base by taking into account the non-linear effect caused by the non linear etch microloading. This approach can at the end leave the OPC model with a more straightforward photo resist model (and prevent the need to recreate a new OPC model), awhile-adding additional step of correction just in the locations of killer effects like bridging may occur.

6520-174, Poster Session

Investigation of DFM-lite ORC approach during OPC simulation

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In recent year DFM, IFD, ORC has been evolved besides OPC (Optical Proximity Correction) to improve time required from design to manufacturing along design to mask data preparation flow. Insertion of ORC (Optical Rule Check) after OPC in separate mask data preparation step has been adopted in order to meet the ever increasing need of advance lithography node like 130nm, 90nm, 65nm & below, during post design mask data prep flow. It is not unusual that different ORC & OPC platform are used during processing. Investigation has been made to look into possibility of DFM-lite ORC approach insertion during OPC run on same Calibre platform, by providing additional intelligence necessary & hopefully achieve lower combined cycle time to realize the benefit of both OPC & ORC in single simulation run.

6520-175, Poster Session

Migrating from traditional OPC to field-based OPC for 45-nm node production

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The upcoming 45nm device node is a point at which newer field-based (i.e., dense pixel-based) OPC computation methods may begin to show

advantages over traditional flash-based OPC computation methods. In very dense and complex layouts, a field-based method has an advantage due to the reduced number of physical locations at which it needs to calculate optical and process information vs. a traditional method. However, new production OPC implementation challenges arise with the switch to field-based methods. The challenges include optimization of hierarchical processing, and asymmetry control in critical matched transistor circuits (such as SRAMs for the 45nm generation where noise margin is a fundamental device control issue). A successful manufacturing field-based OPC solution will overcome these challenges while still providing runtime vs. layout density benefits.

In this paper we describe the manufacturing implementation of field-based OPC at the 45nm device node. We discuss the transition in tools and methods from 65nm and 45nm generation traditional flash-based OPC to manufacturing ready 45nm field-based OPC. We also detail a hybrid OPC methodology which incorporates traditional benefits of flash-based OPC with the runtime improvements for dense layouts of field-based OPC. Runtime, memory usage, model stability, correction accuracy, correction symmetry and ease of implementation results will be shown on product design databases.

6520-176, Poster Session

A study of 3D mask effect on CD variation for 65/45nm

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In the very beginning of the optical lithography simulation, the mask element, though actually with limited thickness, is always considered as purely 2-Dimensional, or in other word, the mask thickness is infinitely thin. This is always a good approximation when the critical dimension is relative large and the Numerical Aperture of the optical imaging system is smaller than 0.7, for which the image distortion induced by the mask thickness and profile under such conditions are negligible. Even adopting infinite thin mask approximation described by Kirchoff approach, accurate simulation results can be achieved. However, for higher NA microlithography processes, the polarization of the illumination source and profiles of mask become important factors that will be reflected in final image formations. Thus, the infinite thin mask approximation will have larger deviation from real world process with the technology goes into 65nm node and beyond.

To describe the 3D mask effect exactly, Maxwell Electric-Magnetic filed equations should be adopted. However, to solve the Maxwell equations mathematically is obviously a horrible work, since the pattern on the mask can be extremely complicated. Fortunately, there are still a lot of algorithms through which numerical results of the Maxwell equations can be achieved. Here, we try to do calculation based on the Finite-difference time-domain method (FDTD), which is developed by K. S. Yee in 1966. And second-order approximation of Mur's absorbing boundary condition is used to enhance the convergence of the calculation. Some simulation results will be demonstrated, including how the profile (footing, undercutting and so on) of the mask affects final images formed on wafer level. And compare the results given by Kirchoff and FDTD approaches. Lastly, brief summary will also be given for the 3D Mask Effect in the image formation.

6520-177, Poster Session

CDU minimization at the 45-nm node and beyond: optical, resist, and process contributions to CD control

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As the industry transitions from to the 45 nm node and beyond, requirements for CD control are getting extremely aggressive. Current 45 nm node specifications call for 2 nm or better CD uniformity (CDU) on the gate level. For critical dimension control in this regime all measurable process effects must be closely monitored and controlled. This includes such effects as etch uniformity, scanner dose and focus consistency, PEB plate uniformity, and incoming wafer variation such as wafer warpage. The problem is that as the number of significant contributors to CDU continues to increase, while the number of parameters that can be used to control CDU has not.

To better understand how to achieve these increasingly stringent CDU targets the authors have explored the role of various optical, resist design, and resist processing effects CD control. The goal of this work is to simulate how process parameters such as dose and PEB temperature can be used to effectively control CD, while minimizing unintended negative effects on thru pitch CD performance, MEEF, and other lithography process metrics. In addition to these traditional lithography metrics, the effect these process changes on CDU is simulated using a Monte Carlo technique. Finally, the impact of resist design on the conclusions is explored and presented.

6520-179, Poster Session

ACLV performance dry versus immersion on 45-nm ground rules

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For CMOS logic, meeting ACLV specifications is crucial for delivering high performance semiconductor devices. Reducing the overall CD variation for gate layer by means of process optimization is therefore one of the most important tasks in process development. On wafer, it is very difficult to size various effects which contribute to ACLV. Variations in mask CD, exposure dose fluctuations, focus changes, lens aberrations, reflection and baking non-uniformities, will all contribute to the measured ACLV after the lithography step. The defocus contribution to ACLV is determined by the curvature of the Bossung plot as a function of defocus, paired with the focus control of the lithography scanner. One way of minimizing the defocus influence is by centering the process at isofocal conditions. This works well if only one pitch is considered. In reality, especially for silicon foundry processes, multiple pitches are required to define semiconductor circuits. With the usage of strong off-axis illumination modes at low k1 imaging, so called forbidden pitches emerge. For the forbidden pitches, the process window is limited by the extreme curvature of the Bossung plots, leading to off-spec dimensions already in slight defocus. The problem can be somewhat relieved by optimized scatter bar placement routines, but in general it can be expected that the CD control for the forbidden pitches is compromised.

With the advent of immersion tools, lithography enjoyed a sudden boost of the focus budget. Generally, the focus window on a water based immersion tool is 40-50% higher than on comparable dry tools, measured on the same features. However, interaction of the shower head with the wafer surface leads to overall reduced focus control over the wafer. As a result, the overall focus window gain is somewhat less than theoretically expected. There has been a lot of discussion whether the increased cost of ownership of immersion tools is justified by the reported performance gains. This paper compares ACLV wafer measurement results from a dry 0.93NA tool with results from a similarly configured 0.93NA immersion tool. We have defined special metrology structures that allow extensive data collection on our 45nm test chips. Comparing CD variations of features that are exposed at isofocal conditions with variations of forbidden pitch features allows sizing the contribution of defocus to ACLV. By comparing immersion and dry lithography side by side on the same mask set, and keeping process conditions otherwise exactly identical, the improvement of overall variation by using immersion is readily available.

6520-181, Poster Session

The feasible study of 45-nm metal patterning on 0.93 NA

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As semiconductor process technology moves to 65nm and beyond, RET (resolution enhancement technology) becomes more and more important. Especially on low k1 process, it is used frequently.

Currently, in 65nm generation, the k1 is ~0.4 on 0.85 NA exposure tool. However, the NA improvement of exposure tool cannot meet the schedule of generation movement very well. Low k1 technology must

be applied on next generation study. For 45nm generation, 0.93 NA exposure tool is available currently and is used to achieve the production criteria. The k1 value is quite low (~0.31), using traditional methods cannot satisfy process requirements.

For metal layer of 45nm generation, 55nm photo-resist CD (critical dimension) patterning of 130nm pitch is difficult goal on 0.93 NA exposure tool. Traditional OAI (off-axis-illumination) (annular mode) cannot provide enough image contrast for pattern printing. Customization illumination mode is an approach on low k1 process. Another one is utilizing light source polarization to achieve resolution improvement. In this paper, we will introduce different approaches on 45nm metal patterning. The RET approach (C-quad. Illumination mode with polarization) can provide enough image contrast on pattern printing to solve process issues.

6520-182, Poster Session

Optimization of DUV lithography for high-energy well implantation

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Presented here is an analysis of resist profile and CD control performance for high-energy well implant lithography as it is implemented in microelectronic devices, including SRAMs, at the 45 and 65nm nodes. As device designs become increasingly smaller to the tune of Moore's Law, deep well implant lithography specifications become more and more stringent, and issues that were trivial for older designs begin to make dominant contributions to CD uniformity and implant profile control. Sharp, ~90 degree sidewall angles, limited resist footing at the resist-substrate interface, and assessing true CD uniformity are key to ensuring desired high-energy ion implantation profiles and controlling device leakage and well counter-doping mechanisms.

First, the behavior and optimization of high-aspect ratio resist features near the well-STI interface will be explored. Due to differences in the substrate, such as material depth and reflectivity, resist edge profiles behave differently when they land on silicon as opposed to shallow trench isolation (STI). CD correlations between control structures on regions of solid silicon substrate and regions of solid STI substrate will be analyzed and related to actual resist profile performance and the silicon-STI interface for lines and spaces at different pitches. These correlations along with NanoSEM, and cross-section CD measurements and profiles of other 1 and 2-dimensional structures will provide insight as too how much combined process window is actually achievable for a given menu of feature designs. Furthermore, this data will be correlated to SRAM electrical leakage performance to yield a true relationship between resist edge profile, implant profile, and electrical performance.

Finally, feature linewidth and overlay metrology performance contributions to specified edge placement error will be assessed based on the aforementioned resist edge profile behavior, as well as an accurate model of the implant profile into the silicon substrate. As the resist feature CD decreases with respect to the resist feature height (thickness), scanning electron microscopy (SEM) measurement algorithm optimization, SEM control feature optimization, and cross-section SEM calibration play an increasingly important role in determining true CD uniformity, as well as determining the size and profile of the resist mask opening that the implant will penetrate. SIMS analysis at the substrate will be used to determine profiles and contributions of: ion scattering due to the high aspect ratio resist, resist foot encroachment over the active area, and implant angle as it relates to well-derived device electrical leakage performance. Furthermore, relatively small pattern overlay errors in the deep wells can cause very significant changes in leakage performance. The electrical effects in terms of leakage of introduced overlay errors in isolation macros will be quantified in order to reflect a more accurate interpretation of the true overlay specifications needed for a given edge placement error budget.

6520-183, Poster Session

Challenges and solutions for transferring a 248-nm process to 365-nm imaging

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In order to minimize manufacturing costs, lithographers have to extend capabilities of KrF and i-line tools working with low k1 factor. In this paper we present results of a successful transfer of a 210 nm lithographic process from KrF to i-line (k1 = 0.37).

During the process transfer the optimal conditions for 365-nm technology were first determined by simulation and then verified by exposure of real production layers on 0.65 NA i-line tool. The goal of the process optimization was to find settings for 365-nm process, which can match the performance of 248-nm process. Proximity matching, CD uniformity, tool throughput and process costs were chosen as the main criteria for successful transfer.

Encountered challenges, the applied methodology and the experimental results have been discussed. Based on the results, we conclude that low k1 i-line lithography is feasible for mass production with CD as small as 210 nm. The process does not require additional preparation for 248-nm masks.

6520-184, Poster Session

New color alignment for CMOS image sensor

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A new alignment mark implementation for Color processing has been successfully tested in a joint activity between ASML and TOWER. Alignability and overlay performance have been proven by application of the combination of a pure high order mark design and a dual implementation using the ATHENA alignment sensor and a PAS5500 / 400 machine.

Color layers are known to strongly absorb alignment light. The pure high order mark design enhances the signal strength. Exposing 2 of such mark pairs in Metal Last layer with 2 different metal plateaus - in previous metal layers: "Metal Last - 2" and "Metal Last -3" - leads to 2 different optical mark depths and therefore mimics a 4 wavelength alignment system. In principle, the evaluated technique might be extended to more (than 4) "wavelengths" as well as other process layers. Moreover, the use of scribe-line marks optimize productivity since no extra lithography step is required to expose Zero Layers. The performance of this implementation has been evaluated for 180-nm CMOS Image Sensor technology.

This paper discusses the overlay and alignment results of the evaluation. Alignment parameters such as absolute signal strength and signal strength variation were studied in detail. It is shown that such mark implementation shows good alignability and easily meets the product overlay Image Sensor requirements.

6520-185, Poster Session

A thin FinFET Si-fin body structure fabricated with 193-nm scanner photolithography

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A thin FinFET Si-fin body structure has been successfully fabricated upon the bulk-Si wafer through using 193nm scanner lithography and a composite hard mask etching technique. First, a 100?thick buffer SiO2 layer was thermally grown upon the bulk silicon layer and subsequently a 1200?thick SiNx layer and a 1000 ?thick TEOS SiO2 hard mask layer was chemically vapor deposited to form a composite hard mask structure of buffer-SiO2/SiNx/SiO2. Second, both 1050?thick BARC and 2650?thick photoresist were coated and a 193nm scanner lithography tool was used for the Si-fin body layout patterning under

relatively high exposure energy. This achieves ADI (after develop inspection) of 80nm from the original as-drawn Si-fin layout of 110nm. Then, a deep sub-micron plasma etcher was used for an aggressive photoresist (P/R) and BARC trimming down processing and both the capping CVD-SiO2 and CVD-SiNx with its underlying buffer oxide layers were subsequently etched in other etching plasma chambers, respectively. Resultantly, the AMI (after mask inspection) can reach 60nm. Continuously, both the P/R and BARC were removed with a nominal plasma ashing as well as a RCA cleaning for the subsequent sub-micron Si-fin plasma etching. Finally, a 60nm-thin and 400nm-height Si-fin body structure, as shown in Fig. 1, can be successfully etched out through a fixed time-mode silicon plasma etching.

6520-186, Poster Session

ARC stack development for hyper-NA imaging

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The merits of hyper NA imaging using 193 nm exposure wavelength with water immersion for 45 nm and 32 nm nodes is clear. However, the challenge remains CD control at hyper NA and the development of ARC stacks to support not only lithographic response but also device integrations. Extreme off-axis illumination, polarization, and dense pitches of the C045 and C032 nodes show a significant degradation of reflection and CD control and a significant loss of resolution. Consequently, hyper NA patterning requires the development of a new ARC to improve the overall CD control. Thus, a single ARC layer could not ensure the reflectivity condition, and ARC stacks must now be decomposed into two or three components in order to suppress reflectivity through a wide range of incidence angle.

In a previous work, we presented the advantage of using an antireflective based on CVD organic - inorganic stacks . This paper presents an upgrade of this type of stack, applied to 1.2NA imaging. We will show stack reflectivity simulations based on S-matrix approach. The capabilities of the CVD tools have been taken into account in the simulations in order to define a reflectivity process window. We will present 1.2NA lithography with different optimized ARC stacks, comparing potential capability and CD control in conjunction with the immersion lithography for 45 nm and 32 nm nodes.

6520-187, Poster Session

A thick CESL stressed ultra-small (Lg=40nm) SiGe-channel MOSFET fabricated with 193-nm scanner lithography and TEOS hard mask etching

W. Liao, United Microelectronics Corp. (Taiwan)

A 100Å-thick SiGe (22.5%) channel MOSFET with gate length down to 40nm has been successfully integrated with 14Å nitrided gate oxide as well as a 1200Å high-compressive PECVD ILD-SiNx stressing layer as the contact etching stop layer (CESL) that enhances the PMOS electron mobility with +33% current gain. To achieve a poly-Si gate length target of 400A (40nm), as shown in Fig. 1, a 193nm scanner lithography and an aggressive oxide hard mask etching techniques were used. First, a 500Å-thick TEOS hard mask layer was deposited upon the 1500 Å-thick poly-Si gate electrode. Second, both 1050Å-thick BARC and 2650Å-thick photoresist (P/R) were coated and a 193nm scanner lithography tool was used for the Si-fin layout patterning with nominal logic 90nm exposure energy. Then, a deep sub-micron plasma etcher was used for an aggressive P/R and BARC trimming down processing and the TEOS hard mask was subsequently plasma etched in another etching chamber without breaking the plasma etcher¡õs loadlock vacuum. Continuously, the P/R and BARC were removed with a plasma ashing as well as a RCA cleaning. Moreover, the patterned Si-fin capping oxide can be further trimmed down with a diluted HF(aq) solution (DHF) while rendering the RCA cleaning process and the remained TEOS hard mask is still thick enough for the subsequent poly-Si gate main etching. Finally, an ultra narrow poly-Si gate length of 40nm with promising PMOS drive current enhancement (+33%) can be formed through a second poly-Si etching, which is above the underneath SiGe (22.5%) channel and upper 14Å-thick nitrided gate oxide.

6520-188, Poster Session

Three-dimensional mask effects and source polarization impact on OPC model accuracy and process window

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As semiconductor technology moves toward and beyond the 65 nm lithography node, the importance of Optical Proximity Correction (OPC) models grows due to the lithographer's need to ensure high fidelity in the mask-to-silicon transfer. This, in turn, causes OPC model complexity to increase as NA increases and minimum feature size on the mask decreases. Subtle effects, that were considered insignificant, can no longer be ignored. Three dimensional mask effects, induced by a given imaging process, become important OPC modeling parameters. Theses parameters can be used to improve model accuracy and the final process window.

In this paper, the effects of 3D mask topology on process window are studied using several 45 nm node mask structure types. Simulations are conducted with and without a polarized illumination source. The benefits of using an advanced model algorithm, that comprehends 3D mask effects, will be discussed, and OPC processing run-time will be addressed. To quantify the potential impact of this methodology, relative to current best known practices, all results are compared to those obtained from a model using a conventional thin film mask.

6520-189, Poster Session

The choice of mask in consideration of polarization effects at high-NA system

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Strong resolution enhancement techniques (RETs) are highly demanded to overcome the resolution limit of sub-60nm lithography. ArF immersion lithography may be the best candidate for sub-60nm device patterning. However, the polarization effect becomes more prominent to degrade the image quality in high NA immersion lithography as the feature size shrinks.

Therefore, it is important to understand the polarization effect in the mask. The induced polarization effect shows the different aspects between the binary and the attenuated phase shift mask (PSM).

In this paper, we considered the effects of polarization state as a function of mask properties. The aerial image depends on the polarization states induced by the mask properties such as materials, thickness, and duty ratios. We evaluated the performances of the binary mask and the attenuated PSM by using simulation, AIMS (Aerial Image Measurement System) tool, and real wafer printing.

We find out that there are no differences between the binary mask and the attenuated PSM in view of image contrast [figure1] and mask error enhancement factor (MEEF) [figure2]. These show that the effect of mask induced polarization is greater than that of interference for phase shifting.

We also consider the haze issue that is also emphasized in ArF lithography. Recently, haze growth in the attenuated PSM seems to override the benefit of resolution enhancement in the ArF lithography.

This paper will describe the details for choosing the binary mask as a appropriate mask for sub-60nm imaging due to it's competitive performance and haze-free environment.

6520-190, Poster Session

Analysis of diffraction orders including mask topography effects for OPC optimization

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In recent years, model-based OPC has been an essential technique. It employs optical simulation and current OPC software has supported thin-mask model or approximated model. For 45nm-node and beyond, it can be seen the simulation results difference between 2D simulation by calculating thin-mask model and 3D rigorous simulation by calculating thick-mask model such as FDTD or RCWA. Especially, it is expected that larger incident angle of off-axis illumination and higher aspect ratio of mask topography can lead more large differences between them. On the other hand, thick-mask model consumes much computation so that it will not be practical.

The difference of these two simulation models is thought that caused from the effect of mask topography and calculation of electromagnetic field on 3D rigorous simulation. The difference also creates the difference of diffraction amplitude and phase. We focused on such diffraction orders with thin and thick-mask model and it has been evaluated.

In this paper, the difference of diffraction orders' amplitude and phase between two simulation models caused by illumination angle, mask materials, thickness or cross-sectional shape is analyzed and then the difference of OPC bias for various pattern pitches is evaluated. From this result, we will also discuss about the compensation methodology of the diffraction differences. Assistance of simple OPC to improve the accuracy which is done prior to thin-mask model's OPC is tried to evaluate.

6520-191, Poster Session

Immersion lithography with numerical apertures above 2.0 using high-index optical materials

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The progress of optical lithography has approached the sub-30 nm regime with 193nm laser as the illumination source. To increase the numerical aperture (NA) further, many issues, especially those related to materials, need to be addressed. In this paper, we present the analytical and experimental results of two-beam interferometric lithography with sapphire (Al2O3) and lutetium aluminum garnet (Lu3Al5O12 or LuAG) as the optical materials. At 193nm, the index of sapphire is 1.92 and LuAG is 2.14 while the typical index of a typical photoresist is 1.7. The classical theory predicts that once the incident angle is greater than the critical angle, boundary waves will be formed and no energy can be carried into the second medium by the wave. However, with our analysis and the experimental results, we show that due to the absorbance of the resist, boundary waves will not be formed and the photoresist can be exposed even when the incident angle is greater than the critical angle. Using the interferometric imaging, an NA of up to 2.1 is enabled, which corresponds to 23nm half pitch. Since both sapphire and LuAG are a crystalline materials, the intrinsic-birefringence results in depolarization effect, which will be analyzed in this as well.

6520-193, Poster Session

Immersion defect reduction, part I: analysis of water leaks in an immersion scanner

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Immersion hood is one of the important components that differentiate the immersion scanner and its dry counterpart. It is used for supplying, confining, and draining the liquid coupling medium during exposure. On the other hand, it is also a dominant defect source generating directly or indirectly the major parts of the immersion-specific defects. Particles composed of metal elements were easily observed if the manufacturing process of immersion hood was not well controlled. Polymer residues also possibly aggregate in the immersion hood and washed back to wafer surface during exposure. Moreover, the immersion hood itself can leak water and cause defects if the water contains particulates.

This paper reports two different modes of water-leakage analysis. The first part involved static exposures. By accumulating the wafer defect maps, the circular defect trajectories clearly indicated the problematic parts in the immersion hood, which may need further cleaning (see figure 1). The second part of this paper deals with the dynamical water-leakage mode. Water may leak during exposure according to the wafer-surface properties, exposure sequence, and immersion hood design. Figure 2 shows the accumulated wafer defect map fitted by the dynamical water-leakage model. By analyzing this type of maps, the weak points of hood design and the effects of wafer-surface property are understood.

6520-194, Poster Session

Defect testing using an immersion exposure system to apply immediate pre-exposure and post-exposure water soaks

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The rapid expansion in the number of semiconductor manufactures using immersion imaging systems confirms the acceptance of immersion lithography for critical layer imaging. One of the early concerns in the development of immersion lithography was defect levels. These defects levels have been dramatically reduced with each new system, and are now approaching defect levels similar to dry imaging systems. Continued reduction of defects will be required as smaller critical dimensions are pursued on immersion systems with NAs well over one. We have studied new ways to further reduce the number of defects. For this investigation an ASML 1150i alpha-immersion scanner was used for both ultra pure water soaking and for image exposure. Previous pre-exposure and post-exposure rinse/soak tests have been conducted on coater/developer tracks; however using the track causes a significant delay from soak to exposure, and vice-versa. For this experimentation a dynamic soak of coated wafers immediately before exposure and immediately after exposure was performed on the immersion scanner with soak times controlled by multiple test routings. The wafers were then processed as normal on a TEL-Lithius coater/developer track. To determine the interactions which reduced defects, defect density and location with respect to defect type and size were analyzed for each immersion scanner pre-exposure and post-exposure soak condition. Initial findings show combinations of pre and post soak reduce certain immersion type defects, along with typical particle defects

6520-195, Poster Session

Characteristics of state-of-art lithography optics represented using the first canonical coordinate of lie group

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The rapid development of integrated circuits has been enabled by extraordinary advances in optical microlithographic systems. The state-of-art of commercial lithography is done with exposure, employing immersion optics and using a laser light source whose wavelength is 193 nm. The wavefront distortion of its projection optics is as low as 1 nm rms. In order to print a line-and-space pattern of 50 nm, the numerical aperture (NA) of the projection lens has been increased to more than 1 by using immersion optics.

Due to the high lens NA, the high incident angle in resist induces vectorial imaging effects, which require polarization control of the projecting light for optimization of the contrast of images. As a result, the conventional scalar representation of the wavefront of the projection optics has to be replaced by vectorial representation, which includes polarization transformation operators.

Polarization analysis of optical systems called polarization aberration was intensively studied by Chipman, completeness of who's representation using Jones matrix is sufficiently high.

There are several proposals of polarization representations of the projection optics. However, the simple Jones representation, although

easy to calculate, is not easy to understand. And the basis matrices are not representative of practical or physical polarization transformations. Polarization states described as eigenvectors of Pauli matrix exactly coincide with the Stokes vectors, however, a single Pauli matrix and one real parameter cannot represent the polarization matrices whose eigenvectors are Stokes vectors. For this reason, considering optical phenomena, Pauli matrices are not suitable as the basis of Jones matrices.

Group theory is a strong tool in physics. Several attempts had been made to understand polarization using group theory. However, their concern is in Jones space, not in generator space. Because the projection optics for microlithography are nearly ideal, a linear sum of the infinitesimal polarization matrices becomes a good approximation. As a result, the first canonical coordinate in Lie group, which is especially important in group theory in physics, is suitable to represent the state of polarization transformation of the projection optics.

In this presentation, we demonstrate a new physically comprehensible polarization representation of projection optics for microlithography, which has eight real parameters on the first canonical coordinate of a Lie group describing individual real optical characteristics and is suitable for conventional pupil representation using Zernike polynomials. Eight matrices for the eight real parameters are not Jones matrices but generators of Jones matrices i.e. Lie ring.

6520-196, Poster Session

Characteristics analysis of polarization module on optical proximity effect

C. Park, Hynix Semiconductor Inc. (South Korea)

In hyper NA system, specific illumination combined with polarization can be used as one of major RET techniques. Polarization at high NA dry system is also regarded as important technology to bring improvement of very low k1 process. The benefits of polarization on repeated structure are very well known. However we also need to understand the effect on random pattern in peripheral region to adopt polarization technology successfully into real devices. Memory device such as DRAM and NAND Flash has repeated cell structure and also loose pattern in peripheral region. In this study two kinds of polarization function will be applied to real memory devices and the polarization behavior on various patterns in peripheral circuit will be analyzed through actual printing process using 6% attenuated PSM at ArF high NA dry system. The printed result will be compared on random patterns through in-line metrology tool and process guideline including OPC treatment will be discussed based on this study, especially with regard to ID bias.

Conference 6521: Design for Manufacturability through Design-Process Integration

Conv. Ctr. A2

Wednesday-Friday 28 February-2 March 2007

Part of Proceedings of SPIE Vol. 6521 Design for Manufacturability through Design-Process Integration

6521-22, Session 7

Model-based assist feature generation

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We optimize a continuous-tone photomask to meet a set of edge-placement tolerances for a set of dose and defocus values. The optimization has both edge-based and image-based goals. Meeting the image-based goals ensures that side-lobes and assist features will not print through the process window. This algorithm derives assist features from first principles: when the mask is optimized for best focus, the optimal continuous-tone photomask does not have any features that resemble assist features. When the mask is optimized for best focus and a defocus condition, the optimal continuous-tone photomask spontaneously grows assist features. The continuous-tone photomask also has features that can be identified as phase windows. Polygonal, quantized assist features are extracted from the optimal continuous-tone photomask. The model-based assist features which are thus derived are subsequently optimized for position of edges of the main features and assist features to create a mask-writing-friendly output.

6521-23, Session 7

Three-dimensional mask effect approximate modeling for sub-50-nm node device OPC

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In order to perform an optical proximity correction of memory device nodes below half-pitch 50nm, so called 3D mask effects need to be accounted for. As the mask pitch approaches ArF wavelength and the angle of off-axis illumination becomes increasingly greater than normal incident beam, combined effects of transmission loss and mask induced polarization induces deviations from thin mask Kirchhoff approximation. Presently, a couple of methods are being developed for commercial use: edge domain decomposition method (DDM) and rim-type boundary layer. However, these methods currently require extensive modeling and correction time. In this work, some results on an alternative approach to 3D mask modeling that is suitable for OPC are presented. Using sub-50nm node test pattern experimental data and FDTD rigorous simulation results, a thin mask approximation and alternative 3D mask approximate approach is compared. The results indicate improved model accuracy in terms of root mean square of 13% and 50% for a cross-pole and a dipole illumination conditions, respectively, while the OPC run-time remained similar. Furthermore, a gate-poly OPC result using the 3D mask approximate model indicates improved correlation to experimental results than a thin mask model at minimum resolution dense feature and narrow space regions (Fig. 1).

Thin mask and OPC 3D mask models were calibrated for three differing illumination conditions: x-dipole quasar illuminations with y-polarization and cross-pole quasar illumination with x-&y-polarization states. For each of the extreme off-axis illumination conditions, 3D mask approximate model developed for OPC indicated better calibration to both test pattern wafer images and rigorous simulation results (Table 1). In addition, OPCed contours of 3D mask approximate model correlated better to wafer image than the thin mask approximation.

6521-01, Session 1

Collaborative platform for DFM

A. R. Neureuther, Univ. of California/Berkeley

No abstract available

6521-02, Session 1

TBD

No abstract available

6521-03, Session 2

Lithography simulation in DfM: achievable accuracy versus requirements

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Lithography simulation remains one of the primary aspects of most DfM flows and various approaches have been taken to find the optimum balance of accuracy, speed, ease-of-use, IP protection and extendibility. In this paper we examine the factors impacting simulation accuracy of various DfM approaches. Sparse and dense simulations are compared, including various model forms associated with each. Differences between detailed simulation, which includes full RET and OPC treatment, and the use of compact models are explored. Simulation results are compared to wafer contours collected at varying process conditions. DfM accuracy over time and across multiple fabs is examined and used as a guide to determine achievable accuracy.

6521-05, Session 2

Structural failure prediction using simplified lithography simulation models

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Ain't no doubt about it: OPC verification via full-chip lithography simulation has already become an integral part of the sign-off flow for technologies at 65nm half-pitch and below. Spawned by start-up companies introducing innovative approaches, a veritable battle for the best tool (and, of course, the largest market share) is currently raging between several EDA vendors. From a user's point of view, the accompanying mutual insemination with good ideas is more than welcome and the maturity and capability the tools have reached meanwhile is indeed quite astonishing.

However, when using full-chip lithography simulation to identify locations with an increased risk of structural failure (i.e., pinching or bridging), the first question one has to answer is: What's the right model to use [1]? The crux here is that full-blown advanced empirical models - calibrated from wafer data for correct prediction of CD (and used, e.g., for OPC) - only contain process input about printing structures, but not from structural failures. In that sense, they have to extrapolate when being used for pinching or bridging detection, such that predictions always have to be taken with a grain of salt. Exactly this dilemma is addressed by the "critical failure ORC" (CF-ORC) approach championed by Mentor Graphics [2]. It introduces a special "CF model" for the boundary between printing and failing structures, explicitly considering the information which structures are failing to print well. The downside of this even more empirical model on a yet higher abstraction level is its increased likeliness to fail outside of the aerial image parameter space used for calibration. Furthermore, being rooted in Mentor Graphic's "sparse simulation" world with edge fragments and simulation sites, the CF-ORC approach has all the corresponding disadvantages.

In this paper, we present as an alternative a systematic method (a) to build a simple, sturdy constant threshold (CTR) model that is valid over the required process window and (b) to determine criteria for structural failure detection. Even though a CTR model is not capable of accurately predicting the CD, it captures trends of the printing behavior very well,

even in the failure regime. From wafer data such as used for OPC model building, it is straightforward to find out which structures are not resolved well with a given process. Combined with the CTR model simulation results for these structures, this can be used to determine a single threshold value for the separation of simulation contours that indicates structural failure. The predictive power of this approach has already been verified on H/W and is used in production.

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6521-06, Session 2

Unified process aware system for circuit layout verification

A. Torres, F. G. Pikus, Mentor Graphics Corp.

Several cornerstones of electronic design are being questioned with new process technologies: Placement independence is no longer guaranteed, which means that cell characterization now has to consider a multitude of cell placements. OPC is limited in its ability to restore exactly the intended layout shapes during manufacturing (due to process variations), thus creating strains in current device and interconnect extraction approaches. Each processing step (i.e. litho, etch, CMP) and each failure mechanism (i.e. interconnect stress, particles, resist collapse) can in principle suggest competing layout configurations that are not compatible with each other.

Finding a global or even local optimal solution has been debated and several papers [1] suggesting regular fabrics or restrictive design rules as the means to overcome process and design limitations. While such approaches are slowly being adopted in new technologies they are not necessarily applicable in some instances, especially legacy IP. Regular design methodologies such as grid-aligned layouts may provide better control of yield-limiting layout features but do not guarantee the most compact design since these methodologies exacts area penalty across of the chip, whether a particular location has litho-related yield problems or not. In addition grids are governed by rules which are designed for one balance of trade-offs between competing yield-limiting factors and cannot dynamically adapt to changes in the manufacturing process.

In addition, one of the biggest challenges has been the definition of a single design quality metric which is able to describe how a given region in the layout will be susceptible to a the manufacturing process. Historically, critical area analysis [2] has been sufficient to evaluate the possible yield of a design, but as the relative importance of systematic mechanisms increases [3], this purely statistical approach needs to be enhanced by incorporating additional process information.

In this paper we describe a consolidated metric and the system that can analyze multiple process conditions and different configurations to arrive to an optimal solution. This solution is based on a cost function which depends on the characteristics of the manufacturing process. A general form of the cost function and the parameters defining individual process impacts are discussed and to demonstrate the system, different layout configurations are analyzed considering litho process variations, particle distributions and recommended design rules. Since all layout configurations represent the same electrical devices, it is possible to dynamically determine the most robust layout implementation according to the cost function which incorporates the current relative importance of each yield loss contributor.

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6521-07, Session 2

Double patterning design split implementation and validation for the 32-nm node

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Exposure systems for the 32nm node may not be ready in time for production. At the available NA of 1.35, one option to generate the required dense pitches is double patterning. Here a design is printed with two separate exposures and etch steps to increase the pitch. If a 2x increase in pitch can be achieved through the design split, double patterning could thus theoretically allow using exposure systems conceived for the 65nm node to print 32nm node designs.

In this paper we focus on the aspect of design splitting and lithography for double patterning the poly layer of 32nm logic cells using Synopsys full-chip physical verification and OPC conversion platforms. All 32nm node cells have been split in an automated fashion to target four different aggressiveness towards pitch reduction and polygon cutting. Every design split have gone through lithography optimization, optical proximity correction (OPC) and lithography rule checking (LRC) at NA's of 0.93, 1.20, and 1.35. Final comparisons are based on simulations across the process window. In addition, we have experimentally verified selected single-patterning problem areas on a 1.20 NA exposure tool (ASML XT:1700Fi at IMEC). With this information, we establish guidelines for double patterning conversions and present a new design rule for double patterning compliance checking applicable to full-chip scale.

6521-08, Session 2

DRC Plus: augmenting standard DRC with pattern matching on 2D geometries

V. Dai, J. Yang, L. Capodieci, N. P. Rodriguez, Advanced Micro Devices, Inc.

Design rule constraints (DRC) are the industry workhorse for constraining design to ensure both physical and electrical manufacturability. However, as technology process continues to shrink and aggressive RET and OPC is applied, standard DRC sometimes fails to fully capture the concept of design manufacturability. Consequently, some DRC-clean layout designs are found to be difficult to manufacture. Attempts have been made to "patch up" standard DRC with additional rules to identify these specific problematic cases. However, due to the lack of specificity with DRC, these efforts often meet with mixed-success. Although it typically resolves the issue at hand, quite often, it is the enforcement of some DRC rule that causes other problematic geometries to be generated, as designers attempt to meet all the constraints given to them. In effect, designers meet the letter of the law, as defined by the DRC implementation code, without understanding the "spirit of the rule". This leads to more exceptional cases being added to the DRC manual, further increasing its complexity.

DRC Plus adopts a different approach. It augments standard DRC by applying fast 2D pattern matching to design layout to identify problematic 2D configurations which are difficult to manufacture. The tool then returns specific feedback to designers on how to resolve these issues. This basic approach offers several advantages over other DFM techniques: It is enforceable, it offers a simple pass/no-pass criterion, it is simple to document as part of the design manual, it does not require compute intensive simulations, and it does not require highly-accurate lithographic models that may not be available during design. These advantages allow DRC Plus to be inserted early in the design flow, and enforced in conjunction with standard DRC. This paper describes the basic concept of DRC Plus, its implementation within the design flow, and experimental results which demonstrate its efficacy.

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6521-09, Session 3

Process window aware layout optimization using hot spot fixing system

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The feasibility of Hot-Spot Fixing system (HSF) in DfM flow are studied and disclosed. Hot spot clearance using process simulation is indispensable under low-k1 lithography process for logic devices with advanced design-rule (DR). Hot spot such as pinching, bridging, line-end shortening will occur, mainly depending on local pattern context. Proper calibration of DR, mask data preparation (MDP), resolution enhancement technique (RET) and optical proximity effect correction (OPC) will reduce potential hot spot. However pattern layout variety is so enormous that, even with most careful calibration of every process, unexpected potential hot spot is occasionally left in the design layout 1-2. OPC optimization is useful to maximize common process margin, but it can not expand individual process margin without modification of design layout.

So, in early design stage, hot-spot extraction using lithography compliance check (LCC) and manual modification of design at hot spot will be simple and useful method. The problem is that, it is difficult to determine how to modify layout to be consistent with DR, MDP/OPC rule. For proper layout modification, intimate knowledge of whole process would be necessary, and even more, the modification work often needs to be iterative. Therefore, using our automated HSF system in cell design stage and also chip design stage is helpful to fix design layout avoiding fatal hot spot occurrence, with enough process margin and also with short turn around time (TAT) 3-4.

The basic system flow in the developed system is as follows;

LCC extract potential hot-spots, and the hot spots are categorized by lithography error mode, magnitude, and surrounding context. And then, hot-spot modification instructor, taking surrounding situation into consideration, generates modification guide for the every hot spot. Design data is automatically modified according to the instruction at every hot spot, complying with the design rule. The design modification process is verified with DRC and process simulation to confirm hot-spot elimination without side effect.

The performance of the provided HSF system has been studied about process margin expansion in several small layouts using process simulation. And more, feasibility of the system has been verified applying for full chip data hot-spot cleaning. Local metal layer in 65nm node device, with size of 10mm square and with hot spot number of 47 thousands, modified in 12 hours and the number of hot spots is reduced to about 40.

In this work, considering necessary depth of focus (DOF) and exposure latitude (EL), hot-spot clearance was checked under prescribed condition of defocus and under/over dose, and consequently, with this method, the optimized layout proved to have required DOF and EL. we extend target layers to multiple critical layers including active area, poly, and metal in various logic devices of 65 nm node. The feasibility of this system for each layout is proved on points of process margin expansion, hot-spot fixing rate, and TAT. Especially, the significant effects of process margin expansion are observed experimentally using SEM wafer image and process simulation. The detailed result will be shown in the paper.

6521-10, Session 3

Automated full-chip hotspot detection and removal flow for interconnect layers of cell-based designs

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An automated flow has been implemented for litho/etch model based hotspot detection and auto-fixing during final routing optimization. A widening manufacturing gap has lead to a dramatic increase in design rules that are either too restrictive or do not guarantee a litho/etch hotspot-free design. Since the semiconductor industry is currently limited to 193nm scanners, no relief is expected from the equipment side and must come from the design side. Rule driven routers fail to capture hotspots as they are based on ideal polygons that do not represent the real silicon image. Model-based hotspot detection can validate design manufacturability and will account for complex 2D effects that stem from aggressive scaling of 193nm lithography.

To enable this solution, manufacturing teams started to release model-based lithography checks; first as a service using the manufacturing flow to check small cells and now by releasing process information to designers for full-chip lithography hotspot detection. However, if manual fix is manageable at the cell level, hotspot removal in large place and routed blocks or even full chip is more challenging. Not only is full-chip litho/etch simulation required to have a reasonable runtime, but the fixing solution needs to be connectivity-aware and incremental with a very fine step size. This is required for a timing aware solution that mitigates hotspots without adversely affecting timing closure.

An automated flow has been developed, as shown in Figure 1, by linking a hotspot detection solution and a chip routing optimization tool. The hotspot detection solution passes to the chip routing optimization tool the hotspot locations and associated fixing guidelines. The chip routing optimization tool removes the hotspots in an incremental fashion as to have no significant impact on timing, but a significant impact on printability (Figure 2). This process of checking for hotspots and incrementally fixing them is iterated until a hotspot-free design is achieved.This paper describes how fabless designers have integrated hotspot detection solution in their design flow and how the hotspot removal flow efficiently removed most hotspots in real designs providing a DFM closure.

6521-11, Session 3

Model-assisted routing for improved lithography robustness

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A correct-by-construction model-assisted routing technique for improving lithography robustness of synthesized layouts is presented. Presupposing an accurate lithography model and a model-based layout weak spot identification procedure, this four-step model produces routed layouts in-situ with acceptable turn-around impact.

The approach starts with a conventionally-routed layout that, although conforming to design rules, may contain undesirable layout configurations that the router can reconcile. Since weak spot identification is computation intensive, rule-based filtering is first applied to the incoming layout to select regions for further model-based analysis. Such filtering is conservative; the selected regions, or potential weak spots, encompass all problematic patterns. To be efficient, however, the superfluous regions should be minimal.

Before deciding which of the selected regions are actual weak spots, the router performs a nondiscriminate correction to reduce the potential number of weak spots. This reduced set subsequently undergoes model-based weak spot analysis, distinguishing the actual weak spots. The router finally optimizes the layout to remove the identified weak spot.

6521-12, Session 3

Model-based approach for physical design verification and design/manufacturability co-optimization

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Model-based hotspot detection and silicon-aware parametric analysis helps designers optimize their products for yield, area, and performance without the high cost of DFM/recommended design rules. This exponentially growing set of DFM/recommended rules is primarily litho driven and in principal, being a function in 2D space trying to communicate a frequency space dilemma, can no longer guarantee a manufacturable design without overly restricting designers. Hence the methodology of making design decision based on idealized polygons that no longer represent what is on silicon needs to be replaced. Using model-based simulation of the lithography, OPC, RET and etch effects and subsequent electrical evaluation of the resulting shapes leads to a

more realistic and accurate analysis that can then be used for intelligent design tradeoffs.

The new DFM design methodology consists of three parts; relaxing litho related recommended design rules to attain a more aggressive design, using a model based Layout Printability Check to identify and fix hotspots, and a process-aware parametric analysis tool for silicon-aware transistor and interconnect analysis. DFM/recommended design rules are intentionally relaxed to offer the ability to have more aggressive cell designs that yield about a 10% - 15% density improvement (Figure 1). Model based litho and etch simulation is done at the cell level to identify hotspots that need to be fixed. Naturally some of the recommended rule violations lead to a higher amount of hotspots, but some layouts with recommended rule violations still passed without any hotspots. Full-chip analysis is employed to fix residual hotspots on interconnect layers, on poly or metal 1 due to interaction between adjacent cells, or on metal 1 due to interaction between routing (via and via cover) and cell geometry. Fixing hotspots was relatively straight forward as generally there was enough space for a simple fix that did not generate new hotspots. Finally, contours of diffusion, poly and metal were used for silicon aware parametric analysis of transistors and interconnect. This is a critical improvement to the previous generic transistor model approach that had to be as pessimistic as the worst printing transistors in the layout. Detailed transistor and net specific information helped avoid process-sensitive layouts, reduce quantity and magnitude of SPICE corners, and lead to more accurate timing closure. Bringing litho and etch modeling to the design flow from the cell level to full-chip allowed designers the flexibility to be creative in their design without any significant delays, as all runs, including full-chip, were done in less than a day and showed a near linear scalability. Overall this approach has proven far more successful than dealing with an ambiguous set of recommended rules that are impossible to follow in entirety.

6521-13, Session 4

Context specific leakage and delay analysis of a 65-nm standard cell library for lithography induced variability

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A standard cell characterization study has been done to look at the influence of cell context when looking at cell delay and leakage at different exposure conditions. Cell context, or proximity effects from neighboring cells, can have a significant impact on cell performance across a process window, especially through focus, which needs to be considered for silicon aware circuit analysis. The traditional lookup table approach used in static timing analysis or leakage power analysis needs to be augmented with an instance specific offset for each cell in a design. Contours need to be generated for each transistor in each cell at different process points and the corresponding delay and leakage offsets should be calculated based on these contours. Electrical characterization also enables the use of other context specific process models such as strain and/or dopant fluctuations without altering the final output and hence any subsequent tools that would use the information for circuit analysis. Although this study was meant to quantify the significance of cell context through focus, this methodology could prove useful in future process-aware static timing and power analysis tools.

Chip layouts where randomly generated using a 759 cell 65nm standard cell library. Using model-based litho and etch simulation at different process conditions, contours were generated for the poly and active layers of each standard cell and the resulting transistor-level netlists were simulated for cell delay and leakage. All instances of the same cell were found to print identically and have the same delay and leakage values at nominal exposure conditions. The context specific discrepancy was calculated by finding the difference in delay or leakage at a particular defocus point among different instances of the same cell in a randomly generated layout. Under strong defocus conditions, simulation results show up to a 10% discrepancy in gate length, 15% discrepancy in delay, and a 200% discrepancy in leakage between different instances of the same cell, but with different neighbors (Figure 1). It is important to note that large gate length variation of one transistor did not directly translate to large leakage or delay variation for the entire cell. Also, comparing standard cells with traditional free-pitch design rules to restricted pitch design rules showed that restrictive design rules help reduce the variation from instance to instance of a given cell by as much as 40% at an area penalty of 10%. Nevertheless, context specific analysis shows significant differences in both cases.

6521-14, Session 4

Patterning effect and correlated electrical model of post-OPC MOSFET devices

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The accurate simulation of nowadays' devices requires accounting for real device geometry complexities after lithography or etching process. Especially when the channel length shrinks to 65 and 45 nanometers. Device performance is believed to be much worse than what designer expects from using the conventional IC design flow. The traditional design lacks consideration of the photolithography effects and pattern geometrical operations at manufacturing side. For the reason of obtaining more accurate prediction for circuits, an efficient approach to estimate nonrectangular MOSFET analytically is proposed. In addition, an electrical hotspot criterion is also proposed to inspect and verify the manufacturability of devices during patterning processes. This electrical rule criterion will be performed after the regular DRC or DFM checking. Photolithography and industrial-strength SPICE model are taken into consideration to further correlate the process variation with SPICE corners. As a result, the correlation between process-windows and driving current variation of devices will be discussed explicitly in this paper.

6521-15, Session 4

Coupling aware mixed dummy metal insertion for lithography

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As integrated circuits manufacturing technology is advancing into 65nm and 45nm nodes, extensive resolution enhancement techniques (RET) are needed to correctly manufacture a chip design. The widely used RET called off-axis illumination (OAI) introduces forbidden pitches which lead to very complex design rules. It has been observed that imposing uniformity on layout designs can substantially improve printability under OAI. In this paper, two types of assist features for metal layer are proposed to improve the uniformity. They bring different costs on performance and manufacturing. Coupling capacitance and lithography costs from these assist features are discussed. Optimal insertion algorithm is proposed to use both types of dummy metals, considering trade-offs on coupling capacitance and lithography costs.

For metal layers, uniformity used to be a design criterion for chemical mechanical polishing (CMP). Now it is also required by lithography for 65nm node and beyond. Uniformity can be achieved simply by inserting dummy metal wires with the same width as main features at all free spaces. Simulation results indeed show significant improvement in printability with such a dummy metal insertion approach. But these assist features are printable and hence increase coupling capacitances. Process variations have been a big issue during the design, making performance harder to predict and leading to lower yield. Excessive coupling capacitance from printable assist features (PAF) may bring more severe manufacturing problems.

The alternative is to use a set of CMP type assist features (CAF), which are segmentations of PAF dummies. With less neighboring metals printed, CAF can reduce coupling capacitances. However, using CAF also has its own costs. First, OPC is needed for CAF to achieve wanted shapes on the wafer. It brings additional cost for mask preparation and writing. Secondly, CAF cannot make features as uniform as PAF. Hence, the depth of focus (DOF) of main features is degraded. Overall, CAF brings a higher lithography cost, which includes mask cost and RET/process expense. The lithography cost from CAF is related to the size

and spacing of segmentations. Extensive simulations are performed to find the optimal CAF configuration. Offsets for CAF in different columns are also considered.

In this paper, we also propose a novel dummy metal insertion method to achieve the uniformity for the lithography. An optimal algorithm is proposed to determine the mixed dummy metal insertion efficiently. Our main contributions include:

1. This is the first work to discuss CMP type dummy metal on lithographic effects.

2. A novel insertion scheme is proposed using both PAF and CAF as dummies. The trade-off between lithography cost and coupling capacitance are considered.

3. An optimal algorithm is proposed to solve the coupling-aware dummy insertion problem that can minimize lithography cost subject to any given coupling capacitance bound.

6521-16, Session 4

Prediction of interconnect delay variations using pattern matching

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Maximum lateral impact functions and netlist tracking software are being developed in a prototype fast-CAD Pattern Matching system that quantifies and sums variations in interconnect delay due to residual process nonidealities.

Variations in interconnect timing due to feature level variations are becoming increasingly significant as we continue scaling down to smaller technology nodes. Traditional design flows do not predict areas that are the most sensitive to fabrication. Pattern-Matcher is a fast-CAD tool that can be used to identify layouts geometries sensitive to non-idealities in fabrication. Opportunities exist to use the Patter-Matcher tool in design flows to compensate for variations from layout hot-spots.

The fast-CAD approach is to first limit the domain of evaluation to most critical paths. The impact of variations in processes such as lithography and CMP can then be estimated at each point along these paths. The estimate of variation is computed through the use of a lateral impact function for each of the processes and computing its

influence at every point along the path. This allows the change in geometry, the electrical parameters R and C, and the delay performance to be estimated. This process is similar to an image convolution with different convolution factors and lateral ranges for lithography and CMP. The speed is enhanced through utilizing only that portion of layout within the influence range of the lateral impact function.

This paper will present studies of the speed and accuracy of this approach. The accuracy of Pattern Matching is assessed through comparison with model based simulation. A set of examples of various types of interconnect runs and surrounding layouts for several levels of severity of process lens aberrations and CMP dishing are considered. The change in delay is characterized in terms of a Taylor series expansion of the degree of these process nonidealities. The results are also examined in terms of the influence of the nonidealities on the wiring geometry, its resistance and capacitance, and the resulting change in delay. The examples are chosen to give insight into how process induced delay variations scale at the 90, 65 and 45 nm generations.

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6521-17, Session 4

OPC to reduce variability of transistor properties

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In recent years, resolution limit has been reduced to 100 nm or below by making full use of various resolution enhancement techniques (RET) without changing the ArF (193nm) light source in optical lithography. Accordingly k1 factor has become lower; the pattern printed on a wafer shows complicated two dimensional (2D) distortion (e.g. rounding, necking, line end shortening, etc.). We have already proposed estimation method of transistor properties by using distribution gate length of simulated print image and SPICE simulation, and the method can reproduce experimental results accurately. On the other hand, we also proposed the advanced mask pattern correction method of alternating phase shift mask (Alt-PSM), and achieved to reduce the necking phenomena which influences leakage current of the transistor. In this study, we propose new gate-layer optical proximity effect correction (OPC) method that could reduce variability of transistor properties (drive current and leakage current) dependant on gate pattern layout. Experimental results show that we have reduced the variability of transistor properties without additional area penalty for 65 nm node standard cell library (S/C).

6521-18, Session 5

Improving the power performance of multicore processors through optimization of lithography

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The 90 nm node technology developed for high-performance processors had electrical gate length (Leff) control as a critical goal from the initial development stages. To increase Leff uniformity an aggressive across chip Lpoly variation (ACLV) target was targeted for the poly conductor layer critical dimension (CD) after etch. The ACLV goal was achieved through significant focus on every aspect of CD control. Optical proximity correction (OPC) models were created to correct through pitch variation. Site to site variation was driven lower by improving mask processes, exposure tools, lithographic process window, and etch process. Topography and orientation effects were also reduced. By reducing Leff variation power-performance metrics were continually improved as the products matured in manufacturing.

With a mature poly-conductor lithography process, three different systematic CD signatures were printed across a field that had 24 PSROs using across field dose compensation. The first “frowned” and had CDs ~1.5 nm smaller at the start and end of the scan than in the center of the scan, the second was flat and the third “smiled” and had CDs ~3 nm larger at the start and end of the scan than in the center of the scan. If Lpoly variation were the sole driver of PSRO variation then it would be expected that the fields printed with the flat CD signature would have the least PSRO variation. This is not what was found. Going from a frowning CD signature to the flat systematic CD signature across the scan did reduce the PSRO variation. However, the flat CD signature across the scan did not lead to a flat PSRO delay signature across the field. Instead the flat CD signature still resulted in the PSROs at the start and end of the scan switching faster than those in the center of scan. In fact, even when the smile CD signature was used the PSROs at the start and end of the scan switched faster than those in the center of scan. While all three systematic CD signatures resulted in a PSRO signature having faster PSROs at the start and end of the scan, going from the frowning to smiling CD signature did reduce the systematic portion of the PSRO delay signature by 45%. The benefits to power performance metrics and yield were ever especially noteworthy. At constant leakage (IDDQ) the decrease in PSRO delay was 6%. Yield of all good chips doubled. By implementing the dose compensation technique described above, cores of multicore chips were matched. With the improved core matching the frequency of a multicore chip was increased without causing the IDDQ spec to be violated.

This paper demonstrates that that decreasing Lpoly variation alone does not necessarily decrease device speed variation as measured by product sensitive ring oscillators (PSRO). It will demonstrate that only by decreasing Leff variation can PSRO variation be decreased.

6521-19, Session 5

Cost-performance tradeoff between design and manufacturing: DfM or MfD?

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Design, CAD, and manufacturing are focused on optimizing conversion methodology from electrical design to physical layout to improve

functionality, reliability, manufacturability, testability, etc., using Design-for-...ability (DfX) rules. A lot of pressure is being put on design to improve their understanding of all these issues, such that the mask pattern generated out of design layout would be "correct by construction" and comply with all of them. One can expect that such DfX-perfect layout should require significant effort to create, and its salient features would include: rectangular grid for critical geometries, such as poly gates, large enclosures of the active area in the corners of implant layers, ideal symmetry of the matched devices, minimal amount of jogs of the complex features, neat alignment of source and drain contacts, line ends of gates and interconnects, identical proximity for matched devices, doubled contacts and vias, etc. The question is if the cost of following all these practices at design time is not higher than that of other design improvement options. One alternative approach is to automatically adjust the "draft" layout using CAD post-processing such that all geometries would be optimized to conform to the DfX rules. This approach could be even more attractive than the "correct by construction" methodology as, in some cases, the optimization may also reduce the layout footprint on silicon. Another approach to the DfX methodology is to improve the manufacturing capabilities for the existing layout such that the process tools would be able to achieve high yield for a layout which conforms to some basic set of rules. This approach becomes even more relevant when the product line tries to address only a selected DfX issue to improve die performance where it is most needed. As an example, in this work we will discuss a few important device integration problems and their prospective solutions as proposed from design, CAD, and technology standpoints. For example, yield and functionality loss due to the high leakage of products for hand-held applications can be improved in three different ways. One is the redesign, using less leaky devices with longer channels. Another one is to increase poly CD by locally adjusting channel lengths using CAD sizing for MOSFETS which exhibit highest leakage, within the conformance to the device models. The third option is to change the lithography and etch process parameters or tools to reduce CD variation across the die and wafer. One can propose a flow chart to determine the best approach, depending on the direct cost of the solution, on the wafer volume, product time to market, and the success confidence level. We will show how the model can be used to optimize the solutions for device functionality, yield, and reliability.

6521-20, Session 5

Hardware verification of litho-friendly design (LfD) methodologies

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With the upcoming technology generations, it will become more and more challenging to provide a good yield and yield ramp. The contribution of Resolution Enhancement Technologies (RET) to Design for Manufacturability (DfM) targets is to provide a good printability over the whole process window and the control by print image simulation (PW-ORC) and to identify and remove yield issues imprinted in the drawn layout in early phases of the design flow. Such a lithography-aware design data flow, which we call LfD (Litho friendly Design) will be a very important step towards a fully developed DfM environment.

We report in this paper the application of a LfD design flow used for library cells at the MAPLE, an Infineon 65 nm design prototype fabricated by Chartered. The results of the process variability analysis are verified by experimental results (dose-focus exposure matrices).

6521-21, Session 5

Lithography and yield sensitivity analysis of SRAM scaling for the 32-nm node

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Memories play an increasingly important role in logic designs. The size and electrical performance of the six-transistor SRAM cell is often considered as the benchmark for a technology, as the typical transistor density of SRAM memory is five times higher than the logic transistor density for the same node. SRAM cells are extremely sensitive to process variations, and the design of a good SRAM cell requires a large effort from both the circuit design and layout perspective. In this paper, we analyze the sensitivity of the area of a 6T-SRAM cell subject to lithographic and non-lithographic constraints, and evaluate the impact of both overlay and CD uniformity on cell and memory yield.

The paper consists of four parts. In the first part, the different device options for scaling to the 32nm node are discussed. Both planar (bulk and SOI) and non-planar (FinFET) device architectures are considered. Circuit-level specifications combined with device behavior and performance lead to specifications for the different critical patterning steps, i.e. the acceptable CD variations for the different layers to ensure correct device operation.

The second part of the paper discusses the area sensitivity of the SRAM cell to the layout changes implied by the different process steps. The sensitivity to the CD and pitch of active, gate and contacts is discussed, as well as the sensitivity to non-lithographic process steps, like the spacer thickness. Additional design margins, needed to cope with the process variability, also have a clear effect on the cell area.

In the third part, the yield of a cell and a memory is found to be a function of the variability of the different process steps, and of the architecture of the memory. Both the functional and the parametric yield are analyzed. The functional yield is limited by fundamental problems in the patterning of the cell (e.g. contact-gate shorts) while the parametric yield is limited by the electrical characteristics of the circuit (e.g. access time, static noise margin). Both require statistical analysis, but the analysis of the parametric yield is non-trivial and requires device models and additional circuit simulations. We focus on the impact of overlay and CD uniformity, and find the minimum specifications for the parameters to guarantee the best functional yield for a given design. Inversely, knowledge of the parameters of the litho process allows for the optimization of the SRAM cell for yield.

In the final part, the results of the device analysis, area sensitivity, and yield analysis are combined. This allows the determination of the optimal 6T-SRAM cell design for a given device type and known process capabilities, and provides guidance as to how the different processes have to be optimized to ensure ITRS scaling.

6521-24, Poster Session

Litho-aware method for circuit power analysis through process

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Device extraction and the quality of device extraction is becoming of increasing concern for integrated circuit design flow. As circuits become more complicated with concomitant reductions in geometry, the design engineer faces the ever burgeoning demand of accurate device extraction. For technology nodes of 65nm and below approximation of extracting the device geometry drawn in the design layout polygons might not be sufficient to describe the actual electrical behavior for these devices, therefore contours from lithographic simulations need to be considered for more accurate results.

Process window variations have a considerable effect on the shape of the device wafer contour, having an accurate method to extract device parameters from wafer contours would still need to consider which lithographic condition to simulate. Many questions can be raised here like: Are contours that represents the best lithography conditions just enough ? Is there a need to consider also process variations? How do we include process variations in the extraction algorithm?

In this paper we first present the method of extracting the devices from layout coupled with lithographic simulations. Afterwards a complete flow for circuit power analysis using lithographic contours is described. Comparisons between power results from the conventional LVS method and Litho aware method are done to show the importance of litho contours considerations.

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6521-25, Poster Session

Circuit size optimization with multiple sources of variation and position-dependant correlation

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The growing impact of process variation on circuit performance requires statistical design approaches in which circuits are designed and optimized subject to an estimated variation. Previous work [1] has shown that by including extra margins in each of the gate delays to account for delay variation due to vth variability and optimizing the gate sizes, the circuit delay variation can be reduced by half. In this paper we are addressing two major limitations in the variation model presented in [1]: 1) Only the effect of threshold voltage is taken into account in formulating the delay variation, and 2) position dependant correlations between two gates are ignored. In the present work, extended models that include delay variations due to threshold voltage and effective gate length, as well as spatial correlations between gates are examined. For each model, circuit delay performance is evaluated using a 32bit Ladner-Fischer adder.

Delay variation due to effective gate length is derived using Pelgrom's model[2], and added to the vth dependent delay of each gate in the circuit. The maximum of the delays over all circuit paths is minimized subject to a total area constraint in order to obtain the optimal gate sizes. A piecewise linear model[3] is used for expressing the position dependant correlation between the gates in the circuit. In such a model, the correlation coefficient rolls off linearly as the separation distance between the gates until the separation is greater than some value XL, beyond which point the correlation remains a small constant. The spatial correlation terms are included in the gate delay formulation for each circuit paths. Due to the branching structure of the circuit, the computation time can be effectively reduced by combining paths that share common ancestors. The optimization schemes are used to size a 32 bit Ladner-Fischer adder and the designs are evaluated using Monte Carlo analysis.

The analysis shows that by including the effects of gate length variations and spatial correlations in addition to the original vth variation, the standard deviation of the circuit delay increased significantly from 0.47 to 1.96 nsec for the design in [1]. After optimizing against the effect of gate length variation in addition to threshold voltage, the standard deviation of the circuit delay is reduced from 1.96 to 1.52 nsec, and, while trying to achieve a 52 nsec maximum acceptable delay, the circuit yield is improved from 92% to 96%. An additional 2% yield improvement and 11% reduction in standard deviation of the delay is achieved by optimizing against the joint effects of gate length variation, threshold voltage variation and position dependant correlations on circuit delay. In our analysis, however, a large-scale spatial correlation model is used. Such model may have underestimated the actually correlations between the gates. Work is in progress to measure such correlation in actual state of the art processes and it will be presented separately.

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6521-26, Poster Session

Multidimensional physical design optimization for systematic and parametric yield loss reduction

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This paper demonstrates one of potential Design-for-Manufacturing solutions where comprehensive lithography analysis such as applying NILS, MEEF and Process Windows is used as a basis for physical design correction and optimization. A physical design flow typically includes RET/OPC and post-OPC verification (Silicon DRC) steps. Error markers, generated at the verification step, show locations of so called "hot spots" which are lithographically sensitive, prone to silicon failures areas. In our approach "hot spots" are traced back to a design and the design has been optimized to make those areas more stable. Hot spot markers of a flat post OPC layout are analyzed and categorized and only a unique instance of a "hot spot" is traced back to design hierarchy and corrected. Layout correction and optimization is guided by litho analysis. A set of lithography specific local constraints is added to a set of global constrains (DRC rules). A constraint-solving engine generates a new version of layout which is DRC correct and is now "litho/OPC friendly". Depending on a user accessible set of parameters design correction could be done with or without polygons edge segmentation and without critical areas increase. Different lithography technologies (such as immersion lithography with hyper NA) and different process models could be applied. Device electrical performance in conjunction with simulated and extracted silicon shapes, are discussed.

Our solution shows substantial hot spot reduction within reasonable layout optimization time.

6521-27, Poster Session

Highly accurate model-based verification using SEM image calibration method

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In the past when design rule is not tight, CD data-based OPC modeling was acceptable but as the design rule shrinks process window lowered, MEEF(Mask Error Enhancement Factor) increased. Hence, Data for OPC modeling have also become more complex and diverse in order to characterize the critical OPC models. The number of measurement points for OPC model evaluation has increased to several hundred points per layer, and metrology requests for realized pattern shapes on the wafer are no longer simple one-dimensional measurements. Traditional CD data-based OPC modeling is based on 1D parameter fitting and has limited information. Due to this error the accuracy of the model has limitations. Currently, further development of modeling resulted in creation of SEM Image Calibration. SEM Image Calibration use SEM Image to calibrate large volume 2D information data. SEM Image Calibration is based on SEM Image but modeling accuracy can be increased using additional CD data. It needs only SEM Images instead of several hundred points CD data, so data feedback is more easy. But this method makes it difficult to predict total region in that SEM Image is restricted in local region. And modeling accuracy is highly depend on SEM Image quality.

In this paper, we propose SEM Image Calibration method that feeds back SEM Image calibrated model set to model-based verification method. By using this method, modeling accuracy is increased and better model-based verification can be made. We will be presenting the result after the method has been applied on sub-60nm device and the capability of this method.

6521-28, Poster Session

The study for increasing efficiency of OPC verification by reducing false errors from bending pattern by using different size of error nonchecking area with various corner lengths

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In recent years, model based verification for optical proximity effect correction (OPC) has become one of the most important items in semiconductor industry. Major EDA companies have released various softwares for verification. They have developed and introduced new methods to achieve more accurate results of OPC verification. The way to detect only real errors by excluding false errors is the most important

thing for correct and fast verification process, because more time and human resource are needed for the review of verification as increasing false errors. As the major sources of false errors are bending patterns. The number of those from bending patterns is over thousands and they are inevitable. The most verification tools have the method for excluding those by using error non-checking area. Real errors around bending pattern will not be able to detect with too big size of area, while too many false error will be reported with too small size of area. Since currently most verification tools have only one size of error non-checking area, it has been impossible to achieve most accurate verification results. Through the optimization of area size with different corner length, we could get more accurate and effective results of OPC verification and decrease the time for review of results. In this paper, the suggestion in order to increase efficiency of OPC verification process by using different size of error non-checking area with various corner lengths is presented.

6521-29, Poster Session

DFM flow by using combination between design based metrology system and model-based verification at sub-50-nm memory device

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As the minimum transistor length is getting smaller, the variation and uniformity of transistor length are seriously affected on device performance. So the importance of optical proximity effects correction (OPC) and resolution enhancement technology (RET) cannot be overemphasized. However, OPC process is regarded by some as a necessary evil in device performance. In fact, every group which includes process and design group, are interested in whole chip CD variation trend and CD uniformity, which represents real wafer.

Recently, design based metrology systems are capable of detecting difference between data base to wafer SEM image. Design based metrology systems are able to extract information of whole chip CD variation. According to the results, OPC abnormality was identified and design feedback items are also disclosed. The other approaches are done on EDA companies, like model based OPC verifications. Model based verification will be done for full chip area by using well-calibrated model. The object of model based verification is prediction of potential weak point on wafer and fast feed back to OPC and design before reticle fabrication. In order to achieve robust design and sufficient device margin, appropriate combination between design based metrology system and model based verification tools is more important.

Therefore, we evaluated design based metrology system and matched model based verification system for optimum combination between two systems. In our study, huge amount of data form wafer results are classified and analyzed by statistical method and classified by OPC feedback and design feedback items. Additionally, novel DFM flow would be proposed by using combination of design based metrology and model based verification tools.

6521-30, Poster Session

Application of enhanced dynamic fragmentation to minimize false error from post OPC verification

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At low-k imaging, the model based OPC technology has been becoming the widespread adoption of in lithography technology. Consequently, for sub-90 nm process, it is extremely important to model the lithography process with high accuracy. As tuning a model-based OPC recipe, most engineers spend most of their time on the model fitting to make simulated curves a better fit to empirical data. Despite of having a good accuracy model, if the OPC correction recipe isn't optimized, the OPC errors will be increased. Most failure cases, however, do not result from a model with bad fitting. Instead it has been frequently found that undesired OPC outcomes were derived from fragmentation process. When OPC verification is performed, mostly error points are due to either low frequency fragmentation or extremely high fragmentation. Especially in the case of logic device, it has various patterns so that correction recipe makes errors.

Conventional OPC fragmentation method operates under a set of simple guiding principles. All patterns are to be uniform in finite size from edge of polygon. Within each fragment, the intensity profile (aerial image) and edge-placement error (EPE) are calculated at a settled location. Finally, the length of the entire fragment is moved to correct for the EPE at that location. This is to be often against simulation like a model based OPC. In the strict sense, model based OPC is depended on simulation results not only moving of all fragments in the layout are reduced to zero but also dividing of all polygon edges. This drastically increased data volume and the computation time required to perform OPC. Therefore, more powerful fragmentation mechanism will be one of major factors for the success of OPC process.

In this study, a new approach of fragmentation has been tested, which reduces OPC correction error. First, we check the weak point of all pattern using NILS and contrast. Second, weak points apply high frequency fragmentation based on simulation contour images. The others are divided into normal correction recipe. This improves to accurate OPC correction for weak point which can divide a fine classification. It also is possible to reduce OPC time for non critical pattern applied moderate fragmentation.

6521-31, Poster Session

Pattern decomposition for double patterning from photomask viewpoint

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Double Patterning Technology (DPT) has been evaluated and reported since 32nm half pitch is recognized to be required with conventional immersion ArF lithography. DPT requires pattern decomposition into two pattern sets and the decomposition becomes more complex for especially so-called logic pattern including irregular pattern placement and many-vertices polygons. The innocent decomposition often creates forced segmentation of those polygons and two different aspects of photomasks such as density or substantial line direction. Those decomposed photomasks not only produce large possibilities of different error behavior but also leave annoyance complexity untouched.

It is well known that line-ends and dense twisted lines produce large MEF. Then tighter specification for photomask fabrication has been required since the resolution limit was getting below the exposure wavelength. So the decomposition that creates tight patterns into separate two photomasks has possibilities of the fabrication load lighter.

In this paper, the decomposition of criteria for DPT, which helps photomask fabrication with small possibilities, is evaluated and discussed. Furthermore though it's getting to popular that overlay and CD uniformity of photomasks for DPT impact to completed CD with wafer exposure directly, considering other errors such as CD shift or phase error which are supposed to recover by exposure in addition to those errors are also studied.

6521-32, Poster Session

A methodology to analyze impacts of proximity effects and layout topologies on circuit performances

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Due to non-ideal optical effects such as aberration and optical diffraction, printed poly gates on the wafer suffer from across-gate linewidth variation (AGLV) and across-chip linewidth variation (ACLV) especially in sub-wavelength technology. In addition, proximity effect caused by optical diffraction makes distorted poly gate pattern layout-dependent. The poly gate distortion will impact the device electrical characteristics, including drive current (Ion), leakage current (Ioff), and threshold voltage (Vt). For circuits sensitive to layout, such as memory cells, different layout topology can result in different image distortion for each transistor. Consequently, the circuit performance will vary with

layout topology and local layout adjustment after applying resolution enhancement technologies (RETs). In this paper, we propose a methodology to examine the impact of circuit layout on circuit performance with examples based on 6T-SRAM cells. The gate pattern is simulated through lithography simulator to get the printed poly image. The device model for each non-ideal transistor is extracted based on poly-gate pattern from lithography simulation. Circuit performance is obtained by incorporating these extracted device models into a circuit simulator. Different layout topologies are also simulated to compare their circuit performances. These results provide circuit designers with layout guidelines considering sub-wavelength lithography effects.

6521-33, Poster Session

Manufacturing for design (MFD) in practice: improving OPC convergence considering design intent

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Model-based Optical Proximity Correction (MBOPC) has become one of the most important resolution enhancement technologies (RETs), which can effectively improve the image fidelity and process robustness. Currently the MBOPC work is performed by iteratively shifting the polygon edges of mask pattern until convergence requirements are achieved. Each MBOPC iteration is very time-intensive, because lithography model simulation requires much processing time. Therefore, how to effectively decrease the MBOPC iteration number becomes an important problem. Typically, MBOPC is performed by heuristically tuning feedback parameters without considering design intent. Nevertheless, the design intent related to the convergence requirement is also an important factor which affects the needed iteration number. Traditionally, lithographers desire the printed wafer pattern to be as close to the corresponding design pattern as possible. They just regard the rectangle-based layout from physical design as the target pattern for OPC without considering any design specification such as timing, power, and so on. Such stringent convergence requirement leads to unnecessary increase of MBOPC iteration number and total tape out cost. As the semiconductor industry is continuously moving to 65-nm node technology and beyond by further pushing 193-nm optical lithography, MBOPC convergence difficulties increase significantly due to even stronger sub-wavelength effects. The pure image-based MBOPC process is no longer sufficient. A concept of manufacturing for design (MFD) is evolving to alleviate RETs difficulties. For example, if the convergence requirement can be relaxed properly without violating any design specifications, the MBOPC iteration number could be effectively reduced. In this paper, we applied MBOPC to a simply practical circuit and examined the influence of different convergence requirements on the needed iteration number. The results assist us in determining appropriate convergence requirements and target pattern which result in fewer MBOPC iteration number while achieving the design specification within the acceptable tolerance.

6521-34, Poster Session

Lithography enhanced manufacturability analysis by using multilevel simulated contours

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Since the sub-50nm logic lithography approaches to k1 value of 0.3, it may be an impossible task to print typical logic patterns composed of random shapes and mixed pitches using the conventional RETs (resolution enhancement technology). As some effective solutions to mitigate the issues, LFD (lithography friendly design) and advanced OPC technology is being considered and developed. However, the investigation on the distortion types of various 2-dimensional real patterns has rarely proceeded up to now, while lithographical hot spots are observed are dominated by the 2-dimensional patterns rather than in the 1-dimensional patterns. In order to provide a litho friendly design layout and a good OPC performance for sub-50nm node logic device, the analysis and the classification of the 2-dimensional hot spots need to be preceded above all. In this study, we have analyzed various types of hot spots such as end-cap pull back/pull up, contact overlap and gate-poly & active coverage of implant levels for most layers of the sub-50nm logic device. We have correlated the dimensional deviation of multi-level simulated contours and then scored the pattern fidelity of the extracted hot spots by using the CDSEM image recognition function. Finally, a feedback strategy was implemented to reduce the 2-dimensional hot spots through the correction stage of the OPC recipes. Especially, in case of the gate-poly layer which requires an accurate CD control, the CD distributions of the effective gate (just on active) provided an improved hidden hot spots detect-ability with the comparison of the estimated gate CD distribution and the drawn CD distribution, and from the analysis of the extracted hot spots, it could be improved that the narrow distance between active and gate-poly at inner vertex structure is one of the major factor inducing the hot spots.

Our study based on a photolithography manufacturability analysis is extended to provide a good guideline for litho friendly design and DFM approaches.

6521-35, Poster Session

Characteristics aware OPC modeling and correction

J. K. Tyminski, Nikon Precision Inc.; L. Depre, Synopsys, Inc. (France); P. J. M. VanAdrichem, Q. Zhang, Synopsys, Inc.

In projection tools used by IC industry, the projection lens only captures finite number of IC pattern diffraction orders. This low pass filtering in scanners leads to a range of optical proximity effects such as pitch-dependent CD variations, corner rounding and line-end pullback, which distort IC patterns imaged on wafers. OPEs are driven by the imaging conditions, such as wavelength, illuminator layout, reticle technology, lens numerical aperture, to name a few. These predictable OPEs result in imaged IC pattern excursions from the intended design, leading to undesired IC characteristics. To mitigate the pattern excursion due to OPEs, the photolithography community developed optical proximity correction methodologies, adopted and refined by the EDA industry. In the current implementations, OPC applied to IC designs can correct the layout to compensate for OPEs and provide imaged patterns meeting the design requirements.

OPC models are dependent on imaging conditions. In principle, OPC models can correct the impacts of all, fundamental and engineering imaging drivers and limiters. However, , the conventional implementations of the OPC models take into consideration only the ideal imaging conditions and scanner characteristics such as real illuminator shape and lens aberration are not modeled. The key question becomes: how effective are these idealized OPC models in dealing with realistic conditions such as the ones present on the scanners used in IC manufacturing.

To illustrate the impacts of realistic imaging conditions on OPC quality, we first studied OPEs generated by imaging setup defined by a combination of idealized illuminator and projection lens. We then compared these results with a set of corresponding OPEs generated under realistic illuminator and projection lens conditions corresponding to the initial, idealized case. The range of scanner characteristics' impacts on OPEs revealed by this comparison showed that the accuracy of the OPC models and the quality of OPC correction are limited by realistic imaging conditions provided by the imaging tools used in IC manufacturing.

To further investigate the scanner characteristics' impact on OPC performance, two OPC models were built: 1) an idealized model representing the ideal illuminator and projection lens, and 2) a realistic model incorporating realistic scanner characteristics. We applied OPC correction to a critical layer of an IC design and performed OPC verification on the corrected layout based on these two OPC models. The resulting CD analysis showed that idealized model based OPC did not correct the design layout imaged under realistic conditions to a sufficient accuracy, while application of realistic OPC model corrected the layout to efficiently compensate for OPEs under realistic imaging conditions. The results of the comparison also highlighted the fact that scanner-characteristics-aware OPC leads to dramatic improvements in imaged pattern CD control.

The impact on OPEs and OPC quality from scanner characteristics. i.e. real illuminator source shape, lens aberration, apodization, and flare, in the past neglected in conventional OPC modeling, are studied in our work. We demonstrated that encoding scanner characteristics in OPC is

the key to enhancing OPC quality in 65nm, 45nm technology nodes and beyond.

6521-36, Poster Session

Design CD pattern recognition for metrology recipe automation

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One of the challenges in metrology today is to automate the process of translating the design CDs to measurement recipes. Recipe makers for most metrology tools require a complete description of the CD types, shapes, and even layers for the case of CD search using multiple layers. However, most CD list created from design rule check, OPC validation or yield analysis do not have these informations. And these CDs can be of variety of sizes, shapes, types, and even from different layers.

This paper proposes a method that bridges the gap from design CD to measurement recipe and enables closed loop automation between design and metrology. One of the key issues to be resolved is pattern recognition with little information about the targets. Random pattern classification can be a very expensive operation and could lead to multiple and unreliable results. We propose to establish a “CD Pattern Vector” library based on tool capability. The reason being CD pattern classification beyond the tool capability is not very useful for metrology.

Once the pattern classification is done, the other challenge is to translate the pattern into a measurement recipe. It is a challenge because there could be multiple structures within a pattern that can be of interest, however, only certain structure can create a hot spot for design team. Through pattern analysis, one can identify the hot spot and create a tool recipe to measure this location. This paper proposes to build in pattern analysis capability to optimize the recipe such that it reflects nature of the hot spot.

The paper will compare the proposed method with conventional pattern matching method, and shows the new method is much more effective in identifying some difficult OPC features. The pattern recognition success rate for various types of structures will also be evaluated. Our proposed solution is robust and can adapt to ever changing metrology capabilities.

6521-37, Poster Session

Wire sizing/spacing for lithographic printability optimization

K. Cao, J. Hu, Texas A&M Univ.

As the VLSI feature size has already decreased below lithographic wavelength,

the printability problem due to strong diffraction effects poses a serious threat to the progress of VLSI technology.

A circuit layout with poor printability implies that it is difficult to make the printed features on wafers follow designed shapes without distortions.

The development of Resolution Enhancement Techniques (RET) can alleviate the printability problem but cannot reverse the trend of deterioration. Moreover, over-usage of RET may dramatically increase photo-mask cost and increase the cycle time for volume production. Thus, there is a strong demand to consider the sub-wavelength printability problem in circuit layout designs. However, layout printability optimization should not degrade circuit timing performance.

In this paper, we introduce a wire sizing and spacing method to improve wire printability with minimal adverse impact on interconnect timing performance. A new printability model is proposed to handle partially coherent illuminations. The difficulty of the interconnect printability optimization due to its multimodal nature is handled with a sensitivity based heuristic. Lithographic simulation results show that our approach can improve the printability in term of EPE (Edge Placement Error) by 20%-40% without violating wire width and spacing constraints.

6521-38, Poster Session

A rigorous method to determine printability of a target layout

B. Yenikaya, A. Sezginer, W. Staud, Invarium Inc.

We present a method to determine if a given combination of target layer, edge-placement tolerances, and dose-latitude violates laws of physics. When this method determines the design requirements are not feasible, the negative result applies to all mask, RET, and OPC technologies except double-patterning (litho-etch-litho-etch).

We rigorously prove that the intensity of the optical image formed in the photoresist is band-limited in the plane of the wafer. The support of the 2-D spatial Fourier transform of intensity is contained in a disk of radius (4 pi NA / wavelength) in the transverse wave-number plane (a.k.a. angular spatial frequency plane). This result is valid irrespective of: the mask technology (binary, attenuated-PSM, alternating-PSM, CPL, multi-tone); the use of assist features; OPC method; and the illumination pattern and polarization. The band-limit is equally valid whether one uses the Kirchhoff approximation or a 3-D, full-wave solution of Maxwell’s Equations to calculate diffraction of illumination by the photomask. Photo-acid generation and reaction-diffusion processes are frequently approximated as linear processes for the purposes of OPC. The latent image (concentration of de-protected sites) is approximated by a convolution of the optical image intensity with a point-spread-function of resist blur. According to this approximation, the latent image is also band-limited by (4 pi NA / wavelength). This result is valid for multi-exposure methods such as the double-dipole method, since the sum of two equally band-limited functions is subject to the same band-limit.

We transform the target pattern, edge-placement tolerances, and dose-latitude requirement into a set of inequalities. Each inequality states that the image intensity at a certain point should be larger or smaller than a value that depends on the threshold and dose latitude. The resulting system of equalities can be infeasible over the set of band-limited functions. Infeasibility of the system of inequalities indicates infeasibility of the design requirements. In that case, to achieve feasibility, either the layout has to be re-targeted, (NA/wavelength) has to be increased, or dose-control has to be tightened. The algorithm returns an intensity image that obeys the band-limit and either satisfies the design requirements, or comes closest to satisfying the design requirements in case of infeasibility. The corresponding resist contours are also provided. When the design requirements are infeasible, offending locations are marked. Such checks can be applied to DRC clean layouts to determine hotspots prior to applying RET/OPC.

6521-39, Poster Session

Computational complexity of image calculation and OPC at the 32-nm node

B. Yenikaya, A. Sezginer, F. X. Zach, W. Staud, Invarium Inc.

We show that computational complexity, hence run-time, of an OPC algorithm is linearly proportional to density when the mechanism that determines length-of-influence is optical diffraction.

Density is proportional to number of features per unit area by definition. This calculation assumes that all physical length parameters are proportional to (wavelength / NA) as the technology node moves from 65 nm, to 45nm, to 32 nm. Consequently, density increases in proportion to (NA/wavelength)2, and k1 remains constant. The number of features, edges, segments, and target points per unit area are linearly proportional to density.

Image calculation by SOCS requires convolution of pre-computed kernels with the mask pattern. The convolution can be performed either in the spatial-frequency-domain or in the space-domain. When length-of-influence is determined by diffraction, the computational cost of both algorithms is proportional to density. If there were a blur mechanism whose length-scale were constant irrespective of the technology node, and larger than the optical length-of-influence, then the computational complexity of the space-domain approach would scale with density-squared.

The OPC algorithm analyzed in this study has target points and line segments. It takes into account the influence of all edge-segment-movements on all target points within the length-of-influence. The algorithm considers all interactions and takes a step in a multi-dimensional search space, which moves all edge segments, by different amounts, at each step. The algorithm converges typically in 3 iterations. We show the actual performance of the OPC algorithm on a fixed sized region. As we move to smaller technology nodes, the features shrink and more features come into the region that is subject to OPC. No improvement in computational resources is assumed.

6521-40, Poster Session

Novel technique to separate systematic and random defects during 65-nm and 45-nm process R&D stage

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Defect inspections performed in R&D may often result in 100k to 1M defect counts on a single wafer. Such defect data combine systematic and random defects that may be yield limiting or just nuisance defects. It is difficult to identify systematic defects from defect wafer map by traditional defect classification where random sample of 50 to 100 defects are reviewed on review SEM. Missing important systematic defect types by traditional sampling technique can be very costly in device introduction. Being able to efficiently sample defects for SEM review is not only challenging, but can result in a pareto that lacks in usefulness for R& D and for yield improvement.

To mitigate the issue and to reduce yield improvement cycle in advanced technology, a novel method has been proposed. Instead of using random sampling method, we have applied a pattern search engine to correlate defect of interest (DOI) to its pattern background. Based on the approach we have identified an important defect type, STI cave defect, to be the major defect type on defect pareto. For the defect type, stack die map was generated that indicated a distinctive signature. The result was compared against design layout to confirm that the defects were occurring at certain locations of design layout. Afterwards the defect types were reviewed using SEM and in-line FIB for further confirmation. We have found the cause of this void defect type to be poor gap-fill in deposition step. Based on the novel technique, we were able to filter out a systematic defect type quickly and efficiently from wafer map that consist of random and systematic defects.

6521-41, Poster Session

Intelligent fill pattern and extraction methodology for sensitive RF/analog or SoC products

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Non-uniform pattern density of physical layers in the die,such as active area, poly, or metals, compromises product manufacturability and electrical characteristics. At active level, variations in pattern density lower the punch-through or breakdown voltages. At poly, macroloading due to the differences in feature proximity impacts pattern fidelity degrading device matching. At metal levels, variations in pattern density and planarity across the die give rise to high via resistances and variations of inter-layer capacitive coupling. These issues are of particular significance to analog devices, especially operating at radio frequencies, or Systems-on-Chip. The die blocks in those products have intrinsicaly different pattern densities due to their different functions and these differences usually can not be mitigated at design stage. Instead, pattern density has to be made acceptably uniform at die integration stage, by global addition of fill features (waffles). While conceptually simple, this presents significant technical challenge as the criteria for the fill pattern are often difficult to meet. This is because a small number of waffles may not be sufficient, whereas a large number of waffles would increase the overall pattern density which may not be possible to meet in all die regions. One way to resolve this would be to iteratively add dummy features by manual drawing and verification of pattern density which is usually too time consuming. However, automated approaches which add fill pattern of fixed density, may not be successful in equalizing all the die regions, even if some changes in the die architecture are allowed. In addition, dummy features of high density are not preferred by for the RF/analog applications, as they compromise signal integrity by capacitive coupling through the waffles. In the methodology proposed in this work, the die pattern density is first analyzed followed by the adjustable, intelligent fill of dynamic density. This way, it is possible to keep pattern density close to the one introduced by design and work only on the areas of small density where dummy structures are needed. We also propose that the waffles are introduced at standard cell level where their electrical impact can be extracted to ensure that all the required blocks could be placed on the product and their properties would not change as a result of creating mask data from drawn design layers.

6521-42, Poster Session

Scanner parameter sensitivity analysis for OPE

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The imaging power of microlithographic lenses, normalized to minimum feature size, has become lower and lower for each generation, even with the progress of high-NA lithography. The rate of increase of NA has not kept pace with Moore's law. Therefore, low k1 lithography techniques such as RET (Resolution Enhancement Technology) have been applied for more than a decade. RET, however, is a technique to increase the imaging contrast only for dedicated pattern types/sizes, and may decrease the imaging power for other than dedicated patterns.

To fill this gap between actual imaging power and required imaging power, OPC (Optical Proximity Correction) technologies are becoming more and more important for leading edge lithography. The accuracy of OPC is important for high performance quality chips. On the other hand, due to low relative imaging power and high NA of the current projection lens, imaging performance is very sensitive to various kinds of errors such as defocus, dose error, aberration, apodization, flare, polarization aberration, polarization status, etc.

In order to solve this, scanner parameters, which can be obtained even before the scanner itself has been completed, should be embedded in the imaging simulation in OPC design and verification to improve the accuracy. In addition, OPE (Optical Proximity Effect) data simulated with the scanner parameters may be useful for early stage reticle design before actual exposure using first lot scanners.

We have studied the sensitivity of OPE to scanner parameters and prioritized parameters to be input to the OPC design and/or verification process for improving the accuracy without significant increase in the amount of calculation. Some experiments for validation of the effects of the scanner parameters embedded in OPC have also been performed using exposure results of the 1.07NA ArF immersion-scanner NSR-S609B.

6521-44, Poster Session

OPC and design verification for DFM

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The downscaling of the feature size and pitches of the semi-conductor device requires the improvement of device characteristics and high yield continuously. In lithography process, RET techniques such as immersion and polarization including strong PSM mask have enabled this improvement of printability and downscaling of device. It is true that this optical lithography is approaching its limit in sub 50nm too. So other lithographic technique like EUV is needed but the application is not yet available. In this point of view, the realization of lithography friendly layout enables good printability and stable process. And its scope is being enlarged and applied in most semi-conductor devices. For this precise and good realization of lithography friendly layout, we need full chip data feedback of design issue, OPC error and aberration and process variables.

In this paper, we report the results of data feedback using new DFM verification tool. This tool enables full chip inspection through E-beam scan method with fast and accurate output. And these data can be

classified with each item for correction and stability check through die to database inspection. Especially in gate process, total CD distributions in full chip can be displayed and analyzed for each target with simple method. At first we can have obtained accuracy data for each target and CD uniformity from hundreds of thousands of gate pattern. And second we can have detected a delicate OPC error by modeling accuracy and duty difference. It is difficult to get from only measurement of thousands pattern. Finally we have checked impact of area density and pattern location in full chip. These results should be considered and reflected on design stage

6521-45, Poster Session

Self-assembled dummy patterns for lithography process margin enhancement

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Over the last couple of years, Design For Manufacturability (DFM) has progressed from concept to practice. What we thought then is actually applied to the design step to meet the high demand placed upon very high tech devices we make today. On of the DFM procedure that benefits the lithography process margin is generation of dummy patterns. Dummy pattern generated at design step enables stable yet high lithography process margin for many of the high technology device. But actual generation of the dummy pattern is very complex and risky for many of the layer used for memory devices. Dummy generation for simple pattern layers such as Poly or Isolation layer is not so difficult since pattern composed for these layers are usually 1 dimensional or very simple 2 dimensional patterns. But for interconnection layers that compose of complex 2 dimensional patterns, dummy pattern generation is very risky and requires lots of time and effort to safely place the dummy patterns. In this study, we propose simple self assembled dummy (SAD) generation algorithm to place dummy pattern for the complex 2 dimensional interconnection layers. This algorithm automatically self assembles dummy pattern based on the original design layout, therefore insuring the safety and simplicity of the generated dummy to the original design. Also we will evaluate SAD on DRAM and FLASH memory interconnection layer using commercial Model Based Verification (MBV) tool to verify its applicability for both litho process margin and DFM perspective.

6521-46, Poster Session

Modeling micron-scale gate length variation and spatial correlation

P. D. Friedberg, G. H. Cheng, Q. Y. Tang, C. J. Spanos, Univ. of California/Berkeley

Systematic gate length variations caused by microlithographic processing [1] have a significant impact on the variability of circuit performance. Previous work [2] has shown in simulation that by completely reconciling sources of deterministic variation, long-range (millimeter separation scale) spatial correlation in the remaining variation is virtually zero. However, Pelgrom's model [3] suggests that at narrow separation distances, some spatial correlation is inherent in the physical properties of semiconductor devices; since our previous work was limited by the mm-scale spatial granularity, shorter separation scales could not be investigated. As a result, a connection between our measurement results and Pelgrom's model could not be made.

To examine the nature of spatial variation and correlation in critical dimension (CD) in the sub-mm regime, a set of electrical linewidth metrology (ELM) test structures was designed [4]. The base-case ELM structure enables the measurement of CDs of neighboring polysilicon lines packed at maximum density. In variants of the base-case structure, dummy lines are inserted between the measurable polysilicon lines, allowing for measurement of near-neighbor lines and thereby increasing the total measurable range. With the fine granularity and wide range of these test structures, spatial variation and correlation in the separation range of 0.2μm to 1.0mm can be measured, and our understanding of spatial variation and correlation in gate length can be completed. The initial design of these test structures was presented at last year's conference; the results and analysis from the finished silicon product will be presented at this year's conference.

In addition, a second set of test structures aimed at deconvolving sources of manufacturing variation has been submitted for manufacture. The ELM test structures from [4] are interleaved with an array of MOS transistors that is fully testable using a four-point method. By measuring the electrical performance of MOS devices side-by-side with CD test structures, we aim to decouple the CD variation from the other sources of variation (primarily random dopant fluctuations and oxide thickness variation) contributing to overall device performance variability. Once all the test structures have been characterized, the spatial variation distributions of both CD and other device parameters will be instantiated in an analytical macromodel-based Monte Carlo simulation framework that enables exploration of the circuit performance variability space under varying forms of process control.

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6521-47, Poster Session

Implementation of a design manufacturing interface for 65 nm and beyond

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As the technology moves towards ever smaller dimensions, processing high-yielding integrated circuits is more and more difficult. The simple Design Rules are not enough to capture the context-dependent process variations. There is a need to have a better connection between design and manufacturing to improve the coverage of the manufacturing variations. To fill this gap, we have implemented a Design Manufacturing Interface (DMI). This DMI comprises all needed information for the designer, from Rule-Based data to Model-Based data.

In this paper we present the implementation of the DMI for 65nm platform and beyond. We provide designers with DFM solutions that cover the Rule-Based domain with the use of DFM guidelines, associated metrics and tools (DFM checker). We also supply the designers with Model-Based information, which allows to check designs for DFM compliancy with respect to CMP and litho (OPC/RET) robustness. We will illustrate this realization with 65nm and 45nm examples. The detailed flow and DFM compliancy will be explained.

6521-48, Poster Session

Novel method for quality assurance of two-dimensional pattern fidelity

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This paper proposes evaluation pattern generating method which realizes two-dimensional feature. Below 65nm design node, even using

the leading edge optical technique, it is close to the resolution limit. As a result, patterning fidelity to the target becomes worse under low k1 lithography condition. Complex layout patterns, especially two-dimensional feature becomes more and more sensitive to photo-resist bridging and necking. This means that rich two-dimensional pattern is becoming more necessary to cope with lithographic patterning fidelity issues, such as quality assurance of OPC script and establishment of Design Rule, and so on.

A new pattern generating method shown by this paper can provide us a plenty of unexpected two-dimensional patterns by way of Monte Carlo method. It can also take Design Rule Checker into account to presents patterns without any Design Rule violation. And in addition, it devises method for generating characteristic feature of each layer.

More than 10000 variations of feature can be generated in one day by this new method and the 10000 variations is estimated to be equal to all pattern variations which show up in 10 real products. More examples are provided to verify the efficacy of two-dimensional pattern generated by this method. It is shown that the proposed method is significant efficient especially for finding out weak pattern feature which are unfaithful to the target with low k1 factor.

Keywords: Two-dimensional pattern, Pattern variations, Unit pattern, Arrangement frame, Design Rule

Figure1 : Two-dimensional patterns generated by new method

6521-49, Poster Session

A systematic approach for capturing interconnects hot spots

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Overlay variations between different layers in Integrated Circuits fabrication can result in poor circuit performance, even worst it can cause circuit mal function and consequently affect process yield. Coupled with other lithographic process variations this effect is highly magnified. This leads to the fact that searching for interconnects hot spots should include overlay variations into account. The accuracy of inclusion of the overlay variation effect comes at the expense of a more complex simulation sit up. Many issues should be taken into consideration including runtime, process combinations to be considered and the feasibility of providing a hint function for correction.

In this paper we present a systematic approach for classification of interconnects durability through the lithographic process, taking into account focus, dose and overlay variations, the approach also provides information about the cause for the low durability that can be useful for building a more robust design.

This classification can be accessible at the layout design level. With this information in hand, designers can test the layout while building up their circuit. Modifications to the layout for higher interconnects durability can be easily made. These modifications would be extremely expensive if they had to be made after design house tape out.

We verify this method by showing real wafer failures, due to bad interconnect design, against interconnects' durability classifications from our method.

6521-50, Poster Session

Ensuring production-worthy OPC recipes using large test structure arrays

C. M. Cork, Synopsys, Inc. (France)

The continual shrinking of design rules as the industry follows Moore's Law and the associated need for low k1 processes, have resulted in more layout configurations becoming difficult to correct acceptably. OPC Verification tools can check the quality of a correction based on predetermined specifications for CD variation, line-end pullback and Edge Placement Error and can highlight layout configuration where violations are found.

The problem for a Mask Tape-Out group is that they have little control over the Design Styles coming in. While most designs may follow an OPC-friendly layout style, the few that don't may need to be sent back to the designers for modifications. Different approaches to eliminating these violations have included highly restrictive Design Rules, whereby certain pitches or orientations are disallowed. The tight link between Design and Mask Tape-Out found in Companies that control both can enforce perhaps just one Standard Cell set and IP that can be pre-qualified for OPC friendliness.

In contrast, Semiconductor Foundries are presented with a much larger variety of design styles and unless the recipe is set up with great care, there is a real possibility that some will contain layout configuration which will have a verification issue. Therefore setting up a recipe to give acceptable verification results, based solely on one customer GDS is clearly not sufficient to guarantee that all future tape-outs will be similarly clean. Furthermore, changing the recipe parameters or code to fix a problem on one particular problematic layout could result in a previously acceptable layout configuration with the old recipe having a violation with the new recipe.

The need to re-qualify a recipe over multiple GDSs at each recipe change could easily result in excessive computational requirements.

An alternative approach suggested by this paper, is to encapsulate the problematic structures into a large array of test structures whose dimensions are varied over the space of the design rules and reasonable design styles. By checking the new recipe over all of these test structures one could gain more confidence that this recipe would be suitable for multiple tape-outs with multiple design styles. This paper gives some examples of the implementation of this methodology. Only once a recipe that gave good results over all of these test structures was it considered for testing over multiple GDS's and then deemed suitable for production.

By using both techniques of Product and Test Structure for recipe validation were the authors able to provide a recipe with a high confidence of correction quality over multiple tape-outs.

6521-51, Poster Session

Intelligent visualization of lithography violations for 45-nm and beyond

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Full chip lithography verification has become a necessary process prior to mask fabrication as critical dimensions have shrunk below 100nm. The challenge for 45nm OPC verification is to enable masks with adequate process margins to be designed and fabricated despite the limited exposure margin and shallow depth of focus required by sub 50nm resolution.

Initially, full chip lithography verification was primarily used to capture fatal pinch/bridge failures. As process margins decrease, the number and sophistication of error checks has substantially increased. Today, it is becoming routine to flag not only pinch/bridge, but also checks such as CDU (critical dimension uniformity), MEEF (mask error), line end shortening and assist feature printing thru the entire exposure/focus process window. Consequently, automated analysis and intelligent presentation of violation results has become a necessity as the amount of data to analyze has exploded.

In this paper, an automated reporting scheme will be discussed. The central element of this automated analysis is a flexible methodology to automatically query captured violations and programmably allow multivariate prioritization according to the user's preference. Prioritized errors are automatically contoured and saved in a report to be reviewed by the user. Another element to be discussed in this paper are graphical techniques which convey data distributions over many variables. Finally, the use and misuse of statistics based on normal distributions to describe modeled lithography violations will be discussed.

6521-52, Poster Session

Production-worthy OPC verification methods for protecting against process variability

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As RET and OPC solutions get more complex and the ability of a process to tolerate small OPC errors decreases due to smaller process

windows, the need for more sophisticated verification solutions is becoming apparent. These OPC verification solutions are needed both for the development of new OPC algorithms and models, as well as for verification of all mask builds as part of a routine production process. At the 90 nm technology node it has been practical to use relatively simple verification methods for routine production use, i.e. simulations at nominal dose and focus only. For each successive generation, the need for including simulations at off-nominal process conditions increases. The most straightforward approach is simply to repeat the verification process at multiple dose, focus, mask biases, etc (using the variables that represent a substantial portion of the process variability). While this may be practical for engineering activity, it is not a practical solution for production, especially in a high part number environment.

For this reason we have explored alternate solutions to protect against process variability - while also focused on minimizing simulation time. We have investigated a variety of techniques, including the use of aerial image parameters to flag sites that might be sensitive to changes in dose and a MEEF check based on biasing of the OPC layer to reflect mask variations. All of these techniques represent shortcuts as compared to simulations of the full chip at multiple process conditions, and thus savings in CPU time. However, use of these short cuts can have several down-sides: first, increased risk of missing a real error, and second, increases in the number of false errors reported.

Use of aerial image parameters to flag errors has been previously reported. Both advantages and disadvantages arise from the fact that only the optical model, and not the resist model, is being considered. In a situation where the resist model is inadequate (e.g. where the simulation is extrapolating beyond the parameter space used to calibrate the model) it may be advantageous to use aerial image parameters, since simulated CD will be inaccurate. On the other hand, use of aerial image to flag errors can have a large false error rate - if one sets the fail limits high enough to flag the errors occurring due to model inadequacy, one will also flag many geometries that that have no problems. Although missing real errors is more serious, a high number of false errors is also unacceptable in a production environment.

The challenge is to find methods to make the short cuts as selective as possible, so that they will flag all potentially failing sites, without flagging too many false errors — sites which have an adequate window to allow for process variability.

We will discuss a methodology for evaluating the advantages of these short-cuts with respect to run times, as well as their limitations, and for optimizing the trade-off between additional simulations and risk of missing an error.

6521-53, Poster Session

New dimensions of control for optical proximity correction

J. C. Word, J. L. Sturtevant, N. Cobb, T. M. Donnelly, D. Dudau, L. Hong, P. J. LaCour, Mentor Graphics Corp.

Optical Proximity Correction has proven to be a critical enabler for semiconductor manufacturing below 130 nm design rules. Continuous improvement in process model accuracy coupled with simulations anchored to input polygon shapes and user defined fragmentation of those shapes has enabled remarkable wafer-level pattern fidelity under nominal manufacturing conditions. Increasing pattern density and complexity at lower k1 have led to increased compute demands that have been addressed through distributed processing on multiple CPUs. A new generation of OPC software and associated optimized hardware offers a breakthrough cost/performance entitlement, but also offers unprecedented control over wafer-level pattern fidelity. This paper describes new degrees of control in achieving optimum wafer realization of design intent.

6521-54, Poster Session

SOFT: smooth OPC fixing technique for ECO process

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This paper attempts to reduce the computation cost and complexities of people's tasks during ECO-OPC (Engineering Change Order-Optical Proximity Correction). We first introduce the polygon comparison algorithm to extract segment and offset information in previous work. We then develop the concept of smooth factor and buffer region to bring a smooth transition effect between different OPC-depth regions. Guided by original segment and offset information, we develop effective smooth OPC fixing technique (SOFT) that can handle layout remodification especially three basic kinds of ECO-OPC processes while maintaining other design closure. Our experimental results show that we can achieve up to 80% computation acceleration and successfully overcome the ripple effects of the lithography change and stitch the Regional ECO-OPC result back into the whole layout seamlessly.

6521-55, Poster Session

Extrapolation and portability of physically based photoresist models

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Accurate modeling of optical microlithographic processes is a prerequisite for successful design-for-manufacturing. However, the models used for applications such as OPC are typically descriptive in nature - that is, they accurately describe the response of the system to changes in the inputs, but only over the same range as was used to calibrate the model. An OPC model, for example, will typically be accurate for mask patterns that are similar to the test structures used for the calibration. Whenever a change to the process is made, such as a change in film stack or illumination setting, descriptive models usually must be recalibrated so that they will match the new process.

Physically-based models, such as the models for photoresist materials found in PROLITH, are predictive instead of descriptive. Because these models are based on the physics and chemistry of the imaging materials, they can extrapolate accurately across different process conditions. This paper will examine in detail the predictive ability of several state-of-the-art physical models across multiple dimensions, including varied optical source shape, varied thermal dose, and mask condition. In addition, we will also show results for a study of site-to-site portability, where the model was calibrated at one site, and then applied to predict experimental results at another site with different process equipment. Portable models that can accurately predict across different process conditions and even site-to-site reduce the calibration burden currently required for DFM.

6521-56, Poster Session

Feedback flow to improve model-based OPC calibration test patterns

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Process models are responsible for the prediction of the latent image in the resist in a lithographic process. In order for the process model to calculate the latent image, information about the aerial image at each layout fragment is evaluated first and then some aerial image characteristics are extracted. These parameters are passed to the process models to calculate wafer latent image. The process model will return a threshold value that indicates the position of the latent image inside the resist, the accuracy of this value will depend on the calibration data that were used to build the process model in the first place.

The calibration structures used in building the models are usually gathered in a single layout file called the test pattern. Real raw data from the lithographic process are measured and attached to its corresponding structure in the test pattern, this data is then applied to the calibration flow of the models.

In this paper we present an approach to automatically detect patterns that are found in real designs and have considerable aerial image parameters differences with the nearest test pattern structure, and repair the test patterns to include these structures. This detect-and-repair approach will guarantee accurate prediction of different layout fragments and therefore correct OPC behaviour.

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6521-57, Poster Session

Double pattern EDA solutions for 32-nm HP and beyond

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The fate of optical-based lithography hinges on the ability to deploy viable resolution enhancement techniques (RET). One such solution is double patterning (DP) as demonstrated in the flow of Figure 1 below. Like the double-exposure technique, double patterning is a decomposition of the design to relax the pitch that requires dual masks, but unlike double-exposure techniques, double patterning requires an additional develop and etch step, which eliminates the resolution degradation due the cross-coupling that occurs in the latent images of multiple exposures. This additional etch step is worth the effort for those looking for an optical extension. The theoretical k1 for a double-patterning technique of a 32nm half-pitch (HP) design for a 1.35NA 193nm imaging system is 0.44 whereas the k1 for a single-exposure technique of this same design would be 0.22, which is sub-resolution. There are other benefits to the DP technique such as the ability to add sub-resolution assist features (SRAF) in the relaxed pitch areas, the reduction of forbidden pitches, and the ability to apply mask biases and OPC without encountering mask constraints.

Similarly to AltPSM and SRAF techniques one of the major barriers to widespread deployment of double patterning to random logic circuits is design compliance with split layout synthesis requirements. Successful implementation of DP requires the evolution and adoption of design restrictions by specifically tailored design rules.

The deployment of double patterning does spawn a couple of issues that would need addressing before proceeding into a production environment. As with any dual-mask RET application, there are the classical overlay requirements between the two exposure steps and there are the complexities of decomposing the designs to minimize the stitching but to maximize the depth of focus (DoF). In addition, the location of the design stitching would require careful consideration. For example, a stitch in a field region or wider lines is preferred over a transistor region or narrower lines. The EDA industry will be consulted for these sound automated solutions to resolve double-patterning sensitivities and to go beyond this with the coupling of their model-based and process-window applications.

This work documented the resolution limitations of single exposure, double exposure, and double-patterning with the latest hyper-NA immersion tools and with fully optimized source conditions. It demonstrated the best known methods to improve design decomposition in an effort to minimize the impact of mask-to-mask registration and process variance. Lastly, it reviewed whether model-based and process-window applications are needed to extend the double-patterning RET beyond the 32nm node.

6521-58, Poster Session

Optimizing gate layer OPC correction and SRAF placement for maximum design manufacturability

J. L. Sturtevant, T. Brist, L. Hong, S. Shang, Mentor Graphics Corp.

Sub-resolution assist features (SRAFs) or scatter bars (SBs) have steadily proliferated through IC manufacturer data preparation flows as k1 is pushed lower with each technology node. The use of this technology is quite common for gate layer at 130 nm and below, with increasingly complex geometric rules being utilized to govern the placement of SBs in proximity to target layer features. Recently, model based approaches for placement of SBs have arisen. In this work, the variety of rule-based and model-based SB options are explored for the gate layer by using new characterization and optimization functions available in the latest generation of OPC verification and correction tools. These include the ability to quantify across chip CD control with statistics on a per gate basis. The analysis includes the effects of defocus, exposure, and misalignment, and it is shown that significant improvements to CD control through the full manufacturing variability window can be realized.

6521-61, Poster Session

Assist features for modeling three-dimensional mask effects in optical proximity correction

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Liberal use of assist features of both tones is an important component of the 45nm lithography strategy for many layers. These features are often sized at lambda/4 on the mask or smaller. Under these conditions, formerly successful approximations of the mask near field using boundary layer methods or domain decomposition methods break down. Rigorous simulations of the mask near field must include a three-dimensional (3D) Maxwell's equation analysis, but these computations are cost-prohibitive for full-chip OPC, RET, and lithographic compliance checking applications.

The purpose of this paper is to describe a simple and computationally efficient method that can improve model fidelity for 45nm assist features of either tone, while still retaining computational simplicity. While the model lacks the generality of a rigorous solution of Maxwell'sequations, it can be well-anchored to the real physics by calibrating its performance to a lithographic TCAD mask simulator. The approach provides a balanced tradeoff between speed and accuracy that makes it a superior approach to boundary layer and domain decomposition methods, while retaining the capability to realistically be deployed on a full-chip lithography simulation. A tentative experiment showed a 17.7% improvement in the critical dimension (CD) fitting errors.

6521-62, Poster Session

Circuit-based SEM contour OPC model calibration

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In order to achieve the necessary OPC model accuracy, the requisite number of SEM CD measurements has exploded with each technology generation. At 65 nm and below, the need for OPC and/or manufacturing verification models for several process conditions (focus, exposure) further multiplies the number of measurements required. SEM-contour based OPC model calibration has arisen as a powerful approach to deliver robust and accurate OPC models since every pixel now adds information for input into the model, substantially increasing the parameter space coverage. To date however, SEM contours have been used to supplement the hundreds or thousands of discreet CD measurements to deliver robust and accurate models. While this is clearly the optimum path for high accuracy, there are some cases where OPC test patterns are not available, and the use of existing circuit patterns is desirable to create an OPC model.

In this work, SEM-contours of in circuit patterns are utilized as the sole data source for OPC model calibration. The use scenario involves 130 nm technology which was initially qualified for production without the use of OPC, but is shown to benefit from model based OPC. In such a case, sub-nanometer accuracy is not required, and in circuit features can enable rapid development of sufficiently accurate models to provide process margin in manufacturing.

6521-63, Poster Session

Boundary based cellwise OPC for standard-cell layouts

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Lithography continues to be the backbone of circuit fabrication. The use of sub-wavelength lithography is needed to continue the progression of technology nodes. To adapt to the optical degradation that becomes exaggerated in the sub-wavelength regime, various resolution enhancement techniques (RET) are employed in mask development. The most prominent type of RET is OPC. Two different forms of OPC exist, ruled based and model based. As IC technology advances into 65nm and 45nm nodes, the need of more aggressive correction demands the accuracy of model-based OPC. There are drawbacks, however, to using model based OPC. The first is the large storage

requirement due to the need of more numerous complex geometries representing the correction. A second problem is the large number of computation hours. This problem will only get worse as the increases in circuit imaging complexity outpace the increase in computation capacity. Another drawback is that the simulation models, although increasingly complex, do not account for all possible sources of printing variation. This can result in actual feature printing to deviate from what the model described, potentially causing imaging failures.

We propose a boundary-based cellwise OPC methodology which can ameliorate these problems for standard cell design. Our approach pre-compute and store the corrected cell layouts where each cell has multiple versions of OPC corrections obtained in the presence of representative environments that model the optical influence of all potential neighboring cells. In a full chip layout, OPC is done cellwise where each cell uses a pre-computed correction based on its neighboring environment. This approach potentially can be more accurate than full-chip OPC. (Full-chip OPC has to sacrifice quality for practical runtime, but the boundary-based approach is only calculated once for a library and therefore has no computation time constraints.) Another advantage of pre-layout OPC correction is that the accuracy of the simulation models can be completely verified before it is applied to full chip layouts. Finally, boundary-based cellwise OPC gives predictable timing. In full chip approach, the delay of a cell is affected by its OPC corrections which can only be determined after full chip OPC. On the contrary, the delay of each OPC version of a cell can be pre-determined. This removes a major source of timing variations.

A representative library of cells was laid out with 45nm gate length and 80nm minimum width for metal1 layer. Each cell has 48 versions of OPC according to various representative neighboring features. Results also show the metal1 layer of cells has more influence from their neighbors than poly and via layers. After cell placement, instead of doing full-chip OPC, we performed cellwise OPC using pre-computed corrections. Finally, we ran full-chip optical simulation to determine the edge placement errors (EPE). Results are very promising: the average EPE for all metal1 features in 100 layouts is 0.731nm which is less than 1% of metal1 width of 80nm.

6521-64, Poster Session

Statistical analysis of gate CD variation for yield optimization

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A new method for analysis of variation and yield across the whole chip is presented. This method takes into account the stochastic distribution of the input process parameters such as focus and exposure, and performs simulations of the design at the extreme points of the process window. Using a robust model to extrapolate the points within the process window, a full distribution of CDs is produced for each gate, which then is analyzed to provide information about both the individual gate and the variation across the chip.

An advantageous aspect of the presented analysis is that only a small number of simulation data points are required, and thus the analysis can be applied to a full chip. Simulations are performed through focus and exposure, but only simulations at the extreme points of the process window, in additional to nominal values are required. CD values across the full range of six sigma are then extrapolated using a model presented by Mack and Byers. Although this analysis can be applied to any design features, this paper concentrates on the gate layer, and CD measurements are recorded across the device.

A full stochastic distribution is generated for each transistor in the same way as described by Charrier et al. Given a distribution for the process parameters, and also the gate CD response to each combination of these parameters, the overall gate CD distribution is produced. This paper explores the analysis that is made possible by generating the distributions for all of the transistors across the chip, rather than for one individual transistor. In particular, we look at the distributions of individual transistor variation and yield. A desirable transistor variation distribution would have a small mean and a tight spread. Additionally, having the actual distribution for transistor yield, rather than an average figure such as ACLV, the sections of the design that give a low yield or high variation can be targeted. One way that hot spots can be identified is with a graphical user interface in the Calibre simulator, Calibre RVE, which produces a histogram of the results and zooms in on transistors in each bin. This analysis allows us to evaluate our OPC for bias, optimize process parameters, and optimize design style. Since the CD response curve to focus and exposure is non-linear, optimization of OPC and input parameters can be non-intuitive, so this method of analysis can provide additional insight.

This paper develops a method for identifying low yield and high variation gates in a layout, and for measuring both the variation across chip and the distribution of transistor variations, while only requiring a small number of simulation points across the process window for each transistor.

6521-65, Poster Session

Minimizing poly end-cap pull back by application of DFM and advanced etch approaches for 65nm and 45nm technologies

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As the feature sizes decrease and the overall design shrinks, it is becoming increasingly difficult to reliably pattern gate line ends, or poly end caps, so that they are able to extend over to the field area without bridging into another adjacent feature. Furthermore, due to the necessary decrease in poly length, the trimming of the lines during the gate etch process is necessary. However, while trimming the gate sidewall, the line end is also trimmed, often at higher rates than the sidewall itself. This investigation focuses on decreasing the poly line end pullback, defined as the tip of the gate past active.

To increase the process window of the photolithography process for poly endcaps and to improve robustness with respect to the gate etch process, several approaches were evaluated. First, an investigation to extend the line end based on proximity was undertaken. Several feature types were evaluated in order to check on how much the line could be extended without bridging into another feature. Secondly, different hammerheads sizes were tested to observe their effect on the line end litho process window. In addition, the impact of hammerheads on the poly line end pullback during etch was investigated.

In parallel, several variants of the poly gate etch process, such as etch chemistries, were tested to observe their impact on the line end pullback. The trim behavior and the natural etch bias of a gate sidewall was compared to the trim behavior of a gate line end when its nearest neighbor was another line end (tip-to-tip trim) or when it was a line (tip-to-line trim). The line end pullback was minimized as a result of changing etch chemistries in the resist and BARC etch as well as changing other etch process parameters.

Finally, to correct for the shortening of the poly line end, the line end was increased by the placement of a hammerhead in the design and the line end was extended as well. However, changing the endcaps by adding hammerheads could have a negative impact on the transistors and the cell stability. An important consideration is to avoid the gate length variation at the active-to-field interface that may arise because the poly line may be coming to an end. A new design with the added hammerheads was electrically tested to confirm that it would not have a negative impact on transistor data, and after this was confirmed, a new reticle with the implementation of hammerheads was implemented.

6521-66, Poster Session

Real-time VT5 model coverage calculations during OPC simulations

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For a robust OPC solution, it is important to isolate and characterize the detractors from high quality printability. Failure in correctly rendering

the design intent in silicon can have multiple causes. Model inability in predicting lithographic and process implications is one of them. Process model accuracy is highly dependant on the quality of data used in the calibration phase of the model. Structures encountered during the OPC simulation that have not been included in the calibration patterns, or even structures somewhat similar to those used in calibration, are some times incorrectly predicted. In this paper a new method for studying VT5 model coverage during OPC simulations is investigated. The aerial image parameters for a large number of test structures used for model calibration are first calculated. A novel sorting and data indexing algorithm is then applied to classify the computed data into fast accessible look-up tables. These tables are loaded in the beginning of a new OPC simulation where they are used as a reference for comparing aerial image parameters calculated for new design fragments. Such new approach enables real time classification of design fragments based on how well covered they are by the VT5 model. Employing this method avoids catastrophic misses in the correction phase and allows for a robust approach to MBOPC.

6521-67, Poster Session

A simple and practical approach for building lithography simulation models using a limited set of CD data and SEM pictures

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Lithography simulation (or OPC) model is generally calibrated with a large amount of SEM CD data measured from standard, regular (isolated and dense) line-shape, T-shape, H-shape, rectangular, and square shape patterns. The simulation model calibrated with these CD data can give an accurate through-pitch, one-dimensional (1D) CD prediction. This calibration approach, however, gives less accuracy for the patterns with two-dimensional (2D) effects such as line-to-tip spacing, line-end shortening, and corner rounding than the 1D accuracy in product layouts.

Another approach for calibrating the model is with limited amounts of SEM pictures of test layouts. This approach, with an aide of software, fits the simulated contours of the test layouts to the contours in the SEM picture until a desired accuracy is achieved. This approach predicts better 2D effects than 1D's.

It could be therefore desirable that the model calibration data with a combination of measured CD data from the standard patterns and product layout SEM pictures for the improved the 2D effect prediction accuracy.

In this work, a simple approach for calibrating the simulation model is developed. This approach calls for a small set of 1D CD data together with layout contours from SEM pictures. The 1D data is composed of the measured CDs of minimum line and space patterns as well as isolated line and space patterns. The SEM pictures for contour calibrations are from the product layouts.

In this approach the small set of 1D CD data is firstly used to calibrate the model. After the preliminary through-pitch accuracy is achieved, the model is used to predict the contour of the product layouts where the SEM pictures are taken. The simulated contours against the SEM pictures are examined and large contour-to-SEM picture mismatch locations are identified. Additional calibration gauges at the locations are then added to the model to improve the prediction accuracy of the 2D effects. This procedure can be repeated several times until desired matching of the predicted and the SEM picture contours is achieved.

This calibration approach has been used for 65 nm lithography process simulations. Hot spots, narrow process window layout patterns, out-of-spec OPC CD locations have been identified and later confirmed from in-line data.

In summary, with a limited set of 1D data and SEM in-line product layout pictures, a simple approach for lithography simulation model calibration is developed. The approach gives improved accuracy for the 2D effect predictions. This model, along with the simulation software has been used for 65 nm layout process window evaluations and OPC recipe improvements. Satisfactory results have been achieved.

6521-68, Poster Session

Accelerating physical verification using STPRL: a novel language for test pattern generation

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In recent decades we have witnessed great improvement in the field of VLSI. Motivated by high demand for sophisticated applications and processes, the IC design field has never been as challenging as it is today. New products and technologies are rolling out every day, and the turn-around time from design to silicon is becoming even more critical. Consequently, technology files and verification code for controlling the novel technologies must also be brought on line quickly. Focusing on physical verification processes, this code might include design rule checking (DRC), optical proximity correction and optical rule checking scripts. As a rule of thumb, all of these programs should be verified against a robust test case before being installed in a production flow.

As a result, designing a comprehensive suite of test patterns for each new technology - capable of covering all design rules and all relevant layouts - in a timely manner is vital. Although it is impractical for test patterns to contain every possible interaction between layers, most of the critical cases can be imported from earlier technologies, after being properly rescaled. Even so, it is still common that large numbers of new test structures must be included, with unique layers and dimensions required for the newest offering. For a full set of technology files, drawing such test patterns can be time consuming and tedious. A more efficient solution is to automate the generation of these sorts of new test cases.

In this work we are providing a solution for dramatically reducing the design time for test-pattern development by introducing STPRL, a standard rule-scripting language for generating test patterns. Our new methodology also enables portable test pattern scripts. This feature allows layouts for different technologies to be generated from the same STPRL script, after adjusting a few variables relating to critical dimensions. As a result, migrating technology files from one generation to the next becomes straightforward and more-easily maintained. STPRL is a Tcl based language that employs the Tcl/Tk functionality available in Calibre simulator tool to generate GDS file formats with pre-programmed test structures.

Along with STPRL we discuss its compiler, the test pattern generator (TPG). TPG provides the user with a library of predefined functions that can be used to manipulate test structures. Programming custom-made functions for more elaborate test structures is straightforward, either by combining different predefined functions or adding new functions to the main library.

STPRL and TPG have been tested and deployed in a production design flow, creating test patterns to support DRC for a 65nm family of technologies. Besides huge reductions in man power and design time required to create the new test patterns, the patten-generation scripts readily extendible to future technologies with new parameters or new design rules.

6521-69, Poster Session

DRC and mask-friendly aberration and polarization monitors

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This paper proposes modifications to aberration and polarization monitors to create parameter specific and parameter sensitive process monitor layouts that pass DRC and mask making checks. Self-interferometric pattern and probe monitors as presented by Robins and McIntyre have been proven highly sensitive to manufacturing nonidealities. These patterns consist of non-Manhattan designs that do not pass DRC or mask making checks. Their quantitative interpretation also requires over exposure sequences, special SEM reading of dots instead of linewidth, and separate calibration of the EM performance of the central reference probe. The principles expressed in the original aberration monitors might, however, be integrated into more traditional layouts to create more processing acceptable patterns that retain unusually high and parameter specific responses.

This paper explores the trade-off in sensitivity as the theoretically most sensitive patterns are morphed in to circuit like layouts. Various levels of pattern modification and SEM reading techniques including contact hole presence and CD variation are considered. These vary from patterns that pass mask making checks used in scribe lines to chip embeddable circuit like layout patterns. The goal is to produce new styles of circuit like layouts that are several times more sensitive and parameter specific than typical circuit layouts. Their layout standard nature would make them very useful in calibrating optical parameters in OPC by SEM and eventually electrical testing.

A number of variations of the focus and coma pattern and probe monitors are presented, as well as the polarization monitors, each of which are many times more sensitive to the tool non-idealities than typical layouts. The patterns are processed with an OPC treatment and their sensitivities to the aberrations are investigated as post-OPC layouts. This result reveals whether OPC might amplify or reduce layout sensitivities to aberrations.

A flow is established to modify the monitors to allow them to pass the DRC and mask making checks. At the points of failure, edges are selected to be moved to create the new pattern which passes the checks. Different patterns are generated depending on edge fragmentation and edge choice for adjustment. The patterns are simulated and compared for sensitivity.

Pattern matching of the monitors will be used to estimate similarity to the theoretically sensitive designs, and aerial image simulation will be used to verify design sensitivity relative to typical circuit layouts. A variety of these patterns will be placed on a future PSM test-reticle for experimental confirmation.

6521-70, Poster Session

Mask manufacturinng rules checking (MRC) as a DFM strategy

P. D. Buck, R. Gladhill, Toppan Photomasks, Inc.; J. Straub, Toppan Photomasks, Inc

Mask Manufacturing Rules Checking (MRC) has been established as an automated process to detect mask pattern data that will cause mask inspection problems. This methodology is unique from the Design Rule Checking (DRC) or Design for Manufacturing (DFM) checks typically performed before sending pattern data to the mask manufacturer in that it examines the entire mask layout and the spatial relationship between multiple patterns in their final orientation, scale, and tone. In contrast, DRC and DfM checks are usually performed on individual pattern files. Also, DRC and DfM checks are not always performed after all pattern transformations are complete, and errors can be introduced that are not caught until the mask is eventually printed on wafers. Therefore, MRC can often be the only comprehensive geometric integrity test performed before the mask is manufactured and the last opportunity to catch critical errors that might have disasterous consequences to yield and consequently to product schedules.

In this paper we review the concepts and implementation of MRC in a merchant mask manufacturing enterprise and introduce methods to empower DfM decisions by mask customers based on MRC results.

6521-72, Poster Session

DFM approach to APSM 2nd-level mask patterning

S. E. Henrichs, M. Chandramouli, Intel Corp.; M. Tsai, Synopsys, Inc.

Alternating phase shift mask (APSM) patterning can significantly improve the wafer lithography process window compared to other lithography techniques like binary or embedded phase shift (EPSM)patterning. A significant barrier to implementing APSM in volume production has been the expense of the mask. The cost of the mask is driven partially by the complexity of the two layer process flow required to make the mask. The second level pattern must open the resist over pi apertures to allow quartz etching while reliably protecting the zero apertures from etching. The process window is limited by the CD control, overlay control, and 2nd level pattern fidelity.

Typically, the 2nd level pattern is generated by upsizing the first level pattern of the pi apertures by a small amount in order to provide some overlay margin. The amount of upsizing is limited by the smallest chrome feature present in the pattern. This scheme produces a pattern with the minimum overlay tolerance over the entire mask even though a typical pattern may only have a small number of minimum chrome locations that require this. A better way to generate the 2nd level pattern would be to take advantage of larger chrome structures when present in order to improve the overlay tolerance in these locations. With a simple set of rules, it is possible to generate a 2nd level pattern with up to ten times reduction in the number of corners, as measured by the number of vertices in the pattern, and minimize the number of marginal patterns in the design. This also has the beneficial side effect of significantly reducing the file size of the 2nd level pattern which can reduce the write time on some writers.

Existing design rules can be exploited or additional rules imposed that can further improve the capability of the 2nd level APSM process. For example, if the minimum chrome width design rule is larger for vertically oriented feature compared to horizontal, then the 2nd level can be sized by different amounts in the two directions which moves the 2nd level corners further away from the first level. The right set of mask design rules can enable the use of lower fidelity writer for 2nd level patterning which can significantly reduce cost.

This DFM approach to generating the 2nd level APSM pattern can significantly reduce the number of process window limiting locations on a the mask without impacting the lithography performance in the fab. The improved margin can increase yield and may even enable a less capable/expensive patterning tool to be used for 2nd level patterning. Both effects reduce the cost of APSM masks making this patterning technique more attractive for high volume wafer manufacturing.

6521-73, Poster Session

Cell-based aerial image analysis of design styles for 45-nanometer generation logic

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Line/space dimensions for 45nm generation logic are expected to be 65nm at a 130nm pitch. Patterning regular grating-like structures has been demonstrated with a 0.93NA scanner using off-axis illumination and an aPSM reticle. More complex layout styles were studied, including grating-like lines with gaps, regular patterns with bends, and finally irregular patterns mimicking traditional random logic. These design styles were studied with rules for 90nm, 65nm, and 45nm generations.

The OPC / aerial imaging software used was the Sequoia Cell Designer [1], a model-based DFM tool. Cell Designer incorporates advanced optical models for accurate prediction of lithography effects in high NA systems including vector effects, polarization, dispersion, aberrations, etc. It is a true DFM tool as it provides a link from the process and layout to electrical performance by generating physically accurate electrical models for as-printed distorted layouts [2]. Simulations were run through focus, typically to +/- 0.1um of defocus.

The aerial images were calculated on layout both with and without OPC. For regular layout with no bends, better results were obtained in several cases without OPC. The OPC caused the end gaps to bridge unless the gap was increased from 1x to 1.5x.

For the layout style having bends, none of the non-OPC aerial images were suitable. Even with OPC, marginal results were found at 65nm and most dimension combinations failed at 45nm. This indicates that conventional design rules are not adequate for more complex shapes, and additional rules are needed for bent lines. Finally, for traditional random style layout, the shapes were not recognizable at 65nm and 45nm without OPC. Even with OPC, in several cases it was not possible to get aerial images without severe necking or bridging. 45nm results are shown in Figures 1a and 1b, comparing bent lines with 1x lines/spaces and 1.5x lines/spaces.

The aerial images were confirmed by experimental results from patterned wafers. An ASML XT1400 scanner with NA=0.93 and cQuad-30 illuminator was used with attenuated Phase Shift masks from Toppan's Dresden mask shop.

Our conclusion is that for a given lithography condition, design style has the dominant role in determining the fidelity of printed images. More

regular layout gives more predictable, successful results with less aggressive OPC treatment needed. It is expected that cell-based OPC, coupled with highly regular layout, will become increasingly used by design teams to reduce their risk of patterning-induced systematic yield problems.[3]

1. SEQUOIA Cell Designer Manual, SEQUOIA Design Systems, 1998-2006

2. Valery Axelrad, Andrei Shibkov, Gene Hill, Hung-Jen Lin, Cyrus Tabery, Dan White, Victor Boksha, Randy Thilmany, “A Novel Design-Process Optimization Technique Based on Self-Consistent Electrical Performance Evaluation”, SPIE Microlithography 2005, Santa Clara, USA.

3. Michael Smayling, “Test Structures, Test Chips, In-Line Metrology and Inspection,” DFM Tutorial, DAC 2006, San Francisco, USA.

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