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8322-01, Session 1

Progress of EUV lithography toward manufacturing

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EUV lithography is a candidate for device manufacturing for the 16nm node and beyond. To prepare the insertion into manufacturing, the challenges of this new technology need to be addressed. Therefore, the ASML NXE:3100 pre-production tool was installed at imec to replace the Alpha Demo Tool (ADT). Since the technology has moved to a pre-production phase, the understanding of the EUV technology needs to become more mature and it needs to demonstrate to meet the strong requirements for sub 16nm devices.

In this paper we discuss the CD uniformity and overlay performance of the NXE:3100. We focus on the effect of EUV specific contributions to CD and overlay control that were identified in earlier work on the ADT. The contributions originate from the use of vacuum technology and reflective optics inside the scanner, which are needed for EUV light transmission and throughput. Because the optical column is in vacuum, both wafer and reticle are held by electrostatic chucks instead of vacuum chucks and this can affect overlay. Because the reticle is reflective, any reticle (clamp) unflatness directly translates into a distortion error on wafer (non-telecentricity). For overlay, the wafer clamping performance is not only determined by the exposure chuck, but also by the wafer type that is used. We will show wafer clamping repeatability with different wafer types and discuss the thermal stability of the wafer during exposure.

8322-02, Session 1

Insertion strategy for EUV lithography

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The first extensive use of extreme ultraviolet (EUV) lithography in logic manufacturing is targeted for the 14 nm node, with possible earlier application to 20 nm node logic device back end layers to demonstrate the technology. Use of EUV lithography to pattern the via-levels will allow the use of dark field EUV masks with low pattern densities and will postpone the day when defect-free EUV mask blanks are needed. Matched machine overlay of via levels patterned with EUV lithography to metal levels patterned with 193-nm immersion lithography will likely require distortion matching of the more mature (sophisticated control) 193-nm immersion lithography tools to the less mature EUV lithography exposure tools. The quality of the imaging at the 14 nm node with EUV lithography is considerably higher than with double-dipole or double-exposure double-etch 193-nm immersion lithography, particularly for 2D patterns such as vias, because the k1-value when printing with

0.25 NA EUV lithography is so much higher than with 1.35 NA 193-nm lithography and the process windows with EUV lithography are huge. Other advantages of EUV lithography include a return to the use of conventional OPC for mask pattern correction (simple biasing of features) and the absence of forbidden pitches.

In this talk, the status of EUV lithography technology as seen from an end-user perspective will be summarized and the current values of the most important metrics for each of the critical elements of the technology will be compared to the values needed for the insertion of EUVL into production at the 14- and 20-nm technology nodes.

8322-03, Session 1

Compact EUV radiation sources

W. Barletta, Massachusetts Institute of Technology (United States)

The potential future viability of compact accelerator sources for uses in commercial EUV lithography applications is presented.

8322-04, Session 1

Pattern collapse mitigation strategies for EUV lithography

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In this study, a comprehensive approach towards assessing pattern collapse challenges and solutions for EUV resists beyond the 14nm node is undertaken. The fundamental forces that drive pattern deformation are reassessed in order to propose a generalized design criterion for EUV photoresists and aqueous surfactanated rinses. Additionally, photoresist formulation casting at elevated speeds has been identified as a usable knob to mitigate pattern collapse for EUV photoresists. A discussion of the potential factors responsible for this effect is included. Furthermore, ultimate pattern collapse solutions such as solvent drying utilizing pressurized fluids (liquid or supercritical CO_2) are exemplified for sub-60 nm pitch EUV patterning. In parallel, alternative EUV integration schemes that use metal-based hardmasks (MHM) are studied using a specifically tailored self-assembled monolayer (SAM) to prevent delamination-driven pattern collapse due to resist-hardmask interfacial adhesion failure. Finally, the marginal image transfer of 40 nm pitched L/S of ultrathin EUV resist into a SiARC-underlayer stack appears to be gated by the EUV resist resolution limit and the reduced film thickness budget. An alternative method for achieving improved post-etch line width roughness (LWR) with an ultrathin MHM-based integration scheme is demonstrated.

8322-05, Session 2

Modeling and simulation of acid diffusion in chemically amplified resists with polymer-bound acid generator

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The development status of extreme ultraviolet (EUV) lithography approaches the requirements for the high volume production of

semiconductor devices with the minimum line width of 22 nm. It has been demonstrated using a conventional non-chemically amplified resist that the resolution of EUV lithography reaches 11 nm. However, not only resolution but also sensitivity is required for resist materials used for high volume production. Therefore, the chemical amplification is an indispensable technology. However, the acid diffusion has been a problem in the development of high resolution chemically amplified resists. Recently, the acid generator, the anion of which is bound to the polymer through a covalent bond, has attracted much attention. It has been demonstrated that the chemically amplified resists with polymer-bound acid generators shows not only high resolution but also high sensitivity comparable to chemically amplified resists with conventional acid generators. This fact indicates that the deprotection of resist polymers is induced without the diffusion of anions. The chemically amplified resists with polymer-bound acid generators are a promising platform for nanofabrication below 16 nm node. In this study, we modeled and simulated the acid diffusion in chemically amplified resists with polymer-bound acid generators. The characteristics of deprotection under the condition that the anions are bound to the polymer is discussed. On the basis of simulation results, the feasibility of <16 nm fabrication with chemically amplified resists is discussed.

8322-06, Session 2

Contact edge roughness: effect of photo-acid generator on EUV resist

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In future, EUV lithography will play vital role in the lithography world. One of the main challenges for developing EUV resist is to satisfy ITRS targets for sidewall roughness. The majority of works have been devoted to the sidewall roughness of resist lines, the so-called line edge (or width) roughness (LER/LWR) issue. However, lithographic features are not characterized by line patterning only but also circular patterning such as contact holes and via, which are opened for connecting transistors to metal circuit layers. The roughness of contact holes (contact hole or edge Roughness, CHR/CER) may affect the Source/Drain (S/D) contact resistance and the saturation current, and may cause time-dependent dielectric breakdown (TDDB) due to the reduction of the space between contact and gate in a transistor [1-2]. Despite these device effects, the characterization of CER and the study of process and material effects on it are still in a preliminary phase [3].

In previous works, we developed a characterization methodology for CER [4] and applied it to study the effects of exposure dose in a EUV resist [5]. With the continuation of our previous work, we extent our study to analyze the effects of dose on CER for a new EUV resist in three formulations having different photo acid generator (PAG) concentrations.

First, the trends of experimental results are in conformity with previous analysis [4]: CD, RMS and   increase with dose while CD variation decreases and saturates over a critical dose (the roughness exponent remains fixed at ~0.65 in all cases). Thus, it seems that in CER we can improve simultaneously the sensitivity and roughness (contrary to LER) at the cost of having increased CD variation. To explain this behavior, one can argue that the sensitivity increase (lower doses) leads to smaller CD and shorter contact edge lengths and therefore to a decrease of rms. However, modeling results show that this effect can provide only a partial explanation of experimental results. The role of the relatively high acid diffusion length (~10nm) with respect to the small CD is also discussed in view of similar considerations in LER [6]

Secondly, the increase in PAG concentration for doses leading to a fixed CD (~45nm) is found to result in a) increase in CD variation, b) slight decrease and saturation of rms value and c) no important effect on correlation length and roughness exponent, Inspection of power spectra reveals the importance of low frequency components in the above dependencies.

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[3] S. Jun, et al., Proc. Of SPIE Vol. 6518 (2007) 65183T-1

[4] Vijaya-Kumar M K, et al Microelectron. Eng. 88 (8), (2011) pp. 2492-2495

[5] Vijaya-Kumar M K, et al Proc. of SPIE Vol.7971, (2011) 79710Q-1

[6] Van Steenwinkel. D et al JVST-B:Nanostructure and microelectronics 24 (1), (2006)pp. 316-320

8322-07, Session 2

Mechanisms of LER degradation in ultrathin EUV resists

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The need to simultaneously improve the resolution, line-edge-roughness (LER) and sensitivity of EUV resists remains one of the most critical challenges in EUV lithography. While the theoretical limitations to the RLS trade-off have been well documented, this work has all been done at constant film thicknesses. Yet, we have found that decreasing film thickness causes degradation in LER. We previously studied the performance of four resists as a function of film thickness (two CNSE and two commercial resists) and found the LER degrades at a rate inversely proportional to the square root of thickness.1

Here, we present a mechanistic study into the cause of this LER degradation in thin films. We have studied four properties of resist films to better understand this thin-film LER problem: Substrate Interaction, Optical Density, Glass Transition and PAG Attachment. We have varied each of these properties systematically and compared the LER at film thicknesses of 90, 60, 40, 30 and 20 nm.

Substrate Interaction. One of the conclusions from our 2010 underlayer program was that the matching of CTE between resist and underlayer is very important in determining adhesion, line collapse and LER. Specifically, we found that the use of an underlayer can give ~1 nm improvement in LER over a primed silicon substrate. Here we have studied the effect that different substrates can have on the relationship of LER degradation as a function of film thickness.

Optical Density (OD). One variable we will explore is EUV optical density. The basic idea is that as resists get thinner, the total amount of light absorbed by the photoresist decreases. We have designed a series of four resists with similar lithographic properties (Rmin, Rmax, Eo), yet with a wide range of fluorine content (Figures 1A & B). We have evaluated these resists lithographically and have compared the LER degradation through film thickness as a function of OD.

Glass Transition (Tg). It has been well documented that the Tg of polymeric films can vary dramatically between film thicknesses of ~250 nm and 50 nm. We have designed four resists with similar lithographic properties (Rmin, Rmax, Eo), yet with a wide range of Tg (Figures 1C & D). We have evaluated these resists lithographically and have compared the LER degradation through film thickness as a function of Tg.

PAG Segregation. Lastly, we consider the possibility that the LER degradation in thin films may be due to PAG segregation. Since PAGs are known to segregate to different depths in resist films, we consider the possibility that the total volume of the film may influence the concentration that is able to develop at the top and bottom interfaces. We have evaluated three resists prepared by a commercial supplier that compares thin-film degradation of a polymer-bound PAG, a blended PAG, and a champion control resist. The LER performance of each resist has been compared as a function of film thickness.

8322-08, Session 2

Optimization of low-diffusion EUV resist for linewidth roughness and pattern collapse on various substrates

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The development of low acid diffusion chemically amplified resists has enabled the resolution of 20nm hp features at doses less than 15mj using EUV technology [figure 1]. However, linewidth roughness (LWR) and pattern collapse remain difficult challenges for EUV resists. This paper will focus on key parameters to optimize LWR such as PAG density and EUV resist absorption. The authors will also report on key parameters such as resist film quantum yield and its key role in LWR improvement. Another very important factor to improve LWR and pattern collapse is optimization of the underlying substrate. This paper will discuss the performance of our resists on primed Si, organic underlayers, and Si-containing underlayers. Figure 2 illustrates dramatic differences in substrate selection on resist performance. For Si underlayers, we see good overexposure performance for 28nm hp patterns with no line collapse down to 20nm CDs. For organic underlayers, we see collapse at the same condition. For Si, we see dramatic resist mottling and poor LWR. Measurement of key surface parameters such as water contact angle and coefficients of thermal expansion will be related to the relative pattern collapse margin and also the contribution to LWR. Lastly, we will discuss pattern transfer through these substrates and the relative improvements in LWR possible through etch recipe optimization.

8322-09, Session 2

EUV resist materials for 20nm and below half-pitch applications

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Extreme ultra violet (EUV) lithography process is one of the most promising candidates for 22 nm half pitch and below generation device manufacturing. It is supposed that implementation of EUV lithography to high volume manufacturing would start at 20 nm or more smaller pitch generation.

Many papers reported that it is important to reduce "resist blur" to achieve good resolution. Recently, very small blur numbers close to non-CAR resist system were found in polymer bound PAG type resist, having very short acid diffusion property coming from the bound PAG structure essentially. Additionally, it was found that polymer bound PAG type resist system has an advantage in dissolution contrast compared to polymer and PAG blending type resist system. However, we could not obtain 20 nm half pitch resolution with polymer bound PAG type so far.

Today, resist blur can easily be controlled with PAG design, therefore, new strategies are needed to obtain further tight pitch resolution. We already found that pattern collapse prevents tight pitch resolution by EB-lithography with polymer bound resist system. Pattern collapse can be avoided with reducing capillary force, improvement of adhesion of resist pattern and substrate, and enhancement of pattern hardness. This paper will report detail study to suppress pattern collapse, and some latest resist materials lead out from this study.

8322-10, Session 2

EUV resist development for 16nm half-pitch and beyond

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Extreme ultra-violet (EUV) lithography is targeted for 10nm logic technology node HVM in 2015 followed by 7nm node in 2017. Next-generation EUV resists are required to improve resolution limit down to less than 16 nm half pitch. To achieve such a performance, innovative materials such as molecular glass, polymer bound photo-acid generator and low acid diffusion length photo acid generators (PAG) are required. In this study we focused on innovative PAG material development through the investigation of PAG acid diffusion length and PAG anion structure. Based on the results of this study, PAG plays a key function in order to resolve 16 nm half pitch and beyond. We are hopeful that these results would contribute to the EUV resist development at sub-16nm half pitch generation.

8322-08, Session 3

EUV mask multilayer defects and their printability under different multilayer deposition conditions

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Defect control in both mask making and wafer processing becomes increasingly critical when using extreme ultraviolet (EUV) pre-production tools. Much effort has been devoted to studying the printability of blank defects on wafers using native defect masks and programmed defect masks. The defect dimensions from metrology tools can be used to characterize their printability behavior on wafers. Although the defect dimensions can be characterized using currently available metrology tools, native and program phase defects cannot be realistically characterized without knowledge of the defect-induced changes in the structure of the deposited multilayer. Researchers have typically tried to predict the phase effects of multilayer and substrate defects based on simple growth models or measured multilayer deformation shapes.

In this paper, we describe the characterization of native phase defects in the multilayer during the manufacturing of EUV mask blanks. We prepared and characterized programmed bump and pit defects of various dimensions using e-beam patterning technology and investigated multilayer decoration on them. The multilayer on native and programmed defects was prepared using several different deposition conditions to study the printability of native and programmed defects under different multilayer deposition conditions. Printability studies also compare both native and programmed defects. Transmission electron microscopy (TEM) was used to study changes in the multilayer ML profile, while SEMATECH's actinic inspection tool (AIT) was used to image defects and predict their printability. We show that the printable regions of native defects are different from the regions of programmed defects. Printability characteristics of native defects and programmed multilayer defects will be compared to determine the effects of defect decoration during multilayer deposition.

8322-09, Session 3

Printability study of pattern defects in the EUV mask as a function of hp nodes

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Amplitude defects (or absorber defects), which are located in absorber patterns and multilayer surface, can be repaired during mask process while phase defects (or multilayer defects) are not. Hence, inspection and handling of both defects should be separately progressed. Defect printability study of pattern defects is very essential since it provides criteria for mask inspection and repair. Printed defects on the wafer kill cells and reduce the device yield in wafer processing, and thus all the printable defects have to be inspected and repaired during the mask

fabrication.

In this study, pattern defect printability of the EUV mask as a function of hp nodes is investigated by rigorous EUV simulations, and the results are verified by comparing with EUV exposure experiments. For higher 2x and 3x nm hp nodes, we use ASML ADT and NXE3100 to verify simulation results. However, for lower 2x nm hp and below, it is not easy to obtain wafer exposure results due to the scanner resolution limit. In this case, we use the actinic inspection tool (AIT) and also micro-field exposure tool (MET) in LBNL (SEMATECH) which apply the concept of high NA and off-axis illumination. As a result, we defined size of defects to be controlled in each device node.

8322-10, Session 3

Smoothing layers for EUV substrate defectivity mitigation

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The defectivity of extreme ultraviolet (EUV) mask blanks poses one of the main obstacles in the realization of EUV lithography. The majority (>80%) of defects-mostly pits, with some scratches and embedded particles-are present on the substrate, all of which originate from substrate chemical mechanical polishing (CMP) and cleaning. Over the past few years, mask suppliers have been able to gradually reduce CMP-induced substrate defectivity, but the defect numbers (at a 50 nm detection sensitivity) are still too high. Note that numerous defects do not show up during substrate inspection (with the Lasertec M7360), but are detected only after they are decorated by multilayer deposition. Printability simulations have shown that pit/bump defects need to be less than 1 nm deep/high to be unprintable. The fact that CMP has not yet been able to yield EUV substrates with low substrate defect counts highlights the challenges of polishing quartz or low thermal expansion material (LTEM) substrates, both of which are oxides. Cleaning the substrates to remove the particles adds to the pit defect count, primarily the result of the physical impact of megasonic-induced cavitation on the oxide surface.

Hence to mitigate substrate defects, smoothing layers made of different materials and processed through alternative techniques must be evaluated. SEMATECH will report on the evaluation of a few techniques that are still in the research phase but may be promising approaches to mitigate substrate pits and scratches. Among them, we report results for smoothing layers comprised of vapor-deposited thin films of amorphous silicon, chosen because of the industry's familiarity with Si. We evaluate a novel polymer-based non-abrasive CMP process where the idea is to deposit a thin film of a-Si on the substrate and determine whether the CMP process generates any pits or scratches on the surface. We also discuss the results from a study of curvature-dependent surface migration of Si upon vacuum annealing as a means to smooth surface asperities. Additionally, results of cleaning experiments on a-Si coated EUV substrates to determine whether fewer pits are added by megasonic cleaning are described. Since Si is a harder material than quartz, it is likely to be more resistant to cavitation-induced pits.

Also, successful results from other exploratory defect mitigation efforts such as spin coating inorganic resists to smooth over surface defects, using a novel non-adiabatic photochemical reaction to selectively etch surface protrusions, and pressing a soft metal to flatten surface asperities via plastic deformation, will be presented. This research aims to find a route to obtain pit-, particle-, or scratch-free EUV substrates with a high enough yield to help pave the way to EUV mask blank commercialization.

8322-11, Session 3

Closing the gap for EUV mask repair

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For reticle production mask repair has become a fundamental part of the production process. The transition from 193 nm to EUV has dramatic challenges especially for performing successful mask repair. Since the EUV-reticle is used as mirror and no longer as transmissive device the severity of different defect types has changed significantly. Furthermore the EUV-reticle material stack is much more complex than the conventional 193nm reticle. As a consequence repair capability is required for defects in the absorber layer and for defects in the mirror. This expands the field of critical defect types even further and requires not only repair capability for smaller defects but also for new material stacks and multilayer defects.

One of the most promising concepts for EUV reticle defect repair is focused electron beam induced processing. This technology employs a high resolution electron beam to induce a local chemical reaction on the EUV mask surface. A suitable precursor gas is dispensed through a nozzle in close vicinity to the incident beam. Depending on the precursor chemistry, a reaction is induced by the electrons, leading to either a deposition caused by fragmentation of precursor molecules or to a reaction between the adsorbed molecules and the substrate material, resulting in volatile products and thus etching of the substrate material. The reaction is confined to the area exposed by the electron beam, so this technique allows high resolution nanostructuring.

From a repair point of view a EUV mask can be separated into 3 layers: The absorber, the capping layer and the multilayer. Different as for 193 nm reticles defects can propagate through these layers, which makes the detection and the repair complex or complicated or impossible if conventional methods are used. In this presentation we will give a brief introduction into ebeam based mask repair. An overview of different defect types show that from a repair point of view all defects condense into two defect types. One is a defect in the absorber itself, which is almost impossible to repair if 193nm repair technology is applied because of parasitic degradation and collateral damage of the capping layer if 193nm repair technology is applied. The second type distorts the mirror quality which has two delicate implications. First the defect is almost invisible in SEM review and until today the repair of a EUV mirror itself.

In this presentation we will give an overview of key features of our e-beam based repair tool, discuss EUV repair requirements and demonstrate current repair performance. It will be demonstrated, by which methods the smooth multilayer defects can be visualized and located. Furthermore a new repair strategy will be introduced and demonstrated on real defects. The repairs will be verified by wafer prints.

8322-12, Session 3

A next-generation EMF simulator for EUV lithography based on the pseudo-spectral time-domain method

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The finite-difference time-domain (FDTD) method, which is widely used in DUV lithography simulation, turns out to be quite unsuitable for EUV lithography simulation because of the limitations discussed below. These limitations are all overcome by the pseudo-spectral time-domain (PSTD) method.

The thicknesses of the molybdenum and silicon layers in an EUV mirror can be quite arbitrary, for example, 2.78nm and 4.17nm, respectively. Since FDTD employs the finite-difference approximation, in order to achieve second-order accuracy, all the FDTD cells must have the same size. Since it is impossible to fit same-size cells exactly into arbitrarily thick Mo and Si layers, FDTD has to resort to some type of approximation in the Z direction, such as grid snapping, which can lead to large numerical errors.

On the other hand, the PSTD method [1] allows variable cell size in all directions. This means that the PSTD nodes in the Mo and Si layers have different spacings depending on the layer thicknesses. As a result, PSTD can model arbitrary Mo and Si thicknesses accurately.

2. FDTD has large numerical dispersion error whereas PSTD does not:

In the PSTD method, the polynomials used for field interpolation are the Jacobi polynomials. The nature of these polynomials is such that

the convergence is exponentially fast. Once the field within each layer is approximated by an expansion in these polynomials, the spatial derivative of the field is calculated by direct differentiation of the polynomials themselves, without using any finite-difference approximation. As a result, PSTD has very small numerical dispersion error. This is of crucial importance in EMF simulation for EUV lithography, since the multilayered mirrors are very delicate resonant structures which require high accuracy to simulate properly.

3. FDTD has difficulty in modeling buried defects whereas PSTD does not:

When a buried defect is present in a multilayered mirror, the layer interfaces are deformed in the Z direction so as to become non-planar. Since the rectangular FDTD cells cannot fit the non-planar layer interfaces nicely, FDTD has to resort to some type of average permittivity approximation. However, such an approximation is known to be very inaccurate unless the cell size is extremely small, which would make the FDTD simulation very slow.

In the PSTD method, the buried defect is modeled simply by deforming the PSTD cells into a non-planar shapes to fit nicely the non-planar layer interfaces. This way, the boundary conditions on the non-planar layer interfaces are satisfied accurately, resulting in very accurate simulation of the buried defect.

Not only is the PSTD method very accurate, but also it is very fast and memory efficient. This is because it requires relatively few nodes per wavelength, compared to FDTD, to simulate a given 3D mask structure accurately, owing to the exponential convergence nature of the PSTD method. In this paper, the accuracy, speed and memory efficiency of the PSTD method for the rigorous simulation of buried defects in 3D EUV masks are demonstrated by detailed comparison with the FDTD method.

8322-13, Session 3

Analysis of EUV mask multilayer defect printing characteristics

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The paper uses fully rigorous electromagnetic field simulations to investigate the printing characteristics of defects below and inside multilayers of EUV masks effects under various process conditions. Selected simulation results are compared to experimental data. Additional simulations demonstrate possible defect repair strategies.

For the simulations, bump and pit defects are characterized by a Gaussian deformation of the layers at the top and bottom of the multilayer stack. The impacts of the defect on lithographic processes are evaluated by computed aerial images and resist profiles.

First, the imaging of defective multilayers without absorber patterns is investigated. Multilayer defects cause a local reduction of the image intensity in the defect area. The resulting intensity loss is quantified by the integral, the minimum and the width of the intensity dip in the resulting aerial image, and by a specific focus position which causes the smallest intensity of the dip. Even planarized defects without deformation of the top layer may produce a significant intensity loss in the defect area. The most critical focus position of the dip varies with the height of the defect on top and at bottom.

Next, multilayer defects with absorber patterns are considered. The most critical defects involve bridging of resist lines and other imaging artifacts. Smaller defects modify the linewidth of neighboring resist lines and produce asymmetric deformations or tilts of the process windows. The resulting effects are studied for various defect parameters. The paper finishes with the presentation and discussion of selected simulations which demonstrate possible defect repair strategies.

8322-14, Session 4

Development of laser-produced plasma-based EUV light source technology for HVM EUV lithography

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Since 2002, we have been developing a CO2-Sn-LPP EUV light source. By now, our group has proposed several unique original technologies:

(1) High efficient Sn plasma generation, driven by a CO2 laser

(2) Double pulse irradiation scheme for Sn plasma generation

(3) Sn debris mitigation by a magnetic field, a small droplet size

(4) Hybrid CO2 laser system that is a combination of a pulse oscillator and cw-CO2 amplifiers

In this paper, we report the present development status. The theoretical and experimental data have demonstrated the advantage of combining a laser beam at a wavelength of the CO2 laser system with Sn plasma to achieve high CE from driver laser pulse energy to EUV in-band energy. We have several engineering data, which include: 20 W average clean power with 2.5% CE and 7 hours of operating time; and the maximum of 4.8% CE, 93% Sn ionization rate, and 98% Sn debris mitigation by a magnetic field. Based on these data we are developing our first light source for HVM: "GL200E." The latest data and the overview of EUV light source for the HVM EUVL are reviewed in this paper. Part of this work was supported by NEDO.

8322-15, Session 4

High-brightness LPP source for EUVL applications

S. S. Ellwi, F. Abreau, Adlyte (Switzerland)

Adlyte has demonstrated exceptional results including high brightness on it's EUV LPP light source. Adlyte is developing and commercializing two products to address the requirements for mask inspection and metrology. The products are low power source (LPS) and high power source (HPS) based on it's proven technology. The product platform has one main core combined with different optics to satisfy each individual application such as AIMS, ABI, and API. The current system demonstrates high brightness, which has been measured to be around 280W/mm2.sr with power at the source of 12W/2pi. The source can operate at high duty cycle, with a compact footprint and flexible architecture. In order to have the highest uptime an auto fuel-handling system has been designed in. The system has also been designed for high reliability in a high volume manufacturing environment. The fuel used to achieve the highest CE when irradiated with a high power diode pumped solid state Nd:YAG laser in the current product is high speed and frequency tin droplets. To minimize debris being detrimental to the first collector optics a state-of-the-art mitigation system has been developed and tested. In this paper we will discuss the current system performance results.

8322-16, Session 4

Wavelength dependence of prepulse laser beams on EUV emission from CO2 reheated Sn plasma

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Extreme ultraviolet (EUV) emission from laser-produced plasmas (LPP) centered at 13.5 nm is considered to be a leading candidate for the light

source in future lithography systems. Tin is considered the best material for generating this EUV emission as it emits strongly within the 13.5 nm region due to its various ionic states (Sn8+- Sn14+). Highly efficient and low-debris LPPs are a pre-requisite for their use as light sources for EUV lithography. Tin plasmas generate debris that can damage collection optics over time. Techniques to mitigate debris will be needed to extend the lifetime of these components and the system. Optimization of plasma conditions is necessary for increasing EUV emission and enhancing conversion efficiency (CE).1 Improving the source CE is necessary in order to reduce the cost of ownership and hence, develop a commercially viable lithography system for the semiconductor industry. One method to accomplish this is to reheat pre-formed plasma with a laser pulse to enhance EUV emission. This enhancement is achieved by controlling those plasma conditions necessary for optimizing EUV emission. Our recent experiments showed that CO2 laser reheating of pre-plasma generated by Nd:YAG laser provided EUV emission enhancement of ~40%, regardless of the prepulse laser energy.2 It was also found that only a small portion of the reheating laser pulse is absorbed by the pre-plasma before its density decreases below the critical density of the reheating laser. At this point, the reheating pulse is able to penetrate the pre-plasma and instead of reheating, begins ablating directly from the target surface, similar to a single-pulse system. We investigated the role of prepulse laser wavelength on pre-plasma formation and EUV in-band signal enhancement. A 6 ns Nd:YAG laser operating at 1064 nm and 266 nm was used for generating the pre-plasma. The pre-plasma was then reheated by a 40 ns CO2 laser operating at 10.6 μm. The role of prepulse wavelength and energy on EUV conversion efficiency is discussed.

1 A. Hassanein, T. Sizyuk, V. Sizyuk, and S. S. Harilal, Journal of Micro-Nanolithography Mems and Moems 10, 033002 (2011).

2 J. R. Freeman, S. S. Harilal, and A. Hassanein, Journal of Applied Physics 110, (in press) (2011).

8322-17, Session 4

Extreme ultraviolet and out-of-band radiation emission from a tin droplet based LPP source

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Extreme Ultraviolet Lithography (EUVL) is a leading candidate for the future development of smaller and faster microchips with feature sizes of 32 nm or less. Tin laser-produced plasmas (LPPs) are the most promising source of in-band radiation for EUV lithography and inspection applications. However, ions emitted from these LPPs may cause significant damage to components, specifically the collector optics. Tin-droplet targets have the ability to supply the minimum mass required to generate the EUV radiation, leading to substantial decrease in the amount of generated debris. Absolute intensity measurements of the EUV radiation formed using a droplet target, have been recorded. Measurements were recorded over 2 pi steradian with respect to the plasma. The droplet generator, a fully in-house developed system, was synchronised with a Nd:YAG laser at a frequency of 6 kHz. The laser pulse was focused to a power density of approximately 10^11 W/cm2 to maximize in-band emission. The EUV detector employed was a calibrated energy monitor, mounted on a custom built robotic arm. To complement the EUV measurements, out-of-band measurements were simultaneously recorded with a calibrated spectrometer from 200 to 1000 nm.

8322-18, Session 4

Debris concerns for actinic EUV metrology sources

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The continued advancement of extreme ultraviolet (EUV) light lithography as a viable next generation tool hinges upon the development of rapid

and accurate mask inspection tools. The most efficient and economical approach to undertaking this inspection process involves the use of actinic high-brightness sources. Yet, as with the high power EUV sources used for exposing wafers, issues are present with regards to debris mitigation. There is still the need to mitigate energetic ions, energetic neutrals, and out of band radiation. However, metrology sources are more geometrical flexibility and need significantly less power. This provides several opportunities not present in EUV lithography sources. The Center for Plasma-Material Interactions (CPMI) at the University of Illinois at Urbana-Champaign has studied this problem. It has been realized that EUV plasma debris is not just a concern located between the source and the collector optics, but indeed extends to the intermediate focus (IF) and even the projection box. The need to have clean EUV photons at the IF is a challenge that metrology source-collector module (SoCoMo) manufacturers must face in addition to improving brightness levels. This paper serves to address these mitigation issues and present methods by which manufacturers can characterize their sources and take advantage of the need for less power and geometrical flexibility. Data will be presented on the effects of metrology source debris mitigation at reducing energetic flux not only reaching collectors, but also the intermediate focus.

8322-19, Session 5

Printability and inspectability of defects on EUV blank for 2xnm hp HVM application

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The availability of defect free masks remains one of the key challenges for inserting extreme ultraviolet lithography (EUVL) into high volume manufacturing (HVM). Among the defects on finished EUV masks, 75 % originate from the blank level. Therefore, accomplishment of defect free masks will depend on the timely development of defect inspection tools which cover both blank and pattern inspections. 23.1 nm SEVD (sphere equivalent volume diameter) size should be detected by the blank inspection tool to support 35 nm half pitch (HP) application using EUVL. And only one blank inspection tool can cover that range. In this paper, defect printability and inspectability are studied using a state-of-the-art blank inspection tool and scanner using real defects from an EUV blank for 2X nm hp application.

First, an EUV blank is inspected with the blank inspection tool, and then the detected defects are classified based on defect type, size, and height. Our preliminary result shows that blank defects less than 20 nm SEVD can be detected with the current blank inspection tool. This means that we can study the requirement of the blank inspection tool for 2X nm hp application. Second, an EUV patterned reticle is fabricated on the blank with the pattern of line and space (L/S) and contact array for 32 nm and 25 nm HP. And the reticle is exposed using the NXE3100 from ASML. Defect printability on the blank is evaluated and the smallest printable defect size is determined. Some defects are reviewed with SEMATECH-LBNL Actinic inspection tool (AIT). Third, the required specification for a blank inspection tool at 16 nm hp and 11nm hp is simulated to understand if a future blank inspection tool can cover these device nodes. Finally this paper will present requirements for the blank inspection tool and gaps for successful EUV implementation for device integration using EUV lithography.

8322-20, Session 5

Closing the infrastructure gap: status of the AIMS EUV project

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The EUV mask infrastructure is of key importance for a successful

introduction of EUV lithography into volume production. In particular, for the production of defect free masks an actinic review of potential defect sites is required. With such a review it can be decided if a defect needs to be repaired or compensated. It also serves as verification whether the respective absorber or compensational repair with e.g. the MeRiT® tool has been successful, i.e. it closes the control loop in mask repair. To realize such an actinic review tool, Carl Zeiss and the SEMATECH EUVL Mask Infrastructure consortium started a development program for an EUV aerial image metrology system (AIMS EUV). In this paper, we will present the status of the AIMS EUV development and show simulations on the expected system performance. We model the impact of small blank defects to line size and discuss their compensation by absorber resizing and the review of that compensation with the AIMS EUV tool.

8322-20, Session 5

Investigation of the performance of state-of-the-art defect inspection tools within EUV lithography

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EUV lithography is bringing many new challenges in the field of defect inspection. Both in wafer inspection and reticle inspection it is not only the fact that EUVL is targeting smaller dimensions which makes the detection of the defects of interest (DOI) more challenging.

For wafer inspection the high line edge roughness (LER) values that are observed in current EUV resist processes contribute to higher inspection noise, which makes it very difficult to distinguish some defects of interest (= defect that causes a CD shift of more than 10%) from LER.

For (reticle) blank inspection (BI) and patterned mask inspection (PMI), the existence of defects inside the multilayer mirror, which is not penetrable by the wavelengths used by the optical inspection tools, makes it more difficult to locate all printing reticle defects. .

This work investigates the potentials and limitations of the most state-of-the-art inspection tools for both wafer inspection (WI), reticle blank inspection (BI) and patterned mask inspection (PMI). The focus is on 'printing' reticle defects and all 3 techniques will be applied to detect defects on reticles which are specifically designed for this investigation.

Wafer exposures are carried out on 2 EUV full field scanners in IMEC, the ASML Alpha Demo tool (ADT) and the NXE:3100 preproduction tool. These wafers are used to review all defect locations that are reported by WI, BI and PMI and only the defects that end up on the wafer are considered as DOI.

Wafer inspection is performed on the latest generation BF inspection tool from KLA-Tencor, KLA2835. Because the design of the reticle allows a cell-to-cell inspection, it is possible to detect repeating defects, which can be assigned to the reticle. Furthermore the reticle has programmed defects of various sizes (see picture 1), which makes it possible to verify the ultimate resolution of the inspection.

An additional target of this work in terms of WI is to investigate whether it is possible to use simulations to predict which parameters can have a beneficial effect on the inspection sensitivity. These parameters can be changes in the lithographic and underlying stack, but also which inspection settings result in the highest S/N for a certain type of DOI, can be predicted with simulation. Any positive outcome of the simulation will be verified experimentally by EUV exposures

Both blank inspection and patterned mask inspection (die-to-die mode) are performed on the KLA-Tencor Teron600. A technique will be shown to translate results of both these inspections into wafer coordinates, which will make it possible to review these defects on wafer.

The final goal is to come up with a defect population of natural printing reticle defects and for each inspection technique it will be possible to indicate which (types of) defects are likely to be detected and what are

the noise sources limiting detection capability. Additionally the known locations and sizes of the programmed reticle defects can result in additional information about the performance of both wafer inspection and patterned mask inspection.

8322-21, Session 5

Experimental quantification of shot noise contributions to contact hole local CD nonuniformity

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As feature sizes continue to shrink, the discrete nature of light and matter is becoming a significant contributor for the variations observed in lithography in general and for EUV in particular. Owing to the 15x higher energy of EUV compared to ArF photons and similar if not lower exposure doses, the number of photons per unit area in EUV is significantly reduced. If the number of photons per contact hole is considered, the situation is even more dramatic, as the target area of a contact is smaller for EUVL than for ArF patterning. However, the latter argument is less of a concern in the case where the contact hole is fabricated by a negative tone rather than a positive tone process. Since photon shot noise scales with 1/sqrt(#photons), shot noise statistics would favor a brightfield negative tone over a darkfield positive tone process. Indeed, stochastic simulations predict improved local CDU performance for 22nm contact hole structures when printed in EUV with a negative tone instead of a positive tone process.

In this paper, we will compare the local CDU performance of contact holes for both negative and positive tone processes at both ArF and EUV wavelengths. In this way, we will look to quantify the contribution of shot noise to the local CDU performance.

8322-21, Session 5

Scatterometry metrology challenges of EUV

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Extreme ultraviolet lithography (EUVL) offers the most promising patterning technology to be adopted for ultra-deep-submicron devices - 16nm and below. EUV using mirror-based mask with oblique incident angle of light in combination with the small wavelength compared to the mask topography. This causes number of effects that are unique to EUV - such as flare, shadowing and horizontal-vertical (H-V) bias CD offset and an orientation dependent pattern placement error. Increased flare and the shadow effect will decrease the contrast of the aerial image and resulting poor line width control. The H-V bias leads to an ellipticity in the contact hole pattern, CD offset in line space pattern resulting in critical dimension (CD) non-uniformity. The shadowing effects can be corrected by means of OPC and MEEF (reducing the absorber thickness, and/or phase shift concept to improve the image contrast with a thinner absorber stack).

With decreasing grating geometry and increasing demand for metrology of the EUV periodic structures, scatterometry offers diffraction based optical method critical dimensions (CD), side-wall angles, and dimensional characterization. The ability to model complex stacks, generate libraries rapidly and measure CDs and SWAs of targets with multiple pitch, line width (or contact hole) dimensions precisely and accurately enables scatterometry as indispensable metrology technique. The resolution characterization of EUV structures are often limited by narrow lines/holes, obscure angles and very thin film structures. Scatterometry is rapid, precise, accurate and non-imaging technique capable of measuring CD systemic errors resulting from EUV patterning for 14nm nodes and beyond.

In our previous work, we performed calibration of OPC model with full CD profile data for 2D and 3D[1,2] using scatterometry measurements with

rigorous coupled-wave analysis (RCWA) approach. In this paper, we will present the CD, sidewall angle and stack characteristics for H-V bias and placement errors of OPC models through focus by scatterometry. We will also report the precision, accuracy and matching parameters of EUV structures.

The spectral response with combined spectroscopic ellipsometry (SE-90) and reflectometry (NI-SR) showed a strong signal with increased sensitivity and improved measurement quality that help resolve the shape variations and derive profile parameters of interest (CD, side wall angle and height) by scatterometry (figure 1 (a) and (b)). The observed offset of 1.12nm for MCD correlation between horizontal and vertical targets (slope=0.97 and R2=0.9) further illustrates H-V bias (figure 2). The effect of CD and pitch variation in horizontal and vertical directions is also examined and the observed MCD variation is plotted in figure 3 (for 32P64, 40P80, and 50P100). OPC targets of varying CD at fixed pitch (64, 80, 100nm etc.) for lines and contact holes is also examined. The observed MCD variation is plotted in figure 4 (for 31P64 - 36P64). The OPC model characterization for the corrected models will be included. The data collection and analysis will be performed on Atlas tool with NISR and SE-90 measurement techniques.

Finally, comparison of CDU systemic variance across various EUV patterning structures by scatterometry will be validated against reference metrology.

8322-22, Session 6

Impact of EUV mask surface and absorber roughness on LWR

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Extreme UV lithography is still the primary candidate to allow scaling below the 22 nm technological node. Three major engineering challenges need to become available simultaneously for a smooth introduction into high volume manufacturing: [1] source power and reliability, [2] mask readiness, and [3] photoresist performance. For the EUV reticle infrastructure most emphasis has so far been put on obtaining and maintaining low defect masks. However, the reticle flatness requirements for EUV are also very stringent. Recent theoretical studies have indicated that multilayer roughness causes intensity non-uniformities through a speckle effect, which in turn contributes to line width roughness (LWR).

In this paper we seek to experimentally verify these predictions. In addition, we will experimentally verify how programmed absorber roughness is translated to the wafer. As a result the required specifications for both mask multilayer roughness and absorber LWR will be discussed.

For the experimental verification, we engineered an EUV mask having both systematic surface roughness variation and a column containing programmed absorber edge roughness. We exposed this mask on the ASML NXE:3100 at imec. In this paper, atomic force microscopy, reflectivity and SEM inspections on the EUV mask will be compared with the corresponding lines/spaces and contact-hole patterning on the wafer. CD, line edge/width roughness and contact hole uniformity is correlated with mask variability by means of fractal analysis, power spectral density calculation, and other previously developed methodologies. Different illumination settings are used in order to evaluate the predicted impact that source coherence has on the speckle effect.

8322-23, Session 6

EUV mask line-edge roughness

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Extreme ultraviolet lithography (EUVL) brings many unique challenges to mask making, including more stringent line edge roughness (LER) requirements. Imaging always de-magnifies and filters mask LER, but the EUV imaging cutoff frequency is higher than the 193nm optical cutoff; a broader range of LER frequencies is relevant for EUVL. An additional contributor to image plane LER is replicated surface roughness of the mask multilayer. The presence of a new error source translates to even tighter requirements for absorber LER.1 Currently the wafer resist contribution to LER dominates the total wafer budget, but when the resist component is decreased, the mask LER will become relevant. More specifically, the EUV mask absorber LER will need to be reduced to reliably meet the 2013 International Roadmap for Semiconductors line width roughness target of 3.3 nm.2

This paper focuses on evaluating resists modified and deployed specifically to reduce LER on EUV masks. Line edge roughness on the mask is complex and originates from multiple sources.3 Masks were built with resist materials modified to modulate acid diffusion and the final mask LER. In Figure 1, initial resist LER measurements are charted to screen potential resist candidates. On wafer, Resist A is the best performer for LER. Further evaluations were performed to understand which resist has the best roughness performance for EUV. Previous work studying LER has typically focused on wafer performance, but the LER performance on the mask is not often characterized. The analysis relies on final absorber top-down SEM images using a variety of algorithms and filtering techniques. An assessment of best methods for mask LER analysis will be provided and used to judge resist performance.

8322-24, Session 6

Using the transport of intensity equation to predict mask-induced speckle through focus

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The shrinking critical dimensions in the semiconductor industry carries with it simultaneous shrinking requirements on line-edge roughness (LER). With the employment of extreme ultraviolet lithography (EUVL), a significant new contributor to LER is apparent in the form of mask roughness induced LER. Several simplified models have been developed for the prediction of mask roughness induced LER. Currently, these models use 2D aerial image thin-mask modeling through focus to obtain the clearfield speckle pattern (dependent on mask surface roughness and illumination), and combine that with fast 1D aerial image modeling of the image-log-slope (ILS) (dependent on feature type and illumination) to predict the overall mask roughness induced LER. We propose a further simplification and speed enhancement by employing the transport of intensity equation to predict how the speckle pattern will evolve through focus starting from the single 2D aerial image of the speckle at the image-plane.

8322-25, Session 6

Study of megasonic-induced damage on the surface of Ru-capped MoSi multilayer EUV blanks

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EUV patterned masks show better resistance to structural damage when cleaned by megsonics rather than other cleaning techniques. However, our recent studies have shown megasonic cleaning can create nanometer-sized pits on the surface of the Ru-capped multilayer EUV blanks. Most cleaning processes use transient cavitations to create fast fluid flows close to the surface, which will separate a particle and carry it away from the surface by hydrodynamic flows. However, very fast jet flows that result from the transient cavitation collapse can also damage the Ru surface and create pits. Therefore, stable cavitations are desirable. Many parameters are involved in determining the proper conditions

for stable acoustic cavitation, however. Acoustic pressure, gas type, and concentration in the liquid are the dominant factors in cavitation formation.

In this report, we present the results of SEMATECH's experimental studies of pit creation by megasonics on Ru-capped multilayer EUV blanks as a function of frequency, acoustic field power, gas type, and concentration in DI water and chemicals during sonication. Pit dimensions were determined by AFM and correlated to different megasonic cleaning parameters. Our results will be complemented by finite element analysis simulation of damage on the surface of the Ru-capped multilayer. Ultra-fast video microscopy (> 100,000 frames/ second) will be used to determine acoustic streaming velocities close to the surface. By correlating fluid velocity close to the surface and studying pit creation on the Ru cap by AFM, we hope to determine the damage threshold for the fluid velocity close to surface above which pit defects will be created on the Ru surface. This study is expected to help reduce one of the defect mechanisms in EUV masks.

8322-26, Session 6

A multistep approach for reticle cleaning

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Within the EUV community there are many concerns regarding cleaning and life time of EUV recticles. One of these concerns is the number of cleaning cycles a reticle can withstand before losing too much reflectivity or have remaining non-removable printable defects. The contamination on the reticles can be of a particulate type or a molecular carbon like layer caused by the incident EUV photons. Both types of contamination can be expected in real life for EUV reticles. At TNO we have started an extensive research program on cleaning of EUV reticles both for particle cleaning and molecular cleaning. We propose a multi step approach with a combination of wet and dry cleaning techniques. We will show our latest results on wet cleaning with nano bubbles as well as dry cleaning with remote plasma's. In our earlier work we have shown that our remote plasma process is capable of cleaning EUV mirrors without loss of reflectance even when over cleaned. In this work we focused on the reticles and investigated the resistance of absorber layers against plasma cleaning and show our latest results.

The nano bubbles cleaning technique looks favorable for the removal of particles in the range 20 - 50 nm, as this technique induces only a very low mechanical stress on the surface of the reticle. Nano bubbles may form an alternative for current wet cleaning methods. Nano bubbles can be generated by the so-called alcohol-water-exchanging process. In this process water is used to flush a surface covered by alcohol. Nano bubbles are formed on the substrate surface and can interact with particles present there. We investigated the particle removal efficiency for different sizes of particles with emphasis on the smaller particles in the nanometer range.

8322-27, Session 6

Molecular behavior of mask cleaning chemicals on EUV mask surfaces

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193 nm photo-induced defects (i.e., haze defects) on optical masks have been a serious challenge not only for reticle engineers during mask manufacturing and handling but also for photolithography engineers. The root causes of mask haze defects are cleaning chemical residues remaining on mask surfaces after cleaning and molecules that outgas from pellicle materials after 193 nm exposure. This places a burden on reticle cleaning engineers to find cleaning chemicals whose residues do not lead to progressive defect formation on the mask surface during exposure without compromising cleaning powers. They also must find better materials to reduce outgassing from the pellicle.

Since EUV masks do not have pellicles to protect against particle contamination, it is assumed that progressive defect creation on EUV masks is likely to be less than on optical masks. On the other hand, EUV masks suffer from another kind of progressive defect caused by the build-up of amorphous carbons released from hydrocarbons by EUV light near the surface. The generation of carbon contamination can be mitigated by improving the exposure environment, and carbon films can be removed by in situ atomic hydrogen cleaning.

It is not yet clear whether mask cleaning chemicals will react under EUV light, creating progressive defects, as they do under DUV exposure conditions. We have observed that carbon contamination prevails over any effects of solvent chemicals in a normal environment (i.e., in a low to medium level of vacuum) during EUV exposure. It is unknown, however, whether the cleaning chemicals would form defects during EUV exposure if carbon contamination is prevented. This may pose another challenge since EUV masks are expected to undergo more frequent cleaning cycles, which could induce more defects.

In this work, we will investigate the molecular behavior of cleaning chemicals on EUV mask surfaces during EUV exposure when carbon contamination is strictly controlled. The movement (e.g., migration or aggregation) of the cleaning chemical molecules near EUV exposure spots on the top surface as well as beneath the EUV mask will be studied. We will also examine whether EUV exposure could trigger the evaporation of cleaning chemicals on the EUV mask surface and possibly contaminate the exposure environment. It is believed that this study will help elucidate the impacts of mask cleaning chemicals during EUV exposure. With knowledge of mask tolerance and patterning performance affected by cleaning chemicals, this information could facilitate the proper selection of mask cleaning chemicals for optimal EUV performance.

8322-28, Session 7

High-sensitivity chemically amplified EUV resists through enhanced EUV absorption

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Resolution, Line edge roughness, sensitivity and low outgassing are the key focus points for Extreme ultraviolet (EUV) resist materials. Sensitivity has become increasingly important so as to address throughput concerns in device manufacturing and compensate for low power of EUV sources. Recent studies have shown that increasing the polymer linear absorption coefficient in EUV resists, translates to higher acid generation efficiency and good pattern formation. In this study, novel high absorbing polymer platforms are evaluated. The contributing effect of the novel absorbing chromophore in the resultant chemically amplified photoresist is evaluated and compared with a standard methacrylate polymer bound photoacid generator (PBP) platform. We report that by increasing EUV absorption, sensitivities less than 10mJ/cm2 can be achieved which is consistent with dose requirements dictated by the ITRS roadmap. Using the Albany eMET tool, the new high absorbing platform cleanly resolves 28nm half pitch line and spaces (Figure 1) with a sensitivity of 8.9mJ/cm2 versus the standard PBP platform that showed a sensitivity of 11mJ/cm2 (Figure 2). In addition, enhanced sensitization using higher absorption PBPs will be probed through quantum yield measurement of acid generation using the Szmanda titration method.

8322-29, Session 7

A new inorganic EUV resist with high-etch resistance

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Performance requirements for EUV resists will necessitate the development of entirely new resist platforms. As outlined in the ITRS,

the new thin film resists for EUVL must show high etch resistance (to enable pattern transfer using thinner films), improved LER and high sensitivity. A challenge in designing these new resists is the selection of molecular structures that will demonstrate superior characteristics in imaging and etch performance while maintaining minimal absorbance at EUV wavelengths. We have previously described the use of inorganic photoresists for 193 nm and e-beam lithography. These high sensitivity (~5 mJ/cm2) inorganic photoresists are made of HfO2 nanoparticles and have shown etch resistance that is 25 times higher than polymer resists. The high etch resistance of these materials allows the processing of very thin films (< 40 nm) which will enable resolution limits below 20 nm without pattern collapse. Additionally, the small size of the nanoparticles (< 5 nm) leads to low LER while the absorbance at EUV wavelengths is low. In this presentation we show that these inorganic resists can be applied to EUV lithography. We have successfully achieved high resolution patterning (<30nm) and low LER.

8322-30, Session 7

Tightly bound ligands for hafnium nanoparticle EUV resists

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EUV lithography has been selected by the ITRS to be the primary choice for the 22, 16 and 11 nm technology nodes. As EUV prints features with smaller and smaller CDs, the thickness of the resist films will need to decrease. Unfortunately, however, traditional organic resists will be unable to provide the necessary etch resistance in these thin films. In response, several researchers have begun to develop highly etch resistant photoresists based on metal oxide nanoparticles.

Using hafnium oxide nanoparticles, the Cornell team has demonstrated 25 nm isolated lines with doses of 6.6 mJ/cm2. The outer organic shell is made of methacrylic acid and provides the desired photochemical properties that allow direct patterning with high sensitivity while, at the same time, stabilizing the high surface area of the nanoparticles. The choice of a low molecular weight ligand, like methacrylic acid, results in a material with high inorganic content (~65-70%) and also helps keep the overall size of the nanoparticles small (2-3 nm) to allow patterning at high resolution. This resist system is compatible with current process technology, and is capable of both positive and negative tone patterning using e-beam lithography and shows great promise for EUV.

Ligand Binding: Central to the stability of nanoparticle suspensions is the strength of the bond between the ligand and the nanoparticle. The shelf-life stability of future nanoparticle photoresists, will therefore, be highly dependent upon the strength of the bond between the ligand and the nanoparticle. We have determined the relative strength of a series of several possible ligand types. The relative binding constants have been determined by allowing the nanoparticles to equilibrate in mixed ligand solutions, followed by precipitation. Relative binding energies were determined by re-dissolving the precipitated nanoparticles and comparing 1H NMR peak integrations. We found that sulfonates bind significantly more strongly than do ligands basdd on carboxylic acids. We have, therefore, used sulfonate functional group as a primary design criteria in subsequent studies (Figure 1).

Free Radical Monomers: Cornell's HfO2 resist system uses methacrylic acid as a ligand, and a method of photochemically cross-linking the polymer film using free radical polymerization (FRP). In order to improve stability, we designed a series of monomers based on the ligand binding study above. These monomers were designed with two overall goals: they were designed with sulfonate functionalities to bind strongly to the nanoparticles, and they were designed with different free radical functionalities (styrene, acrylate and vinyl) to explore the effect on lithographic performance (Figure 2).

Aqueous Development: Nearly all of development processes used in the microelectronics industry use developers based on 0.26 N TMAH. Therefore, one important goal of this project is to explore the use of

ligands that provide nanoparticles with significant levels of solubility in aqueous developer. We have synthesized a series of ligands which would make the unexposed nanoparticle-resists able to be developed in TMAH (Figure 2).

8322-31, Session 7

Evaluation of resist performance with EUV interference lithography for sub-22nm patterning

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EUV lithography (EUVL) is considered as the leading candidate for 22 nm half-pitch (hp) processing and below. The performance of EUV resists is one of the key factors for the cost-effective introduction of EUVL. However, due to aerial image limitations, most of the global effort has concentrated on resist performance at 22-60 nm hp. For the future of EUVL, it is crucial to illustrate and / or challenge the extendibility of the resist paradigm towards further technology nodes and to do so with enough lead time to ensure that any material solution can be commercialized. In the last years, the EUV interference lithography (EUV-IL) tool at Paul Scherrer Institute (PSI), with its high-resolution and well-defined areal image, stable source and interferometer, has been successfully employed for resist performance testing < 30 nm hp.

In this paper, we present performance of different resists using EUV-IL. Results with a chemically-amplified resist (CAR) for 16-30 nm hp are presented, with the aim of resolved patterns with a CAR towards 16 nm hp. Linewidth (CD) and line-edge roughness (LER) are evaluated as functions of dose for different process conditions. Line/space patterns are resolved to 16 nm hp with LER increasing with decreasing feature size. Patten collapse is observed at more aggressive pitches. This can be overcome by reducing the film thickness of the resist, but results in an increased LER. Cross-sectional SEM images of the patterns are presented providing valuable insight into the resist's performance and failure mode. The reproducibility of our experiments are presented by repeating the same exposures with constant process conditions over the course of several months, demonstrating the excellent stability of the PSI EUV-IL tool as well as the long shelf-life of our baseline resist. Moreover, pathways for CAR to achieve the resolution and LER needs for 16 nm hp at the expense of sensitivity have been evaluated.

In addition, patterning capabilities of inorganic non-CARs, such as the silicon-based resist (HSQ) and a hafnium-based resist (from Inpria) have been evaluated, showing resolution < 10 nm hp and modulation to 6 nm hp. Whereas the performances of HSQ and Inpria resist are similarly excellent, the Inpria resist is significantly more sensitive than HSQ. Resolution and sensitivity of CAR and non-CAR resists are compared. These results demonstrate that EUV-IL is a powerful tool for the evaluation of resist performance for future technology nodes, helping to fill the time gap until higher-NA alpha tools are made available.

8322-32, Session 7

Effects of out-of-band radiation on EUV resist performance

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Extreme ultraviolet (EUV) lithography high volume manufacturing tools are expected to use laser produced plasma sources to generate EUV radiation necessary for resist exposure. EUV light from laser sources emit light over a wide spectral range or popularly known as out-of-band (OOB) radiation along with the desired wavelength. EUV resist are sensitive to both EUV and OOB radiation because a fair amount of the EUV photoresists are based on materials designed for 193 nm and 248 nm. Some of the detrimental effects of OOB radiation within the

lithography process can be seen in the form of photoresist film thickness loss, which in turn results in profile degradation. Therefore development of EUV resists which are insensitive to OOB radiation is very important. We investigated EUV resist patterning performance and the effect of OOB radiation specifically in the DUV (193 and 248 nm) wavelength range.. Resist platforms with various DUV absorbance were prepared, and their EUV/DUV (193 nm and 248 nm) sensitivity ratio was measured. By tuning this ratio, EUV lithographic performance was found to improve. In conclusion, from this study effective materials for OOB reduction were identified by EUV exposure results.

8322-33, Session 7

Out-of-band insensitive polymer bound PAG for EUV resist

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Out of band (OoB) radiation has been regarded as one of the key issues on Extreme Ultra Violet Lithography (EUVL). [1] [2] OoB light especially in the deep ultraviolet (DUV) region have a negative impact on image contrast and resist profile, since general PAGs used in chemically amplified EUV resist are sensitive for DUV. It is reported that a Spectral Purify Filter (SPF) would eliminate OoB radiation. However it expense a large reduction in EUV power and hence throughput, so it is reported that HVM EUV exposure tool would not employ SPF.

Therefore, both EUV sensitive and DUV insensitive are required property to overcome OoB radiation issue by resist material itself. [3] Consideration of PAG cation structure was proceeded to control absorption for DUV. Based on the concept, OoB insensitivity was investigated both on blend resist platform and Polymer Bound PAG (PBP) platform. OoB insensitive concept was confirmed with UV spectrum and sensitivity for KrF and ArF. The OoB insensitive PAG cation worked well on PBP, while dark loss are seen on blend resist platform due to lack of inhibition effect. Lithographic performance would be exhibited using Alpha Demo Tool (ADT) and NXE3100. Outgassing property on witness sample (WS) and Residual Gas Analysis (RGA) will be also discussed.

8322-35, Session 8

Analytic treatment of the deformation behavior of EUVL masks during electrostatic chucking

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We present a new analytical approach to predict mask deformation during electrostatic chucking in Extreme Ultraviolet Lithography (EUVL). Given an arbitrary profile measurement of the mask front- and back-side and the chuck non-flatness, this method can be used as a fast alternative to time-consuming finite element simulations for overlay error correction algorithms. Furthermore it provides a theoretical understanding of various effects like the high spatial frequency embedding of the chuck roughness into the mask substrate.

The formulation is carried out via a spatial Fourier analysis of the reticle's back-side shape and the opposing chuck face. Each harmonic component in the profile will be flattened by a corresponding stress distribution on the face of the mask. We solve the mechanical equilibrium equation by employing the Airy stress function for the two dimensional plane strain case and alternately by minimizing the potential energy for the general three dimensional case. In both case, this results in the determination of the transmission coefficient, which describes the ratio of the back-side or chuck feature amplitude and the transmitted amplitude to the front-side of the mask. As a subsidiary result, we can determine the maximum allowable feature amplitude on the mask back-side which can be flattened by an electrostatic chuck without impacting the flatness of the front-side (as a function of applied voltage). The use of linearized elasticity theory also enables us to derive closed form full field

expressions for the mask in-plane and out-of-plane deformation in the two dimensional plane strain case, as well as approximate solutions for the general three dimensional case. The limitation of the analytical model has been assessed by comparison to finite element simulations; it is found that the proposed analytical method is accurate when the spatial wavelength of the non-flatness features in contact is small in comparison to the mask dimension.

Two over arching observations result from our analysis. First, the reticle itself acts as a low-pass filter: Components of high spatial frequencies in the mask backside or clamp non-flatness are damped out and cannot be seen at the front-side after chucking. Second, the applied voltage on the electrostatic chuck imposes a limit on the back-side non-flatness magnitude that can be flattened out, depending on its wavelength. Likewise this limit holds for the embedding of features of the chuck non-flatness into the mask substrate. From a numerical example we conclude that feature wavelengths of less than 30 nm will not result in any noticeable distortion on the mask front-side during the chucking stage.

We further discuss two applications. First, the electrostatic chucking of a general mask surface shape which shows good agreement when compared to time-consuming finite element calculation. Second, engineering design curves are developed for an electrostatic pin chuck such that the distortion on the mask front-side due to the pins remains within a specified tolerance. In particular we consider the critical pin-size and -pitch depending on the applied voltage.

8322-36, Session 8

Effect of radiation on the defectivity and stability of Ru-capped MoSi multilayer blanks

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Despite its effectiveness, Ru is a challenging material with respect to its stability and endurance to cleaning chemistries. In the past few years, we have shown that the Ru surface easily oxidizes, which increases surface roughness and consequently degrades EUV reflectivity because of scattering and absorption. EUV masks will have to be cleaned many times so understanding and avoiding / mitigating reflectivity loss caused by cleans is critically important.

The effect of light radiating from the EUV region to the near-infrared (NIR) region (= 13.5, 178 nm, 266 nm, 532 nm, 1064 nm) on Ru-capped multilayers was studied. In particular, surface oxidation, changes in surface energy, and thermal deformation were considered. The contact angle of the Ru-capped layer was reduced by exposing it to EUV light in vacuum, vacuum ultraviolet (VUV), or DUV light in various gas atmospheres. The probability of a particle adhering to the surface of the Ru cap layer increases as the surface contact angle increases. The contact angle of the Ru cap layer will increase with time depending on the gas mixture used during exposure.

Exposure to longer wavelengths may result in thermal effects such as multilayer intermixing if the radiation dose is above a critical level.

In addition to photon interactions, we studied electron interactions with the surface of Ru-capped multilayers. Depending on the e-beam dose, the adhesion of particles to the Ru cap may increase.

8322-37, Session 8

The SEMATECH Berkeley MET and DCT: a quest for 14nm half-pitch in chemically amplified resist, OOB contrast of EUV resists, and 6.xnm lithography

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In this paper we report on a new champion chemically amplified (CA) resist and characterize several other high-performing CA EUV resists from 16-nm down to 12-nm half pitch, using a pseudo-PSM technique. In addition, we report on the OOB sensitivity and OOB contrast of champion CA EUV resists and discuss the correlation between OOB contrast and the effects of OOB radiation during EUV exposure on patterning performance. Finally, we will report on the absolute sensitivity and contrast of several commercially available EUV resists at 6.x-nm.

8322-38, Session 8

Wavelength selection for multilayer coatings for the lithography generation beyond EUVL

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EUVL at 6.x nm is one of the candidates for the next generation photolithography. Its design requires matching the optimal wavelength of the optics to that of the light sources. Light sources might be based on Tb or Gd, the published spectra of plasmas created from these materials show highest intensities at 6.5 and 6.8 nm respectively. The reflective properties of the La/B4C coating, one of the most promising multilayer compositions for 6.x nm, are mainly determined by the B optical constants, near its K absorption edge (6.6 nm).

We have experimentally assessed the critical material properties required for making the choice on the next stage lithography wavelength from the multilayer optics point of view. Calculations of the maximum reflectance for B-based multilayers show gain near the B absorption edge. Critical wavelength was calculated using experimentally obtained optical data for B and B4C. Results notably differ from obtained using tabulated CXRO data. The wavelength dependency of reflectivity has been experimentally studied for various La-, B-based multilayer structures, including La/B4C, LaN/B4C, La/B and LaN/B, together with predictions of their peak reflectance. These results are of direct relevance for the optimal wavelength choice and the evaluation of the beyond EUV perspective.

8322-39, Session 8

A 6.xnm beyond EUV source as a future lithography source

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The development of efficient and high power extreme ultraviolet (EUV) laser and discharge-produced plasma (LPP and DPP) sources is important in many applications, such as lithography, material science, and biological imaging near the water window. Here, we investigate LPP emission coupled with a La/B4C or Mo/B4C multilayer mirror with a peak reflectance of 40% at 6.5-6.7 nm.

We observed Gd and Tb spectra under various experimental conditions. The in-band emission is attributable to hundreds of thousands of near-degenerate resonance lines, which overlap to form an unresolved transition array (UTA). To reduce the effect of self-absorption, it is important to study the influence of the initial concentration of Gd in the target. We observed the effect of differing initial target densities at a laser intensity of approximately 5.6×10^{12} W/cm2. In the case of lower-density target LPP and DPP sources, we observed enhanced spectral purity, EUV CE, and strong narrowband emission at a wavelength of 6.7 nm. These

data suggest that it is important to use shorter pulse duration irradiation and low density plasmas to increase both the EUV CE and the spectral purity.

In summary, the EUV CE strongly depends on the laser intensity and initial target density. The maximum CE was observed to be 1.8% at a mass density of 30% and the spectral purity was also improved. We will show and discuss the wavelength dependence on the spectral behavior and conversion efficiency in future work.

8322-118, Session 8

EUVL multilayer mask blank defect mitigation for defect-free EUVL mask fabrication

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For Extreme Ultra-violet Lithography (EUVL) targeting at 16nm and beyond technology nodes, the minimum printable EUVL multilayer (ML) mask defect size can be as small as 25-30nm. As a result, defect-free EUVL ML mask blank fabrication remains the top challenge for EUVL mask. Aspects of this challenge include high quality blank substrate material (low thermal expansion material) fabrication, substrate polishing, substrate cleaning, blank handling, ML deposition, and high sensitivity substrate and blank defect inspection. High investment cost and potential low blank yield due to stringent defect-free requirement can quickly drive up EUVL cost of ownership. It is anticipated, however, the EUVL ML blank yield can be drastically improved if we can allow a few defects on a ML blank. Utilizing such a "defective" grade mask blank to fabricate a defect-free EUVL mask requires several defect mitigation schemes during mask patterning processes. These schemes include modifying mask absorber pattern via repair tool to compensate the effect of an adjacent ML defect and using absorber pattern to cover the ML defects. In this paper, we focused on the study and demonstration of using device pattern to cover limited number of blank defects. The steps of this defect mitigation process include blank fiducial mark patterning, defect location relative to fiducial mark precision measurement, automated pattern shift solution simulation for a given ML defect map, and precision alignment of the device pattern to the blank defects during e-beam write. With these steps, we have successfully demonstrated the coverage of several targeted ML blank defects simultaneously via global device pattern shift.

8322-40, Session 9

Development of EUV lithography tool technologies in Nikon

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Today device manufacturing using double patterning technology with ArF immersion lithography has been already started. Because this technology can be applicable to the manufacturing of 22nmHP devices, EUV lithography is expected to be a standard lithographic technology in 16nmHP node and below. Nikon is now conducting a study of high-NA (>0.4) EUV exposure tools which are applicable to multiple-generation lithographic technology from 16nmHP to 11nmHP node. These tools are expected to be delivered in 2015 at the earliest. We are now conducting R&D of fundamental technologies required for high-NA EUV exposure tools. A part of our activities will be presented.

Optical design of projection optics of 6-mirror systems with and without central obscuration and also 8-mirror systems are under investigation. Polishing technology of mirrors is also improved. One example is EEM (elastic emission machining), which is a precision machining technology using a chemical reaction on solid surfaces. It was well known that EEM gives very smooth surface but it was applicable only to nearly plane surfaces. We developed improved EEM technology which can be applicable to curved surface for EUV optics.

On-body wavefront metrology will be used for final adjustment and fine tuning during operation of projection optics. MISTI (multi-incoherent Talbot interferometer) was developed as an on-body wavefront metrology for EUV exposure tools. On-body wavefront adjustment based on MISTI was demonstrated using EUV1. Its consistency with exposure results was confirmed.

We faced rapid degradation of transmittance of illumination optics because of carbon contamination in EUV1. Based on these experiences, contamination mitigation technologies were developed. Mitigation by oxygen introduction during exposure and UV dry cleaning are applicable for carbon contamination control in high-NA EUV exposure tools. Oxide capping layer which has better oxidation durability than conventional Ru capping layer will be applied to suppress oxidation of multilayer mirrors.

It was pointed out by Selete that carbon contamination often contains silicon, though it was not detected from contamination in EUV1. The origin of the silicon is assumed to be siloxane come from synthetic resins. So we have conducted EUV exposure tests on multilayer samples in the vapor of siloxane using a synchrotron radiation source. Degradation rate of EUV reflectivity with siloxane was faster than those with hydrocarbons or fluorocarbons which we have ever tested. And also oxygen increases the degradation rate with siloxane. It should be addressed as the third type of contamination which is different from carbon contamination or oxidation of multilayer. Because siloxane-free clean vacuum was realized in EUV1, we can achieve similar clean vacuum in our high-NA EUV exposure tools.

Behavior of particles in vacuum is much different from that in atmosphere. In vacuum where drag force does not exist, particles can reach incredibly long distance. Concrete example which was observed in EUV1 will be presented.

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8322-41, Session 9

Low CoO grazing incidence collectors for EUVL HVM

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Media Lario Technologies has adapted its proprietary electroforming technology for space applications to successfully develop and manufacture grazing incidence collectors to support the EUVL technology roadmap.

With the experience of more than 20 alpha and pre-production collectors installed to date, we present thermal, optical, and lifetime performance of the grazing incidence collector integrated into the ASML NXE:3100 scanner, meeting the requirements for pilot manufacturing. The grazing incidence collector is produced with a custom reflective layer enabling up to 1-year lifetime of the source-collector module, and has an integrated thermal control capable of 100 W power at intermediate focus.

For High Volume Manufacturing, Media Lario Technologies has developed a collector power loading roadmap extending the thermal extraction and optical stability of the grazing incidence collector from the current 100 W up to 500 W power at intermediate focus, thus enabling the scanner throughput and productivity required for low CoO operation at HVM.

8322-42, Session 9

Optical performance of LPP multilayer collector mirrors

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The usable power of high-power EUV light sources at 13.5 nm and

also the lifetime of source and collector optics are currently considered to be the largest challenges encountered during the transition of EUV lithography from development to production. Fraunhofer IOF Jena has developed technologies for defined coating of highly reflective multilayer systems with lateral gradients on strongly curved collector substrates as well as a method for characterizing the high spatial frequency roughness of EUV substrates.

Substrates with very high surface quality (rms roughness 50 %.The design wavelength of 13.5 nm is routinely achieved within a wavelength deviation of less than 30 picometers (Fig.2). The multilayer coated collectors collect EUV light with 5.5 sr solid angle thus representing by far the largest EUV multilayer collector mirrors coated to date.

8322-43, Session 9

Aerial image monitor for wavefront metrology of high-NA EUV lithography tools

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As EUV lithography tools move to higher numerical apertures (NA) to resolve smaller features, it becomes increasingly difficult to characterize aberrations in the optical system. Interferometric techniques such as phase-shifting point diffraction interferometry (PS/PDI) are difficult to perform at high-NA due to the strict requirements on coherence and reference wave quality. Self-referencing tests such as lateral shearing interferometry (LSI) suffer from tight tolerances on grating and detector tilt.

Although image-based techniques have been shown to be successful in characterizing aberrations in EUV microscopes [1], these techniques require through-focus aerial image data, which is not readily available in lithography tools. However, the development of high-resolution aerial image monitors (AIM) could extend these image-based techniques to print-based systems.

The principal challenge in developing AIMs at high resolution is overcoming the relatively low signal compared with the detector noise. In general, the resolution of the monitor is related to the smallest feature on the AIM mask. In a scanning pinhole AIM for example, measuring a 0.5 NA EUV optic would require a 12 nm pinhole. In addition to difficulties in manufacturing such a small pinhole, very little light would pass through it to the detector.

In this paper, we propose an aerial image monitor that overcomes this challenge in two ways. First we employ a 2-dimensional uniformly redundant array (URA) as the AIM mask. A URA is mathematical function that has desirable mathematical properties and can have thousands of times more transparent area than an AIM based on a pinhole. Second, we describe an iterative, image-based reconstruction method that can determine the wavefront aberrations using features that are larger than the resolution limit of the optical system. In this method, a known pattern is imaged through focus and the resulting series is compared to a computer model with a trial set of aberrations. The aberrations are adjusted and the process is repeated iteratively until a desired tolerance is met. The computation of the partially coherent aerial image intensity is expedited using the Reduced Optical Coherent Sum (ROCS) optimization. This procedure is highly versatile since it is independent of NA or illumination coherence and requires minimal experimental modifications.

8322-44, Session 9

Sub-aperture phase reconstruction from a Hartmann wavefront sensor by phase retrieval method for application in EUV adaptive optics

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Extreme Ultra Violet (EUV) lithography machine uses silicon-molybdenum highly-reflective multilayer (ML) coated mirrors to image a geometrical pattern from a reflective mask to a semiconductor wafer. The typical peak reflectance of these mirrors is around 70% at 13.5 nm at normal incidence. Even though the mirror blank is made of a substrate with good mechanical and thermal stability the ML structure and consequently the reflectivity behavior can be modified by the thermal stress caused by the partial absorption of the ML stack, leading to phase distortion in the image at the wafer.

Therefore a constant monitoring of the phase wavefront in the EUV optical box is necessary to avoid undesired aberrated image at the wafer plane.

Discussion

The Hartmann Wavefront Sensor (HWS) has demonstrated to be a valid candidate for this purpose but it has limitations in the accuracy of the reconstructed wavefront that can be achieved[1]. These limitations come from the fact that HWS measure the average of the wavefront slope at the sampling point (i.e. the sensor sub-aperture) by measuring the angular deviation of the spots in the projected pattern. Thence, the local curvatures of the phase distribution inside the each sub-aperture are not detected and in conjunction with the errors in the spot detection procedure, result in an accuracy loss in the aberration reconstruction[2].

To overcome this limitation we propose to perform a phase retrieval on the intensity data taken from the projected pattern and reconstruct the complete phase distribution inside the sub-aperture [3].

The phase retrieval algorithm is based on non-linear optimization performed on the phase distribution in the object plane (i.e. the Hartmann grid plane) to find the phase that, combined with the known pupil amplitude constrain and propagated, result in the measured amplitude distribution. The optimization finds the minimum of a metric that quantifies the agreement between the measured amplitude $F(x,y)$ in the detection plane and the amplitude of the numerical field $G(x,y)$ and it can be expressed by a squared error metric.

Such a metric is minimized with respect to the value of the phase in the pupil plane $P(x,y)$.

Following this procedure we can expand the phase distribution in term of Zernike basis set so that we optimize directly the Zernike coefficient $alpha_k$.

The chosen optimization algorithm is a gradient search algorithm using a Matlab® environment.

Simulations with realistic data have shown that with this procedure the rms error in the wavefront reconstruction decrease by a factor of 10 compared to the wavefront distribution reconstructed by a spot detection algorithm.

In Figure 1 is shown the sketch of the experimental setup built in our lab used to validate the simulations. We use a Spatial Light Modulator (SLM) to generate a specific wavefront distribution and a Shack Hartmann Sensor to check the agreement of our results with those measured using this last device.

Figure 2 shows our two example of phase retrieval from the Hartmann sensor intensity distribution regarding a tilt and defocus aberration with the relative optimization convergence plot.

The computation time is below 5 min with a normal computer.

Conclusion

A method to improve the accuracy of the wavefront reconstruction using a Hartmann Wavefront sensor has been described and experimentally demonstrated. Further developments are currently under research to push up the computational time and accuracy reconstruction. Such a method could find an application in the development of an adaptive optics system to be integrated in a EUV Lithography stepper to optimize the quality of the optical system.

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8322-45, Session 10

Comparison study for 3xnm contact hole CD uniformity between EUV lithography and ArF immersion double patterning

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In order to continue scaling down the feature sizes of the devices, EUV lithography is regarding as the most powerful candidate for patterning. So It has being studied to overcome the several issues such as source power for high throughput to apply volume production, mask defectivity from mask blank, RLS (Resolution, LWR & Sensitivity) trade off, which is the intrinsic property of EUV resist, and so on.

For 2x node DRAM, dense contact hole, which has 3xnm half pitch, has been issued to be made up to now. There are two well-known methods for pattering; double patterning with contact hole and single patterning with EUV lithography. EUV is more simple solution than double patterning for 3xnm hp dense contact hole, if it has large process window and comparable CD uniformity. Fortunately, EUV process already has larger process window than that of ArFi because its k1 value is a little bit high. But CD uniformity and pattern profile need a lot of effort to be improved and competed with double patterning.

The double patterning performance for 3xnm hp dense contact hole has been shown last year. In this paper, we will investigate on improving CD uniformity and pattern profile for 3xnm hp dense contact hole using upgrade of EUV material. And LWR smoothing technique also will be implemented to improve. We believe that CD uniformity of contact hole can be regarded as low frequency LWR of line and space pattern. So if LWR smoothing technique can reduce the low frequency LWR well, then it can work contact hole either. Finally, the performance of EUV, which is achieved by our experiments, is being compared with that of double patterning in terms of CD uniformity.

8322-46, Session 10

Key parameters of EUV resists for contact hole application

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Patterning of contact hole (CH) features with good critical dimension (CD) uniformity is one of the most critical challenges for 10nm node lithography and beyond. Extreme ultraviolet (EUV) lithography is considered a potential candidate because of its better aerial imaging and larger k1 factor than ArF immersion. To apply EUV lithography to high volume manufacturing, EUV resists are required to overcome the trade-off among resolution (R), local CD uniformity (LCDU), and sensitivity (S) at CH features as well as RLS trade-off at line/space (LS) features. We evaluated various resist materials for CH patterning applications using the micro exposure tool (MET) at SEMATECH in Albany, NY. For this study, we will report the correlation between EUV resist lithographic performance at CH features and physical properties of chemically amplified resist such as their dissolution behavior, the activation energy level of the protective group, and the acidity/acid diffusion length of the photoacid generator (PAG).

8322-47, Session 10

Modeling the effects of acid amplifiers on photoresist stochastics

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The tradeoff between Resolution, Line Edge Roughness (LER) and Sensitivity, the so called RLS tradeoff, continues to be a difficult challenge, especially for EUV lithography. Acid amplifiers have recently been proposed as a method to improve upon the overall RLS performance of EUV resists. Here we discuss a simulation approach to study the issue. The model explicitly captures the stochastic behavior of exposure, acid amplifiers, and photo-acid generators. The model also uses the standard reaction diffusion equations for acid, base diffusion and neutralization with the addition of acid amplifier using the same formalism. Using this model, the impact acid amplifiers have on the RLS tradeoff has been studied under a variety of resist conditions. Here we present the results of this study.

8322-48, Session 10

Calibration and verification of a stochastic model for EUV resist

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Line width roughness (LWR) remains a critical issue when moving towards smaller critical dimensions (CD) in EUV. We present a stochastic resist modeling approach to accurately predict LWR and CDs simultaneously. The model was calibrated for the imec baseline EUV resist (Shinetsu SEVR140) where over 250 measured CDs and corresponding LWR data points have been used. The validation was performed against both 1D and 2D patterns. Especially for 2D patterns the predictability regarding contact hole (CH) CD uniformity (CDU) was investigated. The calibration was carried out with the improved functionality of the Sentaurus Lithography Resist Calibrator where the stochastic model takes into account the roughness effects due to the shot noise and secondary electron effects during exposure, and the interaction amongst the finite number of chemical molecules (inhibitor, PAG, quencher) during PEB. These interactions are modeled by means of a kinetic Monte Carlo simulation. Although the impact of different important parameters for line edge roughness formation can be investigated with this model as well, the focus in this paper lies on accurate calibration and verification against experimental data. In the paper, we also demonstrate how the model can be used to investigate the line width roughness and CD uniformity when moving towards higher NA and off-axis illumination in EUV and to evaluate complex patterns in terms of pattern roughness and microbridging for future EUV nodes.

8322-49, Session 10

Resist outgassing characterization for qualification in high-power EUV lithography

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Extreme Ultraviolet (EUV) Lithography is on its way to high volume manufacturing (HVM). However, some critical issues remain concerning possible tool optics contamination due to resist outgassing [1-4]. For HVM, a practical qualification method to screen a number of resists in a short time is necessary. Methods have been proposed utilizing low power

EUV light sources and electron beam (EB) gun for optics contamination testing [1-4]. In the past, several groups have evaluated the low power EUV-based method [1-3]. But the long time required for contamination testing has been a critical issue. On the other hand, the EB gun-based method has been gaining attention with the capability it provides for short-time contamination testing [2, 4]. However, some issues remain unclear on how these types of light sources (in comparison to high power EUV) affect resist chemical reactions, and ultimately resist outgassing.

Thus, further investigations on optics contamination at high power EUV is essential. It is also important that these be done with the consideration of the chemical configuration of the EUV resist analyzed.

Initial work on resist outgassing induced optics contamination at high power EUV was performed. An evaluation system attached to the 10.8m long undulator of the NewSUBARU synchrotron as light source was utilized [5]. With this system, a peak EUV power as high as 200 mW/cm2 was obtained on the witness samples. The system's exposure chamber is vacuum-pumped to high vacuum conditions (<2 x 10-6 Pa) to ensure a clean analysis environment. For the witness samples, a Ru-capped Mo/Si multilayer mirror was prepared for these optics contamination analyses. The witness sample is placed facing opposite the resist-coated wafer being exposed. Witness sample contamination experiments were performed by exposing the resist-coated wafer with 2.5 times the E0 (dose-to-clear) at a total exposed area which is roughly equal to a 300mm wafer. Contamination thickness evaluations were performed with spectroscopic ellipsometry.

For these experiments, a model EUV resist based on a polyhydroxystyrene-metacryl hybrid polymer with triphenyl sulfunium - nonaflate as photo acid generator (PAG) and tri-n-octyl amine quencher. Utilizing this model resist for these high power EUV resist outgassing experiments, a contamination thickness of 2.9nm was obtained. This contamination thickness value shows a reasonable result with the above system.

During the conference, a detailed analysis of resist outgassing contamination behavior in relation to EUV resist chemical configuration will be presented. Starting from the initial results obtained, a characterization of contamination mechanisms depending on polymer platform, PAG type, PAG loading, etc will be discussed.

These results will be compared with those of the EB gun-based resist qualification system. Such a comparison from the view point of chemical configuration will confirm the EB gun-based method's reliability for HVM resist qualification.

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8322-50, Session 10

Direct comparison of resist outgassing and optics contamination using in-band EUV photon exposure and e-beam exposure from several EUV sensitive resists

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One of the principal challenges in the ongoing EUVL research efforts is the development of a suitable EUV-sensitive resist. In addition to high sensitivity, there is stringent limit to the amount of contaminants that the

resist can outgas during wafer exposure and the related risk for optics contamination in EUV exposure tools.

The outgassing testing using e-beam exposure instead of EUV exposure has been proposed as a more cost-effective method of testing. Due to practical limitations, very little published results are available verifying that the electron induced resist outgassing is equivalent to the EUV induced resist outgassing.

With the recent development of a resist out-gassing testing system equipped with both an in-band EUV photon excitation source and an e-beam exposure capability, a direct comparison of resist outgassing for two modes of excitations was obtained. Measurements were performed in an ultra-clean measuring chamber equipped with a high sensitive residual gas analyzer (RGA), so as not to add background (non-resist related) contamination and a separate electron gun illuminates the witness sample for cracking hydrocarbons during exposure.

Recent RGA and optics contamination results from several EUV sensitive resists using in-band EUV photon excitation and an e-beam excitation under same measurement conditions will be presented.

8322-34, Poster Session

EUV actinic imaging tool aerial image evaluation of EUVL embedded phase-shift mask performance

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Extreme Ultraviolet Lithography (EUVL) embedded phase shift mask (EPSM) can further extend lithography resolution limit and provide better pattern fidelity as compared to that of EUVL binary mask for 16nm node technology and beyond generations. In our previous study, we have demonstrated in wafer printing that EUVL EPSM can provide improved process window for dense lines and contacts as well as having low shadowing effect when compared to that of the EUVL binary mask. Due to limitation of current EUVL resist performances, certain advantages of EUVL EPSM, such as line edge roughness (LER) improvement, cannot be readily seen at wafer resist level. This is because the aerial image quality improvement in LER is over shadowed by the current large resist intrinsic and process induced LER. We believe that when EUV resist and wafer process improves in future, mask induced pattern fidelity difference will start to play an observable role in wafer printing. In this study, we focused on comparing EUV actinic aerial image performance of a EUVL EPSM and a EUVL binary mask for both lines and contacts. Without convoluting with resist effect, the mask aerial image performance comparison of two different masks can better reflect all the effects that are due to mask differences. Our analysis of the EUV actinic aerial images of a EUVL EPSM and a binary mask showed not only the process window advantages of the EPSM as demonstrated previously, but also the improved LER performance of EUVL EPSM when compared to that of the EUVL binary mask. The matrix used to analyze the aerial images includes aerial image contrast, normalized image log-slope (NILS), LER, process windows (Bossung plots), etc. Our detailed analysis is performed for various line and contact features.

8322-60, Poster Session

Study of line-end printing of very low-K1 process

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While the pitch limit of a lithography system can be resolved by pitch splitting techniques, line end printing does not benefit substantially from pitch splitting and is becoming more of a concern at very dense pitches. Historically, line end printability is often measured by the minimum resolvable tip-to-tip space. This paper proposes that, for very dense pitches, the line printing quality near the end is another critical aspect of process control in addition to the minimum tip-to-tip space. It is because, due to the line end diffraction, the line imaging performance near the line end is usually worse than that of one-dimensional structures, which makes linewidth control more difficult near the line end, particularly for low k1 processes. In this paper, both computational and experimental study is done to characterize line end printing for both EUV and double patterning optical lithography.

In this paper, simulation is first done to calculate the line image near the line end for a 90nm pitch with optical lithography. Simulation results show that, moving toward the line end, the line image shows obvious degradation compared with the corresponding one dimension line structure. For low k1 processes, considering that even one-dimensional lines and spaces are hard to print, the printing is even more challenging near the line end and is thus a critical aspect of lithography control.

The line imaging near the line end is simulated for both double patterning optical lithography and EUV lithography, where the minimum pitch of single optical exposure is two times the EUV pitch. For optical lithography, the line imaging deterioration is observed within about 40nm from the line end. On the other hand, in EUV lithography, the degradation of the line imaging near the line end is less noticeable. The same study is also conducted for negative tone development. It shows that applying negative tone development improves line end printability compared with conventional positive tone development. Still, EUV lithography presents better line end printability than optical lithography. Experiments are also done to print nested line tip-to-tip, and the linewidth uniformity at various distances from the line end is characterized for both EUV lithography and optical lithography.

In this paper, line end printability of optical lithography is investigated for different pitches through simulation. For each pitch, an illumination setting is chosen to optimize the minimum pitch and the line image near the line end is then studied. A relationship between minimum pitch and line end printability is then built and analyzed. The illumination effect on the line end printability is also explored for optical lithography.

8322-61, Poster Session

The role resist plays in EUVL extensibility

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Our previous paper investigated the extensibility of extreme-UV lithography (EUVL) based on aerial image simulation. We concluded that there is no problem for EUVL to pattern technology nodes with minimum pitches 64, 44, and 32 nm. However, even with a higher numerical aperture, it is not possible for EUVL to further extend to the node with 22-nm minimum pitch, due to the mask shadowing effect, unless we are able to reduce the absorber thickness by introducing EUV AttPSM. Reducing the angle of incidence on the mask is also helpful, if possible.

In this paper, we consider the role resist plays in the extensibility of EUVL. In the simplest form of resist modeling, resist is characterized by an acid diffusion length (or more generally, resist blur) and the impact on patterning is described by convolving, e.g., a Gaussian with the standard deviation equal to the acid diffusion length, resulting in the diffused aerial image model.

We estimate resist blur of currently available EUV resists by measuring contrast related quantities such as EL and MEEF, etc., and comparing them with the simulated ones with various resist blurs. However, process window simulations using such resist blurs lead to the conclusion that EUVL can only be extended to the node with 44-nm minimum pitch.

Next, we discuss a more refined method to extract the resist blur by considering the contrast loss due to scanner aberration and flare, and then estimate the impact on patterning by considering the reaction and diffusion in the resist process. This results in a smaller resist blur and smaller impact from resist blurs. With improvements in lens aberration, flare, resist materials, and processing techniques, we conclude that EUVL can at least be extended to the node with 32-nm minimum pitch.

8322-62, Poster Session

The factor affecting on LWR and sensitivity in EUV resist material

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We have studied in various ways to reduce LWR from the material point of view. Thus, we pursued to know the means to reduce LWR with substituted ratio of acid labile group, Mw, and Pd. Additionally, we developed various kinds of monomers with steric hinderance of the pending group to make polymers of good sensitivity and resolution. we are also apt to know how is LWR affected by hydroxy group species. In this paper, we will show and discuss the results of these studies obtained by tools of e-beam and EUV.

8322-63, Poster Session

Steady progress on laser-assisted discharge produced plasma (LDP) technology

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Delivering light sources for extreme ultraviolet lithography (EUVL) for more than 10 years, XTREME technologies GmbH is now focused on developing powerful and stable EUV sources that will enable EUVL to transition to high volume manufacturing (HVM). A paradigm shift, EUV raises new challenges demanding performance to increase by several orders of magnitudes. Scalable in terms of optical power and lifetime, XTREME technologies' innovative LDP (Laser-assisted Discharge Plasma) technology combines the specific advantages of the formerly developed LPP (laser produced plasma) and DPP (discharge produced plasma) technologies while overcoming the inherent limitations of those.

As a hybrid technology, LDP uses both a laser and an electrical discharge. The Tin fuel is provided by liquid Tin baths wetting the surface of rotating wheels. Those Tin films are forming the electrodes. A trigger laser of moderate energy evaporates a small amount of Tin from the thin film without damaging the wheels themselves. A capacitor bank then discharges a high voltage/high current into the Tin cloud (see schematics below). Self pinching, a hot dense plasma is generated between the two electrodes. When relaxing to a lower energy state, the plasma emits EUV radiations as a Planck emitter. A long life grazing incidence mirror - protected with a Foil Trap from the damaging debris generated by the plasma - collects and focuses the EUV light towards the scanner. A series of mechanical baffles, together with the Foil Trap, prevent the transport of Tin contaminants towards the scanner and the pellicle-less mask.

Compared to the more traditional purely laser based LPP technology, LDP demonstrates high wall plug efficiency, long lifetimes and high stability. Against the conventional DPP, LDP achieves high electrode lifetime - through the dispersion of the heat load and plasma-wall interaction to a larger and regenerative electrode surface - and offers a path to high power scalability. Also, the small thickness of the Tin film covering the rotating wheels enables mass limited operation i.e. a significant reduction of the amount of debris generated by the source. Complementary to the oral presentation at this conference, in this poster we present further technical details and results of our HVM source development.

8322-64, Poster Session

Sub-atmospheric gas purification for EUVL vacuum environment control

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EUV lithography (EUVL) presents new demand on gas purifiers, targeting removal of key contaminants like moisture and hydrocarbons from

hydrogen and nitrogen gases, to deliver gas flow under sub-atmospheric pressure. Moisture and hydrocarbon contamination in the EUV vacuum environment can result in irradiation induced degradation of multilayer optics operational lifetime. Contamination levels need to be strictly controlled in the EUVL tool environment. Per one requirement (ASML -SPIE 2003, 503, 24) EUV chamber levels of $CxHy \leq 1x10$-9mbar, $H2O \leq 1x10$-7mbar is required. In turn purity levels of parts-per-billion by volume (ppbv) and parts-per-trillion by volume (pptv) are being targeted for gases introduced under vacuum into the EUVL chamber.

Scanner manufacturers employ a gas distribution box to control conditions like flow, pressure and purity of gases supplied to the mini-environment (ME) and EUV vacuum chamber for cleaning, purging exposure optics and providing dynamic gas lock. Gas conditioning in a vacuum environment therefore, requires use of distribution elements including gas purifiers that do not outgas under reduced pressure.

Typically gas purifiers employ adsorption chemistry to selectively remove (adsorb) oxygen and carbon containing contaminant species from the carrier gas flow. Under vacuum gas flow conditions potential adsorbate release can raise the partial pressure of moisture and hydrocarbon background in the EUV vacuum chamber. This can possibly prolong EUVL tool pump down periods (idle time), further exacerbating efforts to improve overall process throughput. We explore moisture removal under sub-atmospheric pressure for HX (Entegris, Inc.) gas purifier.

A commercial (Halo- H2O RP, Tiger Optics) reduced pressure cavity ringdown spectroscopy (CRDS) method is utilized to examine moisture removal performance of H2 and N2 gas purifier, HX (Entegris, Inc.) under sub-atmospheric pressure gas flow. Our studies demonstrate outlet purity levels below instrument LDL (10 ppbv, respectively). This in turn will potentially limit moisture release to EUV chamber from a gas distribution box equipped with HX (Entegris, Inc.) purifier as well as enable shorter tool pump down time.

A key aspect of our test is to mimic the affect of gas supply switch states, adopted in the ME, on moisture outgassing from a gas purifier. To maintain different gas supply states during cleaning and purging nitrogen and hydrogen need to often flow through the same gas distribution path. This requires a single gas purifier solution that is compatible with both N2 and H2 gases. Experimental data (see Figure 1) for HX (Entegris, Inc.) purifier demonstrates no occurrence of moisture outgassing under repeated switching from N2 to H2 near 10 kPa pressure.

In conclusion, our preliminary studies provide a better understanding of gas purifier related moisture outgassing under vacuum and should facilitate better environmental control and standardization of tool operational parameters in EUV lithography. HX (Entegris, Inc.) purifier is vacuum compatible and is seen to give near five times (5x) superior outlet purity performance. Overall reduced moisture outgassing under vacuum and gas switch as well as faster drydown is observed.

8322-65, Poster Session

Low-energy electron bombardment induced surface contamination of Ru mirrors

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Extreme ultraviolet (EUV) radiation induced surface contamination of the Ru capping layer of Mo/Si multilayer mirrors is now of great concern in terms of mirror performance [1]. The lifetime of a Mo/Si mirror is severely affected by surface contamination during EUV exposure. Such concern has previously been explained in terms of the interaction of the hydrocarbons and water molecules with secondary electrons [2]. During the interaction process, water molecules in the test chamber are dissociated on the Ru surface, while carbon is accumulated on the surface following the dissociation of hydrocarbons. In order to understand the impact of secondary electron induced contamination of Ru surface, we bombarded Ru films with low energy (100 eV) electrons and the change in surface chemistry was investigated using X-ray photoelectron spectroscopy (XPS). Along with XPS studies the corresponding effect on in-situ EUV reflectivity was examined by exposing Ru surface to photons at 13.5 nm wavelength in an ultrahigh vacuum chamber. A time dependent decrease in EUV reflectivity up

to ~10 % after 9 hours was recorded during electron bombardment with a sample current of 45 nA and correlated with XPS data. Detailed XPS analyses showed a sudden increase in water molecules and carbon concentrations on the Ru surface in the first 1 hour, followed by a slow but linear growth in carbon concentration in parallel to the linear decrease in water content in following hours of the experiment. A slight oxidation of Ru surface was noticed; and explained in terms of the electrons bombardment mediated dissociation of water molecules. Further analyses show degradation in carbon-oxygen bonds after initial increase in concentration for an hour. The impact of water molecules on Ru surface and accumulation of carbon through dissociation of residual hydrocarbons are discussed. A comparison is made between the effect of low energy electrons and the 13.5 nm EUV radiations on Ru surface behavior during exposure.

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8322-67, Poster Session

Coat-develop track process for inorganic EUV resist

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A baseline coat-develop track process has been established for inorganic EUV resists. Inorganic EUV resists have already been highlighted for their higher resolution and lower Line-Width-Roughness (LWR) for lithography features as well as strong etch resistance. This inorganic resist system is not only interesting due to lithography process capability but also do to its influences on coat-develop track processing. It is understood that this inorganic resist system is dissolved in an aqueous solution and therefore has the different characteristics compared to typical polymer photoresist in organic solvent.

Spin coating this aqueous resist solution leads to several challenges beyond the traditional aqueous Top Anti-Reflective Coat (TARC) materials used decades ago. Resist spin coating systems have continuously improved over the years based on polymer photoresists, therefore it becomes necessary to confirm if the latest coat module design and processes are equally applicable to aqueous resists targeted for EUV lithography. Another characteristic of this inorganic system it is not a chemical amplified resist. Post-Applied Bake (PAB), Post-Exposure Bake (PEB) and develop processes are compared with current polymer photoresist process. In this study, a coat-develop track process baseline is established for metrics such as film thickness uniformity, critical dimension (CD) uniformity and process defectivity. Based on this baseline data areas for improvement in coat-develop track process are identified to enable inorganic resist transition to volume production with EUV or E-Beam lithography

8322-68, Poster Session

Phase defect mitigation strategy: fiducial mark requirements on EUVL mask

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The requirements of Fiducial Mark (FM) on EUVL Mask were studied to establish the phase defect mitigation method with EUV Actinic (at wavelength) dark-field Blank Inspection (ABI) tool, E-beam writer, and other inspection tools.

At first we estimated the accuracy requirements of phase defect

location by considering the defect mitigation strategy of cover and/or compensation to defects by absorber patterning. As shown in figure, to cover the defect by absorber pattern shift with 3 sigma confidence level, the defect size and 6 sigma of total phase defect location accuracy should be less than the pattern width. This total accuracy need to be reduced to 20 nm (1 sigma) for next generation EUV blank inspection tools [1]. Each of EUV ABI tool and E-Beam tool are absolutely necessary for all of the phase defect detection, and mitigation by absorber patterning respectively. Then the total accuracy of phase defect location by at least both of EUV ABI tool and E-Beam tool are required to meet 20 nm total accuracy. This total accuracy is mainly composed of three factors. One is a measurement repeatability of FM location, second is stage movement accuracy between FM and phase defect, and third is a measurement repeatability of phase defect location. Then, as the first step to achieve 20 nm total accuracy, we regard FM line width, depth and fabrication method as key factors to obtain higher S/N ratio of EUV light and E-Beam scattered by FM.

So secondly to identify the optimum ranges of FM requirements to line width, depth and fabrication method like etching in Quartz substrate or Mo/Si Multi-Layer, we tried simulation and experiments. Regarding on the simulation, we calculated expected signal of EUV light scattered and diffracted by FM with various line widths, depths and different etched layers. Regarding on the experiments, we fabricated both of quartz substrate etched and Mo/Si Multi-Layer etched FMs on a test mask. We etched FMs of various line widths and depths by FIB. And we inspected them with and without absorber coated conditions by EUV ABI tool, E-Beam tool, and other inspection tools. We also measured the defectivity of FM test mask etched by FIB with Magics.

In this presentation, we will explain the phase defect mitigation strategy, the estimation of total location accuracy requirement, the simulation and experiment results of FM scattering and diffraction. And we will propose the optimum ranges of FM line width, depth, and fabrication method on EUVL Mask based on above results. This work was supported by NEDO.

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8322-69, Poster Session

Analysis and control of thermal and structural deformation of projection optics for 22nm EUV lithography

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Extreme ultraviolet lithography (EUVL) is one of the most promising technologies targeting 22 nm technology generation and beyond with high throughput. To attain diffracton-limitied resolution, the total rms (root mean square) wavefront error of EUV optics must be less than 1 nm in rms. Consequently, the stringent tolerance on the figure error of each mirror is about 0.2 nm. While the thermal deformation of the mirror derived from the 35% - 40% absorption of the incident power by the multilayers of EUV optics ranging from several nanometer to some ten nanometers will affect the optics performance of the projection optics (PO). Thus it is necessary to analyze the thermo-mechanical effects in a complete system performance research of EUVL.

Several groups have shown the impact of thermal and structural deformation on lithographic performance for four-mirror PO at the 100 nm technology generation with throughput model of 20 200 mm wafers per hour [1]. Impact of thermal and structural deformation on the EUVL performance for six-mirror at 35 nm technology generation with throughput of 80 300 nm wafers per hour has also been reported [2]. To our knowledge, thermal and structural deformation and its impact on optical performance for six-mirror at 22 nm technology generation have not been reported yet.

Our study is based on a six-mirror PO designed for EUVL at 22 nm technology generation with throughput of 100 300 nm wafers per hour. In the heat loading process, simulation details of transient thermal and structural deformation for the six-mirror PO will be presented. When all the six mirrors of PO have reached thermal equilibrium state, steady thermal and structural deformation and its impact on optical performance for EUVL will be analyzed. The results show that (a) the maximum

temperature increase is 9.77 in the smallest mirror, which is taken as a stop of PO; (b)the maximum thermal deformation at clear aperture is about 5.89 nm in rms, including spherical deformation and non-spherical deformation, and (c) the maximum non-spherical deformation at clear aperture is about 3.07 nm rms. While the mirror is heated by partial coherent illumination (partial coherent factor 0.5), the distortion of 22 nm line and space is 6.956 nm, critical dimension (CD) error is 3.414%. So the thermal and structural deformation adversely affects the optical performance.

We need to control the deformation of mirrors of PO, as the deformation of mirrors seriously affects the optical performance of the PO. In the study, the structure of the mirrors of the PO will be optimized to reduce the deformation. As the PO of EUVL is a reflective optical system, the thickness of each mirror can be varied within a certain range. The deformation of mirror will change when the thickness of mirror changes. Compare to the different thickness of mirror by using finite element analysis, the optimal thickness will be chosen to reduce the thermal deformation of mirror. In the paper, we have attained the optimal thickness of each mirror, found the optical performance of the PO enhanced.

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8322-70, Poster Session

Imaging performance of the SEMATECH Albany MET after upgrading the illumination optics

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The SEMATECH Albany micro-exposure tool (AMET) has been playing a significant role in the development of extreme ultraviolet (EUV) resists and materials. Since 2008, more than 4,000 materials and 15,000 wafers have been processed at the Resist Materials and Development Center (RMDC). The current half-pitch resolution limit for the 0.3 numerical aperture (NA) AMET with a 5X reduction ratio is approximately 20 nm with our champion resist and dipole illumination. To fulfill the needs of EUV development at the 16 nm half-pitch and beyond, the AMET illumination optics were upgraded and the outer sigma pupil fill was increased from 0.68 to 0.9.

With an upgraded illuminator and current 0.3 NA projection optics, the modeled aerial image contrast shows the half-pitch resolution can be pushed beyond the current capability of the tool with modified dipole illumination, assuming no flares and wave-front errors. This paper will demonstrate improvements in imaging capability after the illumination optics were upgraded and compare these results against the modeled data. Multiple resist materials including candidates from 193, 248, and hybrid polymer platforms, as well as blended and bound photoacid generators (PAGs) were evaluated to determine the resist performance at the 16 nm node and beyond. Performance criteria will include resolution, line edge roughness, sensitivity, and dark loss, as evaluated by top down critical dimension-scanning electron microscopy (CD-SEM) and cross-sections.

8322-71, Poster Session

Laser-produced plasma UTA emission in 3-7nm spectral region

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An engineering prototype high average power 13.5-nm source has been shipped to semiconductor facilities to permit the commencement of high volume production at a power level of 100 W in 2011. In this source, UTA (unresolved transition array) emission of highly ionized Sn is optimized for high conversion efficiency and full recovery of the injected fuel is realized through ion deflection in a magnetic field. By use of a low-density target, satellite emission is suppressed and appropriate ionization attained with short pulse CO2 laser irradiation. The UTA is scalable to shorter wavelengths, and Gd is shown to have a similar conversion efficiency to Sn (13.5 nm) at a higher plasma temperature, with a narrow spectrum centered at 6.7 nm, where a 70% reflectivity mirror is anticipated. Optimization of short pulse CO2 laser irradiation is studied, and further extension of the same method is discussed, to realize 100 W average power down to a wavelength of 3-7 nm. Because it moves to shorter wavelength with increasing Z, the n = 4-n = 4 UTA can be used for other applications, such as transmission x-ray microscopy for biological imaging in the water window. We have made preliminary studies of the potential of high-Z material as the BEUV sources. Our calculations show that high-Z plasmas, at an electron temperature at 600 eV, radiate strongly near 3.9 nm. We have initiated a number of experiments to explore how this emission may be optimized in practice.

8322-72, Poster Session

Impact of the phase defect structure on an actinic dark-field blank inspection signal and wafer printability

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The influence of phase defects embedded in EUV mask blanks on wafer printing is always standing in the center of attention. There are some ideas to reduce the printable phase defects. One is to hide the phase defects under the absorber layer by adjusting the location of device pattern during mask patterning. The other is to remove the absorber layer appropriately around the phase defects to eliminate the harmful influence of the phase error. Concerning the elimination method, we have to understand accurately the influence from size and shapes of phase defects on wafer printing. As for the growth model of the phase defect due to the bumps on the substrate, previous work indicated that the phase defect does not always vertical-grow from the surface of the substrate. It means that a surface geometry measurement of phase defects using AFM or non-actinic inspection tool is anticipated to be not perfect for mitigation strategy with covering or compensating phase defects by absorber pattern.

In this presentation, we will report a growth model of phase defects and the influence of the three dimensional defect shape on signals of an actinic dark-field blank inspection tool (ABI tool) and wafer printability. As a result, ABI signals were sensitive to not only the shape and size of phase defect but also the growth model of the phase defect. And the non-perpendicular grown phase defect will make it more difficult to mitigate the defects.

8322-73, Poster Session

Study of actinic dark-field inspection with programmed amplitude defects

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One of the key challenges of EUVL is to make defect-free masks. In general, it is considered multilayer phase defect is more serious. Therefore, we have developed an actinic dark-field inspection tool to detect multilayer phase defect. However, there might be some amplitude defects on a surface of multilayer during actinic dark-field inspection.

In this paper, we investigated the characteristics of an actinic dark-field inspection with programmed amplitude defects. In addition we will compare the inspected result with simulated result. Since it is considered the shape of amplitude defect affects inspection result, we used the defects with several values of size, thickness and other parameters in the inspection experiments. In this study, we made the programmed amplitude defect with EB exposure and carbon compound gas.

We obtained the test results that defect size and thickness affected inspection signals. At a certain size, the inspection system detected the defect as bright signal. The defect signal intensity was larger than the background intensities. However, at another size, the inspection system detected the defect as dark signal. The defect signal intensity was less than the background intensities. Also variation of signal intensity was confirmed according to the defect size. It is important to confirm whether these inspection characteristics are reasonable or not. We will calculate the simulation and compare inspected result with simulated result.

8322-74, Poster Session

The novel top-coat material for RLS trade-off reduction in EUVL

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EUV lithography is one of the next generation lithography candidate for hp22nm and beyond, however the light sources, tools, masks and resists are still the key issues for EUV lithography. In light source development, low power is one of the critical issue because of the low throughput, and another issue is Out of Band (OoB) light existing in EUV light. OoB is concerned to be the cause of deterioration for the lithography performance. The metallic filter is applicable as OoB absorber, but the low transmittance for EUV light is the problem.

In order to avoid this critical issue, we focused on development of the resist top coat material with OoB absorption property as Out of Band Protection Layer(OBPL). Because OBPL can be removed by conventional alkaline developer and rinse, the additional rinse process or special equipment are not necessary for OBPL application. We designed this material having high absorbance around 240nm wavelength and high transmittance for EUV light. And this material aimed to improve sensitivity, resolution and LWR performance. This paper describes the material design and lithography performance of OBPL for EUV lithography.

8322-75, Poster Session

Is extreme-ultraviolet pellicle possible? in terms of heat absorption

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To make smaller chips, we have been used the light source of shorter wavelength. Extreme ultraviolet lithography (EUVL), the most powerful technology of next lithography, uses the light of 13.5 nm wavelength. Light has larger energy and the absorption of light to material increases as the wavelength becomes shorter. Because of this property, many problems can happen, and it delayed the development of EUVL. One of the problems is that a lot of contaminations are generated in the process, which affects the quality of mask and finally the pattern on wafer gets worse. To solve this problem, people are trying to develop a (non-removal) pellicle, but it is not easy because of the light properties of short wavelength. In this paper, we estimate the absorption quantity of pellicle with optics concept, and its temperature change with the heat transfer concept. The pellicle which is being developed consists of two structures. One is thin film and the other is wire-mesh. Thin film is a membrane where flying contamination is attached to. There are two purposes in using thin film, one is preventing the contamination from reaching the mask, and the other is inducing defocus of light so that light can be reflected on mask uniformly all over the area to send the clear image to wafer. Wire-mesh is installed to support the thin film not to droop down. Honeycomb structure is the best and the most stable one to meet the requirement. Thus, it is made in regular hexagonal structure.

The bigger wire would be better to support the film, however, the more light would be blocked, then. Thus it is important to make the wire of minimum width to support the film. In the previous studies done by others, there are 3 cases depending on linewidth and pitch and we review all the cases. We take silicon as the material of thin film and Ni/Si for wire-mesh.

First, we are going to calculate how much of light would be blocked or reflected by and absorbed to the pellicle with the optical coefficients of material. Next, with the assumption that all absorbed energy changes to heat, we will see the temperature difference and consider other thermal phenomenon.

The heat has three modes in transfer, which are conduction, convection and radiation. We have checked that radiation is predominant of all. Heat conduction can be explained by Fourier's law, according to which, conduction rate depends on conductivity of material and cross-sectional area. Because of thin structure (~50 nm) of pellicle, the cross-sectional area is very small and the heat transfer by conduction might be so slow that we can neglect. Considering the convection mode, we thought the condition of vacuum (~10-6 torr) makes it ineffective. Thus we roughly consider the radiation only, and see the temperature profile in exposure and cooling time of pellicle. We present the temperature profiles with parameters, the absorptivity and incident power. We suggest our thought about determining the reasonable cooling time in the process.

8322-76, Poster Session

Phase defect printability analyses: dependence of defect type and EUV exposure condition

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As well as a development of multilayered mask blank inspection technique, understanding the impact of phase defects on the printed pattern size variation is also important to clarify the critical defect. In the Selete's work, the printed line pattern affected by the phase defects were demonstrated and the phase defect impact variation with respect to the exposure condition was investigated.

In this study, we investigate more pricisely a phase defect printability by the use of analysis of the EUV light scattering and imaging characteristics. Bump and pit phase defect impacts on printed 24 nm ~ 20 nm L/S patterns were simulated under the two kinds of exposure conditions such as (a) 0.25 NA with dipole illumination, and (b) 0.32 NA with circular illumination.

Before evaluating the phase defect impactl, we investigated scattering characterisrics of EUV light at the phase defect by calculating the near-field intensity. For bump defect, reflected EUV light intensity near the multilayer surface included an intensity loss at the bump location. On the othe hand, for pit defect, a little increase in intensity appeared near the pit location.

Next, we evaluated the space width variation of printed L/S patterns affected by the phase defect located at the center of space, and the impact of bump defect and pit defect were compared under the two

kinds of exposure conditions.

In this presentation, analyitical results of EUV light scattering by the defect, variation of phase defect printability depending on both a defect type and exposure condition will be shown. This work was supported by NEDO.

8322-77, Poster Session

Latest cluster performance for EUV lithography

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Previously, fundamental evaluations of the Extreme Ultra Violet (EUV) lithography process have been conducted using the CLEAN TRACK ACT 12 coater/developer with the ASML EUV Alpha Demo Tool (ADT) at imec.1,2 In that work, we could confirm the basic process sensitivies for the CD and defectivity with EUV resists. Ultimate resolution improvements were examined with TBAH and FIRM Extreme. Moving forward with this work, the latest inline cluster is evaluated using the ASML NXE:3100 pre-production EUV scanner and the CLEAN TRACK LITHIUS Pro -EUV coater/developer. The imec standard EUV baseline process will be evaluated with manufacturability of CDU control based on 27nm HP and ultimate resolution studies focusing on 22nm HP. Optimizations of the baseline process will be performed to reduce defectivity, pattern collapse and line width roughness.

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8322-78, Poster Session

Smoothing of substrate pits using ion-beam deposition for EUV lithography

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Mitigation of pit-type defects proves to be a major hurdle facing the production of a defect-free mask blank for EUV lithography. Recent efforts have been directed toward substrate smoothing methods during deposition. The angle of incidence of the substrate is known to have a significant effect on the growth of defects during deposition. It has been shown that shadowing effects for bump-type defects are reduced when depositing Mo/Si films at near-normal incidence, resulting in a Gaussian growth profile in which the height and volume of the defect are minimized. Conversely, operating at off-normal incidence reduces shadowing of pit-type defects. When altering the angle of incidence of the substrate, the target angle must be changed to maintain uniformity. The resulting mask blank must also meet surface roughness specifications post-deposition while maintaining a low defect density. In this study, various substrate angle and target angle combinations were investigated within the Veeco Nexus Low Defect Density tool at SEMATECH to find optimum in situ pit smoothing conditions using ion beam deposition on both quartz and low thermal expansion material (LTEM) substrates. The possible substrate-target angle combinations are limited by the design of the current deposition tool; therefore, a phase space has been mapped out to determine uniform and non-uniform regions. Other deposition parameters including operating pressure and working gas composition were also explored. After deposition, EUV reflectrometry measurements were taken to evaluate uniformity in the wavelength; surface roughness, change in pit depth, change in full width at half maximum, and pit smoothing power were determined using atomic force microscopy (AFM); transmission electron microscopy (TEM) was used to study the effect of film disruption through the multilayer; and the printability of smoothed pits will be measure actinically using SEMATECH's AIT tool.

Preliminary results show that positive values for substrate angles in the uniform region tend to give a high surface roughness after multilayer deposition; however, the combinations with negative substrate angles show promising results. Substrate angles with lower values resulted in better smoothing than the higher substrate angles. AFM results confirmed that pit smoothing power at lower substrate angles is greater than under the standard deposition conditions employed by the tool. Lower chamber pressure was proven to increase the smoothing power of pit-type defects during deposition. Preliminary TEM cross-section data confirmed the smoothing results obtained by AFM analysis. The use of Ne and Xe as working gases is also under review. Extensive AFM analysis, TEM cross-sections, and printability data will be presented.

8322-79, Poster Session

TiO$_2$-SiO$_2$ ultra-low-expansion glasses for EUVL system evaluated by ultrasonic zero-CTE temperature measurement system

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TiO2-SiO2 ultra-low-expansion (ULE) glasses, with a coefficient of thermal expansion (CTE) within 0±5 ppb/K at desired operating temperatures, are required for substrates of mirrors and photomask blanks in EUVL systems. In particular, the temperature at which the CTE becomes zero, T(zero-CTE), must differ from positions of multiple mirrors and mask substrates because of the high light-source power needed for high volume manufacturing. It is therefore necessary to evaluate T(zero-CTE) and the distributions of EUVL-grade ULE glass ingots and to classify them for proper use according to the T(zero-CTE) data.

We developed an indirect ultrasonic measurement method as a practical system for super-precisely measuring the T(zero-CTE) of TiO2-SiO2 ULE glasses, based on our experience with a line-focus-beam ultrasonic material-characterization system. T(zero-CTE) is evaluated by measuring the velocity of leaky surface acoustic waves (LSAWs), VLSAW, excited and propagated on a water-loaded specimen surface. This method and system have the significant advantage of obtaining two-dimensional CTE distributions on specimen surfaces, which are very important for EUVL, under nondestructive and non-contact measurement conditions. This system operates at 225 MHz and 75 MHz in a stabilized measurement environment of temperature, for example, 23.00°C, with a measurement accuracy of ±0.17 m/s (±0.005%) at 225 MHz and ±0.07 m/s (±0.002%) at 75 MHz, corresponding to resolutions of ±0.4°C and ±0.2°C for T(zero-CTE), respectively.

T(zero-CTE) of TiO2-SiO2 glass depends on both TiO2 concentration C(TiO2) and fictive temperature (TF), a parameter related to the thermal history and OH concentration C(OH). In this paper, we obtained relationships among T(zero-CTE), acoustic properties (VLSAW, longitudinal velocity (Vl), shear velocity, and density), C(TiO2), TF, and C(OH) of TiO2-SiO2 glass.

Homogenized TiO2-SiO2 ULE glass substrates with C(OH) = 100 and 1000 wtppm were heat-treated at different annealing temperatures to obtain specimens with different TF. Specimens with dimensions of 50 × 35 × 10 mm3 were prepared for measuring acoustic properties and CTE characteristics.

We measured acoustic properties, T(zero-CTE), C(TiO2), and C(OH) for specimens and obtained relationships among them. As C(TiO2) increases, Vl and VLSAW decrease, and T(zero-CTE) increases at C(OH) = 1000 wtppm. As TF increases, Vl and T(zero-CTE) increase, and VLSAW increases slightly. Vl measurement is sensitive to TF, and the resolution is ±0.4°C. The strain point (TS) of TiO2-SiO2 glass with C(OH) = 1000 wtppm is 890°C, and annealing temperatures within TS±100°C

are acceptable to obtain large, homogenous ingots considering the structural relaxation time. When C(TiO2) = 6 wt% (9 wt%) at TF = 870°C, T(zero-CTE) become -39°C (94°C). When TF = 770°C, 870°C, or 970°C at C(TiO2) = 7 wt%, T(zero-CTE) become -30°C, 5°C, or 40°C, respectively. We can obtain higher T(zero-CTE) by using glasses with lower C(OH) because TS increases as C(OH) decreases and higher TF are acceptable. We demonstrate that TiO2-SiO2 ULE glasses with T(zero-CTE) ranging from -74°C to 145°C will be available in C(TiO2) ranges of 6 to 9 wt%, TF ranges of 770 to 1110°C, and C(OH) ranges of 0 to 1000 wtppm.

8322-80, Poster Session

Extension of PTB's EUV metrology facilities

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After developing metrology with synchrotron radiation in its laboratories at the electron storage rings BESSY I and BESSY II for more than 25 years, PTB extends its capabilities for EUV metrology with the EUV beamline at the Metrology Light Source. With the new instrumentation PTB is prepared for the metrological challenges when EUV lithography changes over from R&D to pilot production. PTB's EUV reflectometer for large optical components, e.g. collector mirrors for LPP sources, will be transferred to this new dedicated EUV beamline. This allows us to offer services to customers independently of the operation schedule of BESSY as a basic research facility with its regular shut-down times. The new beamline also provides much higher radiant power in the EUV spectral range up to 50 nm wavelength. This will particularly benefit the characterization of sensors regarding responsivity and stability, and characterization of optical components in the out-of-band spectral range. Reliable detector characterization is the basis for source-powermeters or tool-internal sensors. With a new combined ellipso-scatterometer to be installed at the current beamline at BESSY II we will expand our scatterometric capabilities to characterize optical components regarding their polarization properties as well as light scattering for e.g. flare estimation. We present an updated overview of our new metrological capabilities with recent measurement examples.

8322-81, Poster Session

Mirror contamination and oscillatory behavior during EUV reflectivity analysis

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Next generation lithography will use EUV light at 13.5 nm to produce feature sizes of less than 20 nm. Already designs have been proposed using Sn plasma sources, and Ru capped Si/Mo multilayer mirrors to efficiently reflect the 13.5 nm light at near-normal incidence. The single Ru layer can also reflect this particular wavelength at grazing angles, and therefore behave as a mirror. Because the multilayer mirrors are susceptible to mixing upon heat,[1] the necessary vacuum chambers which will house the lithography setup will not be able to be baked out. As a matter of fact, contamination of the Ru layer has become one of the main concerns. While some recent research have focused on in- and ex-situ cleaning techniques,[2] others are currently focusing on how the formation of carbon and oxygen on ruthenium actually occurs and how this affects the reflectivity.[3]

We investigated Ru mirror contamination and subsequent EUV reflectivity loss using the IMPACT facility at Purdue University. Real-time contamination of Ru surface is examined using extreme-ultraviolet photoelectron spectroscopy (EUPS). This approach is extremely sensitive to topmost atomic layers, as the photoelectron escape depth is only few angstroms. Results showed that there is a buildup of secondary electrons with increasing coverage of adsorbents. Using the change in work function, we show the formation of dipoles on the surface and the rearrangement of charge. The overall polarity of the contaminants may affect the electron scattering that degrades the photomasks.

During the contamination process, the EUV reflectivity of the ruthenium not only degraded but also showed an oscillatory behavior. The oscillatory behavior in EUV reflectivity is explained due to the competition between oxidation and carbonization processes on the Ru surface. We examined the angular dependency of XPS intensity at the O1s and Ru3d regions under the effects of sputtering and showed that there is almost no change in grazing angles, while higher angles showed more change in intensity. This can be attributed to the coupling of the electric field (vertical to the beam direction) with the components of the depositing molecules, which causes preferential adsorbing of the EUV light. Finally the angle-dependent components are examined, and showed that water and oxidized carbon are most intense at lower emission angles, and primarily degrade the reflectivity of the Ru layer while OH is dominant at higher angles, and suppresses the optical transmission coefficient. Atomic carbon is found to peak at 30 degrees, and most likely plays an important role in degrading both properties.

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8322-82, Poster Session

Modeling and optimization of mass-limited targets for EUV lithography

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Current challenges in the development of efficient LPP sources for EUV lithography are increasing EUV power at IF and maximizing lifetime and therefore, reducing cost of devices. Mass-limited targets such as small tin droplets are considered as the best choice for cleaner operation of the optical system because of lower mass of atomic debris produced by the laser beam. The small diameter of droplets, however, decreases the conversion efficiency (CE) of EUV photons emission, especially in the case of CO2 laser, where laser wavelength has high reflectivity from the tin surface.

We investigated ways for improving CE in mass-limited targets, considering in our modeling various possible target configurations: from the solid/liquid droplets subjected to laser beam energy with different intensities and laser wavelength and with double-beam lasers - for pre-pulse and main pulse with adjusted delay between them; to composition from the small tin fragments exposed to the laser beams with different parameters. We evaluated the dependence of target vaporization and effect of fragmentation, which can be produced as a result of droplet heating by pre-pulse laser energy, on target configuration, size, and composition. As consequence, we studied the influence of these conditions and parameters on the CE and debris mass accumulation.

For better understanding and more accurate modeling of all physical processes occurred during various phases of laser beam/target interactions, plasma plume formation and evolution, EUV photons emission and collection, we have implemented in our HEIGHTS package state-of-the art models and methods, verified, and benchmarked against laboratory experiments in our CMUXE center as well as various worldwide experimental results.

8322-83, Poster Session

In-situ Sn contamination removal by hydrogen plasma

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EUV light must be produced by plasmas, which deposit condensable Sn fuel onto the collector optic. This reduces efficiency and eventually

necessitates replacement of the collector. In-situ cleaning, however, can increase the effectiveness of the collector and lengthen the time before replacement. As Sn is the leading candidate for EUV fuel, this paper focuses mainly on the reduction of Sn fuel contamination. The use of hydrogen plasma to selectively etch Sn from Si surfaces has been explored at the Center for Plasma-Material Interactions (CPMI) at the University of Illinois at Urbana-Champaign. Previous studies have investigated the removal of Sn deposited via electron beam evaporation. These studies yielded optimized etch rates of ~125nm/min. In this paper, magnetron sputtering is used as the deposition source instead. Magnetron sputtering gives rise to a rougher and less uniform surface coating, which more closely mirrors the conditions found in an actual EUV source. Both small and large Si samples are used as substrates for Sn deposition. Deposition thickness and uniformity are measured. Also measured are cleaning uniformity and etch rates of Sn. After careful study and experimental analysis, the plasma recipes and cleaning procedures were optimized. SEM and profilometry methods were used to analyze the samples. Successful results are obtained, showing in-situ hydrogen plasma cleaning to be a potential technique for selectively cleaning EUV mirrors.

8322-84, Poster Session

Energetic ion and neutral energy analyzer for extreme-ultraviolet light actinic inspection sources

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The role of the extreme ultraviolet light producing sources is currently two fold. Not only are they used to create the photons used in manufacturing the wafer, but they are also currently being investigated for rapid inspection of masks. Despite being optimized for high brightness, instead of power, these actinic measurement sources still suffer the same issues that are observed in the high power-output laser produced plasma and discharge produced plasma sources. As such, it is necessary that focus be placed on characterizing and analyzing debris mitigation techniques utilized in these sources. The Center for Plasma-Material Interactions (CPMI), at the University of Illinois at Urbana-Champaign, has designed a detector capable of providing energy and species analysis of the energetic ions and neutrals created by the dense (~1019cm-3) and warm (~30eV) plasmas utilized to generate extreme ultraviolet light. The device is capable of measuring up to 14 keV singly charged ions and up to 50 keV neutral species. The ion analysis is precise enough to isolate individual isotopes of ions, and capable of detecting any species coming out of an EUV plasma, including non-fuel components such as electrode material. Such a detector allows the manufacturer to explore the tradeoffs between tool lifetime and efficiency in regards to the utilized debris mitigation techniques. CPMI has used the electrostatic energy analyzer to analyze the emitted ion spectrum of four different EUV light sources in the past, but the addition of a neutral detector to the tool allows for the rest of the debris mitigation story to be told. Ultimately the combined neutral and ion energy analyzer provides a way for metrology source manufactures to optimize their tools.

8322-85, Poster Session

EUV assist layers for use in multilayer processes

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Extreme ultraviolet (EUV) exposure is among the front-runners for single-exposure lithography for the 16-nm node and below. Previous work has shown that assist layers are critical for performing the EUV lithography process. Assist layers enhance the adhesion of EUV photoresists, block substrate contamination, and improve the resolution, line width roughness, and sensitivity (RLS) trade-off. As materials progress from development to manufacturing, they must mature to align with industry needs.

To bring devices produced using EUV lithography to reality, we believe that a trilayer process will be required. The requirements for a trilayer process include utilizing assist layers with a good etch selectivity to the carbon-rich etch transfer layer (ETL) and the photoresist coupled with good lithography results.

In this paper, we report the study of new assist layers with novel resins that have shown superior lithography performance, along with high etch selectivity to both the ETL and the photoresist. We have demonstrated how to significantly improve the lithography with the benefits of the pattern transfer requirements for trilayer processing.

8322-86, Poster Session

High-brightness electrodeless Z-Pinch™ EUV source for mask inspection tools

D. Gustafson, M. Partlow, S. Horne, D. Smith, M. Besen, P. Blackborow, Energetiq Technology, Inc. (United States)

Energetiq Technology has been shipping the EQ-10 Electrodeless Z-pinchTM light source since 1995[1]. The source is currently being used for metrology, mask inspection, and resist development [2,3,4]. Energetiq's higher brightness source has been selected as the source for pre-production actinic mask inspection tools. This improved source enables the mask inspection tool suppliers to build prototype tools with capabilities of defect detection and review down to 16nm design rules.

In this presentation we will present new source technology being developed at Energetiq to address the critical source brightness issue. The new technology will be shown to be capable of delivering brightness levels sufficient to meet the HVM requirements of AIMS and ABI and potentially API tools. The basis of the source technology is to use the stable pinch of the electrodeless light source and have a brightness of up to 100W/mm^2-sr. We will explain the source design concepts, discuss the expected performance and present the modeling results for the new design.

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8322-87, Poster Session

Reducing EUV mask blank defects originated at target surface during ion-beam multilayer deposition process

H. Yu, Univ. of Illinois at Urbana-Champaign (United States) and SEMATECH (United States) and Univ. of Electronic Science and Technology of China (China); D. Andruczyk, D. N. Ruzic, Univ. of Illinois at Urbana-Champaign (United States); V. Jindal, P. A. Kearney, T. J. Cardinal, SEMATECH North (United States); Y. Jiang, Univ. of Electronic Science and Technology of China (China)

In EUV lithography mask production, one source of particles is the targets used to make the masks. These targets, which are made of molybdenum or silicon, are sputtered sequentially to deposit bilayer films. A detailed analysis of the targets using scanning electron microscopy (SEM) and energy dispersive X-ray spectroscopy (EDX) revealed that their periphery was rough, with micron-scale hillocks. Modeling shows that if a particular spot on the target surface does not sputter as much as its neighbors, then once the surrounding surface is removed, that spot is now at a higher elevation and shadows the material behind it. Since the sputtering yield at elevated angles is significantly higher than the sputtering yield at normal incidence, the edges of the rising mesa will be sputtered away much more slowly than the surrounding plane, causing the mesa to appear as if it were growing.

To duplicate this behavior in the lab, silicon targets were sputtered under different ion beam conditions and incident angles to understand the mechanism forming particles on the surface. Experiments at angles of 0°, 35°, 54°, and 75° were conducted for 6 hours. Observing these angles should provide clues as to what is happening with the surface features and the formation of the hillocks. At a 0° incident angle, the surface is smooth and has no features. Even at 35°, the surface is relatively smooth with very few hillock features. As the angle is increased to 54° and 75°, the surfaces become rough, exhibiting numerous hillock features. To determine whether a smooth surface could be recovered, a 0° incident beam was directed on the surface where hillocks had been produced. The resultant surface was basically smooth, devoid of any hillocks, but with an occasional "spike," which was predicted by the computer model. This spike represents an intermediate phase in the particle being sputtered away. Eventually, with a longer exposure, this feature will disappear as well. Another sample, run for 6 hours, alternated between sputtering at 0° and at 54° every 5-6 seconds. It was observed that the majority of surface roughness was removed. It is clear from these experiments that the way to remove the structures on Si that lead to particle formation is to expose the surface to an incident beam of 0° (plus or minus a few degrees) at various points during the sputtering process.

8322-88, Poster Session

Comparison of the impact of SPM-based and acid-free cleaning PORs on EUV mask performance

J. Choi, T. Shimomura, SEMATECH North (United States); H. Lee, J. Yoon, SAMSUNG Electronics Co., Ltd. (Korea, Republic of); A. Friz, C. Montgomery, SEMATECH North (United States)

Extreme ultraviolet (EUV) mask structures are being created in which each layer has a particular role in enhancing performance in EUV refractive patterning. Such EUV mask layers have been evaluated for their tolerance to mask fabrication as well as exposure processes. It is known that acid chemical cleaning has the potential to damage EUV mask structures. SPM chemicals can deteriorate tantalum-based absorbers and anti-reflective coating (ARC) layers while ozonated water can aggressively etch the ruthenium capping layer.

We have developed a cleaning process using non-acid chemicals. The cleaning process of record (POR) based on non-acid chemicals results in much less damage to EUV mask films than the SPM or ozonated water POR. Tantalum-based absorber critical dimension (CD) changes induced by the cleaning process, which is the greatest weakness of SPM-based cleaning, significantly improves during the acid-free cleaning POR. Additionally, film thickness as well as EUV and deep ultraviolet (DUV) reflectivity changes in the ruthenium and ARC layers were dramatically reduced using the acid-free cleaning POR.

 In this paper, we will compare the cleaning performance of acid-free and SPM-based cleaning PORs. EUV mask film loss during each POR combined with EUV exposure will be evaluated by measurements of film thickness, roughness, and reflectivity changes. Also, we will examine whether film damage is related to any chemical composition changes in the mask layers during cleaning. Finally, we will briefly address whether cleaning performance and EUV mask film loss are dependent on the different materials used in EUV mask structures.

8322-90, Poster Session

Understanding the ion beam in EUV mask blank production

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One of the major technical gaps to be overcome before EUV lithography can enter high volume manufacturing is the defect level of available EUV mask blanks. Currently, many of these defects occur during the EUV reflector deposition process. The current technology used to deposit this reflector is ion beam sputter deposition. Understanding the properties of the ion beam, and understanding the nature of the plasma in the deposition chamber are critical to understanding defect production mechanisms and their subsequent elimination.

In this work we have studied how the source parameters influence the ion beam divergence, its footprint on the target, and the amount of beam that misses the target and hits the shielding. By optimizing the source parameters we can modulate certain target and shield specific defect types. We have compared this data with models of source performance supplied by the source manufacturer and found general agreement, and have been able to fine tune the theory based on the results of the measurements. Models are being developed to better describe actual source performance. We have also investigated the plasma conditions the ion beam creates in the tool. Understanding this plasma is crucial to understanding the transport of defects from their source to the mask. A well characterized ion beam and plasma will lead to process and tool changes that will reduce defect levels in EUV mask blanks.

8322-91, Poster Session

Light sources for EUVL patterning at 22nm node and beyond

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This paper describes the development of a laser-produced-plasma (LPP) extreme-ultraviolet (EUV) source for advanced lithography applications in high volume manufacturing. EUV lithography is expected to succeed 193nm immersion double patterning technology for sub-22nm critical layer patterning. In this paper we discuss the most recent results from high power testing on our LT1 development system, and describe the requirements and technical challenges related to successful implementation of these technologies. Subsystem performance will be shown including the CO2 drive laser, droplet generation, laser-to-droplet targeting control, intermediate-focus (IF) metrology, out-of-band (OOB) radiation measurements and system use and experience. In addition, a multitude of smaller lab-scale experimental systems have also been constructed and tested. This presentation reviews the experimental results obtained on systems with a focus on the topics most critical for an HVM source.

8322-92, Poster Session

Particle contamination effects in EUVL: enhanced theory for the analytical determination of critical particle sizes

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We refine and extend existing models for mask distortion in Extreme-Ultraviolet-Lithography (EUVL) due to particulate matter entrapped

between the clamping surface of the chuck and the reticle. An analytic derivation of critical particle sizes is shown for various cases, such that the image placement error (IPE) remains within a given tolerance.

Current models in the literature assume a constant pressure acting between the mask and chuck surfaces. In reality, the electrostatic pressure depends on the gap of separation between the mask and the chuck. In this work we analytically solve the classical plate equations in the presence of a gap dependent pressure via Bessel functions. The analysis shows that the gap dependent pressure solution converges to the constant pressure approximation whenever the mask-chuck separation is small in comparison to the thickness of the chuck dielectric surface layer.

Analytic and finite element models that account for mask deformation due to a particle are modeled in the literature via a de-coupled global and local analysis. The global model treats the overall deformation of the mask via a macro-scale plate bending theory and the local model treats the effects of the embedding of the particle in the mask and chuck substrate as well as the particle compression. We newly consider a recursive mesh-refinement scheme for the finite element model in order to efficiently and accurately capture the different length scales involved and then carry out a fully coupled simulation of the mask, particle and chuck in contact. For a given numerical example, the accuracy of the de-coupled analytical formulation as found in the literature is substantiated.

Previous publications model the particle as linear elastic or elastic/perfectly-plastic (Prandtl-Reuss model). Here, we show how to allow for general constitutive laws in the analytic formulation. An example using a more realistic Romberg-Osgood material model shows that softer material response can relax the conditions on the critical particle size. Furthermore, we include in our model the impact of friction and show that higher friction coefficients will decrease the maximum allowable particle sizes.

Lastly, we provide an analytical solution to the crushing of a spherical particle based on the Hertzian contact solution. This solution permits one to analytically explore the relevance of diverse system parameters.

For all cases discussed, critical particle dimensions are derived, in order to keep the effect on the IPE within a given specification. For example a cylindrical aluminum oxide particle with a radius of 10.5 um and a height of 2.3 um will result in an IPE of 1 nm at a chucking pressure of 15 kPa. Accordingly, larger particles should not been accepted for the given error tolerance. Besides the verification of the analytical model via a finite element simulation, our models have been applied to existing experimental data and show good agreement

8322-93, Poster Session

Ion-beam deposition system for depositing low-defect density extreme-ultraviolet mask blanks

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Extreme ultraviolet lithography (EUVL) is the leading next generation lithography (NGL) technology to succeed optical lithography at the 22 nm node and beyond. EUVL requires a low defect density reflective mask blank, which is considered to be one of the top two critical technology gaps for commercialization of the technology. At the SEMATECH Mask Blank Development Center (MBDC), research on defect reduction in EUV mask blanks is being pursued using the Veeco Nexus deposition tool. The defect performance of this tool is one of the factors limiting the availability of defect-free EUVL mask blanks. SEMATECH identified the key components in the ion beam deposition system that is currently impeding the reduction of defect density and yield of EUV mask blanks. The current research is focused on in-house tool component research reducing their contributions to mask blank defects. SEMATECH is also working closely with supplier to incorporate this learning in next generation deposition tool. This paper will describe requirements for the next generation tool that are essential to realize low defect density EUV mask blanks.

SEMATECH has also identified better understanding of the physics of the deposition process as one of the keys to improve the defect performance of Nexus tools. To accomplish this, SEMATECH is developing detailed models of the deposition processes and tool environments backed with an experimental program to characterize processes and tools. The goal of this effort is to enable model based predictions of defect performance and defect improvement for targeted process improvement and component learning to feed into the new deposition tool design. We present the results of simulating the deposition rate and uniformity of deposited multilayers and the growth of the multilayer on a given defect profile. The paper will also highlight the defect reduction resulting from the process improvement and further potential. The paper will furthermore outline the restrictions inherent in the current tool geometry and components in meeting HVM quality EUV mask blanks.

8322-94, Poster Session

Development of the reliable high-power pulsed carbon dioxide laser system for LPP EUV light source

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Extreme Ultra Violet (EUV) light source is expecting for next generation lithography. For recent several years the source has became most critical issues. In addition especially Laser Produced Plasma (LPP) method EUV light source system is expected for higher output power (>250W) to obtain higher throughput of scanner. To realize such as higher power and also highly reliability for industrial use, the main driver laser is one of the key component. Our LPP EUV light source system is using the high power pulsed carbon dioxide (CO_2) laser as a main drive laser.

Our system is a MOPA system based on a small average power pulsed master oscillator and a cascade of some power amplifiers. The current MOPA system cannot provide more than 25% overall operation efficiency. The main reason is an insufficient power level at initial amplifier stages. Also the thermal managements and dynamic stabilities are very important to realize the mass-production level reliable laser output.

In this presentation, some of the pressing technical challenges of the LPP laser driver, such as efficiency and stability of operation, are shown.

A master oscillator system and a pre-amplifier system based on a novel configuration of a RF-excited CO_2 laser are the key to high efficiency. Over 40% energy efficiency and multi-kW output from 100W level input are predicted and verified in our experimental pre-amplifier. And Multiline amplification is efficient to increase the extraction efficiency in the case of short pulse amplification like this application. Numerical result shows the amplification enhancement as 1.3 times higher than the single amplification. Multiline configuration is applied to the master oscillator and the efficiency of multiline amplification is verified in our experimental amplifier system.

To operate this laser for mass-production level, there are two major critical items. That is the optical cavity stabilities and the dynamic stabilities. The laser is operated with various operation mode such as 1000msec on and 500msec off for die exposure, also several second off for cassette change. The thermal distortion change due to the operation mode is caused in the optical components leading to beam propagation instability. To reduce the performance instability, laser cavity and optics thermal distortion need to suppress in required level. All mirrors are made by low thermal expansion coefficient material and windows are made by low dn/dT material. Also some compensation optical systems are equipped inside of beam pass. At the same time, the dynamic stability is necessary to get stable beam performance. As pointed out above, to realize the industrial ready pulsed CO_2 laser system, all functions should be work together. Latest initial performance and long time operation test results are shown.

8322-95, Poster Session

Comparison of EUV and e-beam lithographic technologies for sub-22nm node patterning

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For the semiconductor industry to remain on the growth trajectory depicted by Moore's Law, patterning solutions at the 22nm node and below need to be defined within the next 1-2 years. The ITRS roadmap identifies several options including 193nm Multiple Patterning schemes, Extreme Ultraviolet (EUV) Lithography, e-beam (or Maskless) Lithography and Imprint.

In this paper, we will focus on two leading technologies: EUV and e-beam lithography and compare the merits and demerits of these patterning methods for 22nm hp and beyond. In our comparison of these two lithographic technologies, we will focus on evaluating common resist platforms for fundamental learning. It is anticipated that we will gain insight into the chemical processes involved in resist patterning with the two different types of ionizing exposure available with EUV and e-beam exposure respectively.

Performance criteria will include evaluating patterning capability in terms of the RLS (Resolution, Linewidth Roughness and Sensitivity) "Triangle of Death" and Pattern Collapse Margin (PCM). Early research results comparing EUV and e-beam exposures are provided below for a chemically amplified polymer bound PAG (PBP) resist platform. Under EUV exposure we have demonstrated 20nm L/S resolution for this platform (Figure 1). In contrast, with e-beam exposure we have achieved 15nm L/S with some collapse (Figure 2). This resolution capability is significant for chemically amplified resists and suggests this resist design concept may be extendable to beyond the 16nm node.

8322-96, Poster Session

Liftoff lithography of metals for extreme-ultraviolet lithography mask absorber layer patterning

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The authors present a process for patterning Extreme Ultraviolet Lithography (EUVL) mask absorber metals using electron beam evaporation and bi-layer liftoff lithography. The Line Edge Roughness (LER) and Critical Dimension Uniformity (CDU) of patterned chrome absorber are determined for varying chrome thickness on silicon substrates, and the viability of the method for use with nickel absorber and on EUVL masks is demonstrated. Scanning Electron Microscope (SEM) data is used with SUMMIT software to determine the absorber LER and CDU. The Lawrence Berkeley National Labs Microfield Exposure Tool (MET) and Actinic Inspection Tool (AIT) are used to determine the printability of the pattern.

8322-97, Poster Session

The study of synthesis and photocuring behaviors of organic silicon modified methylacrylate and acrylate

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The monomers of methylacrylate and acrylate belong to free radical reaction which has quick reaction rate, good performance of seperating from matrix, but poor resist ability. After modified by silicon, the monomers' resist ability, activity of UV-polymerization, solidify capability of resist has been improved, while glass-transition temperature, stickiness of liquid resist has been decreased, and strength of polymer film has been sustained with lower surface energy. Methylacrylate monomer within one silicon atom has already been reported, but methylacrylate or acrylate monomers within two or more silicon atoms have not been reported yet.

8322-98, Poster Session

Tin droplets for EUV sources

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The manufacturing technology of the next generation semiconductor devices is extreme ultraviolet lithography (EUVL). The 13.5nm radiation (2% bandwidth) can be generated from a Laser-Produced Plasma (LPP). Typically the irradiation of Tin droplets by a high power (kW) laser yields a plasma, which is highly emissive in this wavelength window. LPP EUV sources are used for high-volume manufacturing in EUV steppers, as well as for actinic mask inspection and metrology.

The Tin droplet generator constitutes a key component of EUV LPP sources. Pure Tin droplets are found to be the only viable target material for long-term operation. Tin droplets have high conversion efficiency (CE) and can be synchronized with the pulsed lasers used for EUVL. The droplet size, which mainly depends on the nozzle orifice size of the droplet generator, can be adapted to match the number of required EUV emitting ions for each laser pulse. As a consequence, the droplet size also helps to control the plasma debris level.

The LEC droplet dispenser has been developed over years, including studies of different nozzle types, excitation mechanisms, thermal management approaches and contamination control systems. The LEC droplet dispenser is patent pending.

A common problem with Tin droplet generators is the inherent droplet instability. Achieving the required droplet stability for stable EUV emission is challenging, especially with decreasing droplet size.

Two types of instabilities are distinguished: axial (along the droplet train) and lateral instabilities. Axial fluctuations induce laser/droplet de-synchronization and lateral fluctuations lead to variations in the laser irradiation onto the droplet. As a consequence, the overall source stability directly correlates with the droplet generator stability. In order to assist the droplets during their path from formation to irradiation point, a steering system has been developed. The aim of this system is to accelerate toward the laser focus the droplets that are not already directed to the irradiation point. This directly improves the source stability.

In this work, the different droplet instabilities are statistically assessed in time and space by experimental and numerical means: the axial jitter between droplets, the mean droplet train drift, as well as the lateral deviations from the droplet train are presented for the LEC droplet generator. The droplet train instabilities are characterized as function of key operating parameters, such as frequency and backpressure. In the second part of this work, the axial and radial stability improvement with steering system is presented. In the third part of the work, the impact of droplet train instabilities on source stability is derived. The misalignment between droplet and laser is numerically investigated. As a result, the impact of droplet instabilites on EUV emission is quantified.

8322-99, Poster Session

EUV mask blank cleaning process optimization using M7360

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Mitigation of EUV mask blank defectivity is one of the greatest challenges to be solved by the time of EUV lithography introduction for high volume semiconductor device manufacturing beyond 22nm HP node. Cleaning technology is a critical enabler not only to reduce the total defect counts of the EUV mask blanks but also keep their cleanliness during the usage.

Key requirements for the cleaning process are to remove all of removable defects without any added defects from the cleaning itself. According to International Technology Roadmap for Semiconductor (ITRS), in 2013 the cleaning processes should remove defects larger than 25 nm for the 23nm Flash half-pitch node. In addition to defect concerns, damages to fragile surfaces are another challenge. Any damages to a Ru capping layer must be prevented since it causes subsequent damages to a multilayer underneath of Ru, resulting in significant reflectivity loss.

In this work, the cleaning performance has been investigated using M7360 which has 50nm defect sensitivity on Ru capped EUV mask blanks. 50nm is current best sensitivity with keeping 100% capture rate. Particle removal efficiency (PRE) and added defects from the cleaning process were evaluated. We found that reduction of the added defects was critical. In order to clarify the root causes, we characterized them using various metrology tools such as Atomic Force Microscopy (AFM) and Auger Electron Spectroscopy (AES). The result has shown that pit defects were primary source of the added defects. Based on the characterization results, we optimized the cleaning recipes and achieved more than 50% reduction of the added defects. In this presentation, combining with PRE results, we will present total cleaning performance of EUV mask blanks which is able to work for defects larger than 50nm.

8322-100, Poster Session

Modeling ion-beam target interaction to reduce defects generated on target surfaces for EUV mask blanks via ion-beam deposition

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The defectivity of Extreme Ultraviolet (EUV) mask blanks is one of the critical issues involved in the success of EUV Lithography. Particle defects have been observed on EUV masks which have originated from the Silicon and Ruthenium sputter targets used in depositing Mo/Si multilayer structures capped with a thin Ruthenium layer. It has been observed that target surfaces can develop many hillock-shaped features which form during the ion beam sputtering process. Two computer models were developed to study the surface morphology and evolution of a target surface under different ion beam conditions. In one, using a fixed in-line series of points, the model tracks changes in the height, curvature, slope and striking angle of each point along a two-dimensional interface. By tracking these changes, the model applies the dependency that sputter yield has with the striking angle of a surface and removes material accordingly. The model was also designed to include shadowing effects. If a point is shadowed by a feature upstream, ions will not strike that point and no sputtering will occur. Shadowing was found to be a very strong mechanism in the evolution of the model's 2-D interface. One limitation of the model was its inability to accurately represent undercutting, however an extension was developed to take into account undercutting by employing a floating-point system. The other model using the Monte Carlo method to launch incident ions at the proper angle to a surface. Ray tracing is used to determine the strike point and the local angle of intersection with the surface so the appropriate sputtering yield can be used. Results show that even a perfectly flat surface can develop roughness through a stochastic process which can then provide the shadowing required to form the hillock and mesa structures seen in the experiments. Extensive simulations were performed with both models in order to understand the ion-target interaction with the target surface. The sputtering of a target surface was studied from high ion beam energies (1000 eV) to low energies (50 eV) at different angles. As the angle is increased the hillock features become more pronounced, with a steep leading edge. The surface features at higher angles have a shadowing effect which causes the elongation in the surface seen particularly at the higher angles in the experiments. The models were

further developed to accommodate divergence in energy and angular spread of the ion beam. Furthermore, modeling which alternated the step arrival angles with a period of normal incident sputtering was shown to prevent the hillock formation as verified by the experiment.

8322-101, Poster Session

The validity of a simplified model for mask roughness induced LER under off-axis illumination and with dense and isolated lines

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As the total line-edge roughness (LER) budget nears the single nanometer regime for future nodes, the employment of extreme ultraviolet lithography (EUVL) must take into account every LER contribution, including that due to the resist, on the mask, and mask surface roughness. While much effort has gone into predicting resist LER and mask LER allowances, contributions due to mask roughness induced LER to this point have been largely ignored and unspecified in the International Roadmap for Semiconductors. As the LER contribution due to mask surface roughness can very easily be on the order of several nanometers for out of focus conditions, it is important to have a means to predict it with ease as a function of NA, illumination type, defocus, feature size, and mask roughness properties. Recently, a new simplified model has been proposed for faster modeling and prediction of mask roughness induced LER based on those parameters. We extend that work and verify the validity of this simplified model across the gamut: from conventional disk-type illumination to off-axis illumination configurations, from dense lines and spaces to isolated ones, down to the 16-nm half pitch, and all through focus.

8322-102, Poster Session

Tradeoffs in mask architecture: dealing with future illumination angular diversity

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Extending EUV lithography to future nodes will lead to significant mask challenges. Higher-NA systems will come with larger angles of incidence on the mask, which further complicate the well-known shadowing problem. Addressing them may require the use of thinner absorbers. At the same time, however, the larger mean angle along with a larger diversity of illumination and diffraction angles can also lead to image degradation. Here we perform a modeling based study to explore the relative importance of these two effects for the 11-nm half pitch node. Specifically, we sacrifice reflectivity for increased angular bandwidth by reducing the number of layers in the multilayer stack. We further explore alternate absorber and multilayer designs in an attempt to mitigate these problems.

8322-103, Poster Session

Mask shadowing and the line-edge transfer function

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Owing to the mask-side non-telecentricity resulting from the reflective nature of extreme ultraviolet lithography (EUVL), mask shadowing is well-known to be an issue for EUVL. The shadowing problem is also expected to become more severe as numerical apertures are increased in the future and even larger mask illumination angles become required. Although the

shadowing problem in general has been well studied, the impact this effect might have on the transfer of line-edge roughness (LER) from the mask to the wafer has not been studied. Here we extend previous efforts in the analysis of the LER transfer function (LTF) to explicitly include 3D mask effects. We show that the LTF differs for the shadowed and non-shadowed directions: moreover, the LTF of the left-side edge differs from the right-side edge in the shadowed direction. Finally, we also observe a breakdown of the linearity of the LTF for shadowed features.

8322-104, Poster Session

Cleaning of EUV substrates for mask blank defect reduction

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Analysis of defects on a champion mask blank at SEMATECH indicates that close to eighty percent of the defects originate from substrate and most of them are pits. Substrate cleaning processes are known to induce pits on surface through the physical cleaning mechanisms such as megasonics used for particle removal. Control of megasonic processes is essential for efficient particle removal without pit generation. Cleaning of finished mask blanks is also challenging due to EUV reflectivity loss, roughness increase and multilayer etching associated with standard cleaning processes in a spin-spray mask cleaning tool. Zero pit generation and no reflectivity loss and no loss in uniformity is desirable while mask blank cleaning. This paper focuses on the progress in pit reduction while cleaning EUV substrates at SEMATECH. In addition, mechanism of pit generation in substrates, progress made in reduction of total added defects on substrates, including particles, from cleaning processes is presented.

Megasonics at 1 Mhz, which is used as the primary mechanism for particle removal from EUV substrate and blanks, has been identified as the major source of pit generation at 40 nm - 80 nm SiO_2 equivalent size. Pit generation depends primarily on the frequency of the acoustic wave and also on the acoustic pressure. Pits are generated by cavitation bubbles collapsing on the surface, the size of which reduces with increasing acoustic frequency. In this paper it is demonstrated that zero pit generation at the size levels discussed above is possible on EUV substrates by moving to a megasonic transducer at 3 MHz rather than 1 MHz.

8322-105, Poster Session

Longer wavelength EUV lithography (LW-EUVL)

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To meet the needs of sub-22 nm device generations, alternatives to optical lithography must be implemented. Extreme UV Lithography (EUVL) is the leading candidate for this next generation lithography. EUVL has occupied the ITRS for at least 15 years and has been principally associated with 13.5 nm as a consequence of the silicon (Si) and molybdenum (Mo) multilayer reflective film stack. When film stacks were originally designed for EUVL, the Si/Mo film stack combinations provided the required material compatibility, stability and high reflectivity in the EUV regime, however; EUVL was not originally placed on the ITRS for device generations as small as sub-22 nm. Decreasing the EUVL wavelength to as low as 6 nm has been discussed to account for the resolution desired. Although resolution scales with wavelength, an increase in wavelength provides a better alternative to meet the requirements of sub-22 nm device generations.

In the EUV regime, optical properties are determined by the interaction or radiation with valence electrons as well as its inner electrons. As a result of these interactions, it is possible to optimize multilayer film stacks that exhibit high reflectivity for the desired wavelength. The optimized Si/Mo film stack at 13.5 nm has a peak reflectivity of 76%. Aluminum (Al) based

multilayer optics can provide strong reflectivity at 17.2 nm. Theoretical results for optimized aluminum based film stacks show reflection near 80%.

Higher resolution is achievable with lower wavelength lithography, but it comes with a tradeoff. As wavelength decreases flare increases proportionally with the relationship $1/\lambda 2$. Flare has negative effects on line edge roughness (LER), depth of focus and exposure latitude. Due to the relationship between flare and wavelength, it is possible to change the wavelength slightly in order to significantly change the amount of flare in the system.

One major problem with EUV sources is the power output. Classically, xenon has been used to produce emission lines at 13.5 nm. By changing wavelengths it is possible to investigate new elements with higher emission lines than that of xenon at 13.5 nm. Oxygen has an emission line at the desired 17.2 nm that exceeds xenon at 13.5 nm.

In addition, sensitivity has been a common problem in EUV resists due to the low power output of the sources. Fluorinated resists have been developed to increase the sensitivity of resists by taking advantage of fluorine's absorption coefficient. As wavelength increases from 13.5 nm to 17.2 nm, so does the absorption coefficient of fluorine. Fluorinated resists will be more effective at longer EUV wavelengths.

Many problems can be solved with the implementation of LW-EUVL. Using longer wavelengths will ensure higher reflectivity in multilayer mirrors, less flare, higher source power, and more sensitive resist. In order to overcome the challenges on the ITRS for EUVL, the operating wavelength must increase.

8322-106, Poster Session

A simulation study of cleaning-induced EUV reflectivity loss mechanisms on mask blanks

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It is widely recognized in the EUV industry that getting to defect-free masks is extremely critical in achieving high volume chip manufacturing yield beyond the 22 nm half-pitch node. Total defectivity of a EUV mask depends on the defectivity of substrate and finished mask blank. Finished mask blanks are normally subjected to a cleaning process to get rid of the loosely adhered particles on top of the mask. This is normally done in a spin-spray mask cleaning tool using traditional mask cleaning processes. It is highly important that this cleaning process does not degrade the properties of the multilayer blank or introduce additional particles or pits during the process. However, standard cleaning processes used to clean multilayer blanks result in EUV reflectivity loss, loss of uniformity in reflectivity, increased roughness and adds pits and particles at 40 nm on mask blanks. The standard cleaning process used consists of various steps, each of which may cause the oxidation of Ru capping layer as well as other underlying bilayers, etching of the multilayer stack and increased roughness of the bilayers thus leading to a loss in EUV reflectivity. It is a challenging task to experimentally correlate the processing steps to the resulting damage and to quantify the reflectivity loss. Furthermore, due to the high cost of materials it is impractical to do any kind of extensive experiments to determine the root cause of problems.

In this work, we have synergistically combined mask blank cleaning using standard processes, TEM cross section studies and simulations to quantify the impact of the multilayer oxidation, etching and roughness on the EUV reflectivity loss and mask blank degradation. Comparisons are made with the experimental reflectivity loss to determine and quantify the contribution of each step to the degradation in reflectivity and multilayer loss due to etching by chemicals. Based on the improved knowledge of reflectivity loss mechanisms, and knowledge which cleaning steps cause what type of damage, mask blank cleaning processes are modified and optimized to reduce their deteriorating impact on the EUV mask blanks.

8322-107, Poster Session

A pathway to resolving RLS tradeoff in EUV lithography: underlying assist layers

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At present, the development of EUV resists has run into serious challenges to effectively take advantage of the high imaging contrast provided by the projection optics employing the short EUV wavelength. The main challenge is how to improve resolution and sensitivity while reducing line width roughness, i.e. resolve the resolution-linewidth-roughness-sensitivity (RLS) tradeoff. In addition, other requirements for making this technology successful in HVM, such as low outgassing of key components and insensitivity to out-of-band irradiation, have made the design matrix in resist formulation very complex. On the other hand, anti-reflective property of the underlying buffer layer has become less critical, allowing it to take on a more active role in the modulation of lithographic performance.

In this study, we examine the process performance enhancement in EUV Lithography using underlying assist layers as a pathway to resolve the traditional (RLS) tradeoff as infrastructure development of this technology is being carried out for its implementation in high volume manufacturing (HVM).

We measure changes in several lithographic performance indices with various assist layer materials and attempt to correlate them with their characteristic optical and chemical properties and establish a model with simplified expression of the property change along the depth in the resist film. Preliminary results indicate that the presence of metal in these layers improves the resist sensitivity up to 20% while maintaining resolution and line width roughness.

8322-108, Poster Session

Effect of extreme-ultraviolet pellicle support to patterned mask

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Extreme ultraviolet (EUV) lithography is about to be realized in mass production even though there are many obstacles to be overcome. The source power is currently the biggest issue besides mask and resist. However, we strongly believe that the source power will reach the target value eventually in the years to come.

Several years ago, EUV pellicle was suggested and studied by some people, but the idea of using EUV pellicle was abandoned by most people because there were big problems that were believed to be almost impossible to overcome. EUV pellicle should be made of inorganic material instead of common organic pellicle and should be very thin due to EUV transmission. In addition to that the support of the very thin pellicle film should be used. The EUV light absorption and thermal increase by the EUV pellicle and the support would change and destroy the original purpose of using the pellicle.

Nowadays, people are beginning to worry about the practical issues in EUV mass production, and the problem of the particles or the contaminations to the mask is the biggest concern to have better yield. This makes people revisit the EUV pellicle.

We have studied the effect of the EUV pellicle support to the mask patterned area among many issues of EUV pellicle in this paper. The structure of the support of the pellicle thin film should not make any noticeable intensity difference on the top of the patterned mask side. However, experimental result of Intel showed the interference images with their suggested support structure.

The following figure shows a typical suggested EUV mask with pellicle. The structure of the support could be honeycomb or regular mesh type with ~ 10 m line and ~ 100 m space width. The height of the support could be ~ 50 um. The distance between the multilayer and the pellicle

would be ~ mm. And the thickness of the pellicle could be ~ 50 nm. The intensity distributions on the top of mask are obtained for various combinations of the above mentioned scale and support structure. The usable structure of the support would be reported as a result and this would open the possibility of using EUV pellicle in mass production.

8322-109, Poster Session

Defect-aware reticle floorplanning in EUVL considering side-to-side wafer dicing

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The blank defect is a critical challenge in extreme ultraviolet lithography (EUVL). Some layout shifting algorithms have been developed to find the best location for a given layout onto a defective blank, such that the defect impact is minimized.

In reality, the die size is usually much smaller than the exposure field. To improve the throughput, there will be multiple copies of a die on each blank. In this case, it is not necessary to always shift all dies together as a whole layout in order to mitigate defect impact. Instead, each die can be shifted separately as long as all layers of the same die are at the same location in relative to the exposure alignment system. In addition, side-to-side dicing is the prevalent wafer dicing technology, which requires the wafer to be diced thoroughly from one side to the other at each cut. And due to the packaging requirement, the blank area at the boundary of each die must be within a certain range. Hence the same row or same column of dies should always be moved together in order to fulfill the wafer dicing and packaging requirement.

In this paper, we develop a EUV reticle floor planning algorithm to maximize the number of effective dies that are immune to defect impact. In the first step, we adopt an efficient layout relocation algorithm to find all candidate positions for every die on the blank. Then the coordinate constraints required by the side-to-side wafer dicing and die packaging are applied to the candidate positions. Finally, we formulate the problem into a dynamic programming problem. In the problem formulation, we simultaneously consider all the layers fabricated by EUVL in order to fulfill the exposure alignment requirement. After wafer dicing, the number of useful dies immune to defect impact is maximized by our proposed floorplanning strategy.

8322-110, Poster Session

Microplasma-pulsed discharge EUV source characteristics

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The roll out of EUV lithography with the associated tools for actinic mask inspections requires specific EUV radiation sources. The radiation at 13.5nm wavelength-band originates from a high energy density plasma at a temperature of 20-40eV. NANO-UV has developed a unique EUV source, CYCLOPS unit, based on a hollow-cathode-triggered micro-plasma pulsed (MPP) discharge, incorporating an intrinsic plasma structure to provide photon collection. Such MPP discharge is characterized by a precursor electron beam producing a tight conductive channel on axis of the capillary. We report here on the light source development, addressing the basic parameters required for high irradiance operating regimes for metrology operation. The source works at 1-3 kHz in a gas admixture at a stored energy up to 0.5J per pulse. Detailed beam light characteristics of the plasma source and measurements on the electrical parameters and the temporal evolution of

the precursor ionization will be discussed in terms of radiation properties observed. Without using external physical optics, the EUV power is delivered in a sub-cm size spot at 74cm distance, with a typical étendue below 10-2 mm2·sr (in 3nm bandwidth around 13.5nm). This low etendue opens up the possibility to increase the power and brightness through spatial and/or temporal multiplexing of such units.

8322-111, Poster Session

Properties of high-intensity EUV radiation plasma sources

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The high intensity radiation in plasma light sources is produced by multicharged ion non-equilibrium plasma. Understanding of complex plasma dynamics and radiation processes is a key issue in power and brightness optimization in radiation plasma sources. The innovative hybrid 2-3D computational code based on the Z* code and its commercially available version Z*BME are designed under international collaborative project FIRE in the framework of FP7 IAPP to model multicharged ion plasmas in experimental and industrial facilities using a hybrid (particle-in-cell + magnetohydrodynamics + non-equilibrium ionization kinetics + multigroup spectral ray-tracing) approach including fast particles and plasma 3D dynamics in an electromagnetic field, the advanced atomic physics models and the spectral radiation transport. The multiphysics code is used to model laser-produced plasma and discharge-produced plasma to understand current physical processes and to optimize on that base the sources by brightness and delivered power for EUV lithographic and metrology applications. The radiation plasma dynamics, the spectral effects of self-absorption in laser-produced plasma and discharge-produced plasma are considered. The radiance and conversion efficiency of laser energy to EUV radiation in LPP is discussed. The generation of fast electrons and an enhancement of the radiance of a fast micro-plasma pulsed discharge created in a capillary wall confined structure is optimized.

8322-112, Poster Session

50X, 75X mask cleaning effects on EUV lithography process and lifetime: lines and spaces, contacts, and LER

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In this study we examine the effects on lithographic performance due to repetitive cleans on a mask patterned for use in extreme ultraviolet lithography (EUVL). Exposures were carried out at the SEMATECH Berkeley micro-exposure tool (MET) on both a cleaned mask and a reference (uncleaned) mask with the same mask architectures. The performance is measured against the process window for lines and spaces and contact size variation measured using scanning electron microscopy (SEM). We also introduce a new method involving the correlation in LER of a single line from exposure to exposure at the same dose and focus. If mask cleaning were to introduce significant damage to either the capping layer or the absorber, we would expect an increase in LER correlation from exposure to exposure of the same feature, as uncorrelated effects due to the resist would be unaffected by the cleans. We look at these metrics on the same mask used in previous cleans studies, now for a 50X and 75X cleans.

8322-113, Poster Session

3D mask modeling for EUV lithography

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With the shipment of the first EUV preproduction tools to different facilities worldwide, the field of EUV lithography has moved forward significantly. Scaling down to a wavelength of 13.5nm for EUV lithography requires dedicated optics, materials, and above all reflective reticles. LTEM (Low Thermal Expansion Material) substrate, multilayer stack, and an absorber material define the standard EUV mask design. However, the short wavelength and mask stack induce new imaging effects which need to be carefully captured through the computational lithography. Two typical EUV effects are the mask shadowing and flare. The EUV mask absorber height and the non-telecentric illumination, at mask level, modulate the captured intensity from the shadowed area through the reflective optics to the wafer. Moreover, a non-zero reflectivity can be observed by thinning the mask absorber height, resulting in unwanted background intensity. A true compromise has to be taken into account for the height parameter of a EUV mask absorber. In this work, 3D mask modeling capabilities will be used to assess mask topography impact on imaging through slit including off-axis illumination. Then, the findings will be validated against experiments on new generation EUV scanner. Masks with two different absorber heights, standard thickness and thinner version, will be evaluated on various features containing line/space down to 27nm half-pitch and contact-hole down to 32nm half-pitch. We will discuss the state-of-the-art 3D mask modeling capabilities, and will present various methodologies to tackle the described EUV imaging effects.

8322-114, Poster Session

Particle mitigation in mask blank deposition tools

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Extreme ultraviolet (EUV) lithography is the leading contender for adoption as the next generation lithography technique. One of the critical challenges in this technology is producing defect-free masks. These masks are mainly fabricated by ion beam deposition. Particles generated during this process often deposit on the mask blank during the formation of multilayers and result in phase and amplitude defects. These defects translate into insufficient intensity contrast, causing defects to print. Hence, it is important to study the transport and behavior of particles in the ion beam deposition tool as well as their generation in the tool itself. Exploring the effect of the ion beam on the transport of particles in the chamber is likewise important. The experimental setup for this study requires that particles greater than 10 nm be detected. Particles larger than about 50 nm can be detected by optical particle counters (OPCs) while particles greater than about 5 nm can be detected by condensation particle counters (CPCs). However, CPCs work only at atmospheric pressure while ion beam sputtering is a vacuum process. We show results in overcoming this challenge and detecting particles in low vacuum systems while also studying particle transport and behavior when using an ion beam. We also show results of using OPCs and CPCs to detect particles generated in ultrahigh vacuum valves.

8322-115, Poster Session

Development of fiducial marks on EUV blanks for defect mitigation process

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Defect free EUV mask is one of critical issues to implement EUV lithography at 22nm hp and beyond. Defectivity on ML (Mo/Si Multilayer) blanks has been steadily improved by modification of fabrication process toward the requirement of zero defects over 20nm. Several kinds of mitigation techniques for defects originated on ML blanks have been developed to relax the defect requirement as practical approach.

Fiducial marks are required on EUV blanks to precisely manage the defect position for a defect mitigation process. High position accuracy in a defect inspection and an EB writing tools is very important for more effective mitigation process. In order to completely cover a defect under an absorber pattern, repeatability of a position on the marks during EB scan in and EB writing process should be within 10nm 3 . Furthermore, defect control in fiducial mark making process is difficult challenge to achieve zero additional defects on an EUV blank.

We developed several kinds of fiducial marks on EUV blanks, and evaluated position accuracy on the marks in a defect inspection process and an EB writing process. Fiducial mark with nearly vertical side wall was successfully made on an EUV blank. Good contrast on the mark was observed in a blank inspection and an EB writing processes. High position accuracy of less than 3nm in an EB writing process was achieved on the fiducial marks. We also evaluated defect quality on the blanks caused by a fabrication process of fiducial marks. A process with nearly zero additional defects was developed for making fiducial marks on EUV blanks. In this paper, the details of fiducial marks on EUV blanks will be presented.

8322-116, Poster Session

Impact of shadowing effect on OPC strategy for contact layer

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Extreme ultraviolet (EUV) lithography is a leading technology for patterning 16nm and smaller node device. One of the new physical effects that need to be considered in EUV is the shadowing effect from the interaction of mask absorber topography and the oblique illumination in the EUV system. It causes features to print differently depending on their orientation (Horizontal and Vertical) and position in the reticle field, and is often referred to as the H-V CD bias. Shadowing effect can be accurately accounted for in the EUV model fitting process, which enables model-based shadowing effect correction in the existing mask synthesis flow. However, H-V CD bias from the shadowing effect poses new challenges to OPC especially for contact layers.

In this paper, we demonstrate the simulated OPC result on a random pitched square contact test layout using the traditional single-segment correction method, which is usually favored due to its performance advantage. A strong H-V CD bias is noticed in the post-OPC contour simulation, whereas OPC is expected to compensate for the H-V bias caused by the shadowing effect and to show an approximately equal distribution between Horizontal and Vertical CD errors. To achieve near 50/50 distribution of H-V CD bias on the square contact layout, a multiple segment cost based solver, which is often used in low K1 lithography OPC to address the strong interaction between neighboring segments, is used to correct the four contact segment edges simultaneously. The H-V CD bias can be well compensated with the multiple segment cost based solver and near 50/50 H-V CD distribution is achieved. In addition, correction quality in terms of EPE is further improved compared to the single-segment correction method. The phenomenon of strong H-V CD bias on contact layout with single-segment solver OPC is also discussed analytically in this paper.

8322-117, Poster Session

Line-width roughness control for EUV patterning

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Controlling line width roughness (LWR) is a critical issue in extreme ultraviolet lithography (EUVL). High sensitivity, high resolution, and low LWR are required for EUV lithography resist. However, it is difficult to achieve optimal properties simultaneously through chemical tuning alone. The track process is one of the factors that impacts LWR. Enhancing the track processes used in EUV lithography is necessary to control LWR.

 This paper describes our approach to mitigating LWR based on optimizing the track-based process and etch-based process. It will also present the results of our newly developed track-based smoothing process as well as the results of combining several track-based techniques. The latest LWR performance from using track-based techniques, optimized track processes and etch-based techniques will be included.

8322-119, Poster Session

Applicability of e-beam mask inspection to EUV mask production

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The installation of multiple EUV scanners in the field signifies the transition into the early learning phase, although at significant delays. As it becomes clear that pre-production phase will occur at below 20nmHP, it also becomes obvious that this will happen at the limiting edge of existing 193-based patterned mask inspection technology, reaching the practical resolution limits at around 20nm HP mask densities. Resolution is coupled with sensitivity and throughput such that the extended sensitivity may come at an unreasonable throughput. Loss of resolution also badly impact defect dispositioning, or classification, which becomes impractical. As resolution is especially critical for die to database inspection, single die masks and masks with high flare bias are at risk of not being inspectable with 193nm based inspectors.

E-beam based mask inspection (EBMI) was proposed and demonstrated as a viable technology for patterned EUV masks. We studied the key questions of sensitivity, throughput, dispositioning, classification in both die-to-die and die-to-database applications. We present new results, based on new generation of e-beam inspection technology, having higher data rate at smaller spot sizes. We demonstrated the feasibility of acceptable inspection time with EBMI. We discuss defect dispositioning and decision flow on EBMI inspections. We also discuss die-to-database inspection and the advantage of using e-beam for meeting future requirements of single die EUV mask inspection or under high flare bias conditions.

8322-120, Poster Session

Coherent short-wavelength plasma light for EUV metrology

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Extreme ultraviolet lithography (EUVL) is the leading patterning technology for IC fabrication below the 22 nm half-pitch node, whose implementation relies on EUVL masks that are free of printable defects. While plasma-based incoherent EUV sources are still not meeting the aggressive industry power specifications, alternative coherent

EUV sources deserve attention for characterizing masks defects at-wavelength. In this respect there is an imaging benefit derived from coherence that could mitigate the specification of in-band power requirement. The University of Bern's EUV laser "Beagle" is a high brilliance (>1026 ph s-1 mm-2 mrad-2 0.1%BW) and narrow linewidth (< 0.01%) source that delivers up to 1011 EUV photons within 2.5mrad collimation, thus eliminating the need for collection optics. Thanks to the impressive improvement in brilliance in the last few decades, especially using grazing incidence multiple pre-pulses and target micro-technology, masks with nano-sized defects can be exposed with a ultrafast single shot on a field of view of approx. 10x10 m. Our exposure chamber has been here equipped with Y/Mo multilayer optics array coupled to Sn laser emission at 12nm, which has provided reliable performance, in terms of illumination and lifetime. No damage was produced to the multilayers for exposures up to 200 shots, since the EUV laser radiation is collimated and the optics can be mounted away from the debris stream-field. The current footprint of the research system is dictated by the optical engineering of our pulse stretching/compression to less than 10 m2 layout, which is further shrinkable in planned commercial platforms. In this paper the experimental data are complemented with simulations.

8322-121, Poster Session

AIT and print validation of EUV multi-layer defect recovery using computational lithography

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Research in EUV is currently focused on detecting and reducing defects on blanks and patterned masks. Bumps and pits found on blank substrates are of particular concern since they cause phase changes and often print under EUV conditions. Given that EUV blanks and patterned masks are currently being inspected with high resolution DUV or e-beam based systems, both detecting and assessing the impact of these defects pose challenges. Even with an EUV AIMSTM, expected in 2014, the location, size, shape, and profile of buried multi-layer defects will still be needed to determine their print impact and possible repair schemes.

In previous papers*, we proposed the use of computational techniques to "recover" buried defect characteristics using the top-surface AFM height profile of the blank or patterned EUV mask in conjunction with a pre-calibrated growth model. The growth model is essentially a forward model, which predicts the shape and height profile of buried bump or pit defects through the multi-layer to the top of the blank surface. This model can be calibrated for a sample with typical buried defects in several ways, for example, by using cross-sectional TEM profiles of buried defects or even by knowing the height and width of a programmed buried defect at the bottom and then at the top of the multi-layer. Using this growth model and the surface profile of the buried defect as indicated in AFM images, the exact nature of the buried defect can be recovered. Knowing the height, shape, and location of the bump or pit defect then allows its printability impact to be estimated by an EUV simulator. This Defect Printability Simulator (DPS) is a fast and accurate EUV simulator with flexible mask, pattern, and exposure condition inputs. Furthermore, the DPS engine can be modified and used to compute changes to the absorber pattern that will compensate for the buried defect's printability affects, i.e., Luminescent's Multi-layer Defect Compensation (MDC).

In this paper, both AIT and wafer print data are used to validate this computational approach to multi-layer buried defect recovery. The initial data are encouraging and promise to enable EUV defect printability and EUV mask repair work 3-4 years ahead of any actinic review tools being available, which will facilitate EUV mask pilot-line operations both in the short- and long-term.

* Pang, L., Peng, D., Hu, P., et al., "Expanding the applications of computational lithography and inspection (CLI) in mask inspection, metrology, review, and repair," Proceedings of SPIE Vol. 7971, 79712A (2011)

* Tolani, V., Satake, M., Hu, P., et al., "EUV mask absorber and multi-layer defect disposition techniques using computational lithography," Proceedings of SPIE Vol. 8166, 81660J (2011).

** Pang, L., Hu, P., Satake, M., et al., "EUV multilayer defect compensation (MDC) by absorber pattern modification: from theory to wafer validation," Proceedings of SPIE Vol. 8166, 81662E (2011).

8322-51, Session 11

From performance validation to volume introduction of ASML's NXE platform

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With the completion of the shipment of six NXE:3100 Step & Scan systems to Semiconductor Manufacturers we are now in the next phase of EUVL implementation into IC manufacturing. Since 2006 process and early device verification have been done using the two ASML Alpha Demo Tools (ADTs) located at IMEC in Leuven, Belgium and at University of Albany, New York, USA. With the shipment of these six NXE:3100's to IC manufacturers, the focus has shifted to the integration of EUVL exposure tools into a manufacturing flow, preparing high volume EUVL manufacturing - expected to start in 2013 with the second generation (0.33NA) of the NXE platform.

ASML's NXE platform is a multi-generation TWINSCAN platform using an exposure wavelength of 13.5nm, featuring a plasma source, all-reflective optics, and dual stages operating in vacuum. The NXE:3100 is the first generation product of this NXE platform. With a 0.25 NA projection lens, a planned throughput of 60 wafers/hr and dedicated chuck overlay of 4 nm, the NXE:3100 is targeted for EUV implementation at 27nm half-pitch (hp) and below. The second and third generation 0.33NA NXE tools include off-axis illumination for high volume manufacturing at a resolution down to 16nm hp and a targeted throughput of >100 wafers/hr.

We will share details of the performance of the 0.25NA lithography products in terms of imaging, overlay, and throughput. We will highlight imaging results using both conventional and off-axis illlumination, and will show that we have met the required imaging performance associated with the 27nm hp node. The paper will also include a summary of the status of EUV source development, which is a key enabler for successful cost-effective introduction of EUVL into high-volume manufacturing.

Later on in 2012 ASML plans to start shipping the first 0.33NA Step & Scan systems to end users. These scanners are targeted for the 22nm hp node imaging and associated overlay. We will highlight some of the technical changes we introduced to enable the transition from 27 to 22nm lithographic performance.

Finally, we will speculate on the opportunities for extensibility of EUVL well into the 1x nm node region.

8322-52, Session 11

Status of the laser-assisted discharge produced plasma (LDP) technology

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XTREME technologies is committed to the development of EUV sources for extreme ultraviolet lithography (EUVL) for more than 10 years. Goal is the development of powerful and stable EUV sources that will enable EUVL to transition to high volume manufacturing (HVM). XTREME technologies' innovative LDP (Laser-assisted Discharge Plasma)

technology, which shows scalability in terms of optical power and lifetime, combines the specific advantages of the formerly developed LPP (laser produced plasma) and DPP (discharge produced plasma) technologies while overcoming the inherent limitations of those.

While the plasma is ignited by a trigger laser, which holds the position and the initial shape of the emission volume steady, the main part of the energy is supplied electrically into the plasma. By crossing over the conversion of the electrical energy into laser light before feeding into the plasma, the conversion efficiency of this technology is much higher compared to the LPP technology. The usage of rotating wheels covered by thin layers of tin provides the target material in a mass limited manner. By rotating the electrodes, for each pulse a fresh surface is available and the thermal load is distributed over a much larger area compared to static electrodes. All these specific properties lead to the possibility of scalability towards the HVM requirements.In this paper, we present the current status of development of HVM sources by using the LDP technology. The reliability and lifetime performances of the sources already installed will be presented as well.

8322-53, Session 11

Laser-produced plasma EUV sources for device development and HVM

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Laser produced plasma (LPP) systems have been developed as the primary approach for the EUV scanner light source for optical imaging of circuit features at sub-22nm and beyond nodes on the ITRS roadmap. This paper provides a review of development progress and productization status for an LPP extreme-ultra-violet (EUV) source with performance goals targeted to meet specific requirements from leading scanner manufacturers. We present the latest results on exposure power generation, stable collection, and clean transmission of EUV through the intermediate focus. Semiconductor industry standards for reliability and economic targets for cost of ownership will be provided. We report on measurements taken using a 5sr normal incidence collector on a production system. The lifetime of the collector mirror is a critical parameter in the development of extreme ultra-violet LPP lithography sources. Deposition of target material as well as sputtering or implantation of incident particles can reduce the reflectivity of the mirror coating during exposure. Debris mitigation techniques are used to inhibit damage from occuring, the protection results of these techniques will be shown over multi-100's of hours.

8322-54, Session 11

EUV resist performance: current assessment for sub-20nm imaging on NXE: 3300

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Simulation results show that ASML's NXE: 3300 EUV scanner using 0.33NA and various illumination modes will enable 16-18 nm half-pitch imaging. Resist processes need to be developed to be ready to take advantage of the NXE: 3300 sub-20nm imaging capabilities.

In order to deliver qualified EUV resist process on time for high volume manufacturing using NXE: 3300, an EUV resist evaluation has been carried out using the SEMATECH EUV MET tool with an 18nm dipole illumination setting at Lawrence Berkeley National Laboratory. Multiple state of the art EUV resists have been collected from all major resist vendors. The best performing resists from the exposures on the Berkeley

EUV MET tool have been exposed on the NXE: 3100. In these evaluations the following figures of merit have been investigated: resist resolution capability, depth of focus, exposure latitude, sizing dose and linewidth roughness.

8322-55, Session 12

Model calibration and full-mask process and proximity correction for extreme-ultraviolet lithography

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Extreme ultra-violet (EUV) lithography is a promising solution for semiconductor manufacturing for the 22nm node and beyond. Due to the mask shadowing effect and strong flare, process and proximity correction (PPC) is required for EUV lithography even though the k1 factor is much larger than that in current 193nm immersion lithography. In this paper, we will report a procedure of model calibration and full-mask PPC flow for EUV lithography. To calibrate the EUV model, identical test structures are placed at various locations on the mask across the slit direction. Figure 1 shows the layout of the test structures at one of the mask locations. Mask shadowing effect and both long range and short range flares will be investigated at different locations. The wafer is patterned with a 0.25 NA EUV scanner and measured with CD-SEM for process evaluation and PPC model calibration. Figure 2(a) shows a point spread function of the flare, and Figure 2(b) shows the simulated long range flare map for the layout in Figure 1. The image simulations will be verified by wafer measurements. A PPC flow with mask shadowing effect compensation and model-based flare compensation is introduced to perform full-mask correction for the BEOL flow at 16nm technology node. Post-PPC verification results will also be reported. The turn-around time (TAT) of PPC and verification will be compared to the TAT using a 193nm immersion flow.

8322-56, Session 12

Model calibration and validation for pre-production EUVL

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As Extreme Ultraviolet Lithography (EUVL) enters the pre-production phase, the need to qualify the Electronic Design Automation (EDA) infrastructure is pressing. In fact, it is clear that EUV will require optical proximity correction (OPC), having its introduction shifted to more advanced technology nodes. The introduction of off-axis illumination will enlarge the optical proximity effects, and EUV-specific effects such as flare and shadowing have to be fully integrated in the correction flow and tested.

We have performed a model calibration exercise on the ASML NXE-3100 pre-production EUVL scanner using a Brion Tachion NXE. Model calibration masks have been designed, manufactured and characterized. The masks have different flare levels, as well as model calibration structures through CDs and pitch. The flare modulation through the mask is obtained by varying tiling densities. The generation of full-chip flare maps has been qualified against experimental results. The model was set up and calibrated on an intermediate flare level, and validated in the full flare range.

Wafer data have been collected and were used as input for model calibration and validation. Both one-dimensional and two-dimensional

structures through CD and pitch were used for model calibration and verification. We discuss in detail the EUV model, and analyze its various components, with particular emphasis to EUV-specific phenomena such as flare and shadowing.

8322-57, Session 12

EUV OPC for the 20nm node and beyond

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Although the k1 factor for extreme ultraviolet (EUV) lithography is much larger than state of the art deep ultraviolet (DUV) lithography, pattern correction is still needed. This pattern correction is referred to as EUV OPC, despite the fact that it accounts for more effects than the optical effects compensated for by conventional optical proximity correction. This paper will describe a recent EUV OPC project, analyze the sources of errors in the OPC, and predict the effects of these errors for future nodes. Possible sources of errors which will be examined are: flare due to density variation, flare to due to field spillover on the wafer, flare due to out-of-band radiation, exposure tool lens aberrations, scanner aperture blade position, critical dimension (CD) variation between horizontal and vertical features (H-V bias), electromagnetic mask effects, CD errors on the mask, measurement errors for OPC model building inputs, and possibly other sources of error such as etch.

First, the current status of EUV OPC will be presented with measured wafer data from an EUV OPC test mask exposed on alpha and pre-production scanners with 0.25NA. The test mask used in this work was designed specifically to capture EUV specific effects, especially flare, and the CD bias between horizontal and vertical lines across the reticle. This mask is composed of one cell repeated 28 times to fill the reticle field. The fill is varied to study the effects of flare and build accurate OPC models which account for flare. The repeated cell contains patterns for OPC model building, scatterometry measurements, and realistic patterns to study the effectiveness of current EUV OPC. The target pitch for OPC model building was 64nm, but this mask includes smaller features down to the limit of the mask making process.

Next, the sources of error in OPC will be examined, and the impact of these error sources will be analyzed for future nodes. Along with the impact of each, the ability of OPC software to compensate for these errors will be discussed. In some cases, for example correcting for H-V bias, compensation with OPC software should be possible even if it requires an accurate three-dimensional electromagnetic model or specific rules for each size and type of pattern. For other effects, such as flare spillover on the wafer, OPC may not be able to compensate effectively because the magnitude of the effect will vary for each exposure.

8322-58, Session 12

Development of practical flare correction tool for full chip in EUV lithography

T. Uno, H. Mashita, M. Miyairi, T. Kotani, Toshiba Materials Co., Ltd. (Japan)

Extreme ultraviolet lithography (EUVL) is one of the most promising methods for patterning below 20 nm generation owing to high resolution with small wavelength of 13.5 nm, whereas various double-patterning techniques in ArF lithography are beset by manufacturing issues such as complicated process flow and critical dimension (CD) control. A light scattered by surface roughness of EUV optical mirror is exposed on the wafer as a flare. The flare amount strongly depends on pattern variation within tens of millimeters around the pattern of interest, and causes degradation of CD uniformity in the exposed area. Thus, flare correction is necessary for improving the CD uniformity by resizing mask pattern, as well as conventional optical proximity correction (OPC).

Previous study showed that a model-based correction technique

modulating the simulated aerial image in response to the amount of flare is indispensable for 20 nm generation to satisfy the required correction accuracy because the flare causes CD fluctuation dependent on pattern variation due to off-axis illumination. Full-chip-level model-based correction, however, requires too much time to run simulation since the hierarchical data structure, which can be handled effectively in conventional OPC for memory device to reduce run time, is broken up during flare correction due to a long flare-influence range. Thus, a fast full-chip-level flare correction tool employing the new concept of a flare correction rule dependent on pattern variation has been developed. In our presentation, the performance of the developed EUV correction tool in terms of the accuracy and the run time will be reported.

8322-59, Session 12

Study on CD variation in the vicinity of the exposure field edge in EUV lithography

S. Kim, S. Koo, J. Park, G. Kim, Y. Hyun, C. Lim, D. Yim, S. Park, Hynix Semiconductor Inc. (Korea, Republic of)

World-wide effort of introducing EUV lithography into semiconductor fabrication processes has brought significant progress recently but still reveals even more challenges. CD uniformity control of EUV lithography is one of them. In this study, we investigate the variation of CD in EUV lithography especially in the vicinity of exposure field edge.

More than 14 times shorter wavelength of EUV source has made the flare of EUV optics very popular research topic, but there has not been relevant emphasize on the flare from adjacent field. The existence of contamination preventing hardware in EUV systems makes it more complex to analyze this leaked flare from neighbor field. In addition, reflection of EUV and DUV light from black border area on mask and REMA needs to be taken into account.

The influence of the flare from adjacent field and the reflection of black border and REMA on CD variation in EUV lithography is investigated by intensive sampling of CD measurement and split of mask border condition and REMA open settings. It will be reported also, how large area is affected by the flare from adjacent field and the reflection of REMA and so forth. Two EUV scanners, alpha demo tool and pre-production tool are used for the experiment and the difference between two tools will be mentioned as well.

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8323-01, Session 1

Future of multiple e-beam direct-write systems

B. J. Lin, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

The crossover of high-speed digital electronics, MEMS, and cost reduction presents an exciting opportunity to extend optical lithography with multiple e-beam direct write systems. Massive parallelism overcomes the throughput limitation of e-beam direct write systems. Many innovative concepts on multiple e-beam imaging have been conceived and are being developed for various applications. Are these systems suitable for high volume semiconductor manufacturing? Will they have acceptable resolution, overlay accuracy, and processing window? How extendable are these systems? What is the required infrastructure? What are the cost and schedule targets, and for which technology nodes? How do they compare with competing imaging technologies such as immersion lithography and EUV lithography? Are there unique niche applications or killer applications for multiple e-beam direct write systems? We will address these questions with updated data and proposals.

8323-02, Session 1

Block copolymer directed self-assembly enables sub-lithographic patterning for device fabrication

H. P. Wong, Stanford Univ. (United States); C. Bencher, Applied Materials, Inc. (United States); H. Yi, Stanford Univ. (United States); X. Bao, Applied Materials, Inc. (United States); L. Chang, Stanford Univ. (United States)

In this paper, we review recent progress in using block copolymer directed self-assembly for patterning sub-20 nm contact holes for practical circuits.

Recognizing that typical circuit layouts do not require long range order, we adopt a lithography sub-division approach akin to double-patterning and spacer patterning. To illustrate the use of this small template DSA approach, we use 193 nm immersion lithography to print the templates for 22-nm node SRAM cells reported by IBM. Using conventional reactive ion etching, DSA contact hole patterns are transferred to dielectric layers and subsequently filled with metals that make electrical contact to the devices.

8323-03, Session 1

Jet and flash imprint lithography: status and roadmap to manufacturing adoption

S. V. Sreenivasan, Molecular Imprints, Inc. (United States)

Jet and Flash Imprint Lithography (J-FILTM) has demonstrated remarkable replication capability down to sub-10nm resolution. Translating this nano-scale resolution to a commercially viable manufacturing approach requires addressing key challenges in tools, materials, masks (templates) and processes that can achieve reliable nano-scale performance at reasonable cost. The speaker will provide an overall status of J-FIL technology and present a roadmap to achieve reliable J-FIL based manufacturing solutions.

In recent years J-FIL has seen significant progress in mask infrastructure, materials, pattern transfer, defect reduction, overlay, and throughput. The speaker will discuss the application of the basic J-FIL technology to stepper and full substrate tool platforms that have led to processes for ultra high density data storage including (i) solid state memory at sub-25nm half-pitch nodes and (ii) bit patterned media for terabit density hard disk drives. In addition, extensions of J-FIL to large format patterning including roll-to-roll printing will be discussed in the context of emerging applications in displays, nano-medicine and advanced energy devices.

8323-04, Session 2

Design considerations for UV-NIL resists

K. Usuki, T. Oomatsu, A. Hattori, S. Wakamatsu, K. Kodama, S. Tarutani, K. Shitabatake, FUJIFILM Corp. (Japan)

– Defectivity remains a key issue in UV-NIL. A major challenge is to prevent sticking of resist chemicals onto the mold surface during separation of the mold from the resist. In this study, we investigate the effects on the release property of fluorinated anti-sticking additives in the resist.

- Acrylate resin was used as UV-NIL resist. A fluorinated non-reactive anti-sticking agent or a fluorinated reactive anti-sticking agent (fluorinated monomer) was added to the resin to improve release property. The reactive anti-sticking additive had an acrylate group that reacts with the acrylate resin upon UV radiation.

- Cured resist films were obtained by UV-imprint using a quartz mold without surface coating. The migration of anti-sticking agent was then characterized by XPS. The results indicate that both the non-reactive and reactive anti-sticking agents are localized in the surface region of the cured films. The change to the contact angle between water and resist film caused by solvent rinse and the TOF-SIMS measurement of the mold surface after imprint show that non-reactive anti-sticking agent easily removes from the cured film surface and transfers onto the mold surface. In contrast, reactive anti-sticking agent is fixed in the surface region of cured film and does not transfer onto the mold surface.

- To understand separation force, a model compound was synthesized by changing the acrylate group of the reactive anti-sticking agent to non-reactive end group. This was done because separation force is strongly dependent on the structure of the anti-sticking agent. Addition of reactive anti-sticking agent can reduce by only 10% the force required to separate from the resist compared to without anti-sticking agent. Addition of non-reactive anti-sticking agent, however, can reduce the separation force by 50%. This is as low as provided by the combination of reactive anti-sticking agent in the resist and release agent on the mold (Optool from Daikin). These results indicate that either transfer of anti-sticking agent onto the mold surface or release agent coating on the mold surface is needed to achieve low separation force.

- It is found that addition of non-reactive anti-sticking agent can drastically reduce separation force, but cannot prevent the transfer of anti-sticking agent onto the mold surface. In contrast, addition of reactive anti-sticking agent can prevent transfer of the resist chemicals onto the mold, but only slightly reduces separation force. In this paper, we discuss release interface design, including an analysis of mold surface and resist surface after 1000 imprints.

8323-05, Session 2

New method for selective transfer of nanostructured assemblies onto an arbitrary substrate by nanoimprinting

S. J. Barcelo, M. Hu, A. Kim, W. Wu, Z. Li, Hewlett-Packard Labs. (United States)

Nanoimprint lithography is conventionally used to transfer a pattern from a mold to a deformable and curable resist layer. Here we report a new method of using nanoimprinting to selectively transfer components of a pre-assembled nanostructure to a new substrate, while retaining the advantages of nanoimprint lithography such as low cost and high throughput. In particular, we have developed a process using a purpose-built nanoimprinting tool to create metal nanoparticle assemblies of controlled symmetry and spacing on an arbitrary substrate as a demonstration. The geometry of the particles was defined by evaporating a thin metal film onto the mold, a flexible polymer pillar array with appropriately designed spacing. Upon exposure to liquid and subsequent drying, microcapillary forces pull the pillars and their metal caps together into the designed structure. Assemblies with a variety of symmetries have been demonstrated, from dimers up to heptamers, and there is great potential for a variety of new designs. For the case of gold particles, the new substrate was coated with a monolayer of thiol terminated molecules prior to the transfer process to generate a strong binding force. Successful transfer was then achieved using a normal nanoimprinting process with no resist layer but under appropriate pressure to ensure even and complete transfer of all the nanostructures. This technique can readily be expanded to new material systems and can be used with many substrates not compatible with conventional nanofabrication methods.

8323-06, Session 2

Single-digit nanofabrication by step-and-repeat nanoimprint lithography

C. Peroz, Abeam Technologies (United States); S. D. Dhuey, M. Cornet, Lawrence Berkeley National Lab. (United States); M. Vogler, micro resist technology GmbH (Germany); D. L. Olynick, S. Cabrini, Lawrence Berkeley National Lab. (United States)

UV Nanoimprint Lithography (UV-NIL) technology is a very attractive technology to reproduce micro/nano-patterns over large area at low cost. The Step&Repeat approach for UV-NIL allows reaching high throughput and is currently in industrial preproduction phase for various applications such as hard disks. Last year, we have reported an attractive method combining the advantages of Step&Repeat technology and the imprinting of spin-coated films. Our process SR-NIL allows imprinting and the pattern transfer of the smallest features reported in the literature and is suitable to fabricate nanophotonic devices. We extend here the potential of this method to replicate sub-10 nanostructures into functional materials.

A novel strategy for fabricating nanoimprint templates with sub-10 nm patterns is demonstrated by combining electron beam lithography and atomic layer deposition. Nanostructures are replicated by step-and-repeat nanoimprint lithography on pre-spin coated resist films. Imprints are performed with Molecular Imprint MII 55 Imprint press. Patterns are then transfered into silicon by plasma etching at cryogenic temperatures. Imprinting and pattern transfer into silicon of gratings with sub-10 nm minimum linewidth is demontrated. The trench in the quartz mold is measured around 7 nm by top-view scanning electron microscopy, the final linewidth after transferring is also around 7 nm confirming the very high pattern fidelity of our process. The process is also suitable to fabricate high aspect ratio nanostructures. Sub-10 nm and sub-20 nm structures with aspect ratio as high as 5 and 10 respectively.

We believe than these results shows the unique potential of step-and-repeat nanoimprint lithography for fabricating nanodevices with sub-10 nm features.

8323-07, Session 2

A cost-effective nanoimprint machine

W. Wu, R. G. Walmsley, W. Li, X. Li, R. S. Williams, Hewlett-Packard Labs. (United States)

In order to extend sub-100 nm overlay capability to nanoimprint machines that are affordable to most universities and research labs (i.e. much cheaper than $1M). We invented a nanoimprint process based on wafer bowing. To demonstrate the potential of the wafer bowing NIL process, we built a stand-alone UV nanoimprint machine with four major improvements (over the nanoimprint module that we reported before) implemented. First, we used a cascaded mechanical design that allowed transfer of mask-to-wafer position control from an external positioning system within the imprint module to one internal to mask and wafer. Second, we built the machine on a platform more stable than a typical contact mask aligner. Third, fully automated pressure control was implemented allowing vacuum/pressure and pneumatic sequences to be entirely computer controlled. That gave us the precise control of both the wafer bowing and the load applied by the mold. Forth, an x-y closed-loop piezo stage was added in order to do nano-alignment. With this NIL machine, we achieved 60 nm single point overlay accuracy by using moiré patterns as alignment markers. With design changes that would include x-y and rotational direct nano-alignment of the mold together with temperature control to within 0.1 °C, ~10 nm alignment over a 25 mm field should be possible.

8323-08, Session 2

Nanoimprint and post nanoimprint process for 30nm full field CMOS process using replica quartz template

B. Lee, D. Lee, W. Ko, J. K. Kim, K. Yang, Samsung Advanced Institute of Technology (Korea, Republic of); B. Kim, C. Park, J. Yeo, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

Replica nanoimprint template is one of solution to apply CMOS process because of easy fabrication of high resolution, large area and low cost. However actual replica template for CMOS has not been fabricated due to the limitation of master template fabrication.

Commonly E-beam lithography is applied to fabricate master template because it has good performance to fabricate high resolution pattern and good pattern design flexibility. However E-beam lithography has critical limitation of long writing time for large area of CMOS pattern.

To overcome this issue, we had suggested replica template from Si master template, which is fabricated by optical lithography. 20nm polymer replica template and 30nm quartz replica template was also announced last year.

In this study, 30nm replica template for full field CMOS pattern is successfully fabricated using blank quartz template. Full field replica template is verified in terms of pattern quality and multi-shot durability after nanoimprint patterning on 300mm wafer. And then post nanoimprint process of hardmask etching for CMOS process was successfully performed

The Si master template was fabricated by using the ArF immersion lithography and the master template pattern was replicated to blank quartz template in a conventional UV-NIL tool. By using the replicated resist pattern, replicated blank template was dry-etched to make the working template. The replica template quality was verified with imprinted pattern in terms of line quality and durability. Finally we applied nanoimprint patterning process on 300mm wafer having etching hardmask and then performed post nanoimprint process of hardmask etching.

Full field master template fabricated by ArF immersion lithography. Pattern depth & Bar CD of master template shows 56.7nm(3σ=2.6nm) and 51.3nm respectively.

Replicated quartz template has high pattern depth of 60nm and good pattern profile. Critical dimension(CD), CD uniformity & Line width

roughness also show acceptable results of 28.7nm, 1.43nm and 2.2nm respectively.

Defectivity of replica template was inspected using both direct SEM inspection of template pattern and indirect optical inspection of imprinted wafer with this template. The residual layer thickness (RLT) showed most critical effect to defectivity. As increasing the RLT, defectivity decreased drastically.

NIL patterning using replica quartz template is performed on 300mm Si wafer having hardmask. Residual layer of nanoimprint pattern was opened by O2 plasma etching and then 1st hardmask and 2nd hardmask is successfully opened.

In conclusion we could fabricated actual CMOS replica mask having full field area of 1.5cm X 1.5cm and then verified NIL process and post NIL process using 300nm Si wafer.

8323-09, Session 3

Etch resistant block copolymers: high χ and orientation control

C. J. Ellison, C. G. Willson, C. M. Bates, C. H. Chen, J. D. Cushen, W. J. Durand, L. J. Santos, T. Seshimo, The Univ. of Texas at Austin (United States)

Block copolymers self-assemble on the order of ca. 5-100 nm, making them potentially ideal candidates for a variety of next-generation lithographic applications, including bit-patterned media, field effect transistors and interlayer connects. The efficacy of these applications relies on block copolymer materials with feature dimensions smaller than those currently achievable with optical lithography, etch resistant domains to facilitate pattern transfer, and thin film orientation control. The aim of the present research is to produce materials that conform to all three of the aforementioned properties through a combination of materials design, synthesis, thin film processing and imaging. Since domain periodicity of microphase separation scales as D ~ aN2/3χ1/6 (where N is the degree of polymerization and χ is a block-block interaction parameter) in the strong-segregation limit, larger χ and smaller N values lead to smaller periodicities and features. Thus, high χ materials are pursued herein to minimize pitch and feature dimensions. Thin film orientation control is achieved through a combination of thermal and solvent annealing techniques, coupled with surface energy control of the thin film interfaces. Finally, etch resistant materials are developed through the selective incorporation of heteroatoms, such as silicon, into one domain of the block copolymer, which has previously been shown to create etch resistant domains upon reactive ion etching.

8323-10, Session 3

Pattern scaling with directed self-assembly through lithography and etch process integration

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Directed self-assembly (DSA) has the potential to extend scaling for both line/space and hole patterns. DSA has shown the capability for pitch reduction (multiplication), hole shrinks, CD self-healing as well as a pathway towards LWR and pattern collapse improvement1-4. The current challenges for industry adoption are materials maturity, practical process integration, hardware capability, defect reduction and design integration. TEL has created close collaborations with customers, consortia and material suppliers to address these challenges with the long term goal of robust manufacturability.

This paper provides a wide range of DSA demonstrations to accommodate different device applications. Directed line/space patterns at 14 nm HP are demonstrated with PS-PMMA using both chemi and grapho-epitaxy process flows. To have higher resolution than a PS-PMMA system, a high chi material process is also explored. In addition, directed self-assembly processes have been applied to holes for both CD shrink and variation reduction.

In this paper, TEL's process solutions for both line/space and hole DSA process integrations are presented.

1 Herr, Dan, "Directed block copolymer self-assembly for nanoelectronics fabrication" J. Mater. Res., Vol. 26, No. 2, Jan 28, 2011.

2 Ross, Caroline, et. al., "Templated self-assembly of Si-containing block copolymers for nanoscale device fabrication" Proceedings of SPIE, Vol. 7637, 2011.

3 Liu, C. C. et al. "Integration of block copolymer directed assembly with 193 immersion lithography" JVSTB, Vol. 28, 2010.

4 Cheng, Joy, et. al. " Directed Self-Assembly for Lithography Applications" Proceedings of SPIE, Vol. 7972, 2011.

8323-11, Session 3

Solvent annealing strategies for the directed self-assembly of poly(styrene-b-dimethylsiloxane)

K. W. Gotrik, J. G. Son, A. Hannon, C. A. Ross, Massachusetts Institute of Technology (United States)

Block copolymers (BCP) are capable of generating patterns with periods ranging from 10 - 100nm and are thus becoming an increasingly important method for nanofabrication. Here we report on the wide range of control that can be exhibited over a cylindrical phase poly(styrene-b-dimethylsiloxane) (PS-PDMS), which exhibits a large Flory-Huggins interaction parameter (~0.26) and shows good etch selectivity for pattern transfer to Si. This is done by using a custom built solvent annealing system in which multiple solvent vapor sources are controlled via mass flow controllers (0-10 sccm) to flow into an annealing chamber (quartz, 80 cm^3). Thin films (30-70 nm) of PS-PDMS together with films of each homopolymer are analyzed in situ using spectral reflectometry (250 - 1500 nm) to observe their swelling behavior. We map the phase behavior of the BCP by selectively etching the PS with an oxygen plasma (50 W) to reveal the PDMS morphology. By changing the flow rates and ratios of the different solvents (toluene, heptane) we are able to explore the range of achievble morphologies of a single BCP. This includes the vertical cylinder morphology which is valuable due to its higher aspect ratio for pattern transfer, but is very difficult to achieve in PS-PDMS due to the different surface energies of the blocks. We also show that thicker films (> 100nm) can form vertical cylinders by properly tuning the deswelling rate. Self-consistent field theory modeling of solvent incorporation is compared with these experimental results.

8323-12, Session 3

All-track directed self-assembly of block copolymers: process flow and origin of defects

P. A. Rincon Delgadillo, Univ. of Wisconsin-Madison (United States) and IMEC (Belgium); R. Gronheid, IMEC (Belgium); C. J. Thode, Univ. of Wisconsin-Madison (United States); M. H. Somervell, K. Nafus, Tokyo Electron America, Inc. (United States); P. F. Nealey, Univ. of Wisconsin-Madison (United States)

Directed Self-Assembly (DSA) of block copolymers is considered to be a potential lithographic solution to achieve higher feature densities than can be obtained by current lithographic techniques. However, it is still not well-established how amenable DSA of block copolymers is to an industrial fabrication environment in terms of defectivity and processing

conditions. Beyond production-related challenges, precise manipulation of the geometrical and chemical properties over the substrate is essential to achieve high pattern fidelity upon the self-assembly process. Using our chemo-epitaxy DSA approach offers control over the surface properties of the slightly preferential brush material as well as those of the guiding structures. This allows for a detailed assessment of the critical material parameters for defect reduction. The precise control of environment afforded by industrial equipment allows for the selective analysis of material and process related boundary conditions and assessment of their effect on defect generation.

In this study, the first implementation of our previously reported DSA process for multiplication of feature density on an industrial fabrication track is described. Each process step in the fabrication of chemical nanopatterns is demonstrated with standard production tools. Critical inspection of the samples at each step of the process allows for the differentiation of defects originating from external sources, from those originating due to the block copolymer assembly process itself. Finally, this control of the substrate fabrication and inspection provides us with detailed experimental analysis into the origin of defects that occur during DSA of block copolymers under conditions relevant to the semiconductor industry.

8323-13, Session 3

Synthesis and characterization of self-assembling block copolymers containing fluorine groups

N. H. You, Cornell Univ. (United States); R. Maeda, Tokyo Institute of Technology (Japan); M. A. Chavis, C. K. Ober, Cornell Univ. (United States)

In this work, we report the synthesis and characterization of new block copolymers containing a functional hydroxylated polar segment such as PHOST (4-hydroxystyrene) and a non-polar PTFEMA (2,2,2-trifluoroethyl methacrylate) segment. A PTFEMA segment can provide a strong degree of segregation between the constituent blocks and degradability of PTFEMA under either deep-UV or e-beam radiation. A block copolymer, PHOST-b-PTFEMA, with a total molecular weight of 1600~50000 g/mol and PTFEMA weight ratio of 31~50%, was designed and prepared by living anionic polymerization and subsequent hydrolytic deprotection as shown in Figure 1. Living anionic polymerization of the fluorinated methacrylate monomers and styrene monomer are well documented. To obtain a monodisperse PHOST, tert-butyl ether protected monomer was used to avoid the termination of the living chain end. The structures of PtBuOS-PTFEMA and PHOST-b-PTFEMA were characterized by FT-IR and NMR spectroscopy. The thermal properties of the PtBuOS-PTFEMA and PHOST-b-PTFEMA were evaluated by TGA, DSC measurements. No significant weight loss was found for any of the polymer systems below 300 °C. Annealing in a nonselective solvent (THF) results in parallel orientation of cylindrical domains, while a mixed solvent (THF and dipropylene glycol methyl ether) leads to formation of a trapped spherical morphology. These thin films can be subjected to conventional lithography using e-beam and deep-UV radiation to generate integrated patterns. The formation of controlled microstructures, solvent annealing and patterning of poly(styrene)-b-poly(2,2,2-trifluoroethyl methacrylate) and poly(hydroxyl-ethyl methacrylate)-b-poly(methyl methacrylate) will also be discussed.

8323-14, Session 4

Sub-20nm hybrid lithography using optical and pitch-division, and e-beam

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A roadmap extending far beyond the current 22nm CMOS node has been presented several times. [1] This roadmap includes the use of a highly regular layout style which can be decomposed into "lines and cuts."[2] The "lines" can be done with existing optical immersion lithography and pitch division with self-aligned spacers.[3] The "cuts" can be done with either multiple exposures using immersion lithography, or a hybrid solution using either EUV or direct-write e-beam.[4] The choice for "cuts" will be driven by the availability of cost-effective, manufacturing-ready equipment and infrastructure.

Optical lithography improvements have enabled scaling far beyond what was expected; for example, soft x-rays (aka EUV) were in the semiconductor roadmap as early as 1994 since optical resolution was not expected for sub-100nm features. However, steady improvements and innovations such as Excimer laser sources and immersion photolithography have allowed some manufacturers to build 22nm CMOS SOCs with single-exposure optical lithography.

With the transition from random complex 2D shapes to regular 1D patterns at 28nm, the "lines and cuts" approach can extend CMOS logic to at least the 7nm node. As shown in Fig. 1a, spacer double patterning for lines and optical cuts patterning is expected to be used down to the 14nm node. In this study, we extend the scaling to 18nm half-pitch which is approximately the 10-11nm node using spacer pitch division and complementary e-beam lithography (CEBL).

For practical reasons, E-Beam lithography is used as well to expose the "mandrel" patterns that support the spacers. However, in a production mode, it might be cost effective to replace this step by a standard 193nm exposure and applying the spacer technique twice to divide the pitch by 4. Extreme off-axis dipole illumination with a single spacer deposition step is also worth considering provided all lines are oriented in the same direction.

The Metal-1 "cut" pattern is designed for a reasonably complex logic function with ~100k gates of combinatorial logic and flip-flops. Since the final conductor is defined by a Damascene process, the "cut" patterns become islands of resist blocking hard-mask trenches. The shapes are often small and positioned on a dense grid making this layer to be the most critical one. This is why direct-write e-beam patterning, possibly using massively parallel beams, is well suited for this task. In this study, we show that, using a conventional shaped beam system, specifications for CD uniformity and overlay errors can be met on generic test structures as well as real IC design.

The combination of design style, optical lithography plus pitch-division, and e-beam lithography appears to provide a scaling path far into the future.

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3. H. Yaegashi, "The self-aligned Spacer DP process towards 11nm node and beyond," Lithography Workshop 2010.

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8323-15, Session 4

50 keV electron multibeam mask writer for the 11nm HP node: 1st results of the proof of concept tool (eMET POC)

C. Klein, H. Loeschner, E. Platzgummer, IMS Nanofabrication AG (Austria)

A proof-of-concept electron Mask Exposure Tool (eMET POC) has been realized in the first half of 2011. In the first alignment phase, the eMET POC is operated with a stationary aperture plate using multipole deflection for X/Y beam placement. 40nm HP and 30nm HP resolution was achieved within the full 82µm x 82µm exposure field , in agreement with ray tracing simulations [1].

In Q4 2011 the eMET POC will be completed by inserting an Aperture Plate System (APS), which generates 262-thousand programmable beams of 20nm beam size. All APS core components have been tested separately and are available for installation. First exposure results of the fully operational eMET POC system will be presented.

The eMET Beta / HVM throughput potential for 11nm HP and extendibility to the 8nm HP and 6nm HP mask technology nodes will be discussed.

[1] Elmar Platzgummer, Christof Klein, and Hans Loeschner, SPIE Photomask Technology BACUS 2011, Monterey, Sept 19 - 22, 2011, t.b.p. in Proc. SPIE 8166 (2011).

8323-16, Session 4

Reflective electron-beam lithography: progress toward high-throughput production capability

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Maskless electron beam lithography is one potential technology to extend semiconductor manufacturing to the 16nm node and beyond. Electron beam lithography offers significant improvements in resolution and depth of focus versus current 193nm immersion lithography and can enable the printing of 2X and 1Xnm features without the need to resort to multiple patterning techniques. While it has been used for many years for mask writing, electron beam lithography has so far been unsuitable for semiconductor production due to extremely low throughput and thus unacceptable cost of ownership. To enable electron beam lithography technology to meet manufacturers' high volume manufacturing requirements for throughput and resolution, KLA-Tencor is developing a Reflective Electron Beam Lithography system (REBL) targeting high volume production at the 16nm node. REBL uses a novel multi-column wafer writing system combined with an advanced stage architecture to enable the throughput and resolution required for a NGL system. Using a CMOS Digital Pattern Generator chip (DPG) with over one million microlenses, the system is capable of maskless printing of arbitrary patterns with pixel redundancy and pixel-by-pixel grayscaling at the wafer.

In this paper we will review progress in the development of the REBL system towards its goal of 100wph throughput for lithography at the 2X and 1X nm nodes. Our prototype system using a 75keV electron beam column coupled with the DPG chip and multi-wafer stage has been assembled and used for lithography. We will demonstrate our ability to print tsmc test patterns with this integrated system in chemically amplified resist on silicon wafers at 45nm resolution. Additionally, we will present our latest experimental and simulation results showing that the system targets for throughput, resolution, overlay, and production cost of ownership are achievable for a typical foundry fab wafer mix.

8323-17, Session 4

Implications of multiple e-beam maskless lithography on process, design, and CAD tools

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The steeply increasing price and difficulty of the mask technology make the mask-based optical lithography, such as double patterning by using ArF immersion lithography and EUVL, unaffordable when going beyond the 32-nm HP node. Electron beam direct writing provides extremely high resolution without jeopardy from masks, but the low productivity of traditional single beam systems makes it unacceptable for mass manufacturing even after over 3 decades of development. Considering production efficiency, the throughput of lithography tools should be in the order of 10 WPH/m2 as compared to that of an ArF scanner. To achieve such a throughput per EB column requires an improvement of more than 3 orders of magnitude. The maturing MEMS technology and electronic control technology enable precise control of more than ten thousands or even millions of electron beamlets, writing in parallel. Without the mask constraint, the exposure can be made by continuously scanning across the entire wafer diameter as long as the ultra-high speed data rate can be supported. Hence a much slower scan speed is required and therefore a small tool footprint is achievable.

The MAPPER Pre-Alpha Tool, composed of a 110-beam 5-keV column and a 300-mm wafer stage within a vacuum chamber of 1.3x1.3m2 footprint, has been installed and operational for process development in the advanced cleanroom environment. By sending the pre-treated optical data to the corresponding photodiode of each blanker, each beam writes its own features independently in raster scan mode. Resolution beyond 30-nm HP resolution for both C/H and L/S by using chemical amplified resist has been demonstrated. Applying proper EPC, a 20-nm node test circuit layout has been successfully patterned. The future upgrade by a new electron-optics column, containing 13,000 beamlets and each beamlet projecting 7x7 sub-beams, will achieve throughput at 10 WPH of 32-nm HP node wafers by a single chamber.

If the productive MEBML2 carries out, it will drastically change the concepts of lithography processing and integration flow from the current double patterning for beyond 32nm HP nodes. First, the cycle time will be largely reduced by saving mask making and reducing double patterning to single patterning for all critical layers. It has the opportunity of quickly modifying the EPC model or even directly correcting vulnerable layout hotspots when found, without the headache of retooling the expensive mask. Owing to its unique processing characteristics such as high resolution, wide selection of resist types, large DOF, stitching and matching among the massive beams in one column and multiple chambers in a cluster which also implies multiple wafer stages, the focus of the lithography process development will shift. The MEBML2 tool specs can be looser because the CD and overlay budget from the mask can all be given to the tool. The data preparation, replacing the mask, may become the bottleneck of cycle time. The current restricted design rules due to the limitation of optical lithography will be removed but some new rules may be added in considerations of the writing approaches. Possible changes on processing, design and CAD tools due to these MEBML2 characteristics will be discussed.

8323-18, Session 5

Influence of thermal load on 450mm Si-wafer IPD during lithographic patterning

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To estimate the effects of heat input on IPD, a respective scenario for electron beam writing has been investigated using FE modeling. A 450 mm Silicon wafer of thickness 925 µm is electrostaically clamped to a LTEM chuck and exposed to a local heat flux of 20 mW. Boundary conditions include conductive heat transfer through an effective layer (which represents the pin-structure) into the chuck and cooling by radiation in a linearized model with an effective cooling rate of 5 W/(m²K).

Temperature gradients in the wafer cause an IPD at the writing position that increases with radial distance from the wafer center and may exceed 7 nm close to the wafer edge. In this simplified scenario, the physical limitation for low IPD is dominated by the inefficient radiation cooling mechanism. IPD may be reduced by more than 90 % to about 0.4 nm by

improving heat transfer off the wafer's backside and maintaining constant chuck temperature, which demonstrates the relevance of cooling provisions for high exposure lithography at the 22 nm node and below.

8323-19, Session 5

Self-consistent field theory of directed self-assembly in laterally confined lamellae-forming diblock copolymers

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Diblock copolymers have recently been the subject of increased interest owing to their potential use as an alternative patterning technique to conventional top-down lithography. However, the prevalence of highly undesirable defective structures remains a major challenge that affects the performance and viability of the technique for future applications. To overcome such a challenge, directed self-assembly (DSA), and graphoepitaxy (or lateral confinement) in particular, offers an inexpensive route with the capability of dramatically reducing defect populations.

In this spirit, we use self-consistent field theory to investigate the DSA of laterally confined diblock copolymers. We consider in this research a two-dimensional model with impenetrable and selective lateral walls, which effectively govern the orientation of the lamellae. Our interest lies in particular in systems with a selectivity that guarantees an assembly of the lamellae parallel to the side walls and thus oriented vertically with respect to the substrate. In this case, we show how the interplay between selective wetting conditions at the walls and the width of the channel can lead to well-ordered, perfect lamellae. Commensurate widths and windows of stability of perfect lamellae are therefore identified in accordance with previous work. We also consider two isolated, experimentally observed defects, namely, dislocations and disclinations. For these two defects, we compute the free energy for various chain lengths, wall conditions and channel widths, As expected, the formation of defects is favored by deviations from commensurate widths and/or smaller chains. Lower selectivity at the walls also leads to a dramatic increase of the free energy of the defects relative to a defect-free system.

In addition to determining the free energies of defective and perfect states, we also investigate the transition path between these two states using the string method. In this method, the two field configurations (local minima of the free energy) are connected by a string of states in configuration space and the minimum energy path (MEP) corresponds to the energetically most probable trajectory between the two states. The various states along the discretized string are relaxed to the MEP in a two step process. First, each configuration in the string of field states is updated using a potential force obtained from the overall Hamiltonian of the system. To avoid clustering of the updated configurations, a second step of reparameterization of the string by interpolation is performed to evenly redistribute the configurations along the path. The trajectories thus obtained not only inform about the two local minima of the free energy but also about the height of the barrier that needs to be crossed for a transition between the two minima. In the case of transitions from defective to well-ordered states, we find that only a few kT of energy is necessary to overcome the barrier and suppress the defect, sharply contrasting with the large gain in free energy (tens of kT) that is necessary for the formation of the defect from the pristine state.

8323-20, Session 5

Models for the power spectra of thermal composition fluctuations and line-edge roughness in an ordered lamellar diblock copolymer melt

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The nanofabrication industry is examining DCP directed self-assembly (DSA) as a pattering methodology for the O(10 nm) nanofabrication node. While DCP DSA may not replace optical lithography in the near future, it has the potential to augment or complement optical nanofabrication techniques in the three- to five-year time frame.

Two of the most important concerns currently preventing DCP DSA implementation in the fab are the defect density across fabrication-scale wafers and the line edge roughness (LER) of the DCP mesophase. Theoretically, DSA allows researchers to control the defect density; however, LER persists even when DCP thin films are fabricated using DSA methods.

The International Technology Roadmap for Semiconductors (ITRS) has set stringent limits on long-wavelength LER. For the CD ~ 10 nm node, where CD is the pattern critical dimension, the ITRS requires 3-sigma LER to be less than approximately 10 % of CD. Much of the research to-date has demonstrated that for CD ~ 20 nm DCPs, the 3-sigma LER is greater then 10 %, and polymer scaling laws suggest that at smaller length-scales, the LER will be an even larger fraction of CD. One way around this scaling catastrophe is to increase the segment-segment interaction parameter "chi"; however, preliminary calculations suggest that exceptionally large values of "chi" are required to meet the ITRS targets. Understanding, controlling, and accurately measuring thermal LER in DCP melts are challenges of critical importance for next-generation DCP DSA applications.

Most models of long-wavelength LER in lamellar DCP melts rely on a capillary wave or fluid membrane theory, and these models can work quite well at high-intermediate to strong segregation strengths. However, at weak-intermediate to intermediate segregation, the capillary wave model is non-ideal because of the periodic nature of DCP mesophases. Accordingly, a more accurate model of LER in DCPs is needed.

The primary source of LER in an ordered DCP mesophase is thermal composition fluctuations. A better understanding of these fluctuations will help advance our understanding of LER and facilitate control/management of LER. Of particular importance is the need for a quantitative framework to describe and measure changes in LER with respect to the physical parameters and processes governing DCP self-assembly.

In this paper, we examine an analytic expression for the power spectrum of equilibrium, thermal composition fluctuations in a lamellar DCP. We then use this expression to examine a phenomenological expression for the thermal LER power spectrum in a lamellar DCP. We compare the expression for the LER power spectrum to data from stochastic simulations of thermal LER in a lamellar DCP, and we demonstrate that the expression approximately fits the simulation data for weakly to moderately segregated DCPs. Finally, we discuss how this expression can be utilized in a scattering-based LER metrology framework.

8323-21, Session 5

Modeling block copolymer directed self-assembly on chemically patterned substrates: effect of mismatch between the morphology and pattern

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Multiple methods have been proposed for directing block copolymer (BCP) self-assembly for advanced lithography applications. For graphoepitaxy of perpendicular cylinders, the directing force applied by posts can be considered to be infinitely strong and able to induce the morphology to stretch or compress to accommodate incommensurate spacing. A chemoepitaxy approach relies upon attractions between BCP molecules and a chemically patterned substrate. Since these attractions are often weaker than the force exerted by rigid posts and only a minority of the film's molecules (those in contact with the substrate) experience the directing force, the BCP morphology is less likely to adjust to any

mismatch with the pattern's spacing. The likelihood of this adjustment is decreased even further by the industry's desire to use sparse patterns that can be generated with current optical lithography techniques. If the industry is going to implement this form of directed self-assembly, the tolerance for incommensurate spacing, as well as the expected mismatch between the diameters of cylinders and optically-generated interacting spots, will need to be determined. To evaluate these forms of mismatch, a model was developed to calculate the area of overlap between large arrays of cylinders and spots. In addition to differences in spacing and feature size, the model allows variation of both the overall system size and the angle of rotation of the morphology relative to the substrate. The angular dependence of cylinder-spot overlap for sparse patterns demonstrates how quickly the morphology's preference for the intended angle (e.g. 30o when directing the vector) disappears as mismatch in pitch and size are introduced. The overlap at fixed angle but varying system size behaves in a sinusoidal manner with a period that depends on the mismatch in pitch. Since the first transition from high to low overlap with increasing system radius is likely to correlate to grain size, these calculations demonstrate that very small degrees of pitch mismatch are enough to cause a morphology to break up into multiple grains. Using block copolymer theory, the energy penalty of stretching or compressing the morphology can be estimated. By coupling these calculations to the model for cylinder-spot overlap, a transition from a perturbed BCP morphology to one with finite grain size can be demonstrated. A comparison between these predictions and results from the literature will be provided.

8323-22, Session 6

Directed self-assembly defectivity assessment

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The main concern for the commercialization of directed self-assembly (DSA) for semiconductor manufacturing continues to be the defectivity. Our research studies the defectivity of DSA in the context of a 300mm wafer fab cleanroom environment; while last year's research1 estimated DSA defectivity of 12nm line and space arrays generated by chemical epitaxy, this paper discusses the missing via density, CD-distribution and registration accuracy (hole-in-hole) for DSA contact rectification by grapho-epitaxy.

The directed self-assembly was conducted using a PS-b-PMMA block copolymer following a typical grapho-epitaxy contact hole rectification process flow. Firstly, a unique "phase-separation" CD-SEM measurement was performed to measure the diameter of the PMMA cylinder domains prior to PMMA removal (figure 1). This technique enables the direct measurement of thousands of phase-separated domains, generation of histograms and image review necessary for yield studies; for example, review of the domains +/- 2 sigma and 3 sigma from the mean. Secondly, following a dry-etch development (removal) of the PMMA cylinders, we measure the phase-separated hole registration relative to the grapho-epitaxy prepattern. The CD measurement computes the center shift between the pre-pattern versus the developed hole and report the displacement as a vector (in nanometers) and direction. This technique enables the measurement of thousands of holes (> 100 holes per minute), generation of histograms, and SEM image review for specific holes of interest; for example, review of the 10 worst (figure 2). Thirdly, we measure defectivity using the bright field inspection, we scanned > 500-million vias evenly distributed across 17 dies, reviewed all defects using a review SEM, classified each defect based on root-cause and identified a total of 22 missing vias (figure 3); thus, the missing via defect density for this study was 1-per-25 million (figure 3).

8323-23, Session 6

Pattern density multiplication by direct self-assembly of block copolymers: toward 300mm CMOS requirements

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Density multiplication of patterned templates by directed self-assembly (DSA) of block copolymers stands out as a promising alternative to overcome the limitation of conventional lithography. Recent works highlighted the capabilities of DSA to be integrated with state-of-the-art 193nm lithography1 and point out the necessity of a 300 mm baseline2.

In this paper we investigate the possibility to reach 300mm CMOS requirements by integrating graphoepitaxy of PS-b-PMMA self assembly. First, the interface between the copolymer thin film and the resist/silicon substrate has to be neutralized in order to avoid a preferential wetting of the substrate by one block and to allow by this way the perpendicular orientation of the structure. This can be done by the chemical derivatization of the silicon wafers with random copolymers containing the same constituents as the block copolymer used3. Then, the PS-b-PMMA is spin coated and annealed in order to generate self assembly, then chemical treatment (dry or wet etching) removes the PMMA block and forms a PS mask. The horizontal and lateral order is controlled by tuning different parameters: molecular weight of the polymeric constituents, correlation between a substrate patterns and the intrinsic copolymer period, interaction with the substrate. Different schemes to integrate DSA process by using 193nm dry lithography or e-Beam lithography will be presented (see figure 1).

Moreover, several challenges like solvent compatibility, bake kinetics and defectivity will be addressed. Concerning defectivity, we will propose a methodology in order to evaluate and optimize the long range order induced by graphoepitaxy of the block copolymer DSA. By implementing a graphoepitaxy methodology with BCP film thickness larger than the trench depth (see figure 2a), the Voronoi analysis may be used to quantify the degree of local order by counting the disclinations. This approach affords the monitoring of the overall block copolymer self-assembly process and enables us to easily optimize the parameters required for a long-range order structuration, leading to zero-defects block copolymers self-assembled networks (figure 2b and c). Transfer capabilities of the PS nanostructures in the bulk silicon substrate by using plasma-etching will be also detailed, both with the film on bare silicon or organized with graphoepitaxy approaches.

These results show the high potential of DSA to be integrated directly into the conventional CMOS lithography process in order to achieve high resolution and pattern density multiplication, at a low cost.

8323-24, Session 6

Measurement of placement error between self-assembled polymer patterns and guiding chemical prepatterns

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Recent demonstrations of directed polymer self-assembly at the 300 mm wafer scale have amplified interest in it as a potential extension to current patterning techniques for sub-15 nm half-pitch features. While the very nature of directed self-assembly implies registration to lithographically defined guiding prepatterns, layout optimization and eventual device fabrication demand a detailed knowledge of the self-assembled pattern placement. In chemical epitaxy with density multiplication, perfect

commensurability between prepattern line widths and pitches and the same respective parameters of the polymer domains they selectively pin is not necessary for successful guidance, a fact that widens the process window but complicates the question of pattern placement. Using specially designed chemical patterns fabricated via electron beam lithography to guide the self-assembly of a 12 nm half-pitch PS-b-PMMA lamellae block copolymer, this study aims to precisely quantify the absolute placement error between underlying prepatterns and the resulting self-assembled patterns as a function of prepattern line width and pitch as well as polymer film thickness for line-space tripling and quadrupling. We will also discuss the formation of more complex self-assembled line-space patterns directed by chemical prepatterns designed for the purpose, with emphasis on the effect of variations in the prepatterns and process conditions.

8323-25, Session 6

Characterization of cross-sectional profile of epitaxially assembled block copolymer domains using transmission small angle x-ray scattering

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Transmission small angle X-ray scattering (tSAXS) was used to characterize the cross section of poly(styrene-b-methyl methacrylate) (PS-PMMA) block copolymer line gratings assembled on chemically-templated substrates with a pitch less than 50 nm. X-ray diffraction data covering a broad Qx and Qz region were collected and analyzed, where the x-axis denotes the in-plane direction perpendicular to the line gratings and z-axis is along the thickness direction. The X-ray data can best be fit with a cross section comprised with footing, waist and top rounding. The simplest model to simulate such a cross section is a stack of four trapezoids, each with discrete side wall angle, height and width. Even with this simple 4-trapezoidal model there exist nine fitting parameters; however, there also exist sufficient X-ray characteristics and quality to ensure a fit with a reasonable confidence. Figure 1 illustrates this point; the 9-parameter model was determined by simultaneously fitting diffraction curves at five discrete Qx values. The best fit cross section of PS-PMMA block copolymer nanopatterns is given in Figure 2. It is noteworthy that the area occupied by each component of the nanopatterns is exact 50%, consistent with the composition of the copolymer used. This observation further highlights the accuracy of the X-ray data and its analysis. The line edge roughness (1s) was also determined by the intensity decay rate along Qx, known as the apparent Debye-Waller factor. The cross section edge profile and the interface roughness value obtained from X-ray data will also be discussed and compared with the results of computer simulation of the self-assembly process.

8323-26, Session 6

Characterization of nanostructures for imprinted dot/hole patterns by x-ray metrology

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We have so far developed x-ray metrology for measuring a cross-sectional profile of surface periodic grating patterns. Nanoimprint lithography is one of the promising candidates for fabricating dozens nanometer scale line patterns and dot/hole patterns. For the master mold, non-destructive characterization and the quality control of nanostructures, such as the pitch, size, height, sidewall angle, corner rounding and these fluctuations are necessary. Because transferred imprinted patterns are affected by the master mold and the device

performances can be strongly correlated with these parameters. We have taken notice of nanoimprint processes of bit-patterned media (BPM). Silicon master mold, nickel father stamper, nickel mother stamper, transparent mold, and BPM etching mask are transcribed in sequence. We have applied x-ray meteorology to these imprinted dot/hole patterns in order to evaluate difference of nanostructures during the transcriptions from the silicon master mold to the BPM etching mask pattern. X-ray diffraction images were collected in grazing incidence geometry, when incidence angle to the sample surface is about the critical angle of total reflection and x-ray wavelength is 0.15418 nm. Several diffraction peaks from the periodicity of the dot/hole array are observed in the lateral direction (2θ-direction) and the dot/hole array can be analyzed as a hexagonal structure with the pitch of 35 nm. On the (10) diffraction peak, we can see a fringe pattern, which indicates depth of the dot/hole. The dot/hole depths can be analyzed from the periodicity of the fringe pattern. The obtained nanostructures were compared with the results of AFM observation.

8323-27, Session 6

Challenges of SEM metrology at sub-10nm linewidth

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Challenges concerning SEM metrology at critical dimensions below 10 nm are discussed. At these dimensions, SEM images are normally noisy and their contrast is low; in addition, the signal formation mechanism is considerably different from that of regular samples. Electron scattering at this size range is strongly affected by the feature size, thickness, and the distance to the neighboring features, as well as beam voltage, beam size and material properties.

Experimental results and simulations are presented for the measurement of lines down to 4 nm. The features were fabricated using direct write EBL and nanoimprint. SEM images of the resulting patterns were taken. Two commercially available software tools were used for the analysis and simulation: a) model based, automatic extraction of CDs from SEM images and b) Monte Carlo simulations to model signal formation in SEM.

CHARIOT Monte Carlo software utilizes advanced physical models with an emphasis on slow secondary electrons; the results were used to understand the image formation at ultra-small feature sizes.

In the analysis of the SEM images, it was shown that commonly used CD extractions based on the brightness threshold method do not yield good results. Alternatively, myCD software utilizing analytical model of SEM produced more accurate data. In real time, the software builds a model of the SEM signal based on the input information regarding the SEM setup and materials; the model is used in the automatic extraction of contours and CD measurements. Results and challenges are discussed.

8323-26, Session 7

Patterned media: disk drive technology at the frointier of lithography

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Recent advances in E-beam directed self assembly of block copolymer films have positioned block copolymer lithography as one of the most promising methods to achieve high resolution, high density patterns with a high degree of in-plane translational order on circular tracks amenable to magnetic bit patterned media technology at densities in excess of 1Tdot/in2.

For block copolymer lithography to move to the next stage and contribute to the advancement of the lithography roadmap, it must overcome several challenges that extend beyond mere pattern formation. Meeting the requirements for a lithographic application such as BPM or semiconductor fabrication, implies that the technology must mature in all of the following fronts: 1) feature density scalability, 2) design rules to achieve non-conventional patterns with the limited set of available geometries, 3) high fidelity pattern transfer and 4) ad hoc metrology for proper defect classification and quantification of pattern quality. Here, we report on recent progress made on all these fronts with a particular focus on bit patterned media applications.

The most common block copolymer patterns used for lithography comprise arrays of periodic dots in a hexagonal lattice or line-space features which restrict lithographic designs to be compatible with this limited set of geometries to define all required features. In BPM applications, the bulk of the lithography is used to define periodic features for the data bits which could be arranged in the form of round dots in a hexagonal lattice or as rectangular bits in a rectangular lattice as we demonstrate in this work. Other non-data, but equally critical, areas used for servo information may require more intricate geometries that differ from the periodicity of the data sectors. Here we discuss advantages and disadvantages of hcp vs line-space geometries for data sector patterns as well as potential designs for servo patterns that are compatible with self assembly.

Pattern fidelity of the transferred features relies on the uniformity of the image that the block copolymer features project at the substrate interface. Three dimensional variations in the direction out of plane can play a detrimental influence in the final quality of the transferred features. These variations may arise from domain tilting or reconstructed features that do not reach the bottom of the film (or that do not cross the totality of the film). We show some examples of the issues that may arise during pattern transfer of both hcp and line-space geometries due to the three dimensional structure of the films.

Lastly, defect classification and quantification of pattern quality becomes also an important metric to gauge the feasibility of block copolymer lithography. We present suggested metrics that may contribute towards establishing standard metrology procedures.

8323-27, Session 7

Evaluation of ordering of block copolymers with pre-patterned guides for bit patterned media

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Bit patterned media (BPM) is a promising candidate for next-generation magnetic recording media beyond 2.5 Tb/in2. To realize such a high-density BPM, directed self-assembling (DSA) technology is a possible solution. Polystyrene-b-polydimethylsiloxane (PS-PDMS) has a possibility of forming fine dot-array pattern with less than 20 nm pitch. And DSA technology is suitable for mass production of devices with nanoscale feature size.

Hosaka et al. have reported long-range-ordering of self-assembled PS-PDMS block copolymer nanodots using guide lines and posts drown by electron beam.[1] Kamata et al. have reported the first successful track-following test in a prototype drive of 2.5 Tb/in2 DSA-BPM using PS-PDMS as pattern template.[2]

In order to read and record magnetic signals on magnetic media, the position of magnetic dots must be controlled with high accuracy. Therefore, it is necessary to evaluate the positioning accuracy of ordered diblock copolymer patterns.

In this study, we optimized the ordering of block copolymers. The issues examined are the treatment of surface of substrate, the shape of graphoepitaxy guide, etc.

Voronoi diagram was applied to evaluate the ordering of directed self-assembly of block copolymers. There was found to be a good relationship between the positioning accuracy and the ratio of 6-fold symmetry of Voronoi diagram. In addition, it is easy to detect the lack of ordering by the Voronoi diagram method.

Applying the optimized conditions, we obtained highly controlled ordering of the dots suitable for magnetic recording media.

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8323-28, Session 7

Integration of nanoimprint lithography into block copolymer directed self-assembly for fabricating nanoimprint templates and bit-patterned media over 1 teradot/in^2

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Directed self-assembly of block copolymers (BCPs) has been proved to be an effective way to generate ultrahigh resolution nanopatterns. The area of the BCP patterns with long-range order is limited by the small area of a guiding pattern, which is typically defined by a slow electron-beam lithography process1-4. Applications like bit-patterned media (BPM), require patterning over a disc-size area. Here, nanoimprint lithography is implemented as a high-throughput and low-cost method to create high-quality guiding patterns over large area. Addressable 1-D or 2-D PS-b-PDMS nanopatterns were demonstrated over several to tens of square centimeters areas using this method. Factors affecting the quality of directed BCP patterns were identified. Extending this method to other BCP systems like PS-b-PMMA was also verified.

As a benchmark of using BCP patterns for high-density nanodevice applications, PS-b-PDMS nanotemplates with a pattern density of over 1 teradot/in2 were successfully transferred into various functional materials, such as carbon, quartz, and magnetic materials (Figure 1). An ultrahigh density quartz template at 1.3 teradot/in2 was fabricated and used for the fabrication of BPM on a 2.5" disc.

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8323-29, Session 7

Line-frequency doubling of directed self-assembly patterns for single-digit bit pattern media lithography

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Directed self assembly is emerging as a promising technology for post-optical lithographic patterning to define sub-20nm features. However, a straightforward path to scale block copolymer lithography to single-digit fabrication remains challenging given the diverse material properties found in the wide spectrum of self-assembling materials. Up to now, a vast amount of block copolymer research for industrial applications has been dedicated to poly(styrene-b-methyl methacrylate) (PS-b-PMMA) block copolymers, a model system that displays multiple properties that make it ideal for lithography, but that is limited by a weak interaction

parameter that prevents it from scaling to single-digit lithography. Other block copolymer materials have been shown to scale down to much smaller dimensions, but at the expense of other material properties that could delay their insertion into industrial lithographic processes. We report on a line doubling process applied to block copolymer patterns to double the frequency of PS-b-PMMA line/space features, demonstrating the potential of this technique to reach single-digit lithography.

We demonstrate a line-doubling process that starts with directed self assembly of lamellae-forming PS-b-PMMA to define line/space features. The trimmed block copolymer pattern is transferred into an underlying sacrificial hard-mask layer followed by a growth of self-aligned spacers which subsequently serve as hard-masks for transferring the 2x frequency doubled pattern to the underlying substrate. We applied this process to patterns defined by two different block copolymer materials to demonstrate line-space patterns with a half pitch of 11nm and 7nm respectively underscoring the potential to reach single-digit critical dimensions. A subsequent patterning step with perpendicular lines can be used to cut the fine line patterns into a 2-D array of islands suitable for bit patterned media. Several key process integration challenges such as line edge roughness, line width control and defect rate are addressed in this paper.

8323-30, Session 7

Imprint process performance for patterned media at densities greater than 1Tb/in^2

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For decades, films with smaller grains were deposited to support higher density recording. Today however, grain sizes have become so small that further shrinkage would cause the grains to be unstable. The most promising route to achieving densities well beyond the apparent limits of this superparamagnetic effect is patterned media (PM). With PM, each bit is stored in a single magnetic switching volume rather than a collection of grains. Since each island is a single domain, patterned media is thermally stable, even at densities far higher than can be achieved with conventional media. The purpose of this paper is to review the process challenges associated with imprinting bit patterned media arrays at densities above 1Tb/in2.

Two-sided imprinting of disk substrates was performed either with a NuTera® HD7000 fully automated UV-nanoimprint lithography tool that has been specifically designed for patterned media applications. The NuTera® HD7000 provide high patterning fidelity with a throughput of >300 disks per hour. 1Tb/in2 bit pattern (27nm pitch) arrays were imprinted and evaluated. The average dot diameter was measured using Simagis software and was 16.6nm with a 1 deviation of 1.1nm.

In order to meet defect targets, it is critical to be able to imprint the bit patterns without causing collapse of the features. This is quite challenging, since the gap between the printed pillars is on the order of 10nm for a density of 1Tb/in2. Improved performance resulting from an imprint resist with an increase in modulus of ~30% relative to the previous resist will be presented. Additional topics, including the pattern transfer of the residual layer of the resist will also be discussed.

8323-31, Session 8

Contact-hole patterning for random logic circuits using block copolymer directed self-assembly

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Block copolymer directed self-assembly (DSA) is a promising extension of optical lithography for device fabrication. The irregular distribution of contact holes in circuit layouts is one of the biggest challenges for DSA

patterning because the self-assembly tends to form regular patterns naturally. In this paper, we show the use of gridded design rules (GDR), while it is not essential for the DSA process, does provide an excellent starting point for DSA patterning optimization by minimizing layout modification, simplifying guiding template design and improving DSA yield. The benefits are maximized when the contact pitch/size matches the geometries of the naturally self-assembled block copolymers.

We designed GDR-compatible standard logic cells based on the layouts from an open cell library, shrinking the cell layouts down to 22 nm node. Overall, we re-designed a total of 85 logic cells layouts (including inverters, buffers, NAND, NOR, AOI, OAI, adders, and flip-flops) from the above cell library into DSA-aware layouts. No area penalty is observed for any of these cells and the full-chip VLSI (physical) design flow is largely unchanged.

The topographical guiding templates for contact holes were patterned on silicon using e-beam lithography and etched to a depth of ~50nm. We use 70:30 PS-b-PMMA diblock copolymer dissolved in PGMEA for self-assembly. The contact holes were achieved with a CD of 15nm and registration accuracy of 1nm using guiding templates with a CD of 51nm. The results show high tolerance for template defects and ensure a large process window for DSA.

8323-32, Session 8

A computationally efficient model for DSA graphoepitaxy

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Combining block copolymer directed self-assembly (DSA) with 193 immersion lithography provides a low-cost and high-throughput route to generate patterns below the optical resolution limit. DSA of block copolymers using graphoepitaxy method has shown great potential in pattern rectification, e.g. improving critical-dimension uniformity and forming sub-resolution features. However, in order to take full advantage of this technique, the guiding prepattern for DSA has to be carefully designed. Thus, a numerical model that can accurately simulate the DSA behavior in free-form guiding patterns is required. Existing Monte Carlo or Self-Consistent Field Theory models are precise enough but too computationally expensive to be incorporated into the design of large-area guiding prepatterns. In this work, a fast model is proposed and investigated. The average difference between the predicted positions by a Monte Carlo method and by the proposed model is less than 2 nm. The computation time over an area of ~10,000 nm2 required for the simplified model is 4 - 5 orders of magnitude faster than the Monte Carlo model. Examples using the new model in prediction of the DSA morphology in simple and complex guiding prepatterns will be presented and discussed.

8323-33, Session 8

Contact-hole shrink process using directed self-assembly (DSA)

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The application of directed self-assembly lithography (DSAL) to semiconductor device manufacturing is just starting. DSAL potentially has several technical and economical advantages when compared to conventional lithography extensions or other alternative technologies. It enables nanofabrication of line and space features below 20 nm HP using conventional lithography tools at a lower cost of ownership (CoO).

We demonstrated the wet development process using polystyrene-block-poly(methyl methacrylate) (PS-b-PMMA), in combination with UV

exposure which breaks the bonding in PMMA part to promote dissolution in developer solvent. The wet development process provides higher development selectivity between PS and PMMA parts. It promises higher remaining PS film thickness as well as improved critical dimensions (CDs) measurement and defect inspection before dry etching of under-layer films.

Contact hole shrink process using the DSA is one of the most promising applications to the semiconductor device manufacturing. It is expected to provide superior CD uniformity (CDU) for contact holes smaller than 30 nm in diameter. In this work, we investigated some key knobs to control CDs and CD uniformity (CDU) in the contact hole shrink process using DSA, and compared the wet development process using different kinds of solvents after UV treatment with the dry development process using oxygen plasma dry etching. The contact hole shrink behavior dependence on contact hole pitches and layout of guide patterns was also investigated.

8323-34, Session 8

Material and process development for block copolymer lithography

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Due to both economic constraints and technical hurdles, conventional "top-down" photolithography is facing significant challenges to continue the march of Moore's Law for advanced IC fabrications. Different paradigms for developing feasible technology to continue the advance of semiconductor technology are being widely discussed. Directed self-assembly (DSA) of block co-polymer (BCP) is one of the candidates under consideration. Fundamental characteristics of block co-polymer self-assembly have been extensively investigated in academia and research institutes in past several decades, and directed block copolymer self-assembly has been attracting increasing industrial interest for potential semiconductor applications in recent years. Recent progress has demonstrated promising versatility of this technology for potential applications in semiconductor industry, although some questions remain as to whether DSA-based patterning processes and materials can meet the rigorous performance requirements of semiconductor fabrication. This communication will report our recent progress in developing DSA materials and processes which will facilitate the adoption of DSA-based patterning techniques by the semiconductor industry.

8323-35, Session 8

Directed self-assembly patterning using PHOST-b-PS block copolymers

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Directed Self-Assembly (DSA) patterning using block copolymers is a promising patterning method that could enable continued fabrication of dense features below 20 nm pitch from relaxed pitch lithographic patterns derived from optical exposure tools. Recent work has shown that simple polymers such as PS-b-PMMA can be used to achieve pitches on the order of 20 nm. However, the relatively low χ value of PS-b-PMMA prevents the extension of its use far into the desired sub-20 nm pitch domain. Therefore, one focus of our work has been on the development and exploration of block copolymer systems, underlayers, self-assembly annealing processes, and block removal processes that can be combined to achieve sub-20nm pitch patterning via DSA. In particular, we have been focusing on block copolymers in which one or both blocks of the copolymer exhibit a strong specific interaction with themselves that is relatively orthogonal to the interactions with the opposite block. In this work, poly(styrene)-b-poly(hydroxystyrene)

or PS-b-PHOST polymers have been synthesized and characterized for use as such a high χ polymer for DSA patterning. In this case, the strong and extensive hydrogen bonding between the phenol sites in the PHOST block result in a χ that may be an order of magnitude or more larger than that in PS-b-PMMA. This paper discusses the synthesis of PHOST-b-PS via nitroxide mediated radical polymerization, resulting in polymers with tailored molecular weights and low polydispersity indices (PDIs). These materials have been characterized by GPC, NMR, and FT-IR analysis. Appropriate neutral underlayers for such materials have also been developed and will be discussed. DSA using PS-b-PHOST and the neutral underlayers developed in this work will be demonstrated, including DSA using a directly photodefinable guiding layer. Novel methods for selective block removal will also be presented and discussed which can produce high aspect ratio DSA structures.

8323-36, Session 9

REBL: design progress toward 16nm half-pitch electron-beam lithography

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REBL is a novel concept for high speed maskless projection electron beam lithography. Originally targeting 45 nm HP (half pitch) under a DARPA funded contract, we are now working on optimizing the optics and architecture for the commercial silicon fabrication market at the equivalent of 16 nm HP. The shift to smaller features requires innovation in most major subsystems of the tool, including optics, stage, and metrology. We also require better simulation and understanding of the exposure process, including limits on resist sensitivity that directly affects throughput per column.

In order to achieve the required blur for 16 nm features, we are working on increasing the beam energy in the column from 50 KeV to as high as 100 KeV. Combined with improved lens design, simulations show that we can meet the blur requirements at high beam currents. High-volume manufacturing will require a tool with multiple columns in order to achieve the necessary throughput. This in turn requires that the column is engineered to be small enough such that several can be placed within the footprint of a single wafer. We will describe some of the novel design aspects we have developed to achieve this goal.

16 nm HP will require a pixel pitch of not more than 6.4 nm, which is difficult to achieve conventionally due to limitations on the optical demagnification combined with the minimum pixel pitch readily achievable at the DPG. To overcome this, we have developed a novel concept for interleaving pixels at the wafer. We have also developed novel concepts for stage metrology in order to achieve sub-nm position data at the wafer in 6 axes.

Throughput is ultimately determined by a combination of resist sensitivity and beam current. The minimum usable resist sensitivity in turn is set theoretically by shot-noise induced line-edge roughness (LER) and CD non-uniformity. We are working on developing a more accurate model based on theoretical and experimental data to predict the minimum resist dose that can meet a given LER target.

8323-37, Session 9

Active-matrix nc-Si electron emitter array for massively parallel direct-write electron-beam system

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We are currently working on the development of massively parallel direct write electron beam system providing a practical throughput comparable to an existing optical stepper. Electron source used in this

system is nanocrystalline Si (nc-Si) ballistic surface electron emitter where 1:1 projection of electron beam has been demonstrated to resolve patterns of 30nm in width in our previous work. A structure of arrayed dot patterns of the nc-Si emitter with an area of 1µm2, arranged in a 1000x1000 pixels, is integrated with an active-matrix driving LSI. The 1million beamlets exposing pixels simultaneously switch on and off by changing CMOS-compatible voltage. Imaging optics projects a reduced image (1/100) of focused electron beams emitting from the device onto the wafer, synchronizing with controlled motion of the stage. This paper presents our designed and prototyped structure of nc-Si electron emitter array compatible with the active-matrix LSI, and describes the validation result of its performance as an electron source for massively parallel direct writing. Emitting part of electron of the device consists of arrayed dots of nc-Si emitter fabricated on SOI or Si substrate, and TSV plugs connected to the dots from the back side. Forming an aligned joint of the TSV plugs with driving pads on the active-matrix LSI constitutes the device structure. Electron emission from a test structure of arrayed dot patterns of nc-Si emitter worked in practice, showing the possibility that the beamlets switch on and off by changing CMOS-compatible voltage. We are currently working on the integration process with the LSI.

8323-38, Session 9

Complementary patterning demonstration with e-beam direct writer and spacer DP process of 11nm node

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Self-Aligned Double Patterning(SADP) would be most promising technology for fine pattern fabrication below 40nm hp, therefore, it has been employed in HVM of memory device. Furthermore, it has wide extendibility to self-aligned multiple patterning(SATP, SAQP), and its resolution achieved to 11nm hp.

Complementary E-beam Direct Writing (EBDW) combined with SADP is most likely potential option for logic device manufacturing. ArF immersion prints line and space with a specified pitch, SADP technology makes the pitch finer, and E-beam cuts the lines.

This paper shows demonstration results of complementary patterning with Spacer DP process and currently used EBDW tool. Metal 1 of SRAM in 11 nm node is used as the targets for this demonstration. Spacer DP process and etching after EB exposure are performed by Tokyo Electron and E-beam exposure is performed by Advantest.

This paper also reports EBDW applicability to complementary patterning. Complementary patterning requires not only resolution, but also overlay for EBDW. Compared to printing device pattern itself, printing cut pattern makes the shot irradiation area smaller because EB tool needs to expose only cut patterns. In the light of resolution, the small irradiation area relaxes the coulomb interaction, therefore the resolution limit on hole pattern can be improved. Overlay requirement is less than the half pitch of double-patterned space. Overlay prospect and improving plan will be also mentioned.

8323-39, Session 9

CP element-based design for 14nm node EBDW high-volume manufacturing

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We have established CP (character projection) based EBDW technology for current device production. And recently we confirmed the resolution of 14nm L&S which meets 10nm logic requirement with CP exposure.

From these outputs multi-beam EBDW combined with CP function, MCC [1] is one of the most promising technologies for future high volume manufacturing if exposure throughput was drastically enhanced.

Our designed parameters to attain 100 WPH for 14nm result in 150 beams, 10cluster, 100 Giga shots/wafer, 250A/cm^2 and 75uC/cm^2.

In addition to multi-beam, drastic exposure shot reduction is indispensable to attain 100 WPH for 14nm node. We have aggressively targeted 100 Giga shot count which is equivalent to covering 300mm wafer with 0.8um square fairly large tile. All device circuit blocks should be structured with only CP defined parts and we should trace back to upstream design flow to RTL. We call this methodology "CP element based design". The primal design factors are Logic cell, Memory macro and random interconnect.

Concerning logic cell, we need cell clustering approach. Our estimation value of logic cell height is around 0.4 um at 14nm node and we should consolidate multiple cells to expose with CP of more than 0.8um square area in average. Especially for frequently used small cells of NAND, INVERTER, BUFFER, we need special attention. We report how to consolidate multiple cells in the stage of physical synthesis and P&R (position & rout) stage in design.

The memory macro is simple to construct with CP elements because of fixed layout. However the shortage of CP elements is critical, because it consists of numerous kinds of line-up, such as 1 port, 2port SRAM, Resister file, ROM, and each of them contains several peripheral circuits such as word decoder, sense amp, IO, and etc. We should save CP consumption with communization of circuits without device area penalty.

Random interconnect is most critical because of its lack of regularity. We propose the concepts of ultra regular layout with only using fixed size CP elements. These elements basically consist of the same pitch Line and Space tracks and fixed position cutting points. For example to 14nm node, each CP contains 20nm width and 80nm pitch 12 tracks. And each track has potentially one fixed position cutting point to electrically separate from other track, and we should prepare 4096 kinds of CP elements to cover all combinations of 12 points on/off equal to 2^12.

We have get some prospects for constructing all device circuit blocks with only CP defined elements and will report these technical outputs.

[1] A.Yamada et al., J. Vac. Sci. Technol. B Vol. 26, pp. 2025-2031 (2008)

8323-40, Session 9

Status on resist development for 5kV mapper multibeam application: correlation using different accelerating beam voltage

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To secure on-time the maturity of the MAPPER technology, multi-beam needs to rely on a robust process infrastructure. A clear and complete status of this point will be developed on this paper.

To secure on-time the maturity of the MAPPER technology, multi-beam needs to rely on a robust process infrastructure. A clear and complete status of this point will be developed on this paper.

Today, four resist/material vendors (TOK, JSR, DOW-EM and Nissan-Chem) joined the IMAGINE consortium and also a track supplier (DNS-Sokudo). They are working in close collaboration with CEA-LETI to give best resist processes platform to MAPPER application, following precise deadlines, focused on 22nm half-pitch and below.

All resist and material were evaluated at CEA-LETI using same protocol. They are firstly checked using a VISTEC SB 3054DW tool at 50kV, which offers a quick overview of the real capability (resolution, sensitivity, contrast, exposure latitude) of the resists or material platforms compared to others, with respect to the ITRS specifications but also MAPPER requirements. If results were correct, resists or materials were evaluated directly at 5kV on the MAPPER pre-alpha tool, located into the CEA-LETI clean room environment. In addition, CEA-LETI offers to resist suppliers the facility to evaluate their resist platforms at 100kV on a Gaussian beam

(VISTEC-VB6-UHR) in order to extract their ultimate resolution capability of their best platforms. Correlations data could be made between 5, 50 and 100kV exposure results on one resist platform using same process conditions. The paper will discuss also of other different tool conditions that can influence the lithographic performances of the resists, such as the spot size, the substrate material...

This paper will be give a global overview regarding resist process progress for 5kV MAPPER application, and by the way an overall understanding of which parameters (from resist etc...) we can play finally to achieve all final specifications required. This infrastructure, available at CEA-LETI, is worldwide unique and can speed up new resist progress from resist vendors point of view.

8323-60, Poster Session

Silicon-containing block copolymers for sub-10nm patterning

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Block copolymers demonstrate potential for use in next-generation lithography due to their ability to self-assemble into well-ordered periodic arrays on the nanometer length scale. Successful application of block copolymers in lithography relies on three critical conditions being met: high interaction parameters (χ) which enable formation of <10 nm features, reactive ion etch selectivity between blocks for facile pattern transfer in template formation, and thin-film self-assembly control. The present work describes the synthesis and self-assembly of block copolymers composed of combinations of three different hydrocarbon blocks coupled to a glassy silicon-containing block synthesized by ARGET ATRP or anionic polymerization. The block copolymers exhibit large χ values, enabling formation of 5 nm feature diameters, and demonstrate bulk self-assembly of body-centered cubic spheres and hexagonally packed cylinders. The homopolymer etch rates were measured and demonstrate remarkable etch selectivity between the two blocks due to silicon incorporation in one block. Furthermore, thin film self-assembly is demonstrated through a combination of spin-coating and solvent annealing techniques, which produce some of the smallest block copolymer features in thin films reported to date.

8323-61, Poster Session

Maskless EUV lithography: an already difficult technology made even more complicated?

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In this paper, we shall present a review of the emerging opportunities across two seemingly unrelated research fields: IC and NEMS (nano-electromechanical systems). The current status of maskless EUV lithography will be updated, as well as the latest NEMS research progress to enable this promising technology. It will be shown the nanomirror based maskless approach is one path to cost-effective EUV lithography, rather than making it even more complicated. Maskless lithography can help to reduce the impact of defects on "masks" by allowing redundant printing and using much higher image demagnification (e.g., 100x). Redundant printing of each pixel with several exposures using different nanomirrors will significantly reduce the defect counts on the wafer. The high image demagnification adopted by maskless EUV lithography is of particular interest as the printable "mask" defects will be much larger, thus easier to be detected. Moreover, the EUV phase errors/defects can

be readily compensated with adaptive wavefront engineering enabled by the grayscale/analog operation of nanomirror array. We shall also report the scaling and fabrication results of nanomirrors actuated by stable high-density vertical comb structures. EUV maskless lithography system requires 100-1000 million programmable nanomirrors to replace the physical masks and achieve satisfactory throughput. Each nanomirror consists of about 40 Mo/Si layers with total thickness of about 0.3um. Although the mirror size is sub-micron, the deep nanoscale vertical-comb actuation gaps will require a sub-100nm (half-pitch) lithographic resolution, resulting in our categorizing this type of mirror as a NEMS device. The stability of nanomirrors is also an important issue, thus stable devices such as the vertical-comb nanomirror was designed to overcome the instability problem. An update of nanomirror system and configuration requirements based on the latest EUV progress will also be presented. 10-16 nm (half pitch) logic patterning can be the possible insertion point for maskless EUV lithography.

8323-62, Poster Session

A phase segregating polymer blend for 2xnm feature applications

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A phase segregating polymer blend comprising a SOD precursor polysilazane and an organic polymer PSαMS [poly(styrene-co-α-methyl styrene)] was studied. Two polymers in this blend are completely miscible in casting solvent. After coating and post-applied bake, two polymers phase separate to form various geometries. By utilizing approaches employed in DSA (directed self-assembly) such as patterned substrates, surface chemical modification etc and their combination, we achieved 2xnm spacer and airgap-like structure. When this blend was coated on dry ArF resist line and space patterned substrate, baked for several minutes, PSαMS aggregates to form cylinder phases surrounded by polysilazane phases. Then the substrate was rinsed by casting solvent of the blend to remove PSαMS cylinder phase, and render airgap-like structure. Herein the unique property of the film allows solvent to pass through to wash off PSαMS .The diameter of airgap-like structure can be controlled by volume fraction of PSαMS in the blend. When this blend was coated on pretreated dry ArF resist line and space patterned substrate, baked for several minutes, vertical segregation proceeds: polysilazane aggregates along the topography of resist and crosslink upon heating, leaving PSαMS phase segregates to film top. Then the substrate was rinsed by casting solvent to remove PSαMS phase, resulting in conformal polysilazane growth on resist line pattern, which was finally dry etched into around 20nm spacer. The CD of spacer can be controlled by process condition and volume fraction of polysilazane. Vertical phase separation and cylinder domains in the film of this blend can be straightforwardly observed by cross-section SEM respectively.

8323-63, Poster Session

2nm quantum optical lithography

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Diffraction effects limit the minimal resolvable feature size to the Rayleigh diffraction limit of $\lambda/2$, where λ is the wavelength of the light. In the past decades many lithography techniques has been tested in order to beat the diffraction limit. Some schemes of quantum lithography are based on an N-photon absorption process and achieve a spatial resolution of $\lambda/(2N)$. Here, we are able to present an optimized material [1-2] with a significant improvement of the lithography resolution beyond diffraction limit of visible light. AFM, TEM and SEM reveal 2nm and 4nm lines realized by direct laser writing (Fig. 1-2). Channel depths between 1.5 - 5 nm were obtained on the recorded samples.

The new 2nm Quantum Optical Lithography (QOL), as extremely high-resolution lithography technique is attractive for fabrication of 3D structures with nano-scaled resolution.

[1] E. Pavel, S. Jinga, E. Andronescu, B. S. Vasile, E. Rotiu , L. Ionescu, C. Mazilu , Nanotechnology, 22 (2011) 025301

[2] E. Pavel, US Patent No. 6,132,643 "Fluorescent photosensitive vitroceramics and process for production thereof"

8323-64, Poster Session

Detailed mesoscale dynamic simulation of block polymer directed self-assembly processes: application of protracted colored noise dynamics

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Directed self assembly (DSA) of block copolymers is a very promising technique for producing sub-30 nm pitch regular patterns. In order to speed the development of such techniques and to understand the behavior and limitations of such processes, computer simulation of such methods are proving invaluable. A variety of computational modeling approaches have already been used to explore the behavior of block copolymer phase separation and directed self-assembly including techniques based on mean field approaches and Monte Carlo techniques. While these methods provide great computational expedience, in general they have suffered from a number of disadvantages, such as the use of less accurate potentials and the requirement that a subset of dynamic moves be intelligently chosen, that can affect the accuracy of the predicted outcomes from such simulations. Conversely, molecular dynamics combined with realistic potentials provide more accurate simulation of the inherent polymer behavior, dynamics, and equilibrium states without a need to guess modes of molecular movement and without oversimplifying interatomic interactions, though computational efficiency is sacrificed. In fact, in theory atomistically detailed molecular dynamics could be used to carefully study such DSA processes, but the large spatial size of the domains of interest in DSA processes cause the number of atoms required in such an accurate simulation to be infeasible currently. In addition, the number of molecular dynamics steps required under realistic simulation conditions (i.e. realistic temperatures and interatomic potentials) to be able study the phase separation process are also currently not practical. In this work, the number of atoms required to simulate a useful size of polymer during the DSA process has been reduced by coarse graining the atomistic model into an accurate mesoscale model based on Kuhn segment beads to represent the polymer chain. The details of these coarse grained models for popular DSA material systems such as PS-b-PMMA will be discussed and validated. Furthermore, techniques based on protracted colored noise dynamics (PCND) for increasing local fluctuations in the polymer that can enhance the polymer diffusivity and allow for study of block copolymer phase separation on reasonable computational time scales have been developed. In these PCND techniques, the frictional coefficient is decoupled from the distribution of the stochastic force which amounts to using a time correlated colored noise instead of the traditional white noise that is used in Langevin dynamics. The combination of these coarse grained mesoscale polymer models with the PCND annealing techniques will be discussed and demonstrated through application to the study of PS-b-PMMA DSA processes. The ability to quantitatively match experimental results, such as domain scaling with polymer molecular weight and defectivity data, will be shown.

8323-65, Poster Session

Novel fluorinated polymers for releasing material in nanoimprint lithography

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In recent years, utilization and reduction of pattern size are following nanoimprint lithography quickly. In nanoimprinting, since it is contact printing, a higher separation force might cause damages to the master and imprinting tool, degradation in pattern quality as well. There is a mold-release characteristic of a master and resin as one of the biggest subjects in utilization. Then, we focused on release materials, the new fluorinated polymers based on α-chloroacrylate, added to mold resin was developed. In this paper, we will report these synthesis methods , specific properties such as static and dynamic contact angle and further fluorinated polymers were segregated resin surface.

8323-66, Poster Session

25nm pitch master and replica mold fabrication for nanoimprinting lithography for 1Tbit/inch2 bit patterned media

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This paper desribes difficulties we faced, and solutuions we established by screening materials and optimizing process, to fabricate a 25nm pitch master by EBL, and a replica mold by NIL as well, for Nano-Imprinting Lithography for 1Tbit/inch2 Bit Patterned Media.

Even by EBL, 16nm holes in 25nm pitch are hardly made in a large area, even if ZEP520A or HSQ used, due to significant dark erosion. The holes in the nearest were sporadically connected, not isolated, below 35nm pitch, even when the most high contrast ZEP developer (IPA+PFC mixture) we found was used. Then, we changed strategy to make smaller holes such as 8nm, and to ream it to the target, and suceeded.

In the 25nm pitch BPM replica fabrication by NIL, there were severe difficulties we found, such as pillar-missing, pillar-collapse, and releasing force increase, which also worked to retard coutinuous imprinting for the mold replication. We have been foucing on a releasing material of "PFPE main chain with -OH termal", and proved that it helped reducing the pillar-missing significantly on 30nm to 25nm diameter pillars. Then, we did keep pursuing if it could be still functional for the 25nm pitch BPM mold, i.e. 15nm pillars. We also studied about adhesion promoter and NIL resist to eliminate the imprintig defects.

8323-67, Poster Session

Combined dose and geometry correction for multi-electron-beam lithography: application to the 22nm node

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Lithography faces today many challenges to meet the ITRS road-map. EUV lithography is still challenged by the availability of high power source and mask defectivity and suffers from a high cost of ownership perspective.Parallel to this, mask less lithography regularly makes significant progress in terms of potential and maturity. The massively parallel e-beam solution even appears as a real candidate for high volume manufacturing. The way to industrial maturity is still long for maskless lithography, as current development is still on the path for the first alpha tools.

Among the developments to be performed to secure the takeoff of the multi-beam technology, the availability of a rapid and robust data treatment solution will be one of the major challenges. Within this data preparation flow, advanced proximity effect corrections must be implemented to address the 22nm node and below. This paper will detail this process and compare correction strategies in terms of robustness and accuracy. It will focus on results obtained using a MAPPER tool within the IMAGINE program driven by CEA-LETI, in Grenoble, France. A status on the development work already done will be presented. Using the advanced E-Beam Proximity Correction (EBPC) available in the software platform Inscale from Aselta Nanographics, 32nm and 22nm SRAM structures could be patterned with high accuracy in terms of CD

control and ISO/dense bias. Finally, the paper will help to get a better understanding of the work still to be done to be on time to meet the maskless lithography challenge.

8323-69, Poster Session

Multiple columns for high-throughput complementary e-beam lithography (CEBL)

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Developers of e-beam lithography systems are pursuing diverse strategies to bolster throughput. To achieve parallelism, some e-beam efforts focus on building multiple-columns, and others focus on developing columns with multiple beamlets.

In this paper, we discuss the benefits of a multiple column approach for a particular application: Complementary E-Beam Lithography (CEBL).

CEBL is a novel approach where the e-beam lithography system is used only to pattern the smallest features. Everything else is patterned with existing optical lithography equipment. By working hand-in-hand with optical lithography, CEBL provides an urgently needed solution to create next-generation microchips. Moreover, CEBL is extendable for multiple technology generations.

We show how a multiple column approach is the best way to meet the requirements for CEBL, including high throughput, high resolution and overlay accuracy, without excess complexity or cost.

Multiple columns enable:

1. Higher patterning currents with one source per column

2. Faster patterning speed with a vector scan shaped beam strategy which leverages CEBL's low pattern density

3. Distributed patterning, reducing localized heating and improving overlay accuracy

4. Parallel data paths, simplifying electronics and system implementation

In addition, we discuss Multibeam's methodology to achieve high overlay accuracy in mix and match with optical lithography. This includes an architecture that enables the calibration of every electron beam using on-stage and on-wafer alignment marks.

We will present these and other features of Multibeam's multiple-column vector-scan shaped-beam technologies, as well as the current status of development.

8323-70, Poster Session

Addressing LER through atomistic self-assembly

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Line edge roughness (LER) is a difficult problem in patterning for advanced technology nodes. Fundamental granularity of the exposure process and the patterning materials are difficult to eliminate. Remaining artifacts of line edge roughness affect the electrical performance of the structures to be created. This is especially critical for FinFET processes, in which the fin shape, width and surface are lithographically defined, and have a dramatic impact on the performance.

The goal of this paper is to explore options to reduce the remaining line edge roughness from the lithographic patterning steps by combining them with process steps typically used in the chip manufacturing process. Epitaxial growth and regrowth processes represent self assembly on an atomistic level of the lattice. We propose and examine combinations of lithographic processes with epitaxial growth and regrowth that address the line edge roughness problem. The resulting combination can be used during the device formation or in the production of hard masks.

The work is based on the extensive use of simulation tools, notably physical lithography simulation tools, which addresses the lithographic processes, and Technology CAD (TCAD), which addresses other processes in the device formation, as well as the assessment of the electrical device performance.

In the first part of the paper, we use TCAD tools to show the impact of process artifacts on the device performance, allowing us to assess patterning options.

In the second part of the paper, we examine the line edge properties of lithographic steps and other processing steps, notably amorphization, epitaxial growth and regrowth, and selective etching. We show several possible combinations of process steps that drastically reduce the remaining line edge roughness by smoothing rough surfaces in the atomistic self-assembly process. The obtained surfaces are smooth on the microscopic scale, with surface atoms aligned along a particular crystallographic orientation and only a few atomistic steps remaining that correspond to three sigma line width roughness of under one nanometer. Such atomistically smooth surfaces enable manufacturing of FinFETs and nano-wires through the end of the roadmap.

8323-71, Poster Session

Plasmonic lithography modeling and measurement of near-field distribution of plasmonic nano-aperture

Y. Kim, H. Jung, S. Kim, J. Jang, Yonsei Univ. (Korea, Republic of); J. Y. Lee, Korea Research Institute of Standards and Science (Korea, Republic of); J. W. Hahn, Yonsei Univ. (Korea, Republic of)

A simple analytic plasmonic lithography model is suggested to predict profiles of exposed and finally developed pattern with a finite contrast of photoresist. In this model, the developing process is revisited by accounting the variation of dissolution rate with respect to expose dose distribution. We introduce the concept of nominal developing thickness (NDT) to determine the optimized developing process fitting to the isointensity profile. Based on this model, we obtained three dimensional distribution of near-field of bowtie shaped plasmonic nano aperture in a metal film from the near-field lithography pattern profile. By illuminating 405 nm diode laser source, the positive type photoresist is exposed by the localized electric field produced by nano aperture. From the measurement of developed pattern profile with a atomic force microscope (AFM), the three-dimensional isoexposure (or iso-intensity) surface at the very near region from the exit plane of an aperture (depth: 5 ~ 50 nm) is profiled. Using the threshold dose of photoresist and exposure time, the absolute intensity level is also measured. Concerning with the error in exposure time and threshold dose value, the error in measurement of profile and intensity are less than 6% and 1%, respectively. We expect the lithography model described in this presentation allows more elaborated expectation of developed pattern profile. Furthermore, a methodology of mapping is useful for the quantitative analysis of near-field distribution of nano-scale optical devices.

8323-72, Poster Session

Analysis of line-width error in digital micromirror device-based maskless lithography

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By defining the diameter of an airy disc as 2.64 µm, the exposure dose distributions of line/space (L/S) patterns were calculated with the variation of the laser source power in a point array technique for a digital micromirror device (DMD) based maskless lithography. Using the result of

the exposure dose distribution, L/S patterns were simulated considering the photoresist contrast effect. With the results of the threshold exposure dose and the clearing exposure dose of the photoresist, we predicted the development tendency of the patterns, whether the patterns will be fully developed, underdeveloped or undeveloped patterns. As the laser source power increases, the line width of the pattern gradually increases and the variation of the line width grows, approaching the narrow L/S pattern, which shows the increase of the pattern width error. An experiment was conducted to verify that the simulation results substantially follow the simulation parameters, finding as a whole that the line widths of the experimental results follow the simulation results. From the results, the minimum line widths of the patterns achieved are about 3.44 µm and 3.89 µm at laser source power levels of 100% and 60%, respectively. The standard deviations of the measured line widths are 0.28 µm and 0.03 µm when L/S = 4 µm and 13 µm, respectively. To analyze the pattern width error, we re-calculated the pattern profile with the random variation of intensity of each airy disc and spot pitch. We set the intensity uniformity of each spot to ±5% and set the spot pitch error to the half of spot separation which is a defined term in point array technique. From this result, the required specifications of spot array for DMD based maskless lithography system will be proposed.

8323-73, Poster Session

Design of a high positioning contact probe for plasmonic lithography

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Plasmonic lithography using a contact probe with nano aperture records nano-meter scale features. The probe is commonly based on a micro-cantilever probe which has been used for atomic force microscope (AFM) and near-field scanning optical microscope (NSOM). To achieve high throughput, a contact mode without feedback is appropriate to the lithography process. A cnatilever probe, however, inherently deviates on the substrate in approach mode since the probe has bending angle by a contact force. The deviation leads to the tip-positioing problem of patterning results with a single probe or array probes. We propose a geometrically modified contact probe to achieve high positioing accuracy. To reduce lateral deviation in a approach to substrate, we design a "circular probe" which has arc-shaped arms. Because the modifeid probe is theoretically based on the "fixed-fixed beam" concept in material mechanism it has a degree of freedom to a contact force opposite to a conventioanl cantilever probe. To confrim its positioning accuracy, we simulate motions of the probe with a finite element method (FEM). We calculate the tip displacement for a circular probe and compare the results with those using a conventional cantilever probe. The desiganed probe has a square outline boundary with a length of 50µm, four arc-shaped arms and a pyramidal tip with a height of 5µm. The circular probe has higher positioning accuracy by a factor 103 and 10 in its approach mode and scan mode, respectively, compared with a cantilever probe.

8323-74, Poster Session

Sub-30nm resolution plasmonic patterning with a circular contact probe

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Current development of plasmonic direct writing technology has enhanced resolution and throughput for the industrial application. We developed a circular contact probe for plasmonic direct writing, maskless lithography. The circular probe has four-armed circular shaped planar spring structure and tip at the center to allow high positioning accuracy in scan mode (< 1 nm). The probe is made of 350 nm-thick silicon nitride membrane and 150 nm-thick aluminum films. By mechanical polishing of and pounding of probe tip surface, we achieved ultra-smooth metal surface (Rrms: < 0.2 nm, Rpv: < 3 nm) over contact area (~ 10 µm2). It

is possible to maintain a uniform gap distance and to minimize damage between a probe surface and a photoresist without external gap control unit. In addition, we applied 5 nm-thick diamond like carbon films as a protection and lubricant layer to reduce stiction and friction. For a sharp ridge shape, we fabricated a bowtie shaped nano aperture by using FIB milling through the SiNx membrane side. To demonstrate a performance of the plasmonic patterning with the circular contact probe, we will introduce the line pattern results having a sub 30nm resolution and arbitrary shaped patterns. For practical applications, we will show that these near-field shallow patterns can be transferred into ~200nm deep silicon substrate by means the hard mask strategy. Thus, we believe that this technique provide a promising way for small size volume fabrication of photonic, plasmonic nano-scale devices.

8323-75, Poster Session

Optimization of chemically amplified resist for high-volume manufacturing by electron-beam direct writing toward 14nm node and beyond

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Electron-beam direct-writing (EBDW) technology is a primary solution that offers cost-saving production of a wide variety of LSIs in small quantities. Moreover, it also seems to be one of the most promising techniques for manufacturing next-generation LSIs by multiple EB writing. Our multi-column cell (MCC) EBDW system based on the character projection (CP) [1] is considered to be the most suitable method from the viewpoint of the extension of the single beam CP based system, which we have already applied to LSI manufacturing [2, 3]. To introduce the MCC system in manufacturing sub-14 nm technology node LSIs, particular resist materials and process development are required to obtain high resolution and throughput.

In this paper, we will present the estimation of the Coulomb effect and electron-beam blurs using the CP based MCC system to calculate the tolerance of resist blur and make use for a material design. For the estimation of the blurs, we use an EB lithography simulator and actual resolution data of a non-chemically amplified resist, hydrogen silsesquioxane (HSQ), exposed by the proof of concept (POC) system of the MCC with an acceleration voltage of 50 kV. We will also investigate the reduction of the resist blur by using a positive chemically-amplified resist with short acid diffusion length. We have already succeeded in resolving 22 nm line and space patterns at a dose of 78 uC/cm^2 and will try for the fabricating of less than 20 nm line and space patterns at 75 uC/cm^2 for a practical use in manufacturing 14 nm technology node LSIs. Further, the impact of an ultra-thin anti-static film onto the resist films will be discussed for the Coulomb effect blur, resolution, and alignment.

[1] A.Yamada et al., J.Vac.Sci.Technol.B, 26 (2008) 2025.

[2] T. Maruyama et al., Proc.of SPIE, 6921 (2008) 69210H.

[3] Y. Machida et al., Microelectron. Eng. 87 (2010) 1131.

8323-76, Poster Session

Novel neutralized layers for DSA lithography by using reactive self-assembled monolayers

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Novel method and materials for nano-scale patterns of self-assembled block copolymers for directed self-assembly (DSA) were investigated. Two kinds of reactive self-assembled monolayers (SAMs), one was photo-reactive and the other was thermal reactive, were synthesized. The cast SAMs were quickly adsorbed on the substrates with high

density and then the spincoated polymers on them for neutralized layers were firmly immobilized by the photo exposure or thermal annealing, respectively. The vertically aligned block copolymers for nano patterning were formed of the neutralized layers. This method has an advantage of short processing time using conventional coaters. In addition, if the polymers for neutralized layer were replaced to photo-sensitive polymers formed by the thermal annealing process, the surface energy would be controlled and chemical guides would be easily prepared.

8323-77, Poster Session

Study of device mass production capability of the character projection based electron-beam direct-writing process technology toward 14nm node and beyond

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The Multi column cell (MCC) exposure system is a promising candidate for the next generation lithography. The key concept of the MCC is the parallelization of electron beam (e-beam) columns with a character projection (CP) [1]. Therefore it can be expected that the property of the existing CP based e-beam direct writing (EBDW) technology will be applicable to the rapid establishment for the next generation process technology using the MCC exposure system. A CP based EBDW technology has been generally regarded as a technology for limited applications such as a prototype device manufacturing. However it can be used for mass production if we could control key factors such as effective utilization of a CP mask, multilayer proximity effect correction, equipment control, etc. We have already established the CP based EBDW process technology for 65nm node with sufficient yield and process margin for a production level.

In this paper, the techniques for the device mass production using the CP based EBDW and the manufacturing field data of 65nm node will be shown. Also 32 nm node device data will be presented and extendability of these techniques to 14 nm node device and beyond will be discussed. Through this work, the CP based EBDW system with 50 kV acceleration voltage, 25 A/cm2 current density and 300mm wafer stage were used.

In our system there are over 200 characters in one area and one CP mask include 25 areas. Therefore only one CP mask was needed for multiple devices and nodes. In addition any critical dimension (CD) change caused by a deterioration of the CP mask has not occurred for over one year.

In order to correct the multilayer proximity effect, the simplified electron energy flux (SEEF) model [2] was adopted. While the SEEF model powerfully corrected the multilayer proximity effect, it was very important to decrease the total amount of backscattering electrons to achieve enough process margin especially for a narrow space surrounded by a large open area. Therefore the EB/KrF hybrid exposure method in a same layer was adapted. By adopting the above techniques the 3sigma of CD variation through multi under layer condition was less than 4 % of the target CD.

Scheduled maintenances have been properly performed, and more than 10,000 production wafers have been successfully exposed so far without any major system downtime.

[1] H. Komami et al., Microelectron. Eng. Vol. 88, Issue 8, pp. 2009-2012. 2011

[2] K.Ogino et al., Jpn, J. Appl. Phys. Vol. 43, pp. 3762-3766. 2004

8323-78, Poster Session

Block co-polymer guided self-assembly by surface chemical modification: optimization of multiple patterning process and pattern transfer

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Block co-polymer (BCP) guided self-assembly is emerging as a viable alternative technology for patterning beyond the 22 nm node [1,2]. Surface chemical modification is one of the approaches to define the guiding patterns. This process is based on using lithography and reactive ion etching techniques for creating different chemical terminations on the surface [3,4]. We present a variation of the process that simplifies the lithography requirements for defining the guiding pattern.

All the styrene and methyl methacrylate co-polymers used in this work have been designed and synthesized on purpose for this study. They have been synthesized by RAFT polymerization (Reversible Addition-Fragmentation Chain Transfer) and by ATRP polymerization (Atom Transfer Radical Polymerization) in order to efficiently control the molecular weights of each block and thus, the poly-dispersity index [5].

The pitch of the guiding pre-pattern can be equal (single patterning) or twice (double patterning) the length of the BCP chain [6]. Although the double patterning process has been shown to prove very good results in terms of resolution and line edge roughness, it imposes a tight restriction to the lithography process to create the pre-pattern. Therefore, we have developed an easier self-assembly process with more relaxed pre-pattern restrictions, which we define as multiple patterning guided self-assembly (see figure 1). We present results on the process optimization including the pattern transfer.

The process sequence is as follows: first, an ultra thin layer of hydroxyl terminated polystyrene as polymer brush is grafted to the silicon substrate. This layer is selectively chemically modified by oxygen plasma, using a PMMA layer which has been deposited on top and patterned by e-beam lithography as a mask. After removing the PMMA, the PS-b-PMMA block co-polymer is spin coated and annealed to obtain the guided self-assembly templates. Then the MMA block is selectively removed by oxygen plasma. After removing the MMA block by oxygen plasma, we remove the brush polymer by oxygen plasma. Then we etch the SiO2 layer by C4F8 gas and finally we remove the rest of polymer on the surface by strong oxygen plasma.

We have determined the optimal conditions of the oxygen plasma process for modifying the brush polymer and the influence of the width of the guiding pattern (see figure 2). In addition, we have tested the use of another brush polymer to create the two different chemical terminations on the surface. In this case, the process consists on completely removing the PS-OH layer in the guiding pattern and then grafting a neutral brush polymer (PS/PMMA random co-polymer) [7] in its place. This neutral brush is less hydrophilic than the plasma-modified PS-OH, so both polymer blocks would have the tendency to wet it producing a more stable final pattern. Three PS/PMMA random co-polymers with different terminations (none, hydroxyl and carboxyl) have been tested.

Multiple patterning process conditions and pattern transfer optimization results will be reported. We conclude that this approach is suitable to create patterns with 22 nm pitch and below while relaxing the requirements of the lithography step.

8323-79, Poster Session

Proximity effect correction using multilevel area density map for character projection-based electron-beam direct writing toward 14nm node and beyond

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Electron beam direct writing (EBDW) is an effective lithographic technique for 14 nm node and beyond. In the past, EBDW was restricted to mostly mask making and small volume device manufacturing because of its throughput limitation. Multi-column cell (MCC) EBDW system based on the character projection (CP) has been proposed [1]. To apply the MCC system in high volume manufacturing sub-14 nm node devices, following problems associated with the proximity effects have to be overcome. Electron-beam blur is a factor determining the resolution of the finest achievable patterns. As the CP technique is able to reduce electron-beam blur, all patterns of various sizes are required to make as CP characters in spite of a limited amount of CP characters on a CP mask. In addition, as the pattern pitch becomes narrower, the proximity effect caused by the middle range scattering between the forward scattering and the backscattering is not negligible. Also, in the conventional shape modification method, the corrected shapes of patterns, which are different depending on neighboring patterns, cause the dramatically increase of required CP characters. In the conventional dose modulation method, additional required exposure shots cause the throughput degradation.

To confirm the feasibility of decreasing the electron-beam blur for any patterns on a chip, we have estimated the range of the designed linewidth that can be supported by a CP character consisting of a line pattern with fixed width. Lines-and-spaces (L/S) patterns of 20 nm or larger in half-pitch can be written by using a CP character consisting of a 23 nm line pattern at the total blur, which includes electron-beam blur, forward scattering and resist blur, is 11 nm. The upper limit of the L/S pattern size supported by the CP character is determined by the amount of corner rounding or the throughput. In this paper, the number of CP characters, which all patterns of various sizes can be written, will be discussed.

For the above-mentioned issues can be solved, we have developed an advanced proximity effect correction method by the backscattering deposited energy, which is estimated by multiple area density maps with different mesh size according to the range of electron scatterings such as the backscattering and the middle range scattering. In our method, after the exposure dose of each CP character's shot is corrected, minimal auxiliary shots are generated by using the multiple area density maps in order to balance the accuracy and the throughput. In this paper, furthermore, the influence of the auxiliary shots will be strictly evaluated for the throughput.

[1] A.Yamada et al., J. Vac. Sci. Technol. B Vol. 26, pp. 2025-2031 (2008)

8323-80, Poster Session

Feasibility study of character projection-based electron-beam direct writing for logic LSI wiring including automatically routed area with 14nm node technology case

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Multi column cell (MCC) exposure system is a promising candidate for the next generation lithography tool. The concept of MCC is parallelization of the electron beam columns with character projection (CP) [1]. CP based electron beam direct writing (EBDW) is regarded as, primarily for hole layers, able to draw only repetitive patterns such as standard cells and memory cells and difficult to be used for router-generated wiring. In this paper, we will describe CP based EBDW method to draw automatically routed wiring area with 14 nm node technology case.

We have been manufacturing 90nm and 65nm technology products with CP based EBDW with the equipment capable to register up to 200 characters of patterns for a layer in which regular patterns of standard cells and SRAM cells are installed [2]. "Master block method" is also available, which realizes to draw required length and width patterns by cutting out of line(s) CP pattern(s).

Though it is possible to draw wiring patterns of LSI products with registered characters and master block method, more improvement of throughput is necessary to apply CP based EBDW for volume manufacturing. In this study, we are going to propose ultra regular layout tiles for automatically routed area drawing.

The next generation CP based EBDW equipment provides 4,000 characters of 1.5 m x 1.5 m (2.25 m2) area each. It is also possible to crop these characters as ones in smaller than 1.5 m x 1.5 m rectangle area which enables to flexibly leverage total CP resources.

To render automatically routed wiring area with ultra regular layout tiles, routing elements with multi layer metal system are proposed. These elements are consisted with vertically crossing metal layers and vias to connect them each other. Each metal shot has a side with open and short control which provides switching state for four sides of the element, attributing sense of wirings. Jog changes for tracks and directions are controlled by vias. Tiling these elements build up wiring network compatible with automatically routed wirings.

We have investigated the feasibility to construct automatically routed area of logic LSIs with defined routing elements consisted with patterns of model character set. Lines and spaces of 20nm half pitch are assumed as for 14nm node technology case. This model set of routing elements provides double via scheme and uniform pattern density with 16 x 16 tracks. CP resource management, trade-off between drawing data volume and routing element granularity, pattern density influence for process margin and shot noise tolerance of model set will be discussed with investigation result of ARM11 based test GDS case.

[1] H. Komami et al., Microelectron. Eng. Vol. 88, Issue 8, pp. 2009-2012. 2011

[2] Y. Machida et al. Microelectronic eng. 87 (2010) 1131

8323-81, Poster Session

High-resolution laser direct writing with a plasmonic contact probe

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We developed a nanolithography system that uses two kinds of contact type near-field optical probe: with a solid immersion lens probe (SIL-probe) or a probe that holds plasmonic nano aperture (Nano-probe). The SIL-probe is made from half ball lens (BK-7) having conical shaped to have small contact area for near-field writing. With a high refractive index medium (n=1.5) between the objective lens and the processing material, the pattern resolution up to 150 nm (FWHM) is achieved in SIL-probe for 405 nm laser source. Using a plasmonic contact probe with bowtie shaped nano aperture in aluminum metal film, we obtained an optical spot beyond the diffraction limit and the size of spot was less than 30 nm at 405 nm wavelength. The nano aperture was milled by focused ion beam (FIB) and diamond-like carbon (DLC) was deposited on the surface of probes for protection and lubrication. The raster scan mode for the arbitrary patterning was developed for practical applications and in both cases, the probe scans over the sample surface in contact mode. By eliminating the external feedback control unit, we achieved high scan speed up to 10mm/s. The system covers pattern resolution from micro-scale to sub-30 nm scale.

8323-82, Poster Session

A new polymer working stamp material investigated for replication fidelity

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We present a full cycle of master->working stamp->imprint in a desktop tool. From a 2" silicon master, we make a cyclic olefin polymer (COP)

replica, and use this COP working stamp to imprint mr-I 7030E, spin coated on a 100mm silicon substrate. We used a Compact Nanoimprint Tool (CNI).

The silicon master contains a 10x30 mm chirped grating field. Master features are 530 nm deep half-pitch grooves. Pitch varies across the grating. Pitch is 1 µm away from the flat and 2 µm near the flat.

We used a blank solid CNI stamp to transfer the master pattern into the inverse pattern on a 200 µm COP film with glass transition temperature 138°C. Imprint parameters were: Temperature 165°C, pressure 6 bar, time 20 minutes, demold temperature 100°C. Long imprint time was chosen to ensure complete filling of the master grooves.

The COP replica was the used to imprint 300nm mr-I 7030E resist with Tg=60°C. Imprint parameters were: Temperature 110°C, pressure 6 bar, time 10 minutes, demold temperature 60°C.

AFM analysis shows that pitch is preserved from master stamp to imprinted structure measuring 2.02 µm on the master south end and 2.00 µm on the imprint south end. The depth of the structures is also preserved being approximately 530 nm and 525nm on master and imprint, respectively.

In conclusion; CNI can successfully make COP working stamps from an expensive silicon master, and these can be used for nanoimprint. High fidelity replications have been demonstrated.

8323-83, Poster Session

Feasibility study of optical/e-beam complementary lithography

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Electron beam direct write (EBDW) has been discussed as possible patterning solution for current and future lithography nodes for many years [1]. Due to the longer writing time and consecutively low throughput, this maskless technology is only applied for R&D and niche applications today such as rapid prototyping, design verification and chip personalization. For real low volume CMOS manufacturing or even mass production, significant throughput enhancements would be necessary and solutions are on the way such as multiple gaussian or multiple shaped beam tools [2,3]. Using e-beam as a complementary approach together with standard optical lithography at 193nm or EUV wavelength has been proposed only lately and might be a reasonable solution [4,5]. Here, the high throughput of the optical litho can be combined with the high resolution and the high flexibility of the e-beam by using a mix & match approach (Litho-Etch-Litho-Etch, LELE).

Complementary lithography is mainly driven by special design requirements for unidirectional (1D gridded) Manhattan type design layouts that enable scaling of advanced logic chips. This requires significant data prep efforts such as layout splitting.

In this paper we will show recent results of complementary lithography using 193nm immersion generated 50nm lines/space pattern addressing the 32nm technology node that were cut with electron beam direct write. Regular lines and space arrays were patterned at GLOBALFOUNDRIES Dresden and have been cut in predefined areas using a VISTEC SB3050DW e-beam direct writer (50KV Variable Shaped Beam) at Fraunhofer Center Nanoelectronic Technologies (CNT) as well as on the PML2 tool at IMS Nanofabrication. Several e-beam resist types with high etch resistance were used for the cut exposure, covering the lines/space arrays as etch mask for the second cut etch step.

Integration issues as well as overlay requirements and performance improvements necessary for this mix & match approach will be discussed.

8323-85, Poster Session

Optimization of the MSB approach for future technology nodes

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The already presented Multi Shaped Beam (MSB) approach is considered a potential solution for high throughput mask write application.

The key element for achieving write time reduction is a higher target current, which can be obtained by increasing the number of beamlets as well as applying a higher current density. In the present paper the approach of a 256 beamlets MSB design will be discussed. For a given image field size both beamlet pitch and size have to be optimized, if the number of beamlets increases. Besides electron-optical constraints, pattern layout aspects have to be taken into account.

The effect of global space charge distortion and its impact on the lithographic performance, depending on the applied current density and image field size will be discussed. Based on first electron-optical simulations for the new final lens a larger demagnification seems to be advantageous.

During the exposure of a pattern layout the number of used beams and their distribution within the image field varies, which can lead to space charge distortion effects (see Figure 1). In regards to this MSB simulation results obtained for an image field of approximately 10x10µm² will be presented.

For the 256 beamlets MSB design and a current density of 60A/cm² write time simulations and LER simulations have been performed. For MSB pattern data fracturing an optimized algorithm has been used. Data integrity as an important aspect of the production worthiness of such a systems will be discussed specifically.

8323-86, Poster Session

Integrated lithography to prepare arrays of rounded nano-objects

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We present an integrated lithography method capable of producing wavelength-scaled periodic arrays of versatile rounded nano-objects with arbitrary array symmetry. The proposed idea is to illuminate colloid sphere monolayers by circularly polarized beams possessing different lateral intensity distributions. Four structure parameters as the t distance, p periodicity, a ring thickness, and d0 ring-diameter can be tuned independently. The integrated lithography combines the advantages of two techniques, as the symmetry and periodicity of the wavelength-scaled interference modulation determines a periodic pattern, while the intensity concentration in the near-field of the colloid-spheres occurs only within an area much smaller than the wavelength.

8323-87, Poster Session

Improved electron backscattering representation using a new class of distribution: application to EUV masks

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In Electron Proximity Effect Correction software, electron lithography or electron microscopy modeling, the influence of electron backscattering from a substrate is generally handled using a Point Spread Function (PSF). Starting from the work of Chang [1], the PSF is commonly approximated as a sum of Gaussian distributions. Recent papers have emphasized that the Gaussian approximation was not perfectly suited

in the case of Extreme UV mask substrates. In this case, an increase of backscattered energy is observed in the mid-range due to the high Z material used as an absorber in EUV mask substrates. An exponential function has been empirically found by Tanabe et al. to provide a better approximation of the mid-range effect than the usual Gaussian. Considering that exponential is not an energy-limited function, it might not be always consistent when writing the equations driving electron proximity correction software tools. In this paper, we will show that another class of distribution can be a good alternative to the usual Gaussian without some of the disadvantage of other functions like the exponential. The advantage of the applied distribution may also be observed for describing the backscattering phenomenon in the traditional chrome-on-glass mask substrates.

The observation of the distribution of backscattered electrons at the sample surface shows off-centered bell shaped components that can be attributed to the backscattering from the absorber and from the substrate. The regular Gaussian used typically is centered on the incident beam, it is therefore not the best choice for an accurate fit. We propose to rather use a distribution that is off-centered. The gamma distribution is a distribution that is well known in statistics. It has a highly tunable shape with a "shape" and "scale" parameter. The analytical form of the distribution and of its cumulative distribution function makes it as convenient to use in practice as the currently used approximations for the computation of intensity distribution in electron beam lithography.

We show a very good fit of the energy distribution in the resist for an EUV mask substrate using a set of two gamma distributions. This legitimates our approach that is especially useful in the case of high atomic number materials like those used in EUV mask substrates.

8323-88, Poster Session

Multistage nanofocusing with 22nm resolution

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A PL that excites and focuses PSPs increases optical transmission of a single sub-wavelength aperture by orders of magnitude, but the demonstrated optical confinement is still limited (about 50 nm in one dimension) by the trade-off between spatial confinement and inherit loss of plasmons. To efficient confine optical energy at deep sub-wavelength scale, a compound multi-stage plasmonic lens (MPL) consisting of a modified ridge aperture, a set of ring couplers and a ring reflector, was designed and prepared on a metallic thin film. Using the dispersion relation of surface plasmons, the MPL excites PSPs with gratings and concentrates them towards the center, where they are converted into LSPs and efficiently penetrated through the ridge aperture, achieving a deep-sub-wavelength confinement with high energy densities. Equipped with a picosecond laser and mounted on an ABS which precisely control the distance at sub-10nm height with a linear speed of 4~14 m/sec, the MPLs enable the high-throughput parallel patterning in practice. Furthermore, with merely 10 mW optical power, the nonlinear thermal pattern formations are observed in the inorganic resist due to the presence of strongly enhanced local field. With 160 MHz repetition rate and 7 m/sec MPL scanning speed, this experiment demonstrates the capability of high-speed patterning with 22 nm half-pitch resolution.

8323-89, Poster Session

Fabrication nanopillars pattern on PDMS using anodic aluminum oxide film as template

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Nano-pillars pattern on PDMS were fabricated by using highly ordered and density nano-pore arrays of anodic aluminum oxide film as template.

We used cyclohexane to dilute polydimethylsiloxane then filled it to template, the pillars diameters range from 100 to 200 nm, pillars height about 3 to 5 µm. The morphologies of template membrane and nano-pillars arrays were investigated by scanning electron microscopy and atomic force microscopy. This process offered a cheaper and easier method to develop a large area and highly ordered nanostructure mold, this mold can be used in a broad range applications such as, optoelectronic devices, semiconductor devices, bio devices, field emission displays, data storage and so on.

8323-90, Poster Session

Spin-on surface treatments for thin film block copolymer orientation control

C. M. Bates, T. Seshimo, C. H. Chen, J. D. Cushen, W. J. Durand, L. J. Santos, C. J. Ellison, C. G. Willson, The Univ. of Texas at Austin (United States)

Block copolymer self-assembly can be exploited to produce sub-optical lithographic resolution1 down to ca. 5 nm, which is especially attractive for emerging technologies such as bit patterned media2. A critical required material property of the block copolymer is that it exhibits a high interaction parameter χ; since minimum feature size is a function of χ, this results in smaller possible features. A particularly challenging consequence of high χ block copolymer materials relates to difficulties in orienting the thin film block copolymer domains perpendicular to the substrate3. A significant contributing factor is the large surface energy combinatorial mismatch between the individual blocks and the two interfaces (non-neutral conditions). While the bottom interface can generally be neutralized using numerous techniques4, the top interface poses a greater challenge. Methods such as solvent annealing have emerged as potentially viable solutions to mitigate the top interface surface energy problem; however, techniques that are compatible with current lithographic production lines would be ideal. The present paper details spin-on surface treatments which were applied directly to a block copolymer thin film. Subsequent annealing and top coat stripping yielded block copolymer self-assembly, which was not observed in films lacking the top coat surface treatment.

8323-91, Poster Session

Environmental control during solvent annealing of silicon-containing block copolymers

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Block copolymers self-assemble on nanoscopic length scales, making them ideal for a variety of lithographic applications including: nanoimprinting, nanoporous membranes, and bit patterned media. The two goals paramount to success are high etch selectivity between the blocks and thin-film orientation control. It has been shown that incorporating silicon into one of the blocks greatly increases the etch selectivity. In addition, the χ value (a block-block interaction parameter) also increases. This is advantageous since the molecular weight of block copolymers able to be synthesized in the ordered region decreases as the χ value increases. As a result, smaller feature sizes are obtainable. Unfortunately, one negative side effect of having dissimilar blocks is an increase in the difference in surface energy between the two blocks. Silicon incorporation lowers the surface energy of its block. Upon annealing, the lower surface energy block migrates toward the low-surface energy air interface in order to minimize the free energy, leading to a wetting layer. Wetting layers promote parallel orientation which is unfavorable. Solvent annealing has been employed as a method of altering the surface energy of the top interface. Solvent annealing has several tunable parameters such as: solvent, annealing time, and vapor concentration. The solvent vapor concentration is important as the block

copolymer swelling thickness varies with changing solvent concentration. It has been shown that orientation is most favored when the block copolymer thickness is a commensurate or incommensurate value of the domain periodicity. Optimal solvents for various silicon-containing block copolymers were selected by studying the swelling ratios of the homopolymers in an apparatus that has tight control over the solvent annealing environment.

8323-92, Poster Session

Block copolymer orientation control using top-coat surface treatments

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Block copolymer thin films, which can self-assemble into ordered, periodic morphologies on nanoscopic length scales, are of particular interest for next-generation lithographic applications. The dimensions of the block copolymer microdomains scale with χ (Flory-Huggins interaction parameter) and N (degree of polymerization). To compete with current optical lithography technology, high χ materials are necessary; however, this introduces problems with thin-film orientation control due to surface energy mismatches between polymer blocks. Polymeric cross-linked surface treatments have been shown to influence the orientation of block copolymer thin films by surface energy matching, but these layers can only influence the underlying surface. An air-polymer interface can disrupt the orientation of high χ materials, complicating pattern transfer. Thus, the focus of this work has been to replace the air-polymer interface with a polymeric material appropriately tuned to minimize the interfacial energy between the underlying block copolymer. The aforementioned material must possess a high glass transition temperature and render the block copolymer unchanged upon deposition and thermal annealing processes. The polymeric top-surface treatment layer has successfully been shown to preclude the formation of low surface energy wetting layers, allowing for pattern transfer of high χ block copolymer materials.

8323-93, Poster Session

Nanosphere lithography technique for fabrication of large area, well-ordered metal particle arrays

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Nanosphere lithography has been shown to be an effective technique for high throughput fabrication of well-ordered patterns over small areas, but expanding the technique to large area coverage of nanoparticles on an arbitrary substrate while maintaining good order has proven challenging. In this report we demonstrate a nanosphere lithography technique for fabricating large area, well-ordered hemispherical metal particle arrays on a variety of substrates. Large area nanosphere monolayers were generated by optimizing assembly at an air-water interface before transfer to a submerged substrate. The addition of PEO to the water bath creates more robust arrays due to the polymer bridging effect. The substrate is supported at a 10o angle so the draining speed can be used to control the rate of deposition, which is essential for defect-free transfer to a hydrophobic substrate, such as the polymer-coated glass used in our work.

With this technique, tunable control over particle size and spacing was achieved in the range of 50-150 nm and 100-400 nm respectively. The final particle spacing is defined by the initial polystyrene diameter, which is reduced by RIE to define the final Ag particle diameter. A double liftoff procedure is then used to transfer the polystyrene pattern to a silver particle array on an arbitrary substrate. Additional control over particle shape and diameter can be obtained by modifying the substrate surface energy. For example, depositing silver on ITO-coated glass rather than a more hydrophilic clean glass substrate leads to a more hemispherical particle shape and a diameter reduction of 20%.

8323-95, Poster Session

Ultimate lithographic performances of advanced resists CAR or non-CAR resist?

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In a period where industry strongly struggles to find a cost effective alternative solution to the double patterning strategy based on 193nm immersion lithography for the 14nm node, resist manufacturers actively started to design new resist platforms for the new potential lithography candidates such as EUV or multibeam lithography. Shall the industry pursue to use CAR or NON CAR for the next generation node? Here is the question. CAR proved its efficiency until now to reach resolution requirements and simultaneously keeping the trade-off between resolution and sensitivity. Nevertheless, below 20nm, edge roughness starts to play an important role on patterning quality and overall critical dimension dispersion. Simultaneously non CAR resist are showing interesting progress in the range of 20-25nm half pitch with reasonable sensitivity levels. In the frame of the IMAGINE program, the open program focused on the development of the multibeam technology launched by LETI and MAPPER, performances of advanced CAR and non CAR platforms have been evaluated at various accelerating voltage from 5 to 100kV. The use of 100kV Gaussian beam is helpful to evaluate with a very small spot size the intrinsic resolution performance of advanced CAR resist versus reference non CAR platforms. These formulations have been then evaluated at 5kV on the MAPPER multibeam platform. This paper reports on the comparison results obtained on those two types of chemistry schemes in terms of resolution, sensitivity and roughness. Then a discussion will be engaged to compare the pros and cons of each chemistry platform.

8323-96, Poster Session

Dithering in raster-scan multiple electron-beam maskless lithography system

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Electron beam lithography provides a potential solution for 22-nm half-pitch and beyond. Recently a production worthy massively parallel electron beam maskless lithography system (MEBML2), with more than thousands of beamlet directly writing patterns on the wafer, has been proposed to overcome the throughput limitation.

In the raster-scan MEBML2 tool, the circuit layout is rasterized into the simple 0 and 1 bitmap format during writing, which simplifies the blanker array design. However, the choice of pixel size of the bitmap has to be optimized between resolution and throughput. A finer pixel size is preferred for better critical dimension (CD) accuracy but it drastically increases data transmission rate to the blanker. A larger pixel size reduces the loading of the data path but may cause truncation error from the original fine-grid OASIS file. Therefore, an appropriate pixel size is chosen and dithering of pixels is introduced to achieve sub-nm electron proximity correction (EPC) accuracy at reasonable data rate. Besides, dithering is also required for beam-to-beam position and dose corrections.

In this paper, the dithering approaches and their impacts to CD and overlay are studied. A Triple Gaussian model to describe the electron forward scattering and backscattering effect in photo resist for proximity correction has been built. By convoluting the kernel to the rasterized layout, we study the impact of CD and overlay error at different pixel sizes. Several dithering algorithms were tested and compared. The writing error enhancement factor (WEEF) and normalized image log slope (NILS) are used to characterize the induced CD error and line width roughness (LWR). Experiments with the 110-beam MAPPER prototype tool were performed to verify the simulation results. To clarify the influence of the blanking performance to CD, a designed experiment at variant blanking speeds was performed. From this study, we built the CD budget table for a MEBML2 tool.

8323-97, Poster Session

Hardware implementation of Corner2 lossless compression algorithm for maskless lithography systems

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Dai and Zakhor (2006) introduced a data delivery system (Fig. 1) with a lossless image compression component for maskless lithography systems. By storing the compressed layout image in the processor board memory and decoding it on-the-fly at the decoder circuit which is connected to the lithography writer with on-chip wiring, they were able to significantly increase the data throughput.

Based on Dai and Zakhor's work, Yang and Savari (2011) introduced a compression algorithm Corner2 that has significantly higher compression ratio and faster encoding / decoding speed while requiring less decoder memory than Block C4 which was proposed by Liu, Dai, Zakhor, and Nikolic (2008). The Corner2 compression algorithm obtained these performance gains by utilizing pattern replacement and a corner (or vertex) based representation of the layout polygons. By replacing frequent layout patterns, Corner2 was able to efficiently handle repeated cell structures.

The Corner2 decoder consists of two parts: an entropy decoder and an inverse transformation as in Fig. 2. The entropy decoder reproduces ternary transformed layout images from the compressed bit streams. The ternary images are sparse and dominated by "0"s which contributes to the high compression ratio of Corner2 algorithm. "2"s are used to indicate the beginning of a frequent pattern while "1"s are used to indicate transitional corners.

Using a row of the ternary transformed image, the inverse transformation produces the decompressed layout image of the corresponding row. The inverse transformation circuit has the architecture shown in Fig. 3. It consists of four parts - corner transformation, frequent pattern reconstruction, row buffer, and frequent pattern dictionary. The corner transformation block reconstructs the polygons from the transitional corners ("1"s) while the frequent pattern reconstruction block reconstructs the corresponding pattern once a pattern has started with symbol "2". The row buffer is used to store the previous row status to decode corner transformation and frequent pattern reconstruction. Finally, frequent patterns are stored in the frequent pattern dictionary and are accessed by the frequent pattern reconstruction block. As mentioned in Yang and Savari (2011), this entire decoding process is applied in a row-by-row fashion making this entire process decoder memory efficient.

In this paper, we implemented the Corner2 decoder in hardware (an FPGA implementation). Since the blocks of the Corner2 algorithm were implemented to simulate decoder circuits implemented in hardware, we were able to design the decoder circuits without major modifications. We used Impulse CoDeveloper to generate Hardware Description Language files from the Corner2 source code and used Xilinx CAD tools to design the FPGA circuit from the HDL files.

By testing the FPGA implementation, we show that the Corner2 algorithm has many advantages over Block C4. It has a better compression ratio and a higher decoding throughput, while requiring less decoder memory. We expect its ASIC design would work fast enough to improve the data delivery throughput and would be small enough to be suitable as an add-on to the lithography writer.

8323-99, Poster Session

Scalable simulations for directed self-assembly patterning with the use of GPU parallel computing

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Semiconductor companies have recently investigated directed self-assembly (DSA) patterning on 300 mm wafers as a possible alternative for future lithographic process. One of the critical specs for DSA patterning is defects generated through annealing process or by roughness of pre-patterned surface and topology. Due to their high sensitivity to the process and wafer conditions, however, characterization of those defects still remain challenging.

DSA simulations can be a powerful tool to predict the formation of the DSA defects. In this work, we take advantage of graphics-processing-unit (GPU) parallel computing for large-scale DSA simulations. As demonstrated in many other applications, we use a consumer graphics card to access its hundreds of processing units for parallel computing. In our test case, we adopt a coarse-grained model of block copolymers and perform Monte Carlo (MC) simulations. By partitioning the simulation system into non-interacting domains, we are able to run multiple MC trial moves effectively in parallel. Our results show a significant improvement in computational performance. We also apply a similar approach to investigate the formation of DSA defects on a large-area, irregularly pre-patterned surface.

8323-100, Poster Session

Modeling line-edge roughness in lamellar block copolymer systems

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Block copolymers offer an appealing alternative to current lithographic techniques with regard to fabrication of the next generation microprocessors. However, if copolymers are to be useful on an industrial manufacturing scale, they must meet or exceed lithography specifications for placement and line edge roughness (LER) of resist features. Here we discuss a field theoretic approach to modeling the LER in the lamellar phase of a strongly segregated block copolymer system. Our model is based on the Leibler-Ohta-Kawasaki free energy functional, which takes the Flory-Huggins parameter and index of polymerization as inputs. We consider a domain with a finite number of phase separated microdomains; at the system boundary, we apply conditions akin to a chemical pinning field. Using a path integral formalism, we determine how fluctuations of the microdomain boundaries depend on distance from the system boundary, number of microdomains, the Flory-Huggins parameter, and index of polymerization.

8323-101, Poster Session

Patterning via directed self-assembly of polystyrene-block-polyacid copolymers for sub-20nm pitch patterning

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Directed self-assembly (DSA) of block copolymers is a promising technology for production of sub-30nm pitch structures. Significant recent work has focused on demonstration of the ability to produce large areas of regular grating structures with low defectivity from self-assembly of polystyrene-b-poly(methyl methacrylate) block copolymers (PS-b-PMMA) using pitch subdivision methods based on guiding patterns produced via optical exposure tools. While these recent results are promising and have shown the ability to print pitches approaching 20nm using DSA, the ability to advance to even smaller pitches is limited by the relatively low χ value of the widely studied PS-b-PMMA system. In order to provide a path forward for extension of DSA to very small pitches, block copolymers with larger χ values are needed along with suitable neutral underlayers, annealing methods, and methods for selective

removal of one of the blocks to produce the desired relief patterns. In this work, block copolymers based on polystyrene-block-polyacids were proposed and investigated as a potential candidate material for enabling sub-20 nm pitch patterning via DSA. The strong hydrogen bonding between polyacid block monomers in such materials results in very large χ values and significantly increases the thermodynamic driving force for block phase separation. The presence of such strong hydrogen bonding sites in the polymers also provides a convenient and relatively specific interaction with which to design materials to act as guiding layers. PS-b-PAA (polystyrene-b-polyacrylic acid) and PS-b-PMAA (polystyrene-b-polymethacrylic acid) polymers were synthesized by ATRP (atom transfer radical polymerization) with controlled molecular weights and low polydispersities. Both thermal and solvent annealing methods were studied as potential methods for annealing such materials and driving the phase separation based self-assembly. It will be shown that such materials can be used to successfully form perpendicular lamellar or cylindrical morphologies over a range of length scales, well below what is accessible with PS-b-PMMA. The scaling of pattern pitch with PS-b-PAA and PS-b-PMAA molecular weight will be shown and discussed. The development of and composition of neutral substrate layers for these PS-b-PAA and PS-b-PMAA block copolymers will be discussed. Both conventional plasma etching techniques for selective removal of the polyacid blocks and novel methods for forming in-situ surface etch barriers followed by plasma etching will be demonstrated and discussed for achieving relief patterns with sub-20nm pitches.

8323-102, Poster Session

Sub-wavelength holographic lithography: the possibilities and advantages

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Authors analyze results demonstrating real possibility to use method and technology of sub-wave length holographic lithography (SWHL) for the purpose of IC production.

Authors theoretically prove that it is possible to use methods of digital holography to synthesize a sub-wave length holographic mask (SWHM) to create an aerial image of real IC topology layer with sub-wave length resolution, with similar (or better) quality of the image compared to images produced by traditional projection photolithography (PPML) using the same resolution enhancement methods and the same source of coherent radiation.

The high level of quality is achieved by combining conventional PPML image optimization routine (for example OPC) with specially developed methods of SWHM digital synthesis for considerable number ($\approx 10^{11}$) of topological elements.

It is proved (by computer simulations on modern computational complexes used for parallel calculation) that it is possible to produce SWHM enabling to create an aerial image of real IC topology layer by using up-to-date e-beam lithographers.

Specially designed parallel calculation algorithms provides SWHM synthesis for real IC layer with $\approx 10^{11}$ topological elements by during ≈ 10 hours on computational complex with max speed 100 Teraflops.

Authors analyze computer simulation and experiment results shows advantages of SWHL compared to traditional PPML for the wide range of parameters, including extremely low sensitivity to mask local defects - up to $\approx 10^{10}$ times higher density of local defects is allowed compared to traditional PPML masks.

Authors show applicability of well-known approaches to resolution enhancement when using SWHM - such as immersion, multiple patterning and phase shift.

8323-103, Poster Session

Fabrication of polymer microneedle array using bulk lithography

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This paper presents the method of fabrication of controlled microneedle array using single scan of laser beam over the unconstraint depth photopolymer resin (pattern making) and subsequent micromolding of polydimethylsiloxane (PDMS) and further casting of photoreactive eShell 200. Pattern of photopolymerized microneedle array is achieved using newly developed microfabrication process termed as 'Bulk lithography'. In this process, very first optical system (mirror lens assembly) is steered to the desired spot, followed by subsequent controlled laser irradiation on unconstraint photopolymer resin bath. Thus, pattern of microneedle array is fabricated by navigating the optical system over entire surface of resin bath. Experimental results reveal that cured depth (length of the microneedle) is dependent on energy exposure. Further, it is also observed that the aspect ratio (in particular base of the microneedle) is dependent on location of laser focal plane with respect to substrate resin interface. Thus, control on size of the microneedle is achieved by tuning these two process conditions. Patterned microneedle array is then surrounded by container which is then filled with solution of polydimethylsiloxane (PDMS). Further, the complete sample is then degassed and thermally cured for cross linking of PDMS. The PDMS bulk is then removed with the help of translation stages to obtained negative mold of microneedle array. Further next, eShell 200 polymer is placed over obtained mold. The mold is then exposed to ultraviolet light emissions for curing of eShell 200. After curing, finally the microneedle array of eshell 200 is released manually from the mold.

8323-41, Session 10

Paradigm shift in nanoimprint lithography

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Photomask has been an important role in lithography for long time. However, recent lithography technology trend makes photomask industry less attractive. The market size of photomask is now less than 1% of total semiconductor market, and seems to be shrinking in future because of less semiconductor players. Compared with photomask, EDA tool market stay on about 2% of total semiconductor market with the strong needs of resolution enhancement technology, such as OPC, ILT, and SMO. The complexity of mask data has been increasing with those technologies, and mask writing time skyrocketed over some days. However the requirements of turn-around-time and cost reduction on photomask are increasing. Moreover, lithography cost should be shared with expensive sophisticated scanner tools and massively increasing process tools, such as Etch and CVD along with multiple patterning application. On the other hand, nanoimprint lithography, one of the next generation lithography candidates, may make the paradigm shift against this situation. This technology needs almost no additional mask data preparation from design, simpler exposure system, and just single patterning process. Additionally, photomask, or template, will control most of pattern qualities, such as resolution, CDs , overlay, and defectivity. As a result, the value of photomask will be rated reasonably high again. In this paper, the historical trend of value shift in lithography, and the hopeful prospect of next generation lithographies will be discussed.

8323-42, Session 10

Cleaning-induced imprint template erosion

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In the UV-imprint process, a silica template with the desired pattern is in direct contact with the resist when UV-irradiation is applied to cure the resist. Imprint process failure can cause the cross-linked resist to stick to the template. The resulting contaminants are resistant to solvent attack, thus, their removal requires the use of cleaning processes with aggressive oxidants.

In this paper we report on the detection of template CD change as a result of template cleaning using spectroscopic ellipsometry optical critical dimension (SE-OCD) measurements. SE spectra of the 72.6nm pitch line-and-space pattern on a silica template were analyzed to extract pattern profile information with good sensitivity. Previously, changes in template features are difficult to characterize using conventional techniques such as cross-sectional SEM or AFM, due to their limited sensitivity, small sampling size, and pattern topography effects.

Using these techniques, we investigated the erosion of the fused silica imprint template in the traditional acid-based SPM (H2SO4+H2O2) cleaning. Our study confirmed the erosion of silica template features at a rate of ~ 0.1 nm per cycle as a result of the SPM cleaning. Although the rate of silica pattern erosion in SPM is slow, the cumulated effects over the lifetime of an imprint template can be significant. Therefore, to establish a reliable manufacturing process based on nanoimprint lithography, better template cleaning processes that are less damaging to template features need to be developed.

Currently, such a process is being tested on HamaTech's MaskTrack TeraPure tool using an acid-free solution. Preliminary results will also be presented and discussed in this paper.

8323-43, Session 10

Nanoimprint template replication from directed self-assembled block copolymer patterns for bit patterned media at 1Tdot/in^2

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Bit patterned media technology relies on high quality nanoimprint templates at densities in excess of 1Tdot/in2 to achieve the high-throughput, low-cost fabrication necessary for disk drive manufacturing. Fabrication of templates at feature densities ahead of those of the conventional semiconductor roadmap represents a significant departure from conventional lithography, requiring the use of alternative lithographic techniques such as directed assembly of block copolymer films. However, in order to comply with the high throughput, yield, repeatability and lifetime specifications set for bit patterned media, it is necessary to feed the master template into a replication scheme that clones the original master pattern into a large number of identical working templates for magnetic media patterning using nanoimprint lithography.

Working templates can be either pillar-tone or hole-tone depending on the choice of transfer materials and transfer techniques such as direct etch or tone reversal. Both processes present advantages and unique sets of challenges. In this work, we demonstrate template replication schemes to fabricate pillar-tone and hole-tone nanoimprint working templates. In both cases, a pillar-tone Si master template is first fabricated using e-beam directed block copolymer assembly. By combining nanoimprint lithography with other nanofabrication techniques, we replicate the master templates into both hole-tone and pillar-tone quartz working templates. With a hole-tone working template, bit patterns in media can be defined using nanoimprint lithography and direct etch, while with a pillar-tone counterpart which may be preferred at higher pattern density, a tone reversal process is needed following the nanoimprinting step. We demonstrate template replication of concentric, full-track bands up to 10mm wide with feature density at 1Tdot/in2 for bit patterned media. We will discuss pattern fidelity and nanofabrication challenges, such as defect density, feature size uniformity and placement accuracy for both template replication methods and put them in perspective considering the specifications needed to support bit patterned media with low bit error rates.

8323-44, Session 10

Fabrication of templates with rectangular bits on circular tracks by combining directed block copolymer self-assembly and nanoimprint lithography

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Directed self-assembly of block copolymer thin films has been demonstrated as one of the most promising methods to achieve high density patterns with a high perfection of size uniformity and placement accuracy. The combination of block copolymer lithography and nano-imprint technique has being developed for the application of magnetic bit patterned media (BPM) at densities beyond 1Tdot/in2. In BPM applications, most studies have been focused on hexagonal close packed (hcp) array of dots, since it can be readily obtained by directed self-assembly of block copolymers with sphere or perpendicularly oriented cylinder morphology and maximizes the areal feature density. However, high bit aspect ratio (BAR) rectangular bits, which are elongated in the cross-track direction and narrow in the down-track direction, may be more favorable to the gradient profile of the writing head. The fabrication of high BAR rectangular bits arranged in quasi-rectangular lattices has been demonstrated in our group by using lamellae-forming block copolymer. Here, we combine block copolymer lithography with nano-imprint technique to generate high BAR templates. Circumferential and radial lines are created separately by directed self-assembly of lamellae-forming block copolymer on chemical patterns prepared by rotary e-beam lithography. In this presentation, we are focusing on generating prepatterns using rotary e-beam lithography and the following directed self-assembly of block copolymer films.

Nano-imprint master templates with precision in size uniformity and placement are required to meet the specification for low bit error rate magnetic BPM. A rotary stage e-beam lithography tool is best suited to define the pre-patterns needed for the circular geometry of magnetic recording disks. Thus we are using a rotary e-beam tool to expose both circumferential lines and radial lines with periodicities commensurate to the nature period of certain lamellae-forming poly (styrene-b-methyl methacrylate) (PS-b-PMMA). Circumferential line patterns with preferred line width and edge smoothness were obtained by varying beam dose. To obtain well defined radial lines on a continuously rotating stage, various beam deflection and blanking strategies were investigated. The resist patterns were transferred to the underlying imaging layer by short oxygen reactive ion etching followed by resist stripping. Line patterns were formed by directed self-assembly of PS-b-PMMA on chemical patterns on two separated templates, one with circumferential lines to define concentric tracks and a second template where the lamellae block copolymer is used to form radial lines at constant angular pitch. The patterns are subsequently transferred to the underlying templates. Using nano-imprint lithography, we combine the radial and circumferential templates into a final working template with rectangular bits on circular track.

8323-45, Session 10

Nanoimprint templates of 6nm half-pitch lines fabricated by helium ion-beam lithography

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Driven by both fundamental scientific research and device applications, particularly in order to keep the ride of the Moore's Law, single-digit nanolithography technologies have attracted significant interests recently. With the progress in study of the resist development mechanisms, electron beam lithography has set a resolution record of 4.5 nm half-pitch

lines in HSQ resist. However, electron beam based lithography exhibits strong proximity effect that limits patterning of high-density sub-10 nm features over a large area.

The recently introduced helium ion microscope provides a unique tool for nanolithography applications. Helium ion beam lithography has a number of advantages including small beam spot size, higher sensitivity and very low proximity effect, which combine to offer the capability of single-digit nanopatterning of dense structures over a large area. Meanwhile, the larger mass of helium ions compared with electrons makes it also a good tool for direct milling sub-10 nm features on various materials.

In this work, we demonstrated sub-10 nm patterning using a Carl Zeiss Orion Plus helium ion microscope equipped with a Raith ELPHY pattern generator. Specifically, we patterned sub-6 nm half-pitch gratings on 15 nm thick HSQ resist and directly milled 10 nm wide trenches with a 30 nm pitch on freestanding gold film. These work convincingly demonstrate the superior capability of helium ion beam lithography in patterning sub-10 nm features. More experiments are still in progress and we expect better results can be reported soon.

One well-known drawback of helium ion beam lithography, as well as other scanning beam based lithography techniques such as e-beam lithography, is that the slow writing speed significantly limits their applications in large volume production of nanodevices. Moreover, helium beam may introduce undesired damage to certain substrates, making it unsuitable for direct fabrication of devices with some functional materials.

In our work, we are also exploring combining nanoimprint lithography with helium ion beam lithography to reliably duplicate sub-10 nm features over large areas at a relatively low cost and high throughput. We first fabricate nanoimprint templates carrying sub-10 nm features by helium ion beam lithography, through both directly milling a layer of hard mold materials and exposing a HSQ resist over a substrate. Then, the fabricated molds are coated with a fluorine-based mold release agent. Finally, the nanoimprint templates are pressed into a UV-curable polymer and then UV exposure is used to cross-link the polymer before separating the mold from the substrate.

In summary, we demonstrate the superior performance of scanning helium ion beam lithography for patterning sub-10 nm features through both HSQ resist development and hard material direct milling. We also demonstrate a viable approach of reproducing these sub-10 nm features on functional materials by nanoimprint. Combination of helium ion beam lithography and nanoimprint provides a promising path towards low-cost and large-volume fabrication of nanodevices at single-digit nanometer scale.

8323-46, Session 10

Deformations of soft imprint templates in the nanoimprint lithography

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Nanoimprint lithography is an attractive technology for the fabrication of diffraction unlimited patterns due to its low cost and high throughput and has the potential to be used in many areas such like the CMOS technology, the storage technology, the display technology and the biotechnology. The imprint template is the basis in the Nanoimprint lithography. Regarding their materials, they can be differentiated mainly in two groups, the hard imprint template of quartz, silicon, metal etc. and the soft imprint template of polymer like PDMS. In comparing with the hard imprint templates, the soft imprint templates have many advantages. They cost less. Most of them are transparent, which is advantageous for the optical adjustment and the UV-exposure. They are flexible, so that they can achieve a complete contact with the substrate, which is difficult for the hard imprint templates especially over a large imprint area. Unfortunately the soft imprint templates trend to deformation when imprint forces are added. This deformation occurs both in the macro aspect (unevenness of the imprint resist layer

through the whole imprint area) and in the micro aspect (deformation of single structure). These deformations will be transferred directly to the imprint resist after its curing and thus influence the imprint results. An understanding of these deformation behaviors in dependence of the template geometry and the imprint process parameters is very important for the process development. In this work the deformation behaviors of the polymer soft imprint template was through FEM method analyzed and experimentally investigated.

8323-47, Session 11

Airbrushing, ink jet printing, replica molding, and microcontact printing of chitin nanofibers with a "chitin nanofiber ink"

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The ability to easily manufacture and manipulate biomaterials is key to the development of biocompatible medical devices. Harsh fabrication techniques derived from the semiconductor industry are often incompatible with biomaterials. Furthermore, these techniques do not take advantage of the natural self-assembly properties that can be exploited to create nanostructures. Chitin has attracted increased attention in biocompatible device fabrication. Chitin has excellent thermal stability, mechanical strength, biodegradability, and anti-microbial properties. However, chitin water insolubility has limited chitin nanofibers to electro spinning with difficult nano- and microstructure fabrication. Here, we present a facile approach to chitin nano- and microstructures composed of self-assembled nanofibers. We have developed a hexafluoro 2-propanol (HFIP) based "chitin nanofiber ink", which self-assembles into ultrafine (3nm) nanofibers upon drying. The chitin nanofiber ink is exploited to fabricate 2-D and 3-D structures via airbrushing, ink jet printing, replica molding, and microcontact printing. Examples include circles, squares, pillars, and optical gratings with features ranging from sub-40 nm to several microns. These strategies were used to produce proof-of-concept chitin biophotonic structures.

8323-48, Session 11

Zone plate focused soft x-ray lithography for fabrication of nanofluidic devices

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The current generation of soft X-ray scanning transmission X-ray microscopes (STXM) routinely focus monochromatic soft X-rays into sub-30 nm spots (Rayleigh criterion) using Fresnel zone plates. We use this fine X-ray beam to pattern resist materials in a direct write manner, analogous to lithography with a focused electron or ion beam[1]. The photon energy tunability of the STXM (80 - 2000 eV) can be exploited for chemically selective patterning of multilayer structures composed of two or more chemically distinct resists. By tuning the patterning energy to specific inner shell excitation resonances, one material can be selectively damaged over others [2,3]. We have used this unique capability to create sub-100 nm diameter buried nanofluidic channels. The optimization of this multi-level lithography, as well as challenges of integrating patterned nano-channels into conventional microfluidic devices will be presented. Other unique lithographic related applications of zone plate focused soft X-rays will also be discussed.

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8323-49, Session 11

New lithographically patterned templates for positioning DNA nanostructures

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One of the current goals of nanotechnology is to couple self-assembly of molecular nanostructures with conventional micro-fabrication techniques to create devices having the addressability and registration required for integration into functional nanoelectronic devices. DNA origami nanostructures1 are excellent candidates for this type of directed assembly. They can be prepared with arbitrary shapes and dimensions on the order of 100 nm and can be functionalized so that they can be as templates for the assembly of even smaller components.

Previously we described methods for positioning individual origami structures on lithographically patterned surfaces employing either patterned hydrophobic films or etched hydrophilic surfaces2. In this contribution we describe a new fabrication process which combines both approaches and incorporates topography into the patterned thin film templates previously described. We discuss the binding selectivity and placement accuracy for origami structures on these new templates that have been patterned with either e-beam or optical lithography followed by pattern transfer into the SiO2 substrate (Figure).

We will also describe our attempts at developing an anisotropic etch process which would allow the transfer of the fine structures in the origami shape to a thin film for use as a hard mask for subsequent pattern transfer steps.

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8323-50, Session 11

Alignment method in plasmonic lithography with a contact optical scanning probe at resonant condition

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In plasmonic nanolithography with a contact scanning probe, alignment process have not yet been well-developed. On this circumstance, we will approach the alignment issue with optical scanning probe using the resonant behavior of the bowtie shaped plasmonic nano aperture. Since both alignment and lithography are realized in the same probe module, aligment aims to provide the position of the probe relative to the fiducial point within reasonable accuracy. For this process, we set the ficucial point with simple shaped mark and find it through imaging technique using bowtie shaped plasmonic nano aperture sensitive to the change of surrounding environment. So, when the bowtie aperture scans over the certain structure that consists of more than two kinds of refractive index, its resonant condition is shifted by the difference of the refractive index, which affects the intensity of the reflection and it will be used to form the image of the mark for finding the reference point. The calculated result of FDTD(finite difference time domain) method and experimental image will be given to show the feasibility. Bowtie aperture in the Aluminum metal film coated on the probe was designed by adjusting the geometry at resonant condition of the specific wavelength and fabricated by Focused ion beam(FIB). The mark of air on the quartz substrate is prepared by direct writing lithography and Reactive ion etching (RIE). Furthermore, we expect that one probe could allow all functions of lithography, imaging and alignment to be achieved by altering the resonant wavelength.

8323-51, Session 11

Progress in scanning proximal probe nanolithography on calixarene

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The ability to pattern at single nanometer scale (SNL) opens entirely new horizons in nanodevice fabrication beyond existing limits. This research aims to tackle this critical challenge by employing scanning proximal probe lithography (SPPL) in conjunction with small molecule resist materials. We demonstrate within this report the utilization of an advanced hybrid set-up for maskless nanoscale lithography based on patterning of ultra-thin spin-coated molecular resist materials. The high, nonuniform electric field created between biased nanoprobe and sample leads to a localized field emission current and in-situ removal / extraction of resist material.

Here we demonstrate positive-tone lithography in ambient conditions on calixarene-based molecular resist materials, especially on calix[4] resorcinarene. As an extension to previously reported results we utilize a modified AFM-system as "Multi-Nano-Tool" for both: (1) Writing of nanostructures in non-contact applying a spatially extreme confined electric field in combination with the regulation of the localized Fowler-Nordheim electron emission between tip and sample, and; (2) Subsequent imaging and analysis of the generated nanostructures within AFM AC-mode using own small, high frequency (1st mode between 2 and 3 MHz) cantilevers with extreme sharp tips. By employing this "writing and reading" tool kit on molecular resist materials the full ultra-high resolution potential of calixarene in combination with excellent overlay alignment accuracy can be exploited. In marked contrast to electron beam lithography and EUV lithography the calixarene derivate reveals a positive-tone self-developing behavior. The results indicate in comparison to resist exposure mechanisms significant higher resolution capabilities of sub-10nm and the sidewalls are practically vertical.

8323-52, Session 12

Roll-to-roll manufacturing of electronic devices

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Roll-to-Roll (R2R) production of thin film based electronic devices (e.g. solar cells, active matrix TFT backplanes & touch screens) combine the advantages of the use of inexpensive, lightweight & flexible substrates with high throughput production. Significant cost reduction opportunities can also be found in terms of processing tool capital cost, utilized substrate area and process gas flow when compared with batch processing systems. Nevertheless, material handling, device patterning and yield issues have limited widespread utilization of R2R manufacturing within the electronics industry.

Recently, significant advances have been made in device patterning enabling the mass production of a variety of flexible electronic devices. These techniques are now so advanced that feature sizes of less than 40 nm can be produced on thin film layer stacks deposited on 50 µm thick polymeric substrates. Significant challenges also exist in terms of the deposition technologies used in R2R manufacture of these devices. Unlike traditional semiconductor or display based cluster tool platforms, R2R systems require to process substrates in a continuous fashion with rolls up to several kilometers in length. Depending upon the process itself, this imposes a limitation in terms of the mean time before cleaning (MTBC) and in some cases the particle management strategy. This has lead to the implementation of "sputter up" configurations in PVD tool designs and vertical web handling in the deposition zones in PECVD tool designs.

Applied Materials has developed a variety of different web handling & coating technologies/platforms to enable high volume R2R manufacture of thin film based flexible photovoltaic, silicon based TFT active matrix backplanes and touch screen devices. The work presented in this paper therefore describes the principal challenges inherent to R2R device

manufacture such as choice of substrate, thermal budget, layer stack stress, patterning, defects, yield & inline process monitoring and control in addition to the strategies used to mitigate these challenges.

8323-53, Session 12

Continuous large area nanoscale patterning using cylindrical phase masks

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There has been increasing demand for large-area, low-cost nanofabrication techniques for many applications. These applications include nanostructured self-cleaning surfaces, nanopatterned light-trapping layers and nanostructured absorbers for photovoltaic devices, wire-grid polarizers for display devices, and optical metamaterials, to name an important few. Current available nanopatterning and fabrication techniques are still unable to meet the required performance, fabrication speed, and cost criteria for such large-area patterning applications. We report the development of a near-field optical nanolithography method by using a roll-type phase-shift mask, which combines some of the best features features in photolithography, soft lithography, and continuous roll to roll/plate patterning technologies Sub-wavelength resolution is achieved using near-field exposure of photoresist through a cylindrical phase-mask, allowing a dynamic and high throughput continuous patterning. We report the first results achieved by a recently built prototype tool and cylindrical phase-shift mask, which were designed to pattern 30-cm-wide substrate areas.

8323-54, Session 12

Sub-100nm pattern formation by roll-to-roll nanoimprint lithography

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Technologies for pattern fabrication on a flexible substrate are having developed for various flexible devices.

We think a patterning technique of the smaller pattern with the size of sub-100 nm will be needed, and a roll-to-roll (R2R) patterning is expected to fabricate the large-area devices with a large volume and extremely low-cost fabrication.

We have already transferred the 100 nm patterns from a replica mold made of a nickel onto an ultraviolet (UV) curable resin on a polyethylene terephthalate (PET) film substrate with the thickness by the R2R-nanoimprint lithography (R2R-NIL).

Now, we are trying to transfer the sub-100 nm patterns, or more specifically, sub-30 nm patterns, with two types of replica molds made of a nickel and a resin which were fabricated from Si wafers with structures with the width of sub-100 nm, and which have the thickness of about 200 micrometer, respectively.

We are estimating conditions for R2R-NIL process, such as a film substrate feeding speed, a mold pressure to the substrate, strength of the UV light, a resin material, and the size of transferring patterns.

And the size of transferred pattern and its defectivity on the film substrate will be evaluated for the process parameters and materials.

In this paper, we will show our status of development of the process for R2R-NIL and possibility for patterning of sub-100 nm with R2R-NIL.

8323-55, Session 12

Planarization coating for polyimide substrates used in roll-to-roll fabrication of active matrix backplanes for flexible displays

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The surface quality of the substrate is essential to reduce pixel defects to an acceptable level during the fabrication of active matrix backplanes for flexible displays by roll-to-roll processes. Standard polyimide substrates have high density of "bumps" from fillers and belt marks and other defects from dust and surface scratching. It is believed that some of these defects could be the source of shunts in our dielectric. Good quality dielectrics are important for working roll-to-roll fabricated active matrix backplanes. The gate dielectric must prevent shorts between the source/drain and the gate in the transistors, resist shorts in the hold capacitor, and in the case of active matrix backplanes fabricated by self-align imprint lithography (SAIL), stop shorts in the data/gate line crossovers. Otherwise the data and gate address lines will become shorted creating line defects or pixel defects where individual pixels no longer function. In this presentation, we will talk about the development of a proprietary UV curable planarization material that can be coated by roll-to-roll processes. This material was engineered to have low shrinkage, excellent adhesion to polyimide, high dry etch resistance, and great chemical and thermal stability. Results from the deposition of the amorphous silicon stack by PECVD on the planarized polyimide and compatibility with roll-to-roll imprinting, and wet and dry etching processes to fabricate active matrix backplanes will also be presented. The effect of the planarization on defects in the stack, shunts in the dielectric and curvature of the finished 1/8 VGA array will also be included.

8323-56, Session 12

Roll-to-roll nanopatterning using jet and flash imprint lithography

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The ability to pattern materials at the nanoscale can enable a variety of applications ranging from high density data storage, displays, photonic devices and CMOS integrated circuits to emerging applications in the biomedical and energy sectors. The cost of manufacturing is typically driven by speed (or throughput), tool complexity, cost of consumables (materials used, mold or master cost, etc.), substrate cost, and the downstream processing required (annealing, deposition, etching, etc.). In order to achieve low cost nanopatterning, it is imperative to move towards high speed imprinting, less complex tools, near zero waste of consumables and low cost substrates.

The integration of these key requirements leads to a novel process concept: Ink Jet based Roll-to-Roll Nanopatterning (i-R2R Nano). Extremely large area R2R manufacturing on flexible substrates is ubiquitous for applications such as paper and plastic processing. It combines the benefits of high speed (>100 ft/min) and inexpensive substrates to deliver a commodity product at low cost. The challenge is to extend this approach to the realm of nanopatterning and realize similar benefits. To address this challenge, we have introduced an i-R2R Nano technology demonstrator product, the LithoFlex 100.

This paper will review tool performance relative to the tool specifications and will also present results on devices patterned with the system. As an

example, an aluminum based wire grid polarizer (WGP) with a half pitch of 50nm was fabricated. Transmission and extinction ratio for the device were, 80% and 4500, respectively. Transmissions as high as 87% have been obtained.

8323-57, Session 13

Optimizing materials and processes for directed self-assembly applications

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Directed self-assembly (DSA) of block copolymers is a promising technology for advanced semiconductor patterning at future technology nodes. Great strides have been made recently to transition DSA from lab to fab, but significant hurdles remain for large scale commercial implementation. Many features, including block copolymer composition, molecular weight, polydispersity, formulation, and commensurality with directing prepatterns, must be controlled to achieve the stringent targets for defects, LER/LWR, CDU, etc.

This talk will provide an introduction to Dow's research capabilities in block copolymers and discuss DSA from the viewpoint of a resist supplier. Focus will be placed on understanding and optimizing factors critical to success using a combined theoretical and experimental approach. Examples of modeling, including Self-Consistent Field Theory (SCFT) and Strong Segregation Theory (SST), will be presented to guide selection of materials and optimize patterning. Synthetic capabilities will also be highlighted with particular emphasis on BCP purity and development of new materials.

8323-58, Session 13

Directed self-assembly of laterally confined lamellae-forming diblock copolymers: polydispersity and substrate interaction effects

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Theoretical methods are critical to our understanding of defect formation in block copolymer lithography processes. In our previous work, we have applied self-consistent field theory (SCFT) to study the energetics of dislocation and disclination defects prevalent in graphoepitaxy of "standing up" lamellae, using the saddle point field configurations corresponding to defective and defect-free solutions to predict the free energy cost of forming a defect under specified conditions. The results demonstrated the existence of a "commensurability width", where the channel dimensions accommodate the natural domain period and the defect energy is greatest, as well as the response of defects to strain about this width. In an effort to further refine our investigation, we sought to address two key assumptions made in our previous work: the assumption of a monodisperse melt, and a bottom substrate neutral to both polymer blocks.

Variations in molecular weight distributions are known to alter ordered phases of block copolymer systems in the bulk. Broadening of the molecular weight distribution will result in larger domains and shifting of phase boundaries, because the presence of longer chains alleviates the stretching contribution to the system's free energy. We employed the SCFT framework using a model of a binary blend of AB copolymers + wall system to examine the degree to which defect energies are influenced by deviations from the monodisperse limit. The results of our study show that much like the bulk system, the natural domain spacing,

and consequently the commensurate channel width, in the confined system is dependent on polydispersity index (PDI). Defect energies of the binary blend system at commensurate widths were shown to decrease with increased PDI, and response to strain around the commensurate widths also varied with a change in PDI, although in all cases the changes were modest for PDIs less than about 1.3.

Lateral order is most effectively imparted on confined diblock copolymer systems by uniform, selective side walls and a substrate perfectly neutral to both polymer blocks. The 2D theory used in our previous study assumes slight deviations from this ideal case will not result in significantly more favorable conditions for defect formation. In order to test the validity of this assumption, we have performed the full 3D calculations with substrate-polymer interaction strengths ranging from selective for A to selective for B. The results demonstrate to what extent polymer-substrate selectivity must be controlled.

8323-59, Session 13

Directed self-assembly of PS-b-PDLA for patterning of sub-10nm half-pitch structures using EUV resist templates

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Directed self assembly (DSA) of block copolymers has drawn great interest from microelectronic manufacturers due to its ability to form highly ordered, sub-lithography resolution structures using patterned templates. Grapho-epitaxy is a widely used technique in DSA research, where lithography patterned topography templates are used to guide the alignment and arrangement of block copolymers. In graphoepitaxy, many groups reported the use of negative tone resists, or crosslinked positive tone resist patterns as templates to avoid undesired solvent interactions of materials and the subsequent high temperature processing required for phase separation of PS-b-PMMA.

We studied the DSA of a lamella-forming block copolymer system, polystyrene-b-poly(D,L Lactide), where domain sizes as small as ~8 nm (lamella spacing, L0 =16 nm) have been measured by Small Angle X-ray Scattering (SAXS) and Scanning Electron Microscopy (SEM). We believe such block copolymers can be viable candidates for sub 10 nm half pitch patterning due to the strong polymer-polymer interaction parameter (χ), high etch selectivity, and low temperature requird ofr annealing. In this work, we report the pattern multiplication and selective degradation of PS-b-PDLA on Electron Beam Lithography (EBL) and Extreme Ultraviolet Lithography (EUVL) patterned EUV resist templates without the need for resist freezing. The developed processes are directly compatible with EUVL and other lithography processes as the annealing temperature can be as low as 90 °C to achieve highly ordered phase separation. The chemistry and properties of modified lactide block copolymers will also be discussed.

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8324-01, Session 1

Can we get 3D CD metrology right?

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Optical lithography is now, and in the future, will be printing photoresist features that are much smaller than the wavelength of the light used, and therefore it is indispensable to use complex lithography and optical proximity correction methods. This includes modeling and compensation for various errors in the lithography process down to sub-nanometer, essentially atomic levels. This process also relies on sophisticated and complex simulations and on accurate and highly repeatable dimensional metrology. The necessary dimensional metrology is well beyond the traditional one-dimensional linewidth and the two-dimensional contour measurements. The metrology must include highly precise three-dimensional measurements of the size, the shape and position of structures. Successful 3D metrology incorporates accurate and highly repeatable measurements on sets and individual circuit structures, for which the critical dimension measurement scanning electron microscope (CD-SEM) is the key metrology tool.

Unfortunately, there are many shortcomings of the current CD-SEMs that make it impossible to achieve excellent accuracy and repeatability, especially in 3D and at high magnifications. Today most SEMs acquire images in a non-optimal way and use algorithms that are arbitrary (with some level of empirical error correction). The results are not based on fundamental understanding of the physics and metrology, and therefore generally carry larger than necessary measurement errors or uncertainties.

NIST is developing SEM-based measurement methods that allow for highly accurate and precise two-dimensional measurements. Advanced image and data acquisition methods and modeled and measured library-based methods recently introduced by NIST offer further advantages, as they significantly improve the precision of the measurements and add a possibility for accuracy, as well. The researchers at NIST are also working on 3D SEM metrology to fulfill current and future requirements of the ITRS Roadmap and deliver reliable, highly repeatable and accurate metrology.

This talk will present the results of new SEM-based measurement methods, including highly repeatable imaging methods that are especially effective for 2D and 3D measurements of OPC and integrated circuit structures. The talk will also demonstrate the advantages of model-based SEM 3D metrology as well as, elaborate on the requirements and possible solutions for 3D metrology that have the potential for highly precise and accurate results.

8324-02, Session 1

Inspection and metrology for through-silicon vias and 3D integration

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3D IC integration employs advanced interconnect technologies including through-silicon vias (TSVs), bonding, wafer thinning, backside processing and fine pitch multi-chip stacking. In 2013, Mobile Wide I/O DRAM is expected to be one of the first high volume 3D IC applications. Many of the manufacturing steps involved with TSV processing and 3D integration can complicate inspection and metrology. A review of a typical "via-mid" flow is presented, with emphasis on the inspection and metrology challenges that result from 3D integration. A preliminary look at the 2011 ITRS roadmap for 3D interconnect metrology is presented, including the gaps in currently available inspection and metrology tools.

8324-03, Session 2

Hybrid metrology solution for 1X node technology

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Every few years the semiconductor industry has widely adopted into manufacturing a new type of equipment capable of dimensional metrology. Some past examples include CD-SEM, AFM, image-based overlay, thin film metrology, and, most recently, scatterometry. The accelerated pace of the industry in recent years is putting a strain on these equipment types to keep up with the ever-increasing metrology challenges. Fortunately, a revolution in dimensional metrology appears to be forming with the recent advent of Hybrid Metrology (HM). HM is the practice of combining measurements from multiple equipment types in order to enable or improve measurement of one or more critical parameters.

In this paper we extend our previous work on HM to measure advanced 1X node layers - resist as well as 3D etch structures such as FinFETs. We study the issue of precision and accuracy matching between toolsets involved in hybridization by comparison to conventional non-hybrid results. We also investigate advanced modes of HM such as impact of strength of hybridization, resist shrinkage, tool matching, sampling differences & line-edge roughness (LER) on HM measurement performance and combination of external (hybridization) and internal (multichannel, multi-stack) sources of information as part of the holistic metrology approach.

Next-generation CDSEM measurements make use of model-based library (MBL) of electron interaction with full profile of line. As an extension of hybrid metrology, we hybridize the CDSEM MBL model using profile information obtained from scatterometry, and verify accuracy improvements. This paper also addresses the issue of the quality of the source data during hybridization.

8324-04, Session 2

Dose-focus monitor technique using CD-SEM and application to local variation analysis

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The process window for ArF immersion lithography continues to decrease, and Depth of Focus (DoF) at leading edge technology node has entered sub-100nm territory. Process control is becoming one of the most critical issues for advanced lithography. Precise monitoring of dose and focus, a key element of process control, has been explored and developed using various targets and metrology methods. A dose-focus metrology technique using Process Monitor Grating (PMG) and scatterometry has been established, where focus errors can be determined to few nm precision and dose errors to 0.1% precision. This technique has demonstrated excellent performance on simple resist/BARC stack wafers for tool monitoring applications. However, for

dose-focus monitoring on product wafers, complicated thin film stacks make it difficult to generate scatterometry models, and the sensitivity to under-layer thickness and optical property variation may degrade the dose-focus monitoring precision. A large target size, necessary for scatterometry metrology, is another issue for on-product application. A CD-SEM method has the potential to overcome these issues by using small targets and by collecting surface topography information which is blind to underlying thin films. The key challenge is the precise metrology of pattern profiles to obtain focus information using top-down CD-SEM technique.

The targets of our CD-SEM dose-focus monitoring technique consist of two structures. The first target is a dense grating structure with isofocal pitch, and is used primarily for dose determination. The second target is a relatively isolated line grating with no assists for high focus sensitivity. The total target measures less than 10um on each side. The model which describes how the top and bottom CD depend on dose and focus deviations is the same as that for scatterometry dose-focus metrology, and monitoring precision is estimated to be the order of 1% for dose and 15nm for focus. Multiple resist process conditions are evaluated in terms of monitoring precision, and versatility of this technique is discussed in the presentation.

By using a mask with a multitude of these targets, it is possible to study focus and dose variations across the wafer in great detail. As a metrology diagnostic, we have measured the focus variation of pairs of such targets. Figure 1 shows the correlation between the two focus values of the pair, for various separations between the two targets. When the separation is very small, the correlation is very good, with only 11nm (3sigma) delta. We feel that the true focus variation between such nearby targets is near zero, and so we attribute the observed variation to the precision of our metrology method. When the distance between the two targets is in the mm range, we see a significantly larger delta up to 27nm (3sigma). We attribute this larger variation to true focus variations, such as wafer thickness variation and other sources. Our small CD-SEM targets allow us to explore this kind of local spatial variation analysis. We will discuss application of this technique in the paper. The method has strong potential to apply to dose and focus monitoring of product wafers.

8324-05, Session 2

Potential new CD metrology metric for future node production

J. Foucher, N. G. S. Figueiro, CEA-LETI (France)

Introduction of new material stacks, more sophisticated design rules and complex 3D architectures in semiconductor technology has led to major metrology challenges by posing stringent measurement precision and accuracy requirements for various critical dimensions (CD), feature shape and profile. Current CD metrology techniques being used in development and production such as CD-SEM, scatterometry and CD-AFM, individually have intrinsic limitations that must be overcome. The approach of hybrid automated metrology seems necessary. Using multiple tools in unison is an adequate solution when adding their respective strengths to overcome individual limitations. Such solution will give the industry a better metrology solution than the conventional approach. Nevertheless, this is not enough since the industry is requested for 2D and 3D profiles information. Indeed, CD, height and/or Sidewall angle are information which is limited for future nodes production. Full profile information is necessary.

In this paper, the first part will be dedicated to the presentation and discussion of the latest results obtained on hybrid metrology related to CD-SEM enhancement with a reference technique such as the AFM3D technology. A second part will be dedicated to Scatterometry potential enhancement with a reference technique. Finally, in a third part in order to enhance the usage of different tools in unison we will define a new potential metric that can be used by the semiconductor industry in a near future. This metric will take into account all pattern's profile information in order to overcome the limitations of simple CD and/or SWA information.

8324-06, Session 2

A comparison of alignment and overlay performance with varying hardmask materials

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In nanoscale patterning technology, an intermediate layer, generally known as hardmask, is inevitable need to further transfer the patterning from thin photoresis to working layer. However, carbonaceous hardmask such as amorphous carbon layer (ACL) can cause degradation of the image quality from align and overlay mark due to its higher extinction coefficient. Thus, the correlation of alignment and overlay performance with varying hardmask materials is required to meet a tight overlay budget of 2x nm node and beyond. In this paper, we have investigated the effects of the hardmask materials with respect to the optical properties on the performance of overlay applicable to 2x nm memory devices.

8324-07, Session 2

High-order wafer alignment in manufacturing

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Requirements for ever tightening overlay control are driving improvements in tool set up and matching procedures, APC processes, and wafer alignment techniques in an attempt to address both systematic and non systematic sources of overlay error.

Thermal processes used in semiconductor manufacturing have been shown to have drastic and unpredictable impacts on lithography overlay control. Traditional linear alignment can accommodate symmetric wafer distortions even if these defects vary in magnitude wafer to wafer. However linear alignment cannot accommodate asymmetric wafer distortions caused by variations in film stresses and rapid thermal processes. Overlay improvement techniques such as product corrections per exposure and tool matching corrections based on reference wafers can be used to compensate for known systematic errors. However, systematic corrections applied on a lot by lot basis cannot account for variations in wafer to wafer grid distortions caused by semiconductor processing.

With High Order Wafer Alignment, the sample size of wafer alignment data is significantly increased and modeled to correct for process induced grid distortions. HOWA grid corrections are calculated and applied for each wafer. Improved wafer to wafer overlay performance was demonstrated.

How HOWA corrections propagate level to level in a typical alignment tree as well as the interaction of mixing and matching high order wafer alignment with traditional linear alignment used on less overlay critical levels. This evaluation included the evaluating the impact of overlay offsets added by systematic tool matching corrections, product specific corrections per exposure and 10 term APC process control.

8324-01, Session 3

Challenges and solutions for overlay in low-k1 imaging: model for the printing of large features with extreme illumination, and the subsequent inspection with edge-detection or scatterometry based metrology

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The continuous shrinking in optical lithography and the physical
limitations in both, shorter wavelengths as well as large numerical
apertures, required the industry to adapt more and more sophisticated
illumination schemes. In order to print lines with a pitch that comes
close to a k1 of 0.25, extreme dipole illuminations with small angular
openings and extremely small ring widths are required. Such illumination
establishes almost a two-beam imaging situation for the small pitches
which results in a good contrast and a large depth of focus. Overlay
markers, however, are typically much larger than the actual device
features, up to several microns. The printing of such large structures
suffers substantially from using these extreme illumination conditions.
Aerial images show optical proximity effects in the order of several 100
nm for these large features which is somewhat counter intuitive. The
resulting resist profiles reveal significantly sloped sidewalls that change
through focus and dose.

Simultaneously with this resolution-driven trend to extreme illumination
conditions, the device physics drives overlay requirements towards single
digit nanometer values. Assigning such a single digit nanometer position
to the aforementioned large and irregularly shaped resist profiles, though,
becomes almost a meaningless task. Both, edge detection based overlay
metrology as well as scatterometry based methods, face a new set of
challenges to return an overlay number that represents the locations of
the actual device structures.

This paper explains why large features print so unexpectedly poor under
extreme illumination conditions, even in the absence of any aberrations.
It further establishes a method how to understand and predict the results
of overlay metrology on 3-dimensional resist profiles. In particular, a
simulation flow is presented which covers the lithographic exposure as
well as the actual inspection of the resist profiles. Both edge-detection
(with broadband illumination) and scatterometry-based metrology are
covered. It is shown how this flow can be used to study the impact
of scanner/process imperfections on the overlay readings. This helps
to classify these imperfections, gain a deeper understanding of the
critical parameters in the printing and inspection of overlay marks, and
eventually develop and assess mark enhancement strategies such as
chopping and/or applying assist features.

The modelling and tooling developed in this paper will be applied in the
paper "Study of high order distortion in intra field using extreme off-axis
illumination on a manufacturing site" by Kiho Yang et al., presenting
simulation studies together with a significant number of wafer data.

8324-02, Session 3

Study of high order distortion in intra field using extreme off-axis illumination on a manufacturing site

J. Lee, B. Lee, T. Lee, J. Park, C. Lim, M. S. Kim, H. Kang, Hynix
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Zeiss SMT GmbH (Germany); E. Janda, ASML US, Inc. (United
States); K. Bhattacharyya, ASML Netherlands B.V. (Netherlands);
B. Geh, Carl Zeiss SMT Inc. (United States); C. Ryu, Y. Min,
ASML Korea Co., Ltd. (Korea, Republic of)

Challenges for the upcoming overlay control under 3Xnm nodes
are unprecedented with usual specifications in semiconductor
manufacturing. As the cell size of memory device is decreasing, various
resolution enhancement techniques have been developed to make
smaller patterns on the wafer. One of preferred techniques to make
fine patterns in microlithography is the application of extreme off-axis
illumination (OAI) which is optimized to specific memory cell structure.
The choice for OAI has been made under the assumption that there
would be little or no impact on the printing fidelity of large structures,
such as overlay marks. We know now, that this assumption - even though

intuitive - is incorrect.

In this paper, we analyzed the origin of intra field overlay error caused
by aberrations under extreme OAI (as it is called 'delta distortion')
with ASML and Carl-Zeiss. Our study will focus on impact of scanner/
process imperfections on the overlay readings in view of real device as
a manufacturing site. In this paper, results on delta distortion study are
reported as below.

1) It was shown that delta distortion level is too high considering normal
scanner aberrations.

2) We confirmed that delta distortion reading varied significantly through
Energy/Focus change as well as among exposure tools.

3) In a separate paper, we will provide the foundation to understand and
predict overlay performance with extreme OAI for both image based
overlay (IBO) and diffraction based overlay (DBO) (Presenter: Jens-Timo
Neumann)

4) We performed various studies to minimize the delta distortion effect of
the overlay reading.

- Overlay mark size split

- Comparison between image based overlay and diffraction based
overlay method.

- Comparison of overlay reading with various segmentations.

- Comparison on overlay of cell patterns and various vernier patterns.

8324-03, Session 3

Spacer process and alignment assessment for SADP process

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Self aligned double patterning (SADP) is now widely accepted as a viable
technology for the further extension of 193nm lithography towards the
22nm /18nm technology nodes. SADP was primary introduced for the
manufacturing of flash memory due to its 1D design geometry. However,
SADP became a main stream technology for advanced technology nodes
for logic product.

SADP results in alignment and overlay marks with reduced image
contrast after completion of spacer patterning. Consequently there is an
elevated risk that the overlay performance of the cut lithography layer on
the spacer may be negatively impacted.

The self aligned spacer process results in asymmetric spacers. Two types
of surface (inside and outside) of the spacer are formed. This asymmetry
has an impact in respect to the decomposition of the layer on overlay and
CD control tolerance.

Immersion scanner has made huge improvement on overlay
specification. A large amount of work has been made to correct the non
linear alignment error and the mask error. An assessment on 193nm
immersion lithography cluster of alignment and overlay tolerance will be
made on wafers with different spacer technology.

SADP is used in combination with trim lithography and results in double
patterning lithography. Some solutions for 22nm and 14nm technology
are combining SADP with different decomposition model. Double
mandrel layer can be used for wiring layer on logic product. SADP can
be as well combined with cut lithography or double cut lithography. The
cut lithography can be varied as positive and negative patterning. The
different decompositions of each layer according to the required design
rules have some consequences on the tolerances used in lithography in
terms of overlay. These different aspects will be discussed in this paper.

8324-08, Session 3

Overlay accuracy with respect to device scaling

P. J. Leray, S. Y. Cheng, IMEC (Belgium)

Overlay metrology performance is usually reported as repeatability, matching between tools or optics aberrations distorting the measurement (Tool induced shift or TIS). Impressive improvements of these metrics have been achieved in the past years by tool suppliers. But, what about accuracy? By using different target type, we have already reported small differences in the mean values as well as the fingerprints [1]. These differences are making the correctable questionable. Which target is right, which translation, scaling should we feedback to our scanner?

In this paper we will investigate the source of these differences using several approaches. First, we measure the response of different targets to several overlay offsets programmed in a test vehicle. Second, we check the response of the same overlay targets to overlay errors programmed by the scanner. We will compare overlay target design: what is the contribution of the feature sizes composing the target? We will use different overlay measurement technique: is DBO (Diffraction Based Overlay) more accurate than IBO (Image Based Overlay)? We will measure overlay on several stacks: what is the stack contribution to inaccuracy? In conclusion, we will explain partially the observed differences and propose solution to reduce them.

[1] "Diffraction Based Overlay Re-assessed" P. Leray, D. Laidler, K. D'havé, S. Cheng. Proc. of SPIE Vol. 7971-14.

8324-09, Session 3

New analytical algorithm for overlay accuracy

B. Ham, S. Yun, M. Kwak, S. M. Ha, C. Kim, S. Nam, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

The extension of optical lithography to 2Xnm and beyond is often challenged by overlay control. With reduced overlay measurement error budget in the sub-nm range, conventional Total Measurement Uncertainty (TMU) data is no longer sufficient. Also there is no sufficient criterion in overlay accuracy. In recent years, numerous authors have reported new method of the accuracy of the overlay metrology: Through focus and through color. Still quantifying uncertainty in overlay measurement is most difficult work in overlay metrology. We develop an analytical algorithm for overlay accuracy. And a concept of non-destructive method is proposed in this paper. For on product layer we discovered the layer has overlay inaccuracy. Also we use find out source of the overlay error though the new technique. Furthermore we compare the empirical data to simulation data. Our results show that to characterize an overlay metrology technique that is suitable for use in advanced technology nodes requires much more than just evaluating the conventional metrology metrics of TIS and TMU.

8324-11, Session 4

ArFi lithogrphy optimizations for thin OMOG reticle with fast aerial imaging

I. Englard, Applied Materials BV (Netherlands); J. M. Finders, ASML Netherlands B.V. (Netherlands); Y. Cohen, S. Mangan, Applied Materials (Israel); B. Connolly, Toppan Photomasks, Inc. (Germany); Y. Kojima, M. Higuchi, Toppan Printing Co., Ltd. (Japan); O. Mouraille, M. Janssen, ASML Netherlands B.V. (Netherlands)

As half pitch decrease to sub 20nm territories, the latest hybrid IC (integrated circuits) designs contain an increasing amount of features, which are closer to the resolution limits of the scanners, compared to previous generation of IC designs. This trend includes stringent design rules and complex, smaller than ever optical proximity correction (OPC) structures. In this regime, new type of mask, known as thin opaque MoSi on Glass (thin OMOG) introduced to overcome the shortcomings of the well-established phase shift masks (PSM).

As for lithography, at the Intrafield domain, closer to the scanner resolution limits, the scanner and mask have 1st order role in determination of the final lithographic performance. Holistic lithography techniques have been developed in order to optimize the mask and scanner entangled performance for the most demanding sub 20nm node features critical dimension (CD) uniformities and common process window (PW).

This paper present an efficient and production worthy methodology for evaluating the latest immersion scanner and thin OMOG mask CDU, PW and 3D effects fingerprints, and optimize them with the latest holistic ArFi lithography high order optimizers.

8324-12, Session 4

Semiconductor device integration scheme impact on wafer inspection

T. F. Crimmins, Intel Corp. (United States)

Up through the 180nm manufacturing node, pitch and CD scaling have been the main drivers of wafer inspection (WI) requirements, with tighter pitches and smaller CD's pushing the adoption of inspection tools with shorter wavelengths and increased photon budgets. Beginning with the introduction of a Cu backend process and continuing with the introduction of strained silicon, Hi-k / metal gates and tri-gate transistors, integration schemes are playing a prominent role in WI scaling requirements.

As an example, consider the comparison between planar and tri-gate transistors. In the planar transistor case, the set of z-planes impacted by sequential processing steps do not overlap. Defects introduced during diffusion patterning and those introduced by gate patterning can be detected separately by scanning after the respective processing steps. Pattern noise from diffusion, such as line edge roughness, can be suppressed during gate pattern inspection by modulating the inspection focus position.

Tri-gate transistors introduce new complexity into the inspection problem. The range of z-planes impacted by gate patterning overlaps heavily with the diffusion fins. The effectiveness of noise separation from different patterning steps via defocus is significantly reduced. Additionally, the fins introduce aggressive feature size and aspect ratio scaling.

The present paper explores, through FDTD aerial image simulations of SRAM bit cells, the impact of device integration scheme on WI, with a particular emphasis on how the system requirement trends are changed. Various defect types are simulated for planar gate, planar Hi-k / metal gate and tri-gate transistors. The key conclusions are that the device integration scheme has a significant impact on WI requirements and that it is critical to simulate complex devices to accurately predict WI performance.

8324-13, Session 4

Ultrahigh resolution EUV coherent diffraction imaging using a tabletop 13nm HHG source

M. D. Seaberg, D. E. Adams, M. M. Murnane, H. C. Kapteyn, Univ. of Colorado at Boulder (United States)

As lithography progresses into the extreme ultraviolet (EUV), there is an increasing demand for imaging and inspection modalities that use at-wavelength light.[1] Since only reflective and diffractive optical elements are possible in the EUV, and since both of these present challenges for implementing a high-resolution imaging system, new imaging techniques that are not limited by the fabrication efficiency of the optics are of increasing interest.

In recent years, coherent diffractive imaging (CDI) has emerged as an

attractive candidate for x-ray imaging. Also known as lensless imaging, CDI replaces the optics of an imaging system with an iterative phase retrieval algorithm-at the cost that spatially coherent illumination is necessary.[2] In this imaging modality, the diffraction pattern of light scattered from an object is detected directly at a distance far enough away to satisfy an oversampling condition. In general, only the scattered intensity can be detected but, by sampling the diffraction pattern at twice the Nyquist frequency the phase of the detected scatter can be shown to be uniquely encoded in the detected intensity.[3] The oversampling requirement can also be understood as a requirement that the object be isolated, with no nearby scatterers. The result is that, with no optical elements between the object and the detector that would introduce resolution-degrading aberrations, the resolution is limited only by the NA of the detected signal; i.e. the diffraction-limit.

Here we have implemented the CDI technique using a high-harmonic generation (HHG) source at 13nm. The HHG source is produced by focusing a 2kHz, 2mJ, 25fs Ti:sapphire laser into a 5cm-long, He gas-filled, hollow waveguide, allowing for phase-matched upconversion of the laser light into the EUV. The phase-matching process produces a spatially coherent, laser-like 13nm beam, ideally suited for the requirements of CDI.[6] Using this source, we have obtained reconstructed images for two test patterns that demonstrate 22nm resolution: a record for any tabletop light-based microscope and high enough for EUV mask inspection. Moreover, we have achieved 25nm resolution images in an integration time of just 30s, with promise for obtaining images in just a single shot in the near future. Finally, we have shown that the high NA (~0.36) of the scatter data allows us to extract a 3D image from a single 2D diffraction pattern.[4,5]

Our current objective in this work is to demonstrate similar resolution in a reflective geometry suitable for mask inspection. An apertured-illumination scheme, which circumvents the isolated-object requirement, will be discussed. The goal is to implement an extremely compact EUV microscopy tool, with particular emphasis on lithography and mask inspection but with numerous other applications including biological nano-imaging, dynamic imaging of magnetic domains and nanoscale heat transport, and imaging the formation of laser-produced plasmas.

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8324-14, Session 4

Beyond 22nm node patterned defect and CD metrology by TSOM

B. D. Bunday, International SEMATECH Manufacturing Initiative (United States); R. Attota, National Institute of Standards and Technology (United States); V. H. Vartanian, SEMATECH North (United States)

Through-focus scanning optical microscopy, or TSOM, is a method [1,2] that transforms conventional optical microscopes into truly 3D metrology tools for nanoscale to microscale dimensional analysis with nanometer scale sensitivity. The method can be used in both reflection and transmission modes of microscopes. It has been shown to be applicable to a variety of target materials ranging from transparent to opaque and shapes ranging from simple nanoparticles to complex semiconductor memory structures, including buried structures under transparent films. Potential applications include defect analysis, inspection, and process control; critical dimension (CD), photomask, overlay registration, nanoparticle, film thickness, and 3D interconnect metrology (large range depth analysis such as TSVs); line-edge roughness measurements; and others [2]. The method is relatively simple and inexpensive, has high throughput, and provides nanoscale sensitivity for 3D measurements. Potential applications have been demonstrated using experiments and simulations [2].

TSOM is not a resolution enhancement method. However, it has the potential to provide lateral and vertical measurement sensitivity of less than a nanometer using a conventional optical microscope [2], comparable to the dimensional measurement sensitivity of other CD metrology tools. The technique is capable of measuring features far beyond the theoretical limits of optical microscopy, due to the much richer data content collected at many z-heights (i.e., through focus). Additionally, TSOM appears to decouple profile dimensional changes at the nanoscale, such as small perturbations in sidewall angle and height, with little or no ambiguity, and may be able to analyze target dimensions ranging from as small as 10 nm to relatively large dimensions (up to many microns) with similar nanometer scale sensitivity.

This work will demonstrate TSOM results of simulations and some supporting experiments to demonstrate the metrology application of TSOM to features at the ITRS 22 nm node [3], including measurement of linewidths down to 10 nm, while showing the ability to measure changes in line height, sidewall angle, and pitch variations.. By extension, these results will show the feasibility of applying TSOM to important contemporary metrology problems in measuring double patterned features and FinFETs.

8324-15, Session 4

Scatterfield microscopy of 22nm node patterned defects using visible and DUV light

B. M. Barnes, Y. Sohn, H. Zhou, R. M. Silver, National Institute of Standards and Technology (United States); A. Arceo, SEMATECH North (United States)

We demonstrate experimental performance gains using scatterfield microscopy techniques for die-to-die defect comparison metrology for 22 nm node patterned defects. Scatterfield microscopy enables design-specific bright field optical tools for use in signal-based defect analysis of features with dimensions well below the measurement wavelength. Central to this approach is engineering the illumination as a function of angle and polarization with analysis of the entire scattered field. We will present our investigation of more advanced implementations using frequency modulation and control in the collection path of the optics. This methodology has been incorporated into simulations that demonstrate improvements in defect inspection for various defect types on intentional defect array (IDA) wafers recently provided by the SEMATECH Metrology group.

Comprehensive modeling has been performed to investigate a range of illumination wavelengths to enhance defect detection for applications at the 22 nm node and beyond. Simulations have been performed to evaluate performance gains obtained at wavelengths ranging from 193 nm to 450 nm. Theoretical simulations to be reported are carried out using a fully rigorous three-dimensional finite difference time domain (FDTD) electromagnetic simulation code. Simulation data for similar stacks show that many defects are more detectable when using the shorter 193 nm wavelength.

While reduced wavelengths in general improve the defect detectability, the best parameters for a given defect may differ due to the process stack, materials, defect type, and directionality, incident angle, and polarization. Experimental validation of simulated trends is required to assess the simulations properly and the extensibility suggested by such calculations. Two optical platforms are used to make comparative evaluations of defect detectability. The NIST 193 nm Scatterfield Microscope and the NIST Visible-Light Scatterfield Microscope are

both custom built tools and each features an "open" architecture which permits the illumination engineering. Recent work evaluating collection path optical field engineering will also be described. The detectability gains obtained from off-axis illumination and polarized visible-light microscopy will be compared with those gains achieved using similar Scatterfield techniques at 193 nm.

8324-122, Session 4

Multiple column high-throughput e-beam inspection

E. D. Liu, C. Tran, Multibeam Corp. (United States); K. M. Monahan, Quantflow Strategies LLC (United States); T. A. Prescop, D. K. Lam, Multibeam Corp. (United States)

Today's single-beam systems for Electron-Beam Inspection (EBI) offer high resolution, but take greater than 10 hours to inspect a 300mm wafer. With each new technology generation, higher resolution is needed to detect critical defects, and EBI throughput continues to plummet.

The single-column EBI approach has limitations. The electron current in the column is limited by Coulomb interaction. As pixel sizes shrink to detect smaller critical defects, fewer electrons are collected per pixel resulting in greater shot noise. The pixel rate is limited by beam current, shot noise and image processing speed. With a typical pixel rate of 200 MHz and 20 nm pixels, it would take about 250 hours to inspect an entire 300mm wafer.

In single-column EBI, there is a fundamental conflict between high-resolution and high-throughput. Multiple columns solve these problems.

Multibeam's approach separates electron beams spatially in multiple columns to minimize image blur and enable higher total beam current. Images acquired from the columns are processed in parallel. A cluster of 200 columns, for example, is 200x faster than a single column, enabling high-resolution high-sensitivity wafer inspection. Each of the all-electrostatic columns is small; a 2D array of multiple columns covers the entire surface of a 300mm wafer for in-line defect inspection. Multiple-chamber cluster tools provide even higher throughput.

Multibeam has designed, built and tested several generations of e-beam columns. The tests demonstrated imaging of alignment marks, voltage contrast inspection, and detection of multiple types of defects including shorts, opens, partially cut lines, etch errors and patterning errors (Figure 1).

In this paper, we discuss the multiple-column system architecture for e-beam inspection with high throughput and high sensitivity. Multibeam's column-arrays are built with identical e-beam columns (Figure 2), each column having an identical electronic control board. The multiple-column architecture has unique advantages:

- Unlike single beam systems, the entire wafer can be sampled at multiple points simultaneously, without moving the wafer stage.

- Unlike single beam systems, the high speed of this initial characterization enables in-line applications such as after-develop inspection (ADI) and after-etch inspection (AEI).

- The cross-wafer sample has the added advantage of including outer regions of the wafer where most defects occur.

- The cross-wafer sample may be repeated with several beam voltages and spot sizes, generating an ultra-fast DOE that optimizes sensitivity to defects of interest.

- In addition, variation in cross-wafer defect counts can trigger real-time adaptive sampling algorithms that increase or decrease sample size when necessary.

Thus, the multiple-column architecture enables rapid optimization of beam parameters and sample plans, and provides the throughput required for true in-line inspection applications.

8324-16, Session 5

Roughness metrology of gate all around silicon nanowire devices

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In this work Silicon Nano Wires (SiNW) ranging in dimensions of 6 - 25nm were characterized. Hydrogen annealing was shown as a useful method for the fabrication of smooth suspended Si nanowires (SiNW) that are used to build gate-all-around MOSFETs [1]. Wires that were annealed in H2 exhibit surface roughness below 1 nm along the full length of 100nm long suspended wires.

Different smoothing processes yield SiNWs with edge roughness values in the sub nm range. Such small differences in roughness values, propose an interesting opportunity to evaluate sensitivity of the SEM metrology algorithms.

A simulation program modeling SEM images including small features was developed, taking into account various SEM signal formation factors. Synthetic (simulated) images of SiNW in a range of 6-25 nm and roughness of 0 - 1 nm were produced. Using the synthetic images, knowing the true values, we characterized the performance and sensitivity of Line Edge Roughness (LER) and Line Width Roughness (LWR) algorithms and metrics. In the meanwhile, real SiNW after various smoothing conditions were measured using a CD-SEM. Results were compared between actual SiNW and corresponding simulated synthetic images.

In this paper we present SEM metrology measurements of suspended SiNW devices having sub 1 nm roughness and we compare our experimental data with simulation results.

8324-18, Session 5

Sensitivity analysis of line-edge roughness measured by means of scatterometry: a simulation-based investigation

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Various reports state that Line Edge/Width Roughness has a significant impact on lithography-fabricated integrated circuits, rendering it desirable to be able to determine the LER in-line so that it never exceeds certain specied limits.

In our simulation work we deal with the challenge of measuring LER on CD-50nm resist gratings using plane-mount scatterometry. We show that there is a difference between LER and no-LER scatter signatures which first: depends on the polarization and second: is proportional to the amount of LER. Moreover - we show that the said difference can be best-fit to the difference between scatter signatures of two rigorously determined, specific no-LER CDs, which allows us to predict the sensitivity of ITRS' "manufacturable solution" for scatterometric LER measurement just by using computationally cheap 1D RCWA simulations. As it can be shown the sensitivity is not uniform for all realizations of the same CD (e.g. for different resist heights), so not in all gratings LER is equally easy to determine.

8324-19, Session 5

Noise effects on contact-edge roughness measurement

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The accurate and precise measurement of the sidewall roughness of lithographic features has been a continuous challenge for litho-metrology community. Although scatterometry and CD-AFM techniques have also been applied, the analysis of top down CD-SEM images remains the

workhorse tool in sidewall roughness measurement. The majority of works have been devoted to the measurement of the sidewall roughness of lines (Line Edge/Width Roughness (LER/LWR)) due to the direct effects of LER/LWR on transistor performance. An important issue in LER/LWR metrology is the effects of SEM image noise and several papers have been devoted to the study of these effects and proposed methods for their elimination and a noise-free estimation of LER/LWR [1-5].

Nevertheless, a semiconductor device contains not only gates but also interconnects, contacts and vias for the vertical and horizontal communication between the different parts of integrated circuits. These features also suffer from the presence of roughness on their surfaces. In the case of contacts, this roughness is usually called Contact Edge Roughness (CER) and its metrology and characterization have been attracted some interest recently [6-8] without, however, considering the image noise effects on the measurement of CER parameters.

The aim of this work is to investigate these effects by utilizing synthesized SEM images similar to the experimental top-down ones used widely in CER metrology. In these images, the contact edges are generated by the inverse Fourier transform technique and CER is characterized by the rms value, the correlation length and the roughness exponent. The image pixel intensity is assumed to increase exponentially on the edges, while the SEM noise is modeled by a sum of Gaussian and Poissonian terms [9]. These images are used for the systematic assessment of image noise effects on CD, CD variation, CER parameters (rms, ξ, α), power spectrum (PS) and height-height correlation function (HHCF). We find that CD remains almost independent of noise, whereas the CD variation, rms and correlation length are the most sensitive to noise amplitude. Also when the noise level is low it is shown that only the high-frequency PS and small-distance HHCF are affected. On the contrary, higher noise amplitudes have also effect on low frequency fluctuations.

Furthermore, these synthesized SEM images are used for the evaluation of the methods proposed in LER/LWR metrology for noise-free LER/LWR estimation [1,2] in order to check their applicability to noise-free CER measurement.

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8324-113, Session 5

High-throughput and nondestructive sidewall roughness measurement using 3-dimensional atomic force microscopy

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As the feature size in the lithography process continuously shrinks, accurate critical dimension (CD) measurement becomes more and more important. With the smaller features, the sidewall increasingly influences the CD measurement and characterizing the CD of a structure becomes more critical on the nanoscale. For the state-of-art extreme ultraviolet (EUV) lithography development, the characterization of the sidewall roughness of the photoresist and the study of how this sidewall roughness of the photoresist will be transferred into the underneath layers during etching is a critically important but yet very challenging task.

Over the past a few years, atomic force microscopy (AFM) has become a powerful tool for accurate nanometrology. However, because most AFMs operate in a top-down configuration, AFM has limited access to the sidewall; this is especially true when the sidewall angle is near or greater than 90 degrees. Some temporary solution has been used to characterize the sidewall roughness by mechanically cleaving the sample and then imaging the sidewall with AFM on tilted sample. But this method only works for large features and it is destructive.

Recently, we have introduced a new 3D AFM imaging technology using tilted Z scanner. In this new 3D AFM configuration, the Z scanner is separate from the XY scanner. When the Z scanner is tilted to one side with respect to the XY scanner, where the sample is attached, the AFM tip attached to the Z scanner is tilted too. By this mean, the sharp end of the tip can easily reach the sidewall of the sample features; even the sidewall angle is close or over 90 degree. This new technology is extremely powerful for sidewall roughness measurement. Because conical ultra sharp tip is used, this 3D AFM imaging technology can achieve same high resolution as regular AFM, even on the sidewall. By scanning along the feature, only a few scan lines are needed to accurately measure the sidewall roughness, and this 3D AFM technology has very high throughput for sidewall roughness measurement. This 3D AFM technology does not require any special sample preparation, and it is non-destructive. Because of it is high resolution, high throughput, and non-destructive, this new technology can be potentially used for in-line metrology for production.

In this paper, we have also studied the throughput and repeatability of this new 3D AFM technology as a metrology solution for sidewall roughness.

8324-19, Session 6

Printability and inspectability of defects on EUV blank for 2xnm hp HVM application

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The availability of defect free masks remains one of the key challenges for inserting extreme ultraviolet lithography (EUVL) into high volume manufacturing (HVM). Among the defects on finished EUV masks, 75 % originate from the blank level. Therefore, accomplishment of defect free masks will depend on the timely development of defect inspection tools which cover both blank and pattern inspections. 23.1 nm SEVD (sphere equivalent volume diameter) size should be detected by the blank inspection tool to support 35 nm half pitch (HP) application using EUVL. And only one blank inspection tool can cover that range. In this paper, defect printability and inspectability are studied using a state-of-the-art blank inspection tool and scanner using real defects from an EUV blank for 2X nm hp application.

First, an EUV blank is inspected with the blank inspection tool, and then the detected defects are classified based on defect type, size, and height. Our preliminary result shows that blank defects less than 20 nm SEVD can be detected with the current blank inspection tool. This means that we can study the requirement of the blank inspection tool for 2X nm hp application. Second, an EUV patterned reticle is fabricated on the blank with the pattern of line and space (L/S) and contact array for 32 nm and 25 nm HP. And the reticle is exposed using the NXE3100 from ASML. Defect printability on the blank is evaluated and the smallest printable defect size is determined. Some defects are reviewed with SEMATECH-LBNL Actinic inspection tool (AIT). Third, the required specification for a blank inspection tool at 16 nm hp and 11nm hp is simulated to understand if a future blank inspection tool can cover these device nodes. Finally this paper will present requirements for the blank inspection tool and gaps for successful EUV implementation for device integration using EUV lithography.

8324-20, Session 6

Closing the infrastructure gap: status of the AIMS EUV project

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The EUV mask infrastructure is of key importance for a successful introduction of EUV lithography into volume production. In particular, for the production of defect free masks an actinic review of potential defect sites is required. With such a review it can be decided if a defect needs to be repaired or compensated. It also serves as verification whether the respective absorber or compensational repair with e.g. the MeRiT® tool has been successful, i.e. it closes the control loop in mask repair. To realize such an actinic review tool, Carl Zeiss and the SEMATECH EUVL Mask Infrastructure consortium started a development program for an EUV aerial image metrology system (AIMS EUV). In this paper, we will present the status of the AIMS EUV development and show simulations on the expected system performance. We model the impact of small blank defects to line size and discuss their compensation by absorber resizing and the review of that compensation with the AIMS EUV tool.

8324-20, Session 6

Investigation of the performance of state-of-the-art defect inspection tools within EUV lithography

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EUV lithography is bringing many new challenges in the field of defect inspection. Both in wafer inspection and reticle inspection it is not only the fact that EUVL is targeting smaller dimensions which makes the detection of the defects of interest (DOI) more challenging.

For wafer inspection the high line edge roughness (LER) values that are observed in current EUV resist processes contribute to higher inspection noise, which makes it very difficult to distinguish some defects of interest (= defect that causes a CD shift of more than 10%) from LER.

For (reticle) blank inspection (BI) and patterned mask inspection (PMI), the existence of defects inside the multilayer mirror, which is not penetrable by the wavelengths used by the optical inspection tools, makes it more difficult to locate all printing reticle defects. .

This work investigates the potentials and limitations of the most state-of-the-art inspection tools for both wafer inspection (WI), reticle blank inspection (BI) and patterned mask inspection (PMI). The focus is on 'printing' reticle defects and all 3 techniques will be applied to detect defects on reticles which are specifically designed for this investigation.

Wafer exposures are carried out on 2 EUV full field scanners in IMEC, the ASML Alpha Demo tool (ADT) and the NXE:3100 preproduction tool. These wafers are used to review all defect locations that are reported by WI, BI and PMI and only the defects that end up on the wafer are considered as DOI.

Wafer inspection is performed on the latest generation BF inspection tool from KLA-Tencor, KLA2835. Because the design of the reticle allows a cell-to-cell inspection, it is possible to detect repeating defects, which can be assigned to the reticle. Furthermore the reticle has programmed defects of various sizes (see picture 1), which makes it possible to verify the ultimate resolution of the inspection.

An additional target of this work in terms of WI is to investigate whether it is possible to use simulations to predict which parameters can have a beneficial effect on the inspection sensitivity. These parameters can be changes in the lithographic and underlying stack, but also which

inspection settings result in the highest S/N for a certain type of DOI, can be predicted with simulation. Any positive outcome of the simulation will be verified experimentally by EUV exposures

Both blank inspection and patterned mask inspection (die-to-die mode) are performed on the KLA-Tencor Teron600. A technique will be shown to translate results of both these inspections into wafer coordinates, which will make it possible to review these defects on wafer.

The final goal is to come up with a defect population of natural printing reticle defects and for each inspection technique it will be possible to indicate which (types of) defects are likely to be detected and what are the noise sources limiting detection capability. Additionally the known locations and sizes of the programmed reticle defects can result in additional information about the performance of both wafer inspection and patterned mask inspection.

8324-21, Session 6

Experimental quantification of shot noise contributions to contact hole local CD nonuniformity

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As feature sizes continue to shrink, the discrete nature of light and matter is becoming a significant contributor for the variations observed in lithography in general and for EUV in particular. Owing to the 15x higher energy of EUV compared to ArF photons and similar if not lower exposure doses, the number of photons per unit area in EUV is significantly reduced. If the number of photons per contact hole is considered, the situation is even more dramatic, as the target area of a contact is smaller for EUVL than for ArF patterning. However, the latter argument is less of a concern in the case where the contact hole is fabricated by a negative tone rather than a positive tone process. Since photon shot noise scales with 1/sqrt(#photons), shot noise statistics would favor a brightfield negative tone over a darkfield positive tone process. Indeed, stochastic simulations predict improved local CDU performance for 22nm contact hole structures when printed in EUV with a negative tone instead of a positive tone process.

In this paper, we will compare the local CDU performance of contact holes for both negative and positive tone processes at both ArF and EUV wavelengths. In this way, we will look to quantify the contribution of shot noise to the local CDU performance.

8324-21, Session 6

Scatterometry metrology challenges of EUV

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Extreme ultraviolet lithography (EUVL) offers the most promising patterning technology to be adopted for ultra-deep-submicron devices - 16nm and below. EUV using mirror-based mask with oblique incident angle of light in combination with the small wavelength compared to the mask topography. This causes number of effects that are unique to EUV - such as flare, shadowing and horizontal-vertical (H-V) bias CD offset and an orientation dependent pattern placement error. Increased flare and the shadow effect will decrease the contrast of the aerial image and resulting poor line width control. The H-V bias leads to an ellipticity in the contact hole pattern, CD offset in line space pattern resulting in critical dimension (CD) non-uniformity. The shadowing effects can be corrected by means of OPC and MEEF (reducing the absorber thickness, and/or phase shift concept to improve the image contrast with a thinner absorber stack).

With decreasing grating geometry and increasing demand for metrology of the EUV periodic structures, scatterometry offers diffraction based optical method critical dimensions (CD), side-wall angles, and dimensional characterization. The ability to model complex stacks,

generate libraries rapidly and measure CDs and SWAs of targets with multiple pitch, line width (or contact hole) dimensions precisely and accurately enables scatterometry as indispensable metrology technique. The resolution characterization of EUV structures are often limited by narrow lines/holes, obscure angles and very thin film structures. Scatterometry is rapid, precise, accurate and non-imaging technique capable of measuring CD systemic errors resulting from EUV patterning for 14nm nodes and beyond.

In our previous work, we performed calibration of OPC model with full CD profile data for 2D and 3D1,2 using scatterometry measurements with rigorous coupled-wave analysis (RCWA) approach. In this paper, we will present the CD, sidewall angle and stack characteristics for H-V bias and placement errors of OPC models through focus by scatterometry. We will also report the precision, accuracy and matching parameters of EUV structures.

The spectral response with combined spectroscopic ellipsometry (SE-90) and reflectometry (NI-SR) showed a strong signal with increased sensitivity and improved measurement quality that help resolve the shape variations and derive profile parameters of interest (CD, side wall angle and height) by scatterometry (figure 1 (a) and (b)). The observed offset of 1.12nm for MCD correlation between horizontal and vertical targets (slope=0.97 and R2=0.9) further illustrates H-V bias (figure 2). The effect of CD and pitch variation in horizontal and vertical directions is also examined and the observed MCD variation is plotted in figure 3 (for 32P64, 40P80, and 50P100). OPC targets of varying CD at fixed pitch (64, 80, 100nm etc.) for lines and contact holes is also examined. The observed MCD variation is plotted in figure 4 (for 31P64 - 36P64). The OPC model characterization for the corrected models will be included. The data collection and analysis will be performed on Atlas tool with NISR and SE-90 measurement techniques.

Finally, comparison of CDU systemic variance across various EUV patterning structures by scatterometry will be validated against reference metrology.

8324-22, Session 7

Phase sensitive parametric optical metrology: exploring the limits of 3-dimensional optical metrology

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There has been much recent work in developing advanced optical metrology applications that use imaging optics for critical dimension measurements, defect detection and for potential use with in-die metrology applications. For some time it has been shown that sensitivity to nanometer scale changes can be observed when measuring critical dimensions of sub-wavelength features or when imaging defects below 20 nm using angle-resolved and focus-resolved optical data. There are many advantages to using low cost high-throughput optical tools. However, these methods inherently involve complex imaging optics and analysis of complicated three-dimensional scattered electromagnetic fields. In this paper we will develop rigorous analysis of these data using both theoretical and experimental methods. This includes illumination engineering and sophisticated tool normalization to implement quantitative phase sensitive measurements of the through-focus three-dimensional field data.

This paper will use rigorous electromagnetic simulation tools and statistical methods to evaluate sensitivities and uncertainties in the measurement of two and three dimensional layouts encountered in critical dimension, contour metrology and defect inspection. This presentation will outline a new approach that enables the rigorous analysis of three-dimensional through-focus optical images. These imaging methods sample the three-dimensional electromagnetic fields above the sample or target of interest. The technique involves parametric fitting of the discretized three-dimensional scattered fields and allows for the quantitative evaluation of correlation effects due to fitting parameters such as side wall, feature profile and etch depth. We will evaluate the

possibility of performing dimensional measurements of in-die layouts through imaging and analysis of high order three-dimensional optical fields.

8324-23, Session 7

Investigation of e-beam patterned nanostructures using Mueller matrix based scatterometry

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Title: Investigation of E-beam patterned nanostructures using Mueller Matrix based Scatterometry

Scatterometry is one of the leading semiconductor metrology techniques used extensively for the characterization of critical dimensions (CD) and detailed topography of periodic structures in microelectronics fabrication processes. Spectroscopic Ellipsometry (SE) and Normal Incidence Reflectometry (NI) based Scatterometry are the most widely used methodologies for metrology of these structures. Evolution of better optical hardware and faster computing capabilities led to the development of Mueller Matrix (MM) based Scatterometry (MMS). In this paper we present the first study of dimensional metrology using full Mueller Matrix (16 element) Scatterometry. Unlike SE and NI, MM data provides complete information about the optical reflection and transmission of polarized light through a sample. MM is a 4x4 transformation matrix (16 elements) describing the change in the intensities of incident polarized light expressed by means of a Stokes Vector. The symmetry properties associated with MM provide an excellent means in measuring and understanding the topography of the periodic nanostructures. The advantage of MMS over traditional SE Scatterometry is the ability of MMS to measure samples that have anisotropic optical properties and depolarize light.

The present study focuses on understanding the precision and accuracy of Mueller based Scatterometry with respect to other methodologies by a systematic approach. Several laterally complex nanoscale structures with line widths between 10-60 nm were designed and fabricated using a state of the art E-beam pattering tool (VISTEC® 300). Later, Spectroscopic Mueller matrix (all 16 elements) and SE data were collected at various azimuthal and incident angles for the samples using J.A. Woollam RC2 Spectroscopic Ellipsometer. NanoDiffract (Scatterometry software provided by Nanometrics Inc.) was used to model the nanostructures to precisely calculate the critical dimensions. Statistical analysis was performed to understand the correlation and precision effects of various modeling parameters. Complementary techniques like SEM were used to compare the results obtained from Scatterometry. Finally, Mueller and SE based Scatterometry techniques were compared commenting on reliability of MM based Scatterometry.

8324-24, Session 7

Accurate optical CD profiler based on specialized finite element method

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As the semiconductor industry is moving to very low-k1 patterning solutions, the metrology problems facing process engineers are becoming much more complex. Choosing the right optical critical dimension (OCD) metrology technique is essential for bridging the metrology gap and achieving the required manufacturing volume throughput. The CD-SEM measurement is usually distorted by the high aspect ratio of the photoresist and hard mask layers. CD-SEM measurements cease to correlate with complex three-dimensional profiles, such as the cases for double patterning and FinFETs, necessitating sophisticated, accurate and fast computational methods to bridge the gap. In this work, a suite of computational methods that complement advanced OCD equipment, and enabling them to operate

at higher accuracies, are developed. In this article, a novel method for accurately modeling OCD profiles is presented. A finite element formulation in primal form is used to discretize the equations. The implementation uses specialized finite element spaces to solve Maxwell equations in two and three dimensions.

The computational domain for the optical grating frequently used in OCD measurements is pseudo-periodic (Floquet boundary condition for the field) in lateral axis, and the FEM domain is restricted only to the optical grating profile where the discontinuities in material properties exist in lateral direction. Using Rayleigh expansion for the field outside the FEM domain, specifically in the top and bottom layers, the computational complexity is limited to the optical grating layer. The fictitious boundary conditions, or equivalently transmission conditions, at the top and bottom of the FEM domain are incorporated in to the weak formulation using the Dirichlet-to-Neumann mappings. Although this kind of approach has been used in the pass for optical diffraction gratings, the vector formulation used in this work differs from the literature in the way the boundary conditions is handled. From the numerical point of view, the challenging problem is to handle non-smooth profiles, such as hat shaped patterns.

The results for different CD profiles are presented. FEM computation of ellipsometric parameters corresponding to a given optical grating for transverse electric and transverse magnetic cases is presented. Simulated ellipsometric measurements are compared to the experimental measurements. Although the results for single optical grating profile are presented in this work, the ongoing work is applying the same technique for multi-layer grating profiles such as the ones appearing in double patterning and overlay metrology.

8324-25, Session 7

Coherent Fourier scatterometry: tool for improved sensitivity in semiconductor metrology

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Introduction:

Incoherent Optical Scatterometry (IOS) is a well-established metrology technique in the semiconductor industry to retrieve the shape of periodic grating structure with high accuracy[1]. The grating is defined in terms of finite number of shape parameters (height, pitch, side wall angles, midCD etc). These parameters are determined through experimental measurements that are obtained by illuminating a grating and recording the scattered far field. This far field is then compared with a library of simulated far fields with different set of grating parameters. With shrinking dimensions in the lithography industry, finding possible improvements in wafer metrology is highly desirable.

The use of coherent light as the illumination, under suitable condition can reasonably increase the sensitivity of measurements of grating parameters. We present a framework to study the increment in sensitivity of Coherent Fourier Scatterometry (CFS). We also report an experimental implementation of a coherent Fourier scatterometer, where a focused beam from a spatially coherent source has been used as illumination. The obtained focused spot is scanned over the grating period, and for each scan position, a far field diffraction pattern is recorded. In order to exploit the full potentiality of the coherent illumination, some overlap between two consecutive scan positions has to be ensured. Phase information can also be directly extracted from a series of intensity maps.

Sensitivity analysis: To compare the CFS sensitivity to the current used technique, we compute uncertainties of grating shape parameters with a maximum likelihood estimate[2]. Rigorous coupled wave analysis is used for the forward simulations of the diffracted far field. The difference between the experimental and simulated far field is modeled by chi-square distribution, then we calculate the covariance matrix to calculate the uncertainties of parameters.

Results and conclusions: We define coherent gain as the ratio between uncertainties of coherent and incoherent illumination. A comparison

between coherent gain in midCD of the grating is shown in Fig.1. The wavelength considered in the theoretical analysis is 632 nm and the numerical aperture of the focusing system is 0.4. The parameters of the grating with half duty cycle are height 130 nm, sidewall angles of 90 degrees each and pitch varying from 0.5 μm to 2.5 μm, with only Si grating. Coherent gain is plotted on the vertical axis while the pitch is on the horizontal axis of the figure. The coherent gain is plotted for the different number of scan positions (1, 4 and 12) of the focused spot with in one period of the grating. The incident field is TE polarized, i.e along the grooves of the grating, and at the detector we have coherent superposition of TE and TM fields. The region in the graph where coherent gain is larger than unity corresponds to the higher sensitivity of CFS for the midCD variation. For regions of pitch where coherent gain is unity, we have identical sensitivity for the CFS and IOS, as there is no overlap of diffracted orders. We also observe enhancement in sensitivity with respect to other grating parameters as height and sidewall angles with CFS.

The experimental setup is shown in Fig.2(a), while Fig.(2b) shows the simulated and experimental far field with only Si grating and above mentioned grating shape parameters. He-Ne laser is used as the coherent light source. We characterize the incident electric field with Shack Hartmann wave-front sensor measurements. This field is then used for computation of the simulated diffraction pattern, which is then compared with the experimental intensity maps.

We observe that the use of CFS enhances the sensitivity in grating shape parameters. Under suitable condition the estimated uncertainties on the shape parameter can be four times better then that obtained with conventional incoherent scatterometry.

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8324-119, Session 7

High-speed, full 3D feature metrology, for litho monitoring, matching, and model calibration with scatterometry

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We studied the potential of optical scatterometry to measure the full 3D profile of features representative to real circuit design topology. The features were selected and printed under conditions to improve the measurability of the features by scatterometry without any loss of information content for litho monitoring and control applications.

One of the means to enhance measurability is shape control. Scatterometry requires a measurement model with sufficient degrees of freedom to describe the feature and its full variability. It is well known that the shape of the printed features can be controlled applying simple rule-based compensation of feature shape at reticle level to improve its profile at the imaging resolution limits. This allows use of a simple measurement model with a minimum amount of free parameters in the scatterometry recipes. The other measure that enabled accurate full profile characterization relies on the fact that the sensitivity of the scatterometer increases with the density of the printed pattern. By proper selection of feature topology, with a high repetition rate in both direction the measurability was improved

We have applied this strategy on a variety of structures for 28 to 20nm nodes, and gathered results using the YieldStar angular reflection based scatterometer. The reported results show that we obtained effective decoupling of the measurement of the 3 dimensions. The results are consistent with predictions by calibrated lithographic simulations.

8324-59, Poster Session

Experimental approach by using CD-SEM to directly measure primal photoresist shrinkage

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We found experimental procedures to directly measure primal shrink caused by CD-SEM measurement.

In CD-SEM measurement of photo-resist line patterns we cannot directly measure original linewidth, because electron beam of SEM causes immediate shrink, said here as 'primal shrink', in the photo-resist materials. To estimate the original linewidth, we extrapolate from shrink curve that can be created from subsequent measurements on the identical measurement-point.

In this work we tested experimental procedures to directly measure the primal shrink by using only CD-SEM and overcoating photo-resist sample. The procedures are for instance: (1) measure linewidth of a photo-resist pattern by CD-SEM, (2) deposit several-nanometer-thick overcoat layer on the photo-resist, (3) measure linewidth at the measured part and at adjacent part, (4) subtract the linewidth at the measured part from that at the adjacent part.

The subtracted value indicates the primal shrink, if the overcoat layer protects and preserves the inside photo-resist against the second CD-SEM measurement. The linewidth that remain after the subtraction is independent on the overcoat thickness.

We found the least thickness to protect the inside photo-resist is about three to four nanometers, which is thin enough to dense lines created by recent fine processes. The results were verified by measurements of atomic force microscopy (AFM).

The merits of these procedures are: (1) practically easy and useful because we need only CD-SEM and the overcoat process that are both available in device manufacturing line, (2) sub-nanometer-accurate as well as CD-SEM's accuracy because we use no mathematical estimation or approximation.

8324-60, Poster Session

Defect distribution study at through silicon via (TSV) bottom by scanning white-light interference microscopy

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Many commercially important devices in semiconductors and flat panel displays etc. are composed of thousand kinds of pattered materials and their metrology is one of key parts of the manufacturing process control for these devices. On Dec, 7th, 2010, Samsung Electronics announced a successful development of 8GB DRAM module with 3D-through silicon via (TSV) technology, ie. Samsung Electronics successfully developed 2-stack 4Gb chip by 2Gb DRAM 3D-TSV technology, and completed qualifications test on customer's server in Oct 2010. However, in the manufacturing point of view, metrology and defect detection at via bottom are still hot issues of the process control.

Unifire 7900 (Nanometrics Inc.) is one of the scanning white-light interference microscopy which can be configured to measure critical dimensions (CDs), film thickness and do simultaneous measurement of CDs and depth of via and it satisfies many requirements for TSV high volume manufacturing - non-contact, non-destructive, quantitative 2D and 3D imaging, high throughput sampling.

In this study, defect distribution at TSV bottom has been studied by using Unifire 7900. Several kinds of via bottom conditions should be sorted by shapes and radius of curvature, and via etching conditions will be organized by TSV depth measurement as well.

8324-61, Poster Session

A scatterometry-based CD uniformity control solution for spacer patterning technology

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Improving Critical Dimension Uniformity (CDU) for spacer double pattern features is a high priority for double patterning technology. In spacer double patterning the gaps between the spacers are established through various processes (litho, etch, deposition) with different process fingerprints and the CDU improvement of these gaps requires an improved control solution. Such a control solution is built upon two pillars: metrology and a control strategy.

First, the metrology parameters of interest, CD and shape of the gaps and the spacers, need to be measured accurately, precisely and promptly in order to optimize CDU performance in a control loop. Scatterometry tools are becoming an alternative to the traditional metrology tool CDSEM to achieve this goal. Scatterometry, however, requires a measurement model that is capable to characterize the parameters of interest of the spacer double patterning gratings, as well as deal with variations and uncertainties in thickness and material properties of the underlying layers.

Second, the control strategy relies on using a well controllable fingerprint in order to compensate for a less-controllable fingerprint and achieve optimal CDU for the parameters of interest. In particular the impact of deposition or etch fingerprints on the CDU of the gaps can be reduced by proper control of the lithography fingerprint.

In this technical presentation Spacer Patterning Technology CDU control using an angle resolved scatterometry tool will be evaluated. CD results obtained with this scatterometer on FEM and CDU wafers will be measured and the results will be correlated with those from the traditional CDSEM. CD wafer fingerprints will be compared before and after applying the advanced control strategy and CDU improvements for both metrology tool types will be reported.

8324-62, Poster Session

Design-based SEM recipe generation for OPC and manufacturing applications

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Metrology requirements for OPC modeling and verification have increased substantially over the past few years. This is partially due to process lithography being driven to deep sub-wavelength imaging, but is also due to the need to capture formerly second-order phenomena such as 3D mask effects. CD-SEM vendors offer offline SEM recipe creation tools to increase CD-SEM throughput, but the process of defining a SEM recipe is largely unchanged and engineer time requirements are only slightly decreased.

We present a solution for improving engineer efficacy using software tools to move regular manufacturing Hot Spot Metrology and OPC-related SEM recipe choices into the OPC environment. Enabling metrology-related decisions at this stage allows the following benefits:

1. Test pattern DOE-centric measurement selection, including automation of complex algorithms measurement selection

2. Modeling engineer can select wafer fields and die to measure to meet process coverage and statistical repeatability requirements

3. Modeling engineer can choose measurements even if another engineer loads and executes the recipe on the SEM

4. Immediate feedback on ability of SEM to take the requested measurement

5. Closed loop feedback, loading metrology data automatically into the model

These software tools have been developed in coordination with SEM vendors to ensure that information is passed smoothly between the OPC environment and the offline SEM recipe creation tools. In addition, not all SEM recipe information must be provided in the OPC environment. Decisions that are typically driven by the SEM engineer can be ignored with no negative impact.

This paper will demonstrate how these software tools work with offline SEM recipe software to enable a metrology ecosystem that maximizes OPC engineer control and efficiency saving valuable SEM tool time. We will assess how well each of the expected benefits is realized and discuss how to integrate these tools into a full workflow environment to maximize the benefits.

8324-63, Poster Session

Small particle defect characterization on critical layers of 22nm spacer self-aligned double patterning (SADP)

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Spacer Self-Aligned Double Patterning (SADP) is one of the leading patterning approaches used to extend the half-pitch limit of a lithography platform. SADP uses CVD spacers formed adjacent to core patterns which serve as hardmask after the core material is stripped - doubling the line density. It is currently used for memory devices but has the potential for application to logic design style Gridded Design Rule (line/space at constant pitch) and logic devices.

Each SADP process step, Lithography, Deposition and Etch, poses a risk to yield due to small particle contamination. Reducing this risk requires a systematic approach to understanding small particle defect sources and their impact on each subsequent process step. With this knowledge, inspection strategies can be developed for each module.

The SADP process flow developed by the Maydan Technology Center, based on immersion Lithography, will be used. Four modules have been identified for the SADP process for small particle defect characterization; Lithography, APF Etch, Spacer Deposition, and Spacer Open. In order to determine the best inspection strategy, wafers from these modules will be inspected using DFinderTM, a DUV laser based DarkField wafer inspection platform and UVision 3TM, a BrightField wafer inspection platform. Inspection recipes will be optimized for small particle (3D) detection. Simulation and modeling will be performed on small particle defects to evaluate the capability of the DarkField inspection platform. Each particle detected at the preliminary step of the SADP process will be traced and reviewed along the remaining steps in order to characterize the defect for defect source analysis. It will also enable better capture of the critical defects at earlier process stages. Based on the results, an optimized mix of inspection strategy will be recommended.

8324-64, Poster Session

Integration and automation of DoseMapper in a logic fab APC system: application for 45/40/28nm node

B. Le-Gratiet, STMicroelectronics (France)

Since few years now we have been presenting some papers regarding logic gate CD dispersion analysis along with DoseMapper corrections. We talked about CD budget ("Process Control for 45 nm CMOS logic gate patterning " - B. Le Gratiet et al. SPIE2008; 6922-33), then we have been focusing on Intrafield CD corrections using Dose Mapper ("Intrafield Process Control for 45 nm CMOS logic patterning "- B. Le Gratiet SPIE2009; 7272-107). The work continued through the evaluation of Dose Mapper Dose Recipes creation before the first silicon is coming, also talking about embedded metrology targets and mask CD correlation to silicon ("Improved CD control for 45/40nm CMOS logic patterning. Anticipation for 32/28nm", B. Le Gratiet et al. SPIE2010, 7638-9)

The main difficulty related to DoseMapper correction is to generate an appropriated CD datacollection to feed DoseMapper and to generate DoseRecipe in a user friendly way especially with a complex process mix.

One can choose to heavily measure the silicon and create in feedback mode the corresponding DoseRecipe. The problem with such approach in a logic fab is that it will become a heavy duty due to the number of different masks / product / processes. We have then chosen for a feedforward approach, looking for systematic CD footprints that can be seen and applied has generic pre-correction for any new product/mask process in-line. The DoseMapper correction we apply on the lot in ST Crolles is based on a CD (intrafield: Mask + Straylight & intrawafer: Etch Bias) variability "model" handled by the FAB APC.

Individual CD profile correction component are generated "off-line" (1) for Intrafield Mask via automatic CD extraction from a Reticle CD database (2) for Intrafield Straylight via a CD "model" (3) for Intrawafer Etch Bias via engineering input based on process monitoring.

These CD files are handled via the FAB APC/automation system which is remotely taking control of DoseMapper server via WEB services, so that CD profiles are generated "off-line" (before the lot is being processed) and stored in a profile database while DoseRecipes are created "in-line" on demand in real time via the automation when the lot comes to the scanner to be processed. DoseRecipe and CD correction profiles management is done via the APC system.

The automated DoseRecipe creation is now running since the beginning of 2011 contributing to bring both intrafield and intrawafer GATE CDu below 1nm 3sigma, for 45/40 & 28nm nodes.

8324-65, Poster Session

Recess gate process control by using 3D SCD in 3xm vertical DRAM

C. Wang, KLA-Tencor Taiwan (Taiwan)

As DRAM design changing continues form planar to vertical one. Recess Gate Process control caused by etching process after patterning is very critical because it will affect device electrical characteristics and furthermore affect yield. 3D Scatterometry Critical Dimension (3D SCD) technology now is wildly used in metrology measurement for process control at CMOS and DRAM in the IC industry.

In the paper, latest 3D SCD combined with feature of date feed forward and pass strategy were used to in the 3D model and calculation. Recess Gate measurement in the cell area can be measured and confirmed with Cross-section of Scanning Electron Microscope (X-SEM) measurement successfully.

8324-66, Poster Session

Apply multiple target for advanced gate ADI critical dimension measurement by scatterometry technology

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The scatterometry-based measurement method for advanced gate ADI and AEI layer structure has been proven in the lots of papers. This paper describes the CD and WA measurement accurate challenges and currently approaches for advanced gate ADI structure. Second, KLA-

Tencor SpectraShape8810 with Multi-Target measurement and AcuShape model software with multi-target library used to measure the critical parameters; Use multi- target to control both of CD and WA to monitor exposure tool. CDSEM are used as a reference metrology to assess the CD accuracy performance of SpectraShape8810. For WA parameter is relative exposure focus is the key fact that is not have accurate reference tool for evaluate. We use the focus matrix to explore the relation between WA with scattermtery-based measurement.

A lot of papers demonstrate that scattermetry-based measurement method is the more accuracy than CDSEM in CD value for FEOL gate ADI layer. We found the characteristic that dense line layout is the best scattermetry-based measurement to do in-line monitor expose tool energy process CD value variation. The other isolate line layout is the best scattermetry-based measurement to do in-line monitor expose tool focus process WA value variation.

First, the paper describes the CD and WA parameter metrology challenges by using scatterometry-based measurement that WA correlate HT and CD in the lower resist profile. The best approach method implement SCD measurement is break correlation by different strategy like as API/DFF and MPM technology. We find the new strategy naming multi- target technology can break correlation between WA with CD and HT well.

Second, the brand-new scatterometry KLA-Tencor SpectraShape8810 was used to measure the critical parameters. CDSEM is used as a reference metrology to assess the accuracy performance. The SpectraShape8810 can use multi- target library was provided by AcuShape software and also can separate dense and isolate line layout mean multi target measurement to monitor CD and WA well simultaneous. We did several evaluations in the different multi target combination to know the best benefit for mass production and find the best repeatability and stability.

The author have a lot of experience on the FEOL layer in the logic device below the 40/28 nanometer node by using SCD tool to measure gate ADI layer. SCD tool have proven on the in-line APC control system to improve process variation compare to traditional CDSEM tool. This paper proving the SpectraShape8810 tool is working on the in-line monitor for expose tool CD and WA measurement. In the future SpectraShape8810 tool will help on the research development and production ramp up process control.

In summary, SpectraShape8810 can achieve advanced generation below 40/28 nanometer node gate ADI PR CD and WA measurements even with lower resist profile. The ADI result will provide data to APC in-line system can reduce gate AEI CD variation and let late implementation process enhance device performance.

8324-67, Poster Session

Fast and accurate scatterometry metrology method for STI CMP step height process evaluation

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This paper discusses the Scatterometry-based measurement method for critical dimension step height of STI CMP layer instead of traditional measurement tool like as AFM. First, the paper statement what is critical parameter for STI CMP layer and discusses current measurement method might be uncertainty in mass production of logical devices below node 40 nanometer. Second, KLA-Tencor AcuShape software go to do analysis what is best incident Azimuth angle and create the best floating parameter library then KLA-Tencor SpectraShape8810 is used to measure the critical parameters and get the best TMU result. AFM and TEM are used as a reference metrology to assess the accuracy performance of the SpectraShape8810.

For drive and maintain device performance a lots of IC maker foundry

spend huge monitor step to control chip making flow. In FEOL STI step that need to keep STI CMP layer step height control to avoid the next step process won't smoothly and keep device stress well control. IC maker integration spent a lot of effort to control this key parameter step height by using TEM and AFM measurement tool.

First, the paper discusses the TEM and AFM are in the higher cost and measurement might be has uncertainty error. TEM need to cut a lot of many wafers that did the higher cost. AFM tool is simple tool and can measure this kind of step height parameter but it measurement error is high and it result is also depend on the tool operation. This layer must to have a new measurement method to reach process control requirement.

Second, the brand-new scatterometry KLA-Tencor SpectraShape8810 was used to measure the critical parameters of STI CMP layer. AFM and TEM are used as a reference metrology to assess the accuracy performance. The SpectraShape8810 extended wavelength range down into the deep UV (DUV) and enhanced ultra violet reflectivity (eUVR) can provide a noticeable improvement in measurement accuracy due to the significantly greater parameter sensitivity in this wavelength range. This paper showing the result of the Scatteromerty metrology method can provide best repeatability and stability in the mass production of logic devices below node 40 nanometer.

The author have a lot of experience in the FEOL layer CMP process on the node 40/28 nanometer device by using SCD tool to measure STI SIN-REM and CMP layer. SCD tool have been proven on the in-line monitor control system to improve process variation compare to traditional AFM and CDSEM tool. This paper proving the SpectraShape8810 tool is working on the productivity of the STI CMP layer. In the future SpectraShape8810 tool will help on the research development and production ramp up process control.

In summary, SpectraShape8810 can achieve STI CMP step height measurements. The result will provide data to feedback process CMP system can reduce step height process variation. SpectraShape8810 provides fast and accurate measurement result to reduce cost and reply soon process variation to control well process result that make next step process will be more smoothly and enhance device performance and wafer yield.

8324-68, Poster Session

Diffraction-based overlay measurement on dedicated mark using rigorous modeling method

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We propose an alternative DBO technology using a dedicated overlay mark and rigorous modeling. The mark consists of three contiguous pads. Pad I has a lower grating layer fabricated by former processes, all other layers are films; pad III has an upper resist grating layer with all other layers being films. Both resist grating and lower grating layer extend to pad II. In pad II, the two grating layers are separated by some intermediate layer(s), such a structure is same as an empirical DBO pad. The resist grating layer has a pitch/4 pre-offset to the lower grating layer, so one pad is enough to determine both amount and direction of overlay provided overlay is less than pitch/8. Measurement is performed on pad I, pad II and pad III successively to obtain diffraction signals. Using scatterometry technologies, structure parameters are extracted for pad I and pad III. Since both pad I and III have only one grating structure, much fewer unknown parameters should be extracted. Such a measurement has proved to be highly precise and accurate. Grating structures in pad II is same as their counterparts in part I and III, so there is only one unknown parameter in pad II, overlay ε. Rigorous model can be set up for pad II with measured structure parameters. By varying overlay in this model, different diffraction signals can be calculated. Overlay is determined when calculated signal fits signal measured on pad II best.

8324-69, Poster Session

Contamination control: removing small particles from increasingly large wafers

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Semiconductor manufacturers continue to push for smaller and cheaper devices, following a trend that has become known as Moore's Law. In order to maintain this trend, critical dimensions of devices shrink while at the same time wafer size increases. The scale-up of semiconductor wafers is necessary to reduce the manufacturing costs: the same process steps produce roughly twice as many components when wafer size is increased from 300 to 450 mm. European OEMs are busy developing their equipment and processes in line with this trend. Part of the development takes place in the "European Equipment & Materials Initiative for 450 mm" (EEMI450), a European project coordinated by ASMI under the ENIAC research program. Within this European project, TNO is responsible for addressing contamination control issues.

With shrinking line width and increasing wafer size contamination is becoming an issue for reliability and yield. Cross contamination from back side to front side can cause yield losses and carry over to clamps may cause overlay problems. Particles on the back side can cause wafer bending during the lithographic step and in metrology processes. Within the EEMI450 project, TNO has built a set-up to remove contamination from the backside of wafers. The aim of the study is to show the feasibility of such a cleaning system in a cluster tool without affecting the throughput of such a tool. Experiments are planned to study the efficiency of a combination of three cleaning techniques. Sticky rollers, RF plasma and strong electric fields all work together to remove both organic and inorganic particles and molecular contamination layers. In this presentation, we will report on the design and experimental results of this cleaning unit.

8324-71, Poster Session

Overlay accuracy improving device: Qmerit

G. Cohen, E. Amit, D. Klein, D. Kandel, V. B. Levinski, KLA-Tencor Israel (Israel)

As overlay budget continues to shrink, an improved analysis of the different contributors to this budget is needed. A major contributor that was never quantified is the accuracy of the measurements. This accuracy stems from the response of the measurement system to target asymmetry, and its theoretical origin is described elsewhere.

While the accuracy concept is theoretically interesting, the true benefit of its analysis can be realized only if a practical tool is established, that identifies excess asymmetry, and even better, correct the OVL result using this information. KLA-Tencor developed such a tool, titled Qmerit, that calculates and attaches an accuracy value to each OVL value. This operation is performed on the fly during measurement without affecting MAM time or throughput. To show the benefits of such a tool, one must prove that indeed the quality values supplied by the Qmerit matches an independent measurement that can be trusted. The fact that no tool is capable of measuring the sub-nanometer regime in discussion makes it even tougher. Using linearity array we demonstrate that the Qmerit identifies targets deviating from the intended OVL value, with no false alarm.

8324-72, Poster Session

Weighted least squares regression for advanced overlay control

J. C. Robinson, KLA-Tencor Corp. (United States); D. Klein, G. Cohen, KLA-Tencor Israel (Israel); C. K. Huang, B. Pierson, KLA-Tencor Corp. (United States)

Controlling overlay performance has become one of the key lithographic challenges for advanced integrated circuit (IC) manufacturing as the industry pushes to 3x and 2x nm nodes. Improved overlay control includes advances in lithographic exposure systems, overlay metrology, and overlay control schemes. Overlay control methodologies include modeling of overlay errors based on schemes which have advanced significantly in recent years. For the most part overlay data modeling is based on ordinary least squares (OLS) regression, which assumes that each data point provides equally reliable information about the process variation. This assumption, however, is not valid in every modeling situation and is typically dealt with by using flier (or outlier) removal methods based on metrology quality metrics, data values outside an expected range, or how well data points fit applied models. Reliable flier removal methods are an important part of advanced overlay process control, however, data points are categorized as either "good" or "bad" for a particular purpose without any way of attributing gradations of accuracy or precision to a given measurement. Weighted least squares (WLS) regression can be used to improve overlay modeling by giving each data point an amount of influence on the model which depends on its quality or precision. The ability to perform regression analysis in situations in which the data is of varying quality, in conjunction with advanced flier rejection methods, can provide the most precise parameter estimation possible. One scenario for WLS would be the incorporation of small in-die target data with larger high-precision target scribe-line data. Another scenario would be to take advantage of the considerable information content of imaging overlay metrology to estimate quality of each measurement. This paper discusses multiple applications of WLS methodologies to improve overlay process control.

8324-73, Poster Session

Toward faster and better litho-control in high-volume manufacturing

C. Huang, C. Chiu, W. Wu, C. Shih, Nanya Technology Corp. (Taiwan); J. Manka, KLA-Tencor Corp. (United States); C. H. Huang, KLA-Tencor Taiwan (Taiwan); D. Choi, KLA-Tencor Korea (Korea, Republic of); A. Lin, KLA-Tencor Taiwan (Taiwan); D. Tien, KLA-Tencor Corp. (United States)

As the cost of manufacturing high-end semiconductors continues to increase, the value of combining and streamlining metrology steps also increases. The two critical metrology steps for litho control are 1) CD and 2) overlay. In this study, the authors demonstrate the capability of just such a combo CD and Overlay metrology solution to improve not only the cost of manufacturing but also the quality of data and information feedback for better scanner control in high volume production.

For overlay, the need for fine-segmentation is critical to meet the requirements of advanced process nodes, especially for critical layers with advanced illumination conditions. Imaging overlay technology continues to be the best suited metrology technique to robustly measure such target designs. More specifically, since fine-segmentation is limited by lithographic optical conditions (NA, sigma, illumination pupil shape), it is important that the metrology system be flexible enough to encompass the range of dimensions that are sensitive to these lithographic effects. If fine-segmentation is applied without regard to lithographic conditions, the resulting non-optimal target structures may either be insensitive to the desired lithographic effects (pattern placement errors), or even worse, may be unprintable on the wafer (and therefore unmeasureable).

For CD, the need for better precision and more sampling to meet the requirements of smaller design rules continues unabated. Scatterometry technology with its fast throughput and proven performance has been well established as a common metrology solution for CD control. The combination of scatterometry technology for CD metrology with imaging technology for overlay metrology on a single platform now enables both CD and overlay to be monitored at the same metrology step in the process, allowing faster time to results, less wasted time waiting for overhead lot transfer, and more information for better and more accurate scanner control in production.

In summary, the authors will demonstrate how using imaging and scatterometry technology on a single platform can provide a

comprehensive litho control solution for both CD and overlay in the litho module. In the study, the authors will use full stack wafers from an advanced process node running in high volume manufacturing, Specifically, data will be generated using PROLITH for lithographic simulations for optimal target designs and then empirical data will be collected using the Archer 300LCM from which optimal target selection and system performance will be determined and validated on wafers using this advanced process technology.

8324-74, Poster Session

Overlay control methodology comparison: field-by-field and high-order methods

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Overlay control in advanced integrated circuit (IC) manufacturing is becoming one of the leading lithographic challenges in the 3x and 2x nm process nodes. Production overlay control can no longer meet the stringent emerging requirements based on linear composite wafer and field models, based on sampling 10 to 20 fields and 4 to 5 sites per field, which were the industry standard for many years. Methods that have emerged include overlay metrology in many or all fields, including the high order field model method called high order process control (HOPC), and field by field control (FxFc) methods called correction per exposure (CPE). The FxFc methods were initially introduced as relatively infrequent scanner qualification activities meant to supplement linear production schemes. More recently, however, it is clear that production control is also requiring intense sampling, similar CPE methods, and HOPC. The added control benefits of CPE and HOPC overlay methods need to be balanced with the increased metrology requirements, however, without putting material at risk. Of critical importance is the proper control of edge fields, which require intensive sampling in order to minimize signatures. In this study we compare various methods of overlay control with respect to benefits, costs, and risks.

8324-75, Poster Session

CD-SEM and e-beam defect inspection of high-aspect ratio contact holes: measurement and simulation of precharge

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At feature sizes below 45 nm, contact holes are the most difficult fabrication steps; an aspect ratio higher than 1:10 is required. At this aspect ratio, SEM metrology and electron beam defect inspection face extreme difficulties because secondary electrons from the bottom of the contact holes are absorbed by the walls and do not reach the detector. One solution is to pre-charge a large area before taking images of the hole. Understanding of the physics involved in contrast formation and optimization of the system setup are important in order to enable metrology and inspection. Experimental and simulation results of e-beam defect inspection and CD-SEM of the contact holes using the flood beam are presented.

Pre-charge and imaging were simulated using CHARIOT Monte Carlo software. The physical model includes generation of secondary electrons, accumulation of charge, several discharge mechanisms, electron trajectories in the created local electrical field, and detector properties. Pre-charge and observation conditions were varied. It was found that at certain parameters in the e-beam setting, image contrast is sufficient for metrology of the defect inspection. The simulations involved high

aspect ratio contact holes without defects and with two types of defects: with the remaining under-etched layer at the bottom, and with a particle defect at the bottom. The thickness and size of the defects were on the order of a few nm. Experimental results of e-beam defect inspection and CD-SEM of the contact holes using the flood beam are presented. Simulation results qualitatively agreed with the measured data.

8324-77, Poster Session

Multilevel overlay techniques for improving DPL overlay control

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The motivation for this paper is based on improving DPL overlay control in face of the high complexity involved with multi-layer overlay requirements. For example, the DPL-2nd-litho layer will need to achieve tight registration with the DPL-1st-litho layer, and at the same time, it will need to achieve tight overlay to the reference-litho layer, which in some cases can also be a DPL layer. Of course, multi-level overlay measurements are not new, but the combination of increased complexity of multi-DPL layers and extremely challenging overlay specifications for 20nm node together will necessitate a better understanding of multi-level overlay control, specifically in terms of root cause analysis of multi-layer related overlay errors and appropriate techniques for improvement

In this paper, we start with the identification of specific overlay errors caused by multi-layer DPL processing on full film stack product wafers. After validation of these findings with inter-lot and intra-lot controlled experiments, we investigate different advanced control techniques to determine how to optimize overlay control and minimize both intra-lot and inter-lot sources of error. A new approach to overlay data analysis will also be introduced that combines empirical data with target image quality data to more accurately determine and better explain the root cause error mechanism as well as provide effective strategies for improved overlay control.

8324-79, Poster Session

Process monitoring by measuring bias-free LER on EUV lithography

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Measurement conditions and methods used in CD-SEM for line edge roughness (LER) and line width roughness (LWR) were optimized for photo-resist line patterns processed with extremely ultra violet (EUV) lithography, because measured LER is strongly dependent on measurement parameters such as smoothing and/or summation of pixels on SEM image. The best combination is standard LER-measurement conditions and Bias-Free method, as explained in followings.

The standard LER-measurement conditions are height of measurement box-cursor set at 400 pixels and vertical magnification set at 52,700. Also sum-line-per-point is set at 2 pixels. In these conditions sampling-point interval is 10 nm and sampling-area is 2000nm in longitudinal direction.

In the conventional LER-measurement conditions, height of box cursor is set at 300 pixels and vertical magnification is set at 150000. Also sum-line-per-point is set at 16 pixels. In these conditions, sampling-point interval is 16.9 nm and sampling-length is 540 nm in longitudinal direction.

The Bias-Free method can minimize LER bias, that is to say, false increase caused by random image-noise. The Bias-Free method was used on SEM image taken in the standard LER-measurement.

In combination of the measurement conditions and methods, the standard conditions with the Bias-Free method indicated the best sensitivity to focus change of the lithography. Repeatability was improved with the Bias-Free method because the random image-noise causing data fluctuation can be minimized. On the other hand, line width did not indicate significant change against the focus change. The results were verified with atomic force microscopy (AFM).

8324-80, Poster Session

The root cause of ArF resist CD shrinkage induced by defect inspection

P. Kuo, United Microelectronics Corp. (Taiwan)

For our first impression, defect inspector is considered to be a non-destructive equipment in an advanced Fab. When doing ADI inspection, only defect check is performed and photoresist keeps the same without any physical or chemical change. But is this true for now? I don't think so. Many phenomena or evidences tell us - in advanced processes, defect inspection does play more at the inspection step than what we expected before. Inspection can no longer be regarded as non-destructive. Some thing really happens when ADI inspection is executed. As a result, product suffers yield drop eventually. In the experiment below, different ArF resists among various processes are tested and investigated. Some ArF resists do react on UV light and contraction occurs. Basic studies and experiments based on our limited resources, equipment and time are carried out. We try to find out the mechanism and prove it.

From the absorption spectrum of ArF resist, we know that light is absorbed at a quite wide bandwidth, not only at 193nm wavelength.

By 248nm PEB shrinkage plot, we prove that PAG is triggered by UV light to deliver proton and then proceed acid catalyze de-protection reaction. Since CD shrinkage behavior follows Leaving Group character, therefore different LGs deliver different shrinkage level and lead to distinct ADICD output.

8324-81, Poster Session

The study of high-sensitive and accurate metrology method by using CD-SEM

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The earliest semiconductor device manufacturing employed optical microscopes for measurement and control of the manufacturing process. The introduction of the Critical Dimension Scanning Electron Microscope (CD-SEM) in 1984 provided a tremendous increase in capability for process monitoring and has been the standard for in-line metrology for over 25 years. The advantages of the CD-SEM are highly accurate and stable measurement reproducibility at very specific locations throughout the device. The evolution of the CD-SEM in Metrology has included improved resolution, development of advanced measurement and pattern recognition algorithms, all required by performance improvement demands from the market.

Current conventional metrology using the in-line CD-SEM involves measuring about ten points per wafer (one point per one chip). at a magnification of over x150k(Field of View is about 1μm2). In contrast, the area of measurement pattern on chip is much larger than the area of CD-SEM measurement (mm2 : (on chip) versus μm2 : (CD-SEM measurement)). This would mean that the result of the CD-SEM measurement is influenced by local pattern variation.

The very stringent requirements placed on in-line Metrology for the last couple of technology nodes has produced an additional metrology methodology, beyond the CD-SEM, that involves large area measurements with very high precision for the most critical levels. We will refer to this methodology as "Macro Area Measurements".

We reported the applicability of using a CD-SEM Macro Area

Measurements methodology in SPIE2011(7971-77). In the results, we were able to validate a new methodology that we called "Macro Area Measurement" which is demonstrated to successfully detect small process variations with the same throughput and reduced damage to the pattern.

This time, we investigated the additional applicability of using a CD-SEM Macro Area Measurement methodology in this paper.

The areas investigated focused on the following points:

1) Measurement repeatability related to CD-SEM measurement.

2) Optimization of the measurement parameters using new function.

3) Verification of Macro Area Measurement with a leading -edge device.

In the results, we are able to validate "Macro Area Measurements methodology which is demonstrated to successfully detect further small process variations with the almost same throughput and reduced damage to the pattern.

8324-82, Poster Session

Nanoemitter: ultra-high-resolution electron source for CD metrology

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Nanoemitters are a promising replacement for electron sources in producing field emission CD-SEMs and CD-TEMs. Due to their cold emission characteristics and atomically sharp tip radius, they show drastically improved resolution, especially at large working distances as required in, e.g. cross-beam systems. So far, nanoemitters have been fabricated by CNTs or nanowhiskers of conductive materials. However, none of these methods have been successfully applied in reliable, larger scale manufacturing.

Here, we present a new method to manufacture nanoemitters using electron beam induced processing (EBIP) - a method well established in the nanofabrication of supersharp probes for scanning probe microscopy - and show their unique performance.

Functional nanoemitters consists of a core made of high dense, diamond like carbon (HDC/DLC), which defines the desired aspect ratio and tip sharpness of typically 1-2 nm, and a highly conductive coating of typically 0.1-10 nm thickness.

With this technique, we can easily batch fabricate nanoemitters of desired sharpness, shape, mechanical stability and conductivity. These nanoemitters can easily be implemented into existing SEMs and TEMs.

More than 500 functional nanoemitters have been made so far. Nanoemitters have been operated for more than 5.000 hours in different standard CD-SEMs without any sign of degradation. Thereby a beam current of 3 μA was achieved and stayed comparatively constant, with maximum current oscillations of 10%, and < 3% over a time span of several minutes, respectively.

Due to its cold operating temperature and small tip radius, the resolution improved up to 50% compared to a standard Schottky thermal field emitter. The improvement becomes even more obvious at low kV and large WD. A typical Fowler-Nordheim behaviour for field emission nanoemitters is observed.

8324-83, Poster Session

Carbon contamination removal in larger chambers with low-power downstream plasma cleaning

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There is a need for pristine vacuum environments free of carbon contamination in many lithography tools. Carbon is a particularly irksome contaminant due to its ubiquity and its reactivity with energetic electron or EUV photon beams. When residual hydrocarbons land on a surface

that is being impinged by an energetic beam, they will crack and reform as less mobile deposits. Carbon buildup cause loss in image resolution resulting in line width measurement increases during multiple CD-SEM scans, and on EUV optics it can lead to lower reflectivity and throughput of a lithography system.

A new downstream plasma cleaner has been developed to clean larger chambers at lower pressures and higher RF plasma power (50W) and operates efficiently with current turbomolecular pumps. Cleaning rates can be measured by using a quartz crystal microbalance (QCM) with its surface previously contaminated with hydrocarbons. Rates have been measured at over 1 nm/minute at a distance of over 0.5 m from the plasma source. The cleaner can be used with room air, oxygen gas mixtures, and hydrogen gas. Although it is slightly larger than the currently available Evactron® De-Contaminator, it still has a compact footprint which allows it to be easily installed on lithography tools. This paper will explore the operation of the new plasma cleaner, examining the effect of the cleaning rate due to changes in various conditions including power, pressure, flow, gas mixture, and distance from the plasma source.

8324-84, Poster Session

Applying design data to improve inspection tool recipe creation

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Background: High-end wafer inspection sensitivity and high throughput requirements, together with the increased die layout complexity of advanced products, have imposed new challenges to wafer inspection optimization. A significant fraction of BF inspection tools recipe creation time for advanced products, is typically allocated to defining the die layout, including the different area types. One of the basic area types that are defined are the memory areas within the die. Memory areas, characterized as having repetitive patterns or arrays, are preferably inspected in a cell-to-cell mode, to provide both higher detection sensitivity and higher inspection throughput. During recipe creation, when defining the die layout, array areas are identified and defined by the tool operator, as shown in Fig. 1. This process is typically lengthy and exhaustive. Hence, in advanced products, due to the large number of array areas and their distribution across the die, the operator may not be able to identify and define them all. This in turn leads to reduced inspection sensitivity on array areas that were not defined as arrays and are inspected in a die-to-die mode.

In this work, we present results of an automated tool, developed to systematically identify and define all the array areas within the die, replacing the current lengthy and non-systematic manual process. The new tool is based on analysis of design data, to identify the different area types. Using the new tool, array areas are automatically identified, filtered according to the specific inspection tool and fab requirements, and grouped according to their cell size and pattern characteristics. The information on the automatically identified and defined array areas is in turn transferred to the inspection tool and serves as part of the recipe.

Results: Complex layout dies, which typically require 3 day shifts of tool time to fully define the die layout for optimized inspection, were defined automatically, using the new automated tool, in less than 2 hours. A significant improvement of the recipe creation time was demonstrated, as well as higher sensitivity.

Conclusions: Design data can be used, when integrated into an inspection tool recipe creation flow, to both reduce the recipe creation time and improve the inspection sensitivity.

8324-85, Poster Session

An improved technique for measuring LER and LWR

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With the continued shrink of semiconductor devices, line edge roughness (LER) and line width roughness (LWR) have more impact on device performance than ever before[1][2]. The most important process step which to control roughness is lithography because the roughness in the resist profile is the origin of roughness at post etch. However, it is not certain which part of the resist profile, for instance roughness on the top or bottom of the resist, is actually transferred.

Conventional CD-SEM metrology makes use of frame averaging, typically in the order of 16 or 32 frames, in order to obtain high enough signal to noise ratio. In the case of resist, this could result in inaccurate representation of LER/LWR, due to shrinkage. In this work we propose an alternative method to frame averaging which uses enhanced image processing on only a single frame, to minimize this shrinkage. We believe that by using this technique, a better understanding of LER/LWR can be achieved and the impact of LER/LWR and its transfer from litho to etch better assessed. Additionally a metrology friendly design is described and used which enables the step by step transfer of LER/LWR through the process to be studied. These results were analyzed using spatial frequency distribution[3] and compared to AFM as a reference.

8324-86, Poster Session

An attempt to build an OPC model using yieldstar metrology

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Line end gap measurement for OPC calibration is a challenge for metrology. Even for CD-SEM, the rounding shape of the line end makes it very difficult to measure precisely. We have presented preliminary results of the application of scatterometry to these challenging structures using an angle resolved polarized scatterometer: ASML YieldStar S-100 [1]. In this paper, the exercise was extended to several different structures combining multiple line end gap situations using different resists. Systematic comparison with CD-SEM is performed and discussed. Lithographic behavior of the main parameters is analyzed. Strengths and limits of the technique will be shown. Once validated, the metrology is used to build an OPC model and correct our test vehicle.

[1] "3D features measurement using YieldStar, an angle resolved polarized Scatterometer" A.L. Charley, P. Leray, K. D'havé, S. Cheng, P. Hinnenb, F. Li, P. Vanoppen, M. Dusa, Proc. of SPIE Vol. 7971 - 2E.

8324-87, Poster Session

E-beam inspection system for comparison of wafer and design data

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One of the most critical challenges for semiconductor manufacturing at present is realization of the intended pattern on the wafer. The lithography process is extensively simulated and test patterns are even printed on wafers to check the design data preparation algorithms used to generate the masks. Despite these precautions, patterning problems still occur and can result in a major delay in the qualification of a technology or product.

In this paper, we introduce a system and methodology for die to database comparison (D2DB) using E-Beam Inspection (EBI). Compared to the standard approach of using brightfield inspection for quantifying pattern variation, this system offers the following advantages:

1) Resolution.

2) Comparison to design intent rather than to a nominal die. This allows systematic defects that show up on each die to be detected.

3) Automatic binning of all defects using patch images. BF generally

requires SEM review.

4) Defect patch images include design target shapes making it clear what is defective.

Die at the edge of the lithography process window are targeted to bring out the patterning weak spots. The defects are binned by geometry and by yield significance. These results are fed back to the OPC, ORC, design for manufacturing and lithography teams for any necessary corrective action. Two examples, a double exposure patterned metal layer and a via layer, are presented in this paper. For the via layer, an issue with printing assist features was detected.

8324-88, Poster Session

Electron-beam proximity effect model calibration for fabricating scatterometry calibration samples

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Scatterometry has been proven to be effective in critical dimension (CD) and sidewall angle (SWA) measurements with good precision and accuracy. In order to study the effectiveness of scatterometry measurement of line edge roughness (LER), calibration samples with known LER have to be fabricated precisely. The relationship between ITRS LER specifications and the feature dimension design of the LER calibration samples is discussed. Electron-beam-direct-write lithography (EBDWL) has been widely used in nano-scale fabrication and is a natural selection for fabricating the designed calibration samples. With the increasing demanding requirement of lithography resolution in ITRS, the corresponding LER features become more and more challenging, even for EBDWL. Proximity effects in EBDWL mainly due to electron scattering can cause significant distortion of fabricated patterns from designed layouts. Model-based proximity effect correction (MBPEC) is an enhancement methodology for EBDWL to precisely define fine resist features. The effectiveness of PEC depends on the availability of accurate electron-beam proximity effect models and simulation methods. In this work, a proximity effect model at 50 keV accelerating voltage is calibrated to actual EBDWL results by employing double Gaussian approximation and optimizing the parameters of double Gaussian approximation, the effective beam size and the resist development threshold energy which are the key parameters in the model. The effectiveness of MBEPC corresponding to the calibrated model is predicted by simulation.

8324-89, Poster Session

How to minimize CD variation and overlay degradation induced by film stress

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It is getting harder to minimize feature size to satisfy bit growth requirement. 3D NAND flash memory has been developed to meet bit growth requirement without shrinking feature size. To increase the number of memory cells per unit area without shrinking feature size, we should increase the number of stacked film layers which finally become memory cells. Wafer warpage is induced by the stress between film and wafer. Both of film stress and wafer warpage increase in proportion to stacked film layers, and the increase of wafer warpage makes CD uniformity worse. Overlay degradation has no relation with wafer warpage, but has indirect relation with film stress. Wafer deformation in film deposition chamber is the source of overlay degradation. In this paper, we study the reasons why CD uniformity and overlay accuracy are affected by film stress, and suggest the methods which keep CD uniformity and overlay accuracy safe without additional processes. Post exposure bake temperature is one of factors which affect CD uniformity, and depends on the distance between wafer and hot plate. Since wafer warpage generates the variation of the distance between

wafer and hot plate, the local variation of post exposure temperature also increases within wafer, and finally degrades CD uniformity. To improve CD uniformity from wafer warpage, we prefer the method which temporarily reduces wafer warpage during post exposure bake. Wafer warpage can be minimized by additional process such as removing the films on wafer backside, but this method is not the best way because the cost should be considered. The mechanism of overlay degradation is different from CD uniformity degradation. While films are deposited on wafer, wafer is deformed by the local temperature difference within wafer. Though the local temperature difference disappears after film deposition, unfortunately wafer deformation does not disappear. Nonlinear errors due to wafer deformation can be minimized with high order overlay correction, but it seems not easy to suppress wafer to wafer overlay variation. Therefore wafer deformation should be illuminated with optimizing film deposition condition for overlay control.

8324-90, Poster Session

Improving the measurement performance of angle-resolved scattermetry by use of pupil optimization

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In present paper, we introduce a novel angle-resolved scatterometer with pupil optimization. Light from the source is collimated and then spatially modulated. The intensity distribution of the incident light in the pupil plane is optimized considering the feature and the image sensor response properties. The collimated beam is focused onto the feature on wafer via a projector lens and then the reflected light from the sample is collected by the same lens. The light beam passes through at the beam splitter, and the pupil is imaged by the relay lens. The pupil image, which represents the light reflected from the sample at a different altitude and azimuth angle, is detected by the image sensor. Feature parameters, including critical dimension, sidewall angle and height, are determined using intensity distribution at the image sensor.

A first order analysis of measurement sensitivity under different polarization conditions is carried out on resist-coated wafers with 32nm features using Rigorous Coupled-Wave analysis. Based on the criteria defined as the sum of the absolute difference of the relative intensity values between the nominal and varied conditions in the pupil, the sensitivity of the new technique and traditional scatterometer is compared. Simulation results show that sensitivity in p-polarization increases by more than 90%, while sensitivity in s-polarization increases by more than 150%. Reproducibility is analyzed using a Monte Carlo method and models for sensor, imaging, and illumination errors. Comparison of reproducibility of CD, sidewall angle, and resist height measurement is demonstrated.

8324-91, Poster Session

In situ critical dimension control during post exposure bake with spectroscopic ellipsometry

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Strong correlation between de-protection induced thickness reduction and amplified chemical reaction in the exposed area of the chemically amplified resist (CAR) during post-exposure bake (PEB) has been established. The optical properties of the resist film due to the thickness reduction can be detected using a spectroscopic ellipsometer. In this paper, a rotating polarizer spectroscopic ellipsometer is developed and a proposed control scheme is presented for signature profiles matching. With the implementation of the control scheme, wafer-to- wafer critical dimensions (CD) non-uniformity is improved by 5 times.

8324-92, Poster Session

Parallel GPU scatterometry simulations with GA and RCWA

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In Microlithography 2010-2011, we developed the scatterometry simulation software which has the spectroscopy calculation and optimization algorithm systems. We calculated the spectroscopy using the rigorous coupled wave analysis (RCWA). The conjugate gradient (CG) and the Genetic Algorithm (GA) methods were used to automatically search the data which matches the given spectrum. A lot of calculation time for GA is required and the accuracy of probing variable is not raised because the gene is taken in the integer. So, we combined GA with CG. We sped up the parallelization using the NVIDIA Geforce GPU. However, the computation speed was almost the same. Here are the reasons why as follows; (1) The Geforce GPU is dropping the performance of double precision floating point of C language. (2) The data movement between CPU and GPU memories takes time. So, in the case of little calculation amount, the benefit of using GPU was mute.

In this paper, we continue to speed up the scatterometry simulation software using the NVIDIA Tesla C2050 GPU (448 cores) and the programming language CUDA. The Tesla GPU has many threads and can handle the double precision floating point calculations. The RCWA calculation is carried out using numerical calculation libraries, CUBLAS and CULA. The scatterometry characteristic is examined by choosing the n-th power cosine type period groove. An parallel genetic argorithm (PGA) and a parallel conjugate gradient (PCG) method are used as the technique which automatically searches the data which matches the given spectrum. Finally, the results using this simulator are provided.

8324-93, Poster Session

Application of review-SEM to high-resolution inspection for 3xnm nodes

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As the pattern size shrinkage, it becomes difficult to detect the small physical defects using the conventional DF/BF inspection system, especially at the critical layer of the hp 32nm and beyond.

To solve this problem, the new inspection method 'iPQ' (Inspection and Process Qualifier) using the high-resolution-Defect-Review-SEM images had been developed for hot spot inspection.

This iPQ method is available to 1) Capture SEM images at the resisted points of each die inside of wafer, 2) Detect the defects using the image processing, 3) Qualify the defectivity of each die, 4) Output the qualified results to the server, which are not available at the conventional Defect-Review-SEM.

The following techniques are developed to achieve this inspection; 1) High S/N golden image creation for the reference of image comparison, 2) Fine care area setting, 3) Image processing technique using more than 50 types of image characteristics.

This iPQ method was applied to the advanced Flash Memory devices and the result indicates that iPQ is effective to monitor the distribution trend of fine size physical defects such as micro bridges and oxide voids. Especially, the significant defect distribution of wafer edge area was obtained at oxide trench layer of advanced node Flash memory.

Using this inspection, it becomes effective that the automatic inspection of large number point becomes and the reduction of inspection variation caused by manual classification.

In this paper, the detail of new techniques and application results of actual advanced memory devices will be discussed.

8324-94, Poster Session

A nonuniform SEM contour sampling technique for OPC model calibration

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OPC model calibration techniques that use SEM contours are a major reason for the modern day improved fitting efficiency in complex mask design compared to conventional CD-based calibration. However, contour-based calibration has a high computational cost and requires a lot of memory. To overcome this problem, in conventional contour-based calibration, the SEM contour is sampled uniformly at intervals of several nanometers. However, such sparse uniform sampling significantly increases deviations from real CD values, which are measured by CD-SEM. We also have to consider the shape errors of 2D patterns. In general, the calibration of 2D patterns requires higher frequency sampling of the SEM contour than 1D patterns do. To achieve accurate calibration results, and while considering the varied shapes of calibration patterns, it is necessary to set precise sampling intervals of the SEM contour. In response to these problems, we have developed a SEM contour sampling technique in which contours are sampled at a non-uniform rate with arbitrary mask shapes within the allowable sampling error. Experimental results showed that the sampling error was decreased to sub-nm when we reduced the number of contour points.

8324-95, Poster Session

Advanced full-automatic inspection of copper interconnects

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In copper (Cu) damascene interconnect processing, various defects such as wire disconnection, dishing, erosion and void are critical issues. These defects affect the electrical characteristics of the interconnects and have become important challenges with the aggressive shrinking of the critical dimensions. Sub-surface voids possibly present in nano-interconnects are not always detectable when using conventional BF/ DF inspection technologies and top-view SEM inspections, and can be very detrimental to the electrical performance of the devices. Therefore, an early detection of sub-surface voids in nano-interconnects during processing is required. For this purpose, we have developed a new full wafer void detection methodology described as following:

1) Detection of the sub-surface void using high voltage SEM with the newly optimized BSE detector.

2) Use of the Inspection and Process Qualifier (iPQ) system for analyzing high resolution SEM images with fast detection and ultra high sensitivity in order to detect voids and verify the void distribution over the wafer.

In this paper, we report on the development of a methodology for the detection of sub-surface voids in interconnects with CDs ranging from 15 to 35 nm wide using the Hitachi Multipurpose SEM Inspago RS6000 full wafer inspection system. The results of total void area, total void counts and void ratio within the Cu trenches for every die and structure inspected indicate that this methodology is effective to monitor process trends as a function of structure type with varying CDs, line density (isolated vs. dense lines), and dummy patterns around the structures. We demonstrate that our innovative technology provides a fast inspection of the metallization quality of narrow interconnects at early stages of processing.

8324-96, Poster Session

Classification and recognition of diffraction structures using support vector machine in optical scatterometry

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In scatterometry-based critical dimension (CD) and overlay metrology, library search is a widely used method. In library search, an optimized set of geometrical parameters for a diffracted structure can be achieved by searching for a best match between the measured spectrum and the simulated one. The speed and accuracy of searching is the key to guarantee the effectiveness of this method. In this paper, we propose a method for CD and overlay metrology using support vector machine (SVM) combined with library search. We firstly use a SVM classifier to identify the structural geometry of a diffracted profile. Next we use another multi-classification SVM to set the searching range for the CD or overly error of the identified diffracted profile into a small scale. Finally, by using some reliable and mature searching algorithm in this optimized and small range we can deduce the value of CD or overly error fast and accurately.

8324-97, Poster Session

A study of optical penetration into the micro-periodic structure of semiconductor devices

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The shrinking of design rule of semiconductor device continues unlimitedly and the defect detection with the optical inspection system grows in severity every year. As hp size of the micro Line/Space structure decreases, the shorter wavelength has been used in the inspection equipment to maintain the defect detection ability. For detecting the defect, probe light penetration to the defect position and getting high scattering efficiency of defect are necessary. For probe light penetration, there is alternative way to using the short wavelength light. That is, in the long wavelength region, the probe light reaches to the bottom of Line/Space structure according to the polarizing condition. Mechanism of this optical penetration will be clarified in our presentation, and the penetration condition of the long wavelength light is considered.

The probe light illuminates the pattern composed on wafer from its upper side in optical inspection equipment, and the scattered light from the defect is detected. A new model was introduced to analyze this penetration length.

From our analysis, we obtained the result that the penetration length becomes long as increasing the wavelength depending on the polarization. In our presentation, the detailed mechanism of this increasing of the penetration length will be explained. The effectiveness of the long wavelength light in the defect detection equipment will be described.

8324-98, Poster Session

Mechanism of photoresist shrinkage investigated by single-line scan of electron beam

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For mass productions of semiconductor devices, ArF scanner is believed to stay as a major lithography tool for several years due to postponed launch of EUV-lithography. In the ArF-lithography process, photoresist shrinkage due to electron beam irradiations during critical dimension (CD) measurements with a CD-SEM is an issue since it affects the certainty of the measurements. Recently, the effect of the shrinkage on the cross section shape of photoresist line patterns, and elastic simulation of the pattern distortions due to the shrinkage were reported. In this study, we examined the shrinkage caused by a single-line scan of electron beam. The range of the skrunk region perpendicular to the scan line was estimated in order to investigate how the incident electrons affect the photoresist patterns.

For experiments, ArF-photoresist line and space patterns of 45-nm half-pitch were used. We performed single-line scans with accelerating voltage of 500 V and probe current of 8 pA to obtain 1-pix-height SEM images. We repeated single-line scans at the same position of the sample and performed CD measurements for each 1-pix-height SEM image. Accordingly, we obtained the shrinkage development caused by repeating scans. The shrinkage caused by the first single-line scan was estimated by approximating the shrinkage development with exponential decay. We also repeated ordinary 2D scans to estimate the shrinkage caused by one ordinary 2D scan.

As a result, the shrinkage caused by a single-line scan and an ordinary 2D scan were 0.06 nm and 1.4 nm, respectively. For a quantitative evaluation of the range of the shrunk region along the pattern direction, we assumed the Gaussian shrinkage distribution of 0.06 nm peak-height by taking its standard deviation, as a parameter. The shrinkage of an ordinary 2D scan was calculated by summing up the contribution from the neighbor scan lines. From the comparison with the experimental data, 1.4 nm, we found the best fit with 35 nm width (twice of the standard deviation of the Gaussian distribution). This range is slightly wider than the scattering range of the secondary electrons induced by the incident electrons estimated by the Monte Carlo simulation.

In summary, we investigated the photoresist shrinkage caused by a single-line scan. Its magnitude and range along to the pattern direction were 0.06 nm and 35 nm, respectively, in above mentioned condition. The magnitude is significantly smaller than a typical shrinkage value, which is a few nm in this condition. This result implies the possibility of considerable shrinkage reduction. The shrinkage range was found to be slightly wider than the electron scattering range estimated by Monte Carlo simulation. In the presentation, a possible explanation for this discrepancy will be discussed considering the difference between the shrinkage due to the electron irradiation at top of the patterns and that due to the electron irradiation at bottom of the pattern.

8324-99, Poster Session

Influence of mask linewidth roughness on wafer performance

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Influence of the mask error continues to shrink with device pitch. The impact of Mask linewidth roughness (LWR) on wafer CD LWR becomes more obvious. The electrical characteristic of MOSFETs is making the influences of line-edge roughness (LER) or linewidth roughness (

LWR) on transistor performance a serious problem. In-gate LWR and gate-to-gate linewidth variation will be critical issues in the near future. The effects of sampling interval LWR measurements by critical-dimension scanning electron microscopy on measurement accuracy were examined by both experiment and simulation.In this study report, we examine the mask (i.e.,193-PSM,EUV) LWR and wafer printing result for establishing the Mask LWR specification.

8324-100, Poster Session

Optimization of blended virtual/actual metrology schemes

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Virtual metrology (VM) is an alternative scheme to conventional metrology

which takes the processing data produced by the processing tool in real time, (plasma etching data during isolation trench formation, for example) and predicts an outcome of the wafer (e.g. critical dimension of the trench) utilizing an empirical model. However, VM prediction quality is not as good as that of conventional metrology and VM models may need frequent recalibration in order to maintain acceptable predictive capability. Still, VM may provide a significant benefit over conventional metrology in that it produces an immediate, low cost prediction for each wafer going through a process. In real life we envision that practical metrology schemes will involve VM in combination with actual metrology, the latter being used for the needed periodic recalibration of the VM empirical model. We also envision an algorithm that would respond to a fault being predicted by the VM model by requiring additional actual measurements. The purpose of this work is to analyze the conditions under which such a blended metrology scheme would be advantageous, and to provide rules that will let us optimize such blended metrology schemes.

Any metrology scheme, whether conventional, virtual or blended, used for fault detection may produce false alarms (type I error) or may fail to detect a fault (type II error). Those two types of errors are associated with operational costs that depend on the metrology scheme and the algorithm used in response to an alarm. In this work, we formulate the costs associated with type I and type II errors that result from a blended metrology scheme, and we propose a general framework that can be used to quickly lead to the optimal design of such schemes given the characteristics of the process in question. This is done by exploring the effects of variables such as the frequency of samples that go through conventional metrology, the prediction quality of the VM model, the cost of missed or false alarms, processing and actual metrology costs etc. The resulting framework is being used to evaluate the efficacy of blended metrology schemes for actual process steps.

8324-101, Poster Session

Reticle intensity-based critical dimension uniformity to improve efficiency for DOMA correction in a foundry

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CDU improvement is an essential element for getting the process margin better in wafer and increasing production yield. Variations in global CDU measured during the manufacture of integrated circuits arise from three contributions - Mask, Scanner and Wafer process. Conventional Dose Mapper (DOMA) method, that relies on wafer CD-SEM measurements, correct errors from above all 3 factors but it is time-consuming and lacks accuracy since it involves actual wafer printing, CDSEM measurement accuracy and sampling plan, etc.

This paper will demonstrate a new method of DOMA creation (iCDU) that consists of 2 parts:

1) Part 1 addresses the CDU contribution from the reticle, through an intensity-based, 'in-die' method with no special measurement targets, and automatic identification of dominant pitch of a repeating pattern, by KLA-Tencor's TeraScan (SLQ26x) reticle inspection tool, during reticle requalification. We describe its basic theory and results on advanced Logic Poly masks, as well as the application of CDU maps for optimizing the wafer manufacturing process in adjusting scanner dose to improve Intra-field CD uniformity.

2) Part 2 addresses the CDU variations of scanner signature. This factor has been derived in a preliminary step and stored in a database which is periodically updated after preventive maintenance with CD.

8324-102, Poster Session

Experiment analysis of absolute flatness testing

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High-accuracy interferometeric surface metrology is constantly gaining importance, not only in the classical area of optical fabrication, but also for new application such as semiconductor and lithography lens. Requirements for the measurement resolution in the sub-nanometer range have become quite common. This includes not only the repeatability or reproducibility but also the absolute measurement accuracy, in which both the slowly varying shape error and the medium-to-high spatial frequency waviness of the surface under test, is important. Result of the testing contain the reference surface errors and test surface errors in the high-accuracy Phase shifting interferometeric which test the relative phase between the two surface. The test accuracy can be achieved by removing the error of reference surface. In this case, one of body of so-called absolute tests must be used which can test the systematic errors, including the reference surface, of the instrument to be used to improve the test accuracy.The accuracy of the interferometer needs different methods to determine in the high accuracy testing.In this paper, we did two experiment including even-odd functions and rotation shear absolute testing methods. The flat in the experiment are the Veeco standard flat lens 4" , Zygo standard flat lens 4", 4" standard flat lens made by Nanjing Technology University in China. The accuracy of the rotation flat roof is 1/400 degree.The result of the experiment can determine the accuracy of the arithmetic.

8324-103, Poster Session

Lithography process control using in-line metrology

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Focus and dose have always been the primary variables2 of concern in CD uniformity. Generally, theses parameters are fixed when the process is set up. In order to maintain process capability one needs to characterize and to correct the focus and dose errors produced by each contributor (tool, layer, resist, reticle) with high sensitivity and good repeatability. Run-to-run3 in manufacturing is required to address CD variations to each contributor.

To correct theses variations, a lithography process model has been built. A Bossung curve is first set up with high dimensional sensitivity to dose and focus patterns. Scatterometry4 metrology tools is used because of the significant benefits, fast, accurate, repeatable, and non-destructive measurements of critical dimension and their profile shape. Top and bottom CD of resist shape are used to calculate best CD and, dose and focus sentivity coefficients5. These coefficients will be used to extrapolate the focus and dose from the data measured on production wafers. A new analytical deconvolution method, using the difference between the Top and the bottom CD, is implemented, so that every measured (CDbot, CDtop) pair results in a dose/focus deviation (D, F).

The run to run flow is wafers are exposed and processed in the lithography cluster. These same production wafers are measured on the scatterometry tool. Immediately after the measurements have been completed, the raw measurement data are passed (along with any needed coefficients) to the new deconvolution analyzer. At this moment, each point measured on the wafers can be associated to couple of dose and focus offsets. Then, on the photolithography tool, a new recipe is created with a dose and focus offset matrix. Finally, this new recipe can be applied on the next lot. With this method, dose and focus can be corrected, enabling seamless transition to technology nodes with reduced depth-of-focus (DOF).

C040 acti and gate production wafers have been the primary vehicle used for this study. The paper provides, on this technology, experimental evidence confirming CD variation by 45% and reduce the slope variation by 49% with the uses of this method. Because of theses improvements, this method will reduce the after etch CD uniformity dramatically.

8324-104, Poster Session

Development of charging simulator and prediction of intensity profile of line and space pattern of resist

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Simulator of electron motion under charged material has been developed to investigate charging phenomenon on surface of semi-conductor during the SEM observation. The simulator is based on finite element method calculating for electric field, it also includes operation of the electron scattering, transport and recombination with hole in the layer of materials.

The signals from line and space pattern of resist are influenced by the scanning direction of electron beam. The peaks of the two edges in intensity profile of a line appear as symmetric on the condition that electron beam scans to the line of the pattern vertically. However in the parallel scanning case, the peaks of it are asymmetric. The other hand, the intensity of signal from a space by vertical scanning is lower than that of parallel experimentally.

We have calculated these experiments using by our simulator. The results of it agree with those experiments, and we have found that those phenomena can be explained the charging effect by scattering electron and relaxation of charging surface properly.

8324-105, Poster Session

Investigations into an electrostatic chuck for 450mm wafer

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We report on theoretical and experimental investigations into electrostatic chuck designs for use in future e-beam lithography on 450 mm Si-wafers. Subject to a mass budget of 8 kg, massive and light-weight chuck designs of low thermal expansion materials (LTEM) were evaluated by finite element (FE) modeling. Chuck positioning on a kinematic 3 point mount results in bending under gravity and out-of-plane distortions (OPD) of about 1250 nm (400 nm) of the initially flat surfaces, for the massive (light-weight) designs. Corresponding surface in-plane distortions (IPD) for a chucked Si-wafer of thickness 925 μm attain about 3 nm and 1 nm for the massive and the light-weight design, respectively. By using a 6th order polynomial correction upon e-beam writing, the former (latter) value is easily reduced to IPD ≤ 0.67 nm (≤ 0.44 nm).

Various pin-patterns for the chuck's surface were adopted and resulting wafer bending under the influence of electrostatic forces was determined. At a typical electrostatic pressure of about 18 kPa, a perfectly flat square pin pattern of pin-pitch 3.5 mm and pin-diameter 0.5 mm results in wafer IPD < 0.5 nm, which is considered sufficient for obtaining the desired total overlay accuracy of about 3.5 nm. In preparation for later chuck manufacturing, the pin structuring process for a corresponding LTEM chuck surface was experimentally tested and verified. The homogeneity of the etching process is crucial for local variations in wafer attraction /1/ and will be reported.

8324-106, Poster Session

Real-time scanning detection system of defects on a photomask by using the light scattering and interference method

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In the process of lithography for semiconductor devices, the disuse of semiconductor devices are caused by the several hundred nanometer size pollutants, generated by photochemical reactions, which call the haze. Therefore, the real time visual scanning detection system is needed to inspect the haze before the generation of disuse semiconductor devices. We proposed and experimental confirmed the concept of the real time scanning detection system for the defect on the photo-mask by interference fringes.

We considered the visualization to catch small defects easily, the high resolution and the real time scanning on the design. The interference method is used to catch the small defects easily because the divergence waves get larger interference fringes on the detector. The short 532 nm green laser is chosen to increase the resolution. The incidence laser beam is expanded to 5 mm x 5 mm for unit inspection area with the beam expander and square mask to scan in real time. The expanded beam propagates to the tainted photo-mask with incidence angle nearby Brewster angle. The laser beam scatter on defects and the laser beam reflect on the rest area of the front surface. The separated light waves, reflected and scattered light waves, generate interference fringes about the unit inspection area, 5mm x 5 mm, on the detector. For all of the Cr defects from size of 500 nm to that of 25 we succeeded to detect the interference fringes in 30 minutes for 6 inch by 6 inch 6 mm thickness photo-mask.

8324-107, Poster Session

Overlay mark design and evaluation for SADP process

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Overlay performance has been a critical factor for advanced semiconductor manufacturing for many years. Over time these requirements become more stringent as design rules shrink. Overlay mark design and selection are the first two steps of overlay control, and it is known that different overlay mark designs will have different responses to process setup conditions. An overlay mark optimized for traditional process might not be suitable for Self-Aligned Double Patterning (SADP) technology due to changes in lithography and etching process conditions. For instance, the traditional Box-in-Box (BiB) target defined by the core mask becomes a template structure in SADP flow, the pitch and cycle of the overlay mark is further changed after spacer formation and core film removal hence the mark recognition and robustness have been challenging for the subsequent process layers.

The studies on alignment mark and overlay mark design for SADP process have been discussed in several papers with the concepts of spacer merged. However, the comprehensive study on the methodology of overlay mark design and selection is still not available. In this paper, various types of overlay marks were designed to comply with the SADP process to get rid of the weaknesses of traditional BiB target. In addition to the traditional TMU performance, the source of variance (SOV) methodology, which decomposes and compares overlay raw data into various systematic components such as wafer, field, and un-modeled terms, was adopted to determine the optimal overlay marks for meeting production overlay control requirements in SADP process flow.

8324-108, Poster Session

Overcoming silicon limitations: new 3D-AFM carbon tips with constant high-resolution for sub-28nm node semiconductor requirements

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The AFM technology is more and more introduced in the semiconductor industry for new material surface roughness, accurate depth

measurements and critical dimensions measurements of multiple patterns after lithography and etching technological steps. Whatever enhancements done on the AFM head in order to reduce noise level, to increase throughput, to reduce measurement uncertainty, the tip remains a crucial consumable that make the link between the AFM and the sample to be measured. In most of the case, the AFM tip is unfortunately considered as simple consumable. However, we have reached such stringent needs in the semiconductor industry that the tip has become a full functionality of the AFM technique that also needs to be enhance in order to use the AFM tool at the maximum of its performances. Current limitations include (i) changing tip dimensions over tip lifetime, thus reduced accuracy, (ii) lack of sharpness and too large tip radius/diameter, and (iii) total cost which are not conform with production environment needs.

In this paper, we will present and discuss a new AFM tip design. A unique T-shape like design allows for constant resolution, independent from tip wear. This design is unachievable with current silicon based technology - in contrast to the well established electron beam induced processing (EBD), which allows to manufacture 3D shapes of the desired design with nanometer precision - in bulk amorphous, high dense carbon (HDC) material.

We will show the advantages of such process for the semiconductor industry. A large part will be dedicated to the use of this process on AFM3D technology in order to answer to sub-28nm nodes requirements. We will present 15nm tip diameter with 3nm tip radius associated to advanced measurements on FinFET structures and advanced lithography patterns (typically sub-30nm spaces). Results will be compared to conventional silicon tip performances. We will show how silicon tips technology can degrade measurement resolution over tip lifetime while EBD technology keeps it constant. Finally, we will propose a technological tip roadmap dedicated to the semiconductor industry

8324-109, Poster Session

Surface scanning inspection system particle detection dependence on aluminum film morphology

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Physical vapor deposition (PVD) aluminum films present unique challenges when detecting particulate defects with a Surface Scanning Inspection System (SSIS). Aluminum (Al) films 4500Å thick were deposited on 300mm particle grade bare Si wafers at two temperatures using a Novellus Systems INOVA® NExT, an ionized PVD deposition tool. Film surface roughness and morphology measurements were performed using a Veeco VX-310® atomic force microscope (AFM). AFM characterization found the high deposition temperature (TD) Al roughness (Root Mean Square 16.5 nm) to be five-times rougher than the low-TD Al roughness (rms 3.7 nm). High-TD Al had grooves at the grain boundaries that were measured to be 20 to 80 nm deep. Scanning electron microscopy (SEM) examination, with a Hitachi RS6000 defect review SEM, confirmed the presence of pronounced grain grooves. SEM images established that the low-TD filmed wafers have fine grains (0.1 to 0.3 um diameter) and the high-TD film wafers have fifty-times larger equiaxed platelet-shape grains (5 to 15 um diameter).

We will explore the feasibility of utilizing a bidirectional reflectance distribution function (BRDF) light scattering modeling as a means of determining the most appropriate polarity prior to the SSIS recipe creation process.

8324-110, Poster Session

Residual layer thickness control and metrology in jet and flash imprint lithography

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S. V. Sreenivasan, The Univ. of Texas at Austin (United States)

Jet-and-Flash Imprint Lithography (J-FIL) has demonstrated capability of high-resolution patterning at low costs. It uses a patterned template or master to press on an array of droplets of a polymerizable liquid dispensed on the wafer to form a contiguous fluid film while filling the features on the template. This is then cured using UV-light leading to polymerization and creation of a patterned resist layer. The template is then separated, leaving the patterned resist behind. Control of the residual layer thickness (RLT) of cured resist underneath features is critical for subsequent pattern transfer into the substrate. Variation in RLT leads to critical dimension variation, degrading device performance. This paper studies the effect of different process parameters on RLT variation. Through experiments and modeling, it has been found that flatter wafers with lower nanotopography, and thinner RLT lead to better uniformity.

For studying RLT variation, accurate metrology is critical. Currently, all metrology is done using destructive cross-section SEM, which is only useful for studying a few reference cases. To this end, nondestructive optics based methods have been explored, including the TSOM method (1) for viability in metrology for J-FIL. TSOM enables nanoscale metrology by making use of a set of through-focus images from a conventional optical microscope. A series of metrology experiments on wafers with patterns of varying pitch and RLT have been conducted. The evaluated optics based methods appear promising for measuring the mean RLT and variation, with a potential thickness measurement accuracy of 1nm. Both simulation and experimental results will be presented.

1. Ravikiran Attota, Ronald G. Dixson, John A. Kramar, James E. Potzick, András E. Vladár, Benjamin Bunday, Erik Novak, and Andrew Rudack, "TSOM Method for Semiconductor Metrology," Proc. of SPIE Vol. 7971, 79710T, 2011.

8324-111, Poster Session

Sub-40nm high-volume manufacturing overlay noncorrectable error characterization

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Circuit layout and design rules have continued to shrink to the point where a few nanometers of pattern misalignment can negatively impact process capability and device yields. As wafer processes and film stacks become more complex, overlay and alignment performance in High Volume Manufacturing (HVM) have become increasingly sensitive to process and tool variation experienced by incoming wafers. Current HVM relies on overlay control via feedback APC, single exposure tool grid stability, scanner to scanner matching, correction models, sampling strategies, overlay mark design and metrology. However, even with improvements in these, a significant fraction of the non-correctable error i.e. residuals. While lower residuals typically lead to increased yield performance, it is difficult to achieve in HVM due to large combinations of wafer pedigree in terms of prior tools, recipes, and the variety of ongoing process conversions. It is this residual error that is important to monitor as a metric of line stability, understand origin of any changes and setup mitigation strategies. In this study, we investigated residual errors of sub-40nm processes as a function of correction models, sensitivity of the model parameters to data quality, correlation of parameter changes to process drifts and expected magnitude of changes. Additionally we use the results to identify appropriate strategies for improved performance.

8324-112, Poster Session

Nanoparticle size and shape evaluation using the TSOM method

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For most cases where nanoparticles play important roles, it is important to measure not only their size, but also their shape for effective use.

Even though there are several size measuring methods, limited three-dimensional shape measuring methods are available such as atomic force microscope (AFM), scanning electron microscope (SEM), and transmission electron microscope (TEM). Every method has advantages and disadvantages. In spite of the availability of various established methods for dimensional analysis, there is a need for accurate, yet, high throughput tools or methods that are also economical. We present here one such novel method developed at the U.S. National Institute of Standards and Technology.

A novel optical through-focus scanning optical microscopy (TSOM) method that yields nanoscale optical information from images obtained at multiple focal planes will be used here for nanoparticle dimensional analysis. The TSOM method can account for not only size differences but also for shape differences among nanoparticles. Size evaluation based on simulations will be presented along with experimental data for nanoparticles and nanodots with sizes going below 100 nm. Experimental size determination using experimentally created library will also be presented. Simulation analysis shows the ability of TSOM method to distinguish if a particle is an isolated one or an agglomeration of several particles. The results show applicability of the TSOM method for nanoparticle dimensional analysis.

8324-114, Poster Session

Photoresist qualification using scatterometry CD

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As the semiconductor industry advances to smaller design rules, photoresist performance to meet the tight requirements are critical for the lithography process. Critical Dimension (CD), Side Wall Angle (SWA) and photoresist height, which are critical for the final semiconductor patterning, depends on the photoresist chemistry. Each photoresist batch has to be qualified to verify that it can achieve the required quality specifications. Photoresist qualification is done by exposing photoresist and monitoring outcome after develop.

In this work, Archer 300LCM Scatterometry CD was evaluated using DOW 193 Immersion Top Coat Free Commercial Photoresist and Anti Reflected Layers (ARL). As part of the sensitivity analysis, changes in photoresist thickness, ARC thickness and photoresist formulation were evaluated. Results were compared to CD-SEM measurements. The CD sensitivity was evaluated on two grating dense line and space features with nominal MCD values of 37nm and 75nm.

Sensitivity of the SCD for photoresist parameters was demonstrated.

8324-115, Poster Session

Rigorous 3D electromagnetic field simulations for EUV mask metrology

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Extreme ultraviolet (EUV) lithography is discussed as an alternative for replacing DUV photolithography for manufacturing features on integrated circuits with critical dimensions as small as 16 nm or beyond. Computational lithography allows to enhance attainable resolution and has allowed to push the limits of DUV lithography to a small fraction of the optical wavelength. Rigorous simulations of light propagation through photomasks are also an essential component in optical metrology of such structures.

In DUV lithography and metrology simulations a main challenge consists in accurate resolution of light fields in the presence of complex 3D absorbing structures of high refractive index-contrasts. In the EUV regime available materials exhibit far lower refractive index-contrasts. This leads

to additional challenges for rigorous simulations: Computational domain sizes increase due to the fact that absorber structures need higher volumes. EUV Masks are mounted on multi-layer mirrors with a high number of single layers. This again increases 3D computational domain size and complexity. Deviations from ideal geometries like defects or sidewall-angles have a larger effect on the diffraction spectra.

We develop a time-harmonic finite-element (FEM) solver which also allows to address 3D EUV simulation tasks. The solver incorporates higher-order edge-elements, domain-decomposition methods and fast solution algorithms. In this contribution we report on rigorous modelling of EUV masks with buried defects.

8324-117, Poster Session

Improving lithography throughput and minimizing waste using predictive multi-area scheduling

J. R. Moyne, Applied Materials, Inc. (United States)

Many of the challenges in improving operational processes in wafer fabrication, such as throughput and on-time delivery, can be impacted by scheduling. A view of the resulting requirements shows that while individual area predictive scheduling can provide significant benefit, especially for bottleneck toolsets, coordinated multiple area scheduling on top of individual area scheduling can address all of the challenges from a fab-wide optimized perspective. Thus we must leverage the technology of a predictive area scheduler into a fab-wide coordinated WIP optimization solution. In this coordinated solution the area predictive schedulers draw from the same set of scheduling services to achieve area objectives. These objectives are governed by a higher layer fab-level WIP management plan that determines how individual areas should be optimized to support overall fab scheduling objectives with respect to the ERP. In considering the implementation plan for predictive scheduling, the Theory of Constraints suggests that we should target the bottleneck process first, which is oftentimes lithography; thus there has been a focus on predictive area scheduling for lithography. As we expand the scheduling solution to other areas, we must focus on other potential bottleneck processes, and also look at processes that interact with the bottleneck process, as these interactions might be a source of performance degradation.

As an example assume we have two products running recipes AL and BL at lithography and AP and BP at plating respectively. Assume specific lithography tools are dedicated to each recipe and specific plating chambers are dedicated to each recipe. If a chamber 1 goes down in the plating bay, because this chamber is dedicated to the production of product A, the area capacity for product A is reduced. With individual area scheduling optimization lithography production would continue as before resulting in WIP accumulation of product A at plating. With fab-level WIP management in place the directives for lithography optimization could be changed to provide a better balance of WIP for plating (i.e., higher ratio of product B to A). This could be done through scheduling changes or potentially requalification of a lithography tool for product B.

The predictive multi-area scheduling and WIP optimization approach presented provides a framework for addressing lithography throughput maximization and waste minimization, whether or not lithography is the bottleneck process.

8324-118, Poster Session

Evaluating diffraction-based overlay

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We evaluate diffraction-based overlay (DBO) [1,2] metrology using different test wafers. The test wafers have different film stacks designed to test the quality of DBO data under a range of film conditions. We present DBO results using both traditional empirical approach (eDBO)

and a model-based analysis (mDBO)[3]. eDBO relies on linear response of the reflectance with respect to overlay displacement within a small range. It offers convenience of quick recipe setup since there is no need to establish a model. However, it requires specially designed multiple pads for each direction (x or y), which increases measurement time and occupies too much space. mDBO requires film stack information and optical properties to set up a model, but it allows overlay measurement with reduced number of pads, thus reducing measurement time and DBO target space. We evaluate the accuracy and precision for eDBO and mDBO methods using various DBO targets designed with different pitches and programmed shifts. One way of testing measurement accuracy is to compare the overlay results from closely located DBO targets. We investigate how the pitch of the gratings in DBO targets affects overlay sensitivity and linearity and influences precision and accuracy of overlay measurements. We compare the DBO results with image-based overlay (IBO) as well. We demonstrate that both mDBO and eDBO methods are capable of making high quality overlay measurements.

8324-120, Poster Session

Apply low-temperature plasma in the rework procedure of Al film structure to prevent pattern collapsed and CuAl2 precipitation

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In a conventional lithography process with Al film structure, the photo resist pattern is removed by two methods: wet etch (solvent - NMP plus chemical - EKC) or wet etch combine with dry strip process.

There were some problems in these kinds of processes. Pattern collapsed after wet etch process due to the photo resist (PR) adhesion capability reduced by EKC. Contact angle can be the index to measure the adhesion capability.

So as to prevent the pattern collapsed issue, a plasma treatment step was increased after wet etch. But it induces another issue. IC devices fabrication in Al interconnect process, 0.5wt% Cu is generally used in Al film deposition for better Al electron migration performance. High temperature Plasma (>250) with high potentiality of CuAl2 precipitation, which will form a residue cause the metal line bridge induce yield loss.

In this paper, we modify the rework procedure as NMP only and lower the plasma temperature to the "room temperature" to prevent the pattern collapsed issue and the CuAl2 precipitation.

The modified rework procedure is not only improved the defect, WAT and yield, but also shorten the cycle time of resist remove process.

8324-121, Poster Session

Automated heuristic defect classification (AHDC) for haze-induced defect growth management and mask requalification

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This article presents the results from a newly developed heuristic, yet highly deterministic and repeatable, computational algorithm designed to automatically disposition defects found in Mask inspection tools. The algorithm mimics the manual rules followed by the mask manufacturing technicians when classifying defects flagged by an inspection system. The power of this algorithm lies in that it is able to compute the critical dimension (CD) variation between defect and reference image pairs reported in the mask inspection reports without using any CAD or GDS data. It bins defects as lithographically significant or insignificant, leading to a fully automated (no human in the loop) defect classification implementation, and is designed to be tolerant to noise in the inspection images. Results from various program defects mask covering a host of geometries are presented.

Computer algorithms as found in mask inspection systems primarily operate by differencing the defect and the reference images and than scan for defective pixels in a "serial" fashion. This is done either at the individual pixel level or by convolving the differenced image by an appropriately shaped kernel to overcome signal to noise ratio. These algorithms are entirely based on the "differenced" image. This has an enormous advantage in that the inspection system can inspect a very large mask field in a reasonable time using its already massive computational horse power. Another advantage is that the knobs to tune the inspection algorithm are relatively simple, thus an operator with no image processing skills can quickly arrive at a reasonable inspection recipe setting. The disadvantage is that defects in tight geometries may be treated in a comparable manner to those in sparse geometries. A further problem is that there is a loose correlation between lithographically significant and insignificant defects.

Human's on the other hand "look" at images and make decisions in a rather "parallel" thinking structure. A technician would surely look at the differenced image, but also look at the individual defect and reference images to determine if the defect lies in tight or open geometries. A technician may also compare contours of defect and reference geometries in question. When a defect lies in a tight area, the deviations in multiple opposing contours are heuristically added to arrive at a classification decision. Specs for tight and loose geometries may be different. Further complications arise due to bright-field and dark-field masks with contact and SRAF type geometries. Since the inspection systems do not operate heuristically, a technician is generally able add value by visually disposition defects after the inspection process to cut down the number of defects that need to be repaired. It is common knowledge that humans inevitably make mistakes or make non-repeated dispositioning decisions that frequently go untracked due to a lack of robust software framework for ensuring consistent decision making. The difficulty with codifying the numerous heuristic rules that the inspection technicians generally follow into a computer algorithm are somewhat challenging. Where this has been done there are usually a lot of software parameters (knobs) that need to be set to optimally tune the algorithm. This alone renders such algorithms impractical for high volume production.

This paper will show the results from the AHDC algorithm that heuristically dispositions defects from mask inspection tools in a high volume production environment; robustly and repeatedly.

The article begins by pictorially outlining manual methods for dispositioning complicated geometries. Once the general rules of manually disposition defects are established for the reader, the same defects are than classified via the fully automated heuristic defect classification algorithm. It is shown that the heuristic algorithm arrives at the same answer, in a repeatable fashion, cutting down the defect classification time to a few milliseconds. If probed, the software framework is able to pictorially and in a physically motivated manner render to the user, how a decision was made. Such a user interface is critical to gaining the confidence of the technician as the algorithm is no longer presented as a black-box that needs to be blindly trusted.

Since AHDC computes various image based metrics, such as area, CD, residue, intensity difference, it is shown that such metrics can be very beneficial for tracking the size of defects in repeated inspections. A case where this is extremely important is in the management of haze induced defects that grow in size over time, as found in 193 immersion lithography. A software framework has been developed and deployed, that can track metrics computed by AHDC for every defect in every inspection of the same reticle, via a powerful relational database management system. This framework presents these metrics to a technician for rapid mask requalification decision making in a high volume production environment, in a concise and filtered manner.

8324-22, Session 8

Directed self-assembly defectivity assessment

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The main concern for the commercialization of directed self-assembly
(DSA) for semiconductor manufacturing continues to be the defectivity.
Our research studies the defectivity of DSA in the context of a 300mm
wafer fab cleanroom environment; while last year's research1 estimated
DSA defectivity of 12nm line and space arrays generated by chemical
epitaxy, this paper discusses the missing via density, CD-distribution
and registration accuracy (hole-in-hole) for DSA contact rectification by
grapho-epitaxy.

The directed self-assembly was conducted using a PS-b-PMMA block
copolymer following a typical grapho-epitaxy contact hole rectification
process flow. Firstly, a unique "phase-separation" CD-SEM measurement
was performed to measure the diameter of the PMMA cylinder domains
prior to PMMA removal (figure 1). This technique enables the direct
measurement of thousands of phase-separated domains, generation of
histograms and image review necessary for yield studies; for example,
review of the domains +/- 2 sigma and 3 sigma from the mean. Secondly,
following a dry-etch development (removal) of the PMMA cylinders, we
measure the phase-separated hole registration relative to the grapho-
epitaxy prepattern. The CD measurement computes the center shift
between the pre-pattern versus the developed hole and report the
displacement as a vector (in nanometers) and direction. This technique
enables the measurement of thousands of holes (> 100 holes per
minute), generation of histograms, and SEM image review for specific
holes of interest; for example, review of the 10 worst (figure 2). Thirdly,
we measure defectivity using the bright field inspection, we scanned >
500-million vias evenly distributed across 17 dies, reviewed all defects
using a review SEM, classified each defect based on root-cause and
identified a total of 22 missing vias (figure 3); thus, the missing via defect
density for this study was 1-per-25 million (figure 3).

8324-23, Session 8

Pattern density multiplication by direct self-assembly of block copolymers: toward 300mm CMOS requirements

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Density multiplication of patterned templates by directed self-assembly
(DSA) of block copolymers stands out as a promising alternative to
overcome the limitation of conventional lithography. Recent works
highlighted the capabilities of DSA to be integrated with state-of-the-art
193nm lithography1 and point out the necessity of a 300 mm baseline2.

In this paper we investigate the possibility to reach 300mm CMOS
requirements by integrating graphoepitaxy of PS-b-PMMA self assembly.
First, the interface between the copolymer thin film and the resist/
silicon substrate has to be neutralized in order to avoid a preferential
wetting of the substrate by one block and to allow by this way the
perpendicular orientation of the structure. This can be done by the
chemical derivatization of the silicon wafers with random copolymers
containing the same constituents as the block copolymer used3. Then,
the PS-b-PMMA is spin coated and annealed in order to generate self
assembly, then chemical treatment (dry or wet etching) removes the
PMMA block and forms a PS mask. The horizontal and lateral order
is controlled by tuning different parameters: molecular weight of the
polymeric constituents, correlation between a substrate patterns and
the intrinsic copolymer period, interaction with the substrate. Different
schemes to integrate DSA process by using 193nm dry lithography or
e-Beam lithography will be presented (see figure 1).

Moreover, several challenges like solvent compatibility, bake kinetics and
defectivity will be addressed. Concerning defectivity, we will propose
a methodology in order to evaluate and optimize the long range order
induced by graphoepitaxy of the block copolymer DSA. By implementing
a graphoepitaxy methodology with BCP film thickness larger than the
trench depth (see figure 2a), the Voronoi analysis may be used to quantify
the degree of local order by counting the disclinations. This approach
affords the monitoring of the overall block copolymer self-assembly
process and enables us to easily optimize the parameters required for a
long-range order structuration, leading to zero-defects block copolymers
self-assembled networks (figure 2b and c). Transfer capabilities of the
PS nanostructures in the bulk silicon substrate by using plasma-etching
will be also detailed, both with the film on bare silicon or organized with
graphoepitaxy approaches.

These results show the high potential of DSA to be integrated directly
into the conventional CMOS lithography process in order to achieve high
resolution and pattern density multiplication, at a low cost.

8324-24, Session 8

Measurement of placement error between self-assembled polymer patterns and guiding chemical prepatterns

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Recent demonstrations of directed polymer self-assembly at the 300 mm
wafer scale have amplified interest in it as a potential extension to current
patterning techniques for sub-15 nm half-pitch features. While the very
nature of directed self-assembly implies registration to lithographically
defined guiding prepatterns, layout optimization and eventual device
fabrication demand a detailed knowledge of the self-assembled pattern
placement. In chemical epitaxy with density multiplication, perfect
commensurability between prepattern line widths and pitches and the
same respective parameters of the polymer domains they selectively
pin is not necessary for successful guidance, a fact that widens the
process window but complicates the question of pattern placement.
Using specially designed chemical patterns fabricated via electron
beam lithography to guide the self-assembly of a 12 nm half-pitch
PS-b-PMMA lamellae block copolymer, this study aims to precisely
quantify the absolute placement error between underlying prepatterns
and the resulting self-assembled patterns as a function of prepattern line
width and pitch as well as polymer film thickness for line-space tripling
and quadrupling. We will also discuss the formation of more complex
self-assembled line-space patterns directed by chemical prepatterns
designed for the purpose, with emphasis on the effect of variations in the
prepatterns and process conditions.

8324-25, Session 8

Characterization of cross-sectional profile of epitaxially assembled block copolymer domains using transmission small angle x-ray scattering

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Transmission small angle X-ray scattering (tSAXS) was used to
characterize the cross section of poly(styrene-b-methyl methacrylate)
(PS-PMMA) block copolymer line gratings assembled on chemically-
templated substrates with a pitch less than 50 nm. X-ray diffraction
data covering a broad Q_x and Q_z region were collected and analyzed,

where the x-axis denotes the in-plane direction perpendicular to the line gratings and z-axis is along the thickness direction. The X-ray data can best be fit with a cross section comprised with footing, waist and top rounding. The simplest model to simulate such a cross section is a stack of four trapezoids, each with discrete side wall angle, height and width. Even with this simple 4-trapezoidal model there exist nine fitting parameters; however, there also exist sufficient X-ray characteristics and quality to ensure a fit with a reasonable confidence. Figure 1 illustrates this point; the 9-parameter model was determined by simultaneously fitting diffraction curves at five discrete Qx values. The best fit cross section of PS-PMMA block copolymer nanopatterns is given in Figure 2. It is noteworthy that the area occupied by each component of the nanopatterns is exact 50%, consistent with the composition of the copolymer used. This observation further highlights the accuracy of the X-ray data and its analysis. The line edge roughness (1s) was also determined by the intensity decay rate along Qx, known as the apparent Debye-Waller factor. The cross section edge profile and the interface roughness value obtained from X-ray data will also be discussed and compared with the results of computer simulation of the self-assembly process.

8324-26, Session 8

Characterization of nanostructures for imprinted dot/hole patterns by x-ray metrology

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We have so far developed x-ray metrology for measuring a cross-sectional profile of surface periodic grating patterns. Nanoimprint lithography is one of the promising candidates for fabricating dozens nanometer scale line patterns and dot/hole patterns. For the master mold, non-destructive characterization and the quality control of nanostructures, such as the pitch, size, height, sidewall angle, corner rounding and these fluctuations are necessary. Because transferred imprinted patterns are affected by the master mold and the device performances can be strongly correlated with these parameters. We have taken notice of nanoimprint processes of bit-patterned media (BPM). Silicon master mold, nickel father stamper, nickel mother stamper, transparent mold, and BPM etching mask are transcribed in sequence. We have applied x-ray meteorology to these imprinted dot/hole patterns in order to evaluate difference of nanostructures during the transcriptions from the silicon master mold to the BPM etching mask pattern. X-ray diffraction images were collected in grazing incidence geometry, when incidence angle to the sample surface is about the critical angle of total reflection and x-ray wavelength is 0.15418 nm. Several diffraction peaks from the periodicity of the dot/hole array are observed in the lateral direction (2 -direction) and the dot/hole array can be analyzed as a hexagonal structure with the pitch of 35 nm. On the (10) diffraction peak, we can see a fringe pattern, which indicates depth of the dot/hole. The dot/hole depths can be analyzed from the periodicity of the fringe pattern. The obtained nanostructures were compared with the results of AFM observation.

8324-27, Session 8

Challenges of SEM metrology at sub-10nm linewidth

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Challenges concerning SEM metrology at critical dimensions below 10 nm are discussed. At these dimensions, SEM images are normally noisy and their contrast is low; in addition, the signal formation mechanism is considerably different from that of regular samples. Electron scattering at this size range is strongly affected by the feature size, thickness, and the distance to the neighboring features, as well as beam voltage, beam size and material properties.

Experimental results and simulations are presented for the measurement of lines down to 4 nm. The features were fabricated using direct write EBL and nanoimprint. SEM images of the resulting patterns were taken. Two commercially available software tools were used for the analysis and simulation: a) model based, automatic extraction of CDs from SEM images and b) Monte Carlo simulations to model signal formation in SEM.

CHARIOT Monte Carlo software utilizes advanced physical models with an emphasis on slow secondary electrons; the results were used to understand the image formation at ultra-small feature sizes.

In the analysis of the SEM images, it was shown that commonly used CD extractions based on the brightness threshold method do not yield good results. Alternatively, myCD software utilizing analytical model of SEM produced more accurate data. In real time, the software builds a model of the SEM signal based on the input information regarding the SEM setup and materials; the model is used in the automatic extraction of contours and CD measurements. Results and challenges are discussed.

8324-28, Session 9

Contour metrology using critical dimension atomic force microscopy

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We describe scanning techniques and profile extraction methods used to obtain contours from critical dimension atomic force microscopes (CD AFM). We present the details of our technique, how we validate them, and some limitations. The goal is to show which data acquisition and analysis methods yields optimum contour information while preserving some of the strengths of CD AFM metrology.

Specifically, we look at scanning strategies, contour extraction methods, imaging modes, and ways to account for errors on sections of the feature that the CD-AFM probe cannot access. Our technique relies on identifying and extracting information called critical points from images taken in different scan directions to form a composite contour profile. Potential sources for error for this approach are quantified, and a rigorous uncertainty model is presented. The model includes treatment of error sources that are related to our scanning technique, and those that are specific to our analysis and contour extraction approach.

We present comparison of contours extracted using our technique to those obtained from the scanning electron microscope (SEM), and the helium ion microscope , which has the potential of achieving higher resolution and greater surface sensitivity than conventional SEM. We describe how the AFM images could be used to establish traceability for contour extracted from these other techniques.

8324-29, Session 9

On CDAFM bias related to probe bending

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Critical Dimension AFM is a widely used reference metrology. To characterize modern devices very small and flexible 15-20nm diameter probes are used. Several recent publications reported on uncontrolled and significant probe-to-probe bias variation during CD and sidewall angle measurements. Results obtained in this work suggest that probe bending can explain this CDAFM probe-to-probe bias variation. We developed and tested a model for bending of cylindrical probes. Sub-nanometer matching of the model results with experimental data for linewidth measurement is achieved. Watanabe's probe bending model was corrected and improved. Contributions from several new phenomena were considered: probe misalignment, near apex CNT diameter variation, probe bending before snap-in, distributed van der Waals-London force, etc. The procedure for extraction of Hamaker probe-surface interaction

energy from experimental probe bending data was developed. In contrast to results previously published by Watanabe et al. (2008) , the corrected model and new data evaluation methodology yield significantly lower Hamaker energies (1.5-6.1)eV. The model is used to optimize CNT and c-Si probe dimensions for high-aspect ratio measurements. Limits of high-aspect ratio AFM imaging are also discussed.

8324-30, Session 9

Capturing resist dissolution dynamics with AFM

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High-performance resistant materials are required to extend resolution limits. Monitoring and understanding dissolution, swelling, and material surface energy and stiffness during wet development and drying is essential. In-situ characterization tools with both the spatial and temporal resolution to monitor resist development are required. Atomic force microscopy is ideally suited for the task but typical image acquisition times are too long and in-situ imaging significantly increases tip sample interaction forces leading to deformation and loss of resolution. We have developed new AFM probes for operation in liquid that are orders of magnitude lower force noise than typical probes while retaining high resonance frequency for high speed imaging. We are also developing scan algorithms and image processing tools which enable 10 times faster frame rates than regular raster scanning for the same equipment. Together these tools enable the real-time monitoring of resist dissolution and swelling during development.

To enable gentle in-situ imaging we reduced force noise by reducing the fluid viscosity with a protective encasement for the cantilever. The cantilever operates in air and the probe protrudes from the encasement through the solution to the sample. Encased cantilevers have exceptionally high resonance frequency, Q factor, and detection sensitivity and low force noise enabling gentle high speed imaging.1 They also work in all commercial AFM systems without modification.

Present raster scan techniques are poorly matched to the instrument limitations of Atomic Force Microscopy. Serial data collection from the local probe makes image collection slow and unable to match the timescale of resist dissolution. One basic issue is the propensity of scientists to oversample data. We have used advanced image processing tools such as inpainting to recover high-resolution images from sparse quickly collected images to improve temporal resolution without applying more force or increasing bandwidth.2 We are also using non-raster scan algorithms such as spiral and cyclic scanning to increase temporal resolution. Spiral scanning better matches the mechanical limitations of the AFM scanner and allows higher tip velocities without distortion. Inpainting or interpolation is used to quickly create images from the nongrided data.3

The use of gentle high bandwidth probes and fast scanning algorithms will enable Atomic Force Microscopy to probe soft resist materials with high resolution and capture dynamics of dissolution during development.

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8324-31, Session 10

Sub-nanometer calibration of line width measurement and line edge detection by using STEM and sectional SEM

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The novel method of sub-nanometer accuracy (uncertainty) for the line width measurement and line edge detection using STEM (Scanning Transmission Electron Microscope) and sectional SEM images is proposed to calibrate CD-SEM line width measurement and standardization of line edge detection. In accordance with the proposed method, the traceability and reference metrology are established using Si lattice structures with metal coating.

A specimen of Si line and space is coated with metal, then, it is sliced on Si 110 surface as a thin specimen of 100 nm thickness by FIB (Focused Ion Beam) micro sampling system. Then the bright-field and dark-field STEM images of the specimen are obtained by STEM (HD-2700) with accelerating voltage of 200 kV and magnification of x150,000. The high magnification STEM images show Si lattice structures clearly.

The STEM image is transformed to the frequency domain image by 2D-FFT (Fast Fourier Transform). The image magnification is calculated by the relationship between the Si lattice structure and image pixels. The edge position on the each Si lattice line is defined at the 50% intensity between the metal coating area and SiO2 area. Then the detected line profiles are compared with the measurement results by CD-SEM and CD-AFM.

We applied the above methods to the 50 nm Si line width standard. The edge positions on the Si lattice are detected using the proposed method, and the line profile is also calculated with absolute positions. The expanded uncertainty of the line edge positions is evaluated from the uncertainty contributors of repeatability, image magnification, Si lattice counting by edge detection, environmental condition and so on. From these calculation, the expanded uncertainty (k = 3) will be estimated less than 0.5 nm (3 sigma).

8324-32, Session 10

Analysis and control of profile variation impact on focused ion-beam cross-sectional metrology

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The focused ion-beam (FIB) milling tool is an important component of reference metrology and process characterization, both as a supporting instrument for bulk sample preparation before forwarding to the transmission electron microscope and other instruments as an in situ measurement instrument using angled scanning electron microscopy (SEM). As features grow tighter and more demanding, reference metrology is needed, and this instrument will only grow in importance. Thus, the ability to extract accurate dimensional and profile information out of the cross-sectional faces produced by FIB milling is critical.

For features that demonstrate perfect symmetry in the plane of the cross section, analyzing images and extracting metrology data are straightforward. However, for industrial material, symmetry is not a safe assumption: as features shrink, the relative magnitude of line edge and sidewall roughness grows proportionally to the overall feature dimensions. Furthermore, with the introduction of more complex features such as 3D memory and FinFETs, the areas of highest interest, such as the intersections of wrap-around gates, cannot be assumed to be symmetrical in any given plane if cut placement is not precisely controlled. Therefore it is critical to establish the exact location and repeatability of the cross-section plane, both in terms of coordinate

placement and effective angle of the milled surface.

To this end, we will employ prepared, designed-in line edge roughness samples created in the Albany Nanotech facility using SEMATECH's AMAG6 metrology reticle. The samples are thoroughly characterized before being cut by a non-destructive, sidewall-scanning atomic force microscope (AFM) and then milled and measured under varying process and setup parameters using a single-beam FIB with angled SEM. One of our goals will be to establish methodologies that precisely align the cut planes of slice-and-view FIB milling to 3D-AFM scan lines to compare repeated sections throughout a feature. This, in turn, will give us a large amount of data to test the accuracy and repeatability of cut placement using various alignment and recipe setup schemes.

8324-33, Session 10

Automated S/TEM metrology on advanced semiconductor gate structures

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The increasing complexity of advanced semiconductor gate structures, including 3D transistors (e.g. FinFET or Tri-gate), shrinking line widths, thin films, and etch profiles, may require new metrology techniques beyond those currently offered by conventional CD-SEM or scatterometry, when used independently.

Automated STEM-based dimensional metrology (CD-STEM) was developed in recent years as a response to the complex 3D geometries, sub-surface and re-entrant features encountered in read and write head metrology in the hard disk drive (HDD) industry. Automated STEM-based metrology has been widely adopted, and has created a paradigm shift in the way S/TEM is viewed and used within the HDD industry. It has become the process of record for metrology of their most challenging processes. The volume of STEM images and data in the automated environment, coupled with the precision, has enabled HDD head manufacturers to dramatically reduce both development cycle time and the number of information turns in development for new products. For the first time HDD manufacturers have statistically significant data from their smallest features; enabling truly informed decision making.

Similar challenges are being presented in the development of advanced semiconductor device architectures. In this paper, the methodology and results of a detailed study using automated S/TEM metrology to investigate advanced semiconductor test vehicles containing FinFETs and fine pitch gate structures are presented. The tool set used for this work has the capability to prepare the S/TEM samples (a FIB/SEM DualBeam), image them in the S/TEM (CD-STEM) and then perform robust, automated, high resolution measurements.

Current metrology solutions such as scatterometry and CD-SEM offer excellent repeatability and throughput, but they each have limitations for investigating advanced three-dimensional integration schemes. For example, scatterometry does not offer the capability for line edge roughness analysis, and it is not possible to undertake sub-surface analysis using CD-SEM. The S/TEM solution discussed in this paper is intended to complement these other methodologies. S/TEM metrology provides improved resolution, sub-surface analysis capability and high spatial frequency capability that enables high accuracy line edge roughness measurements.

Manual metrology measurements can be made on current S/TEM imaging tools, but this technique is generally throughput limited, has poor repeatability and is prone to error. Automated S/TEM metrology solves these issues and enables high volume, high accuracy characterization of thin films, etch profiles, and 3D gate structures within wafer, wafer-to-wafer and lot-to-lot. This enables more process "learning per wafer" and faster process development.

The results of this study, obtained from 20nm FinFET test structures, reveal that fully automated S/TEM metrology is a viable technique, with good repeatability and robustness. Consistent automated throughput of 10 samples per hour was achieved, which is ground breaking compared with most conventional S/TEM based processes. Automated S/TEM

sample (lamella) preparation was developed with sufficient throughput and quality to support the automated CD-STEM.

This work is part of an ongoing development to provide further resolution and automation capability using S/TEM imaging. A comparison of the current automation capabilities to manual operator performance, relating to speed and repeatability, will be presented.

8324-34, Session 10

Compensation of CD-SEM image-distortion detected by View-Shift Method

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Local CD-SEM image distortion can be detected and compensated by unique technique: View-Shift method. As the design rule for semiconductor device is getting shrunk, metrology for the critical dimension scanning electron microscope (CD-SEM) is not only for measuring the dimension but also the shape, such as 2D contour of hot-spot pattern and OPC calibration-pattern. Accuracy of the shape metrology is dependent on distortion of CD-SEM image. The distortion of magnification can be measured by pitch-calibration method, that measures pitch of identical line patterns while shifting the identical pitch on the image. However, this method cannot measure distortion of shape, for instance, bending of a line that has uniform line that has uniform linewidth.

We invented View-Shift method for quick and accurate measurement of the image-distortion. In this method SEM images are taken on two areas separated by 100nm from each other on evaluation sample that has a lot of unique texture. Displacement of the unique texture between two images indicates the local image-distortion. In this work, we demonstrate a method to compensate the image-distortion detected by the View-Shift method. Edge-points dislocated by the image-distortion can be relocated according to the detected local-distortion. Even though the dislocation is not stable day-by-day, our compensation method can be practically applied, especially to contour metrology, with the View-Shift method that can be completed in a few minutes.

8324-35, Session 11

In-line metrology of 3D interconnect processes

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The continuous development of three-dimensional chip/wafer stacking technology has created a need for in-line metrology and characterizations. Many of these challenges are novel due to the relatively large variety of TSV (Through Silicon Vias) sizes and density, and new processes such as wafer thinning and stacked wafers bonding with alignment. This paper summarizes the developing metrology technologies that have been used during via-middle & via-last of 3D interconnect processes development at EOL/ITRI. While there is a variety of metrology and inspection applications for 3D interconnect processing, the main topics covered here are via CD/depth/profile measurement, thinned wafer thickness measurement and wafer warpage/bow/stress measurement.

A. Via CD/depth/profile measurement: Silicon wafers with 5-200 um diameter vias and a nominal depth from 30 to 150 um were studied. For via CD 10 um, a patented technique capturing images by an IR microscope from bottom of vias to the top of the vias is applied for the Top/bottom CD and depth measurements. For via CD 10 um, a modified normal incidence spectral reflectometer which is implemented a novel theoretical model and analysis algorithm is used for via depth/profile measurements.

B. Thinned wafer thickness measurement: The bonded wafer were ground down to several tens of microns during the wafer thinning

process. A self-developed objective based on the IR wavelength dependence of longitudinal chromatic aberrations is used to focus different wavelengths at different depth level. Thus the thinned wafer thickness and total thickness variations after thinning process were obtained by the reflectance spectrum analysis with no need of longitudinal translations.

C. Wafer warpage/bow/stress measurement: a new metrology module based on two sets of dual channel capacitive sensors module is use for wafer warpage/bow measurement. Metal films with varying thickness are deposited on the essentially planar Si wafer surfaces; the rapid planar to compression stress transition might be associated with a threshold phenomenon in terms of grain boundary relaxations. The conversion stress map is obtained based on the Stoney's formula and couple assumptions. The main purpose of this application is to optimize process control from minimizing warpage condition.

8324-36, Session 11

Measuring thermally induced void growth in conformally filled through silicon vias (TSVs) by laboratory x-ray microscopy

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Laboratory-based x-ray microscopy combined with computed tomography imaging is demonstrated to have advantages over other methods of inspecting through silicon vias (TSVs). The goal of this work is two-fold: (1) to understand the best imaging method for understanding void growth in TSVs during thermal processing and (2) to understand the mechanism of void growth in conformally filled TSVs. We show that the 8 keV x-rays used by the Nano X-ray Computed Tomography (NanoXCTTM) are capable of imaging voids inside filled vias before and after annealing without cross-sectioning the TSV.

The NanoXCTTM can obtain two-dimensional (2D) and three-dimensional (3D) tomographic images. The tomographic images are calculated from a series of 321 images taken at different incident angles, allowing 3D structural information of the sample to be obtained. With 3D structural information, we are able to internally inspect the TSV as well as its liner and barrier. Conformally and bottom up-filled TSV arrays (5 μm diameter) were inspected by x-ray microscopy before annealing. Pre-existing voids in the seamline were observed in conformally filled TSV before annealing, while bottom up-filled TSVs do not have the seamline or voids. The same TSV samples were repeatedly annealed at 200oC, 225oC, 250oC, and 300oC. After annealing, the x-ray micrograph of the same TSV array showed void growth in only the conformally filled TSV. In addition, the total volume of void growth increased with annealing temperature. Figure 1a-1d compares bottom up-filled and conformally filled samples before and after annealing, respectively.

8324-37, Session 11

Through-silicon via plating void metrology using focused ion-beam mill

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A focus ion beam (FIB)-SEM is demonstrated as a viable metrology tool to detect and characterize copper plating voids in through-silicon vias (TSVs) used in 3D integration. The FIB-SEM technique is compared with an inductively coupled-plasma source for the FIB-SEM (PFIB-SEM), demonstrating a 20-X improvement in milling times required for five micron diameter TSVs that are 50-microns deep (10:1 aspect ratio).

Process feed-back for detecting plating voids in copper-filled TSVs is limited by a lack of adequate in-line monitoring tools capable of detecting plating defects. PFIB-SEM is proposed as a fast, reliable method for non-

destructive monitoring of TSVs on whole wafers in the copper plating process with minimal sample preparation.

8324-38, Session 11

Measurement of through silicon via etch profile by dark-field optical microscope

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With rapid development of semiconductor industry, the 3D packaging has grown significantly in the past few years. In the 3D packaging, the through silicon via (TSV) is made by the Bosch process and used to provide multi-chip interconnects. Briefly, it involves forming deep vias in the chip at front-end processing, isolating them from the surrounding silicon, and filling them with metal. Then, the wafer is grounded from the backside to expose the vias from below. The steps described above must be monitored during the fabrications. Many of the steps are still in process development, thus process control is particular important. In this paper, we will focus on the metrology of via etch profile.

Currently there are no in-line TSV etch profile metrology tools suitable for use in high volume manufacturing. Cross-section SEM analysis can be utilized for process development, but it is a destructive technique. In our research, A dark-field optical microscope is developed to measure the via profile. It provides high contrast between the object and the surrounding field. As the name implies, the background is dark and the object is bright. Thus, a tiny structure of object can be viewed more clearly than a bright-field optical microscope. An analysis algorithm is developed to analyze the images of via which is measured by the dark-field microscope and then the profile of bottom and sidewall can be reconstructed. In the experiment, vias with nominal CD from 30 um to 150 um are measured, and the results are verified by the cross-section SEM.

8324-39, Session 11

Wafer level warpage characterization of 3D interconnect

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Wafer warpage is one of the most challenges for successfully subsequent processes in three-dimensional stacking integration which has been analyzed by considering different factors such as CTE mismatch, residual stress, and ground wafer thickness. It induced stress is one of the root causes leading to process and device failure such as delamination, cracking, within wafer uniformity, and defect density increasing. Therefore, it is crucial to measure the wafer warp before and after any stacking process. Full field optics methods, such as interferometer, fringe reflection method, CGS interferometer have been adopted for measuring out-of- plane deformation of a wafer.

In this work, we developed wafer level warpage characterization by a whole field fringe reflection method using phase shift algorithm. Silicon (Si) wafers of 8"and 12" diameters are used in the 3D interconnect process development. A set of periodic fringe patterns are projected onto the wafer surface and the reflection fringe images are recorded by a CCD camera. The fringe patterns are deformed due to the slope variation of the wafer surface. By analyzing the fringe shift, the wafer surface slope variation and 3D surface profile including tiny dimples and dents on a wafer can be reconstructed. The resolution is enhanced by an order of magnitude if the phase shifting setup and subsequent algorithms are employed. Experimental results show that bonding wafer warpage varies with bonding glue uniformity and grinding wafer thickness. Such measurement results can be used in the bonding process and wafer thinning process optimization to reduce wafer warpage.

8324-40, Session 11

Three-dimensional nanoscale metrology of CDs and TSVs using the TSOM method

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As the applications of nanotechnology become widespread, three-dimensional (3D) analysis of micro/nanostructures with nanoscale measurement resolution becomes increasingly important. There is a great need for 3D measurement tools that are economical, versatile, easy-to-use, non-destructive and provide high throughput nanoscale measurement resolution, especially for industrial applications in the current nanotech world. Here we present the relatively new "through-focus scanning optical microscopy" (TSOM) method that shows potential for 3D metrology [1]. By analyzing a set of through-focus images, the TSOM method potentially extends conventional optical microscopes for 3D metrology applications and provides nanoscale measurement sensitivity comparable to scatterometry, SEM and AFM in both lateral and vertical dimensions. Even though TSOM method, in principle, can be used to determine absolute dimensions, in this paper we concentrate on relative changes in the dimensions. As an example, for the first time we present experimental CD and sidewall angle analysis of nominally 45 nm to 55 nm wide isolated Si-on-Si lines with nanometer level measurement sensitivity using 546 nm wavelength illumination, which is beyond the classical Raleigh image resolution limit. Several important characteristics of the TSOM method that were previously identified using simulations have now been experimentally verified for the first time and are presented here. In principle, the TSOM method is able to analyze structures as large as 100 m in both lateral and vertical dimensions. The methodology is applicable in both optical transmission and reflection modes, and for target shapes ranging from simple nanoparticles to complex semiconductor memory structures, including buried structures under smooth transparent films, which are challenging using SEM and AFM. Several industries related to micro/nano technology are expected to benefit, such as semiconductor, micro and nano electro mechanical systems (MEMS/NEMS), data storage, photonics, biotechnology, and nanomanufacturing.

1. Ravikiran Attota, Ronald G. Dixson, John A. Kramar, James E. Potzick, András E. Vladár, Benjamin Bunday, Erik Novak, and Andrew Rudack, "TSOM Method for Semiconductor Metrology," Proc. of SPIE Vol. 7971, 79710T, 2011.

8324-41, Session 12

Overlay accuracy fundamentals

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Currently, the performance of overlay metrology is evaluated mainly based on random error contributions such as precision and TIS variability. With the expected shrinkage of the overlay metrology budget to < 0.5nm, it becomes crucial to include also systematic error contributions which affect the accuracy of the metrology. Here we discuss fundamental aspects of overlay accuracy and a methodology to improve accuracy significantly.

We identify overlay mark imperfections and their interaction with the metrology technology, as the main source of overlay inaccuracy. The most important type of mark imperfection is mark asymmetry. Overlay mark asymmetry leads to a geometrical ambiguity in the definition of overlay, which can be ~1nm or less. It is shown theoretically and in simulations that the metrology may enhance the effect of overlay mark asymmetry significantly and lead to metrology inaccuracy ~10nm, much larger than the geometrical ambiguity. The analysis is carried out for two different overlay metrology technologies: Imaging overlay and DBO (1st order diffraction based overlay). It is demonstrated that the sensitivity of DBO to overlay mark asymmetry is larger than the sensitivity of imaging overlay.

Finally, we show that a recently developed measurement quality metric

(Qmerit) serves as a valuable tool for improving overlay metrology accuracy. Experimental data demonstrates that the accuracy of imaging overlay can be improved to sub-nanometer values. We conclude that imaging overlay metrology complemented by appropriate use of Qmerit results in optimal overlay accuracy.

8324-42, Session 12

Size matters in overlay measurement

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Driven by an increase in intrafield sample density there is demand for a reduction in overlay target size to 10x10um or even smaller. But TMU increases as the target size is reduced, as has been demonstrated experimentally. The drive to deduce target size runs counter to that for lower measurement uncertainty.

In this paper we report results from a study of the ultimate capability of overlay measurement as a function of target size. Test targets were fabricated as simple resist on silicon patterns printed in a single lithography operation, removing as far as possible all process effects on measurement uncertainty. Because printing was performed in a single pass the expected overlay measurement at each target is zero.

Measurements were obtained from bar-in-bar and Blossom imaging overlay targets, and from scatterometry overlay targets. Fitting the measurement precision, TIS, TIS variation and the measurement standard deviation to a model of error sources in the measurement allows removal of tool measurement uncertainty, leaving a Residual Measurement Uncertainty (RMU).

RMU is 0.1nm for large targets but 1.0nm for 5x5μm imaging targets. RMU is independent of measurement technology and target design. It is wafer dependent and appears to be caused by line edge roughness in the pattern.

Reducing target size allows increased sample density, but with an increase in both TMU and the normally undetected RMU. We will discuss how to reduce the effect, which is necessary if small targets are to provide the benefits expected.

8324-43, Session 12

Feasibility study of matched machine overlay enhancement toward next-generation device development

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This study proposed the concept of high order field-by-field correction for matched machine overlay (MMO) error minimization and we have validated through experiments. Because scanners have unique grid fingerprint, MMO value between machines is higher than the one of single machine overlay(SMO). In some cases, the localized grid distortion is mainly distribute the MMO value. However, this localized grid distortion cannot be flatten by a normal correction method such as 10 parameter correction. Until now, in order to flat the localized grid distortion, ultimate correction capability can be realized by combining 6 parameter field-by-field correction and intra-field high order correction methods. In this case, however, the improvement of MMO value is limited due to the diversity of local distortion of each exposure field. Base on the budget estimation, we found that the correcting the field-by-field distortions with high order parameter was a successful way to lower the MMO value. In this study, 3rd order field-by-field correction functionality was investigated. High order parameters were extracted from each exposure field and then they were applied respectively. In result, the MMO error by this correction was decreased as compared with the existing ultimate method. It means that this correcting method is more effective to correct localized grid distortion. This results will be helpful to achieve the MMO specification for the next generation device.

8324-44, Session 12

Evaluation of a novel ultrasmall target technology supporting on-product overlay measurements

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The drive in industrial optical lithography to push for smaller overlay targets is two-fold: (1) metrology space consumption needs to be minimized to allow for maximum product real estate on the wafers; (2) ITRS roadmap requires aggressive overlay budgets where higher order exposure tool corrections are necessary, requiring dense intrafield sampling schemes. Therefore, overlay needs to be measured in-die for single die devices, which demands that ultra small targets can be placed in the close vicinity to the product structures. In such in-die application, it is important to keep the overlay measurement unaffected by the product structures surrounding the target. This is a challenging task. The technology and data discussed in this publication address the latest development in this area.

In this paper, overlay measurements with YieldStar metrology tool based on angle-resolved scatterometry are presented. The micro-diffraction-based overlay (uDBO) measurements are performed on target-size down to 10 x 10 um^2. Results on product wafers show that in-die targets located adjacent to product environment are well-measurable for overlay, with excellent correlation with nearby 30 x 60 um^2 (scribe-line) targets. 10 x 10 um^2 targets are 18 times smaller than typical scribe-line targets of 30 x 60 um^2. As expected, results show a clear scaling of the measurement noise with the inverse of the square-root of the grating area. Even so, a total-measurement-uncertainty (TMU) of below 0.5 nm was achieved for 10 x 10 um^2 targets in product environment.

The uDBO technology allows for selection of only the diffraction efficiency information from the grating, by efficiently separating it from the neighboring product structure reflections. This removes the need for a large clearance area around the ultra-small targets, so that they can be placed in the immediate vicinity of product structures. Furthermore, the uDBO targets are fully compatible with the product structures through segmentation. The uDBO implementation of YieldStar is insensitive for small position variations, and the technique is as insensitive to tool-induced-shift (TIS) as any other DBO techniques. The uDBO method is capable of filtering the grating edge effects from the desired signal. An additional benefit is that it allows for inspection of the local diffraction efficiency over the grating. Consequently, printing and process issues, such as micro-loading of the targets, can be identified and excluded from result in a relatively simple and non-destructive way. Furthermore, uDBO allows for simultaneous read-out of several small gratings that fit within the illumination spot, enhancing the throughput.

Concluding, the new uDBO technique allows for accurate metrology on ultra small targets (including in-die application), while retaining the excellent TMU performance of diffraction-based overlay metrology.

8324-45, Session 12

Application of DBM system to overlay and wiggling quantification in advanced process

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Because of the difference of shape and position between cell and overlay marks, cell to overlay mark position miss-match occur when there are some lens aberrations or mask registration errors. Therefore, the best way to measure overlay without error is to measure real cell

itself, if possible. The overlay of Double Patterning Technology(DPT) cell layer can be measured by analyzing the relative positioning of 2nd exposure pattern to 1st exposure pattern. But it is not possible to clearly distinguish 1st layer and 2nd layer in cell array image. But, since Design Based Metrology(DBM) can identify which cell is 1st or 2nd layer, it is possible to measure overlay error between 1st and 2nd layers using real cell image. In addition, as the pitch of line/space shrink, the metrology for wiggling becomes more important. But, there is no clean and systematic way to verify the wiggling level of small pitch line/space pattern.

In this paper, we will describe a metrology measuring the overlay of DPT cell pattern and the wiggling of line pattern. Die to DB matching method for e-beam inspection tool has been applied to measure the overlay of cell layers that use DPT and the wiggling of small line patterns. The experimental results of overlay and wiggling measurements are shown.

8324-46, Session 12

Quality indicators of image-based overlay

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The image quality of the overlay mark influences the overlay measurement significantly. According to the ITRS roadmap, the tolerance for overlay control is 6.4 nm and its measurement error budget is just 0.64 nm in 2012. So the overlay metrology requirement has become very stringent. To achieve the overlay capability of less than 5 nm, many factors such as scanner control, process improvement, reticle registration, APC, and metrology enhancements, need to be considered.

The total measurement uncertainty (TMU) for the overlay metrology is defined as the square root of square sum of three following indicators: the precision, the mean of the tool induced shift (TIS) 3-sigma, and tool-to-tool matching. They can describe the total overlay performance however all of them are calculated based on the overlay measurement values and are insufficient to guarantee a good overlay measurement. Hence new quality indicators need to be established to score the overlay measurement results. Two quality indicators, the contrast index (CI) and the asymmetry index (AI), are proposed in this paper. The CI is a crucial quality indicator that affects the overlay accuracy greatly. The AI, based on an imaging process with modified cross-correlation operation, shows alignment mark robustness in both the x and the y directions. The box-in-box overlay marks are measured to obtain the images. An overall matrix of quality indicators including the AI, CI and the three typical indicators is created to judge whether the overlay results are reliable and can be applied to monitoring of process variations and determination of the best recipe.

8324-47, Session 13

Scanning electron-microscope image processing for accurate analysis of line-edge and line-width roughness

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In order to accurately characterize line-edge and line-width roughness (LER/LWR), statistical noise and scanning-electron-microscope (SEM) image noise need to be reduced. We previously proposed guidelines for selecting measurement and analysis conditions for suppressing the former. The latter is usually reduced by averaging image pixels perpendicular (crosswise) or parallel (longitudinal) to pattern edges. Recently, we experimentally demonstrated that the longitudinal averaging appreciably distorts power spectral densities (PSDs) whereas the former does not. Here, we provide a theoretical support for these results. First, two-dimensionally arrayed image pixels were assumed in accordance with actual SEM images. Crosswise SEM signal distributions at these pixels were modeled using Gaussian functions with random noise. After averaging the pixels, pattern edges were located at maximal signal intensities. The PSDs of these edges agreed fairly well with experimental PSDs in both the crosswise and longitudinal averaging cases. In the

case of crosswise averaging, the theoretical PSDs agreed with each other except for white image-noise components. The variance of the noise-induced LWR first decreased exponentially with the number of crosswise averaged pixels, bottomed, and eventually increased. In the case of longitudinal averaging, the PSDs exhibited spurious oscillation and the noise components were not white. The noise variance decreased in an inverse proportion to the square root of the number of longitudinally averaged pixels. Because the PSDs in this case are thus complicated requiring us to use the time-consuming Monte-Carlo method in their simulation, we again propose to apply only the crosswise image-averaging method for suppressing the image-noise effect.

8324-48, Session 13

Static and dynamic photoresist shrinkage effects in EUV photoresists

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Photoresist shrinkage is an important systematic uncertainty source in critical dimension-scanning electron microscope (CD-SEM) metrology of lithographic features.[1] In terms of metrology gauge metrics, it influences both the precision and the accuracy of CD-SEM measurements, while locally damaging the sample. Minimization or elimination of shrinkage is desirable, yet elusive. This error source will furthermore be a factor in CD-SEM metrology on such polymer materials into the era of EUV lithography, such that learning to work around this issue will continue to be necessary.

Recent works have demonstrated improved understanding of the trends in the shrinkage response depending on electron beam and target parameters in the static measurement case.[2][3] Another recent work has highlighted a second mode of shrinkage that is apparent over time and progresses as a function of time between consecutive measurements, a form of "dynamic shrinkage" which appears to be activated by electron beam, where the activated feature perpetually and logarithmically shrinks.[4]

In this work, we will explore both the static and dynamic shrinkage behaviors on a few EUV photoresists of various types. Adherence of the static shrinkage behaviors will be tested for compliance to the SEMATECH shrinkage model [2][3] and further studies will confirm whether or not the dynamic effects are observable. Knowledge of secondary trends in the dynamic shrinkage case will also be further explored, including how these vary with electron beam energy, activation dose, feature size, and other parameters.

8324-49, Session 13

SEM metrology on bit patterned media nanoimprint template: issues and improvements

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Metrology using SEM provides crucial feedback in nanoimprint lithography (NIL) master and template replication processes due to its ease and flexibility of measuring features of various geometry and dimensions in the imprinted plane. In operation, SEM images are collected and feature locations are determined and the feature size/distribution and pitch variation are then calculated. Because the feature size on the templates is in the range of 12 to 20 nm, the assessment of measurement uncertainty and improvement on accuracy are very important.

In this work we examined two approaches to SEM measurements: regular measurements using brightness threshold method and SEM model based image analysis. Before tests, the beam size of SEM was characterized. BEAMETR test sample and software were used to measure beam size at various SEM settings; the most appropriate SEM setup was selected to acquire images of template features. A series of

images were obtained on 27 nm nominal pitch dot array patterns. The image intensity threshold method was used to extract needed metrology information and the measurement uncertainty was estimated. The same set of images then went through the second approach using model based algorithm processing through myCD-CH contact hole software with characterized beam parameters as part of modeling input. We compared measurement metrics from both approaches and identified the strength of model based analysis for its improvement in feature size and feature pitch measurement uncertainty and accuracy. The effect of pixel dosing on measurement uncertainty in both approaches was also discussed. TEM cross sections on the same features were done after SEM image collection. They served as accuracy reference for better understanding the source of measurement accuracy deviation.

8324-50, Session 13

Methodology for establishing CD-SEM robust metrology algorithm for development cycles applications

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ArF lithography is still the main technology in the most advanced process of semiconductor fabrication. The critical dimension (CD) of ArF resist patterns changes during measurement by CD-SEM (critical dimension-scanning electron microscope) because an ArF resist easily shrinks by electron beam irradiation. This CD change depends on several CD-SEM parameters. For example, a low electron dose and low acceleration voltage reduce shrinkage. However, they deteriorate the precision of CD-measurement due to degradation of the S/N ratio in the SEM images. So there is a trade-off relationship between shrinkage and precision. Therefore, the measurement condition of CD-SEM should be optimized in terms of shrinkage and precision. There are many imaging parameters and image processing parameters to be optimized. The authors proposed an optimization method for the trade-off relationship between shrinkage and precision that uses the Taguchi method. Also CD under the untested measurement condition was predicted by this method. In addition to shrinkage and precision, CD offset caused by changing the measurement condition of CD-SEM is also predicted. In this paper, the authors optimized imaging parameters such as acceleration voltage, number of frames and magnification of CD-SEM, and image processing parameters such as threshold, sum lines per point and smoothing parameter. As a result, the authors found that we can predict shrinkage, precision and CD offset for any combination of measurement parameter settings used in the 18 experiments with Taguchi method. This method should be a great help for finding the optimum measurement condition of CD-SEM.

8324-51, Session 14

Data feed-forward for improved optical CD and film metrology

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Advanced integrated circuit (IC) manufacturing requires high quality metrology for process disposition and control in order to achieve high yields. As the industry advances in high volume manufacturing of 3x and 2x nm nodes with the associated advanced materials and complex structures, understanding and reducing film and critical dimension (CD) measurement uncertainty is more critical than ever. Optical film metrology (OFM) for measurement of n & k, thickness, composition, etc. and optical CD (OCD) metrology for CD, sidewall angle (SWA), height, etc. utilize advanced structure modeling that includes fitting parameters of the device stack for multiple layers simultaneously. These methods have been proven and established in both R&D and high volume manufacturing scenarios. As film stacks and structures become more

complex and design tolerances shrink, however, additional parameters need to be included in the modeling, in some cases leading to reduced parameter precision, unwanted parameter correlation, and the like. In this paper we discuss the utilization of multiple metrology steps, and the feed forward of the derived parameters to subsequent metrology steps, and show improvements in measurement sensitivity and quality. Examples discussed in this work include logic FinFET, DRAM FinFET, SiGe on planar gate, and SiGe on FinFET. In addition, we discuss metrology integration schemes and fab integration concerns including metrology tool utilization and material routing.

8324-52, Session 14

Faster diffraction-based overlay measurements with smaller targets using 3D gratings

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Diffraction-based overlay (DBO) [1,2] technologies have been developed to address the overlay metrology challenges for 22nm technology node and beyond. Most DBO technologies require specially designed targets that consist of multiple measurement pads, which consume too much space and increase measurement time. The traditional empirical approach (eDBO) using normal incidence spectroscopic reflectometry (NISR)[3] relies on linear response of the reflectance with respect to overlay displacement within a small range. It offers convenience of quick recipe setup since there is no need to establish a model. However it requires three or four pads per direction (x or y) which adds burden to throughput and target size. Recent advances in modeling capability and computation power enabled mDBO[4], which allows overlay measurement with reduced number of pads, thus reducing measurement time and DBO target space. Previously single pad DBO measurement was demonstrated using 3D gratings with modeling approach. In this paper we further evaluate the performance of DBO measurements with targets that comprise of 3D gratings. We compare the DBO results using targets that vary in pitch and grating shapes. The impact of process variation on overlay measurements are studied by using a wafer with intentionally introduced focus and dose variation. We also compare DBO results with image-based overlay (IBO). We demonstrate the feasibility of single pad DBO measurements with faster throughput and smaller target size, which is particularly important in high volume manufacturing environment.

8324-53, Session 14

Novel prediction methodology in etched hole-patterning failure

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The continuous pattern size reduction of high-end semiconductor devices requires complex lithography process optimization. Especially the process optimization for fabricating etched hole pattern is complicated and time-consuming because the optimization should involve not only lithography but also etching process. One of the most severe problems in the fabrication of etched hole pattern is non-resolved type failure. In order to decrease the turn-around-time (TAT) of the process optimization for the eradication of the failure, the prediction of the failure of the etched hole pattern at the step of resist hole pattern formation is effective. Because the failure of the etched hole pattern cannot be predicted by the critical dimension (CD) of resist hole pattern, a new model which can predict the failure at the step of the resist hole pattern formation should be constructed.

Recently we have presented a model which predicts a resist patterning failure (bridge and collapse type) for lines and spaces (L/S) [1]. The model, which we call a "CD-NILS" model, is an application of the dicriminant analysis using resist CD and calculated normalized image log slope (NILS) as the inputs. The pattern failure is modeled and predicted with high accuracy using the CD-NILS model.

In this study, we present a model which predicts the non-resolved type failure of etched hole pattern from the CD-SEM measurement values of resist hole pattern. The model is an application of the discriminant analysis. The CD-SEM measurement values are, for instance, hole CD, variation of hole CD, and ellipticity of the hole shape. By the discriminant analysis, the best combination of the measurement values for the modeling is selected.

We used 130nm-pitch dense holes for the modeling. Firstly, resist hole pattern was formed by optical exposure using an immersion-type ArF scanner for focus-exposure matrix (FEM) conditions and resist development. Secondly, CD-SEM measurements were performed. The measurement values were hole CD`s (the threshold of secondary electron intensity is high, middle, and low), variation of hole CD, and ellipticity of the hole shape. Thirdly, the resist hole pattern was transferred to an silicon dioxide film by dry etching, and the non-resolved type failure of the etched hole pattern was inspected. Finally, in order to model and predict the failure, the discriminant analysis was performed for several kinds of combinations of the CD-SEM measurement values of the resist hole pattern as the inputs. The analysis showed that the best model was obtained using the combination of the following three measurement values: 1) resist hole CD (middle threshold), 2) the difference of resist hole CD between that of middle threshold and that of low threshold, 3) the ellipticity of the resist hole shape. The difference of resist hole CD between that of middle threshold and that of low threshold corresponded to a tapered resist profile. Therefore, the tapered resist profile was found to be one of the main causes of the non-resolved type failure. By using the model, the prediction accuracy of the failure of the etched hole pattern for the FEM conditions increased up to > 98 %, which was about 10 point higher than that of the conventional prediction model. By applying the model, the TAT of the lithography process optimization decreased down to 1 day, which is about 1/10 of that of conventional optimization methodology.

[1] S. Miyoshi et al., Proc. SPIE 7140 (2008) p.714011.

8324-54, Session 14

Direct-scatterometry-enabled lithography model calibration

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Optical scatterometry is crucial to advanced nodes due to its ability of non-destructively and rapidly retrieving accurate 3D profile information. In recent years, an angle-resolved polarized reflectometry-based scatterometry which can measure critical dimensions, overlay, and focus in single shot has been developed. In principle, a microscope objective collects the diffracted light, and the pupil image is collected by a detector. For the application of calibrating lithography models, a spectrum can be generated and fit to a database pre-characterized by rigorous electromagnetic simulation to estimate the dimensional parameters of developed resist profiles. The estimated dimensional parameters can then be used for model calibration. In this study, we propose a new usage of scatterometry by directly utilizing the pupil image to calibrate lithography models without needing dimensional parameter estimation. To test the feasibility and effectiveness of this new method by numerical simulation, a reference lithography process model is built with a set of parameter values complying with ITRS. A to-be-calibrated process model is initialized with a different set of parameter values from those of the reference model. Rigorous electromagnetic simulation is used to obtain the pupil images of the developed resist profiles predicted by both process models. An optimization algorithm iteratively reduces the difference between the pupil images by adjusting the set of parameter values of the to-be-calibrated process model until the pupil image difference satisfies a predefined converging criterion. This

method can be used to calibrate both rigorous first-principle models for process and equipment development and monitoring, and fast kernel-based models for full-chip proximity effect simulation and correction. Preliminary studies with both periodic and aperiodic layouts indicate that when the pupil image difference is minimized, the lithography model can be accurately calibrated.

8324-55, Session 15

Bridging CD metrology gaps of advanced patterning with assistance of nanomolding

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With the advancements in the semiconductor technology such as sub-22 nm nodes, advanced patterning processes such as double patterning, dual-damascene processes, EUV patterning and the complex 3D device architectures such as FinFET devices, via-in-trench, elongated contacts have challenged the current state of CD metrology in terms of capability, measurement quality and time-to-solution. Either the CD-metrology solution does not exists or it's not meeting the requirements resulting in gaps. CD-AFM providing reference metrology for resist and dielectric patterns is limited by the probe geometry. Due to probe geometry limitations CD-AFM is challenged in measuring the true bottom CD (< 15 nm from bottom) , sub-5 nm foot and undercut, sub-40 nm trenches, charged samples, small CD high aspect ratio structures like via in trench, deep trench (DT) and through silicon via (TSV), and various CDs of interest in the FinFET type 3D devices. TEM cross section is used as another reference metrology for dielectric patterns but it is subject to error in sample preparation (especially for contacts in sub-22 nm nodes) and limited statistics. CD-SEM and scatterometry which are workhorse metrology, needing reference metrology for measurement accuracy, also face challenge in measurement of advanced patterning.

In this paper we report an innovative CD metrology approach based on nanomolding of the master structure (via in trench, charged sample, trench < 40 nm, FinFET and EUV patterns) with potential to address various metrology gaps. Nanoscale molding of the master results in its inverted replica where the top CD and profile correspond to the bottom CD and profile of the master enabling the measurements using currently existing CD-AFM capabilities which otherwise is not possible. We studied different molding materials/methods on variety of master samples challenging the current metrology to investigate accuracy of replication which is the key requirement for the success of this approach. We compare the CD-AFM measurements of master and mold where the master can be measured via conventional CD-AFM to demonstrate accuracy of the approach. In cases where CD-AFM failed to measure master we deployed TEM cross sections as reference. Measurement of the common region in the master and molded replica allowed the self-referencing to ensure accuracy of the CD measurements. We investigated the limitations of this methodology as well. The molded structure reveals larger trench depth CD than conventional method. Nanomolding assisted measurement of CD in FinFET devices can help break the cross correlation of different parameters in scatterometry which is otherwise challenged in such cases.

In summary, the nanomolding assisted 3D CD-Metrology approach has shown the potential to turn some of the red sections in the ITRS metrology roadmap to yellow or green. This is a major step in bridging the metrology gap posed by the advanced patterning technology.

8324-56, Session 15

SEM imaging of ultrahigh aspect ratio trench and hole features

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As the semiconductor industry continues to behave by Moore's Law and increase functional density on microchips, true 3D memory devices will soon be manufactured. These can take many different forms, but a common building block will be ultra-high aspect ratio (ultra-HAR) etched features. Holes and trenches of 30:1, 40:1 or even 60:1 will enter production, with these etches being applied to various homogeneous and multi-layer stacks of Si and SiO2.[1] Logic devices also are now demanding higher aspect ratio contact holes to minimize capacitance and electrical breakdown paths. Note that these features should not be confused with thru silicon vias (TSV's) which are HAR features, but much larger and deeper; here we are considering features with bottom CDs at ITRS node sizes,[2]

In-line, non-destructive process control metrology of HAR holes and trenches has long been a known gap in metrology.[3] Because of complex charging issues, it is difficult to image the bottoms of 5-10:1 AR contact holes in oxide, and imaging beyond 10:1 has not yet been demonstrated. As lateral dimensions are reduced (and thus increasing confinement) this problem will be exacerbated.

In this work, we show simulated and experimental results that assess the feasibility of measuring such features using not only conventional Low Voltage-SEM, but also using higher beam energies and low vacuum conditions to ameliorate charging. Measurement of the bottom CD is the ultimate goal, but depth and profile are also parameters of interest. The NIST JMONSEL SEM simulation software [4,5] has been modified to incorporate the effects of charging. This virtual tool, combined with experimental measurements, help lead to an understanding of the important role that charging plays in this imaging problem.

8324-57, Session 15

Impacts of overlay correction model and metrology sampling scheme on device yield

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The purpose of this study is to investigate the advantages of process corrections of overlay errors using different reduced measurement wafer schemes, and the improvement in yield by applying optimized overlay correction models. A process layer where the overlay errors are sensitive to device yield is chosen for our experiment. One wafer lot that is randomly selected from production line is split into five groups; four groups with various wafer sampling schemes and overlay correction models, and one group with a programmed overlay error. The first three groups of this experiment are: (a) full wafer measurement, (b) baseline sampling scheme for production and (c) an optimized scheme. A high order process correction (HOPC) with 3rd -order tx and ty correction function is applied to these three sampling maps. More aggressive overlay correction model; intrafield high order process correction (iHOPC) with partial 3rd -order terms together with CPE (corrections per exposure), is applied to group (d). It leads to field-by-field overlay correction and is expected to have the best correction result. The correction models are generated with measured overlay data for each group and applied to the same group of wafers after they have been reworked, except for group (b), which is modeled by using the existing advanced process control (APC) system in the production line. To clearly clarify the correlation between overlay errors and yield, we introduced a large wafer scaling error (35nm in wafer edge) to wafers in group (e).

8324-58, Session 15

Characterization of ultrathin films by laser-induced sub-picosecond photoacoustics with coherent extreme-ultraviolet detection

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Photoacoustic measurements are powerful tools for characterizing thin films. Ultrafast lasers can be used to generate both surface acoustic waves (SAWs) and longitudinal acoustic waves (LAWs). SAWs propagate with a penetration depth proportional to the SAW wavelength ΛSAW, making them sensitive to the mechanical properties of thin films and interfaces. LAWs travel inside a material and measure properties in the z-direction. Therefore, when both waves are fully confined within a thin film and their dynamics directly observed, the 3D mechanical properties of the film can be precisely characterized.

In this paper we demonstrate the ability to characterize a 100nm thick film using extreme-ultraviolet (EUV) light. A set of 1D sub-optical nickel gratings of thickness 15nm, and periods ranging from 150nm to 1500nm, were patterned on a 100nm SiC:H film deposited on a silicon substrate. The grating patterns were heated by a femtosecond ti:sapphire laser pulse with a wavelength of 800nm, generating SAWs with wavelength set by the grating period, and LAWs that propagate into the grating, thin film and substrate. The coherent EUV probe beam at 29nm was generated from the same Ti:sapphire laser using high-order harmonic generation. By scanning the pump-probe time delay, we observe transient changes in diffraction of the EUV probe from the nano-grating. Since the wavelength of the EUV light is shorter than the grating period, the use of EUV light provides a much larger signal compared with traditional optical transient reflection techniques, allowing us to measure deflections in the picometer range.

The signal at both short and long time delays yields important information about the sample. In the first 100ps, similar signals show up for all samples: a fast oscillation corresponding to longitudinal waves within the 15nm thick nano-grating, followed by an echo at ~38ps corresponding to LAWs in the 100nm film. Knowledge of the film and nanostructure thickness allows us to determine the LAW speed for both the nanostructure (nickel) and the thin film.

On longer time scales, a SAW oscillation is observed, with frequency fSAW. The SAW velocity can be calculated from vSAW = ΛSAW* fSAW; this is sensitive to the mechanical properties of nano-grating, thin film and substrate. In large 1500nm gratings the SAWs propagate mostly in the silicon substrate at velocities of 4900 ± 380 m/s, matching silicon. However, for 150nm gratings, the SAWs are confined entirely within the thin film, yielding a velocity of 2800 ± 312 m/s. To separate the thin film from the nanostructure properties, we measure a series of gratings and use finite element simulations to match our measurements.

Combining both SAW and LAW velocities, the Young's modulus E and Poisson's ratio ν can be determined from elastic equations as E = 36 ± 5 GPa, close to the designed 30GPa; and ν = 0.24 ± 0.05, in a reasonable range for the SiC:H thin film.

In conclusion, we have demonstrated a new technique to precisely characterize mechanical properties of very thin films. This method can be used even for sub-10nm thin films given current nanofabrication techniques.

8324-116, Session 15

Technology review of silicon imagers-based application study for see-through silicon inspection and metrology

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While semiconductor fabrication technology hits harder on Moore's law to reduce fabrication node size to increase transistor density, 3D packaging technology becomes the most promising way for this purpose cost-effectively. Through-Silicon-Via (TSV), the newest generation of 3D packaging technology, drives see-through-silicon inspection and metrology as an essential quality control method. Due to spectral sensitivity, InGaAs based imagers are historically treated as the optimized option for such applications, even with lower resolution, larger pixel size, lower speed and a much higher cost compared to silicon based imagers.

This paper reviews the novel technologies that enable the silicon based imagers like CCD or CMOS for see-through silicon inspection and metrology applications. The wavelength range of 1.0um to 1.2um is the interesting window for silicon material optical properties, where absorption rate reduces dramatically, the transmittance increases accordingly and the reflectance keeps almost constant under Fresnel's law. Higher transmittance opens the opportunity to see-through silicon material; while absorption rate is proportional to silicon imagers' sensitivity. Therefore the Silicon imager based system inherently has a low SNR due to this trade-off, and reflections on the top surface typically dominate the signal back to camera and reduce SNR even worse. The new technologies successfully improve the silicon imager based system's SNR competitive to InGaAs system.

In addition, this paper compares the system level performances between InGaAs camera system and Silicon camera system to explore more advantages of Silicon imagers for this application.

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8325-01, Session 1

The evolution of lithography materials research from the perspective of a two term Conference Chair

R. Allen, IBM Almaden Research Ctr. (United States)

No abstract available

8325-02, Session 1

Factors that detemine the optimum dose for sub-20nm resist systems: DUV, EUV, and e-beam options

M. E. Preil, GLOBALFOUNDRIES Inc. (United States)

No abstract available

8325-03, Session 2

Optical performance comparison between negative tone development and positive tone development

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A negative tone development (NTD) process has been considered as the promising candidate for the smaller contact solution due to the remarkable image quality over a positive tone develop (PTD) process. However, it has not been investigated why NTD has higher optical performance than PTD yet. Contrast and ILS are compared for PTD and NTD with binary and phase shift mask (PSM) with splitting mask bias. In terms of contrast, PTD binary shows similar optical performance with NTD while it does not in terms of ILS. It is not appropriate any more with binary type of lithography, whose dose distribution around the threshold energy of photo resist is critical. Instead, ILS can depict it better than contrast from its definition. From the simulation results, ILS of NTD for the critical dimension (CD) target 50nm shows Contrast is simply a function of the mask bias. However ILS is varied with the CD target as well as the mask bias. From simulation results, it is clearly shown that NTD, especially PSM, provides better image quality with CD target 50nm. However the simulation of CD target 90nm provides different results. In conclusion, NTD is a suitable choice for the smaller CD target but it is not for the bigger CD target. Although there is optimum mask width difference between two different pitches, higher ILS is obtained with NTD PSM for smaller CD target, 50nm while higher ILS is achieved with PTD binary mask for bigger CD target, 90nm from both pitches.

8325-04, Session 2

Functional resist materials for negative tone development in advanced lithography

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Immersion lithography extension is one of the candidates for further pitch shrink down to 2x nm and below design rule, and negative tone development (NTD) is a good candidate for trench and C/H patterning. Tone reverse enables very nice optical image contrast with bright mask, and NTD process is one of the tone reverse process, using organic solvent as the developer. The resist material at exposed area has highly hydrophilic property due to generated carboxylic acid unit by the de-protection reaction, which can not dissolve to organic solvent.

Much thinner resist film process should be considered in further immersion lithography extension application. Therefore, we positioned etching resistance of resist material and substrate dependency to be studied with high priority. Since NTD process is based on the polarity change property of the resin in resist by the de-protection reaction, and the protection unit in resin has a role to afford etching resistance to resist film, this process has the risk of poor etching resistance essentially. Most of the commercial substrate materials applied to HVM are basically optimized to positive tone development (PTD) process that the hydrophobic blocked resin remains as a resist pattern, whereas the hydrophilic de-blocked resin remains in NTD process. In this paper, studies of etching resistance and substrate dependency of several resist platform will be reported, and concepts to improve these performance and new resist material showing better performance will be introduced.

8325-05, Session 2

Assessment of negative tone development challenges

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The objective of this work is to describe the advances in 193nm photoresists using negative tone developer and key manufacturability challenges associated with 20nm and beyond technology nodes.

Unlike positive tone resists which use protected polymer as the etch block, negative tone developer resists must adhere to a substrate with a cleaved polymer matrix; this poses adhesion and bonding challenges for this new patterning technology. This problem can be addressed when these photo resists are coated over silicon- containing anti-reflective coatings (SiARC) which are specifically tailored for compatibility with solvent developing resist. We characterized modified SiARC materials and found improvement in pattern collapse through pitches down to 100nm.

Fundamental studies have been carried out to understand the interactions among resist materials and developer. Different types of developers were evaluated and the best candidate was down selected

for contact holes and line space applications. The negative tone developer proximity behavior has been investigated through optical proximity correction (OPC) verification. The defectivity through wafer has been driven down from over 1000 adders/wafer to less than 100 adders/wafer by develop process optimization. Electric yield test has been conducted and compared between positive tone and negative tone developer strategies. In addition, we have done extensive experimental work to reduce negative tone developer volume per wafer to bring cost of ownership (CoO) to a value that is equal or even lower than that of positive tone CoO.

8325-07, Session 2

Evolution of negative tone development photoresists for ArF lithography

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Absent the implementation of EUV lithography, sub-22 nm node devices require alternative immersion optical lithographic processes to drive down to smaller feature sizes. The imaging process for dark field resist features benefits from using a bright field mask. Negative tone photoresist, via cross-linking chemistry, has been tried in the past in conjunction with bright field masks but they suffered from effects due to swelling in aqueous developer. An alternative when using BF masks is to change the developer to a solvent that does not dissolve the exposed photoresist after post-bake. This mode, termed negative tone development, extends ArF immersion lithography to the 14 nm regime by single or double-patterning methods, depending on the pitch being printed.

Extending ArF lithography requires the resist to provide acceptable performance under ever more stringent requirements. Contact holes can be better imaged in a single patterning process using a BF mask. The printed features, of course, require acceptable process latitude. This work shows results for dense pitch contacts used as the anchor feature. This is compared to the results for semi-dense features to show the large overlapping process latitude is possible. This set of features is chosen for demonstration because the only OPC possible is mask bias. The increased demands are placed on the resist are not only because CD and pitch are smaller, but that via layers require local interconnects to be printed on the same level. Part of the development for NTD resist is the convergence required for simultaneously printing line/space and contacts with the same resist. As a single BEOL photoresist, dense and isolated trench performance is also reported in this work. This supports via level patterning as well as the metal layers patterned in a LELE process. The latter enables the simplest implementation of double patterning for the additive metallization because it obviates the need for an image reversal step. This enables process simplicity as a necessary cost control for DPT. The chemistry of NTD photoresist has evolved over the past few years to the level of performance necessary for pilot line integration studies. In this paper the performance of a series of NTD resist systems is reported; with particular focus on process latitude, CDU, thickness control, LWR and resolution limit.

8325-05, Session 3

Modeling and simulation of acid diffusion in chemically amplified resists with polymer-bound acid generator

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The development status of extreme ultraviolet (EUV) lithography approaches the requirements for the high volume production of semiconductor devices with the minimum line width of 22 nm. It has been demonstrated using a conventional non-chemically amplified resist that the resolution of EUV lithography reaches 11 nm. However, not only resolution but also sensitivity is required for resist materials

used for high volume production. Therefore, the chemical amplification is an indispensable technology. However, the acid diffusion has been a problem in the development of high resolution chemically amplified resists. Recently, the acid generator, the anion of which is bound to the polymer through a covalent bond, has attracted much attention. It has been demonstrated that the chemically amplified resists with polymer-bound acid generators shows not only high resolution but also high sensitivity comparable to chemically amplified resists with conventional acid generators. This fact indicates that the deprotection of resist polymers is induced without the diffusion of anions. The chemically amplified resists with polymer-bound acid generators are a promising platform for nanofabrication below 16 nm node. In this study, we modeled and simulated the acid diffusion in chemically amplified resists with polymer-bound acid generators. The characteristics of deprotection under the condition that the anions are bound to the polymer is discussed. On the basis of simulation results, the feasibility of <16 nm fabrication with chemically amplified resists is discussed.

8325-06, Session 3

Contact edge roughness: effect of photo-acid generator on EUV resist

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In future, EUV lithography will play vital role in the lithography world. One of the main challenges for developing EUV resist is to satisfy ITRS targets for sidewall roughness. The majority of works have been devoted to the sidewall roughness of resist lines, the so-called line edge (or width) roughness (LER/LWR) issue. However, lithographic features are not characterized by line patterning only but also circular patterning such as contact holes and via, which are opened for connecting transistors to metal circuit layers. The roughness of contact holes (contact hole or edge Roughness, CHR/CER) may affect the Source/Drain (S/D) contact resistance and the saturation current, and may cause time-dependent dielectric breakdown (TDDB) due to the reduction of the space between contact and gate in a transistor [1-2]. Despite these device effects, the characterization of CER and the study of process and material effects on it are still in a preliminary phase [3].

In previous works, we developed a characterization methodology for CER [4] and applied it to study the effects of exposure dose in a EUV resist [5]. With the continuation of our previous work, we extent our study to analyze the effects of dose on CER for a new EUV resist in three formulations having different photo acid generator (PAG) concentrations.

First, the trends of experimental results are in conformity with previous analysis [4]: CD, RMS and   increase with dose while CD variation decreases and saturates over a critical dose (the roughness exponent remains fixed at ~0.65 in all cases). Thus, it seems that in CER we can improve simultaneously the sensitivity and roughness (contrary to LER) at the cost of having increased CD variation. To explain this behavior, one can argue that the sensitivity increase (lower doses) leads to smaller CD and shorter contact edge lengths and therefore to a decrease of rms. However, modeling results show that this effect can provide only a partial explanation of experimental results. The role of the relatively high acid diffusion length (~10nm) with respect to the small CD is also discussed in view of similar considerations in LER [6]

Secondly, the increase in PAG concentration for doses leading to a fixed CD (~45nm) is found to result in a) increase in CD variation, b) slight decrease and saturation of rms value and c) no important effect on correlation length and roughness exponent, Inspection of power spectra reveals the importance of low frequency components in the above dependencies.

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8325-07, Session 3

Mechanisms of LER degradation in ultrathin EUV resists

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The need to simultaneously improve the resolution, line-edge-roughness (LER) and sensitivity of EUV resists remains one of the most critical challenges in EUV lithography. While the theoretical limitations to the RLS trade-off have been well documented, this work has all been done at constant film thicknesses. Yet, we have found that decreasing film thickness causes degradation in LER. We previously studied the performance of four resists as a function of film thickness (two CNSE and two commercial resists) and found the LER degrades at a rate inversely proportional to the square root of thickness.1

Here, we present a mechanistic study into the cause of this LER degradation in thin films. We have studied four properties of resist films to better understand this thin-film LER problem: Substrate Interaction, Optical Density, Glass Transition and PAG Attachment. We have varied each of these properties systematically and compared the LER at film thicknesses of 90, 60, 40, 30 and 20 nm.

Substrate Interaction. One of the conclusions from our 2010 underlayer program was that the matching of CTE between resist and underlayer is very important in determining adhesion, line collapse and LER. Specifically, we found that the use of an underlayer can give ~1 nm improvement in LER over a primed silicon substrate. Here we have studied the effect that different substrates can have on the relationship of LER degradation as a function of film thickness.

Optical Density (OD). One variable we will explore is EUV optical density. The basic idea is that as resists get thinner, the total amount of light absorbed by the photoresist decreases. We have designed a series of four resists with similar lithographic properties (Rmin, Rmax, Eo), yet with a wide range of fluorine content (Figures 1A & B). We have evaluated these resists lithographically and have compared the LER degradation through film thickness as a function of OD.

Glass Transition (Tg). It has been well documented that the Tg of polymeric films can vary dramatically between film thicknesses of ~250 nm and 50 nm. We have designed four resists with similar lithographic properties (Rmin, Rmax, Eo), yet with a wide range of Tg (Figures 1C & D). We have evaluated these resists lithographically and have compared the LER degradation through film thickness as a function of Tg.

PAG Segregation. Lastly, we consider the possibility that the LER degradation in thin films may be due to PAG segregation. Since PAGs are known to segregate to different depths in resist films, we consider the possibility that the total volume of the film may influence the concentration that is able to develop at the top and bottom interfaces. We have evaluated three resists prepared by a commercial supplier that compares thin-film degradation of a polymer-bound PAG, a blended PAG, and a champion control resist. The LER performance of each resist has been compared as a function of film thickness.

8325-08, Session 3

Optimization of low-diffusion EUV resist for linewidth roughness and pattern collapse on various substrates

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The development of low acid diffusion chemically amplified resists has enabled the resolution of 20nm hp features at doses less than 15mj using EUV technology [figure 1]. However, linewidth roughness (LWR) and pattern collapse remain difficult challenges for EUV resists. This paper will focus on key parameters to optimize LWR such as PAG density and EUV resist absorption. The authors will also report on key parameters such as resist film quantum yield and its key role in LWR improvement. Another very important factor to improve LWR and pattern collapse is optimization of the underlying substrate. This paper will discuss the performance of our resists on primed Si, organic underlayers, and Si-containing underlayers. Figure 2 illustrates dramatic differences in substrate selection on resist performance. For Si underlayers, we see good overexposure performance for 28nm hp patterns with no line collapse down to 20nm CDs. For organic underlayers, we see collapse at the same condition. For Si, we see dramatic resist mottling and poor LWR. Measurement of key surface parameters such as water contact angle and coefficients of thermal expansion will be related to the relative pattern collapse margin and also the contribution to LWR. Lastly, we will discuss pattern transfer through these substrates and the relative improvements in LWR possible through etch recipe optimization.

8325-09, Session 3

EUV resist materials for 20nm and below half-pitch applications

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Extreme ultra violet (EUV) lithography process is one of the most promising candidates for 22 nm half pitch and below generation device manufacturing. It is supposed that implementation of EUV lithography to high volume manufacturing would start at 20 nm or more smaller pitch generation.

Many papers reported that it is important to reduce "resist blur" to achieve good resolution. Recently, very small blur numbers close to non-CAR resist system were found in polymer bound PAG type resist, having very short acid diffusion property coming from the bound PAG structure essentially. Additionally, it was found that polymer bound PAG type resist system has an advantage in dissolution contrast compared to polymer and PAG blending type resist system. However, we could not obtain 20 nm half pitch resolution with polymer bound PAG type so far.

Today, resist blur can easily be controlled with PAG design, therefore, new strategies are needed to obtain further tight pitch resolution. We already found that pattern collapse prevents tight pitch resolution by EB-lithography with polymer bound resist system. Pattern collapse can be avoided with reducing capillary force, improvement of adhesion of resist pattern and substrate, and enhancement of pattern hardness. This paper will report detail study to suppress pattern collapse, and some latest resist materials lead out from this study.

8325-10, Session 3

EUV resist development for 16nm half-pitch and beyond

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Extreme ultra-violet (EUV) lithography is targeted for 10nm logic technology node HVM in 2015 followed by 7nm node in 2017. Next-generation EUV resists are required to improve resolution limit down to less than 16 nm half pitch. To achieve such a performance, innovative materials such as molecular glass, polymer bound photo-acid generator and low acid diffusion length photo acid generators (PAG) are required. In this study we focused on innovative PAG material development through

the investigation of PAG acid diffusion length and PAG anion structure. Based on the results of this study, PAG plays a key function in order to resolve 16 nm half pitch and beyond. We are hopeful that these results would contribute to the EUV resist development at sub-16nm half pitch generation.

8325-11, Session 4

Overview: continuous evolution on double-patterning process

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Our proposed photo-resist core SADP has wide extendibility to Self-aligned Pitch-Tripling (SATP) and Pith-Quadrupling (SAQP) achieved 11nm hp as introduced in last SPIE[1]. PR-core technique will be most friendly for lithographer, because its property can be recognized on lithography view point.

ALD (Atomic Layer deposition) SiO2 process is the one of unique technique for multiple-patterning, and it is also useful for pitch-doubling in hole pattern[2].

Beside the invention of novel technical solutions, Double-patterning process is evolving steadily and its applicability is widened.

In this study, we would demonstrate newly developed multi-patterning techniques and optimize CD-uniformity, LWR and process latitude.

In this study, we would demonstrate newly developed multi-patterning techniques and optimize CD-uniformity, LWR and process latitude.

8325-12, Session 4

CD uniformity improvement on the self-aligned spacer double-patterning process by resist material modification

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Double patterning techniques (DPT) with 193nm immersion lithography are being thought to be one of the most promising candidates for the 22nm node and beyond. Especially, self-aligned spacer double patterning (SADP) has already been established as pitch doubling process and adapted in high volume manufacturing of NAND flash memory device. Moreover, ultra fine resolution can be obtained to repeat the SADP step twice as pitch quadrupling.

Simple cost effective SADP scheme which is resist core SADP process has already been demonstrated to obtain not only simple line and space patterning also trench and 2D patterning as well by Tokyo Electron LTD. [1, 2, 3] In this process, a SiO2 spacer film is being directly formed on a tri-layer resist stack. This pattern is then transcribed onto an underlying spin-on carbon (SOC) film and the final pattern is resolved on the TEOS film. Roughness and verticalness of resist pattern could affect the quality of SiO2 spacer film deposition and it could determine the CD uniformity of final pattern. Therefore, it's been thought that low line-width roughness (LWR) resist pattern and vertical resist profile make a better CD contribution and uniformity on final pattern.

Experimental results on SADP process will be shown and then it'll be discussed that specially designed resist materials which indicates small LWR and vertical profile could have a potential to improve CD uniformity after pitch splitting SADP process.

8325-13, Session 4

SADP for BEOL using chemical slimming with resist mandrel for beyond 22nm nodes

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The fundamental limits of optical lithography have driven semiconductor processing research to push the envelope. Double patterning (DP) techniques including litho-etch litho-etch (LELE), litho-litho etch (LLE), and self-aligned double patterning (SADP) have become standard vernacular for near term semiconductor processing as EUV comes readies itself for volume production. The challenge, even with techniques like LLE and SADP, remains that printing small lines on tight pitches beyond 22nm nodes for either LLE or SADP is not trivial. We have demonstrated a track-based slimming technique that can produce sub-25nm resist lines for either SADP or LLE DP processes. Our work includes results for varying shrink amounts at different target critical dimensions (CD) and for multiple pitches. We also investigated CD uniformity (CDU) and defectivity. In particular, optimization of the amount of slimming is critical as it allows for much greater process latitude at the lithography step. In addition to the lithography work, we have continued the processing for both integration schemes to include oxide deposition and etch for SADP and through etch performance for DP. We have demonstrated sub 45nm pitch structures. The wide variety of process uses, as well as the ability to achieve a large range of shrink amounts shows that track based slimming is a viable solution to achieve target CD and pitch values for sub 22nm technology node.

8325-14, Session 4

Synthesis and characterization of "two-stage" photobase generators for pitch-division lithography

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We previously reported on a new material that enables doubling the resolution of current exposure tools without any additional processing steps by a technique termed pitch division. The only modification required to achieve pitch division is a reformulation of the light-sensitive resist. The modified resist produces solubility responses at twice the frequency of the aerial image, thereby doubling the resolution. Pitch division is achieved by incorporating both a photo-acid generator (PAG) and a photo-base generator (PBG) in the resist formulation. Pitch division was successfully demonstrated at various pitch sizes with a NA of 0.85, which lead to an obtained k1 value of 0.20. While this works remarkably well, the line edge roughness (LER) of the images is unacceptable for commercial use. Computational studies predict the LER is partially the result of poor resist chemical contrast. The chemical contrast may be improved by increasing the slope of the net acid production as a function of exposure. One method to achieve a sharper slope in a pitch division formulation is to use a "two-stage" PBG, which undergoes a series of linked photolysis reactions before generating base. The desired base generator starts as a latent PBG that upon exposure to a photon becomes an active PBG. Subsequent exposure to a second photon leads to the generation of base. Ideally, this series of reactions would give a pseudo-quadratic generation of base, in turn leading to increased chemical contrast. In this paper we describe the design, synthesis, and characterization of the first generation of "two-stage" PBGs developed in our lab for use in pitch division lithography.

8325-15, Session 4

Applications of polymer blends DSA for lithography

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Directed self-assembly (DSA) provides an alternative approach to create sub-lithographic features. While most DSA demonstrations use block copolymers to create phase separated domains with precise periodicity, dimension, and morphology, the use of polymer blends provides a simple, lower-cost route to generate phase-separated polymer domains. Polymer blends system also could provide superior materials and process flexibility than those of block copolymer system. Without the intrinsic domain dimensions and symmetry characteristic of self-assembled block copolymers, polymer blends form conforming sub-lithographical polymer structures with a variety of geometries. Through the study of polymer blend DSA process, it was revealed that optimization of combination between polymer blends and guide-pattern feature provided valuable patterning for sub 10nm generation lithography. In this paper, we report DSA results based on the combination of binary polymer blends and various 193 nm resist topography including line-and-space, trench and hole features. The materials, processes and pattern transfer of guided polymer blend patterns will be discussed.

8325-16, Session 4

Comparison of directed self-assembly integrations

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Directed Self Assembly (DSA) is gaining momentum as a means for extending optical lithography past its current limits. There are many forms of the technology1-3, and it can be used for creating both line/space and hole patterns. As with any new technology, adoption of DSA faces several key challenges. These include creation of a new materials infrastructure, fabrication of new processing hardware, and the development of implementable integrations. Above all else, determining the lowest possible defect density remains the industry's most critical concern.

Over the past year, our team, working at IMEC, has explored various integrations for making 15 nm half-pitch line/space arrays. Both grapho- and chemi-epitaxy implementations have been investigated in order to discern which offers the best path to high volume manufacturing. This paper will discuss the manufacturing readiness of the various implementations by comparing the process margin for different DSA processing steps and defect density for the entirety of the flow. As part of this work, we will describe our method for using programmed defectivity on reticle to elucidate the mechanisms that drive self-assembly defectivity on wafer.

1 Cheng, Joy et al. "Simple and Versatile Methods to Integrate Directed Self-Assembly with Optical Lithography using a Polarity Switched Photoresist," ACS Nano, 4, 4815-4823, 2010.

2 Ross, Caroline et al. "Templated self-assembly of Si-containing block copolymers for nanoscale device fabrication" Proceedings of SPIE, Vol. 7637, 2011.

3 Liu, C. C. et al. "Integration of block copolymer directed assembly with 193 immersion lithography" JVSTB, Vol. 28, 2010.

8325-09, Session 5

Etch resistant block copolymers: high χ and orientation control

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Block copolymers self-assemble on the order of ca. 5-100 nm, making them potentially ideal candidates for a variety of next-generation lithographic applications, including bit-patterned media, field effect transistors and interlayer connects. The efficacy of these applications relies on block copolymer materials with feature dimensions smaller than those currently achievable with optical lithography, etch resistant domains to facilitate pattern transfer, and thin film orientation control. The aim of the present research is to produce materials that conform to all three of the aforementioned properties through a combination of materials design, synthesis, thin film processing and imaging. Since domain periodicity of microphase separation scales as $D \sim aN^{2/3}\chi^{1/6}$ (where N is the degree of polymerization and χ is a block-block interaction parameter) in the strong-segregation limit, larger χ and smaller N values lead to smaller periodicities and features. Thus, high χ materials are pursued herein to minimize pitch and feature dimensions. Thin film orientation control is achieved through a combination of thermal and solvent annealing techniques, coupled with surface energy control of the thin film interfaces. Finally, etch resistant materials are developed through the selective incorporation of heteroatoms, such as silicon, into one domain of the block copolymer, which has previously been shown to create etch resistant domains upon reactive ion etching.

8325-10, Session 5

Pattern scaling with directed self-assembly through lithography and etch process integration

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Directed self-assembly (DSA) has the potential to extend scaling for both line/space and hole patterns. DSA has shown the capability for pitch reduction (multiplication), hole shrinks, CD self-healing as well as a pathway towards LWR and pattern collapse improvement1-4. The current challenges for industry adoption are materials maturity, practical process integration, hardware capability, defect reduction and design integration. TEL has created close collaborations with customers, consortia and material suppliers to address these challenges with the long term goal of robust manufacturability.

This paper provides a wide range of DSA demonstrations to accommodate different device applications. Directed line/space patterns at 14 nm HP are demonstrated with PS-PMMA using both chemi and grapho-epitaxy process flows. To have higher resolution than a PS-PMMA system, a high chi material process is also explored. In addition, directed self-assembly processes have been applied to holes for both CD shrink and variation reduction.

In this paper, TEL's process solutions for both line/space and hole DSA process integrations are presented.

1 Herr, Dan, "Directed block copolymer self-assembly for nanoelectronics fabrication" J. Mater. Res., Vol. 26, No. 2, Jan 28, 2011.

2 Ross, Caroline, et. al., "Templated self-assembly of Si-containing block copolymers for nanoscale device fabrication" Proceedings of SPIE, Vol. 7637, 2011.

3 Liu, C. C. et al. "Integration of block copolymer directed assembly with 193 immersion lithography" JVSTB, Vol. 28, 2010.

4 Cheng, Joy, et. al. " Directed Self-Assembly for Lithography Applications" Proceedings of SPIE, Vol. 7972, 2011.

8325-11, Session 5

Solvent annealing strategies for the directed self-assembly of poly(styrene-b-dimethylsiloxane)

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Block copolymers (BCP) are capable of generating patterns with periods ranging from 10 - 100nm and are thus becoming an increasingly important method for nanofabrication. Here we report on the wide range of control that can be exhibited over a cylindrical phase poly(styrene-b-dimethylsiloxane) (PS-PDMS), which exhibits a large Flory-Huggins interaction parameter (~0.26) and shows good etch selectivity for pattern transfer to Si. This is done by using a custom built solvent annealing system in which multiple solvent vapor sources are controlled via mass flow controllers (0-10 sccm) to flow into an annealing chamber (quartz, 80 cm^3). Thin films (30-70 nm) of PS-PDMS together with films of each homopolymer are analyzed in situ using spectral reflectometry (250 - 1500 nm) to observe their swelling behavior. We map the phase behavior of the BCP by selectively etching the PS with an oxygen plasma (50 W) to reveal the PDMS morphology. By changing the flow rates and ratios of the different solvents (toluene, heptane) we are able to explore the range of achievble morphologies of a single BCP. This includes the vertical cylinder morphology which is valuable due to its higher aspect ratio for pattern transfer, but is very difficult to achieve in PS-PDMS due to the different surface energies of the blocks. We also show that thicker films (> 100nm) can form vertical cylinders by properly tuning the deswelling rate. Self-consistent field theory modeling of solvent incorporation is compared with these experimental results.

8325-12, Session 5

All-track directed self-assembly of block copolymers: process flow and origin of defects

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Directed Self-Assembly (DSA) of block copolymers is considered to be a potential lithographic solution to achieve higher feature densities than can be obtained by current lithographic techniques. However, it is still not well-established how amenable DSA of block copolymers is to an industrial fabrication environment in terms of defectivity and processing conditions. Beyond production-related challenges, precise manipulation of the geometrical and chemical properties over the substrate is essential to achieve high pattern fidelity upon the self-assembly process. Using our chemo-epitaxy DSA approach offers control over the surface properties of the slightly preferential brush material as well as those of the guiding structures. This allows for a detailed assessment of the critical material parameters for defect reduction. The precise control of environment afforded by industrial equipment allows for the selective analysis of material and process related boundary conditions and assessment of their effect on defect generation.

In this study, the first implementation of our previously reported DSA process for multiplication of feature density on an industrial fabrication track is described. Each process step in the fabrication of chemical nanopatterns is demonstrated with standard production tools. Critical inspection of the samples at each step of the process allows for the differentiation of defects originating from external sources, from those originating due to the block copolymer assembly process itself. Finally, this control of the substrate fabrication and inspection provides us with detailed experimental analysis into the origin of defects that occur during DSA of block copolymers under conditions relevant to the semiconductor industry.

8325-13, Session 5

Synthesis and characterization of self-assembling block copolymers containing fluorine groups

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In this work, we report the synthesis and characterization of new block copolymers containing a functional hydroxylated polar segment such as PHOST (4-hydroxystyrene) and a non-polar PTFEMA (2,2,2-trifluoroethyl methacrylate) segment. A PTFEMA segment can provide a strong degree of segregation between the constituent blocks and degradability of PTFEMA under either deep-UV or e-beam radiation. A block copolymer, PHOST-b-PTFEMA, with a total molecular weight of 1600~50000 g/mol and PTFEMA weight ratio of 31~50%, was designed and prepared by living anionic polymerization and subsequent hydrolytic deprotection as shown in Figure 1. Living anionic polymerization of the fluorinated methacrylate monomers and styrene monomer are well documented. To obtain a monodisperse PHOST block, tert-butyl ether protected monomer was used to avoid the termination of the living chain end. The structures of PtBuOS-PTFEMA and PHOST-b-PTFEMA were characterized by FT-IR and NMR spectroscopy. The thermal properties of the PtBuOS-PTFEMA and PHOST-b-PTFEMA were evaluated by TGA, DSC measurements. No significant weight loss was found for any of the polymer systems below 300 °C. Annealing in a nonselective solvent (THF) results in parallel orientation of cylindrical domains, while a mixed solvent (THF and dipropylene glycol methyl ether) leads to formation of a trapped spherical morphology. These thin films can be subjected to conventional lithography using e-beam and deep-UV radiation to generate integrated patterns. The formation of controlled microstructures, solvent annealing and patterning of poly(styrene)-b-poly(2,2,2-trifluoroethyl methacrylate) and poly(hydroxyl-ethyl methacrylate)-b-poly(methyl methacrylate) will also be discussed.

8325-17, Session 6

EUV resist formulation insight from stochastic lithography simulation

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We have recently proposed a stochastic resist model that can predict both the CD and LWR response for a variety of exposure conditions [1]. In this paper, we compare the model to the experimental data from Higgins et al [2]. In their study, Higgins et al. measured resolution, exposure latitude, dose-to-size, and LWR for an open resist formulation (Open Source 2, or "OS2") with a variety of PAG and quencher loadings. Because the formulation is known, we can determine the parameters in our model for this resist system with a minimal amount of empirical fitting, and then compare the model predictions with the experimental results. In addition, Higgins [3] also showed the dependence of LWR on film thickness for OS2. We show that our model can reproduce the trends in the data, and then demonstrate how simulation can be used to evaluate potential improvements to the resist formulation.

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8325-18, Session 6

Correlated surface roughening during photoresist development

C. A. Mack, Lithoguru.com (United States)

Stochastic models of lithography consider fundamental events such as the absorption of a photon or the chemical reaction of a molecule as stochastic events. As such, these events are described probabilistically, with the mean-field "rate" equation describing the probability that the event occurs. In previous work, the concepts of dynamical scaling in the study of kinetic roughness were applied to the problem of photoresist development in an open frame exposure. This paper will extend this previous work in several new ways.

First, simulations using correlated development rate noise (rather than the uncorrelated noise of previous work) will show whether kinetic roughness during development dominates the final lithographic roughness or whether the underlying development rate noise, coming from earlier stochastic processes such as exposure and reaction-diffusion, controls the final surface characteristics. Second, by slowing down the mean development rate while keeping the noise term high, simulations will indicate whether the KPZ universality class holds in this regime or a more complex depinning percolation class is needed. Finally, a thorough understanding of the uniform, open-frame development case will lead the way to the more difficult and interesting case of roughness formation during development in the presence of a steep development rate gradient, as is found at the edge of a photoresist line. Correlations in the underlying noise only partially influence final surface height correlations, depending on the mean development rate and the steepness of the development rate gradient at the final resist edge.

8325-19, Session 6

Mesoscale simulation of the line-edge structure during positive and negative tone resist development process

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Recent studies have shown that the semiconductor industry is seeking the possibility of utilizing both positive tone photoresist development (PTD) and negative tone photoresist development (NTD) to pursue ultimate pattern resolution. In particular, a minimal line edge roughness (LER) is one of the key performance indicators. Our current work is aimed at studying mechanisms of LER generation by simulating dynamics of polymer molecules in PTD and NTD.

In order to analyze dynamics of photoresist polymer chains during PTD and NTD, we apply a meso-scale simulation technique called Dissipative Particle Dynamics (DPD). In DPD method, several neighboring monomers in a polymer chain are represented by one DPD particle with soft interaction potentials to accelerate calculation of polymer dynamics. In our previous studies (SPIE 2009, 2010, 2011), we performed virtual lithography experiments to get the line pattern profile with molecular level polymer configuration. By changing the non-bonding interaction parameter between polymer and solvent in DPD method, we can control the dissolution rate and we can obtain the line patterns including line edge structures. This simulation has been useful in analyzing the correlation between the input aerial image contrast and the dynamics of LER generation. In the current work, in order to make this simulation method more practical for resist polymer design, we develop a method to tune the model parameters by calibrating to the experimental data obtained by development of actual resist polymers.

8325-20, Session 6

Line-pattern collapse mitigation status for EUV at 32nm HP and below

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Line pattern collapse (LPC) is becoming a critical concern as integrated circuit fabrication continues to advance towards the 22nm node and below. Tokyo Electron Limited (TEL) has been investigating LPC mitigation methods for many years including offering surfactant rinses to help reduce surface tension and Laplace pressures forces that are accompanied with traditional water rinses. However the ability to explore line pattern collapse mitigation techniques at EUV dimensions is experimentally limited by the cost and availability of EUV exposures. With this in mind, TEL has adopted a combined experimental and simulation approach to further exploring LPC mitigation methods.

With regards to the simulation approach, several analytical models have been proposed, but the analytical models based on Euler beam are limited in the complexity of profile and material assumption, as well as being used outside of the originally intended aspect ratio regime. The authors here explore the use of finite element methods in addition to Euler-beam models to understand resist collapse under typical EUV patterning conditions. The versatility of current finite-element techniques allows for exploration of resist material property effects, profile and geometry effects, surface versus bulk modulus effects, as well as rinse and surfactant rinse effects. This paper will discuss pattern-collapse trends and offer critical learning from this simulation approach, combined with experimental results from a EUV exposure system and CLEAN TRACK (TM) LITHIUS (TM) platform utilizing state of the art collapse mitigation methods.

8325-21, Session 6

Simultaneous calibration of acid diffusion and developer loading parameters for computational lithography

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This work is continuation of the goal to stream-line and improve precision of Analog components patterned in the lithographically sub-wavelength regime. The key enabler for sub-wavelength lithography with cost-effective RET has been model-based OPC. The traditional method of collecting empirical data and running correction recipes based on that is significantly challenged for Analog technologies. Not only is the Analog product space very broad, but same designs have to be patterned across imaging tools from different generation's. Moreover, some of the components require robust imaging capability with high aspect ratios followed by etch process with large iso-dense bias. The principal challenge for the modeler is to calibrate models with extracted optical parameters that reflect the imaging system used and the empirical resist parameters to be reasonably accurate. The first part of this requirement has been significantly met by the process of data-scaling with tremendous reduction of input measurements [1]. The major weakness in any method is the reliance on empirical calibration of the resist portion of the model.

The focus of this work is to utilize an independent data-set to extract the resist and etch parameters to simplify the procedure while improving the accuracy and portability. It is understood that even KrF resists can have developer loading (chemical flare) and acid diffusion parameters that range beyond the ambit of optical diffraction theory [2, 3]. Initially, the focus is to introduce the developer loading parameters for the resist. Depending on the magnitude of residual fitting error, the acid-quencher diffusion model will be considered to replace a straight Gaussian diffusion kernel [3]. To accomplish this, a set of gratings were generated. The main feature spacing is designed to lie beyond the ambit of what would be expected from a true optical diffraction theory. The main feature proximity is modulated by placement of sub and near resolution assist

features at a constant spacing. Modulating the size of the assist features results in varying the amount of photo-acid that is generated adjacent to the main feature. For cases where the features are sub-resolution, the acid formation is varied while maintaining a constant developer loading. With the near-resolution features, simultaneous variation in acid and developer loading would occur. Data as bias CD, representing developer loading for some of these structures was measured. The data shows that the extent of developer loading is as much as 15nm with the interaction range >3um. Even for 180nm node, this represents a significant amount of variation. As the model grid can be as fine as 1/16 nm, a threshold based model that incorporates this kernel should improve OPC.

8325-22, Session 7

Examination of the role of PAG structure on acid diffusion during sub-millisecond post exposure bake of chemically amplified photoresists

M. E. Krysak, B. Jung, M. O. Thompson, C. K. Ober, Cornell Univ. (United States)

Chemically amplified resists, the current workhorse of the semiconductor industry to achieve sub-30 nm resolution and beyond, require a post exposure bake (PEB) to complete the resist deprotection after photoacid generation. Sufficient time is needed to achieve the level of deprotection required for the solubility switching in a developer, but the seconds timeframe of conventional hot plate PEB leads to an undesirable amount of acid diffusion. We utilize a laser (CO2) based scanned heating system to achieve sub-millisecond to milliseconds heating durations with temperatures up to the thermal decomposition limit of the resist. This project focused on varying the structure of the photoacid generator (PAG) in order to investigate the role of PAG

structure on acid diffusion during sub-millisecond heating. A variety of PAGs with different anion sizes have been synthesized and tested on the laser system, and their lithographic performance and effect on acid diffusion has been studied. The effect of these new PAGs on resist performance will be shown. By understanding how PAG anion structure affects the resist performance, PAGs can be designed to further improve both resolution and sensitivity under laser PEB.

8325-23, Session 7

Kinetic rates of deprotection and diffusion in chemically amplified photoresist using sub-millisecond post exposure bake

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A line-focused continuous wave laser sources is used shift the temperature/time regime of post-exposure bakes from the seconds time frame at 90-150°C to sub-millisecond times at temperatures of 250-550°C. Under laser PEB (l-PEB), dwell times (heating durations) from 50 s to 10 ms have been explored, with the shortest times permitting characterization of CARs at temperatures as high as 800°C.

To understand the behavior of CARs during l-PEB, kinetic rates of deprotection and acid diffusion in model resist systems were quantitatively determined as a function of hot-plate PEB and l-PEB temperature and duration. Under l-PEB, the deprotection rate is inversely proportional to the UV dose (initial acid concentration) for temperatures between 300 and 450°C. In contrast, the deprotection rate scales inversely with the fourth power of the dose under hot-plate PEB. These data suggest simple first-order deprotection kinetics under l-PEB at high temperatures but much more complex kinetics at hot-plate temperatures. We suggest that the deprotection rate is limited by segmental dynamics in the vitrifying resist matrix near the glass transition temperature, but becomes simple Arrhenius far above Tg. Acid diffusivity at hot-plate temperatures follows the expected William-Landel-Ferry (WLF) model

near the resist's Tg. As the temperature approaches 325°C, the diffusivity under l-PEB transitions from WLF to a simple Arrhenius behavior.

These fundamental measurements provide a basis for understanding previously observed sensitivity enhancements (up to a factor of 3 for comparable resolutions) and the reduced LWR (as much as 20%) during l-PEB under DUV and EUV exposures.

8325-24, Session 7

Contrast improvement with balanced diffusion control of PAG and PDB

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For semiconductor manufacturing of the 20-nm node and beyond, immersion lithography is still an important option for process development and production. As feature size reaches the resolution limit, many resolution enhancement techniques and processes are developed to meet the stringent imaging requirements. However, as the optical contrast was poor for 20nm application, the optimizing conditions for DOF, MEEF, LWR, 2D features, top view profile, and defect become a challenge for manufacturing. The low k1 induced poor ADI top view profile makes it quite difficult for KLA defect review. Such difficulty is dominated by the end-to-end spindle profile. Moreover, its AEI is unacceptable as well. .

From previous publications, the photo-decompose base (PDB) is proven effective to enhance the contrast and improve the DOF by more than 50% from conventional quenchers. In this paper, we report further improvement of the litho performance from controlling the PAG and the PDB diffusion lengths. By selecting similar polarity and size for the PAG and PDB, the diffusion length can be well controlled. We show profile improvement from rounding to vertical by select a higher diffusion length for the PDB than that of the PAG. The scattering bar printing window is also improved. With the PAG and the PDB sharing the same diffusion length, the MEEF, LWR, CDU, and end-to-end profile are dramatically improved. Application of this new technology on L/S and C/H resist will be discussed.

8325-25, Session 7

An in situ analysis of the resist-pattern formation process

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As the resist lithographic targets for resolution, line width roughness (LWR), and sensitivity move to fine patterning beyond the 16nm half-pitch lines and spaces (L/S), a re-thinking of present resist formulations / platforms and related processes is necessary. On material research, investigations on alternative chemistries such as; low molecular [1], photo acid generator (PAG)-bound [2], inorganic resists [3], etc. have shown potential results. For resist related processes; non-conventional baking methods, developer, and rinse solutions have been proposed [1] to further improve the lithographic performance of presently available resists. This shift to new resist materials / processes suggests the need for more fundamental studies in better understanding and achieving the stringent targets required.

The characterization of the pattern formation process after exposure (resist dissolution, rinse, drying, etc.) is one fundamental area of research that has been continuously investigated for further enhancement of resist materials. Recent results related to the optimization of these processes indicate possible solutions to the LWR issue [4], which presently has become one of the most difficult lithographic targets [1].

In previous papers, the authors have proposed the use of high speed atomic force microscopy (HS-AFM) for the in situ analysis of resist dissolution and characterization during the rinse process [1]. With this method, a visual appreciation of these chemical reactions was made

possible [5]. Initial investigations on resist dissolution have shown resist film swelling of EUV exposed areas as a main factor in pattern collapse that occurs in high performance acryl-based polymer resists [6]. These results also showed how the use of an alternative developer, tetrabutylammonium hydroxide (TBAH) [7], suppresses this film swelling phenomenon, and in effect pattern collapse, thus further extending the resolution limits of the acryl-based resist to the lower 2x-nm L/S. During the rinse process, results obtained using a reconfigured HS-AFM analysis system showed how alternative rinse solutions (surfactant rinse) helps in suppressing resist film swelling during this process [8].

Utilizing the same system, initial work has been started on the analysis of resist patterns during the drying process after rinse. The addition of this new capability enables the analysis of the whole resist pattern formation process after exposure. This may allow the visual appreciation of the formation of LWR during these processes, which could translate to new pointers for its minimization.

During the conference, a detailed discussion on the analysis of the resist pattern formation process using the HS-AFM will be presented. Utilizing this analysis method, a comparative study on resist pattern formation between presently utilized resist chemical platforms will also be shown. Likewise, fundamental studies on the dissolution characteristics of ultrathin resists (film thickness lesser than 20nm) will be presented.

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8325-26, Session 7

Understanding dissolution behavior of 193nm photoresists in organic solvent developers

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Herein, we investigate the dissolution behavior of 193-nm chemically amplified resist in different organic solvents at a mechanistic level. We previously reported the effect of solvent developers on the negative tone development (NTD) process in both dry and immersion lithography, and demonstrated various resist performance parameters such as photospeed, critical dimension uniformity, and dissolution rate contrast are strongly affected by chemical nature of the organic developer. We further pursued the investigation by examining the dependence of resist dissolution behavior on both processing variables and molecular parameters in both ketone and acetate based solvents. The effects of monomer structure, and resist composition, and the effects of processing conditions such as post exposure bake temperature and developer temperatures on dissolution properties were evaluated by using laser interferometry and quartz crystal microbalance. We have found that dissolution behaviors of methacrylate based resists and acetal based resists are significantly different in different organic solvent developers, affecting their resist performance. We also examined the different dissolution rate-derived parameters and related them to lithographic performance. For example, slope Tan ϕ of the steepest region of the dissolution rate contrast curve can provide useful information for critical dimension control such as line width roughness (LWR) and critical dimension uniformity (CDU). In summary, this study reveals that understanding the resist dissolution behavior in organic solvents helps to optimize the NTD process for higher resolution imaging.

8325-27, Session 7

Critical material properties for pattern collapse mitigation

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Modern high-resolution lithography, which employs a chemically amplified resist (CAR) and either a 193 or a 13.5 nm wavelength, is often limited by pattern collapse. While the general concepts of how CAR platforms work are widely understood, the influence of composition on pattern collapse has been studied to a lesser extent. In addition, the subject matter is often further complicated by non-disclosure of the resist chemistry used in the lithographic evaluation.

Open-source photoresist platforms can be beneficial for fundamental studies on how individual components influence pattern collapse. Such platforms should mimic a typical CAR, containing - apart from the polymer - additional components such as photo acid generators (PAGs) and base quenchers.

In this paper, 193 nm and EUVL open-source platforms are presented wherein the chemistry, composition, and concentration are all disclosed. With the aim to fundamentally understand how resist composition and behavior influences pattern collapse, the molecular weight of the polymer backbone and the concentration of both PAG and base quencher were varied. These sets of resists were exposed using both high-end 193 nm and EUV scanners. The results are presented in such a way that the probability of pattern collapse is derived as a function of the exposure wavelength, chemistry, and component concentrations.

8325-28, Session 7

Accelerated purge drying to prevent pattern collapse without surfactant rinse for high-aspect ratio resist patterns

T. Goto, C. N. Pieczulewski, A. Morita, SOKUDO Co., Ltd. (Japan)

Semiconductor lithography processing is a key enabler of integrated circuit (IC) miniaturization. As a result resist pattern feature sizes continue to progressively shrink year-to-year. However, miniaturization of the resist pattern often leads to challenging high aspect ratio patterns which have a tendency to collapse during the develop process causing lower yields in IC manufacturing process. Historically, lithography processes which are discovered to have resist pattern collapse phenomenon during develop process are often resolved by using a surfactant rinse agent blended with the developer or post-develop rinse water. Unfortunately, surfactant rinse agents are also known to cause their own wafer surface defects created by surfactant chemistry residuals remaining behind after develop processing.

We developed a pattern collapse prevention method which does not use a surfactant rinse agent. The pattern collapse phenomenon is commonly expressed by the stress applied on the pattern with key components including "the surface tension of the rinse agent" and "contact angle between pattern surface and rinse agent." Using a surfactant as a rinse agent is targeted at reducing "the surface tension of the rinse agent." However, it is also reported that pattern collapse is influenced by the rinse agent drying process. The pattern collapse prevention method of focus in this report evaluates the "the drying rate of a rinse agent" and "the accumulated stress on a pattern" in relation to the pattern collapse phenomenon. By increasing the drying rate of the rinse agent, the integrated stress on the pattern is reduced allowing for the pattern collapse prevention. Dramatically speeding-up the drying rate of rinse agent by Accelerated Purge (AP) drying integrated into a photolithography track develop module and without using a surfactant rinse agent we have confirmed the ability to control the pattern collapse phenomenon. With AP drying we have also confirmed further defect reduction that would normally result from rinse agent remaining on a wafer, which has been significantly improved by the super-fast drying

process. AP drying is a promising technology which can control pattern collapse phenomenon without using a surfactant rinse agent with advantages in yield improvement, process time reduction and chemical cost reduction.

8325-50, Poster Session

EUV photoresists formed by molecular layer deposition with sub-100nm resolution

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EUV lithography introduces many challenges to photoresist materials, particularly the need for photoresists to be less than 50 nm thick, highly homogeneous, and with good photospeed, resolution and line edge roughness. Current spin-on photoresists face difficulty in meeting these requirements, leading to interest in development of alternative resist materials. We demonstrate that the technique of molecular layer deposition (MLD) can be used to gain precise control over photoresist film thickness and composition, and hence is an attractive method for synthesizing EUV resists. As an analogue to atomic layer deposition (ALD), MLD utilizes a sequence of self-limiting reactions of organic precursors to directly build a thin film on a substrate surface. In this work, polyurea thin films are deposited using 1,4-butylene diisocyanate (BDIC) and 2,2'-(propane-2,2-diylbis(oxy))diethanamine (PDDE), by which acid-labile ketal groups are embedded in the backbone of the organic film. Ellipsometry measurements show that the film thickness has a linear dependence on the number of MLD cycles. The presence of the urea linkage is observed by infrared spectroscopy, and x-ray photoelectron spectroscopy confirms that the films are deposited with stoichiometric composition. Upon incorporating a photoacid generator (triphenylsulfonium triflate) into the MLD film via a soak step, the MLD photoresists become photoactive. In place of EUV exposure, electron-beam lithographic tests are carried on the MLD photoresists to mimic the secondary electron effects generated in EUV exposure. Preliminary results show that the MLD photoresists have a good sensitivity of 30 μC/cm2 with a 100kV e-beam exposure system, and a patterned line resolution of sub-100 nm.

8325-51, Poster Session

Limitation of blend type of resist platform on EUV lithography

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Extreme Ultra Violet Lithography (EUVL) generation is being thought to be one of the most promising semiconductor fabrication technologies for the 22 nm node and beyond. On the other hand, blend type of chemically amplified (CA) resist which is formulated with polarity changeable polymer, photo-acid generator (PAG) and base quencher is being widely used for 248 nm and 193 nm lithography technology. For EUV resist development it looks suitable to start with this platform to consider what major issues on realistic EUV process are and how resist performance could be improved to overcome such challenges because this platform is based on very mature technology and can allow us to change resist components very easily at the first era of EUV resist development.

Under existence of huge flare and out-of-band (OoB) radiation on EUV exposure process, it's critical to mitigate film thickness loss and top profile roughness of resist feature from device manufacturing point of view. This could be easily maintained by changing hydrophobicity of PAG structure. Then in order to achieve enough high sensitivity it's well-known that increase in PAG loading ratio should be good way however this was not successful due to the plasticization effect of PAG molecules resulting in decrease in film glass transition temperature in case of blend type of CA resist. Experimental results on blend platform will be shown and then it'll be discussed that polymer bound PAG platform could have a potential to overcome challenges shown on blend resist platform.

8325-52, Poster Session

High-resolution nonchemically amplified resists for extreme-ultraviolet lithography

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Chemically amplified resists (CARs) utilizing acid-catalyzed reactions have been widely used as photoresists to achieve practical throughput. However, CARs suffer from serious problems such as the appearance of an anomalous insoluble skin, T-top, or line-width shift caused by the acid diffusion in CAR films and the air-borne contamination when the post-exposure bake is delayed and these post-exposure delay problems make it difficult to fabricate nanometer-scale patterns.

In this study, we propose a novel non-CAR using photoactive diazo-groups and hydroxyl-functionalized compounds. Several PACs which contain diazoketo groups have been reported for deep UV lithography. Diazo-functionalized polymer is a proper resist that is processable without photoacid generator and induces both photobleaching and polarity change upon exposure. Therefore, there are no serious chemically amplified system problems which hinder fabrication of nanometer-scale patterns. The polymers were synthesized by radical copolymerization of 2-(2-diazo-3-oxo-butyryloxy)-ethyl methacrylate, and 2-hydroxyethyl methacrylate. Using EUV radiation, 70 nm line patterns were obtained. Non-CARs are crucial technology for the high-volume manufacture of semiconductor devices and a key technology for the next generation lithography.

8325-53, Poster Session

Theoretical study on structural effects of polymer ionization for EUV resist

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Upon EUV exposure to the polymer in resist, the ionization of the polymer occurs and the secondary electron generates. The secondary electron from the polymer causes the reaction of photoacid generator and the photoacid generates1. Thus, the sensitivity of resist for EUV depends on the ionization of the polymer and the electron affinity of photoacid generator. We so far theoretically calculated electron affinity of photoacid generator and found that fluorine atom enhances the electron affinity of photoacid generators.

In this paper, the study of polymer was performed. During the ionization, the radical cation of polymer is produced. As the radical cation is unstable, the energy barrier between before and after ionization of polymer was calculated. Smaller energy barrier means more products of secondary electrons, which leads to the increase of resist sensitivity. Gaussian 09 calculation program based on Density Functional Theory (DFT) was used. High order basis function of molecules of 6-31G polarized was applied to quantitatively calculate the energy.

The typical polymers for EUV resist were investigated. We found polyhydroxystyrene has less energy barrier of ionization than poly(acrylic acid) , which was coincided with more unstable radical cation of poly(acrylic acid). As the effect of acid leaving groups of polyhydroxystyrene, the protection of hydroxy group of polyhydroxystyrene resulted in the large increase of energy barrier. It is found that stable acid leaving group leads to less energy barrier.

Substituent effect on polymers will be also discussed and we will propose the effective polymers for EUV resist.

8325-54, Poster Session

Development of a negative tone molecular resists based on hydroxyphenyl calix[4] resorcinarene derivative for EUVL

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EUV lithography (EUVL) and Electron Beam Lithography (EBL) are significant benefits to multiple technology rules (22 nm, and below). The 2x nm half-pitch patterns require simultaneously the resist characteristics: resolution, high sensitivity, low line edge roughness (LER), no pattern collapse, and low outgassing. The high-quality EUV resists has recently been one of top three critical issues in EUVL.

The polymer resists seemed to be already established. However, it was difficult to meet these requirements by polymer resists from the view point of three respects: large molecular size, twisted molecular-chains, and non-uniformed molecular compositions. Therefore, molecular resists were regarded as the one of the promising methods for obtaining resist patterns with high sensitivity and low LER.

Therefore, we have been developing negative-tone molecular resist based on hydroxyphenyl calix[4]resorcinarene derivative. In our previous study, we could comfirm the excellent patterns with high resolution and small LER by using this resist by EBL and EUVL. However the pattern collapse was shown at sub 30 nm half-pitch, so it should be improved.

Herein we report a new negative-tone molecular resist based on hydroxyphenyl calix[4]resorcinarene derivative synthesized by the condensation of alkylcyclohexyloxyphenol and hydroxybenzaldehyde, CR-1.

The EB patterning result showed that the resist containing CR-1 on an organic layer substrate had sensitivity of 180μC/cm2 for 20 nm half-pitch without pattern collapse. Futhermore sub 20 nm half-pitch patterns were partially resolved.

We will present the EUV patterning result at the presentation.

8325-55, Poster Session

A novel single-component resist based on poly (4-hydroxylstyrene) applicable for EUV lithography

J. Liu, L. Wang, Beijing Normal Univ. (China)

With the growing demand of the electronics industry for smaller, higher resolution features, next generation lithographic techniques, such as Extreme Ultraviolet(EUV) lithography has caused widely attention from scientists. As the EUV absorption is determined by the nature of atoms but not by the structure of molecules, poly(4-hydroxylstyrene)(PHS) based resists can be employed and performed in EUV lithography. The poor compatibility in two-component or three-component resists between the PAGs and the polymer matrix could cause acid diffusion and non-uniform deprotection reaction and some other problems. In order to improve the performance of the resists, single-component resist system has been proposed which is generally constructed by the polymers consisting of two major functional components, photoacid-generating unit and the acid-labile group. In this paper, PHS was used as raw material and a novel polymer was synthesized with triflate sulfonuium salt group attached onto part of the benzene rings by chemical reactions and the hydroxy groups partly protected by t-BOC, which can be used as single-component chemically amplified photoresist applicable for EUV lithography. The polymer material can be dissolved in common resist solvents. The thermal stability, acidolysis and photolithographic property of the resist material were investigated.

8325-56, Poster Session

Laser anneal PEB: a viable route to RLS improvement?

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In recent years, researchers have investigated a variety of processing techniques - looking to find anything which offers the promise of simultaneous improvement in resolution, LWR, and sensitivity (RLS). One intriguing approach, presented by Cornell University, is the use of a laser annealing tool (CO2 laser, lambda = 10.6 um) for sub-millisecond post exposure bakes (PEBs).[1,2] Using both DUV and EUVL exposures, the authors demonstrated that a laser-anneal PEB could outperform their hot plate PEB control sample. They postulate that the shorter time / higher temperature regime (which can only be probed via a laser annealing technique) modifies the deprotection and diffusion kinetics which may be helpful in the industry's push to ever-tightening patterning requirements.

In the present work, we use advanced commercial-grade toolsets for both the lithography (an ASML ADT or Alpha-Demo Tool (EUVL)[3], an ASML NXE3100[4] (EUVL), and a ASML 750 (KrF)) and for the laser anneal (AMAT Vantage Astra DSA diode bar system[5], lambda = 808 nm) to assess the viability of such a laser PEB based process flow at more relevant feature sizes.

For that purpose, we characterized the lithographic performance of our champion EUVL material on a standard organic underlayer using both KrF and EUVL exposures. We compared the standard hot plate PEB to a laser PEB and will describe the impact of laser power and dwell time. We will also report the impact which material selection has on the laser anneal PEB results.

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8325-57, Poster Session

Effective resist profile control for 20nm node and beyond

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As the critical pitch and critical dimension (CD) continue to shrink, the optical intensity and contour between different patterns become more complicated. For the 20-nm logic node and beyond, it is difficult to improve the resist resolution and maintain the same resist sidewall profiles for different patterns. For example, when a high-resolution resist is developed to meet hole pattern requirement, the trench pattern would easily suffered T-top induced scum. Improving resist resolution and profile simultaneously is urgent for low k1 manufacturing.

In this paper, we will introduce new techniques to overcome the trade-off between resist resolution and profiles. New floatable PAG, floatable additives, and new monomer groups for profile modification will be discussed in this paper. Based on X-SEM results, the original T-top profile could be improved without resolution loss with this new technology. With the help of floatable PAG, the trench scum can be improved from 73% to 0%. Moreover, optimizing the polymer with more hydrophilic monomer can also improve the scum from 73% to 7%.

8325-58, Poster Session

Defining and measuring development rates for a stochastic resist

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Photoresist development rates are commonly measured to characterize photoresist dissolution behavior. Such data are frequently used by simulators to create development models. An important though frequently unstated assumption of this use is the equivalence of microscopic and macroscopic development rates. Microscopic development rate is the development rate at a point in the resist and is the rate used by simulators. Macroscopic development rate is the mean rate at which a large open area develops down and is the quantity

measured when development rates are measured. In the absence of stochastic effects that result in surface roughness, these two rates are identical.

In the real, stochastic case, the mean propagation rate of a large open area is a strong function of the stochastic uncertainty of the development rate. The ratio of the macroscopic to microscopic development rates can easily be 2 - 5 or greater when developing near the knee of the development curve for a high-contrast resist for typical parameters. This paper will explore this ratio of macroscopic to microscopic development rates through the use of stochastic development simulations. Varying both development rate parameters and the underlying stochastic noise in resist inhibitor concentration, a simple semi-empirical model relating macroscopic to microscopic development rates will be developed. The consequences of these effects on resist simulation will also be explored.

8325-59, Poster Session

Diffusion of acid from resist to Si-hardmask layer

M. Shirai, H. Takeda, H. Okamura, Osaka Prefecture Univ. (Japan); H. Wakayama, M. Nakajima, Nissan Chemical Industries, Ltd. (Japan)

In the chemically amplified (CA) resist process, photo-chemically generated acid can diffuse in the resist matrix, inducing the de-blocking reactions. The concentration of acid in resist matrix should be constant during the post-exposure-bake treatment. In the practical resist processes, bottom anti-reflective coating (BARC) is essentially important to provide reflectivity control for resist patterning. In some cases, however, the photochemically generated acid in resist layer can diffuse into BARC layer, which causes the footing for resist patterns. In the previous work, we have reported the diffusion characteristics of acid from resist layer to organic BARC layer. In this work, we have studied the diffusion of acid from CA resist layer to Si-hardmask (Si-HM) layer. The Si-HM is essential for the multi-layer patterning process. The acid concentration in the resist layer was estimated based on the de-blocking reaction kinetics for the CA resist using rapid scan FT-IR spectroscopy. It was found that the acid in resist layer diffused into the Si-HM layer. Diffusion efficiency of the acid was dependent on the crosslinking density of the Si-HM and the chemical structure of the resist.

8325-60, Poster Session

LER reduction by photoresist formulation optimization for 193nm immersion lithography

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Line edge roughness (LER) is always one of the critical performance indexes for low k1 ArF immersion Lithography. Various factors, such as structures, anti-reflective coating (ARC), photoresist, baking condition, illumination condition and track process, are impacting for LWR performance during Lithography process. However, structures and ARCs are strongly related to integrated and Etch processes, and the illumination condition including mask bias is decided by simulation software and the track condition is fixed at initial process setup step. Therefore, photoresist evaluation with baking condition optimization is a typical way to improve LER performance.

The photoresist formulation contains photosensitive polymers, photoacid generators (PAGs), quenchers, additives, and solvents. Based on photoresist's point of view, the first two are main factors of LER performance control. In this paper, we will do several design of experiments (DOEs) by polymers, PAGs, and baking conditions, and then find out the optimization formulation by DOEs analysis software. The target is to achieve LER under 3nm.

8325-61, Poster Session

Observation of swelling behavior of ArF resist during development by the QCM method

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This equipment incorporates a high-precision developing solution temperature controller and features a high-precision air conditioning function for the measurement chamber. We also measured swelling behavior during development using a TBAH developer solution, which features larger molecules than TMAH, comparing these results with those obtained with TMAH. The results of this measurement indicate that the extent of resist swelling during development is less with TBAH developer solution than with TMAH developer solution. This result is consistent with results of a study by Itani et al. using high-speed AFM, suggesting the suitability of the measurement equipment used in our experiments.

8325-62, Poster Session

Study of the lithography characteristics of novolak resist at different PAC concentrations

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We previously examined the effects on lithography characteristics of differing molecular weight distributions in novolak resists. In a more recent study, we measured the development characteristics of five types of novolak resists with varying photoactive compound (PAC) concentrations. This report presents measurement results, as well as results of comparisons of patterns and process margins, obtained using the PROLITH lithography simulator. We also used the PROLITH to investigate the effects of PAC concentrations on the swing ratio. This is also discussed.

8325-64, Poster Session

Synthesis and properties of novel triphenylsulfonium salt bound polymer resists for electron-beam lithography

H. Lee, K. Sohn, O. Kwon, H. N. Kang, M. Kim, Hanyang Univ. (Korea, Republic of)

A novel acrylic monomer, triphenylsulfonium salt methyl methacrylate (TPSMA) was synthesized by reacting diphenyl sulfoxide and benzyl methacrylate dissolved in methlene chloride with trifluoromethanesulfonic anhydride. Homo-, co- and terpolymers of TPSMA with methyl methacrylate (MMA) and glycidylethacrylate (GMA) at different composition were prepared by free radical solution polymerization. The triphenylsulfonium salt-bound polymer, such as poly(TPSMA), poly(MMA-co-TPSMA) and poly(GMA-co-MMA-co-TPSMA) were synthesized in various ratio contents of in the polymer. For comparing the blending system with the photoacid bound polymer system, both TPSMA and triphenylsulfoium triflate are prepared with poly(GMA-co-MMA) each separately. The TPSMA bound polymers render the high thermal stability, high resolution, and high sensitivity depending on the content of TPSMA in the polymer main framework. These polymers were applied to electron beam lithography in order to demonstrate the effects of triphenylsulfonium salt bound resists. In bounding system, pinhole phenomenon was deleted after soft baking on surface and the low triphenylsulfonium salt loaded resist showed high efficiency in patterning, and the line edge roughness (LER) is quite improved. The effect of the TPSMA contents of resist has been analyzed with resists in sub-100 nm thickness. The obtained minimum widths were about 20 nm, and TPSMA blending and bounding systems related to triphenylsulfonium salt concentration indicated that the photoacid generator bound resist is

more superior to blending resist due to controllability of TPSMA bounding content for the acid diffusion. The triphenylsulfonium salt bound polymer resists might trap the secondary electrons so that the LER is improved and the high resolution can be achieved.

Triphenylsulfonium salt bound resists including GMA and MMA were well qualified and successfully applied to the fabrication of crosslinked negative-tone patterns. The resolution of the TPSMA-polymer resist reached sub-30 nm hp with 75 nm thickness and the resolution could reach down to sub-20 nm hp. A contrast curve showed that the sensitivities of triphenylsulfonium salt bound resists were about 100 C/cm2.

8325-65, Poster Session

Synthesis and photopolymerization kinetics of a novel oxime ester sulfonic acid photoacidgenerator

Y. Zou, Beijing Normal Univ. (China)

Ultraviolet spectrum experiment shows that (5-Hydroxyimino-5H-thiophen-2-ylidene) -phenyl-acetonitrile has the larger absorption peak near 405nm.In order to develop the efficient Photoacidgenerator (PAG) for 405nm violet laser imaging system, Taking the basis of the chemical structure of (5-Hydroxyimino-5H-thiophen-2-ylidene)-phenyl-acetonitrile,we synthesized a novel sulfonic oxime ester photoacidgenerator named (5-P-toluenesulfonyloxyimino-5H-thiophen-2-ylidene)-phenyl-acetonitrile (TTPA) .It is synthesized from 2-Nitrothiophen ,Phenylqcetonitrile and P-toluenesulfonyl chloride .TTPA was characterized by FTIR,1HNMR and UV absorption spectra.Real time infrared spectroscopy(RT IR) was used to investigate the effect of different monomer system and different concentrations of PAG on the polymerization kinetics .The results showed that with the increase of TTPA concentration with limits ,the rate of polymerization(Rp) and final double bond conversion increased and the induction period shortened.

8325-66, Poster Session

New two-stage photo-aromatization type photo-base generators for pitch-division photolithography

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We previously reported a new resist that enables doubling the resolution of current exposure tools without any additional processing steps by a technique termed pitch division. The only modification required to achieve pitch division is a reformulation of the resist. The modified resist produces solubility responses at twice the frequency of the aerial image, thereby doubling the resolution. Pitch division is achieved by incorporating both a photo-acid generator (PAG) and a photo-base generator (PBG) in the resist formulation. Pitch division was successfully demonstrated to provide a k1 well below 0.25. While this process works remarkably well, the line edge roughness (LER) of the images is unacceptable. Computational studies predict that the roughness is due, in part to poor chemical contrast in the resist. So, the image quality should be improved by increasing the slope of the net acid production as a function of exposure response. One method to achieve a sharper slope is to use a Two-Stage PBG, which gives a delayed onset of base production. We have designed and synthesized several types of two-stage PBGs. In this paper we describe a design based on photo-aromatization. This class of Two-Stage PBGs incorporates an aliphatic ring that undergoes a Norrish type II reaction upon exposure to a first photon, to yield an aromatic ring. The aromatic product is an active PBG that generates base by reaction with a second photon. We will describe

the design, synthesis and characterization of photo-aromatization type Two-Stage PBGs for use in pitch division photolithography.

8325-67, Poster Session

Synthesis of stable acid amplifiers that produce strong, highly fluorinated polymer-bound acids

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One challenge facing the developers of EUV resists is the need to simultaneously improve resolution, line-edge roughness (LER), and sensitivity. However, these characteristics are inversely related, a relationship commonly referred to as the RLS trade-off.[1] EUV resists are composed primarily of organic polymers and photoacid generators (PAGs). During exposure to extreme ultraviolet (EUV, 13.5 nm) light, the PAGs produce strong, fluorinated acids. Acid amplifiers are compounds that detect an acid signal (from PAG) and produce additional acid. This can be helpful in a photoresist by creating more acid in the exposed region which could give a better overall contrast.

As resolution has been pushed down to the 22 nm h/p node, acid diffusion has become increasingly more important. Since the PEB is a thermal process, acid from the exposed region can diffuse into the unexposed region, degrading resolution significantly. One method to reduce the acid diffusion length, yet still maintain acid catalysis during PEB is to bind the acid to the polymer (Polymer Bound PAG).

We have developed a series of novel Polymer-Bound Acid Amplifiers. These are compounds that have the ability to increase acid yield in the exposed region, with minimal acid diffusion into the unexposed region. In Figures 1 and 2 we show the imaging results of a polymer bound AA along with a comparable blended AA and a resist without AA. The blend shows the best improvement in sensitivity with a significant decrease in exposure latitude (EL). We think this is largely due to acid diffusion from the acid amplifier. The polymer bound AA still shows significant sensitivity improvement, but actually shows a gain in EL.

Although it shows a gain in EL, the polymer bound AA along with the AA blend shows relatively poor imaging. This poor imaging may be due to the weak acidity of the acid generated (pKa ~ 1) compared to the strong fluorinated acid amplifiers typically used in PAGs (pKa ~ -10). In order to improve imaging, we have developed a series of fluorinated polymer bound AAs. We have developed a new series of Polymer-Bound acid amplifiers that combine three important properties:

Low Diffusion. We have developed acid amplifiers that generate acid-bound sulfonic acids.

Strong Acid Catalysts. The acids must be very strong so that they can efficiently catalyze the deprotection of polymers.

Stability. The acid amplifiers must be thermally stable in the absence of acid and stable under polymerization conditions. This is difficult since AAs that generate strong acids are typically less stable.

We have designed and synthesized a series of new polymer-bound AAs that produce very strong acids. We will explicitly describe the structures and preparations of these new compounds in our poster and manuscript.

8325-68, Poster Session

Ionic carbamate photoacid/photobase generators for the advancement of dual-tone photolithography

G. L. Hallett-Tapley, T. E. Wee, J. C. Scaiano, Univ. of Ottawa (Canada); J. Eldo, E. A. Jackson, SAFC Hitech (United States)

Current work in lithographic patterning has been carried out using 193

nm excitation sources, limiting the pitch division to approximately $\lambda/2$ and the advancement of Moore's law. Recently, double patterning has emerged as a potential extension of 193 nm techniques due to potential to pattern two lines in one exposure. In this contribution, the double patterning features of single component carbamate photoacid/photobase generators (PAG/PBG; Figure 1) were examined. At lower exposure doses, sulfonic acid is generated, while at higher doses, a photochemical rearrangement is initiated to activate the PBG component. Noteably, the presence of the sulfonic acid and the newly formed amines photobases in the same molecule results in a proton transfer causing deactivation of the photoacid precursor. Optimally, at intermediate doses, photoacid and photobase components could exist concurrently resulting in negative and positive imaging and the desired dual tone lithographic features. The carbamate systems of interest, 4NSS and 4NSI, have shown clear dual tone features, with the former being the more efficient of the two. The energy required to initiate dual tone behavior can be tailored through co-added amine quenchers and carbamate concentration. Using ellipsometry, the energy required for the resists to have the first sign of photoacid generation (film dissolution), E0, and at the energy required for photobase activation (En) were determined, as this value dictates the ability to achieve desired pitch division.

Finally, laser flash photolysis (LFP) was implemented to give some insight into the mechanism by which the proposed rearrangement reaction occurs.

8325-69, Poster Session

Positive-tone chemically amplified Fullerene resist

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With continuing efforts to achieve higher lithographic resolution there has been on-going interest in the development of low molecular weight resists, such as molecular glasses. We have previously presented results of a fullerene derivative based three component negative tone chemically amplified resist capable of 12 nm isolated patterning, 20 nm halfpitch and with a sensitivity of less than 10 microC/cm2 at 30 keV.

Here we present the initial results of a study into the development of a positive tone two component chemically amplified resist based on a similar methanofullerene derivative. Figure 1 shows the fullerene derivative MF- tBAC, which has been used with the photoacid generators triarylsulfonium hexafluoroantimonate (PAG1), triphenylsulfonium triflate (PAG2), diphenyliodonium triflate (PAG3) and tris(4-tert-butylphenyl) sulfonium perfluoro-1-butanesulfonate (PAG4). Mono, di, tris and hexa adducts of the MF- tBAC, (MF- tBAC(1), MF- tBAC(2), MF- tBAC(3) MF- tBAC(6) respectively) were synthesized and evaluated. Additionally mono and di adducts of the closely related derivative MF-tBOC were also evaluated.

Fullerene resist films were prepared by spin coating on freshly cleaned hydrogen terminated silicon substrates. Films have been spun from propylene glycol monomethyl ether acetate (PGMEA), ethyl lactate, chloroform, anisole and other organic solvents. Films were irradiated using a Philips XL30SFEG scanning electron microscope equipped with a Raith lithography system. Development was in either deionised water (DI), 0.26N or 0.026N TMAH. Figure 2 shows the sensitivity of the MF-tBAC(2) with three different PAGs and various PAG loadings. Development was in 0.26N TMAH for figure 2(a), and 0.026N TMAH in the other cases, followed by a DI rinse. No bake was applied after exposure. The MF-tBAC derivative does not show a positive tone response in its pure film. Adding PAG1 gave a range of doses from 114 to 136 microC/cm2 dependant on the loading. PAGs 2 and 3 gave significantly more sensitive resists with PAG2 showing a sensitivity of up to 11 microC/cm2 and PAG3 giving 20 microC/cm2. The EUV sensitivity of MF-tBAC:PAG1 has also been evaluated at the PSI tool and found to be 11 mJ/cm2. Figure 3 shows initial results of high resolution patterning in MF-tBAC(6):PAG1. 20 nm isolated lines and 60 nm halfpitch dense lines have been achieved.

8325-70, Poster Session

Synthesize and polymerization of novel photocurable vinyl ether monomers containing perfluorinated aromatic units

W. Li, Y. Zou, Beijing Normal Univ. (China)

UV curing technology has been widely applied in the fields of UV curable coatings, adhesives and printing inks. Fluoropolymers have the merits of low surface energy, water proof, oil resistance, excellent weatherability, chemical resistance and anti-pollution. These excellent performances which other polymers are difficult to match will promote the further application of UV curing technology. In this paper, we designed and synthesized a series of novel UV-curable vinyl ether monomers with perfluorinated aromatic units for photoresist. Perfluorinated aromatic vinyl ether derivatives were prepared through the reaction of 2-vinyloxy ethanol with hexafluorobenzene and decafluorobiphenyl in the presence of sodium hydride. It is an effective method to generate fluorine-containing aromatic vinyl ether monomers in high yields of greater than 85%. The novel photocrosslinked perfluorinated polymers obtained by PAG201 initiating. The photocuring kinetics and surface energy of these polymers were investigated by Real Time Infrared and Contact Angle Measurement. The photopolymerization kinetic results showed that an increase of the initiator content strongly accelerated the photopolymerization of the photocuring monomers and the maximum of the polymerization rate was achieved earlier. Contact angle results indicated that fluoro-polymers had lowest surface energe. And their physical and chemical properties satisfied the material requirements for photonic devices.

8325-95, Poster Session

Reduced Zeta potential for improved polyimide process perfomance and minimizing material consumption

L. D. Hodgson, MOXTEK, Inc. (United States); A. Thompson, DisChem, Inc. (United States)

This paper presents the results of a non-HMDS adhesion promoter that was used to reduce the zeta potential for coating very thin (proprietary) polymer on silicon. By reducing the zeta potential, as measured by the minimum sample required to fully coat a wafer, the amount of polymer required to coat silicon substrates was significantly reduced in the manufacture of X-ray windows used for high transmission of low-energy X-rays. Moreover, this approach used aqueous based adhesion promoter described as a cationic surface active agent that has been shown to improve adhesion of photoresists (positive, negative, epoxy [SU8], e-beam and dry film). As well as reducing the amount of resist required to coat substrates, this aqueous adhesion promoter it is non-toxic, non-hazardous and contains non-volatile solvents.

8325-46, Poster Session

Characteristics analysis of RELACS process from an OPC point of view

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There are strong demands for techniques which are able to extend application of ArF immersion lithography. Especially, the leading edge techniques are required to make very small hole patterns below 50nm. Several techniques such as double patterning technique, free-form illumination and resist shrinkage technology are considered as viable candidates. Most of all, NTD (Negative Tone Development) is being regarded as the most promising technology for the realization of small hole patterns

When NTD process is applied, hole patterns are defined by island

type features on the reticle and consequently its optical performance shows better result compared with PTD (Positive Tone Development) process. However it is still difficult to define extremely small hole patterns below 40nm, new combination process of NTD with RELACS is being introduced to overcome resolution limitation. NTD combined with RELACS, which is the most advanced lithography technology, definitely enable us to generate smaller size hole patterns on the wafer.

A chemical shrinkage technology, RELACS (Resolution Enhancement Lithography Assisted by Chemical Shrink), utilizes the cross linking reaction catalyzed by the acid component existing in a predefined resist pattern. In case of PTD combined with RELACS process, we already know that CD change after the shrinkage process is not influenced by duty ratio. So we could easily reflect the RELACS bias to meet the CD target during OPC (Optical Proximity Correction) procedure.

But NTD combined with RELACS process was not understood clearly, nor verified. It requires more investigation of physical behavior during combined process in order to define exact hole patterns. The newly introduced process might require additive OPC modeling procedure to satisfy target CD when NTD RELACS bias has different values according to pitch and shape.

8325-49, Poster Session

Inhomogeneous kinetics of solid state photochemical reactions of PAG or PBG and the molecular design for their high performance

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Quantum yield of photo-reactive materials are defined as the rate of the product formation over the sum of various deactivation process rates, which is usually regarded as identical to the molecule. The quantum yields of their photo-chemical reactions in solid state polymer are not only determined by the photo-physical, however, but also by the effect of free volume of polymer matrix. Therefore the quantum yields of photo-reactions of photo-reactive molecules in solid state polymer have inhomogeneous distribution.

We have determined the quantum yield distribution of various photo base generators (PBG) and photo acid generators (PAG) to find that they become much reactive in solid state polymer than in solution, where free volume in the polymer is rather "static" than "dynamic" characteristics. Increase in the size of substituent on PAGs also increases the size of free volume around them, to our surprise, to increse their photoreactivity.

Thus, free volume properties of the solid state reaction is affected by the size of substituent, lifetime of reactive intermediates. These understanding provies us with valuable strategy of designing more reactive PAG or PBGs.

8325-71, Poster Session

Universal templates for nanostructure arrays using silicon-containing block copolymers

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Fabrication of freestanding one-dimensional nanostructure arrays has attracted considerable attention because these structures can potentially be used for nano- and microscale devices. However, it is difficult to achieve uniform and highly dense freestanding 1D nanostrcutures over a large area using a relatively simple method. Here, we report a simple, rapid, and scalable method to fabricate a versatile nanoporous template, based on the combination of self-assembly of a silicon-containing block copolymer and a lithographic bilayer system. This approach used a top thin film of self-assembled asymmetric polystyrene-block-poly(4-(tert-butyldimethylsilyl)oxystyrene) (PS-b-PSSi) as a hard etch mask and an underlying thick film of a negative-tone photoresist (SU-8) for pattern transfer. Solvent annealing of PS-b-PSSi resulted in well-ordered cylindrical PS nanodomains, oriented perpendicular to the surface and

embedded in the PSSi matrix. A single etching step converted the PSSi matrix to a self-hard mask of silicon oxide and removed the PS cylinders and the underlying SU-8 completely. As a result, a template with high-aspect-ratio arrays of cylindrical nanopores was fabricated on a large area of the substrate with no complex steps. We demonstrated the applicability and versatility of the template by controlling the pore size and applying it to various functional substrates.

8325-72, Poster Session

Dual-responsive photoresists for sequential pattering by thermal imprint and photolithography

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Curing imprint lithography (UV or thermal) has emerged as a less expensive alternative to print nano-scale features. But typical imprint resists is difficult to degrade because of highly cross-linking. By designing a resist in which all of the cross-linkers are cleavable under mild acid conditions, we would require only a simple degradation step to remove the film after imprinting. In this study, methacylate monomers containing tertiary ester linkages and hydroxyl groups were copolymerized with diazoketo-functionalized monomers, and then polymers were coated on substrate with a photoacid generator. Polymers were patterned with thermal imprint lithography to create cross-linked films through hydroxyl-diazoketo linkages. Films could be sequentially patterned in a subsequent photolithography step by thermal and acid-catalyzed decomposition of tertiary ester linkages. We introduce the combination of thermal imprint and photolithography into a single system.

8325-73, Poster Session

Development of Si-HM for NTD process

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Negative Tone Development (NTD) process with ArF immersion has been developed for the next generation lithography technology because it shows good resolution performance and process window for C/H and trench patterning. Recently, the resist and the developer materials for NTD process have been investigated to improve the lithography performance.

Because of the etch requirement, tri-layer process {photo resist/ silicon contained hard mask (Si-HM) / spin on carbon hard mask (SOC)} has been used popularly below N45 device manufacturing already. However, most of the Si-HM materials are optimized for positive tone development process and most of them show poor lithography performance in NTD process - for example, the process window of pattern collapse is narrow.

To improve the lithography performance of NTD process, it is very important to match Si-HM and resist for the next generation. In this paper, we study the behaviors of Si-HM for NTD process, develop new concepts and optimize the formulation of Si-HM to match the resist for NTD process beyond N28 node device.

8325-74, Poster Session

Negative-tone development of photoresists in environmentally friendly silicone fluids

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The large amount of organic solvents and chemicals that are used in today's microelectronic fabrication process can lead to environmental, health and safety issues. This will be particularly true as interest grows in the negative tone developments of chemically amplified resists. It is therefore necessary to evaluate new materials and new processes to reduce the environmental impact of the lithographic process. In addition, as the feature sizes decrease, other characteristics such as pattern collapse, which is related to the undesirable high surface tension of the developers and rinse liquids, can occur and limit the resolution. In order to solve these issues, silicone fluids have been selected as alternative developing solvents in this study. Silicone fluids, also known as linear methyl siloxanes, are a class of mild, non-polar solvents that are non-toxic, not ozone-depleting, and contribute little to global warming. They are considered as promising developers because of their environmental-friendliness and their unique physical properties such as low viscosity and low surface tension. Recently, there have been emerging interests in negative-tone development (NTD) due to its better ability in printing contact holes and trenches. It is also found that the performance of negative-tone development is closely related to the developing solvents. Silicone fluids are thus promising developers for NTD because of their non-polar nature and high contrast negative-tone images are expected with chemical amplification photoresists due to the high chemical contrast of chemical amplification. We have previously shown some successful NTD with conventional photoresists such as ESCAP in silicone fluids. In order to achieve higher resolution patterning, development of molecular glass photoresists in silicone fluids was studied and due to the low surface tension of silicone fluids, we have been able achieve high aspect-ratio, high-resolution patterns without pattern collapse.

8325-76, Poster Session

High-etching selectivity of spin-on-carbon hard mask process for 22nm node and beyond

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As the design rule of semiconductor process shrinks, the resist film thickness is getting thinner and the etching process using resist mask is becoming more difficult. In recent years, the film structure used in the resist process has been changing from the single-layer process (BARC and resist stacked film) to the multi-layer process (Carbon hard-mask, middle layer and resist stacked film) in order to solve this problem. There are two types of carbon hard-mask of multi-layer process: CVD-carbon (CVD-C) that uses chemical vapor deposition method and Spin-on-carbon (SOC) that uses spin-coating method. CVD-C is very attractive because of its high etching selectivity but still has big challenges such as particle generation, lower flatness and high process cost. On the other hand, SOC has the benefit of low cost, higher flatness and no generation of particle.

Based on this background, we considered the development of SOC with high etch selectivity using our original bake method and improving material. We successfully fabricated the 22nm pattern on SiO2 and also suggested the possibility of its application to extreme ultraviolet lithography (EUVL).

This paper reports on the results of a comprehensive process evaluation of the multi-layer technology of SOC using lithography clusters and etching tools.

8325-77, Poster Session

Applicability of double-patterning process for fine hole pattern

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Self-aligned spacer Double Patterning (SADP) has been adopted in HVM of NAND FLASH memory device, because SADP can fabricate fine periodical line pattern more easily than pitch-split type DP. Furthermore, SADP can mitigate overlay accuracy such like pith-split type DP needed. The remarkable feature of SADP process is the adoption of a SiO2 film that can be deposited at extremely low temperatures for spacer formation. SADP and this deposition process also produce wide applicability to density multiplication on hole pattern.

In our previous study, hole pattern fabrication below 40nmhp was examined. 30nm hp hole pattern was viable with single 193-immersion exposure successfully with our newly developed process scheme named EKB, and ultimate down-scaling on hole pattern, achieved to 20nm hp, was introduced utilizing cross-SADP[1][2].

In logic device manufacturing, pattern layout is getting to single directional, tabbed Gridded design rule (GDR) for the mitigation of various lithographic issues. Although Self-aligned type DP for hole pattern can describe periodical layout, it is really enabled for future simplified pattern layout.

In this paper, successful demonstration results would be introduced in process simplification, process extendibility, CD controllability and further downward scaling.

8325-78, Poster Session

Plasmon mediated polymerization on the surface of silver nanoparticles for advancements in photolithographic patterning

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Metal nanoparticles and plasmon excitation have been used to enhance spectroscopic transitions and chemistry on metal nanoparticle surfaces.(1, 2) The size and shape of the enhancement area around the nanoparticles is dependent on the size, shape, and dielectric constant of the matrix and metal. We have recently reported on the use of plasmon excitation to induce acrylic polymerization on the surface of silver nanoparticles and have made ~10 nm polymer features far below the diffraction limit using visible LED irradiation.(2) The acrylic polymerization takes advantage of increased excitation of azo photoinitiators in the vicinity of nanoparticles, causing cross-linking only in the enhancement region. The formation of a cross-linked polymer on the surface of the particles causes a solubility switch, where the regions unaffected by irradiation remain soluble and can be selectively washed away leaving behind the AgNP with a polymer coating.

Plasmon excitation also generates a significant amount of heat. Caprolactam polymerization to nylon can be initiated simply with heat (and atmospheric moisture) allowing for the reaction to take place on the surface of metal nanoparticles, essentially mapping the heat dissipation in the vicinity of the particles. It is expected that nylon formation on the surface of metal nanoparticles causes a solubility switch leaving behind irradiated features after washing, as with negative photoresists. The formation of nylon polymers on the surface of particles can be combined with a conventional lithographic mask and particle formation steps to give a hierarchy of imaging with combined larger and smaller features.

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8325-79, Poster Session

Advanced multipatterning using resist core spacer process for 22nm node and beyond

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As the design rule of semiconductor process gets finer, extreme ultraviolet lithography (EUVL) technology is aggressively studied as a lithography technology for 22nm-node and beyond. At present, however, many technical issues are still being reported and it has not yet been adopted as mass production technology. In the face of these technical issues, the development of multi-patterning technology using 193nm immersion lithography: Self-aligned double patterning (SADP), Self-aligned triple patterning (SATP), Self-aligned quadruple patterning (SAQP) is getting much attention for 22nm-node and beyond. However, process cost and CD controllability are major challenges since multi-patterning technology that utilizes spacer process requires larger number of etching and deposition process steps.

Based on the above background, we began to study the simplified spacer process using resist core in order to decrease process cost and improve CD controllability and we verified its process performance (Process window, LWR, LER, CDU, Defectivity) and also succeeded in improving CD controllability by adjusting the shape of the resist core material.

This paper reports on the results of a comprehensive process evaluation of multi-patterning technology using lithography clusters, etching and deposition tools.

8325-80, Poster Session

Enhanced self-aligned multiple patterning for 1xnm half pitch

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Self aligned double patterning (SADP) has been extended to sub 20nm hp HVM because the development period of EUV lithography has been postponed. Therefore we have investigated ArF immersion based SADP as fine patterning option for 20nm/10nm hp devices.

In general self aligned multi patterning consist of SADP, SATP(triple patterning), SAQP(quadrupling pattenring). We have already introduced innovative resist core based SADP/SAQP demonstrated results in past SPIE.[1][2] Our proposed SiO2 spacer is directly deposited on resist core via a low-temperature deposition process.

SATP and SAQP enable making further down scaling to 10nm-15nm hp from SADP, however CD controllability of SATP/SAQP become more sensitive.

In this paper we would discuss about CD error budget analysis for self aligned multi patterning including a newly developed SATP scheme.

8325-81, Poster Session

Combinatorial process optimization for negative photo-imageable spin-on dielectrics and investigation of post-apply bake and post-exposure bake interactions

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Patternable dielectric materials were developed and introduced to reduce the semiconductor manufacturing complexity and cost of ownership (CoO). However, the bestowed dual functionalities on photo-imageable spin-on dielectrics (PSOD) put great challenges on the material design and development. In this work, we investigated the combinatorial process optimization for the negative-tone PSOD lithography by employing the Temperature Gradient Plate (TGP) technique which significantly reduced the numbers of wafers processed and minimized the developmental time. We demonstrated that this TGH combinatorial is very efficient at evaluating the effects and interactions of several independent variables such as post-apply bake (PAB) and post-exposure bake (PEB). Unlike most of the conventional photoresists, PAB turned out to have a great effect on the PSOD contrast and pattern profiles. Based on our extensive investigation, we observed great correlation between PAB and PEB processes. In this paper, we will discuss the variation of the contrast curves and pattern profiles as a matrix of PAB and PEB and propose two possible cross-linking mechanisms for the PSOD materials to explain the unusual experimental results.

8325-82, Poster Session

Tunable resin reactivity of spin-on dielectric by controlling synthesis process

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On the course of R&D on SOD material, we discovered that SOD resin reactivity have meaningful correlation with the degree of planarization. In this paper, two experiments have been illustrated to prove this correlation, step coverage test and humid air bubble test. In step coverage test, the lower the resin reactivity is, the larger the circle from the coating of SOD on the specific size of silica-bead. It is hypothesized that the low reactivity of resin causes more fluidic nature of the SOD and thus size of circle formed around the silica-bead becomes larger. In the humid air bubble test, the lower the resin reactivity is, the slower the rate of molecular weight growth when humid air bubbles travel through the SOD solution because high resin reactivity results faster crosslinking between SOD polymer chains. Not surprisingly, the results of the above two tests are correlated to each other. Lower reactivity SOD resin has larger size of circle around silica-beads and also slower molecular weight growth under the same humid bubble condition. Considering the manufacturing process of devices, tunable resin reactivity is anticipated to be a powerful toolbox to approach problems such as minimizing various types of defect or adjusting the degree of global planarization.

8325-83, Poster Session

Developable BARC for special applications

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Developable Bottom Anti-Reflective Coating (DBARC) technology becomes more and more attractive for lithographical processes and has proven over the last two years the high volume manufacturing capability. As main application of DBARC the implant lithography has long been considered as the ideal insertion point for DBARC technology. Taking the advantage of eliminating the cost intensive BARC open etch step and an improved reflectivity control compared to conventional top anti-reflective materials (TARCs). But also non-implant levels can benefit by exchanging conventional BARC technology to a DBARC system with the ability to simplify lithographic and integration process efforts.

We will describe our work and the results of introducing the DBARC material compared to our standard processes. Besides the usage for implant applications, we especially focused on the influence of DBARC material on topography issues, e.g. topography due to STI leveling, which generates a lot of problems with respect to CD uniformity and profile integrity. Therefore the BARC material was not only used for standard 248nm or 193nm processes, but was also implemented in our i-line process. Besides the decoupling from highly reflective, rough substrates, DBARC is expected to provide significant resist budget for critical etch processes compared to standard BARC approaches. This was also investigated on an i-line metal layer and on DUV metal/nitride stack. The benefit of DBARC materials for reflectivity control can be enlarged by improving the resist adhesion on challenging underlaying subtrates and by suspending the negative influences of topography issues for integration schemes which do not allow the usage of standard BARC or TARC processes.

8325-84, Poster Session

KrF resists for implant layers patterning extreme-high-aspect-ratio structures with a double focal plane exposure technique

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In the Image Sensor development path design rules shrinkage has become one of major challenge also for KrF technology. In particular, for the implant Photo layer the need for blocking high energy boron-implant (well above 2 MeV) with extremely localized implant profiles requires aspect ratio of deep well structures greater than 10:1. Other desirable attributes of a good photoresist for such demanding application are high transparency, good wall profile through entire thickness, good adhesion with no structure-collapse and wide process window.

In this paper, we will discuss the role of a chemically amplified, ESCAP-type of resist in meeting above described design criteria with a double focal plane exposure technique. The Track Equipment challenges for high resist thickness photoresist will be illustrated as well.

8325-85, Poster Session

Gray-level 3D resist process and its application

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Gray level 3D resist process were developed by using negative e-beam resist and multiple coating multiple electron beam wafer direct write alignment, and are now going into be used to create complex 3D structures in thick resist. Gray level resist process to create 3D structure in thick resist can be used as mold or photomask to be used for manufacturing Fly's-eye lens array, Fresnel lens, Prism, Flat prism, Light guiding plate, Lenticular lens and Linear Fresnel lens. Such optical devices can be used for TFT LCD display, Fresnel lens for solar concentrator and LED. Fig.1 and Fig. 2 Show the SEM picture of negative type e-beam resist NEB22 with multi coating and multiple electron beam wafer direct write alignment, the thickness of this 3D gray level resist structure is 0.8um. Fig. 1 is top view and Fig. 2 is resist profile. The single coating thickness of NEB22 with spin speed 4000 rpm is about 200nm. The multiple level electron beam wafer direct write used in this work is Vistec WePrint 2000, the exposure dosage is about 8 µC/cm2 with 40 kV and the data base is from 0.8 µm to 0.2µm with 0.2µm steps. Detail gray level 3D resist process and its application will be presented in the conference.

8325-96, Poster Session

Measurement and reduction of micro-bubble formation in high-viscosity fluids

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Gases at high drive pressure can initially dissolve into the fluids used in lithography and other critical processes during the fabrication of integrated circuits. In the low pressure portion of the dispense train, the dissolved gases can revert to bubbles. These bubbles can:

1. Affect the compressibility of the working fluid and change the flow characteristics of the dispense heads which require frequent re-tuning of the coating tools.

2. Contribute to defect formation on the surface of the wafer if the bubbles are trapped on the surface of the wafer.

Photosensitive Polyimides (PI) have high viscosities (1000 to 20,000 cP). Because of the high viscosity, high-powered, expensive pumps are needed to effectively remove the fluid from its container. Suction from the pump filling cycle easily causes cavitation, which can create flow rate variability, and microbubble formation. It is a common practice to apply pressure to the PI resists to minimize cavitation in the pump. The trade-off to this practice is the entrainment (dissolution) of the drive gas into the resist and the risk of micro-bubbles forming later in the dispense train.

In the current study, ATMI measured the effects of two methods of pressure dispense from the container on the amount of gas entrained in a viscous fluid: (1) indirect pressure dispense and (2) direct pressure dispense. The main analytical method employed to measure the amount of dissolved gases is a gas chromatograph (GC), which can measure the concentration of gases dissolved in a volatile fluid. It is not suitable to measure gases in low volatility fluids. ATMI has also developed indirect pressurization containment systems to minimize the entrainment of gases into fluids used in critical processes during the fabrication of integrated circuits.

In this paper we will report on a new developed analytical method which can directly measure the presence of small bubbles (i.e. about 0.1 µL and larger bubbles) that may form in high viscosity fluids.

The formation of bubbles is dependent on the method of operation and we will present data on this aspect as well. Further, data comparing the effects of indirect and direct pressurization on bubble formation in the fluid will be presented.

8325-86, Poster Session

Blob defect prevention in 193nm topcoat-free immersion lithography

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In this paper, we discussed the relationship between blob defect counts and resist surface hydrophobicity, and illustrated the increased trend of blob defect count with the decrease in receding contact angle until the receding angle reach a breaking point below which the resist surface exhibits good dynamical wetting under a given dynamic condition.

In this paper, novel EBL material design is also discussed. These novel EBL materials perform a change from hydrophobic to hydrophilic upon contacting with the alkaline developer solution, and hence are able to ensure good dynamic wetting of a resist surface to the rinsing DI water, and thus are able reduce the blob defect count to the levels comparable to or lower than that of an immersion topcoat process.

8325-87, Poster Session

Solvent pre-wetting as an effective start-up method for point-of-use filter

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An effective filter start-up method has been required by device manufacturers, mainly in order to reduce waste volume of lithography process chemicals, which become more expensive as lithography technology advances. Pall Corporation has quantitatively demonstrated the effectiveness of filter start-up methods, such as static-pressure-driven method, application of back pressure, and deaeration of the fluid, using a proprietary developed method for dynamically measuring the remaining air within a filter.[1,2] In this paper, the effectiveness of pre-wetting a Pall PhotokleenTM EZD-2 point-of-use (POU) filter with asymmetric nylon 6,6 membrane rated at 20 nm (PHD11ANMEH11) with solvent, prior to the introduction of Fujifilm topcoat-less resist (FAiRS-PA01), and a study of solvent optimization for pre-wetting are reported.

Remaining air was monitored during static-pressure-driven filter start up (Figure 1). As a result, 4 quarts of the resist was needed to eliminate remaining air (Figure 2). For improvement, solvent pre-wetting was applied prior to the resist introduction. An organic solvent was introduced to the filter capsule and subsequently resist was introduced. In this case, the total resist consumption was equal to an amount needed to sufficiently displace the pre-wetting solvent from the filter capsule volume, as evaluated via spin thickness recovery. Cyclohexanone, which was confirmed not to affect the solubility of the resist polymer, was used for initial testing. As a result, the resist volume needed for the solvent displacement was 2 quarts, approximately half the volume required for static-pressure-driven start-up.

Other solvents were evaluated for the pre-wetting start-up method. A pre-wetting solvent that can easily displace air within the filter capsule is preferable. Performances of cyclohexanone, PGMEA, PGME, and isopropanol (IPA), were compared for another test filter (PHD11ANMEH11). Results, in descending order of performance (remaining air after 700 mL throughput) were PGME (best) < PGMEA = IPA < cyclohexanone (worst). Moreover, air displacement performance strongly correlated with Hansen solubility parameter (HSP) distance between each solvent and nylon 6,6 material (Figure 3). HSPs quantitatively describe the affinity for non-bonding interatomic and intermolecular interactions between two materials.[3]

Additionally, the effect of solvent deaeration was evaluated by means of the remaining air measurement, and the effect of solvent-prewetting on after-development inspection (ADI) result of bridge defects on a 45 nm L/S pattern was evaluated.

8325-88, Poster Session

Study of filter adsorption mechanism in photoresist materials

T. Kohyama, Nihon Entegris K.K (Japan)

Recently nylon filters have been widely implemented in photolithography processes to improve the yields because many IC and photoresist manufacturers have empirical evidence indicating that the nylon membrane can adsorb impurities. However, the mechanism by which the nylon membrane reduces defects is unclear and it is unknown how the removed components would ultimately affect yield. Therefore, basic study on the removal mechanism of defect-causing species must be undertaken. In particular, it is useful to study different defect-causing mechanisms by focusing on the particular components of photoresists.

In this paper various adsorption tests were performed utilizing surface modification and different photoresist components to measure the effect of nylon membranes on resist properties, including surface tension, PAG (photoacid generator) concentration, and quencher concentration. Ultimately, the study hopes to determine the most effective way to increase yields by focusing on how to best implement a nylon filtration strategy.

8325-89, Poster Session

Post-developed defect in word-line SADP process

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SADP (Self-Aligned Double Patterning) technology has been widely adopted in flash memory device manufacturing. To delineate the word-line layer of our product by the SADP technology, three mask layers including core layer, trim layer and periphery layer, were adopted. The process flow starts with the 1st exposure of core layer then spacer formation, followed by the 2nd exposure of trim layer to cut away the closed line end formed by spacer. Before the final etch for word lines, the 3rd exposure was conducted for defining the peripheral patterns as well as the word line pads. Among the above three mask layers, the periphery layer is with the extremely low pattern density of ~10%, and a

post-developed defect unlike the traditional satellite defect was observed on it. The defect tended to happen around boundary of with and without patterns and finally yielded pad distortion or bridging (called "distortion" hereafter), as shown in Figure 1. This defect has been characterized as yield killer since it caused word line bridging after etching.

To eliminate the distortion defect, resist type, TARC(Top Anti-Reflective Coating), various development puddle/rinse schemes, HB(Hard Bake) splits and ADR (Advanced Defect Reduction) function of track were evaluated. The change on photo-resist thickness and type has minor effect on the defect count. TARC has been indentified as an effective solution to reduce the conventional satellite defect but the experimental result on eliminating the distortion defect is also not obvious. In resist processing, HB showed strong correlation to the distortion defect count. The defect count of distortion reduced as lowering the HB temperature and the defect was not observed by experimentally skipping the HB step. The evidences orientated the defect source toward voluminous development by-products resulted from extremely low pattern density of process layer. The mass flow of by-products was expected to be interfered around boundary of with and without patterns during the development/rinse steps, hence the re-deposition of by-products around the pattern boundary could be possible. Multiple cycles of development puddle and longer rinse were hence employed to more uniformly disperse the by-products and significant defect reduction was achieved. The double development puddle was adopted to further reduce the concentration of development by-products in advance of the rinse step, together with long dynamic rinse, the distortion defect was dramatically reduced. To tackle with the long development time induced throughput loss, ADR is another solution to eliminate the distortion defect via N2 blow in advance of spin dry step.

8325-91, Poster Session

Pattern dependent satellite defects in via lithography

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In patterning the via-hole process, uneven hole-size and missing-hole defects were identified through AEI (After-Etch Inspection) and were attributed to the post-developed satellite defect finally. These defects have been characterized as yield killer since it caused electrical open and were targeted for immediate improvement. The distribution of satellite defect always shows a strong photo field dependence that was discovered to correlate with the scribe lane pattern density. Apart from the modification on pattern density in the scribe lane of the photo mask, this paper describes the work done in reducing the satellite defect. Several development experiments including multiple cycles of dynamic puddle, multiple cycles of dynamic rinse, pre-wetting before development, spin speed of rinse, spin speed of drying and ADR (Advanced Defect Reduction) function of track were carried out. The multiple cycles of dynamic rinse coupling with the optimal spin speed of rinse effectively suppressed the size of satellite spots. Pre spin dry in advance of the DI water rinse are also effective to reduce the defect. Multiple cycles of development puddle and rinse have a synergy effect to lower defectivity up to complete suppression of satellite defect. To minimize the throughput loss induced by the long development time, ADR is another solution to eliminate the satellite defect via N2 blow during spin dry step.

8325-92, Poster Session

Resist process optimization for further defect reduction

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Defect reduction is one of the most important technical challenges in the recent device mass-production. Knowing the fact that resist caused

defect is strongly related to track process in many cases, we have been trying to improve the process to meet requirements as a track supplier. For example, residual type defect and pattern collapse are strongly related to process parameters in developer, and we have reported new develop and rinse methods in the previous papers. Also, we have reported the optimization method of filtration condition to reduce bridge type defect which is mainly caused by foreign substances such as gels in resist. Thus we have contributed resist caused defect reduction in the past studies, but the requirement of defect reduction is still high yet. In this paper, we will introduce further improved process in terms of resist defect reduction including the latest experimental data.

8325-93, Poster Session

Effects of nylon filter properties on contact-hole photoresist imaging performance and defectivity

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Previous studies of contact hole photoresist performance1 with various filter membranes showed that UPE membranes were effective in reducing defectivity with minimal changes in the resist's imaging properties. Nylon filters, known to have absorptive properties, altered the imaging of the photoresist and as a result produced higher overall defectivity.

This study will more closely examine the absorption effects of Nylon membrane on contact hole photoresist and attempt to quantify changes to the resist by measuring the change in lithographic performance and the effect on defectivity. Additionally, this study will recommend filtration parameters which will take advantage of the absorptive capability of the Nylon membrane, while minimizing the changes to the lithographic performance of the photoresist.

1 Braggin, J., et al, "Characterization of Filter Performance on Contact Hole Defectivity", SPIE vol. 7972, 79722Y, (2011).

8325-94, Poster Session

Consideration of equipment sequence in optimizing filter priming methods

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Reducing lithography application cost of ownership is an ever-present priority to the process engineer, regardless of technology node or the type of semiconductor device that is manufactured. Opportunities for cost reduction exist within the process of priming a new filter with process fluid, whether for defect excursion recovery or as a part of coater/developer (track) preventive maintenance. As the removal efficiencies of filter media have been enhanced, with state-of-the-art product ratings reaching well below 10 nm, the challenge of priming a new filter assembly for production use while minimizing both method duration and fluid consumption has become increasingly complicated. Moreover, the configurations and sequences of hardware elements that constitute process fluid flow paths vary between commercially available track systems. Specifically, the sequence in which a process fluid encounters the dispense system (pump) and the point-of-use filter assembly can significantly influence the order and optimization of steps within the filter priming procedure. The present work principally investigates the effects of pump-filter sequence on filter priming methodology. Overall quality of the filter priming procedure, as measured by on-wafer defects, fluid consumed, and procedure duration, is evaluated for a single-stage pump, which can be installed either between the fluid source and filter, or between the filter and point of dispense. Results for each permutation are compared while varying process fluid

type, filter media materials, and filter media symmetry. Defect adders for spin-on films are measured using a commercially available inspection tool. Based on results, generalized filter priming procedures are recommended for various equipment setups.

8325-29, Session 8

Investigation of pattern wiggling for spin-on organic hardmask materials

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Semiconductor manufacturing technology is currently undergoing a transformation from immersion photolithography to double patterning or EUV technology. The resultant resist pattern size and pattern height shrink require improved pattern transfer techniques and materials. Underlayer (UL) processes which include chemical vapor deposition (CVD) and spin-on underlayers play a very important role in various chip manufacturing integration schemes. A pattern wiggling problem during substrate etch has arisen as a critical issue when pattern dimsensions shrink. CVD processes have shown better pattern transfer performance than spin-on processes but at higher cost and process complexity along with difficulty in obtaining planarization and good gap fill. Thus spin-on process development has received increased attention recently as an attractive alternative to CVD processing. In this work we focus on elucidating the mechanism of UL wiggling and have synthesized materials that address several hypothesized mechanisms of failure: hydrogen content, modulus, film density, charge control unit type and thermal resistance. UL materials with high thermal resistance additionally provide the ability to expand the application of spin-on applications. Material properties and wiggle failure test results will be discussed.

8325-30, Session 8

Spin-on-carbon-hardmask with high wiggling resistance

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For the mass production of the advanced semiconductor device, the multi-layer process has been used for the essential technique {photoresist/ silicon contained hard mask (Si-HM)/ spin-on-carbon-hardmask (SOC)}. Spin -on-Carbon material plays a very important role during the etching process of substrates. The substrate etching process induces severe pattern deformations (called wiggling) especially with fine line/space patterns. Therefore, both the high etching resistances and the high wiggling resistance are demanded for SOC materials.

In this study, we investigated the etching performances with several SOC materials. We found that the relationships between SOC properties and the resistance for wiggling generation. We will discuss the material design of novel SOC for high wiggling resistance.

8325-31, Session 8

Substrate and underlayer dependence of sub-32nm e-beam HSQ pillar patterning process for RRAM application

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E-beam patterned HSQ resist pillar (island) is used as the mask for transferring pattern during dry etching. However, HSQ pillar is prone to collapse for aspect ratio (AR) over 2 during wet development. Therefore high AR bi-layer resist (BLR) pillar with organic underlayer (UL) is inevitable for etching of thick RRAM film stacking considering etch selectivity [1]. Selection of UL is a key factor to determine the AR of BLR pillar and selectivity during etching of hard mask (HM) and RRAM film stacking. Highly Carbon-contained UL has the advantage of achieving high AR BLR pillar and etch selectivity. In this work, e-beam patterning of HSQ pillar under various e-beam dose conditions, pattern density and HSQ thicknesses are studied on carbon highly contained UL TBLC-100PM. Hard mask layer of low temperature nitride (LTN) or oxide (LTO) above TiN/Ti/HfOx RRAM film stacking are also studied for achieving highest HSQ CD resolution.

8325-32, Session 8

High-resolution dry development

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As features sizes continue to shrink, new approaches are required to overcome roadblocks towards high-resolution lithographic patterning. One significant roadblock towards miniaturization is pattern collapse due to capillary forces during drying.[1] We have invented a dry development method for creation of high resolution and high aspect ratio resist features. We use resists that undergo an optical absorption change after exposure to high-resolution radiation (here we use electron beam lithography). This optical change allows the material to be selectively laser ablated such that the resolution is defined by the high-resolution radiation and not limited by the laser spot size. Using methyl-acetoxy calix[6]arene, a CW 532 nm laser, and spot sizes ~300 nm, we have produced features down to 10 nm in a film 120 nm thick, with pitch resolution down to 30 nm and aspect ratios of ~4:1 (Fig. 1). Calixarene was introduced as a high resolution electron-beam resist [2] and has demonstrated 12.5 nm half-pitch in extreme ultra-violet lithography.[3] Typically, films are spun thin to prevent high-resolution pattern collapse in thicker films but using the dry development, the patterns are well defined even in the thick, 120 nm film. Note, the resist acts negative with solvent development, as the cross-linked material can not be removed, whereas it is positive under laser dry development at the same electron-beam dose conditions. The mechanism and opportunities in other systems will be discussed.

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8325-33, Session 8

Conductive layer for charge dissipation during electron-beam exposures

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Electron beam resists develop a surface potential during exposure, which can lead to image placement errors of up to several nanometers [1] and account for poor CD uniformity and image quality. To address this problem, we have formulated a conductive polymer that can be coated onto the resist. Our conductive discharge layer (CDL) is water-soluble and it is easily removed during the processing steps.

Having established that our material has a low enough resistance for full charge dissipation, we have carried out extensive tests to evaluate the impact of the layer on lithographic performance. We will report these findings, which include measurements of effect of CDL application on the resolution, contrast, and speed of the resist, as well as analysis of, contact angle and surface roughness.

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8325-34, Session 8

Fabrication of high-aspect-ratio patterns by thermal nanoimprint lithography and a new bilayer resist system

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Nanoimprint lithography (NIL) has turned out as a very promising technique for the manufacturing of various micro- and nanostructures in research and industry.[1] However, most of the currently employed NIL resists only function properly for the imprinting of structures with low or moderate aspect ratios up to 3. But for specific applications, e.g. the fabrication of high-brightness LEDs, resist structures with significantly higher aspect ratios are well predestinated for such tasks. Such systems typically comprise of a thicker organic underlayer (transfer layer) and a thinner Si-containing layer on the top of the stack. The Si-containing resist material is imprinted with a relatively small aspect ratio of around 1. Due to the significantly higher etch resistance of the Si-containing resist toward oxygen plasma compared to the purely organic material of the underlayer, the relief profile and thus the aspect ratio is strongly amplified in an oxygen reactive ion etching (RIE) step. The obtained high-aspect-ratio patterns can be further used for a pattern transfer into the underlying substrate material utilizing adequate etching procedures.[2] Up to now, such bilayer systems are much more established for UV-based NIL rather than for thermal nanoimprint lithography (T-NIL) where only few literature has been published.[3]

Basically, a successful commercialization of a T-NIL resist depends considerably on a high flowability of the material to ensure a fast processing, and moreover on excellent release properties to minimize defects occurring during the demoulding step.

In this contribution we present a bilayer system with newly developed

materials for both the organic underlayer as well as the Si-containing T-NIL resist. As the synthesis of the T-NIL resist has already been published elsewhere,[4] we focus here primarily on the film forming properties, the imprint and demoulding characteristics, the flowability and in particular on the etching characteristics.

Both materials exhibit excellent film forming and adhesion properties, i. e. they show a good film homogeneity and a facile adjustablility of their film thicknesses via the spin-coating process, spanning from the sub-100 nm range up to several microns. The superior inherent flowability of the T-NIL resist was evidenced by applying short imprinting cycles while still obtaining a complete filling of even large microstructures exceeding the dimensions of several tens of microns. During the thermal imprinting of the upper Si-containing layer the organic underlayer is not affected or modified indicating a sufficient inherent dimensional stability of this material.

Due to the unpolar nature of the T-NIL resist material and also the admixing of a small amount of a fluorinated additive to the T-NIL resist formulation, the resist material revealed outstanding mould release properties enabling successful imprintings of 50 nm line-space patterns with excellent fidelity.

A removal of the residual layer consisting of the Si-containing material could be easily accomplished by a RIE applying fluorinated gases (CHF3 and CF4) while the anisotropic etching of the organic transfer layer was performed by an oxygen RIE. The generated high-aspect-ratio features were then further transferred into the underlying substrate material by applying suitable plasma etching procedures.

8325-27, Session 9

The development of a fast physical photoresist model for OPE and SMO applications from an optical engineering perspective

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Photoresist models and simulators are routinely used in lithography process analysis, problem solving, predictive estimation, and optical proximity correction determination. Most models tend to fall into 3 categories: 1) a very simple model, such as a threshold model, with few parameters; 2) a pure physical model that can have an enormous number of variables; or 3) an approximate model for OPC that will have interacted parameters that are used more as tuning "knobs" rather than actual physical parameters.

From the viewpoint of an optical engineer, the chemical processes effecting the interaction of light with the photoresist are seen as overly difficult to comprehend, especially to the non-chemist. They appear to the un-initiated as "voodoo physics", attempting to describe all mechanisms that occur with the photoresist process. Simulation algorithms such as molecular development effects, higher order post exposure bake kinetics and exact photoresist sidewall calculations can often seem unnecessary and even computationally excessive, especially when much of the subsequent metrology concerns itself with critical dimension measurement and/or two-dimensional top down profiles. The optical engineer will often resort to using a category (1) simulation, which while being simple may result in less accuracy and a more restricted region of validity. Unfortunately, when using advanced optimization techniques needed for optical proximity effect (OPE) matching and source mask optimization (SMO), even small errors in simulation accuracy are often unacceptable.

This work will describe a new photoresist imaging model and simulations that retain the fundamental physical and chemical properties of optical exposure, post-exposure bake and development. We apply dimensional reduction algorithms that reduce the imaging aspects of the problem, but preserve the imaging and thin film physics. This has the effect of simplifying the overall model and increasing the computational speed, while retaining an extremely accurate predictive capability. The model, named the RoadRunner Model, gives more detail and parameter intuition than a basic threshold model and agrees well with full photoresist

simulation. The model is easily adapted into OPE analysis and source-mask optimization.

We demonstrate the accuracy of this new model by experimental verification using one-dimensional and two-dimensional features through a pitch range on a Nikon immersion scanner. We show that the model can be extrapolated to multiple illumination source shapes. Specifically, the use of the model is examined for analysis of OPE and compared to more traditional simulators. An example of this is shown in figure 1 where a comparison is made of the RoadRunner model to a full photoresist simulation.

Finally, we will discuss the range of applicability of the model and its use in applications such line wide roughness analysis and EUV imaging. We will present an adaption of the model to incorporate relevant stochastic processes.

8325-28, Session 9

Simulation study of LWR bounding of depth of focus of various lithographic techniques: interference, optical projection, EUV, e-beam and hybrid complementary lithography, and proposal for a new production interference tool

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Interference lithography (IL) using coherent two-beam imaging generates image contrast neighboring in the 98% range in low flare, vibration mitigated systems. If system flare is maintained less than 6% then LWR is nearly 1 nm less than that of the next best imaging technique, dipole projection lithography and this is true over its entire dipole processing windows; but with less dependence on focus IL's capability extends well past that window too. This work shows that at a 76 nm pitch LWR of interference lithography potentially achieves the 2.5 nm ITRS limit, which when used in sidewall quadruple patterning or directed self-assembly allows 19 nm pitch processing with water. This work maps LWR to image contrast using LER parameterized resist models that are imaged using interference lithography, dipole projection printing and EUV and we also compare these results to literature results for all including e-beam (literature only). The contrast is varied in four ways: 1. By unbalancing the electric field between the two interfering beams. 2. By varying flare. 3. By defocus. 4. By pole size. To check these models we show for 193 nm imaging regardless of the way contrast is varied the LWR exhibits the same image contrast dependence for interference and projection lithography. Then we use this information to provide insight into imaging system extendibility and performance specifications. This work also shows how projection, direct-write and EUV imaging technologies can benefit from interference lithography with throughput enhancements from 2X to 20X and, arguably, with less LWR.

8325-35, Session 9

The Saga of Lambda: spectral influences throughout lithography generations

B. W. Smith, Rochester Institute of Technology (United States)

No abstract available

8325-36, Session 9

LER: the ultimate limiter for resolution in production?

C. A. Mack, Lithoguru.com (United States)

No abstract available

8325-37, Session 10

Patterning developments in spin-on hard mask systems for 30nm half-pitch EUV technology

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As Extreme Ultra Violet technology (EUV) is being introduced, multilayer hard-mask patterning becomes a key option in order to transfer the lithographic patterns into the circuit stack. In particular, spin-on multilayers can play a decisive role on the process roadmap as a more cost-effective solution than Chemical Vapour Deposition options. The integration of spin-on hard masks in EUV technology nevertheless requires these products to be EUV-outgassing friendly. In addition to this, the spin-on solutions must withstand the demanding photoresist and circuit stack aspect ratios during patterning. This paper presents the EUV process developments for contacted metal lines with 30nm half-pitch dimensions in a dual damascene application. We demonstrate the performance of an all-spin-on multilayer system composed of an EUV-photosensitive layer, an organic underlayer, a silicon-rich middle layer and a carbon-rich bottom layer.

Firstly, outgassing of the various polymer layers in vacuum is a critical parameter to control since it can directly impact the EUV-tool-optics lifetime. The qualification, selection and process optimisation of different materials for use in the ASML NXE:3100 EUV scanner is shown by correlating Residual Gas Analysis, Fourier Transform Infra-Red Spectroscopy and Spectral Ellipsometry. The outgassed species for different types of layers are compared. In this study, we quantify the shielding effects of the top layers on the outgassing of the layers underneath. The influence of the layer composition is also discussed.

Secondly, the lithographic performance of the 30nm half-pitch process on the NXE3100 is characterized with process windows and profile control using the IMEC process-of-reference and possibly newer state-of-the-art EUV photoresists for further scaling. The overlay results and CD uniformity within wafer and across wafer-batches are used to show the maturity of the process control.

Finally, considering the patternability of our EUV process, we demonstrate the ability of the all-spin-on multilayer system to planarize over the challenging dual damascene topography. To conclude on the potential of this scheme, we describe the etched dual damascene patterns into a dielectric stack which is representative for the 30nm half pitch technology node.

8325-38, Session 10

The novel spin-on hard mask and ultrathin UL material for EUVL

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For below Hp22nm generation, Hard-mask strategy is one of the key issues to achieve the good balance for Lithography and Etching performance.

The thickness of resist should be thicker enough to obtain the etching margin for the substrate etching. However, the thickness of resist needs to be thinner to obtain the good pattern collapse margin and resolution. In order to solve this tread-off, the spin-on hard mask (HM) technology can be applied.

On the other hand, the ultra thin organic Underlayer (UL) being combined with the CVD-HM film stack is also one of the processes for EUV lithography. In order to avoid the film loss of resist during UL open, the thickness of UL must be thinner and the etch rate need to be faster. We studied the effect of UL design and thickness for the EUV lithography performance.

For EUV lithography, the electron generation effect from UL is one of the key factors to improve the patterning performance of resist. In this paper, we studied the suitable functional group for the Si-HM and UL, which has high potential to generate 2nd electron and enhance the resist performance, and discuss the material design and performance.

8325-39, Session 10

EUV resist processing with flash-lamp

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EUV lithography (EUVL) remains as the leading candidate for the manufacture of devices beyond the 16-nm node. However, many challenges remain before EUVL is ready for application in volume production at these pattern sizes.

One of the most critical issues for EUVL is the readiness of resist materials for these stringent targets. For EUV resist materials, the main development issue is how to concurrently achieve high sensitivity, minimal resolution limit, and low line width roughness (LWR). At present, sensitivity and resolution continue to be improved through advances in resist material research. However, reduction of LWR remains a difficult issue [1]. Thus, the investigation of LWR-reduction from the viewpoint of resist processing has become necessary [1]. In recent years, some groups have reported resist process enhancements in the form of alternative developer and rinse solutions as possible methods for LWR reduction [1]. Another method that is being considered is shortening the acid-diffusion length of the photo-acid generator (PAG) through the optimization of the post-exposure bake (PEB) processes [3-5]. This has been shown to be feasible with the utilization of sub-millisecond bake technologies, as reported elsewhere [6].

With this concept, earlier reports have shown the potential of the flash-lamp (FL) bake process for EUV resist processing [7]. In earlier investigations, the FL bake method was utilized for post-exposure bake (PEB) applications. The bake process was performed utilizing a Xe lamp for instantaneous full-wafer (300-mm) baking. With this process, PEB times as short as a few milliseconds were achieved. Results indicated that resist lithographic performance using the FL PEB method was comparable to those obtained using conventional hot-plate based bake technologies.

With the feasibility of FL bake process as an alternative bake method for EUV resists, initial work has been started on its application for post-development bake (hard bake). The hard bake, when utilized at conditions beyond the resist's glass transition temperature will cause resist flow and/or in effect surface smoothening [6]. This effect can be manipulated in improving the LWR of very fine patterns. However, precise control at these unconventionally high bake temperatures will be necessary to avoid degradation of the resist patterns. The FL bake method is viewed as an effective way of achieving this, given its precise and instantaneous high-temperature heating capability.

During the conference, detailed results of these initial investigations on FL post-development bake on LWR, as applied on a variety of presently available high performance resists such as acryl-based, polyhydroxystyrene (PHS)-based polymer resists, and fullerene-based low molecular resists, will be presented.

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8325-40, Session 10

Stable, fluorinated acid amplifiers for use in EUV lithography

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One challenge facing the developers of EUV resists is the need to simultaneously improve resolution, line-edge roughness (LER), and sensitivity. However, these characteristics are inversely related, a relationship commonly referred to as the RLS trade-off.1 EUV resists are composed primarily of organic polymers and photoacid generators (PAGs). During exposure to extreme ultraviolet (EUV, 13.5 nm) light, the PAGs produce strong, fluorinated acids. Acid amplifiers are compounds that detect an acid signal (from PAG) and produce additional acid. This can be helpful in a photoresist by creating more acid in exposed regions thereby creating faster resists.

This paper is focused on the development of stable acid amplifiers (AA) and PAGs that produce lithographically useful strong, fluorinated acids. It has been shown that fluorinated sulfonic acids give improved lithographic performance due to more efficient catalysis with decreased diffusion. This, ultimately, allows the photoresist to have improved sensitivity and better resolution. Central to the design of new acid amplifiers for EUV lithography, is the need to control four properties:

Acid Strength: Catalytic acids should be as strong as possible, which is best done by incorporating fluorine atoms into sulfonic acids.

Acid Diffusion: Generated acids should diffuse as little as possible, which can be done through covalent linkage to polymer molecules.

Stability: Acid amplifiers should be as stable as possible in the absence of catalytic acid, and be thermally unstable in the presence of acid.

Unfortunately, acid amplifiers are significantly less stable as the strength of the acid generated by them increases. Figure 1 shows twelve first-order thermal decomposition rate constants as a function of acid strength as predicted pKa's and acid-amplifier body type. Figure 2 shows a plot of log decomposition rate vs. pKa of the acid generated by the AA. For the twelve compounds shown in Figure 1, the log-log plot is linear with R2 all greater than 0.98. We will present in our SPIE presentation and manuscript the structure of the new body type that provides 4-5 orders of magnitude greater stability when the acid generated is pentafluorosulfonic acid, and can produce a stable AA that produces one of the strongest acids, known-triflic acid. The design and structures of several additional AAs will be presented along with their lithographic performance.

8325-41, Session 10

Shrinkage distortions in EUV resists: CD-SEM and AFM investigations

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Both EUV and 193 nm photoresists are known to undergo significant electron beam damage during CD-SEM metrology. Damage is manifested as shrinkage that systematically distorts measurements of both one- and two-dimensional patterns.

Recently, Pistor et al. examined the issue of pattern distortion in EUV resists in some detail and concluded that observed pattern distortion could be linked predominantly to CD-SEM effects as opposed to other possible sources of shrinkage. By implementing a three-dimensional elastoplastic shrinkage model into a lithographic simulator, pattern distortions similar to experimentally observed observed distortions could be predicted.

Since interpretation of three dimensional resist profiles remains a long-standing challenge for CD-SEM metrology, we have been interested in AFM metrology as a method to complement and confirm CD-SEM measurements. Here, we link AFM measurements to CD-SEM measurements by comparison of pristine resist features with the identical features subjected to controlled amounts of e-beam damage. Additionally, we examine shrinkage-induced AFM profile changes and compare them with changes predicted by currently available simulation methods.

In addition to providing insight into fundamental metrology issues associated with measuring very small resist patterns, these studies may ultimately impact design and selection of future resist materials as well as development of pattern compensation methods.

8325-42, Session 10

Improvement of EUV resist performance through develop threshold modifications

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One of most persistent challenges in EUV patterning is the improvement of resolution, LER, or sensitivity (RLS) without negatively affecting the other two outcomes. This paper examines methods for altering the develop process and their impact to the RLS trade-off. Some of these methods include changing the developer (TMAH) concentration and introducing developer temperature changes. The impact of changes to the developer process can be quantified by measuring the resist dissolution rate at different exposure dose conditions. Simulation results with a stochastic resist model has shown the potential to impact LER by altering the dissolution characteristics. The authors use a development rate monitor (DRM) in order to measure the dissolution rate of resist materials and experimentally construct a dissolution curve or model. This technique demonstrates if a change to the development threshold at a given deprotection comes from an actual shift of the curve, a loss of develop contrast or a reduction in the maximum development rate. An approach to regain any sensitivity losses caused by threshold shifting will also be explored.

8325-43, Session 11

CD error budget analysis for self-aligned multipatterning

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EUV lithography is one of the most promising techniques for sub 20nm hp HVM devices, however it is well known that EUV lithographic solution still has significant challenges. Therefore we have focused on self aligned double patterning (SADP), because SADP easily enables the fine periodical patterning. As you know, SADP technique has already been applied to HVM devices such as NAND Flash memory. This technique also will be extended to DRAM and logic mass production devices in near future.

In general self aligned multi patterning consist of SADP, SATP(triple patterning), SAQP(quadrupling pattenring) and so on. We have already introduced innovative resist core based SADP/SAQP demonstrated results in past SPIE.[1][2] Our proposed SiO2 spacer is directly deposited on resist core via a low-temperature deposition process.

SATP and SAQP enable making further down scaling to 10nm-15nm hp from SADP, however CD controllability for SATP/SAQP become more

sensitive.

In this paper we would discuss about CD error budget analysis for self aligned multi patterning including a newly developed SATP scheme.

8325-44, Session 11

Demonstration of 22nm SRAM features with patternable hafnium oxide based resist materials using electron-beam lithography

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Scaling down the critical dimensions (e.g. of the transistor gate length) is the main driver in semiconductor business. Resists with high resolution, low LWR/LER and high sensitivity are needed for electron beam lithography to fulfill the requirements of future technologies. The tradeoff between high resolution and low sensitivity for non-chemically amplified resists needs to be overcome. Electron beam exposure results using new inorganic non-chemically amplified resists with high resolution and high sensitivity have been shown. These inorganic resists are promising candidates for electron beam lithography as well as for EUV lithography. As metal oxides these resists have etch resistance comparable to hardmask materials. So far, the feasibility of these resists in a near production environment and first exposure results of real application pattern have been shown.

Inorganic resists were investigated which are directly imageable. The resists are based on hafnium oxides and cast from aqueous solutions. They differ in sensitivity and resolution. The resists were processed in a 300mm CMOS manufacturing environment and exposed on a 50kV VISTEC SB3050DW variable shaped electron beam direct writer at Fraunhofer CNT.

In this paper, the evaluation of inorganic resists will be discussed. The resists were evaluated in terms of contrast, sensitivity, resolutions and LWR/LER. The exposure sensitivity, also called base dose characterization, is observed with the CD-dose matrix exposure of 1:1 dense pattern. The process characteristics required for CMOS manufacturing such as shelf life, vacuum stability, post coat and post exposure delay will be examined. Furthermore, it will be demonstrated the exposure of real application pattern, for example large SRAM layer shrink down to the design CD of 22 nm.

8325-45, Session 11

Direct implant through BARC

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Implant lithography had been considered as a non-critical layer in device manufacturing for a long time. But beyond N32 node, implant lithography will be as a critical application to manufacture device because of CD shrinkage and tighter pitch.

Options for implant layer lithography are (1) TARC / resist stacks, (2) resist / DBARC stacks and (3) resist / BARC stacks using dry etching. TARC / resist stack is the industry standard process for implant lithography but causes issues of resist pattern profile such as standing wave and notching because of reflectivity derived from substrate surface. For resist / DBARC (Developable BARC) stack, DBARC thickness influences shape of DBARC pattern, and causes the smaller litho-margin and scum issue in case of topography wafer. Resist / BARC stack using dry etching has concern of high etching cost and damage of substrate surface. As above, these three methods have the problems for implant lithography process. How to solve this problem is very important topic now.

In this paper, we propose a new concept that we use resist / BARC stacks and directly implant through BARC. The biggest advantage of this concept is that substrate is not damaged and good lithography process window can be obtained. We study the influence of polymer type of BARC, the thickness of BARC, dose of implant energy and type of implant ion. Based on these results, we report the performance of direct implant through BARC.

8325-47, Session 11

Focus improvement with NIR absorbing underlayer attenuating substructure reflectivity

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Process dependent focus leveling error occurs in photolithography due to the unpredicted reflectivity from multi-structures on the fully integrated process wafer. Typical wavelength used in optical focus sensor is in the near IR range which is highly transparent to most of the dielectrical materials. Therefore, the reflected light from multi -structures perturbs the accuracy of leveling signal reflected from resist surface. To alleviate this issue, air-gauge focus sensor has been used to measure the wafer surface topography for an in-situ calibration to correct the focus leveling error. Since it will take longer time for air-gauge sensor to measure the wafer z height on every wafer, it has been used as an offline focus calibration. Even with this approach, throughput has been an issue and wafer to wafer focus variation has not been fully compensated.

To prevent the NIR light reflected from muti-structures shifting the regular NIR light reflected from resist surface, an NIR absorbing layer is needed to attenuate this reflected NIR light. Therefore, NIR absorbing underlayer has been developed for easy insert to existing resist coating process. To effectively reduce the reflection from the multi-structures, proper absorbing dye has been chosen and tailored to absorb the majority of the broad band NIR leveling signal.

Formulation of the dye and polymer resin plus various other components was optimized to have good reflectivity control at 193nm, at the same time to meet the solvent rinse resistance, etch and outgassing requirements. It has been demonstrated that focus range was reduced from 80nm to 30nm when regular underlayer was replaced with NIR underlayer, and more than 40% common DOF improvement was observed on stacked wafer. It has also been demonstrated that air-gauge sensor can be turned off without showing any degradation in leveling data or litho performance on BEOL integrated wafer.

8325-48, Session 11

Design, synthesis, and characterization of KrF negative developable bottom antireflective coating materials

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With the demands in the shrinkage of microelectronic feature size of the circuitry integration and the increasing pressure to cut lithography operation cost, high performance KrF negative implant resist has become the interest of research and development due to its trench clearing power, low shrinkage upon high energy implant process and cost competitiveness when compared to its KrF/ArF positive counterparts. However, the challenges to develop a successful KrF negative implant resist are the topography after gate patterning and reflectivity complexity of silicon, silicon oxide and silicon nitride surface that resist is laid upon. Reflectivity control, resist profile control, and critical dimension (CD) uniformity have then become critical issues to enable its lithography performance at high numerical aperture. Generally, substrate reflectivity, resist profile, and CD uniformity were controlled by a top anti-reflective coating (TARC) layer, but it is becoming less effective in 14 nm node implant process than prior nodes.

Here we describe the design, synthesis and characterization of a series of novel KrF negative developable bottom anti-reflective coating (NDBARC) materials suitable for KrF negative implant resists. When these NDBARCs are used in combination with implant resists, they demonstrate desirable physical properties such as solvent resistance, developer solubility, film forming quality and optical density. These NDBARC are compatible with negative implant resists at the matching photosensitivity. When screened against single layer KrF negative implant resist with TARC, these NDBARC/implant resist combinations offer a comparable lithography performance, excellent trench clearing power and reflectivity control.

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8326-01, Session 1

Challenges and solutions for overlay in low-k1 imaging: model for the printing of large features with extreme illumination, and the subsequent inspection with edge-detection or scatterometry based metrology

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The continuous shrinking in optical lithography and the physical limitations in both, shorter wavelengths as well as large numerical apertures, required the industry to adapt more and more sophisticated illumination schemes. In order to print lines with a pitch that comes close to a k1 of 0.25, extreme dipole illuminations with small angular openings and extremely small ring widths are required. Such illumination establishes almost a two-beam imaging situation for the small pitches which results in a good contrast and a large depth of focus. Overlay markers, however, are typically much larger than the actual device features, up to several microns. The printing of such large structures suffers substantially from using these extreme illumination conditions. Aerial images show optical proximity effects in the order of several 100 nm for these large features which is somewhat counter intuitive. The resulting resist profiles reveal significantly sloped sidewalls that change through focus and dose.

Simultaneously with this resolution-driven trend to extreme illumination conditions, the device physics drives overlay requirements towards single digit nanometer values. Assigning such a single digit nanometer position to the aforementioned large and irregularly shaped resist profiles, though, becomes almost a meaningless task. Both, edge detection based overlay metrology as well as scatterometry based methods, face a new set of challenges to return an overlay number that represents the locations of the actual device structures.

This paper explains why large features print so unexpectedly poor under extreme illumination conditions, even in the absence of any aberrations. It further establishes a method how to understand and predict the results of overlay metrology on 3-dimensional resist profiles. In particular, a simulation flow is presented which covers the lithographic exposure as well as the actual inspection of the resist profiles. Both edge-detection (with broadband illumination) and scatterometry-based metrology are covered. It is shown how this flow can be used to study the impact of scanner/process imperfections on the overlay readings. This helps to classify these imperfections, gain a deeper understanding of the critical parameters in the printing and inspection of overlay marks, and eventually develop and assess mark enhancement strategies such as chopping and/or applying assist features.

The modelling and tooling developed in this paper will be applied in the paper "Study of high order distortion in intra field using extreme off-axis illumination on a manufacturing site" by Kiho Yang et al., presenting simulation studies together with a significant number of wafer data.

8326-02, Session 1

Study of high order distortion in intra field using extreme off-axis illumination on a manufacturing site

J. Lee, B. Lee, T. Lee, J. Park, C. Lim, M. S. Kim, H. Kang, Hynix Semiconductor Inc. (Korea, Republic of); J. T. Neumann, Carl Zeiss SMT GmbH (Germany); E. Janda, ASML US, Inc. (United States); K. Bhattacharyya, ASML Netherlands B.V. (Netherlands); B. Geh, Carl Zeiss SMT Inc. (United States); C. Ryu, Y. Min, ASML Korea Co., Ltd. (Korea, Republic of)

Challenges for the upcoming overlay control under 3Xnm nodes are unprecedented with usual specifications in semiconductor manufacturing. As the cell size of memory device is decreasing, various resolution enhancement techniques have been developed to make smaller patterns on the wafer. One of preferred techniques to make fine patterns in microlithography is the application of extreme off-axis illumination (OAI) which is optimized to specific memory cell structure. The choice for OAI has been made under the assumption that there would be little or no impact on the printing fidelity of large structures, such as overlay marks. We know now, that this assumption - even though intuitive - is incorrect.

In this paper, we analyzed the origin of intra field overlay error caused by aberrations under extreme OAI (as it is called 'delta distortion') with ASML and Carl-Zeiss. Our study will focus on impact of scanner/process imperfections on the overlay readings in view of real device as a manufacturing site. In this paper, results on delta distortion study are reported as below.

1) It was shown that delta distortion level is too high considering normal scanner aberrations.

2) We confirmed that delta distortion reading varied significantly through Energy/Focus change as well as among exposure tools.

3) In a separate paper, we will provide the foundation to understand and predict overlay performance with extreme OAI for both image based overlay (IBO) and diffraction based overlay (DBO) (Presenter: Jens-Timo Neumann)

4) We performed various studies to minimize the delta distortion effect of the overlay reading.

- Overlay mark size split

- Comparison between image based overlay and diffraction based overlay method.

- Comparison of overlay reading with various segmentations.

- Comparison on overlay of cell patterns and various vernier patterns.

8326-03, Session 1

Spacer process and alignment assessment for SADP process

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Self aligned double patterning (SADP) is now widely accepted as a viable technology for the further extension of 193nm lithography towards the 22nm /18nm technology nodes. SADP was primary introduced for the manufacturing of flash memory due to its 1D design geometry. However, SADP became a main stream technology for advanced technology nodes

for logic product.

SADP results in alignment and overlay marks with reduced image contrast after completion of spacer patterning. Consequently there is an elevated risk that the overlay performance of the cut lithography layer on the spacer may be negatively impacted.

The self aligned spacer process results in asymmetric spacers. Two types of surface (inside and outside) of the spacer are formed. This asymmetry has an impact in respect to the decomposition of the layer on overlay and CD control tolerance.

Immersion scanner has made huge improvement on overlay specification. A large amount of work has been made to correct the non linear alignment error and the mask error. An assessment on 193nm immersion lithography cluster of alignment and overlay tolerance will be made on wafers with different spacer technology.

SADP is used in combination with trim lithography and results in double patterning lithography. Some solutions for 22nm and 14nm technology are combining SADP with different decomposition model. Double mandrel layer can be used for wiring layer on logic product. SADP can be as well combined with cut lithography or double cut lithography. The cut lithography can be varied as positive and negative patterning. The different decompositions of each layer according to the required design rules have some consequences on the tolerances used in lithography in terms of overlay. These different aspects will be discussed in this paper.

8326-08, Session 1

Overlay accuracy with respect to device scaling

P. J. Leray, S. Y. Cheng, IMEC (Belgium)

Overlay metrology performance is usually reported as repeatability, matching between tools or optics aberrations distorting the measurement (Tool induced shift or TIS). Impressive improvements of these metrics have been achieved in the past years by tool suppliers. But, what about accuracy? By using different target type, we have already reported small differences in the mean values as well as the fingerprints [1]. These differences are making the correctable questionable. Which target is right, which translation, scaling should we feedback to our scanner?

In this paper we will investigate the source of these differences using several approaches. First, we measure the response of different targets to several overlay offsets programmed in a test vehicle. Second, we check the response of the same overlay targets to overlay errors programmed by the scanner. We will compare overlay target design: what is the contribution of the feature sizes composing the target? We will use different overlay measurement technique: is DBO (Diffraction Based Overlay) more accurate than IBO (Image Based Overlay)? We will measure overlay on several stacks: what is the stack contribution to inaccuracy? In conclusion, we will explain partially the observed differences and propose solution to reduce them.

[1] "Diffraction Based Overlay Re-assessed" P. Leray, D. Laidler, K. D'havé, S. Cheng. Proc. of SPIE Vol. 7971-14.

8326-09, Session 1

New analytical algorithm for overlay accuracy

B. Ham, S. Yun, M. Kwak, S. M. Ha, C. Kim, S. Nam, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

The extension of optical lithography to 2Xnm and beyond is often challenged by overlay control. With reduced overlay measurement error budget in the sub-nm range, conventional Total Measurement Uncertainty (TMU) data is no longer sufficient. Also there is no sufficient criterion in overlay accuracy. In recent years, numerous authors have reported new method of the accuracy of the overlay metrology: Through focus and through color. Still quantifying uncertainty in overlay measurement is most difficult work in overlay metrology. We develop an analytical algorithm for overlay accuracy. And a concept of non-destructive method

is proposed in this paper. For on product layer we discovered the layer has overlay inaccuracy. Also we use find out source of the overlay error though the new technique. Furthermore we compare the empirical data to simulation data. Our results show that to characterize an overlay metrology technique that is suitable for use in advanced technology nodes requires much more than just evaluating the conventional metrology metrics of TIS and TMU.

8326-04, Session 2

Extending the DRAM and FLASH memory technologies to 10nm and beyond

U. Chung, Samsung Advanced Institute of Technology (Korea, Republic of)

No abstract available

8326-05, Session 2

CMOS device technology: current status and future prospects

T. Ghani, Intel Corp. (United States)

No abstract available

8326-06, Session 3

Lens heating challenges for negative tone develop layers with freeform illumination: a comparative study of experimental versus simulated results

S. D. Halle, IBM Corp. (United States); M. Crouse, ASML US, Inc. (United States); T. A. Brunner, IBM Corp. (United States); A. Jiang, ASML US, Inc. (United States); M. Colburn, IBM Corp. (United States); H. Cao, Brion Technologies, Inc. (United States); B. Minghetti, Y. van Dommelen, ASML US, Inc. (United States)

Immersion lithography continues to add complexity to meet the challenges of future generations of CMOS for 22 nm and beyond. The needs of double patterning (DP) are being met with the latest generation of ASML's NXT scanners, which achieve 175 wafers per hour throughput and sub-5nm overlay performance in manufacturing. However, future nodes are demanding further complexity in terms of Source Mask Optimization (SMO) and freeform pupils enabled by ASML's FlexRay illuminator. In addition to DP & SMO, tone reversal is being pursued to enhance the printability of 22 nm node BEOL layers through Negative Tone Development (NTD). These components taken together: higher throughput for DP, freeform illumination for SMO and higher transmission masks for NTD BEOL levels can create significant amounts of lens-heating induced aberrations that must be addressed as part of the process development effort. In this paper, we examine the lens-heating induced aberrations due the cumulative complexity of DP, SMO and NTD for IBM's BEOL levels both experimentally and in simulation through the use of ASML's BRION Tachyon Lens Heating Module (LHM).

As a result of this work, we demonstrate the primary impact of lens-heating induced aberrations are CD changes (through best focus drift) and pattern placement (through odd Zernike orders impacting overlay). Specifically, Zernike orders Z5, Z7, Z9, Z12 and Z17 were found to be strong functions of lens heating for the BEOL NTD levels. Additionally, the Tachyon simulated lens-heating behavior and correction recipe (C-ASCAL) were demonstrated to closely match the performance of experimentally measured lens heating behavior both in terms of within lot heating behavior (from first to last wafer) and CD through-slit signatures ("hot lens" condition and within a given exposure field). A significant

advantage of the LHM + C-ASCAL simulation approach to predicting and correcting for lens heating induced aberrations is that this approach can be done completely offline and thus does not consume scanner time to produce calibration curves. Additionally, ASML's BRION Tachyon LHM is demonstrated for pre-screening lens heating induced process impacts for a given set of mask features. This allows for lens-heating aware iteration of all or any of the following: design, RET, SMO and/or OPC. Thus enabling correction of the mask or process prior to discovering the lens heating induced effects on production wafers. Lastly, we examine lens heating induced pattern placement errors (overlay errors) demonstrated for strong dipole pupils and asymmetric reticles. Experiments and simulations are compared for overlay errors created by effects of coma, focus shift and 3-foil aberration. Tachyon simulated and experimental corrections are shown to match and a mitigation strategy of C-ASCAL with ASML's Advanced Lens Controller (ALC) is demonstrated.

8326-07, Session 3

Single method as OPC reference and fast tool with linear time and memory resort for exact reticle modelling

A. V. Tishchenko, Univ. de Lyon (France)

The status of OPC is presently characterized by a systematic resort to FDTD as a reference, and approximate tools such as the DDM or M3D [1] which combine the speed of Kirschoff's approach with the exactness of the FDTD by empirically importing some corrective factors provided by the FDTD. These however are not broadband and the stability of the optimisation process is still a matter of concern. Thus, the interest for a method which is both a reference and an OPC-tool. This is beyond reach for both FDTD and RCWA methods. The method presented here does it.

The present paper limits itself to the most critical task: the calculation of the complex transmitted field through a reticle under arbitrary incidence, leaving the field propagation to the resist-coated wafer to existing methods like field tracing [2].

The method models the transmission of a reticle area large enough to be representative of the function that it will perform once integrated in the wafer. N being the number of diffraction orders representing the 3D complex index distribution of the considered reticle area, the required calculation time and memory resort grows like O(NlogN) and N, respectively, instead of O(N3) and O(N2) as in standard methods like the RCWA [3] for a comparable accuracy as shown in Fig. 1 on a test structure. The method achieves this by a disruptive algorithm based on the Generalized Source Method [4] expressing all matrices in the Töplitz and diagonal forms, resorting to the FFT and skipping matrix inversions by means of the GMRES [5]. The slope of the flanks is considered as is without staircase approximation. The accuracy and the calculation time and memory characteristics of Fig. 1 were compared with the RCWA [3] and the C-methods taken as references.

The rationale of the method involves the following steps. The considered reticle area is sliced, in each slice the permittivity and flank slopes are Fourier transformed. The unknown field implicitly contained in an integral volume equation is in turn Fourier transformed. This integral equation is then discretized and expressed in terms of matrices which are all reconfigured in form of Töplitz and diagonal matrices. All matrix inversions are replaced by multiplications using the GMRES and FFT.

The presentation will identify the critical passages of the treatment and reveal the keys enabling this dramatic time and memory reduction. The method can also be applied at the level of the wafer where any topography and material diversity can be exactly accounted for. This method is also breakthrough in other domains, eg, high-NA DOEs, scattering layers in LEDs/OLEDs.

References

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8326-08, Session 3

Evaluation of various compact mask and imaging models for the efficient simulation of mask topography effects in immersion lithography

V. Agudelo, P. Evanschitzky, A. Erdmann, T. Fühner, Fraunhofer-Institut für Integrierte System und Bauelementetechnologie (Germany)

A major concern of mask and imaging modeling in lithographic simulations is to obtain a good compromise between accurate models, e.g. fully rigorous mask diffraction and vector imaging computation without the Hopkins approach, and fast models like Kirchhoff approach. Compact models such as decomposition techniques and boundary layer models provide an alternative to speed up calculations while yielding results with reasonable accuracy.

In this work, correction techniques in the spatial and frequency domains are applied to improve the accuracy of less rigorous but more efficient mask models. In this way it is possible to reproduce the EMF effects predicted by the rigorous model preserving the simplicity of the Kirchhoff model.

In the frequency domain, two approaches are considered. First, a Jones pupil function is introduced in the projector pupil plane to describe amplitude, phase and polarization effects which are introduced by the mask. Second, a correction process performed directly on the scalar spectrum is used to tune the diffraction orders that get into the pupil of the optical system. In this case, since a vector description is needed to include the polarization phenomena, the spectrum for the different polarization components is constructed from the scalar spectrum transformed with the corresponding computed filter. The Jones pupil and correction functions are obtain by calibration with a rigorous model.

In the spatial domain the well-known boundary layer method is considered. In this case, the thick mask is replaced by a modified thin mask. The bright features of the mask are surrounded with a semi-transparent region with a certain width, transmission and phase. Alternatively, the bright mask features of the Kirchhoff model are modified by adding delta functions to the edges of the absorber. The amplitude and values of the boundary layer and delta function, respectively, are obtained by a calibration with a rigorous model.

The validity of these filtering techniques for different illuminations, materials, feature sizes, pitches and shapes is investigated.

8326-09, Session 3

A full-chip 3D computational lithography framework

P. Liu, M. Feng, S. Lan, Q. Zhao, Z. Zhang, H. Liu, V. Vellanki, Y. Lu, Brion Technologies, Inc. (United States)

As semiconductor feature sizes continue to shrink, the allowable error margins for critical dimension (CD) control become increasingly tight. As a result, 3D lithography effects previously considered trivial start to show bigger impact to device patterning processes. These effects include mask topography, resist profile and wafer topography.

Mask topography effects have already generated a lot of studies since the minimum feature size on mask reduced to below the exposure wavelength. These studies have shown that some important experimental observations cannot be explained by thin mask model (a.k.a. Kirchhoff model). Examples of these observations include image imbalance in earlier development of alternating phase shift mask and more recently best focus variations among different device features. These observations can only be explained by the electromagnetic field (EMF) scattering effects caused by the mask topography.

Device makers also begin to observe resist profile related patterning issues, for example, effects of resist top loss and sidewall angle on the subsequent etch process and printing problems of sub-resolution assist

features (SRAF). Standard full-chip optical proximity correction (OPC) and verification applications generally compute only 2D resist contours in a given horizontal resist plane. However, it has been shown that 3D resist simulations are required to identify those patterning problems that are impossible to detect with 2D contours.

Lastly, wafer topography effects from underlying patterned layers begin to receive attentions as well, particularly for patterning layers where no or less effective bottom anti-reflection coatings (BARC) are used. Both experimental studies and rigorous 3D wafer simulations have shown that the exposure image distortions caused by the underlying wafer topography are so severe for some features in an implant patterning process that model-based OPC is required to correct the problem.

In order to detect and mitigate the problems related to 3D lithography effects via OPC at the mask data preparation stage, the associated computational lithography model must have the capability to accurately simulate these effects. Although rigorous physical models are available for accurate simulation of these effects, they are computationally too expensive to use in full-chip OPC and verification applications. In this work, we will describe a 3D computational lithography framework for full-chip applications. We will first discuss efficient and accurate methods that extend the existing 2D framework to 3D, and then present evaluation results against rigorous simulations and experiments.

8326-10, Session 4

Interactions between imaging layers during double-patterning lithography

S. A. Robertson, KLA-Tencor Corp. (United States); P. Wong, P. De Bisschop, N. Vandenbroeck, V. Wiaux, IMEC (Belgium)

Immersion ArF double patterning techniques using either LLE (Litho-litho-Etch) or LELE (Litho-Etch-Litho-Etch) processing schemes are the most promising short term solution for near future device shrinks with the continued delay in the arrival of production ready EUV.

In recent experimental work from Imec [1], interactions have been observed between the first and second litho steps of a LLE process. These interactions show that the line printed in the second litho step trends with the line size in the first litho step. As the litho 1 line CD increases, so does the litho 2 line size, even though the second lithography step is utilizing a fixed focus and dose.

A high accuracy physical model had been developed for the LLE resist process in question [2]. When simulations of the Imec experiments were run, similar interactions between the two lithography process were observed.

In this study, we use lithography simulation to indentify the major causes of the cross-talk between the lithography steps. Three sources are identified: two optical whilst one is related to the resist post-exposure bake process. Having identified the sources of the interaction, simulation is then used to evaluate a process strategy for mitigating the effect.

We then use simulation to evaluate the extent that local linewidth variation in the litho 1 features (LER) is transferred to litho 2 imaging, i.e the degree of correlated LER between the two imaging layers.

Finally, simulation is used to evaluate the impact of similar phenomenon occurring during LELE processes - in both bright field and dark-field patterning (LLE processes only being suited to bright field patterning).

1. Wong et al., "Litho 1-litho 2 proximity differences for a Litho-Process-Litho Double Patterning Process" submitted to this conference.

2. Robertson et al., "Characterization of a 'Thermal Freeze' LLE Process for Predictive Simulation", Proc. SPIE 7973, 79730L (2011)

8326-12, Session 4

Design compliance for spacer is dielectric (SID) patterning

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Self-Aligned Double Patterning (SADP) is an option for the Metal layers of the 14 nm node because of several advantages over Litho-Etch-Litho-Etch (LELE) Double Patterning. First, SADP has lower LWR (line-width roughness) and better CD control due to process characteristics. Second, line-end spacing can be tighter than for LELE since a Trim mask in SADP can perform line-end cutting. For example, the first SADP mask can create a line-space array, and the second SADP mask (the Trim Mask) can remove unwanted portions of that array. Third, SADP can be less sensitive to overlay errors than LELE due to its self-aligned nature.

Among the several flavors of SADP, we will focus on the Spacer Is Dielectric (SID) flavor. SID allows the largest range of feature CDs, and is suitable for the Metal layers. However, SID SADP has some drawbacks. First, SID has more complex processing than LELE. Second, it is not practical for random contact or via layers. Third, only certain space CDs are achievable. Finally, and most importantly for this study, the layout design is more restricted than for LELE. That is, among all possible layouts, a smaller set is compatible with SID than with LELE.

To illustrate that SID puts additional restrictions on design, Fig. 1 shows LELE-compliant designs that are not SID-compliant. In particular, SID does not allow polygon stitching, as shown in Fig. 1a. Even if a layout does not require stitching, the Trim mask for SID can have minimum-space violations, as shown in Fig. 1b.

When creating layouts to be patterned with SID, we should be aware of the following issues. First, SID has overlay-sensitive regions. That is, there are features whose size depends directly on the position of the Trim mask, as shown in Fig. 2. Second, it may be necessary to upsize features because we are restricted to certain space-CD values. Third, as mentioned, the Trim mask can be prone to spacing violations.

In this work, we will explore how to construct or modify layouts to be SID-compliant. For shrinking existing layouts from an earlier technology node, asymmetric shrinking works well for LELE. For example, we can shrink more in the x direction than in the y direction. This approach may need adaptation for SID. On the other hand, for constructing a new layout, we may begin with a simple uni-directional layout. We will then explore the spacing rules required for features in the non-preferred direction. In addition, we are interested in a basic set of design rules for SID. That is, in a simple dictionary of forbidden layout configurations. This dictionary would not be exhaustive. This paper will present the most common layout configurations that are not SID-compliant and which can therefore hopefully be avoided.

8326-13, Session 4

Litho 1-litho 2 proximity differences for a litho-process-litho double-patterning process

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Double Patterning (DP) is the most immediate lithography candidate for IC technologies requiring pitches below the single exposure capabilities of today's ArF immersion scanners. Litho-Process-Litho-Etch (LPLE) double patterning processes potentially offer substantial cost and throughput benefits over the more proven Litho-Etch-Litho-Etch (LELE) approaches. However, LPLE DP approaches typically use a different resist for each lithography step and there are many potential process and material interactions between the lithographic layers which could have an impact on proximity effects after full DP flow.

In this work, one specific LPLE process is used and the impact of process and material interactions on proximity effects is investigated. The process windows for several pitches and optical proximity behaviour of both litho 1 and litho 2 are studied. Results obtained from a single patterned wafer are compared to results from a single patterned and double patterned area on a double patterned wafer.

The results reveal that there are process window and proximity differences between single and double patterned wafers showing the

influence of a neighbouring line from another patterning step. The process windows are different for all cases : single patterned wafer versus single patterned and double patterned area on double patterned wafer. Moreover the process window differences do not just consist of a simple shift along the dose axis.

For a few specific cases the experimental results are compared to calibrated LPL Prolith model predictions. The Prolith simulation model matches the experimental data and helps to distinguish between chemical, optical and processing effects as the root cause of the observed differences.

8326-15, Session 4

Characterization and decomposition of self-aligned quadruple patterning friendly layout

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As the self-aligned technology has shown its great advantages in process control, memory process has jumped ahead into 14nm half-pitch process with the help of self-aligned quadruple patterning (SAQP) process. With the upcoming process requirement for the random logic circuit to also achieve sub-14nm technology, while EUV is still lagging behind, SAQP is now facing a promising challenge to be implemented in the random logic design.

However, SAQP process has its own intrinsic properties. One property is its periodical pattern structures, which always follow an A-B-A-C pattern around the core feature. Another property is the different line-width variation according to the formulation of the pattern. Both of those properties will generate very strict SAQP friendly design rule, and a thorough characterization of the SAQP friendly design is greatly needed.

In this paper, similar to the 2D layout decomposition problem for SADP process, we will introduce the algorithm for layout decomposition and mask preparation for core and trim. With the information of the periodic structure and the distance between the features, the layout that is friendly for SAQP can be characterized. The information can thus be easily generate the recommended design rule to increase the decomposability ratio and help bridge the gap between the manufacturing requirement and the design preferences.

8326-89, Session 4

Stack effect implementation in OPC and mask verification for production environment

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With the decrease of the transistors dimensions, process steps usually considered as not critical become challenging. This is the case for implant levels patterning, which can be strongly impacted by reflections and diffusion on the underlying active and gate patterns, especially when no anti-reflective coating can be used. This stack effect leads to unexpected resist shape on wafer if not taken into account during OPC flow.

We propose a solution to integrate stack effect onto existing OPC models in order to allow a stack-aware OPC or mask verification. This method can be implemented in a standard OPC flow offered by EDA OPC software. It provides effective results compatible with production constrains, such as stack-aware full chip simulation and run time efficiency.

8326-16, Session 5

Source-mask optimization incorporating manufacturability constraints

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At low k1 factors, source-mask optimization (SMO) is required for obtaining sufficient process stability (MEEF, DoF, EL). However, frequently the optimization quality for source and mask patterns is diminished by manufacturability constraints, e.g. to achieve acceptable mask writing time. Optimization results often require post-processing in order to fulfill these constraints. This approach is time-consuming and can compromise the optimized process stability. The presented method overcomes these problems by solving directly a constrained optimization task. Constraints cover symmetry and distance relations between mask features and control source properties. Such an optimization results in a manufacturable solution. The concept of constrained optimization can be also extended to assist feature placement. Assist feature seeds can form real assists during SMO at favorable positions only if manufacturability conditions are met. In that way source shape and main features as well as model-based assist features are optimized simultaneously. Moreover, the method can also be extended to a rigorous simulation approach, where for instance physical resist modeling and/or 3D mask effects are incorporated. The examples shown in this paper demonstrate the particular suitability for symmetrical and/or periodical mask patterns, e.g. SRAM and other array cells. In addition, the computational SMO engine can handle simultaneous multi-pattern optimizations and also allows optimizing larger regions including array edges/corners, taking into account pre-optimized surroundings.

8326-17, Session 5

Achieving first-time-right mask layouts

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Source mask optimization (SMO) and inverse litho technology (ILT) solutions have recently proven the potential of extending the lifetime of ArF Lithography. The application of those technologies for production demands a first-time-right capability. We are proposing three criteria for first-time-right SMO/ILT with focus on layout optimization.

The first criterion is optimal process stability for individual critical dimensions. We introduce a cost function that allows a site specific control of the individual process performance metrics exposure latitude, depth of focus and mask error enhancement factor to guarantee a balanced overall process window as well as best point pattern fidelity.

The second criterion is mask rule compliance and cost efficient mask making. SMO/ILT usually yields complex pixelated and/or curvilinear mask solutions to fulfill high demands on the process stability of optimized patterns. The complexity of these patterns increases mask writing cost so that mask simplicity becomes an important measure for optimization results. Subsequent clean up steps and mask rule enforcement is required, modifying the previously found optimal mask pattern and possibly compromising valuable patterning performance for manufacturability. We circumvent this issue by applying a mask representation that guarantees the fulfillment of mask rules for both main features and model based assist features intrinsically and keeps mask layout at a mask writer friendly complexity, so that a post correction or post simplification is not required. In order to fully explore the many degrees of freedom of the mask we run optimization with millions of iterations.

The third criterion, model accuracy and reliability, shall ensure a ready-

to-tape-out optimized mask layout without the need of OPC post processing, experimental or simulation verification. The vast variety of mask patterns that span the possible solution space demands a simulation model that is capable of extrapolating beyond its calibration dataset. We use rigorous simulation models to provide that predictive performance. A hybrid method allows the application of calibrated rigorous models despite the aforementioned millions of iterations.

The new optimization technique fulfilling the above criteria was applied to a generic DRAM contact array edge with 160nm x 160nm pitch in a stepwise optimization: First, the inner region of the array is source-mask co-optimized to meet the tight CD specification. The resulting source is available as a pixelated source and also as a derived parameterized source and will not be touched for further optimization. Second, the horizontal and vertical edges are optimized separately and finally the corner is optimized having the edges as static boundary conditions. The stepwise treatment showed advantages with respect to runtime and conservation of given symmetries. Process performance criteria with respect to previously defined DoF, EDL and MEEF were met for all patterns.

8326-18, Session 5

Mutual source, mask, and projector pupil optimization

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Source/mask optimization (SMO) is considered one of the keys for lithography to meet upcoming requirements. More recently, the projector pupil has been demonstrated to be another candidate for wavefront engineering. This paper presents a combined source/mask/pupil optimization (SMOP) procedure, whose goal is the maximization of the common process window of different features including contact holes and line/space patterns with different pitches and orientations.

For the illumination source, a pixelated representation, where each pixel takes one of a discrete set of intensities, is chosen. In order to adequately restrict the search space, the grid is defined as a polar one, subdividing the source into tracks and sectors. Different sample densities and their impact on both the optimization results and the efficiency are examined. The parameters of the photomask include the line width of features and the number, position and dimension of SRAFs. Variations of the pupil wavefront are represented using Zernike polynomials, whose coefficients form additional optimization parameters. Different spherical and astigmatism aberrations are included. The process window overlap is mutually optimized for a number of different polarization degrees of an x/y-polarized illuminator, rendering the optimization problem a multi-objective one. It is solved with a multi-objective evolutionary algorithm. This approach allows to optimize for sources with a reduced sensitivity against deviations from the intentional polarization. Results obtained with the different optimization options are presented and discussed, specifically demonstrating the impact of pupil optimization on SMO. Moreover, the solution candidates are evaluated with respect to other criteria such as MEEF and NILS.

8326-19, Session 5

Convolution-variation separation theory for fast and rigorous first-principle modeling of optical lithography

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In this paper, we propose a method of convolution-variation separation (CVS) for fast and accurate modeling of optical lithography. For any particular combination of values for process variations and illumination variations, the proposed formulation is rigorously derived from first principles, and can be characterized by a series expansion comprising a plurality of predetermined basis functions weighted by a corresponding

plurality of expansion coefficients, where the predetermined basis functions are independent of the process variations, while the expansion coefficients depend only on the process variations. Due to the independency of the basis functions on process variations, the optical images under process variations can be calculated efficiently and accurately by merely changing the expansion coefficients weighting partial images that are computed and stored in advance. Simulations under various process conditions are presented and verified to demonstrate the proposed CVS method.

8326-20, Session 5

Application of illumination pupilgram control method with freeform illumination

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In this paper we present an illumination pupilgram re-adjustment method that can effectively control the various illumination parameters to recover optimum imaging performance as required by the lithography process.

The adjusting method uses pupilgram modulation functions that are similar to the Zernike polynomials used in wavefront aberration analysis for lithographic projection lenses to describe the optimal pupilgram adjustment in terms of OPE characteristics. The modulation functions are called Zernike intensity/distortion modulations. Since the pupilgram modulation is expressed by Zernike polynomials, a high degree of pupilgram adjustment freedom is provided to the intelligent illuminator (freeform illumination) which can be effectively modeled in the optimization.

The method is combined with an imaging simulator that includes resist models and optimization algorithms in a pupilgram refinement software. The software can take into account the scanner signature and various constraints so that the result of the optimization can be accurately realized on the scanner. The optimization can be performed based on rigorous imaging simulation and Zernike linear combination analysis, which is based on a pre-calculated Zernike linear sensitivity table. The user can select the optimization mode and image calculation to fit the objective of the pupilgram adjustment.

8326-21, Session 6

1.35 NA immersion lithography scanner evolution down to 1xnm nodes

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Mainstream high end lithography is currently focusing on 32 nm node and 22 nm node where 1.35 NA immersion technology is well established for the most critical layers. Double patterning and spacer patterning techniques have been developed and are widely being used to print most critical layers.

Further down the lithography roadmap we see the 1x nm nodes coming where EUV lithography will take over critical layers from immersion. In order to enable a smooth industry wide transition towards EUV, the 1.35 NA immersion technology will continue to play a critical role in manufacturing front end layers in the coming years. Using the immersion technology beyond the 22 nm node, we expect an increase in the use of double patterning technology for the critical layers. This demands for tighter control of overlay, focus and imaging performance on the 1.35 NA immersion tools. Also full flexible illumination and wave front control will be needed optimizing the contrast for these low k1 applications.

In this paper we will present the latest evolutions and results on 1.35 NA NXT immersion exposure systems. The latest overlay, focus, and contrast improvements will be shown to enable device shrink. Cost of ownership improvements will be shown by means of extending productivity and optimizing defect control by new immersion technology.

8326-22, Session 6

EUV and 193nm mix and match overlay optimization for critical layers

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In state of the art production, in order to obtain the best possible overlay performance between critical layers, wafers are often dedicated to one scanner. With the introduction of EUV scanners, not all critical layers will be exposed on an EUV scanner, so it needs to be demonstrated that the same overlay performance is achievable when tool types are mixed and matched as when we run with tool dedication. To do this it is critical that we understand the overlay matching characteristics of 193nm immersion and EUV scanners and from this learn how to control them, so that the optimum strategy can be developed and overlay errors between these tool types minimized.

In this work we look at the matching performance between two generations of 193nm immersion scanner and an EUV pre-production tool. We discuss the difference in grid and intrafield signatures between the tool types and how this knowledge can be used to minimize the overlay errors between them. Also discussed will be the alignment strategy used, dealing with direct versus indirect alignment, linear and high order alignment models and if there are any new concerns which impact the chosen strategy when the two tool types are mixed and matched.

8326-23, Session 6

Imaging optics setup and optimization on scanner for SMO generation process

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Source & Mask Optimization is a promising low-k1 technique to extend ArF immersion-lithography. However, imaging with such a small k1 factor is very sensitive to many imaging parameters, such as details of the illumination source shape, lens aberrations, process settings, etc. As a result, all imaging-related parameters should be closer to the designed parameters used in SMO process than before.

In this paper, we discuss how we realize this in the imaging system setup on the scanner. The setup process includes freeform pupilgram generation, pupilgram adjustment and thermal aberration control. For each step the important factors are speed, accuracy, and stability.

[Freeform pupilgram generation]

This step includes pupilgram prediction, pupilgram generation, pupilgram adjustment with the intelligent illuminator and stabilization of the generated pupilgram. For the prediction we use a pupilgram predictor algorithm, which predicts the pupilgram generated on scanner by using design information from the illumination system. Then the freeform pupilgram can be generated by Nikon's intelligent illuminator.

After initial pupilgram settings, pupilgram adjustment using pupilgram modulation functions, which are similar to Zernike polynomials, is performed.

[Thermal aberration prediction and control]

This step also starts with prediction. The thermal aberration during the wafer lot is predicted using modeled intensity distribution in the projection lens pupil. This modeled distribution is calculated by the illumination pupilgram and mask pattern spatial frequency distributions. Then, the thermal aberration is predicted using a fast thermal aberration analysis method. Finally, optimization of the thermal aberration control is performed based on the predicted thermal aberration.

8326-24, Session 6

Model-based OPC for implant layer patterning considering wafer topography proximity (W3D) effects

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Implant layer patterning is becoming challenging with node shrink due to decreasing critical dimension (CD) and usage of non-uniform reflective substrates.

Conventional OPC models are calibrated on a uniform silicon substrate which the model does not consider any effect from sub layer. So, the existing planar OPC model can't predict the sub layer effects such as reflection and scattering of light from substrate and non-uniform interfaces. For the 45nm and over nodes, that effect has been ignored or compensated using rule based OPC. However, when the node reached 40 nm and below, the sub layer effect causes undesired critical dimension (CD) variation and resists profile change.

It is necessary to model the wafer topography proximity effects accurately and compensate them by using a model based OPC. However, it may take a long time to calibrate rigorous model and compensate sub-layer effect using that model. In this paper, we demonstrate accurate and rapid method that aware topography effects by using kernel based model. We also demonstrate application of this model for full chip OPC on implant layers.

8326-25, Session 6

Implementation of reflectivity control on block mask lithography at 20 and 14nm nodes

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Block mask lithography has become extremely challenging due to a combination of resolution scaling and tolerance values, coupled with substrate topography from isolation and gate structures that have not been scaled. In fact, this topography has become more extreme with introduction of non-planar devices. Current applications may require advanced reflectivity control schemes in order to provide adequate device behavior and yield.

We will report our results on the optimization of antireflective materials for use on block masks at the 20 and 14 nm nodes, on isolation, gate, and finfet topography. Both KrF and ArF dBARC solutions have been systematically evaluated to compare the relative advantages of each option with respect to single layer process. This paper also addresses the unique challenges of different dBARC systems in patterning implementation. Our electrical results show that reflectivity control can provide significant enhancements to device behavior, with lithographic modeling data matching the observed experimental results.

8326-26, Session 6

Process window control using CDU master

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As double patterning techniques such as spacer double/quadruple patterning mature, ArF water immersion lithography is expected to be applied down to the 1x nm hp node or beyond. This will necessitate precise process control solutions to accommodate extremely small process windows.

Additionaly,in the case of an actual IC device, some critical patterns may not always be exposed with their optimum process condition. This is because the common process window, which includes other patterns such as some peripheral circuit or via contact pad, has to be considered.

In this paper, we will first discuss optimizing the common process window for multiple patterns using CDU Master, which is a CD uniformity compensation solution that was reported at SPIE 2010 [2]. By simultaneously compensating for dose/focus errors, CDU Master successfully maximizes the process window. We will also discuss CD uniformity stability. Dose and focus errors are separated into several components that have characteristic stability behavior. Therefore, correction using only the large characteristic errors is an effective solution that also reduces CD measurement time. This work will demonstrate how CDU Master successfully reduced the error by approximately 30% while using remarkably fewer measurement points.

8326-27, Session 7

The development of a fast physical photoresist model for OPE and SMO applications from an optical engineering perspective

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Photoresist models and simulators are routinely used in lithography process analysis, problem solving, predictive estimation, and optical proximity correction determination. Most models tend to fall into 3 categories: 1) a very simple model, such as a threshold model, with few parameters; 2) a pure physical model that can have an enormous number of variables; or 3) an approximate model for OPC that will have interacted parameters that are used more as tuning "knobs" rather than actual physical parameters.

From the viewpoint of an optical engineer, the chemical processes effecting the interaction of light with the photoresist are seen as overly difficult to comprehend, especially to the non-chemist. They appear to the un-initiated as "voodoo physics", attempting to describe all mechanisms that occur with the photoresist process. Simulation algorithms such as molecular development effects, higher order post exposure bake kinetics and exact photoresist sidewall calculations can often seem unnecessary and even computationally excessive, especially when much of the subsequent metrology concerns itself with critical dimension measurement and/or two-dimensional top down profiles. The optical engineer will often resort to using a category (1) simulation, which while being simple may result in less accuracy and a more restricted region of validity. Unfortunately, when using advanced optimization techniques needed for optical proximity effect (OPE) matching and source mask optimization (SMO), even small errors in simulation accuracy are often unacceptable.

This work will describe a new photoresist imaging model and simulations that retain the fundamental physical and chemical properties of optical exposure, post-exposure bake and development. We apply dimensional reduction algorithms that reduce the imaging aspects of the problem, but preserve the imaging and thin film physics. This has the effect of simplifying the overall model and increasing the computational speed, while retaining an extremely accurate predictive capability. The model, named the RoadRunner Model, gives more detail and parameter intuition than a basic threshold model and agrees well with full photoresist simulation. The model is easily adapted into OPE analysis and source-mask optimization.

We demonstrate the accuracy of this new model by experimental verification using one-dimensional and two-dimensional features through a pitch range on a Nikon immersion scanner. We show that the model can be extrapolated to multiple illumination source shapes. Specifically,

the use of the model is examined for analysis of OPE and compared to more traditional simulators. An example of this is shown in figure 1 where a comparison is made of the RoadRunner model to a full photoresist simulation.

Finally, we will discuss the range of applicability of the model and its use in applications such line wide roughness analysis and EUV imaging. We will present an adaption of the model to incorporate relevant stochastic processes.

8326-28, Session 7

Simulation study of LWR bounding of depth of focus of various lithographic techniques: interference, optical projection, EUV, e-beam and hybrid complementary lithography, and proposal for a new production interference tool

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Interference lithography (IL) using coherent two-beam imaging generates image contrast neighboring in the 98% range in low flare, vibration mitigated systems. If system flare is maintained less than 6% then LWR is nearly 1 nm less than that of the next best imaging technique, dipole projection lithography and this is true over its entire dipole processing windows; but with less dependence on focus IL's capability extends well past that window too. This work shows that at a 76 nm pitch LWR of interference lithography potentially achieves the 2.5 nm ITRS limit, which when used in sidewall quadruple patterning or directed self-assembly allows 19 nm pitch processing with water. This work maps LWR to image contrast using LER parameterized resist models that are imaged using interference lithography, dipole projection printing and EUV and we also compare these results to literature results for all including e-beam (literature only). The contrast is varied in four ways: 1. By unbalancing the electric field between the two interfering beams. 2. By varying flare. 3. By defocus. 4. By pole size. To check these models we show for 193 nm imaging regardless of the way contrast is varied the LWR exhibits the same image contrast dependence for interference and projection lithography. Then we use this information to provide insight into imaging system extendibility and performance specifications. This work also shows how projection, direct-write and EUV imaging technologies can benefit from interference lithography with throughput enhancements from 2X to 20X and, arguably, with less LWR.

8326-35, Session 7

The Saga of Lambda: spectral influences throughout lithography generations

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No abstract available

8326-36, Session 7

LER: the ultimate limiter for resolution in production?

C. A. Mack, Lithoguru.com (United States)

No abstract available

8326-29, Session 8

High-overlay accuracy for double patterning using an immersion scanner

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Double patterning (DP) is widely regarded as the lithography solution for 32 nm half pitch semiconductor manufacturing, and DP will be the most likely litho technology for the 22 nm node. When using the spacer DP technique, overlay accuracy and CD control are of critical importance.

We previously introduced the NSR-S620D immersion scanner, which provides 2 nm overlay capabilities. In the case of the latest generation NSR-S621D system, improvements to the encoders have been developed for further overlay accuracy enhancement.

When considering overlay on product wafers, the interaction between the different machines (Mix-and-Match capabilities) contributes additional errors beyond single machine overlay. For the NSR-S621D, optimal total overlay accuracy for DP is obtained using high order grid compensation and high order distortion compensation by shot, as well as high order reticle expansion compensation techniques, etc.

In addition, alignment mark detection accuracy also greatly influences product process overlay. For spacer DP, because the alignment mark is composed of a detailed segmented mark, detection can become challenging for the alignment sensor. However, these difficulties can be successfully overcome by optimizing the optical condition of the alignment sensor and the algorithm condition used for signal processing.

In this paper, we will show the overlay accuracy and Mix-and-Match performance of the NSR-S621D. Further, the marked improvement in product overlay as a result of enhanced alignment accuracy will also be shown.

8326-30, Session 8

Modeling for field-to-field overlay control

K. D'havé, IMEC (Belgium)

The tightening of overlay budgets forces us to revisit the characterization and control of exposure tools to eliminate remaining systematic errors.

Even though field-to-field overlay has been a known characterization and control technique for quite some time [1], there is still room to further explore and exploit the technique. In particular, it can be used to characterize systematic errors in a scanner's dynamic exposure behavior [2].

In this paper we investigate the modeling of field-to-field overlay starting from a scanner point of view. From a set of general equations we show how systematic dynamic differences between up and down scanned fields can be extracted from field-to-field overlay measurements. The model separates combined static effects, such as reticle error and clamping, from dynamic effects. We point out how apparent static effects may have a dynamic cause. Finally we demonstrate the use of the model in an experiment wherein the scan speed dependent dynamic behavior is characterized for an immersion scanner.

8326-31, Session 8

Free form source and mask optimization for negative-tone resist development for 22nm node contact holes

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Contact hole patterning in general has been one of the most challenging patterning features in semiconductor device manufacturing, due to the low contrast and smaller process windows. The current positive tone ArF immersion resist single exposure process is only capable of printing contact hole for the 32nm node with an Attenuated PSM mask. Extreme ultra-violet (EUV) lithography is currently not ready for High Volume Manufacturing (HVM) at the 22nm node due to the challenges in developing the needed EUV source, defect free masks, and high sensitivity resists. Another alternative solution is Litho-Etch-Litho-Etch (LELE) double patterning. But it is more economical to explore a single exposure process. It is natural to extend 193nm immersion lithography with single exposure, bright field mask with Source and Mask Image enhancement techniques leveraging a Negative Tone Development (NTD) process as a bridging technology for the 22nm node and below before EUV is available for HVM.

In this paper we demonstrate the feasibility of NTD process to pattern the 22nm node contact holes leveraging a freeform source and model based assistant feature methodology. We demonstrate this combined technology with detailed simulation and wafer results. This analysis also includes further improvement achievable using a freeform source compared to a conventional standard source while keeping the mask optimization approaches the same. Similar studies are performed using the Positive Tone Development (PTD) to demonstrate the benefits of the NTD process.

8326-32, Session 8

Process development using negative tone development for the dark field critical layers in a 28nm node process

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The demand for ever shrinking semiconductor devices is driving efforts to reduce pattern dimensions in semiconductor lithography. In this work, the aim is to find a single patterning litho solution for a 28nm technology node using 193nm immersion lithography. Target poly pitch is 110nm and Metal1 pitch is 90nm. For this, we have applied a range of techniques to reach this goal. At this node, it becomes essential to include the layout itself into the optimization process. This leads to the introduction of restricted design rules and the use of intermediate metal (IM) layers to connect the front-end and back-end-of-line. At the same time, co-optimization of source and mask (SMO) and the use of customized illumination modes are employed.

Traditionally, the printing of contacts and trenches is done by using a dark field mask in combination with a positive tone resist and positive tone development. The use of negative tone development enables images reversal. This allows benefiting from the improved imaging performance when exposing with bright field masks. The same features can be printed in positive resists and with much improved process latitudes.

In this study, we explore the use of negative tone development, and successfully demonstrate its use for the various dark field critical layers in a 28nm node process. In order to obtain sufficiently large process windows, structures are printed larger than the design target CD. Subsequently, a shrink of the structures needs to be applied to obtain the target CD after etch. Final results on wafer will be discussed, focusing on critical layers as IM1, IM2, Via0 and Metal1.

8326-33, Session 8

Process requirements for splitting pitch LELE double-patterning technique at advanced logic technology nodes

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The discussions on controlling laser spectrum effects to reduce circuit CD variation for the 32nm node and beyond have been made in our previous work. Circuit CD variations were calculated by a photolithography simulator with consideration of laser spectrum effects under optical single exposure conditions. As IC dimensions continue to shrink beyond the 22nm node, optical single exposure can not sustain the resolution required and various double patterning techniques have become the main stream prior to the availability of EUV lithography. Among various kinds of double patterning techniques, splitting pitch lithography-etch-lithography-etch (LELE) double patterning is chosen for printing complex foundry circuit designs. Tighter circuit CD and process margin control in such splitting pitch LELE double patterning process becomes increasingly critical especially for topography issues induced by the 1st mask patterning with the 2nd mask exposure during this splitting pitch LELE double patterning processes. Source-Mask Optimization (SMO) is then widely adopted to improve the process margin under such a small geometry, however, different SMO may generate different CD sensitivities from various sources of error, including contrast variations and laser bandwidth. In this paper, laser parameters, topography issues with the 2nd mask exposure, and SMO effects on CD performances are described in terms of the proximity CD portion of the scanner CD budget. Laser parameters, e.g. spectral shape and bandwidth, were input into the photolithography simulator, Prolith, to calculate their impacts on circuit CD variation. Mask-bias dependent lithographic performance was calculated and used to illustrate the importance of well-controlled laser performance parameters. Stable through-pitch proximity behavior was one of the critical topics for foundry products, and also is described in the paper. Recommended laser parameter, topography and SMO requirements are proposed, based on simulation results to ensure that the tight CD control (< 1nm) required for advanced technology node products can be achieved.

8326-34, Session 9

Scanning interference evanescent-wave lithography for sub-22nm generations

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Current assumptions for the limits of water immersion optical lithography include NA values close 1.35, largely based on lack of materials with indices above those of water and fused silica. We have been working with high-NA static evanescent wave lithography (EWL) where the NA of the projection system is allowed to exceed the corresponding acceptance angle of one or more materials of the system. This approach is made possible by frustrating the total internal reflection (TIR) induced evanescent field into propagation. With photoresist as the frustrating media, the allowable gap for adequate exposure latitude is in the sub-100 nm range and increases with the use of higher index gap fluids. We have demonstrated the ability to resolve 26 nm half-pitch features at 193 nm and 1.85 NA using conventional resist, interferometric imaging, and commercially available sapphire optical materials. Through double patterning, such imaging could lead to the attainment of 13 nm half-pitch.

In this paper, we report progress in developing a flying EWL imaging head with a two-stage gap control system including a DC noise canceling carrying air-bearing pad that flies at a constant air gap with regulated air pressure, and a AC noise canceling piezoelectric transducer with real-time closed-loop feedback from gap detection. Various design aspects of the system including gap detection, prism design and alignment, software integration, feedback actuation and scanning scheme have been carefully considered to ensure sub-100 nm gapping. To date, preliminary results showed successful gap gauging at sub-100 nm with gap noise RMS around 2.3 nm in static gapping and 3.5 nm in linear scanning gapping. We also demonstrate both static and scanning imaging results with NA comparable to previously reported values of 1.4 for fused silica prism and 1.8 for sapphire prism. Our gapping and imaging results confirmed the promise of scanning EWL to extend optical lithography to sub-22 nm generations.

8326-35, Session 9

Using a numerical aperture of 1.85 to image high-aspect ratio structures in photoresist

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Imaging at ultra-high numerical apertures (NAs) using near-field techniques severely limits the aspect ratio of the printed pattern due to exponential decay of evanescent waves. We show how reflection resonances from an underlying effective gain medium (EGM) significantly enhances evanescent fields allowing fabrication of high aspect ratio (2.8) structures at NAs close to 1.85 with industry-standard λ=193 nm using TE polarization.

Previously we presented SILMIL (Solid Immersion Lloyds Mirror Interferometric Lithography) to produce ultra-high-NA features. We have successfully used SILMIL as an evanescent interference lithography test-bed to achieve large area (>100 microns) gratings with NAs as high as 1.824 (half-pitch 55nm or λ/7.3) at λ = 405 nm having 60 nm depth.

We also proposed that surface states on metals enhance evanescent fields with TM polarization. Upon theoretical investigation, we find this enhancement is also possible with TE polarization (good polarization in lithography) and other materials supporting surface states.

One example is an EGM, which we implement using a high-index dielectric on a low-index dielectric. This acts as an underlying energy bank/pseudo-source. The thickness of the high index dielectric is chosen to resonate the evanescent field. We provide a design example at λ = 193 nm to pattern NA = 1.85 (26 nm half-pitch) structures with aspect ratio of 2.8. The EGM is a 142-nm layer of Al2O3 sputtered upon SiO2.

We have also discovered that, provided the solid immersion prism material is available, the aforementioned technique may be used to pattern any NA with an aspect ratio of 1.3.

8326-36, Session 9

Doubling the spatial frequency with cavity resonance lithography

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We describe the theory and the first experimental demonstration of Cavity Resonance Lithography (CRL); a double pattering (DP) technique that can pattern 1) twice the spatial frequency of the lithography mask, and 2) at large offset distance.

CRL utilizes wave interferences and field resonances within an optical cavity formed by the mask and the substrate (with PR and immersion fluid being the dielectric medium of the cavity) to create spatially doubled sub-diffraction limited patterns in the farfield. The mask pattern is a periodic grating whose pitch is designed such that only the 0th and the 1st order (+1 and -1) diffracted waves propagate to far field while higher order waves are evanescent and decay away in the nearfield. The first order diffracted waves pass through a thin metal layer (a cavity mirror) and enter the cavity. Their planar wave vectors (kx) have the same periodicity as the mask gratings (kp), and the interference of the waves traveling in opposite directions (k(x) and k(-x)) generates field patterns with twice the spatial frequency (2kp) of the mask gratings.

Because CRL utilizes the propagating - rather than the evanescent - portion of the diffracted waves, the doubled patterns are not restricted to the near field but enables lithography with a large off-set distance. CRL requires only single exposure and development step with no need for additional processes. It is also possible to combine CRL with other double patterning techniques for quadrupling of the spatial frequency.

With commercially available photoresists (PR) and developers, we have recorded a 32.5 nm half-pitch pattern (well below the diffraction limit) at the distance of 180 nm (well beyond the evanescent decay length) using 193 nm illumination. We also discuss strategies to improve the minimum feature size and potential implementation schemes.

8326-37, Session 9

Pupil wavefront manipulation for optical nanolithography

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As semiconductor lithography is pushed to smaller dimensions, the process yields tend to suffer due to sub-wavelength topographical imaging effects. In response, resolution enhancement technologies have been employed together with optimization techniques, specifically source mask optimization (SMO). However, SMO has a limitation in that it fails to compensate for undesired phase effects. For mask features on the order of the wavelength, the topography of the mask can influence its diffraction field which causes phenomena such as a pitch dependent best focus and ultimately decreases the process window. In this work, wavefront phase correction is achieved by optimizing the spherical aberration coefficient in the lens pupil plane, which balances the spherical aberration induced by the mask. Simulations show that primary spherical aberration can improve the depth of focus for an alternating phase shift mask (PSM), and decrease the best focus deviation for a binary and an attenuated PSM. Experimental data with a binary and an attenuated PSM are presented, showing the characteristic decrease in best focus deviation.

8326-38, Session 9

14nm M1 triple patterning

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With 20nm production becoming a reality, research has started to focus on the technology needs for 14nm. The LELE double patterning used in 20nm production will not be able to resolve M1 for 14nm. Main competing enabling technologies for the 14nm M1 are SADP, EUV, and LELELE (referred as LELELE in the future) triple patterning.

SADP has a number of concerns of 1. density, as a layout geometry needs to stay complete as a whole, and can not be broken; 2. the complexity in SADP mask generation and debug feedback to designers; 3. the subtraction nature of the trim mask further complicates OPC and yield. While EUV does not share those concerns, it faces significant challenges on the manufacturing equipment side.

Of the SADP concerns, LELELE only shares that of complexity involved in mask generation and intuitive debug feedback mechanism. It does not require a layout geometry to stay as a whole, and it benefits from the affinity to LELE which is being deployed for 20nm production. From a process point of view, this benefit from affinity to LELE is tremendous due to the data and knowledge that have been collected and will be coming from the LELE deployment.

In this paper we first recount the computational complexity difference between that of a LELE decomposition algorithm and that of LELELE decomposition algorithm. Then we describe an algorithm that, though in the worst case runs in exponential time, can be quite efficient when layous satisfy certain conditions. We further outline a set of restricted design rules which we feel are not overly restrictive and will make LELELE design tractable. Last, we explore some of the options for LELELE debug feedback mechanism, and conclude with experimental data.

8326-11, Poster Session

Modelling of side-wall angle for optical proximity correction for self-aligned double patterning

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SADP decomposes the design into two different masks: the core mask and the trim mask. The core mask will be exposed to give a mandrel on which sides will be deposited a spacer. After removal of the mandrel, the trim mask will be exposed to give the original design with the help of the spacer pattern.

From process side, SADP is considered as one of the most credible solution for sub-20nm nodes due to its better process tolerance and lower overlay problem.

As spacer width defines the minimum dimensions of the design, it is necessary to exert a tight control on it. The spacer material is being deposited on the sides of the mandrel. Thus the Side-Wall-Angle (SWA) of the mandrel will have a strong impact on the final width as well as on the robustness of the spacer pattern.

The SWA is pattern-dependant: it is more critical in 2D patterns containing corners, or on line-ends. A SWA model has been developed, enabling prediction of mandrel resist profile. This allows tighter control of Critical Dimension (CD) by Optical Proximity Correction (OPC) for sub-20nm technological nodes.

In this study, we propose to calibrate a SWA model based on AFM measurements on 1D and 2D patterns, and to correlate it to the final spacer width. We will then study the influence of OPC techniques on the SWA, and propose some solution in order to achieve better process control on the CD of the design using SADP technique.

8326-55, Poster Session

New methodology to predict pattern collapse for 14nm and beyond

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Critical aspect ratio induced pattern collapse has been a concern for lithography process engineers since before the 180 nm node. This line bending can lead to pattern deformation or complete substrate adhesion failure. Several process improvements, such as surfactant-laced final rinse, have been proposed to alter surface energies and increase the critical aspect ratio for collapse. The challenge is more severe for sub-60 nm pitch ground-rules that are being developed for the 14 nm technology node, since 30nm and smaller spaces will produce extremely large capillary forces acting on very narrow resist patterns. In previous studies (see Ref. [1-3] for example), an analytical model was used to predict pattern collapse of simplified line/space structures. In this work, we propose a new framework to predict pattern collapse of sub-60 nm pitch EUV resist structures by the use of a semi-empirical model. This semi-empirical model is derived from the one-dimensional analytical model, which includes a term dependent on the local pattern geometry and the physical properties of the resist and rinse solution. We calibrate/verify the model with various EUV pattern collapse data collected from one-dimensional (e.g., line/space) patterns. Hotspots predicted by the semi-empirical model are compared with those obtained from EUV wafer exposures. Weaknesses in model prediction were then used to adjust the model terms. Determining pattern collapse and identifying hot-spots early in the development cycle is critical for setting restricted design rules and refining DFM/RET solutions.

8326-56, Poster Session

Building 3D aerial image in photoresist with reconstructed mask image acquired with optical microscope

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Calibration of mask images on wafer becomes more important as features shrink. Two major type of metrology have been commonly

adopted. One is to measure the mask image with SEM to obtain the contours on mask. The other is to use an optical imaging tool AIMS to emulate the image on wafer. However, the SEM method is indirect. It just gathers planar contours on a mask with no consideration of optical characteristics such as 3D topography structures. Hence, the image on wafer is not predicted precisely. Though the AIMS method is able to directly measure the intensity at the near field of a mask but the image measured this way is not quite the same as that on the wafer due reflections and refractions in the films on wafer.

Here, a new approach is proposed to emulate the image on wafer more precisely. The behavior of plane waves with different oblique angles is well known inside and between planar film stacks. In an optical microscope imaging system, plane waves can be extracted from the pupil plane with a coherent point source of illumination. Once plane waves with a specific coherent illumination are analyzed, the partially coherent component of waves could be reconstructed with a proper transfer function, which includes lens aberration, polarization, reflection and refraction in films. It is a new method that we can transfer near light field of a mask into an image on wafer without the disadvantages of indirect SEM measurement, losing effects of mask topography, and neglecting reflections and refractions in the wafer film stacks. Furthermore, with this precise latent image, a separated resist model also becomes more achievable.

An algorithm is shown to reconstruct the mask image in photoresist, whose comparison with wafer CD will be discussed.

8326-57, Poster Session

Proximity diffraction correction for generating three-dimensional structures using graded-tone mask lithography

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For specialty analog or mixed-signal devices, three-dimensional (3D) structures on a single layer often appear. One might realize such structures by applying straightforward multiple patterning processes. Alternatively, one might merge the multiple patterning processes into single one by utilizing graded-tone mask lithography to achieve well-aligned 3D structures and cost-effective process flow at the same time. However, the graded-tone mask, consist of sub-resolution patterns with density modulation coincide with target intensity profile, have been adopted for limited applications such as a large-sized (> 100 um) single feature or small-sized (1-2 um) repeated features due to design complexity of a mixed-tone mask containing sub-resolution patterns for arbitrary graded-tone features and conventional non-graded-tone features in a single mask.

In this presentation, we study resist profile for a 3D structure in a simplified mixed-tone mask consists of alternating graded-tone micro-lens features and neighboring large pads in a checker board configuration. We found cross sectional resist profile of the graded-tone micro-lens deformed seriously in the mixed-tone mask. Intensity profile simulations show the same profile deformation, indicating profile degradation due to proximity diffraction onto graded-tone feature from neighboring non-graded-tone large pad. By simulating series of proximity diffraction corrections for neighboring pads, we propose a method to realize mixed-tone mask for arbitrary features without degrading graded-tone features. Experimental resist profiles for the simplified mixed-tone mask confirm that the method corrects the proximity diffraction and remedies the resist profile deformation effectively.

8326-58, Poster Session

Wafer CD variation for randomly correlated track units and polarization

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After wafer processing in a scanner the process of record (POR) flows in a photo track are characterized by a random correlation between post exposure bake (PEB) and development (DEV) units of the photo track. The variation of the critical dimensions (CD) of the randomly correlated units used for PEB and DEV should be as small as possible - especially for technology nodes of 28nm and below. Even a point-to-point error of only 1nm could affect the final product yield results due to the relatively narrow process window of 28nm tech-node. The correlation between reticle measurements to target (MTT) and wafer MTT may in addition be influenced by the random correlation between units used for PEB and DEV. The polarization of the light source of the scanner is one of the key points for the wafer CD performance too - especially for the critical dimensions uniformity (CDU) performance.

We have investigated two track flows, one with fixed and one with random unit correlation. The reticle used for the experiments is a 28nm active layer sample reticle. The POR track flow after wafer process in the scanner is characterized by a random correlation between PEB- and DEV-units. The set-up of the engineering (ENG) process flow is characterized by a fixed unit correlation between PEB- and development-units. The critical dimension trough pitch (CDTP) and linearity performance is demonstrated; also the line-end performance for two dimensional (2D) structures is shown. The sub-die of intra-field CDU for isolated and dense structures is discussed as well as the wafer intra-field CD performance. The correlation between reticle MTT and wafer intra-field MTT is demonstrated for track POR and ENG processes. For different polarization conditions of the scanner source, the comparison of CDU for isolated and dense features has been shown. The dependency of the wafer intra-field MTT with respect to different polarization settings of the light source is discussed. The correlation between reticle MTT and wafer intra-field MTT is shown for ENG process without polarization. The influence of different exposure conditions - with and without polarization of scanner laser source - on the average CD value for isolated and dense structures is demonstrated.

8326-59, Poster Session

Field performance availability improvements in lithography light sources using the iGLX gas management system

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At high-utilization lithography sites, laser light source gas replenishments and gas maintenance operations typically require between 9 and 16 hours per year, during which the light source is unavailable for production. Reducing this downtime is important for increasing the productivity of the lithography cell. Finally, light sources sometimes require intermittent gas maintenance that must be performed manually and therefore can be subject to variability in duration and repeatability.

This paper will outline the targeted improvements in availability experienced by equipping the light source with Cymer's iGLX Gas Management system. The iGLX System extends the shot-based interval between gas refills to 4 Billion pulses for Cymer's XLA and XLR light sources, while maintaining existing laser performance. Additionally, the iGLX System automates some gas maintenance events that were previously manual, improving their speed and reducing their variability. We will provide some performance data during extended light source operation on litho cells equipped with the iGLX System.

For high-utilization litho cells, the iGLX System can reduce gas maintenance related downtime by up to 75%, increasing light source availability up to 12 hours per year. Total halogen gas usage can also be reduced by up to 4%, and manual gas maintenance events can be eliminated.

The iGLX System has been installed on multiple high-volume scanner systems, which experienced these improvements immediately, and are continuing to operate nominally. As the iGLX System is deployed in volume, additional availability improvements can be realized by more readily synchronizing other lithography line maintenance events with the gas replenishment and maintenance events.

8326-60, Poster Session

Can fast rule-based assist feature generation in random-logic contact layout provide sufficient process window?

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A two-step full-chip simulation method for optimization of sub-resolution assist feature placement in a random logic Contact layer using ArF immersion Lithography is presented. Process window, characterized by depth of focus (DOF) , of square or rectangular target features is subject to optimization using the optical and resist effects described by calibrated models (Calibre nmOPC, nmSRAF simulation platform). By variation of the assist feature dimension and their distance to main feature in a test pattern, a set of comprehensive rules is derived which is applied to generate raw assist features in a random logic layout. Concurrently with the generation of the OPC shapes for the main features, the raw assist feature become modified to maximize process window and to ensure non-printability of the assist features. In this paper, the selection of a test pattern, the generation of a set of "golden" rules of the raw assist feature generation and their implementation as well as the assist feature coverage in a random logic layout is presented and discussed with respect to performance.

8326-61, Poster Session

ZERODUR®: bending strength data for tensile stress loaded support structures

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In the past ZERODUR® was mainly used for mirror and substrate applications, where mechanical loads were given by its own weight. Nowadays substrates become more sophisticated and subject to higher stresses as consequences of high operational accelerations or vibrations. The integrity of structures such as reticle and wafer stages e.g. must be guaranteed with low failure probability over their full intended life time. Their design requires statistically relevant strength data and information.

The usual way determining the design strength employs statistical Weibull distributions obtained from a set of experimental data extrapolating the results to low acceptable failure probability values. However, in many cases this led to allowable stress values too low for the intended application. Moreover, the experimental basis has been found to be too small for reliable calculations.

For these reasons measurement series on the strength of ZERODUR® have been performed with different surface conditions employing a standardized ring-on-ring test setup. The numbers of specimens per sample have been extended from about 20 to 100 or even much more. The results for surfaces ground with different diamond grain sizes D151, D64 and D25 as well as for etched surfaces are presented in this paper.

Glass ceramics like all glassy materials exhibit some strength reduction when being exposed to loads above a tensile stress threshold over long time periods. The strength change of ZERODUR with time will be discussed on the basis of known and newly determined stress corrosion data.

The results for samples with large numbers of specimens contribute new

aspects to the common practice of extrapolation to low failure probability, since they provide evidence for the existence of minimum strength values depending on the structures surface conditions. For ground surfaces the evidence for minimum strength values is quite obvious. For etched surfaces minimum values are to be expected also. However, here closer observation is still needed. The systematic deviations from Weibull distributions lie below about 5 % failure probability and thus could not be seen in small samples as they were common in the past.

8326-62, Poster Session

OPC model prediction capability improvements by accounting for mask 3D-EMF effects

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As mask feature sizes have shrunk well below the exposure wavelength, the thin mask of Kirchhoff approximation breaks down and 3D mask effects contribute significantly to the through-focus CD behavior of specific features. While full-chip rigorous 3D mask modeling is not computationally feasible, approximate simulation methods do enable the 3D mask effects to be represented. The use of such approximations improves model prediction capability. This paper will look at a 28nm metal layer dataset that was calibrated with a Kirchhoff model and with two different 3D-EMF models. Both model calibration accuracy and verification fitness improvements are realized with the use of 3D models. In addition, the role of variable optical diameter and sum of coherent systems (SOCS) kernels is explored.

8326-63, Poster Session

Defects reduction at BEOL interconnect within 300mm manufacturing environment

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Process yield is a critical factor for a success of 300mm manufacturing. Typically, higher yield corresponds to lower defect counts within the respective processing steps (lithography, etch, plating, and CMP). Within BEOL lithographic processes, there are issues of defects within same lithographic technology and there are concerns of defects between generations of lithographic technologies, for example, immersion, 193nm "dry", and DUV (248nm). In order to have an effective defect reduction strategy, defects have to be monitored, identified, and analyzed for points of origins. In this paper, we explore three areas of interests in the BEOL: 1) defects occur between different processing steps, specifically, after Immersion Lithography, after Reactive Ion Etch (RIE), and after Chemical Mechanical Polish (CMP), 2) defects after CMP between lithographic technologies (Immersion, Dry, and DUV), and finally 3) defects between different devices. We were able to find evidence of transferable processing defects.

8326-64, Poster Session

CD signature monitoring based on AMAI sensor measurements

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Lens aberrations are a major source of across-chip linewidth variation at low k1, and need to be carefully balanced and monitored in a lithographic exposure tool. Tools without an in-situ interferometer have little capability

to measure Zernike aberrations of a lens with enough accuracy and speed to be used for in-line aberration control. A method to predict across-chip CD profile directly from AMAI sensor measurements proves to be more useful than Zernike-based methods. The measured AMAI sensor data typically relates to a combination of Zernike coefficients, as this sensor only provides data in one lateral dimension. Attempts to calculate individual Zernike coefficients are hampered by a strong correlation between members of the same aberration group, for example low- and high-order comas. However, when the goal is to predict CD signature of another one-dimensional feature, it is possible to establish a more direct equation with a streamlined correlation matrix. Using a principal components-based analysis of both AMAI and wafer image formation process, we create a conversion matrix that allows prediction of feature CD directly from the sensor measurements. We carry out experiments comparing CD profile predictions to CD-SEM measurements on 150 nm features exposed on two different tools. Features of the same linesizes are exposed on both an ArF tool and a KrF tool, with different aberration levels. The results are compared with predictions, and are found to have a closer relationship than those calculated using Zernike measurement approach. We propose that direct CD calculation method is thus better suited for image quality monitoring and control.

8326-65, Poster Session

Edge placement error reduction and ringing effect suppression using model-based targeting techniques

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For 32nm and 20nm nodes strong off axis illumination and double patterning are seen as the preferred imaging techniques. Strong off axis illumination is associated with contour ringing effects on 2D patterns which can lead to oscillations that extend for up to a micron along nominally straight edges. Not only must these stronger and less predictable oscillations be controlled but the allowed edge placement variation continues to scale with design rules even if double patterning allows printed dimensions to be kept constant. Both of these methodologies demand increasing performance from the OPC recipe in terms of reducing edge placement errors. While restricted design rules may include orientation preferences and thus help to reduce these effects, Metal 1 logic standard cells with double patterning still require 2D layouts to achieve good density. Optical proximity correction recipes have traditionally relied on using just one target point for each correctable segment. The lateral placement of these target points within a segment are determined by rules based on the local design geometry. Poor placement can result in degradation of CD control and even pinching or bridging. Correct placement especially on vertex segments can remarkably reduce these issues. As neighboring shapes have increasing influence over patterning, these rules become increasingly complex, with the large variety of layout combinations possible, the targeting rule set becomes unmanageable and a move to model based targeting becomes inevitable. Various model based targeting approaches will be briefly discussed. To resolve the long range oscillation effects, an in-recipe simulation of these contours far from the corner or line-end vertices is essential. This paper therefore concentrates in particular on the implementation of an Edge Placement Error extrema based target point placement methodology, which showed encouraging results. An analysis of issues seen during development and how they were resolved will be presented. For instance the optimal placement of target points for vertex segments was seen as critical to damping long range oscillations farther out. A few different methodologies for doing this are discussed and compared. Results from test structures specifically designed to be sensitive to long range ringing will be presented. Improvements will also be presented due to smarter target point placement for shorter edges. These come from a variety of test patterns with irregular 2D layouts where target point placement rules are difficult to define well. This suggests such model based targeting techniques may be generally beneficial in OPC correction and not just for strong off axis illumination.

8326-66, Poster Session

Source Mask Optimization Methodology (SMO) & Application to Real Full Chip Optical Proximity Correction

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Due to the continuous shrinking in half pitch and critical dimension (CD) in wafer processing, maintaining a reasonable process window such as depth of focus (DOF) & exposure latitude (EL) becomes very challenging. With the source mask optimization (SMO) methodology, lithography process window can be improved and smaller mask error enhancement factor (MEEF) can be achieved.

In this paper, the optimized SMO work flow (as shown in figure. 1) is used and the SMO methodology to optimize the illumination source is evaluated. The optimum source is achieved through evaluation of the critical designs with Tachyon SMO software and the simulated performance is then verified on another test case. Criteria such as DOF, EL & MEEF are used to determine the optimum source achieved from the evaluation. Furthermore, the process variation band (PV-Band) and the number of hot spot (design weak points) are compared between the baseline and the optimum source. The simulation result shows the DOF, MEEF & worst PV-Band are improved by 20%, 17% & 12%, respectively with the optimum SMO source.

In order to verify the improvement from optimum SMO on the silicon level, a new OPC model is recalibrated with wafer CD from the optimized source. OPC recipe is also optimized and a reticle is retrofitted with the new OPC. By comparing the process window, hotspots and defects between the original vs. new reticle, the benefit of the optimized source is verified on silicon.

8326-67, Poster Session

Source optimization incorporating margin image average with conjugate gradient method

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As Moore's law marches on and semiconductor manufacturers make the push towards the 20nm technology node and beyond, the challenges faced by optical lithography are ever increasing. The need to print such small features using 193nm illumination -- which is way beyond the Rayleigh diffraction limit -- has made resolution enhancement techniques (RETs) mandatory to improve lithography performance including pattern fidelity, process window (PW), edge-placement error (EPE) and image contrast.

Mask correction are the most widely used RETs due to the cost and hardware flexibility. In current state-of-the-art mask modification techniques, inverse lithography (IL), which inverse calculates the optimal mask configurations, provide the theoretical free type mask patterns. Nevertheless, the shrinking CDs and highly dense configures of drawn mask, ex : Dynamically Random Access Memory (DRAM), limit the correction space of IL. Thus in advance lithography generation, not only mask optimization (MO) but also source optimization (SO) should be considered into the standard lithography flow. Actually the SO can be seen as another inverse technique for resolution enhancement like IL. All algorithms used in IL can be applied to SO and have similar thorny issues such as local minimum trap and slow convergence.

Therefore, free form source optimizations for sub-wavelength corrected mask are recently attached great importance by lithographers as lithography node still progressing. Image formations via source integration can be seen as a linear system. However, the sigmoid function widely used to convert aerial image to resist image is a nonlinear operation. The linearity is loss when resist images are considered in cost function. In this paper, we propose a cost function incorporating margin image average to simulate the resist performance without nonlinear conversion. Such operation masks our optimal calculation in image space and stay with linearity. Therefore the cost can be presented as a quadratic form where the local minimizer is also global minimizer. Moreover the conjugate gradient descent algorithm is exploited to guarantee the global minimizer to be found at most iterations equal to source variable numbers. We also demonstrate the optimal source by using sigmoid conversion with steepest descent and have near results.

8326-68, Poster Session

Integration of pattern matching into verification flows

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The OPC verification problems tend to get more complicated in terms of coding complexity and TAT (turnaround time) increase as the gate length get smaller. A well known example of coding complexity is waivers (OPC verification errors that are priory known to be safe on silicon) detection and elimination. Potential locations for hot spots extraction as well could be a time consuming process if executed on full chips. And finally, OPC verification flows run time is sometimes even larger than OPC runs.

In this work, we introduce the use of pattern matching as a potential solution for many verification flows problems. Pattern matching offers a great TAT advantage since it is a DRC based process, thus it is much faster than time consuming LITHO operations. Also, its capability to match geometries directly and operating on many layers simultaneously eliminates complex SVRF coding from our flows. Firstly, we will use the pattern matching in order not to run OPC verification on basic designs identified by the OPC engineer to be error free, which is a very useful technique especially in Memory designs and improves the run time. Then, it will be used to detect waivers, which is hard to code, while running verification flows and eliminate it from the output, and consequently the reviewer will not be distracted by it and concentrate on real errors. And finally, it will be used to detect hot spots in a separate very quick run before standard LITHO verification run which gives the designer/OPC engineer the opportunity to fix design/OPC issues without waiting for lengthy verification flows, and that in turns further improves TAT.

8326-69, Poster Session

Advanced mask aligner lithography (AMALITH)

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Projection lithography pushed mask aligner lithography out of semiconductor front-end in the early 1980s. However, mask aligner technology was never phased-out. The installed mask aligners remained in operation for less critical layers. Back-end, advanced packaging, MEMS, TSV, and - most recently the very cost-sensitive LED manufacturing - maintained a continuous demand for some hundreds of new mask aligners installed every year in industry. Mature technology, high throughput, ease of operation, low maintenance, moderate capital costs and attractive cost-of-ownership are the key factors. Since the 1980s, these mask aligners have much evolved from the manual 4" aligner to the fully automatic 300mm cluster systems of today. Interestingly, the shadow-printing lithography process itself was never improved.

Inspired by pupil-shaping methods for DUV steppers, we have recently introduced a novel mask aligner illumination system, referred as MO Exposure Optics (MOEO). The MO Exposure Optics system is based on high-quality micro-optical homogenizers (Kohler integrators) for light shaping and allows to improve mask aligner lithography beyond current limits. Improved light uniformity, telecentric illumination and the possibility of freely shaping the angular spectrum of the illumination light are the main features.

Full control of the illumination light allows to simulate and optimize the mask aligner lithography process from the light source to the photoresist process. Simulation tools like the LayoutLAB software of GenISys and the Fraunhofer IISB development and research lithography simulator Dr. LiTHO were used to optimize mask aligner lithography.

Full control of the illumination light and lithography simulation are allow to reduce diffraction effects at the photomask, enhance resolution, improve CD uniformity, stabilize critical features and finally increase the yield in mask aligner lithography. For the first time it is now possible to implement front- end lithography enhancement technologies like customized illumination, optical proximity correction (OPC) and source-mask optimization (SMO) in mask aligner lithography.

Novel mask aligner lithography techniques, like halftone-proximity and pinhole-Talbot-lithography, allow printing periodic sub-micron structures like Patterned Sapphire Substrate (PSS) for LEDs at large proximity gap. Fresnel-lens-imaging allows printing vias for TSV with extended depth-of-focus. Photomasks with sub-resolution features and multilevel phase masks allow to generate a desired aerial image in the wafer plane. Mask aligner lithography has entered a new era referred as Advanced Mask Aligner Lithography (AMALITH).

8326-70, Poster Session

Improved flexibility with grayscale fabrication of calcium fluoride homogenizers

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High quality and highly uniform illumination is a critical component for advanced lithography systems and wafer inspection tools. Typical sources cannot provide the required uniformity, particularly when used in the higher power modes required by the lithographic projection fields. One approach is to break the incident field up into a large number of sub-apertures and superimpose them on top of each other.

The challenge with this approach is to fabricate a high efficiency sub-aperture array element with low surface roughness and good uniformity. CaF2 tends to be the material of choice for these homogenizer elements due to its transmission properties in the deep UV spectral range. Previous research has demonstrated excellent uniformity from cylindrical homogenizer elements in CaF2 fabricated with a grayscale lithography process. An alternative approach to crossed cylinders is an array of spherical micro lenses. The micro lens arrays (MLAs) have a clear advantage over the crossed cylinder approach in that only a single fabrication process is required. The reverse side of the homogenizer element may be left as a highly polished plano surface. The MLA fabrication utilizes a similar grayscale process to the one used previously for the crossed cylinder homogenizer element. However, since the entire surface is created in one fabrication step, there is no chance of a process asymmetry that could introduce astigmatism to the element.

We fabricate and compare MLAs and crossed cylinder homogenizer elements fabricated using grayscale photolithography processes and discuss the added flexibility and performance of the MLA approach.

8326-71, Poster Session

Technological merit, process complexity, and cost analysis of self-aligned multiple patterning

Y. Chen, Peking Univ. (China)

As EUVL continues to slip as a high-volume manufacturing technology, self-aligned multiple patterning (SAMP) has become the only practical solution to move Moore's Law ahead. In this paper, we shall discuss the perspectives of several SAMP techniques and make some predictions about SAMP based scaling trend. Accurate technology and cost analysis of SAMP techniques must consider not only the process itself, but also the affected patterning steps (including the overlay strategy) of each critical layer. From process complexity & cost point of view, the SATP (triple patterning) technique is the most cost-effective while it has its own challenges in forming small mandrels. The DUV+SASP (6x) is most likely the maximum of frequency multiplication cycles assuming high-volume EUVL eventually becomes a reality in time. Beyond 5nm half pitch, the SAMP techniques do not bear much manufacturing meaning based on the future LWR and CDU control capability.

8326-72, Poster Session

The near-field characteristics of the focused-field embedded in a superresolution layer applied to lithography

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In the past years, resolution improvements in optical lithography have been done by continuously decreasing the illumination wavelength or improving the optical system. However, optical lithography is ultimately limited by the diffraction limit. In order to beat this limit, many techniques have been proposed during the last years. Among them, the Super Resolution Near Field (SRens) effect is a promising candidate that can potentially be applied in lithography. In this technique, a thin layer of a non-linear material is placed on the focal plane of the optical system. Under right exposure conditions, a submicron sized optical aperture will be opened in the SRens layer, which results in a focused spot smaller than the diffraction limited one. Although the SRens technique has been successfully applied, the near field characteristics of the super resolution spot is not well known up to date.

In the present work, we show a rigorous numerical study on the SRens focused spot formed from an AgInSbTe (AIST) SRens layer. The results indicate that a fine structure with high intensity is created at the top of the SRens focused spot, which can become very pronounced for certain conditions. Computation of the full width half maximum (FWHM) shows that the focused spot also becomes smaller. Thus, by optimizing the system parameters, such as the optical aperture, layers thickness, etc, a small spot with highly localized energy density at its center can be generated, which may be useful for lithographic applications. Moreover, we have analyzed the imaging properties of the AIST layer, and we have found that the material is also capable of imaging, in the near field regime, structures that are beyond the diffraction limit.

8326-73, Poster Session

Quantum mechanics in optoelectronic efficient material

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In addition, new types of integrated optical devices such as switches, modulators, solar cells and filters are made from the quaternary systems and integrated optoelectronics nanostructure materials for mathematical computations, that for customized boson particle energies( ) below the semiconductor band gap( ), the OAC (optical absorption coefficient) exhibits an decay off with the electric field and the photon energy correspondingly. The main purpose of the present study is to reformulate Callaway's theory for the transition matrix element, on the basis of the three band model of Kane and considering the fact that the OME depends on the electron wave vector and hence show that for modified photon energy greater than , oscillations are initiated in the OAC without any effect of Wannier-Stark levels; where as for modified photon energy below , no oscillations occur. These oscillations that Callaway and others have predicted are the additional ones due to Wannier-Stark levels and their results can be obtained from the present analyses under certain limiting conditions.

8326-74, Poster Session

Impact of non-uniform polarized illumination on hyper-NA lithography

X. Guo, Y. Li, Beijing Institute of Technology (China)

Polarized illumination has been considered as a significant resolution enhancement technique and successfully implements the 45nm node volume production for the hyper-NA lithography. In order to get superior critical dimension uniformity (CDU), most of the parameters in polarization illumination system should be accurately calibrated. Since lithography performance is sensitive to the illuminator imperfections [1, 2].The effects of parameters' imperfection have increasingly significant impact on the pattern fidelity as the critical dimension (CD) continuously decreases. There are many system errors in illuminator due to the limitations of material and fabrication technology, such as intrinsic and stress birefringence, align mistake, etc. These imperfections can lead to the degradation of degree of polarization (DOP) and the decrease of both image contrast and depth of focus, which motivate us to control the DOP as well as possible [3].

In the past, an ideal top-hat model is used to describe the light source in simulation [2], however the perfect top-hat illumination source never exists, neither does the distribution of DOP [3]. This hypothesis loses its accuracy when evaluating the performance of the polarized illuminator. In this research, we focus on studying the impact of DOP on CDU under various conditions, especially for the non-uniformity distribution of DOP (NU-DOP) across pupil. The spatial non-uniform characters of DOP are formulated in the Gaussian distribution model, from which we generate different type of illumination sources and perform simulation analysis.

DOP obeys a random Gaussian distribution on the pupil plane. μ is the mean value of NU-DOP across the whole pupil, and δ is the Gaussian standard deviation (SD) of the NU-DOP. The Gaussian distribution DOP value is constrained in the range of [0, 1]. In order to minimize the influence of the random distributions of the DOP, we generate 50 groups of source at the same time and simulate CD error of each single group. Finally, the average CD error has been calculated to represent the overall impacts on CD.

The simulation is carried out by PROLITH™ X3, where we choose Line/Space pattern to study the impact of non-uniform polarized illumination on CD. We use a water immersion projection lens with hyper-NA (1.35) to achieve the resolution of 45nm. 6% attenuated phase shifting mask and annular illumination are used to enlarge the process window.

The result shows that the proposed model can evaluate the property of illuminator efficiently. When the mean NU-DOP approaches to 1, the effect of non-uniformity becomes more pronounced. In addition, the greater the SD is, the CD error becomes larger and the CDU becomes rougher. Furthermore, the NU-DOP distribution causes more CD error at defocus position. The CD error caused by NU-DOP distribution increases exponentially when pitches increase from 90 nm to 150 nm.

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8326-75, Poster Session

Three-dimensional polarization aberration in hyper-numerical aperture lithography optics

J. Wang, Y. Li, Beijing Institute of Technology (China)

Polarization aberrations (PA) of projection lenses have obvious impacts on imaging results in hyper-NA immersion lithography, and have been introduced into vector imaging models.[1] Precision of lithography simulation depends greatly on the accuracy of PA obtained from real optical systems.

All current representations of PA are two-dimensional (2D) PA. Lithographic imaging models separate polarization effects of optical systems into two parts: 2D PA and transformation effects from 2D PA to 3D pupil polarization functions (PF) due to the curvature of the exit pupils. And 2D PA calculated by polarization ray tracing (PAC) are directly used for imaging simulation.

In this paper, the shortages of 2D PA are analyzed. We discover that 2D PAC and 2D PA utilized in imaging simulation (PAI) are based on different coordinate systems that cannot be transformed to each other. Moreover, transformation matrices from 2D PAI to 3D PF are decided only by their pupil positions and have no relationship with the field of view. The difference of coordinate systems and the imprecise transformation brings errors to imaging simulations, and it goes worse when considering point near periphery of field and when numerical aperture increases.

An innovative three-dimensional PA is introduced. Three-dimensional (3D) PA is composed of three-dimensional "polarization ray tracing matrices"[2], representing transformation effects on the three elements of electronic field. Three-dimensional PA unify the polarization coordinate systems of PAI and PAC into global coordinate system. PF in conventional imaging theory are substituted by 3D PA, so transmission matrices are abandoned in imaging theory. Furthermore, without complex definitions of local coordinate systems, 3D PA are easy to calculate and understand.

The method of calculating 3D PA is presented in detail. We apply polarization ray tracing to rays propagating through the optical system. 3D polarization ray tracing matrix of each polarization element can be calculated by sandwiching Jones matrix in local coordinate systems between two orthogonal transformation matrices. Polarization ray tracing matrix of all optical elements is obtained by cascading the polarization ray tracing matrices for each element ray. Then polarization ray tracing matrices constitute 3D PA.

As an example, we calculate the 3D PA of lithography optics. The experimental optical system is a 5× reduction immersion lithography optics with NA 1.30, and the refractive index of immersion fluid is 1.435 at wavelength 193nm. Moreover, 3D PA are compared to PF transformed from 2D PAI to illustrate errors of 2D PA. The results show that conventional 2D PA have obvious errors in contrast with three-dimensional PA. Especially, errors at the edge of pupil are larger than that at the center of pupil. Errors of real parts of P11 and P22, which mainly represent the diattenuation of x and y direction, can be as large as 0.2. And distribution of errors moves when considered field is changed.

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8326-76, Poster Session

Overlay performance optimization based on the auto grid correction system

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Based on the metrology sampling and modeling connected to specific process history, APC has ever been widely used in control the combined effect suffered from the uncertainty process. With the shrinking of overlay performance, the automated optimized overlay correction system

has already become more necessary. To further improve the overlay performance in SSA600/10A of SMEE, the Auto Grid Correction method is introduced into the experiments. The UniLith Tool which developed for the Litho optimization is partly included into AGC system and used to decomposition and analysis of sampling data. Furthermore, several different kinds of correction method integrated in the AGC system has been designed separately and shown some effective result in automated overlay control. Finally the balance between overlay performance and Lot circling time is also concerned. By using the exponential weighting method in AGC system, the sampling time consumption can be reduced adequately.

8326-77, Poster Session

A hybrid model/pattern-based OPC approach for improved consistency and TAT

T. S. Desouky, Mentor Graphics Egypt (Egypt)

As the technology advances, OPC run time turns to be a big concern and a great deal of our efforts is directed towards speeding up the LITHO operations. In addition, the OPC simulation consistency is sometimes deteriorated which is a critical issue especially for anchor features. On the other hand, full chip designs usually comprise large arrays of basic cells, used by OPC engineers to tune OPC recipes, which is evident for instance for memory design and processor chips. The model based OPC technique is not necessary for such designs provided that the equivalent mask shapes for one cell of these arrays are already known.

In this work, we introduce a combined approach using model and pattern based OPC. Pattern matching is used to extract regions from full chips that match the basic designs stored in pre-created libraries. When matching occurs, OPC solution stored in these libraries is used and populated across matched areas. Special treatment for large array boundaries is applied due to proximity effects. Model based OPC is used for the rest of the chip. This approach has two main advantages. First, simulation consistency is greatly improved since the OPC solution for standard cells is priory known. Also, pattern matching is a DRC based tool and thus it is very fast compared to LITHO operations and hence TAT is further enhanced.

8326-78, Poster Session

High-hydrophobic topcoat approach for high-volume production and yield enhancement of immersion lithography

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Immersion lithography is applied widely in high volume semiconductor production. Semiconductor industry's demands are increasingly to push the throughput up further, miniaturize the critical dimension more, and reduce immersion defectivity to almost zero level. To meet these severe requirements, immersion scanner performance is being improved generation by generation. The NSR-S621D is the latest immersion lithography scanner by Nikon that can meet these requirements. Stage scan speed becomes faster at 700mm/s to increase the productivity. This high stage motion requires higher hydrophobicity of the immersion process materials. Higher hydrophobicity also helps to reduce immersion defectivity. Edge peeling control which is known as one major source of immersion defect becomes more critical to meet very low immersion defect requirements.

There are two immersion lithography processes. One is topcoat process. Another is topcoat-less process. The beauty of the topcoat process is to allow the chip manufacturers to optimize their resist and topcoat process independently. It increases the freedom of process material choice for the users. Therefore, the topcoat suppliers can focus on the immersion related topcoat performance improvement, while the chip manufacturers can continue to use their own optimized resist process by incorporating the latest topcoat with specific material property to meet

the requirements of the next generation immersion lithography.

There are, however, several challenges to increase the hydrophobicity of topcoats.

1.The method itself to increase the hydrophobicity

2.How to optimize high hydrophobicity with adequate dissolution rate to the developer solution. Development process related defects like bridge defect would be increased if dissolution rate became lower.

3.How to manage high hydrophobicity with low blob defect. Blob defect is also development related defect and have a tendency to increase with increasing hydrophobicity.

4.How to balance high hydrophobicity with good adhesion performance to the wafer. Adhesion usually becomes weaker with increasing hydrophobicity of topcoat.

5.How to compromise high hydrophobicity with zero bubble defects. Some type of immersion scanner shows increasing tendency for bubble defects with increased hydrophobicity of topcoat.

To overcome these challenges, both material and immersion scanner requires special tuning and optimization. Nikon as an immersion scanner vendor collaborated with JSR as a topcoat supplier to address these challenges. This collaboration enabled the clarification of each technical aspect specifically aimed to meet the next generation topcoat requirements, including hydrophobicity and adhesion strength to the wafer. In this paper we initially clarify these aspects and their determination method. Secondly, we will introduce the newly developed, a very high hydrophobic topcoat with dynamic receding contact angle (D-RCA) exceeding beyond 75 degree. Its basic performances and the method of how to overcome various tradeoffs for increasing hydrophobicity will be discussed. Thirdly, we will discuss scanner related improvements to increase productivity and stability including enhanced tandem stage control method and local fill nozzle technology. Finally, we will show the ultimate performance of the newly developed very high hydrophobic topcoat and the new generation immersion scanner with lithography performance and defectivity data.

8326-79, Poster Session

A computation of partially coherent imaging illuminated by a polarized source via the stack pupil shift matrix approach

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A salient feature of numerical simulations of the partially coherent imaging applied to the DUV projection lithography pre-fabrication testing is the intensive utilization of the SVD and FFT algorithms. A large number of the algorithms reported have so far focused on the computation of a kennel function known as the Transfer Cross Coefficients (TCC) in the Hopkins imaging theory. Recently, Yamazoe et al reported a new imaging formulation based on the Abbe imaging theory. They proposed methods of computing the Stack Pupil Shift Matrix (SPSM) as the kernel. In their approach, the computation complexity for both SVD of the kernel and FFT is demonstrated to be impressively reduced.

We report a computation of the partially coherent imaging with a polarized illumination using an improved SVD algorithm applied to the stack pupil shift matrix computation method. To our knowledge, the case of a polarized source is taken into account by directly stacking the x-, y- and z-direction stack pupil shift operator. The polarization of the source is described with a 2x2 coherent matrix which is decomposed in two independent polarized modes with certain weight determined by the polarization. For each of the polarization, we compute the stack pupil shift function in each of the x-, y- and z-direction. For a fast computation of the aerial image, the SVD algorithm is applied to each of the polarized directional kernel. In this way, the total complexity of the SVD computation is reduced. To compute the full mask image, we compute the sum of convolution of the eigenvectors of each of the kernels and the 2D mask. For a fast decaying spectrum of the stack pupil shift matrix, we make the truncation of the sum with an estimate of the global precision. In a test with an annular source, we design a mask pattern and the result of our computation agrees with that of a computation with the Prolith package.

8326-80, Poster Session

In-situ measurement of lens aberrations in lithographic tools using CTC-based quadratic aberration model

X. Wu, S. Liu, S. Xu, X. Zhou, W. Liu, Huazhong Univ. of Science and Technology (China)

The quadratic aberration model used in optical lithography is a natural extension of the linear model by taking into account interactions among individual Zernike coefficients. Although the model has been tested and verified in many applications, the effects of Zernike coefficients under partially coherent imaging are usually obtained by extensive experiments due to complexity of the model expression. In this paper, a generalized triple cross-correlation operator (TCO) is proposed, and a fast algorithm to simulate the quadratic aberration model is developed. Simulations were performed by the proposed TCO base algorithm with different input Zernike aberrations for binary and phase shift masks with multiple pitches and orientations, which demonstrate that the proposed approach is not only accurate but also efficient for revealing interactions among different Zernike orders under partially coherent illumination.

8326-81, Poster Session

Robust resolution enhancement optimization methods to process variations based on vector imaging model

X. Ma, Y. Li, X. Guo, L. Dong, Beijing Institute of Technology (China)

In order to push the optical lithography systems to their resolution limits, the resolution enhancement techniques (RET) are extensively used in the electronics industry, which promise to deliver superior sub-wavelength printability. Optical proximity correction (OPC) and phase-shifting mask (PSM) are two major RET approaches. OPC modifies mask amplitude patterns by the addition of the sub-resolution assistant features (SRAFs), while the PSM modulates the phases of the transmitted field to achieve a favorable constructive or destructive interference effect.

Recently, a set of OPC and PSM optimization algorithms were developed under nominal conditions and scalar imaging models. However, these methods above have two main disadvantages, thus, not yet fully applicable to the real world manufacturing. First, these methods are only designed for the nominal system settings without giving sufficient attention to the process variations caused by the aberrations, defocus and dose variation. However, the process variations existing in the practical optical lithography systems become more pronounced as the critical dimension continuously shrinks. The effects of the process variations may degrade the image fidelity of the printed images that are projected by the mask patterns optimized under nominal conditions. On the other hand, most of current OPC and PSM optimization algorithms are based on the scalar imaging models that fall short to take into account the vector nature of the electromagnetic field in the optical lithography systems. As the technology nodes enter the sub-wavelength realm, the lithography systems with larger NA (NA>0.6) begin to serve as the predominant microlithography technologies, and their vector nature cannot be ignored.

To overcome the above limitations, this paper focuses on developing the robust gradient-based OPC and PSM optimization algorithms to the process variations based on the vector imaging model. This is accomplished as follows: The projection optics model described in [1] is used to calculate the aerial images and formulate the objective functions of the optimization problems. The effects of process variations are explicitly incorporated into the vector imaging model. The robustness of the proposed algorithms to the process variations is assessed by the process windows (PW) of the optical lithography systems. To improve the robustness of the proposed algorithms to the process variations, the weighted average imaging performance is optimized by minimizing the superposition of the objective functions under both of the nominal

and defocus conditions. Meanwhile, the objective function under certain imaging condition is designed as the Euler distance between the target pattern and the actual aerial image projected on the wafer. Subsequently, the steepest descent algorithm is used to optimize the mask iteratively. We also apply a set of acceleration techniques to speed up the proposed algorithms. Finally, the Prolith software is used to evaluate and validate the improvement of the PWs due to our proposed algorithms. The extensive simulations presented in this paper illustrate that the proposed algorithms are effective to improve the PWs whenever the aberrations exist or not. The universality of the proposed algorithms is also proven by the extensive simulations based on different mask structures.

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8326-82, Poster Session

Gradient-based resolution enhancement optimization methods based on vector imaging model

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Due to the resolution limits of optical lithography systems, the electronics industry has relied on resolution enhancement techniques (RET) to compensate and minimize mask distortions as they are projected onto semiconductor wafers. Optical proximity correction (OPC) and phase-shifting mask (PSM) are two major RET approaches. OPC modifies mask amplitude patterns by the addition of the sub-resolution assistant features (SRAFs) that can pre-compensate for imaging distortions. PSM induces phase shifts in the transmitted field which have a favorable constructive or destructive interference effect.

Recently, model-based RETs (MBRET) gain a revival of interest for the advanced lithography with technology nodes under 45nm, since they introduce more degrees of freedom during the optimization process, and may result in higher resolution of the printed image. However, most of current MBRET optimization algorithms were developed under the scalar imaging models, which are only accurate for numerical apertures (NA) less than approximately 0.4. As the critical dimension (CD) continuously shrinks, the immersion lithography system with hyper-NA (NA>1) begins to serve as the predominant microlithography technology, where the vector nature of the electromagnetic field must be taken into account. Thus, the MBRET methods based on scalar imaging models are not adequate to produce desired performance when applied to immersion lithography systems.

The major contribution of this paper is the development of gradient-based OPC and PSM optimization algorithms based on the vector imaging model. First, an integrative and analytic vector imaging model of the optical lithography system is formulated in matrix format according to the projection optics model described in [1]. Subsequently, the steepest descent algorithm is used to optimize the mask iteratively. We also apply a set of acceleration techniques, such as the electric field caching technique and the fast Fourier transform, to speed up the proposed algorithms.

A second contribution of this paper is to introduce the generalized wavelet penalty (GWP) to reduce the complexity of the optimized mask patterns. Although the traditional wavelet penalty (WP) proposed in [2] has been proven to be effective for the optimization of binary masks and four-phase PSMs, it is not tailored for two-phase PSMs. The reason is that the WP intends to keep a pixel value on the mask as close to its neighboring pixels' as possible. Thus, the WP tries to divide the clear openings and 180°shifters far away from each other. However, the above concept of WP conflicts with the key point of PSM, which is to pose clear openings and 180°shifters close to each other, and induce a favorable constructive or destructive interference effect. In order to overcome this limitation, we propose the GWP in this paper, where the traditional WP is independently applied to the clear openings and the 180°shifters. Extensive simulations show that the proposed OPC and PSM optimization algorithms are adequate to effectively enhance the

resolution and image quality for the immersion lithography systems. In addition, the GWP is capable of reducing the complexity of the optimized mask patterns.

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8326-83, Poster Session

Consideration for application of NTD from OPC and simulation perspective

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State of the art Extreme Ultra Violet Lithography (EUVL) gives high hope for further shrinkage of semiconductor devices, but currently, EUVL is not ready for 2Xnm node manufacturing and ArF immersion must extend its capability in manufacturing 2xnm devices. Extending the limit of ArF requires varieties of Resolution Enhancement Techniques (RET) such as inverse lithography (ILT) , double patterning (DPT), spacer patterning and so on. One of the most brightest candidate for extension of ArF for contact layer is negative tone development (NTD), since this process utilizes the high contrast of the inverse tone of the mask for patterning. NTD usually results in high process margin compared to conventional PTD process.

Therefore, in this paper we will study application of NTD from OPC and simulation perspective. We will first discuss difference of NTD from PTD. We will also discuss on how to optimize NTD process in simulation perspective, from source optimization to simulation calibration. We will also discuss what to look out for when converting PTD process to NTD process, including OPC models to design rule modification. Finally, we will demonstrate the superiority of NTD process though modeling and simulation results with considering these factors mentioned above.

8326-85, Poster Session

Predictable turn-around time for post tape-out flow

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A typical post-out flow data path at the IC Fabrication has following major components of software - Boolean operations before RET, RET [SRAF and Optical proximity operations], post-RET Boolean operations and sometimes in same flow Simulation based verification. There are 2 factors that an IC Fabrication data path manager wants for the flow - predictable completion time and fastest turn-around time. At times they may be competing. There have been studies and literature modeling the turn-around time from previous runs and using that to dedicate resource allocation [3]. This is more workable in predominantly simulation dominated tools but for edge operation dominated flow it may not be possible especially if some processing acceleration methods like pattern matching or hierarchical processing is involved. In this paper, we suggest a method where we provide a concept of not doing any upfront resource modeling and even resource planning but providing target turnaround time and priority of the jobs. The methodology then systematically either meets the turnaround time need and potentially lets the user know if it will not be met as soon as possible. This builds on top of resource management work previously published [1][2]. Following graph is initial demonstration of the concept.

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8326-87, Poster Session

Optimal modeling for model-based OPC using genetic algorithms

J. Jeong, S. Park, S. J. Lee, S. Lee, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

In many wafer level experiments involving photo-lithographic processing via model-based OPC, a key role of successful performance is supported by an accurate OPC model where increasingly small and dense designs requiring adequate DOF, MEEF, and EL have been employed to increase yield. Once an initial choice for the model is made, it is not easily modifiable after other optimization efforts have already been involved such as recipe tuning, process optimization and so on. Model optimization should be done in the early stage separately from knowledge of the fab's OPC correction, but conventional modeling method especially for sub 20x nm nodes brings into question the model accuracy, in other word whether the model parameters are globally optimized or not.

In this paper we employ genetic algorithms (GAs) to determine the model parameters that produce an accurate prediction for the photo-lithographic process. These multidimensional optimization techniques proceed by parametrizing an objective function in terms of a finite set of coefficients so as to produce a globally optimized OPC model with improved accuracy followed by lithographic performance. The use of GAs allows global optimization without falling in local optimum via selection, crossover and mutation operating which are verified in the full chip level. We show optimal modeling results which enable production at below 20nm node.

8326-88, Poster Session

A full-chip NILS aware OPC solution

X. Li, Y. Ping, R. Lugg, Synopsys, Inc. (United States)

Traditional Optical Proximity Correction (OPC) only minimizes the edge placement error (EPE) at nominal condition (nominal focus and nominal exposure dose), which may result in an unacceptably small process window at more advanced technology nodes. Therefore, to improve process robustness and enhance yield, more advanced OPC techniques such as process window aware OPC (PWOPC) has been developed. PWOPC typically requires extra process window models at process corners in addition to the nominal model. However in practice it may be difficult to create such process window models due to lack of measurement data and other reasons. The normalized image log-slope (NILS) at nominal condition is a generic metric of aerial image quality and it is closely correlated to the exposure latitude. In this paper, we present a full-chip NILS aware OPC solution which only requires the nominal model. The overall flow of NILS aware OPC solution will be demonstrated, which is fully compatible with Synopsys' PWOPC solution. We will show how different requirements such as EPE, NILS, MRC can be better met with more advanced correction techniques. We will apply the NILS aware OPC solution to several test patterns and use a lithography verification tool to demonstrate how NILS and process window will be improved compared to traditional OPC methods.

8326-90, Poster Session

Lithographic tool dynamic coordinate calibration for CDU improvement

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In lithographic scanner, many different physical factors could impact to image quality and CD uniformity. In optical systems, the pupil filling quality (source shape), wavefront error and stray light can decrease the intensity contract and shrink the process window. In mechanical domain, the vibration and scanning synchronization error have the similar effect to imaging process.

Imaging in scanner is a dynamic exposure process and in this process, aerial image should keep the same relative position to the wafer. It requests the lithographic tool must have a very stable mechanical frame and very good motion control performance. In addition, the wafer stage, reticle stage's coordinate and projection lens' grid should be matched exactly, include the scanning direction and velocity ratio. The tool's alignment system can calibrate the statistic coordinate for overlay, but it cannot calibrate the dynamic coordinate in scanning direction very well because project lens' grid has a small asymmetric signiture. This systematic error should be calibrated for CDU improvement.

An imaging model considering the motion blurring is represented in this paper and based on this model, the dynamic coordinate's error could be analyzed. Furthermore, exposure method can be used to calibrate the dynamic coordinate and improve the CD uniformity.

Exposure latitude will be used to check and calibrate the lithographic tool's dynamic coordinate. We designed a special calibration process to obtain the best dynamic coordinate setting for scanner. In this process, some tool's coordinate parameters (scanning skew and scale) have been changed for every field to obtain the multi-dimensions' exposure information. Exposure window can be represented from this result, and in this exposure window, the best dynamic coordinate setting could be found. After the dynamic coordinate calibrated, the CDU is improved.

8326-91, Poster Session

RET and DFM techniques for sub-30 nm

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The resolution enhancement through lithography hardware (wavelength and Numerical Aperture) has come to a stop putting the burden on computational lithography to fill in the resulting gap between design and process until the arrival of EUV tools.

The 28nm node presents many difficulties due to low k1 lithography whereas the 20nm requires double patterning solutions. In this paper we present a global view of enhanced RET and DFM techniques deployed to provide a robust 28nm node and prepare for 20nm.

These techniques include optimized sub resolution assist features (SRAF) placement, advanced OPC manipulation, pixelated OPC as well as decomposition solutions for double patterning. These techniques are coupled with a fast litho print check, aka LFD, for 28nm P&R and a FEOL LFD kit for 20nm.

This work is part of the joint development work DECADE between ST and Mentor in the framework of Nano2012 sponsored by the French government.

8326-93, Poster Session

Resist model validity regarding source variation in SMO

C. Alleaume, E. Yesilada, V. Farys, STMicroelectronics (France)

Source Mask Optimization (SMO) is an advanced resolution enhancement technique with the goal of extending optical lithography lifetime by enabling low k1 imaging [1,2]. On that purpose, an appropriate source and mask duo can be optimized for a given design. SMO can yield freeform sources that can be realized to a good accuracy with optical systems such as the FlexRay [3].

Such optimization process is done through optical simulation to determine the source shape and need a resist model to predict the final wafer result. This resist model is calibrated once for a given source and corresponding wafers measurements. SMO will yield different sources for different design layout. With the existing flow, a new optical model is generated for each source. But resist model remains unchanged due to unavailability of corresponding wafer data.

We study the validity of the resist model calibrated for a given source with respect to other sources. A model calibrated for a given source is cross checked against wafer data obtain with different sources. Both freeform and parametric sources are studied.

The main goal of such study is to confirm if different sources can be used with the same resist model.

8326-94, Poster Session

Studies of the source and mask optimization for 20nm node in the active layer

C. Wei, United Microelectronics Corp. (Taiwan)

As semiconductor process technology moves to smaller dimension, RET (resolution enhancement technology) becomes more and more important, especially in low k1 processes. From 28nm node to 20nm node, the k1 becomes smaller with smaller dimension and pitch because exposure tool can provide larger NA (numerical aperture) or smaller exposure wavelength. SMO (source mask optimization) is a RET solution for low k1 process and provide better lithographic common process window in single exposure technology area.

Base on our studies of aerial image simulation and real wafer experiments on 20nm node, SMO could provide a better solution for 20nm node with 1.35 NA and 193nm exposure wavelength than the other RET sources (Quasar, C-Quad., Dipole).

In this paper, we will show you the optical theory, simulation result and wafer performance of SMO technology.

8326-95, Poster Session

Influence of SRAF size on main feature CD variation on advanced node

W. Lo, Y. C. Chen, Y. F. Cheng, M. J. Chen, United Microelectronics Corp. (Taiwan)

The mask error budget continues to shrink with device pitch. In advance node, Mask Error Enhancement Factor (MEEF) will increases up to over 4. The impact of assistant feature size on Main feature CD variation become more obvious. Generally, Sub Resolution Assist Feature (SRAF) use is an indispensable technique to provide adequate depth of focus (DOF) for larger pitches on layers with lithography settings that are optimized for denser pitches. But SRAF width will be critical issue with shrinking design rule. We investigated the impact of the assist feature size on through pitch performance. Using M3D model of Prolith to simulation the main pattern variation by adjust assistant feature size. SRAF printability through simulation and experimental wafer results were compared. We showed that the various mask CD cause wafer CD variation and the influence of assistant feature size on dense main feature become more obvious.

8326-96, Poster Session

Complementary polarity exposures for cost-effective line-cutting in multiple patterning lithography

F. T. Chen, W. G. Chen, M. Tsai, T. Ku, Industrial Technology Research Institute (Taiwan)

Multiple patterning is the only known way to extend current 193 nm immersion-based optical lithography beyond 40 nm half-pitch. A highly effective technique for multiple patterning uses self-aligned etched spacer to define the tightest pitch lines as critical features. However, to complete the patterning, the lines must be cut with at least one separate exposure. Beyond the 20 nm hp node, it is currently expected that multiple such exposures could be required, due to the multiple cut locations, which can be sized and spaced on the order of 10 nm. This, in turn, is expected to increase the cost of the multiple patterning.

In order to reduce the costs associated with multiple cut locations, it is proposed to group the locations into portions of larger features. In the simplest case, for crossed lines or at least two cut points on adjacent lines, it easier to unify the cut points with a straight rectangle or oblique parallelogram. Other than this case, the cut locations can be grouped into portions of polygon boundaries. These polygons will be much wider than the critical half-pitch and span several of the lines to be cut, and may be irregularly shaped as well. The cuts are effectively implemented by first exposing and patterning the polygon, and then exposing to protect the areas of the polygon not corresponding to the cuts. The polygon and protect exposure patterns must therefore be of complementary polarities. As expected, design rule restrictions for the cuts would be necessary to minimize the number of total exposures. Conversely, allowing more successive complementary polarity exposures and additional etch mask layers would enable more freedom in the cuts.

The cost reduction is determined by the reduced number of exposures, as well as the looser pitch and dimensions of the exposures. The number of e-beam shapes that must be generated for the polygons can be minimized by applying specific guidelines for the cut locations. Besides cost reduction, greater immunity to exposure shot noise (if EUV or EBL is used for cutting) is provided by the use of larger polygons. The benefits of complementary polarity patterning based on these key issues will be analyzed for the 10 nm half-pitch application, and extensions to even smaller half-pitches will be discussed.

8326-97, Poster Session

Rigorous Maxwell solver for real-time optical metrology

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A rigorous and fast Maxwell solver is an important ingredient for reaching today's and future goals on the semiconductor road map. Shrinking feature sizes and fabrication tolerances lead to the necessity of tailoring complex mask and illumination setups in the framework of computational lithography, e.g., OPC or source-mask optimization. The demand for highly accurate metrology methods on the other hand requires accurate real-time near and far field simulations for inverse parameter reconstruction. In most of these applications the investigated mask or wafer patterns are parametrized with a possibly large number of variable material and geometrical parameters. In order to obtain simulated quantities of interest like diffraction intensities or the aerial image for

a given set of parameters, today often simplified models or databases are used. Both have a number of disadvantages. Increasing accuracy requirements often rule out the usage of approximative solutions from the beginning. Databases suffer from the curse of dimensionality, i.e., exponential sampling costs of high-dimensional parameter spaces. Furthermore, they are very unflexible and their construction requires a lot of computer resources and, even worse, man power in order to develop sampling rules.

The reduced basis method is a very well suited technique to overcome these problems. It generates a reduced model of a given parametrized mask or wafer setup which can then be solved extremely fast in an application. The construction phase of the reduced model requires minimal user input and the results of the reduced model are rigorous Maxwell solutions. In this contribution we will explain the features of the method, apply it to challenging 3D mask simulation setups, and analyze accuracy and computational costs.

8326-98, Poster Session

Determination of dynamic perturbations in optical systems from wavefront data based on opto-mechanical simulations

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High performance objectives pose very strict limitations on errors present in the system. External mechanical influences can induce structural vibrations in such a system, leading to small deviations of the position and tilt of the optical components inside the objective from the undisturbed system. This can have an impact on the imaging performance, causing blurred images or broadened structures in lithography processes. A concept to detect the motion of the components of an optical system is presented and demonstrated on a simulated system. The method is based on a combination of optical simulation together with mechanical simulation and inverse problem theory. On the optical side raytracing is used for the generation of wavefront data of the system in its current state. A Shack Hartmann sensor is implemented as a model to gather this data. The sensor can capture wavefront data with high repetition rates to resolve the periodic motion of the vibrating parts. The mechanical side of the system is simulated using multibody dynamics. The system is modeled as a set of rigid bodies (lenses, mounts, barrel) represented by point masses connected by springs and dampers that represent the coupling between the individual parts. External excitations will cause the objective to vibrate. The vibration can be characterized by the eigenmodes and eigenfrequencies of the system. Every state of the movement during the vibration can be expressed as a linear combination of the eigenmodes. The reconstruction of the system geometry from the wavefront data is an inverse problem. Therefore, Tikhonov regularization is used in the process in order to achieve more accurate reconstruction results. This method relies on a certain amount of a-priori information on the system. The mechanical properties of the system are a great source of such information. It is taken into account by performing the calculation in the coordinate system spanned by the eigenmodes of the objective and using information on the spectrum of frequencies present in the current vibration as a-priori data. The position and tilt of the individual lenses as a function of time is then calculated from several frames of the wavefront data and extrapolated to future timesteps. Information on the system gathered with this method can be useful for applying and controlling countermeasures against the vibrations during use of the objective or for designing new systems that are less influenced by vibrations.

8326-99, Poster Session

Enhancing lithography process control through advanced, on-board beam parameter metrology for wafer level monitoring of light source parameters

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Light sources for lithography have previously relied on three major metrics to determine if the quality of the light produced meets requirements for wafer production: center wavelength, bandwidth and energy. However, it is known that there are other independent laser beam parameters which can affect the ability of the lithography cell to controllably image a pattern onto the wafer. In general, these parameters are characterized and measured with off-line field service tools between before and after the laser service events. Off-line beam metrology takes long time to define beam parameters with limited information, and can't provide the real-time information during normal operation of the laser.

This paper will show real-time beam monitoring method using Cymer's on-board beam parameter metrology module attached to the XL light source platform (XLA and XLR). This tool has the ability to monitor laser beam parameters, including, but not limited to: beam divergence, near field profiles, polarization, energy density and beam pointing during wafer exposure. Experimental results will be shown to evaluate the effects of advanced beam parameters on scanner beam parameters, wafer imaging performance, and long-term wafer CD trend. In addition, wafer level source data monitoring and analysis tools will be used, which will provide a new opportunity for improving lithography process control for the most highly optimized low k1 lithography processes by providing additional high accuracy and high resolution laser parameter monitoring.

8326-100, Poster Session

Lithography target optimization with source-mask optimization

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In the very low k1 regime in optical lithography, strong off axis illumination is needed to print aggressive features at small pitches most of the time at the expense of other pitches. Catastrophic OPC was introduced to improve process windows at these pitches by biasing design line/space width using retargeting rules. With the increase of design density, model-based retargeting [1] is needed to deal with complex 2D patterns which are not easily addressed by rule-based approaches. With the introduction of double patterning, minimum pitch is relaxed but design feature sizes still remain the same. Often design targets are enlarged for lithography for better process window and printed features are trimmed back by etch process on the wafer. However the lithography target shapes can be still very critical for OPC in complex 2D cases [2]. Optimized lithography target shapes can greatly improve pattern fidelity as well as overall process window.

In this paper, we will consider a lithography target optimization in the source mask optimization (SMO) flow. The goal of the optimization is to obtain the best process under lithography and etch process constrains while meeting given design rules and design intents. A 20nm metal case will be studied. We propose to generate more litho-friendly targets from these target optimization integrated SMO runs. As a result of this tight integration, lithography target, source, and mask will be tuned together to provide best overall process window for the newly defined targets. Retargeting rules can be extracted from these litho-friendly targets for a library of test patterns. This lithography target optimization flow can provide a faster tuning and extension of lithography target rules. It also helps to define new retargeting rules during process development by bringing achievable process goals to design side.

8326-101, Poster Session

Weighting evaluation for a hybrid OPC modeling by using advanced SEM-contours from wafer and mask

D. Hibino, H. Shindo, Y. Hojyo, Hitachi High-Technologies Corp. (Japan); T. Do, I. Kusunadi, J. L. Sturtevant, Mentor Graphics Corp. (United States)

As design rule shrink down to 28nm node or below, Optical Proximity Correction (OPC) becomes complicated. As a result, measurement points have increased, and improving the OPC model quality has become more difficult. From the viewpoint of decreasing OPC calibration runtime and improving OPC model quality concurrently, Contour-based OPC-modeling is superior to CD-based OPC-modeling, because Contour-based OPC-modeling uses shape based rich information. Contour-based OPC-modeling by using Advanced SEM-contour which is combined of Fine SEM Edge, alignment and averaging technologies was examined, and model quality was significantly improved, as reported in SPIE advanced lithography 2010.

In SPIE advanced lithography 2011, an advanced hybrid OPC modeling which uses 1D CD measurements by CD-SEM and 2D contours created by the advanced SEM-contouring technology and panoramic Mask SEM-contour showed high predictability for both 1D and 2D, even though the relationship between 1D and 2D calibration has trade-off.

In this study, a weighing function on Calibre ContourCal produced by MentorGraphics was evaluated using the OPC data set same as the data set used in SPIE2011. The weighting function can be set for 1D structure and 2D structure separately. The quality of OPC model by using the weighting function will be discussed.

8326-103, Poster Session

Full-chip correction of implant layer accounting for underlying topography

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Photolithography for the formerly "non-critical" implant blocking layers is becoming more challenging as edge placement control budgets shrink with each node. In addition to the traditional proximity effects associated with the implant layer mask, the underlying active and gate layers can interact through a variety of mechanisms to influence the edge placement of the developed implant layer. These mechanisms include bulk reflectivity differences, resist thickness thin film interference effects, and reflective notching from pattern sidewalls. While the use of organic developable bottom antireflection coating (dBARC) can be effective in minimizing these influences, it does represent an added complexity and cost. Without such a dBARC, the CD impact can exceed 50 nm, or more than 25% of the target dimension. We propose here a framework for modeling and correcting for these underlayer effects. The approach is based upon calibration of an optical model representing only implant proximity effects and two additional optical models which represent the effects of the underlayer topography. Such an approach can be effective in delivering much improved CD control for complex layouts, and represents only a small impact to full-chip correction runtime.

8326-104, Poster Session

Pattern collapse improvement in LDD, S/D implant photo process

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Recently, in order to increase the number of transistors in wafer by small feature size, optical lithography has been changed to low wavelength from 365nm to 193nm and high NA of 0.95(dry ArF). And further wavelength is aggressively shifting to 13.5nm for more small feature size, i.e., Extreme Ultra Violet Lithography(EUVL), a kind of Next Generation Lithography(NGL)1. Because of that, minimum design of LDD(Lightly Doped Drain), S/D implant photolithography after gate process is also reduced and most semiconductor companies usually use dry ArF(193nm) source for fine patterning of this under 90nm technology node. And reduction of CD(critical dimension), more complicated sub-topology and dependency of surface status or treatment, lead to collapse of long line pattern or bridge of space pattern.

Recently, semiconductor companies had been troubled with line-pattern collapse/lifting, bridge of space-pattern and resist cracking, and there are many attempts to solve the collapse problem, for example, O3 surface treatment, photosensitive BARC, TARC and surface treatment of previous step. However, it's hard to avoid perfectly, process weakness and it involves other side-effect such as difference of iso-/dense-pattern CD, increasing of process cost and time delay due to increased process step.

So, we illustrate the feasibility of reduction of long line collapse/lifting or bridge of space using LER(Layer Extraction Rule) modification for mask level treatment and ultra-thin wet BARC for process treatment when we use KrF source.

8326-105, Poster Session

Symmetric polarization aberration compensation method based on scalar aberration control for lithographic projection lens

Y. Tu, X. Wang, L. Duan, P. Bu, Shanghai Institute of Optics and Fine Mechanics (China)

In recent immersion lithography, the numerical aperture of the projection lens is larger than 1 and polarized illumination is adopted as an effective resolution enhancement technology. Under such circumstance, polarization aberrations of the projection lens can induce non-ignorable imaging degradation, such as critical dimension (CD) error, best focus shift and image placement error, which lead to accuracy loss in OPC and overlay control. To minimize these adverse effects and improve the image quality, the methods to compensate the polarization aberrations are required for high resolution lithography.

An effective optimization procedure of exposure tools with polarization aberrations has been proposed by Tadashi Arai, et al, which is based on Polarization-Pauli-Zernike (PPZ) coefficients and lens position adjustment. Good results have been obtained for an actual immersion lens by this method. However, the optimization procedure is relatively complicated. According to the principle of the optimization process, PPZ sensitivity should be calculated by optical simulator and imported to the aberration solver before the lens position adjustment.

In this paper, we propose a symmetric polarization aberration compensation method based on scalar aberration control for lithographic projection lens. This method focuses on the compensation of polarization aberrations induced by radially symmetric retardances. Two typical radially symmetric retardances are described as follows: (a) A quadratically increasing radial retardance, whose fast axes are along the radial directions; (b) A high-order retardance, whose fast axes rotate 90 degree at the minimums of the retardance. Using the lithography simulation tool Dr.LiTHO, the best focus shift induced by polarization aberrations in situations (a) and (b) are calculated for two Att-PSM gratings oriented in X direction and Y direction, respectively. According to the results, polarization aberrations in situation (a) induce the same best focus shift in X and Y directions as spherical aberration does, while polarization aberrations in situation (b) induce different best focus shift in X and Y directions as astigmatism does. Based on this analysis, a linear relationship is established between conventional even aberrations and polarization aberrations induced by radially symmetric retardances. Once the linear relationship is established, polarization aberrations induced by radially symmetric retardances can be simply compensated by scalar

aberration control. The compensation accuracy is dependent on the even aberration adjustment accuracy of the projection lens and the sensitivity of mask pattern to even aberrations. When the retardances in situations (a) and (b) are both 10nm and the even aberration adjustment accuracy of the projection lens is 1.0 nm, the residual best focus shift can be reduced to be lower than 1.0nm for a grating of 45nm size and 90nm pitch. In situation (b), the process window increases 11.5% for 2D contact hole array of 90nm size and 180nm pitch by using the polarization aberration compensation method.

8326-106, Poster Session

Influence of sub-resolution assist feature size on main feature linewidth variation on 28nm node

Y. C. Chen, Y. F. Cheng, United Microelectronics Corp. (Taiwan)

The mask error budget continues to shrink with device pitch. In advance node, mask error enhancement factor (MEEF) will increases up to over 4. The impact of assistant feature size on main feature CD variation become more obvious. Generally, sub resolution assist feature (SRAF) use is an indispensable technique to provide adequate depth of focus (DOF) for larger pitches on layers with lithography settings that are optimized for denser pitches. But SRAF width will be critical issue with shrinking design rule. We investigated the impact of the assist feature size on through pitch performance. Using M3D model to simulation the main pattern variation by adjust assistant feature size. SRAF printability through simulation and experimental wafer results were compared. We showed that the various mask CD cause wafer CD variation and the influence of assistant feature size on dense main feature become more obvious.

8326-107, Poster Session

Computing exact Fourier series coefficients of IC rectilinear polygons from low-resolution fast Fourier coefficients

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No abstract available

8326-39, Session 10

Sub-20nm logic lithography optimization with simple OPC and multiple pitch division

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The CMOS logic 22nm node is being done with single patterning and a highly regular layout style using Gridded Design Rules (GDR). Smaller nodes will require the same regular layout style but with multiple patterning for critical layers. A line/cut approach is being used to achieve good pattern fidelity and process margin.[1] As shown in Fig. 1a, even with line patterns, pitch division will eventually be necessary.

Design-Source-Mask Optimization (DSMO) has been demonstrated to be effective at the 20nm node.[2] The transition from single- to double- and in some cases triple- patterning was evaluated for different layout styles, with highly regular layouts delaying the need for multiple-patterning compared to complex layouts.

To address mask complexity and cost, OPC for the "cut" patterns was studied and relatively simple OPC was found to provide good quality metrics such as MEEF and DOF.[3,4] This is significant since mask data

volumes of >500GB per layer are projected for pixelated masks created by complex OPC or inverse lithography; writing times for such masks are nearly prohibitive.

In this study, we extend the scaling using simplified OPC beyond 20nm in small steps, eventually reaching the 14nm node. The same "cut" pattern is used for each set of simulations, with "x" and "y" locations for the cuts scaled for each step. The test block is a reasonably complex logic function with ~100k gates of combinatorial logic and flip-flops.

Experimental demonstration of the cut approach using simplified OPC and conventional illuminators at the 14nm node dimensions will be presented with comparison to the complex OPC result. MEEF can be measured experimentally. Lines were patterned with 193nm immersion with no complex OPC. The final dimensions were achieved by applying pitch division twice.[5]

8326-40, Session 10

Fast source independent estimation of lithographic difficulty supporting large scale source optimization

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Source mask optimization (SMO) technology allows improved process window and variability for small numbers of critical clips and canonical layout configurations, and is emerging as a tool for technology development. Large scale SMO has been demonstrated recently, but processing thousands of patterns still presents performance challenges. We describe a fast, source independent method to identify patterns which are intrinsically difficult. Since lithographic performance is dominated by the weakest patterns, typically only a few patterns of the represented layout determine the source; adding additional patterns to the optimization does not change the result, so we would like to predict the subset of patterns likely to determine the source. We call this prediction problem lithographic difficulty estimation (LDE). LDE ranking may be used as a filter after clustering, or to choose representative cluster elements. A fast polygon based FFT gives a complex spectral representation (diffraction order weights) serving as as input to several functions corresponding to different aspects of imaging difficulty: Near Nyquist-limit spatial frequency, iso-dense patterns, frequency and phase diversity, and 2D vs. 1D. Each term contributes to an overall weighted formulation of estimated difficulty.

The method was validated by various approaches using synthetic and hand designed 22 nm patterns:

- Matching ranks provided by lithographic experts for a set of 2D metal patterns. Weights of the components of the LDE function were adjusted to improve the conformity of the sort order to expert judgment.

- With a ranked most difficult 10% subset of 1000 synthetic contact patterns (240 nm) , we used joint optimization to design a source, then performed process window simulation to estimate common process window (CPW) (Fig 1). We score within 5% of CPW metric obtained using all patterns as input to joint optimization. Using the 10% lowest ranked subset did not achieve the target depth of focus and degraded CPW 15%. Using a 10% random draws misses DOF target and degrades CPW 7% on average. Combining clustering with LDE representative element selection gave a CPW within 4% of the full set, combining coverage and possible interaction of weak and stronger patterns. It is shown to be robust as compression ratios are decreased; that is, the patterns from higher compression ratio are a proper subset of patterns selected with lower compression ratio.

- Using highest LDE rank to choose representative patterns after clustering, we show 79% reduction in ORC errors compared to a previous SMO source generated by joint optimization followed by spatial domain optimization from a few hand chosen patterns. The data in this case were 1000 M2 synthetic patterns of 400 nm extent.

The execution time of the method is lightweight compared to methods based on evaluating the mask transfer function (MTF) of a pattern based

on a specific source (Torres, 2009); this high performance also supports use of the method in interactive DFM scenarios, where designers or algorithms may obtain feedback on more lithographically friendly solutions.

Limitations where the method fails due to limits of OPC only correction, pattern interactions, and possible improvements to address these issues are described.

8326-41, Session 10

Generator of predictive verification pattern using vision system based on higher-order local autocorrelation

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Although lithography conditions, such as NA, illumination condition, resolution enhancement technique (RET), and material stack on wafer have been determined to obtain hotspot-free wafer image, those are still often found on a wafer. This is because the lithography conditions are optimized with limited variety of patterns. For 40nm technology node and beyond, it becomes a critical issue and causes not only the delay of process development but also the opportunity loss of the business. One of the easiest ways to avoid unpredictable hotspots is to verify enormous variety of patterns in advance. This, however, is quite time consuming and cost inefficient.

This paper proposes a new method to create a group of patterns to cover pattern variations in a chip layout based on Higher-Order Local Autocorrelation (HLAC), which consists of two phases. First one is "learning phase" and second is "generating phase". In the learning phase, geometrical features are extracted from actual layouts using HLAC technique. Those extracted features are statistically analyzed and define "feature space". In the generating phase, a group of patterns which represent actual layout features, are generated by correlating feature space and process margin. By verifying the proposed generated patterns, the lithography conditions can be optimized efficiently and dramatically reduce the number of hotspots.

8326-42, Session 10

Demonstration of an effective flexible mask optimization (FMO) flow

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The 2x nm generation of advanced designs present a major lithography challenge to achieve adequate correction due to the very low k1 values. The burden thus falls on resolution enhancement techniques (RET) in order to be able to achieve enough image contrast, with much of this falling to computational lithography. Advanced mask correction techniques can be computationally expensive. This paper presents a methodology with proof data that demonstrates a mask optimization flow and technology that enables access to advanced technique levels of performance but with the costs of much simpler methods. Brion Technologies has developed a product called Flexible Mask Optimization (FMO) which identifies hotspots, applies an advanced technique to improve them, performs model based boundary healing to reinsert the repaired hotspot cleanly (without introducing new hotspots), and then performs a final verification. ST Microelectronics has partnered with Brion to evaluate and prove out the capability and performance of this approach.

The results shown demonstrate improved performance on 2x nm node complex 2D hole layers using a hybrid approach of rule based sub resolution assist features (SRAF) and model based SRAF (MB-SRAF). The effective outcome is to achieve MB-SRAF levels of quality but at only a slightly higher computational cost than a quick, cheap rules based approach.

8326-43, Session 10

Full-field lithographical verification using scanner and mask intrafield fingerprint

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Full chip verification has become a key component of the Optical Proximity Correction over the last decade. Full field verification to catch the cross-field effects based on scanner information becomes more important in lithography verification. Lithographic Manufacturing Check (LMC) performed on Brion Tachyon's engine, which is the industry reference tool, now provides the capability to predict wafer CD variations across the entire field through process windows. LMC is catching and reporting weak lithographic points having small process windows or excessive sensitivities to mask errors based on the simulation from models with ASML scanner specific parameters.

ASML scanner intra-field information such as Dose, Focus, Flare, Illuminator Map, Aberration files or Mask Bias Map are integrated into the LMC run to create an across-field verification and can improve the accuracy of the prediction at different field locations. This run could then be compared towards a reference LMC result which does not have any scanner specific data.

Scanner information has been loaded into the LMC model by using the Scanner Fingerprint File (SFF) functionality. Various across field LMC runs with realistic scanner information have been then performed and compared to identify critical design hotspots or scanner drifts. Hotspots are then measured on silicon with Scanning Electron Microscopy (SEM) on a matrix product to correlate with simulation and to a ranking of Intrafield parameter contribution

8326-44, Session 10

Pattern selection in high-dimensional parameter spaces

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The calibration of models for OPC and lithography process simulation is done using experimental data from printing large number of patterns and measuring the results. Reducing the number of patterns used in calibration without compromising simulator accuracy and stability is important to reduce metrology requirements and calibration turn-around time.

A well accepted approach is based on ensuring that the patterns provide a good coverage of an image parameter space (IPS): Here, the aerial images of the patterns are characterized by a number of image parameters, such as Imin, Imax, curvature, slope and image density. Each image is represented by one point in the n-dimensional space spawned by these parameters. Patterns are assumed to be similar and redundant for calibration if their points are close to each other in IPS. A pattern selection using the IPS can be done, for example, by selecting one representative pattern from each region using a grid based approach. Techniques such as Principal Components Analysis (PCA) can further reduce the dimensionality of the parameter space -because of the "curse of dimensionality" for larger n where no two images are close to each other. Unfortunately, the reduction of an image with thousands of different pixel intensities to a small number of parameters causes a loss of important information, sometimes resulting bad pattern selections.

In this paper, we show that an IPS based pattern selection works well for certain interpolation based simulation models. In essence, it works well if closeness in IPS is predictive for closeness in the resulting pattern, and - more importantly - if a large image difference will lead to large distances in IPS. We show that this generally is the case for certain interpolating simulation models, but not necessarily for physical models. We propose a statistics based method that can handle IP-spaces with large dimensionality n, in principle allowing to use each pixel (n>>1000) as an individual parameter. The results from a prototype application of the method are discussed.

8326-19, Session 11

Design and manufacturability tradeoffs in unidirectional and bidirectional standard cell images in 14nm

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Regular design methodologies, local interconnects, multiple patterning processes and fin-based devices are enabling scaling to the 14 nm node. With the adoption of these new technologies it becomes necessary to rethink the conventions followed in standard cell library design that proved successful in the past. In this paper we have studied the interaction between standard cell library design and pattern transfer techniques in the 14nm node. Results of this work have identified a limited set of layout constructs which are needed for manufacture-able and efficient library design, with special emphasis on unidirectional BEOL standard cell libraries.

Bidirectional, unidirectional and fixed pitch BEOL standard cell images have been created and studied on the IBM 14nm FINFET based process. Even though design technology co-optimization (DTCO) revealed that the 14nm process is more amenable to unidirectional standard cell image design than its precursors, still a competitive unidirectional standard cell image required the following major changes compared to a bidirectional standard cell image: i)the transistor gates were contacted on the outside, ii) the power and ground were run inside the cell and iii) local interconnect was used to connect NMOS and PMOS networks.

As part of our holistic standard cell image design process we have considered physical design (or design integration) issues like pin access, power rail robustness and conflict-free coloring of multi-patterned BEOL levels. Standard cell image design results indicate that a unidirectional standard cell image has nearly the same active fin (or diffusion) efficiency as the bidirectional standard cell image, i.e. around 66% as seen in Figure 1. In order to compare the design-ability and manufacturability of the three classes of standard cell images we have also created a cell image evaluation framework. The framework starts with a medium sized library as input and performs the timing characterization of the cells. It proceeds with a real block design implementation using an automated commercial design flow (adapted to 14nm) to compare the design efficacy of the various standard cell images. Pattern construct counts and litho simulations demonstrate the superior manufacturability of unidirectional standard cell libraries. Preliminary construct count results as seen in Figure 2 reveal more than an order of magnitude fewer constructs on the M1 level for a unidirectional standard cell library as compared to an extremely regular bidirectional library. Thus the cell image evaluation framework would help identify patterning tradeoffs for an effective standard cell image design.

8326-20, Session 11

Design rule driven source mask co-optimization methodology for sub-20nm logic and SRAM

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Our study focuses on Back End of Line (BEOL) DRs optimization because BEOL includes a lot of critical DRs related to scalability for metal and via. The most critical DRs in metal layer are Tip to Tip (T2T) space and Tip to Side (T2S) space because T2T and T2S space are limiting scalability and routability for BEOL. However, as T2T and T2S become smaller as PW also becomes smaller. In our experiments, we show that through co-optimization of DRs, source and mask can improve 7% scaling of T2T and T2S DRs without reducing of process window. For via layer, the most critical DR is via to via (V2V) space and have to consider diagonal direction since via is located between bottom and upper metal overlap area orthogonally. It is important that reduce V2V space on diagonal direction because supposed that reducing metal pitch is available but cannot support V2V space on diagonal direction those does not have any improvement for routability. Our experiments show that 6% scaling improvement of V2V space on diagonal direction. We get to the conclusion which DRs optimization with SMO allow that improve scalability, PW and routability without any other process development at sub-20nm technology node.

8326-21, Session 11

A novel methodology for triple/multiple-patterning layout decomposition

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Double patterning (DP) in a litho-etch-litho-etch (LELE) process is an attractive technique to scale the K1 factor below 0.25. For dense bidirectional layers such as the first metal layer, however, density scaling with LELE suffers from poor tip-to-tip (TT) and tip-to-side (TS) spacing. As a result, triple-patterning (TP) in a LELELE process has emerged as a strong alternative. Because of the use of a third exposure/etch, LELELE can achieve good TT and TS scaling as well as

improved pitch scaling over LELE if further scaling is needed.

TP requires the layout to be decomposed into three different masks. In common practice, layout decomposition is converted into a graph coloring problem, where nodes represent layout polygons and edges represent same-color spacing violations. Layout decomposition is challenging for DP and it is even more challenging for TP.

In this paper, we propose a novel method that performs TP layout decomposition that uses existing methodologies and algorithms developed for DP decomposition. Our TP decomposition method maximizes the use of stitching (among all three masks) to result in the least number of coloring conflicts. The proposed method is also scalable and can be used to perform layout decomposition for multiple patterning with k-colors (with k being greater than or equal to 3). We verify the method on 20 and 14nm layouts and obtain conflict-free coloring for almost all layouts and a modest number of conflicts in the case of extremely dense layouts.

8326-22, Session 11

Overlay, decomposition, and synthesis methodology of hybrid self-aligned triple and negative tone double-patterning

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A negative-tone SADP (nSADP) process can be accommodated in a SATP (self-aligned triple patterning) process by printing wider mandrels such that the left space for the second spacers is reduced and only one line structure is formed by merging neighboring spacers together. Two different layout design strategies need to be applied to SATP and nSADP regions separately. In addition to design flexibility and pitch reduction, a 3-mask SATP mandrel recession (SMR) technique is proposed to use a lateral undercut/recession process to separate the mandrel edge from the line ends of the second spacers. In this manner, the overlay requirement of the final pad layer can be relaxed. We shall discuss several 2-D pattern decomposition and synthesis techniques based on mandrel & spacer engineering: shape symmetry based patterning, lateral protrusion for line ending, dummy aided patterning, mandrel recession to relax overlay requirement, etc. These techniques may open the opportunities to remove some strict design limits posed by 1-D gridded layout.

8326-23, Session 11

Computational lithography work flows and design rule exploration automation

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Lithography development has become extremely computationally intensive. For a particular technology node being developed, it is critical to determine the optimum source and OPC/RET for each layer. In this paper we present a flexible new computation system for automation of source, OPC and RET optimization of advanced lithography layers. Of course, before determining the optimum source/RET/OPC of any layer, it is equally critical to determine the design rules which can be manufactured at a particular technology node. The design rule computational lithography problem is a superset of the source/OPC/RET optimization problem. With an automated methodology, time for process development can be reduced dramatically if a process development engineer can determine the design rules through accurate, automated simulation of the entire flow. This paper further provides examples of the determination of optimum design rules for a 14nm process, through the use of a computational lithography Design Rule Exploration (DRE) flow inside the flexible computation system. The optimum design rules have been determined by utilizing user defined filters of the computational results, such as CD variation metrics, process window metrics, etc.

8326-45, Session 12

Multiple-image-depth modeling for hotspot and AF printing detections

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Typical OPC models focus on predicting wafer contour or CD; therefore, the modeling approach emphasizes careful determination of the location in photo resist (PR) and the exposure threshold, so that the 'cut' model image matches the wafer SEM contours or gauge the CDs most closely. This is an exquisite approach with regard to the contour-based OPC, for the model is calibrated directly from wafer CDs. However, for other applications such as hotspot detecting or assist feature (AF) printing prediction that might occur at the top or the bottom of the PR, the typical OPC model approach may not be accurate enough. Usually, these kinds of phenomenon can only be properly described by rigorous simulation, which is very time-consuming and hence not suitable for OPC.

In this paper, the approach to build the OPC model with multiple image depths will be discussed. This approach references the images at the bottom and/or the top of the PR. This way, the behavior of the images which are not shown at the normal image depth can be predicted more accurately without distorting the optical model. This compromised OPC modeling approach is beneficial for runtime reduction compared to the rigorous simulation, and for better accuracy compared to conventional model. The applications for AF printing and hotspot predictions using the multiple image depth approach will be demonstrated.

8326-46, Session 12

Process optimization through model-based SRAF printing prediction

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Sub Resolution Assist Features (SRAFs) are used in lithography to improve the manufacturing process window. As the critical dimensions (CDs) that need to be patterned shrink with every technology generation, SRAFs have be-come a critical and key component in enabling processes with manufacturable process windows (PWs).

SRAFs are added to the mask shapes to create a dense environment that improves the printability on wafer of the target design shapes. The size and placement of the SRAFs must be carefully optimized to provide the maximum process window robustness while avoiding printing on resist that could affect subsequent etching processes. The un-intended printing of assist features on wafer is an critical yield detractor, especially in newer technology nodes, where complex SRAF patterns and placement are becoming commonplace. The need for the accurate prediction of SRAF printing is therefore very important to achieve the maximum PW benefit without SRAF printing.

Often in the past, this optimal SRAF sizing and placement was based on a set of rules obtained through the analysis of PWs of a variety of assisted patterns on wafer as well of Scanning Electron Microscope images of the resist sur-face to monitor unwanted sraf printing. More recently, a model-based OPC (MBOPC) approach has been developed that involves training an OPC model by using assisted and non-assisted calibration patterns. This model can then be used to determine the size and placement of SRAFs through simulations during OPC computations, and is also used to ensure non-printing of SRAFs.

OPC models are traditionally calibrated to CDs at the bottom of the resist. These models are naturally better at accu-rately predicting the printing of SRAFS on bright field exposure or other exposure configurations where unwanted assist features appear as residual resist lines in resist. When employing exposure configurations where SRAFs ap-pear as holes in resist, for eg. assist features supporting main features on a dark field mask, or SRAFs supporting inverse tone features on a bright field mask, these models often fail to provide the required accuracy in predicting SRAF printing. SRAF printability prediction has thus far been tackled by large dose adjustments to the OPC model, to match simulation to wafer results. The drawbacks of this method have been two-fold - simple dose adjustments do not accurately predict printing across various SRAF configurations and the main feature printability is compro-mised.

We present in this paper a method to calibrate and predict printing of assist features that appear as a dimpling in the resist surface, by separately tuning the model parameters for the main feature and of the sraf printing model. With this method, we obtain a model that accurately predicts the printing of various configurations of SRAFs on wafer while still maintaining the accuracy on the main features. Figure 1(a) shows an example of a SEM top-down image of the resist surface where some amount of assist feature induced dimpling is present. Figure 1(b) shows the resist contours simulated by the main feature model while figure 1(c) displays the simulated contours of the sraf printing model accurately predicting the printing of the assist features. In the second part of the paper, we will present an analysis of the implementation of such a model in the OPC flow, and a discussion of the issues of trade-off between PW and full SRAF print avoidance.

8326-47, Session 12

Finite element models of lithographic mask topography

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Photolithography simulations are widely used to predict, to analyze and to design imaging processes in scanners used for IC manufacture. Much effort has been devoted to understanding the impacts of illuminator and projection lens models on the accuracy of the lithography simulations. Of equal significance is the role of the mask models and their interactions with the illuminator models.

To construct such models, the interactions of the fields with the mask topography have to be accounted for by numerically solving Maxwell's equations. Such simulators present fundamental tradeoff between the accuracy of the results they produce and the compute time. To quantify the accuracy vs. compute time tradeoff, we have evaluated the performance of mask topography model employing the Finite Element Method, FEM. By design, the FEM models provide the means to optimize the grids on which Maxwell equations are solved, and to allocate the computational efforts to the mask features most critical to the accuracy of the simulated images.

In our accuracy vs. compute time studies we used topographic mask models of the patterns representative of the current generation of the IC designs. The imaging models we studied incorporated illuminator designs available in the leading-edge lithographic tools. In this report we will discuss the accuracy vs. compute time tradeoffs of simulators incorporating oblique incidence illumination and FEM mask topography models. The examples we will present are representative of the analysis of the optical proximity effect for the current generation of IC designs.

8326-48, Session 12

Resist loss in 3D compact modeling

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Complex patterning schemes and shrinking process margins inherent in low k1 processes need more sophisticated verification checks, which may require the checks traditionally performed with compact litho models to be augmented with information from rigorous models, which include 3-D descriptions of process behavior. Production requirements cannot accept the turnaround time (TAT) impact of deploying rigorous models for full layout OPC and Validation applications. Therefore the capability to model resist loss and sidewall angle at different heights in compact form becomes a necessity for advanced node (28nm and below) processes. In one potential flow, regions identified by the compact model will later be passed to rigorous simulation. The same potential flow can be deployed for correction in a Process Window Aware (PWA) OPC scheme. Other approaches include more sophisticated compact models to take account of vertical profile of resist and simplified rigorous models which increase speed at a minimal price of accuracy.

Our method is an enhancement of compact modeling capability to include photoresist (PR) loss at different heights. We apply a first principle approximation to estimate the "energy loss" from the resist top to any other plane of interest as a proportional corresponding change in model threshold, which is analogous to a change in exposure dose.

This can be described as below using the center of PR thickness as example:

$E\_lost\_percentage = (E\_PRtop - E\_PRcenter)/E\_PRtop$

Feeding this number to the threshold value (C0) of compact model as the threshold value (C_PR_loss) for PR loss model, the model threshold value for PR loss model becomes:

$C\_PR\_loss = (1 - E\_lost\_percentage) * C0$

We used rigorous modeling tool, "Sentaurus Lithography" (S-Litho), to confirm our resist loss model and their contours show perfect matches. Those contours are further validated by overlay with SEM images. The pinching area is well captured by our compact model quantitatively while SEM can only show the trend to some extent. Another big plus is that our method has no TAT increase comparing to any rigorous solutions. So using this technique, resist profile degradation, which can be significant under limited Useable Depth Of Focus (UDOF) and is ignored in conventional OPC modeling and mask decoration, can be accounted for with UDOF + PWA modeling.

8326-49, Session 12

Binary modeling method to check the sub-resolution assist features (SRAFs) printability

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As modern photolithography feature sizes reduce, the use of sub-resolution assist features (SRAFs) to improve the manufacturing process window has become more prevalent. Beyond the assist features placement based on rules, model based assist feature (MBAF) flow is called to optimize the shape and the size of SRAFs, so that the process margin of the main features (MFs) is maximized. In the MBAF flow, a vital component is to build an accurate model that specifically checks the printability of SRAFs, which are supposed to leave no trace on wafer. Compared to the traditional optical proximity correction (OPC) model, the SRAF printability check model faces extra challenges, i.e. the small size of SRAFs represents the difficulty of describing the features precisely, the SRAFs are usually not measurable on wafer and the worst-case SRAFs printability is typically off-nominal condition. In this paper, we propose an innovative binary modeling method for SRAF printability check model, which does not require the measurement of SRAFs' size and yet provides accurate prediction of SRAFs printing on wafer. In this modeling method, the binary data entry of SRAFs print/clean on wafer was acquired by inspecting the SEMs taken from real wafer measurements, the local extrema of the signal intensity around the SRAFs was computed and classified to print/clean groups, and a special cost function was designed to separate the print SRAFs and clean SRAFs as much as possible.

To test the validity of the new algorithm, two experiments were designed to calibrate the SRAFs printability check model with the binary data entry and the gauges placed across the SRAFs. Both data sets were acquired from IMEC photolithography processes. The first experiment is for contact layer, in which the process has a phase shifted field with bright MFs and SRAFs mask and an optical system with hyper NA of 1.35. The annular source has a wavelength of 193nm and σin of 0.65 and σout of 0.9. The source polarization is chosen to be x-y sector polarization. The second experiment is for poly layer, in which the process has a bright field with phase shifted mask and an optical system with hyper NA of 1.35. The quasar source has a wavelength of 193nm and σin of 0.6 and σout of 0.96 and an open angle of 20 degree. The source polarization is chosen to be x-y sector polarization as well.

In both experiments, the SEMs were inspected manually and all SRAFs gauges were categorized into print/clean groups. Then the binary modeling method was applied to the data sets. The results show that the print/clean gauges in two experiments are in full separation, indicating the accurate prediction of the binary SRAFs printability check models. And the models were further verified with SEM images.

The details about the binary modeling method and the calibration process of the experiments will be disclosed in the full paper.

8326-50, Session 13

A study of vertical lithography for high-density 3D structures

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In recent years, with smart phones, tablet PCs and other electronic devices becoming progressively smaller and more intelligent, the demand for integration-of-semiconductor devices has increased. As Nanofabrication proceeds with difficultly, one alternative that has attracted attention is 3D structure technology; layering multiple semiconductor chips vertically and interconnecting the chips using Through Silicon Via (TSV) and Bump processes.

Canon's rich experience in the field of i-line lithography led to the development of the new "FPA-5510iV" i-line lithography tool that accommodates patterning in thick resist.

"Vertical Lithography" is required to provide vertically deep imaging of holes with diameters ranging from one to several tens microns in thick resist.

The FPA-5510iV supports vertical lithography with a new projection lens having a large depth of focus. The Numerical Aperture and Sigma of the projection lens is adjustable, allowing control of the depth of focus and the resist profile for various patterns.

Canon has developed novel functions to adapt the FPA-5510iV to vertical lithography including the Through Silicon Alignment scope (TSA-scope). The TSA-scope provides IR backside alignment capability that is required for TSV and MEMS fabrication.

Another new function is the non-contact Wafer Edge Shielding (WES) unit that accurately masks a portion of shots that lay along the edge of each wafer during exposure. The WES allows negative-tone resist along the perimeter of the wafer to be stripped away during development, a requirement of back-end plating processes.

In addition, the FPA-5510iV lithography tool is capable of handling warped and distorted wafers that often result from the 3D wafer bonding and thinning operations.

Initially, Canon is applying the FPA-5510iV to TSV and Bump processes for 3D packaging. In the future, we would like to increase our contribution to the development of various high density 3D structures as typified by MEMS.

In this paper, we will report on FPA-5510iV evaluation results that were gathered in cooperation with several advanced device makers. We will also introduce our product strategies including discussion of the lithography challenges for 3D packaging and Canon's efforts to solve them.

8326-51, Session 13

A reliable higher power ArF laser with advanced functionality for immersion lithography

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Nowadays ArF immersion lithography is widely used for device manufacturing at the 45nm node. For the micro-fabrication at the 32nm node and beyond and until EUV lithography is ready, double patterning lithography using ArF laser is considered to be a strong candidate.

So far, in order to achieve high throughput and high NA in immersion lithography, narrower spectral bandwidth is required for ArF lasers. If double patterning technology is introduced to micro-fabrication at the 32nm node and beyond, not only high throughput but also Reliability, Availability and Maintainability are required. Because double pattering lithography may increase the number of processes and as a result the manufacturing cost is expected to significantly increase. Reliability, Availability and Maintainability are important keys to reduce the cost.

We developed a new laser, which is made on GigaTwin platform. The new laser inherits the performance of GT62A-1SxE, realizes higher Reliability, Availability and Maintainability and also meets a latest illumination enhancement technology.

The three innovative technologies are employed on the new laser. The first one is new chamber technology. It can significantly extend chamber life time and contribute to higher reliability and availability. (fig.1)

The second one is advanced gas management technology. It can realize operation laser without gas exchange and contribute to higher availability. (fig.2)

The third one is advanced monitoring and self-diagnostic system. It can always monitor laser performances and keep them optimum. It can reduce downtime and contribute to higher availability and maintainability.

These technologies and performance data are shown in our report.

8326-52, Session 13

Advanced light source technologies that enable high-volume manufacturing of DUV lithography extensions

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Deep UV (DUV) lithography is being applied to pattern increasingly finer geometries, leading to solutions like double- and multiple-patterning. Such process complexities lead to higher costs due to the increasing number of steps required to produce the desired results. One of the consequences is that the lithography equipment needs to provide higher operating efficiencies to minimize the cost increases, especially for producers of memory devices that experience a rapid decline in sales prices of these products over time. In addition to having introduced higher power 193nm light sources to enable higher throughput, we previously described technologies that also enable: higher tool availability via advanced discharge chamber gas management algorithms; improved process monitoring via enhanced on-board beam metrology; and increased depth of focus (DOF) via light source bandwidth modulation. In this paper we will report on the field performance of these technologies with data that supports the desired improvements in on-wafer performance and operational efficiencies.

One of the methods that can lead to higher wafer throughput is an increase in scan exposure speed which results in fewer light source pulses per scan window (assuming a fixed light source repetition rate). In order to provide an equivalent exposure dose at the wafer, the light source needs to provide a higher energy per pulse, which has been one of the drivers for introducing higher power DUV light sources. Moreover, pulse-to-pulse energy stability needs to be improved such that the dose repeatability can be maintained with fewer pulses, and pulse-to-pulse wavelength and bandwidth stability have to follow at least similar improvements. These improvements have been demonstrated with fielded systems running 90W power (15mJ @6kHz) over the course of nearly 2 years, and the performance data will be presented here.

For increased system uptime, improved light source gas management has been implemented with successive technology iterations requiring fewer interruptions under the category of gas lifetime extension (GLX). We will report on the most recent development, iGLX, which not only extends the time between automated gas maintenance events to every 4 billion pulses (Bp), but includes automated optimization of the gas mixture to ensure high efficiency. Field data from this new technology will be presented showing stable performance over extended periods.

To enable improved lithography process stability, we will report on the field performance of new, on-board light source beam parameter metrology which expands on the key performance indicators for the light source. The data will show approximately one year of monitoring under various operating conditions and illustrate the importance of integrating this data with other lithographic parameters for process monitoring. Finally, we will also report on the performance of focus drilling, the technology behind increased DOF using bandwidth modulation. This technology has been fielded for one year and tested under various operating conditions to demonstrate improvements in DOF which will be summarized here. The improvements described in the paper and supported by field data collectively support further extension of DUV lithography to multi-patterning applications for continued high performance at the lowest operational cost.

Immersion and dry ArF scanners enabling 22nm HP production and beyond

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Multiple patterning techniques will be utilized to the 22 nm HP and beyond. Building upon the proven NSR-S620D Streamlign platform, the NSR-S621D immersion scanner was developed to deliver enhanced product overlay and CD uniformity with improved productivity for 22 nm and subsequent generations. Since many different products are made within an IC manufacturing facility, various wafer process-related issues, including the flatness or grid distortion of the processed wafers and exposure-induced heating had to be addressed.

To enable continued process technology advancements, in addition to pattern shrinks at the most critical layers, resolution for less critical layers must also be improved proportionally. As a result, increased demand for dry ArF instead of KrF scanners is expected for less critical layers. Further, multiple patterning techniques actually enable use of dry ArF instead of immersion scanners for some critical layers having relaxed pattern resolution requirements. However, for this to be successful, the ArF dry tool must deliver overlay performance that is comparable to the latest generation immersion system. Understanding these factors, an ArF dry scanner that has excellent overlay performance could be used effectively for critical layers and markedly improve cost of ownership (CoO).

Therefore, Nikon has developed the NSR-S320F, a new dry ArF scanner also built upon the proven S620D Streamlign platform. By incorporating the Streamlign innovations, sufficient overlay accuracy for critical layers, as well as maximized productivity can be achieved.

In this paper / presentation we will introduce the latest S621D and S320F performance data.

Driving imaging and overlay performance to the limits with advanced lithography optimization

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Long time ago, the lithographer's life was relatively easy. The exposure system optimization choices were limited to only a few basic ones, like focus and dose for imaging and translation, rotation and magnification for overlay. However, with continuing shrink the complexity of lithography optimizations has increased significantly, resulting in today's status that high order process control for imaging and overlay is needed to keep up with the requirements. The newest scanner technology is introducing even a higher degree manipulation capability with the introduction of freeform illumination and wavefront control. Also for overlay a high degree of freedom is possible by applying corrections per exposure (CPE).

In this paper we will discuss the overlay and CD control budgets and present ways to extend NXT immersion lithography towards the 1X-node by improving imaging and overlay performance. The improvements are based on deploying the actuator capabilities of the immersion scanner for scanner generic and application specific lithography optimization. The recipe generation for the application is based on a combination wafer metrology data and computational lithography methods. For overlay, focus and CD metrology we use the YieldStar optical scatterometer. metrology using scatterometry. In specific we will show that on product overlay is improved by applying applications specific control using high frequent CPE. Intrinsic imaging performance is improved by using the freeform optimization of pupil and lens and across wafer CD control is improved by applying free form dose corrections. Additionally we show focus improvements based on a novel on-product focus metrology method.

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Part of Proceedings of SPIE Vol. 8327 Design for Manufacturability through Design-Process Integration VI

8327-01, Session 1

Bridging the resolution gap in 14 nm: designing for efficient transition to EUV

L. W. Liebmann, IBM Corp. (United States)

No abstract available

8327-02, Session 1

Implications of triple patterning for 14 nm node design and patterning

K. Lucas, Synopsys, Inc. (United States)

No abstract available

8327-03, Session 1

Yield enhancement with DFM

S. Paek, SAMSUNG Electronics Co., Ltd. (Korea, Republic of)

No abstract available

8327-04, Session 2

Layout optimization through robust pattern learning and prediction in SADP gridded designs

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Double patterning (DP), a technique which prints design physical layouts in two steps, is capable of doubling the pattern density and achieving the continued down-scaling of feature sizes and pitches. Since advanced lithography systems such as EUV are not expected to be ready for mass production any time soon, optical lithography with double patterning techniques is currently the only solution for sub 32nm nodes. Two main DP approaches are Self-Aligned Double Patterning (SADP) and Double Exposure Double Patterning (DEDP). SADP determines patterns through a spacer mask, formed by a film layer defined by a set of core (or mandrel) patterns. SADP is particularly robust in achieving good line width and pitch control. This advantage makes SADP an excellent choice for printing highly-regular patterns such as polysilicon and lower metal interconnect layers where the patterns are uni-directional.

Gridded layout style tries to strike a balance between performance and manufacturability. As printability continues to raise as a major problem for current sub-wavelength lithography systems, gridded design rules reduce allowable physical design space and enhance geometrical regularity. Consequently, manufacturability is enhanced, and this also results in less performance variability and higher reliability.

In this paper, we study the problem of placement-level layout optimization. We use a 32nm standard cell library where the metal-1 interconnects of the cells are uni-directional and patterned by SADP technique. Our goal is to minimize potential bridging hotspots in design layouts through predictive models constructed via machine learning methods and placement-level optimization algorithms. These potential hotspots result from the non-ideal printing of customized trim mask on top of the gratings patterned by SADP. Figure 1 shows example drawn shapes and the simulated PV-bands of the metal-1 layer.

In the first part of the paper, we explain how to build a predictive model for layout pattern classification using machine learning. Our support vector machine (SVM)-based pattern classification model categorizes a given layout clip as either robust or non-robust. We demonstrate the accuracy and efficiency of our predictive models. In the second part of the paper, we apply the predictive modeling of layout patterns to placement-level optimization. Our algorithm identifies and eliminates printing hotspots in standard cell based layout by applying local cell position modifications. Experimental results demonstrate the effectiveness of our proposed algorithms.

8327-05, Session 2

Self-aligned double patterning (SADP) compliant design flow

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In general, two major double patterning techniques, litho-etch-litho-etch (LELE) and spacer technology, a self-aligned double patterning technique (SADP), are targeted to enable the production of the key technologies below 20 nm node if EUV is not ready1. In the past, we have demonstrated that the critical design rules, such as line end-to-end, end-to-side, are smaller for SADP than for LELE, either due to their different decomposition natures, or due to their different sensitivities to process variations like overlay2-3. However, very aggressive tip-to-tip and tip-to-side may not be fully realized when routing is on grid for correct-by-construction purposes3. In addition, because of their different decomposition natures, the design rule set-up for SADP is expected to be different from LELE.

In this paper, we will present a SADP-compliant design flow by discussing the SADP-compliant design rules and investigating how SADP-compliant placement and routing are affected by the rules. We will evaluate the final design results from routing up to metal 5, and hope to provide objective guidelines of design-technology co-optimization. We will also present a simple design methodology that uses 2-color mapping which can be used by layout designers to determine if a layout is compatible with SADP.

8327-06, Session 2

Design-friendly double patterning

E. Yesilada, STMicroelectronics (France)

Double patterning using 193nm immersion has been adapted as the solution to enable sub 30nm technology nodes until the arrival of EUV tools. As a result the past few years have seen a huge effort in creating double patterning friendly design flows. These flows have so far proposed a combination of decomposition rules at cell level and/ or at placement level as well as sophisticated decomposition tools with varying density, design iteration and decomposition complexity penalties. What is more, designers have to familiarize themselves with

double patterning challenges and decomposition tools. In this paper an alternative approach is presented that allows the development of dense standard cells with minimal impact on design flow due to double patterning. A real case study is done on 20nm node metal1 layer where standard cells are designed without considering decomposition restrictions. The resulting layout is carefully studied in order to establish decomposition or color rules that can map the layout into two masks required for double patterning but without the need of complex coloring algorithms. Since the rules are derived from a decomposition unaware design they do not in return impose any restrictions on the design at the cell or placement level and show substantial density gains compared to previously proposed methods. Other key advantages are a simplified design flow without complex decomposition tools that can generate a faster time to market solution all at the same time keeping designers isolated from the challenges of the double patterning.

8327-07, Session 2

Pattern matching for double-patterning technology compliant physical design flow

L. T. Wang, V. Dai, L. Capodieci, GLOBALFOUNDRIES Inc. (United States)

This paper presents a pattern-based methodology for fixing DPT-compliant violations using a foundry-characterized library of "difficult to decompose" patterns with known corresponding solution(s). A pattern matching engine scans the layout at DPT-compliant error locations for patterns from the pattern library. If the layout patterns at the error locations were matched to the patterns from the library, one or more DPT-compliant alternatives are provided to the layout designers to be used as guidance for modifying the original layout.

This methodology is demonstrated on a sample 180,000 um^2 layout migrated from a previous technology node. A small library of 12 patterns is captured, which accounts for 53 DRC violations. Thus, by using this methodology, the number of DRC violations decreased by 5.3%. For some patterns, multiple DPT-compliant solutions exist. Some solutions preserve drawn design geometries, while others recommend specific changes to the original design for more robustness to manufacturing process-induced variation. For instance, extending the line-ends at which the two mask layers intersect increases the pattern's robustness to misalignment. The Pattern Matching users' interface can output multiple DPT-compliant patterns and present them simultaneously. The layout designers can then decide which solution to adopt.

8327-08, Session 3

Design-of-experiments-based design rule optimization

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Design rules are the primary abstraction between design and manufacturing. The analysis of the collective impact of rules on design scaling, design metrics and manufacturing yield is an intractable problem that is often solved in an empirical and unsystematic fashion. A systematic analysis of design rules would minimize the penalty of DRs in design metrics and relax selective DRs without any design impact.

We propose a novel compaction based methodology for design rule optimization which allows systematic exploration of complex design rules and their interactions. Sagantec iDRM tool was used as a part of our approach. We developed a multi-step methodology where we first choose a set of critical rules and perform a 2-level full factorial design of experiment (DOE) using the compaction framework. We compute the area of all variant layouts. By treating each design rule as a Boolean

variable (0 for nominal value and 1 for 20% higher value), we explore the interaction between rule combinations and the output cell area using Boolean minimization.

We apply this methodology to a set of ten, critical middle of line (MOL) layer design rules from GLOBALFOUNDRIES 20nm technology. The analysis was performed on six different standard cells. For most standard cells, only 2-3 design rules are found to be area-critical. This implies that the remaining 7-8 design rules that we analyzed can be relaxed by 20% without any increase in cell area.

In the future, we plan to co-optimize the critical set of design rules obtained from this approach with respect to both design and process metrics and extend this framework to front-end and back-end design rules as well.

8327-09, Session 3

Fully integrated litho aware PnR design solution

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Design For Manufacturing (DFM) is becoming essential to ensure good yield for deep sub micron technologies. As design rules are sometimes not sufficient to prevent manufacturability from problematic 2D patterns, optical proximity correction (OPC) limits have to be anticipated at design level.

To deploy DFM strategy at back end levels, STMicroelectronics has implemented a CAD solution of lithographic hotspots search and repair. This allows the detection and the correction, at routing step, of hotspots derived from lithographic simulation after OPC treatment.

The detection of hotspots is based on pattern matching and the repair uses local reroute ability already implemented in Place and Route (PnR) tools.

This solution is packaged in a Fast LFD Kit for 28 nm technology and fully integrated in PnR platforms. It offers a solution for multi suppliers CAD vendors routed designs. To ensure a litho friendly quality of repair, the flow integrates a step of local simulation of the rerouted zones.

This paper explains the hotspots collection, and the steps of the flow. Run time, efficiency rate, timing and RC parasitic impacts are also analyzed.

8327-10, Session 3

Replacing design rules in the VLSI design cycle

P. Hurley, K. Kryszczuk, IBM Zürich Research Lab. (Switzerland)

No abstract available

8327-11, Session 3

Smart double-cut via insertion flow with dynamic design-rules compliance for fast new technology adoption

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For advanced technology nodes (sub 28-nm), reduced margins on process variability and increases in design feature densities have slowed the turn-around time (TAT) for reaching mature yield, thus increasing the cost of IC fabrication. Therefore, methods involved

in design for manufacturability (DFM) have become essential to improve manufacturability of IC designs. This paper will present flow improvements related to the DFM method of increasing via redundancy, resulting in improved yield and functional performance of the chip.

In integrated circuit design, the via is a vertical conductor that allows electrical connection between different interconnect layers. Vias may fail partially or completely due to various process or reliability related issues such as random-defects, electromigration, misalignment, and/or thermal-stress-induced-voiding effects. Partially-failed vias will reduce reliability of the feature node, causing a short life-cycle before its complete failure. Also, such partially-failed vias will induce high resistance resulting in timing problems and degrading circuit performance. Completely-failed vias will introduce opens on the circuit, which may cause the entire chip to fail. Via-open defects are considered one of the most important causes of failure, and via yield is a primary factor in chip yield loss.

Yield can be enhanced by reducing the probability of partial or complete via failures. Insertion of another redundant via, connecting the same upper/lower metal-junction is a well-known and highly recommended practice for improving design reliability. If a single via amongst redundant via sets fails, supplementary vias will provide alternate connectivity. Previous studies have shown that redundant vias can lead to 10X-100X lower failure rates compared to single vias.

The solution for this problem must be automated because it needs to effectively operate on an extremely large number (up to hundreds of millions) of non-redundant vias. Another very critical requirement is that any enhancement to increase design redundancy should not introduce any new design rules violations after automatic-enhancement. Because of the extremely large number of vias involved, and multiple levels of via stacks, run time is a serious concern in implementing such a flow.

This paper presents run time optimization techniques which reduce run time by 8x to 10x when compared to flows operating without such an optimization strategy. The improved optimization scheme was achieved primarily by enhancing redundancy of via stacks in parallel as compared to enhancing them sequentially. We also present advanced techniques to identify physically or electrically non-redundant single vias in a computationally efficient manner. This flow uses Mentor Graphics® Calibre® YieldAnalyzer(YA) and YieldEnhancer(YE) toolsets for its implementation, and has a very efficient and optimized filtering component which selects only DRC clean enhancement shapes while filtering any vias that introduce new design rule violations. This guarantees a design rule clean output from this flow. Finally, this flow also provides an option to back annotate new shapes to the original design.

This flow was tested on various test chips with hundreds of millions of vias. We present the result of this flow on a mixed-signal test chip of 124mm2 that has 3+ Billion vias counted on four metal layers. We could enhance via redundancy by 89.2%, 99.5%, and 100% on the three via levels respectively from V1-V3, running on 65-bit 8-CPU machines with 16-GB of RAM in less than 5-days. We conclude that such a flow can efficiently enhance overall via-redundancy at the full-chip level.

8327-12, Session 3

Local loops for robust inter-layer routing at sub-14nm nodes

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Patterning the tight wire and via pitches found in 14 nm node presents severe challenges that can be overcome with regular layout techniques, double-patterning, EUV or emerging patterning techniques such as directed-self-assembly pitch multiplication. These processes, however, present restrictions on key layout constructs used for yield and reliability. Double-cut vias (Figure 1b) and via bars (Figure 1c) can form robust inter-layer connections. But, in these constructs, either the orthogonally routed lower metal (Mx) or upper metal (Mx+1) must route in a non-preferred direction to establish redundant connections. But at the wire pitches seen

in the 14 nm node, wrong-way metal exhibits excessive corner rounding or is even prohibited in the most aggressive resolution enhancement techniques. Under these patterning constraints, double vias or via bars block too many adjacent routing tracks, hurting the overall design quality. One alternative via redundancy technique is the local loop construct. The local loop consists of a single via connection (Figure 1a) and a redundant secondary path made of one Mx segment, one Mx+1 segment and 3 Vxs (Figure 1d). This layout construct blocks two metal tracks even at the scaled down metal pitches.

In this paper, we discuss various local loop constructs and use lithography simulations to assess their manufacturability and present area models of local loop and double via densities based on 14 nm process lithography and design rules. Lithography simulations show similar process variability (PV) bands and process windows for the different via constructs. In addition to layout dependent via failures, there may be random failures. Given a simple random via failure model, a single via has failure rate of p (e.g. 0.2 fail/109); a double via has a failure rate of p2 (e.g. 0.04 fail/1018); and the more lithographically-friendly local loop has a failure rate of 3p2-3p3+p4 (e.g. 0.12 fail/1018).

The paper also evaluates the "designabilty" of local loops, single vias and double vias by evaluating benchmark designs for power consumption, clock cycle time, area and redundancy insertion success rates. Local loop insertion can be easier than double via insertion owing to the flexibility in placement of the local loop, often without re-routing. Minimal extra capacitance of short redundant loop wires limits RC delay impact on critical paths.

8327-13, Session 4

A primer of physical design for lithographers

C. Yuan, Freescale Semiconductor, Inc. (United States)

Traditional DFM techniques such as OPC and lithography hotspot detection were typically applied in the mask preparation stage after a design tape-out. As the industry moves into advanced nodes, we find more restrictions are being imposed on designs to help alleviate the issues from ever shrinking process windows. These restrictions manifest themselves into various DFM rules or kits, which are often implemented in the design stages so that designs are correct by construction. In the Microlithography DFM conference, the number of papers related to physical design-for-manufacturing has been steadily increasing in the last few years. A few examples from the 2011 conference are

- DPT-aware "standard cell" designs, "placement" and "route" (TI, GF/Cadence/AMAT, IBM/ARM)

- litho-aware "STA" to accelerate "timing closure" on "hold time" (Renesas/Cadence)

- "AOI"-based implementation of the logic functions such as "XOR, MUX, and DFF" (PDF/CMU)

- "Rip-up and reroute" to fix litho hotspot (Infineon)

- etc.

Since the majority of the audience in this conference have a background in lithography, some of the terminologies and methods described in the presentations maybe hard to understand.

This paper gives a very basic introduction to the physical design implementation process that is applicable to lithographers. Simple examples will be used to explain some of the physical design terminology commonly heard in the DFM world. The goal of the paper is certainly not to enable a lithographer to begin working in the design area. Instead, it is to help lithographers understand some of the basics of physical design, so that they can better understand other DFM papers to be presented at the conference.

8327-14, Session 4

Analysis, quantification, and mitigation of electrical variability due to layout-dependent effects in SOC designs

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Motivation

With decreasing CMOS feature sizes, variability in devices has a significant impact on the performance and power of digital circuits. While some of this impact can be modeled by considering devices in isolation [1], it is also apparent that lithographic effects, and in particular stress, also make a major contribution [2]. Consequently, the context of a cell has to be considered [3]. Conversely, there have been attempts to mitigate the effects of variability by making cell layouts more regular, perhaps by including dummy diffusion. Such mitigation comes at a price - wasted area.

The objective of the study described here has been to investigate the effect of context upon variability in performance and power in standard 40nm and 28nm cell libraries. For the purposes of this study, we are primarily concerned with analyzing the cells used to build the clock tree, and here, we take "context" to mean those cells that lie on all sides of the cell under analysis - not the cell itself.

Case Study

We have used commercial 40nm and 28nm cell libraries for our study. We have generated a constant context for each of the clock tree cells, using just one cell to surround the cell under analysis. This should be consistent with the data supplied by the vendor and gives us a base context. We have then generated a large number of random contexts, in which any cells from the library may be placed around the cell under analysis. In both cases, we have used Cadence's Litho Electrical Analyzer (LEA) to automatically generate the context, extracted the stress effects of each context, quantify the delay and leakage variability, and compile variability reports. Furthermore, in the 40nm library, regions of dummy diffusion were included in the cell library in an attempt to standardize the context effects. We have modified the cell layouts in the library to determine whether these efforts are effective.

Results

Figures 1 shows typical results, in this case the variations of IDSAT for n and p-type transistors in a standard Inverter which consists of two n and two p-type transistors connected in parallel, simulated in 1000 different contexts. The contexts are generated such that the top and bottom surroundings are FILL cells while the left and right surroundings are selected randomly from the library. The inset texts in the figures show the reference IDSAT characterized from the base context. It is found the relative variation of IDSAT_N is about 6% and the IDSAT_P is about 9%, suggesting that the effects of stress on device characteristics are significant. Our study shows that the device/cell performance variability is mainly due to well proximity effects and the stress induced by diffusion spacing; the influence from the length of diffusion and poly spacing are negligible. Significant variation of the device leakage current, IOFF, is also noticed.

We investigated the effect on variability of dummy diffusion rails in standard cells. The dummy diffusions of both the victim and the context aggressors were removed. Table 1 compares the IDSAT variation with and without dummy diffusion. The differences are not significant. It is suggested that the dummy diffusion causes a small shift of IDSAT, but does not improve the systematic variability.

The performance and leakage variability of clock tree cells due to stress were simulated. Table 2 shows the worst and best 5 clock trees' timing and leakage variations. As stress plays a more important role for devices located near the border of the cell, the proportion of devices along the cell border determines the whole cell's variability. Therefore, smaller cells demonstrate higher variability. It is also found that the top and bottom contexts cells have negligible effect on cell variability, confirming that the

relative systematic variability of bigger cells should be less.

Conclusions

Dummy diffusion rails have a very small effect in terms of reducing systematic variability. Dummy diffusion enhances NMOS driving current but reduces the PMOS driving current. We have conducted similar analyses of other mitigation strategies, for example, the spacing between diffusion areas. Similarly, removing dummy poly increases IDSAT and IOFF, but does not affect the variability; and the smaller the distance from an active area to a well edge, the higher the impact on Vth. These effects and their impact on variability and on cell area will be discussed in detail in the full paper.

8327-15, Session 4

Development of connectivity based checks for analog circuits

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As we continue down the inexorable path of design scaling, the semiconductor industry continues to focus on both the manufacturability and the reliability of new and larger designs. That said, up to now there has been no seamless flow to correlate circuit topography checks with layout electrical and geometrical checks on devices to address reliability challenges.

We consider DfM to be techniques beyond simple adherence to design rules that improve manufacturability of designs. Such techniques typically yield their biggest advantage in technology ramp, but are also important for squeezing out yield from more mature technologies. In Freescale we continue to "stretch" the definition of DfM beyond its traditional boundaries. This includes design for reliability, where process maturity often lags that of simple manufacturability mechanisms.

Analog design is still focused on the 130-250nm nodes, with the cutting edge at 90nm. For analog mixed-signal (AMS) devices, sizes and spacings exceed minimum DRC values, meaning that analog technology shrink is not as aggressive as in the digital universe. For AMS DfM , the concern is parametric yield, with variability and mismatch the major focus.

Circuit checking has evolved from LVS to traditional ERC and now to new techniques such as Programmable electrical rule checker (PERC). PERC (Mentor Graphics- Calibre®) can empower advanced ERC checks in a user-defined fashion. The tool enables integrated electrical/geometrical checking and design guideline verification. The user can input a layout or netlist along with PERC/LVS rules and get violations as the output.

The focus of our work is two-pronged: first to develop connectivity checks at the schematic level and second to develop physical verification at the layout level. Standard verification capability for checking circuit topography is too limited and often requires time-consuming visual inspection before sign-off. There is great potential for human error in the specification of device recognition layers and other covering layers needed to perform such checks on physical layout. As such, we have begun investigation into device checks that no longer require such covering layers.

8327-16, Session 4

Design level variability analysis and parametric yield improvement methodology

R. Maerz, M. C. Keck, Intel GmbH (Germany)

Yield losses due to parameter variations of device and circuit parameters can be divided into three classes: statistical effects, mainly caused by local density variations of dopants, systematic effects, mainly caused by lithography and chemical mechanical polishing (CMP), and finally layout effects due to the biasing of wires and - to a lower extent - due to resolution enhancement technologies. Statistical effects are purely statistical, systematic effects describe changes caused by statistical variations of the fabrication process, and layout effects describe context

sensitive behavior which is not statistical at all.

Starting from the 32/28 nm platform, parametric yield losses start to become dominant. Under such circumstances global chip figures such as the architecture of the clock tree and/or the global clock frequency are affected by the parameter variations described above. The goal of this paper is to derive a methodology to handle the variability of device and circuit parameters event-by-event. Such a methodology allows to score parameter variations, identify thus the most critical devices and interconnections, reduce the variability by local repair, and finally to mitigate the variability by changing and/or adapting the design style and/or router settings.

It covers the prerequisites, i.e. the quantification of effects driving the variability and - based on this analysis - the setup of improvement actions. The effects under discussion include dose, focus and - to a lower extent - mask bias variations governing lithography, as well as dishing and anti-dishing caused by chemical mechanical polishing.

The paper presents a sensitivity analysis based on field solver simulations, which allows comparing the impact of competing variations of geometrical parameters such as line widths and thicknesses on the circuit parameters by computing the partial derivatives. For the design of clock trees, the analysis of the variations of coupling capacitances plays a prominent role. Such a methodology is in particular useful in an early development phase when the variabilities themselves are still drifting due to an increasing maturity of the underlying fabrication process.

This paper shows an analysis and quantification of the impact of lithography and chemical mechanical polishing (CMP) on the variations of interconnect structures in the metal layers. It includes a discussion of the process variabilities. A sensitivity analysis of metal layers is used to compare the impact of lithography and CMP.

8327-17, Session 4

Analysis of layout-dependent context effects on timing and leakage in 28 nm

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In advanced process technologies, layout context (i.e., the layout surrounding a cell) can impact the timing and leakage of a cell due to stress induced by layout features, well proximity effect, and other layout-dependent effects. Using Cadence LEA (Litho Electrical Analyzer), we conducted analysis on 28nm standard cells to assess the variation in timing and leakage characteristics due to layout-dependent effects. Our work extends prior cell library analysis using LEA [1] into 28nm; additionally, we describe our test structure design to validate layout dependent effects in Silicon. Furthermore, we study the timing impact at the block level and present best practices to mitigate the effect.

Cell-level leakage and timing analysis was conducted on a representative sample of 130 combinational and sequential cells each in the ULVT (ultra-low Vt) and LVT (low Vt) base cell-sets, and a smaller set of HVT buffer cells, in a 28nm library. A random set of contexts was generated for each cell in the study. We observe leakage spreads due to context of up to 28%, with average spread over all cells and states of 4.5%. As expected leakage spread in %age basis decreases with cell size. We measured levels of correlation of shifts across P transistors and show corresponding non-correlation between P and N device impacts from context.

For timing, we observed cell-level timing impacts across slew and load conditions, and identified conditions where shifts would be the greatest. Figure 1 shows the context-induced timing spread of the NAND3B_X1M in the LVT cell-set. Figure 2 shows context-induced timing spread in percentage for HVT INV_X1M. High load and slew conditions lead to the highest absolute spread (10.7ps in this case), while high slew and low load produce conditions for the highest percentage timing spread (8.5% in this case).

As results are sensitive to the specific contexts used in analysis, we analyzed additional context sets that include particular conditions, such as double-height, top-row and bottom row conditions. This helps

determine both the additional range of context-induced variation due to having these cells as neighbors, and also provided guidance for possible layout restrictions to reduce context-induced variations. For example, a 'lone context' cell with no neighbors is a significant outlier versus cells surrounded by cell neighbors, and so layout rules require neighbors around all active cells.

To further study the impact of context on timing, we analyze full paths in context to determine the timing variation at the path level versus timing. We do this by taking contexts from full block layout, obtaining extraction and timing for the layouts with contexts, and adjusting path timing accordingly. Analysis is ongoing (to be completed by full paper) to determine the impact of specific cell types as neighbors and the path-level timing impact of contexts in design. It is possible to either margin for the context-variation, mitigate through constraints on neighbors, or measure directly through a context-aware timing flow. We aim to show the benefits and tradeoffs of each of these approaches as a result of the path-level context-aware timing analysis.

8327-18, Session 4

Variability aware compact model characterization for statistical circuit design optimization

Y. Qiao, C. J. Spanos, Univ. of California, Berkeley (United States)

As integrated circuit manufacturing enters the nanometer regime, circuit performance variation is becoming more and more prominent. Variability modeling at the compact transistor model level can enable statistically optimized designs in view of limitation imposed by the fabrication technology. One such method uses an efficient Back Propagation of Variance (BPV) technique. However, these techniques do not accommodate the hybrid-hierarchical variation structure of the manufacturing processes. In this work we propose an efficient variability-aware compact model characterization methodology based on the linear propagation of variance. Hierarchical spatial variability patterns of selected compact model parameters are directly calculated from transistor array test structures. We call this method the Spatial Backward Variability Propagation method, or SBPV. This methodology has been implemented and tested using transistor I-V measurements and the EKV-EPFL compact model. The model parameters that will capture the spatial variability are characterized using linear regression on spatial pattern coefficients, using a spatially-tuned sensitivity matrix, which is first verified by the traditional linear BPV method. Calculation results compare well to full-wafer direct model parameter extractions. Further studies are done on the proper selection of both compact model parameters and electrical measurement metrics used in the method.

The proposed SBPV method can be extended and applied on more complicated and complete compact models, such as the industrial standard BSIM or PSP models. This can be realized with measurement data from well-designed variation-sensitive test structures, including I-V/C-V test structures of transistors with a wide coverage of different dimensions, Vth types and with DUTs placed in various optical proximity environments. Such test macros are designed using STMicroelectronics 28nm technology, which is being fabricated on both bulk and FD-SOI wafers.

In practice, variability-aware statistically characterized compact models can be integrated into the existing statistical circuit design flow for accurate prediction on circuit performance deviations caused by process variations. SBPV will serve in the statistical IC design flow by providing large numbers of physical-variation-aware compact model cards for Monte Carlo simulations or customized corner simulations. Furthermore, since the combination of random and spatial variability often yields non-Gaussian distributions, SBPV will more realistically capture the non Gaussian tails of those distributions and therefore be more suitable for generating proper corner models. Customized model cards for different design parameters, such as transistor length and width, can be generated as well. This will help increase both the speed and accuracy of statistical circuit simulation results.

8327-29, Poster Session

Framework for identifying recommended rules and DFM scoring model to improve manufacturability of sub-20nm layout design

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For advanced technology nodes, DFM methodologies have become increasingly important in mitigating yield-loss by

1. Addressing known yield-related issues early in the design cycle through recommended rules, and

2. Enabling CAD tools to quantify and score recommended rule compliance of a design.

DFM scoring quantifies the severity of a recommended rule violation based on a scoring model. This paper addresses a framework for building critical recommended rules and a methodology for devising scoring models using simulation or silicon data.

Recommended rules need to be applied to critical configurations (edge- or polygon-based geometric relations) which can cause yield issues depending on design variability (configurations with varying context) and process variability. Determining of critical recommended rules is the first step for this framework.

Based on process specifications and design rule calculations, we first characterize a recommended rule by evaluating the manufacturability response to improvements in a layout-dependent parameter. The region at which these response curves saturate is then identified.

Methods used here are:

1. Geometric budgeting (based on process specifications like overlay and CD uniformity margins) can be used for single dimensional rules (like short edge, min length rules, etc).

2. Monte-Carlo methods can be used for multi-dimensional rules (like overlap, enclosure, area rules, etc).

3. If the rule's origin is based on the lithography process, highly accurate litho-printability simulations can be leveraged to frame a scoring model. Here, printability simulations are used to simulate the printed-image contours on photo-resist or wafer (after etch). For rule-specific test structures, simulated litho-contours are then used such that the behavior of a litho-printability metric vs. drawn design data is generated.

4. Based on the learning from previous technology nodes, like redundancy rules.

After the rule selection, the next step is to correlate simulation and/or silicon data with rule-based scoring. Here, the scoring model is fitted to a response function obtained from computational methods like Monte-Carlo and/or litho-printability simulations or directly from silicon data.

The final step is to devise a chip-based scoring model. Here, multiple rules are scored based on their individual layout density weighted with their relative fault rates or priority.

In this paper, we present the above methodology for critical 20nm recommended rules.

In order to enable the scoring of layouts, this paper also discusses a CAD framework involved in supporting the use-models for improving the DFM-compliance of layout designs.

8327-30, Poster Session

Self-aligned double-patterning layout principle

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Self-aligned double patterning (SADP) has become one of the key

manufacturing processes for sub-20nm and smaller technology because of its robustness against the overlay. Differently from other double patterning technologies such as litho-etch-litho-etch (LELE) and litho-freeze-litho-etch (LFLE), patterns formed by SADP are not intuitive due to its distinctive process since layout data (patterns on a silicon wafer) and its mask data are not equal.

In the SADP damascene process, mandrel patterns must be formed with the mask to form spacer sidewalls. Final patterns on a silicon wafer are formed via these sidewalls, where some patterns are formed on mandrel positions and the other patterns are formed between sidewalls. This is the reason why patterns in the layout data cannot directly convert to mandrel patterns in the SADP process. Therefore, it is hard to judge where to set mandrel patterns in the given layout. If mandrel patterns are not set adequately, we cannot make the mask data properly.

So far, as well as LELE and LFLE double patterning technology, various layout decomposition methods for SADP have been proposed to select mandrel patterns adequately. However, it is difficult to select which patterns as mandrel and to decide where to place trim patterns. Also, Li proved the problem of SADP manufacturability is NP-complete. Consequently, our considerations are not to take the same strategies as LELE and LFLE double patterning technology.

Therefore we consider to design a manufacturable layout and not to decompose a given layout. We propose a new layout method for the SADP damascene process. First, we prepare a fundamental layout data painted in different two colors interchangeably. We can connect arbitrary patterns of one color of the two and at the same time, patterns of the other color will be cut to avoid two colors' crossing each other. Additionally, we can also cut arbitrary patterns in the layout. We call this connecting and cutting rule "SADP layout principle". According to this rule, the two colors in the resultant patterns are kept as initially colored interchangeably, and we can select either of the two colored patterns as mandrel.

8327-31, Poster Session

In-design hierarchical DFM closure for DFM-clean IP

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This paper identifies the needs and requirements for manufacturability checks such as litho and CMP at 28nm. We outline why these checks must be done early on and with minimum overhead to designers so that it reduces the risk of finding DFM issues at tape out time when design changes are very expensive. One of the challenges of checking IP for long-range DFM effects such as CMP is that the IP environment is often unknown at the time of the design. In this paper we outline block-based methodology that allows IP designers to perform quickly a comprehensive DFM analysis, including litho and long-range CMP effects.

At 28nm, most foundries stipulate that designs are checked for systematic manufacturing issues related to lithography and Chemical and mechanical Process (CMP). When first introduced lithography analysis was done by the fab after optical proximity correction just prior to mask making. To avoid finding these defects on silicon, thorough model-based checks were done to identify and fix these "hotspots" prior to mask making. But as process technologies evolved, the number of hotspots increased and correction became more challenging because the degree of freedom is very limited at that late stage of the design. Foundries started to recommend at 65 nm and, at 45 nm and below have made it a mandatory step to identify and correct these hotspots on the design side during design. Similarly, CMP, a mandatory manufacturing step used to polish away excessive copper above dielectric areas to define the copper lines in trenches, can leave Large variations in interconnect thickness. To minimize the effect of CMP, foundries have imposed the insertion of dummy-fills and rule-based checks, and to account for on-chip interconnect thickness variation, foundries have defined a rule-based

approach based on erosion tables, which approximate the thickness variations are as a function of metal pattern density or width. However, the CMP effect is quite complex to predict with rules. The thickness variation due to dishing and erosion depends not only on layout patterns, such as density and feature width, but also on process equipment, pad characteristics, slurry type, and dielectric materials. Contrary to lithography effect, which is localized, the CMP effect has much longer range, usually in millimeters. In addition, CMP has a multi-level effect, which means that any surface topography variation will propagate to the metal level above. As a result, the rule-based approach is not adequate to capture both long range and multi-level effects. Therefore, foundries have released model-based CMP sign-off that can be run on the design prior to manufacturing [2][3][4].

First, we outline how 28nm Physical verification has been augmented with litho and CMP sign-off. When only applied on the final chip database, it has been quite disruptive to find hotspots during tape-out, and equally hard to fix them. The need to create litho- and CMP-clean layout during creation emerged and required a tighter integration of the litho and CMP checks in design implementation. In-Design litho and CMP analysis and has been a key contributor to the adoption of DFM-aware designs.

Even with strong motivations and mandatory checks imposed by foundries, it is challenging to add new tasks to design flows. So it is important to implement a convergent, fast and integrated flow to get it accepted by designers.

Finally, our IP can be targeted to multiple designs. So it is a key requirement that the lithography and CMP checks can be easily applied during design and at block level. This creates a particular hard challenge for CMP which has a long-range effect [1].

The requirements for an efficient DFM sign-off for the IP developer are the following:

- Minimum overhead and ease of use for our designers

- Support block-based approach for both litho and CMP

In the section 2 we describe the block-based litho analysis. We've developed and deployed a solution that allows launching the litho sign-off directly in the implementation tool. In order to reduce the risk of user error, all parameters of the litho signoff can be preset up-front, and designers just have to launch the sign-off with a single command. If any hotspot is detected, the results are automatically loaded in the design environment for manual or automatic fixing as shown in Figure 1. The simplicity and reliability of this methodology has been key for the adoption by our IP designers.

In the section 3, a block level CMP analysis methodology is proposed to check for design robustness of an IP block against variations created by CMP. The application involves virtually placing the IP block in several environmental conditions, running CMP simulations on all of them, and checking the block thickness variations against tolerance ranges. This block level CMP simulation methodology enables designers to check for CMP related issues during early design stages. We also demonstrate that the same CMP physical hotspots captured at the chip level can be detected at the block level as shown in Figure 2 and Figure 3.

8327-32, Poster Session

Automated yield enhancements implementation on full 28nm chip: challenges and statistics

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At advanced technology nodes such as 28nm, design-related systematic yield loss is a dominant component of the overall yield loss Implementation of recommended design rules can help improve robustness of designs to manufacturability issues. While there are several tools and algorithms available for automated implementation of recommended rules, running these tools and managing the flow at the full chip level is a very complex task considering the extremely large amounts of data involved for a full chip database. In this paper, we present the details of a yield enhancement flow applied on a 28nm chip, including hierarchy and efficiency optimizations needed for successful implementation at the full chip level, while mitigating any runtime impacts on downstream mask data prep operations

We also give a brief overview of the Yield Enhancement tool developed and used by us to implement these changes, Yield Enhancement Suite: YES. YES insert polygons without impacting existing geometries, and without creating any new Design Rule Errors such that all added shapes increase the manufacturability of the chip. The focus, in this paper, for yield enhancements includes inserting redundant via, improving small metal area shapes and increasing the end-of-line metal via overlap.

First, before running the yield enhancement, we analyze drawn geometries in the full chip such as small area polygons and number of non-redundant via present. The analysis details are presented in this paper to benchmark enormous data involved as the starting point. Second, we run automated Yield Enhancement Utility YES on full chip gds files. In the experiments done on full chip, YES tool increased redundancy of vias, improved minimum metal area shapes as well as improving the end-of-line metal via enclosures. We share the detailed statistics for the impact of YES on full chip data detailing run time, machine resource and data size. The challenges faced in handling full chip are also shared and good techniques for efficient flow management of such large database are presented. After the YES tool creates the enhanced layouts, we discuss the algorithm used to measure the efficiency of the tool as well as share some alternate algorithms possible to measure efficiency.

Finally, we discuss techniques used to optimize the run time for YES, physical verification and mask data preparation involved in handling 28nm full chip large database of original layout as well as the enhanced layout.

8327-33, Poster Session

A study of pattern variability for device performance

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In this paper, we introduce a various analysis methodology of pattern variability for higher device performance using with applications of DBV (Design Based Verification).

Pattern variability is affected by both pattern process margins and electrical margins such as distribution of gate length.

In this report, we investigated about the relationship between a pattern feature and pattern distribution of transistor length.

AEI (the after etch inspection) silicon pattern-based distribution of transistor length analysis is substantially different from that based on the drawn layout because of OPC and dry etch loading.

Variability is a problematic phenomenon since during scaling of deep sub-micron technologies, pattern distribution ranges are increased and affected by it. Some pattern variability can affect certain transistor configuration, and because of that, it is important to identify the root cause for this sensitivity. In addition, extraction of the worst "eliminated" pattern group that will yield higher performance with the smallest distribution of transistor length range is needed.

8327-34, Poster Session

Intracell process variability: from self-aligned multiple patterning to multiple-gate MOSFETs

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Multiple-gate MOSFETs such as FinFET and Tri-gate MOSFET have become the mainstream logic device structures for continuous scaling of IC into deep nanoscale. Both multiple-fin and gate patterning of these

devices are becoming increasingly difficult as the optical resolution limit of immersion lithography has been reached. Apparently, prior to EUVL's readiness for high-volume manufacturing, multiple patterning is the only solution to break the optical limit. For example, 1-D grating structure plus the cropping process, so called "complementary patterning", may be used for future logic patterning. The idea is to create the grating structures by self-aligned multiple patterning (SAMP) while using extra masks to cut the grating structures to form useful logic features. However, SAMP processes have shown significant intra-cell variations, which is different from the optical and SADP processes. Therefore, we shall study intra-cell process variability and their impacts on device performance of advanced MOSFETs such as FinFET or Tri-gate MOSFET.

8327-35, Poster Session

Consideration of correlativity between litho and etching shape

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We developed an effective method for evaluating the correlation of shape of litho and etching pattern. The purpose of this method, makes the relations of the shape after that is the etching pattern an index in wafer same as a pattern shape on wafer made by a lithography process. Therefore, this method measures the characteristic of the shape of the wafer pattern by the lithography process and can predict the hotspot pattern shape by the etching process. The method adopts a metrology management system based on DBM (Design Based Metrology). This is the high accurate contouring created by an edge detection algorithm used wafer CD-SEM.

Currently, as semiconductor manufacture moves towards even smaller feature size, this necessitates more aggressive optical proximity correction (OPC) to drive the super-resolution technology (RET). In other words, there is a trade-off between highly precise RET and lithography management, and this has a big impact on the semiconductor market that centers on the semiconductor business. 2-dimensional shape of wafer quantification is important as optimal solution over these problems. Although 1-dimensional shape measurement has been performed by the conventional technique, 2-dimensional shape management is needed in the mass production line under the influence of RET. We developed the technique of analyzing distribution of shape edge performance as the shape management technique. In this study, we conducted experiments for correlation method of the pattern (Measurement Based Contouring) as two-dimensional litho and etch evaluation technique. That is, observation of the identical position of a litho and etch was considered. It is possible to analyze variability of the edge of the same position with high precision. The result proved its detection accuracy and reliability of variability on two-dimensional pattern (litho and etch) and is adaptable to following fields of litho pattern quality management.

- Estimate of the correlativity of shape variability and a process margin.

- Determination of two-dimensional variability of pattern.

- Verification of the performance of the pattern of various kinds of hotspots.

In study, it reports on the outcome of the experiment for effectiveness and the accuracy of this method.

8327-36, Poster Session

Advanced techniques for design assembly and characterization for the 14nm node with LFD using a black box API

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As circuit design scale beyond the 22nm node, the need to quickly and flexibly characterize the design manufacturability increases. Improvements in design practices as well as design software side are enabling this process. The use of carefully characterized design subunits (cells) in the general assembly of the chip is one way to ensure that products are optimized for increasingly difficult lithographic process challenges. Additionally, software for assessing design robustness is enhanced to deal with ever more complex resolution enhancement techniques. The current state of the art simulator and verification tool set contains a necessary step in creating simulation contours and process variability bands upon which various checks can then be performed and the construction of these contours and bands is often hidden from the user as it is assumed that traditional single or double exposure processes in which one or two masks create the final pattern in the layout are used.

With the introduction of many different process techniques that include double or multiple patterning steps, such traditional assumptions are no longer valid and a new mechanism needs to be implemented that supports any type and combination of patterning processes in a simple yet accurate fashion to construct the process variability bands that will be used for verification of the pattern manufacturability of the layout.

To address these concerns a new Black Box Interface (BBAPI) has been introduced that allows process teams to customize the generation of process variability objects to reflect the specific manufacturing steps of the Fab, without losing the data encapsulation needed to protect the process' intellectual property and maintain the usability of litho friendly design (LFD) concepts during physical synthesis.

The increased flexibility in creating contours and bands ultimately leads to more robust physical designs which are aware of every part of the patterning process. This paper addresses the techniques to improve design and process co-optimization including: optimization of base technology (pcell) constructs, choice of base technology constructs in IP cell design, and a new API (application program interface) to simulation tools. The paper will show an optimized design process that integrates use of these techniques to improve design stability and ease of assembly of robust chip designs for advanced optical process technologies.

8327-37, Poster Session

CMP effect due to perimeter: a perimeter drive dummy fill optimization approach

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In this paper, we investigate CMP impact on 1D polygon vs. 2D polygon for 28nm node. We demonstrate a perimeter driven dummy fill optimization methodology to minimize topography variations. Once a 28nm physical CMP model is calibrated, the model can then be used to predict surface topographies and thickness variations for a 28nm design. While keeping constant density and effective line width, we created a CMP test keys layout with varying perimeters for this study. Topography variations including dishing and erosion for the layout is then simulated and analyzed for copper ECD and CMP process flow steps, including CMP intermediate steps. Furthermore, the simulation results are validated against silicon data to ensure model predictability. Traditional dummy fill optimization applies density driven methodology to choose the best fill shape and size. Once the perimeter effects are decoupled from the density effects, designers can now apply perimeter optimization to further optimize fill shape and size that minimize thickness variation. This approach can also be extended for FEOL STI process.

8327-38, Poster Session

Lithography hotspot detection and classification through FEM and pattern matching

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As today's lithography technology advances towards printing features even below a quarter exposure wavelength, the process window has been shrinking smaller and smaller. At the same time, design complexity has increased drastically. Simulation based OPC verification has been widely adapted to remove potential hotspots before mask making. However, in today's advanced technology nodes, simulation alone before tape-out still cannot eliminate all potential hotspots due to increased design and process interaction. Some process sensitive hotspot patterns may pass rigorous simulation checks in design flow, but show up in production as yield impact systematic defects due to process variations. In this paper, we present a methodology by combining pattern matching, manufacturing metrology, as well as simulation to setup a flow to screen out those process sensitive patterns and build up process related hotspot pattern library.

In lithography process development of critical layers, FEM (Focus Exposure Matrix) wafers are routinely created for process window determination and assessment. We use special exposed FEM wafers and defect inspection system to pick pattern failures on wafers. The wafer inspection result of FEM wafers are then analyzed, ranked and classified with design based pattern centric defect analysis software. Simulation can be also used to test selected defect sensitivities. The most sensitive and repeating patterns will be outputted into a pattern library. By using Anchor Semiconductor's proprietary user-defined pattern search with pattern library, incoming designs can be quickly screened to improve pattern sensitivity in OPC; the pattern search result can serve as a good sampling guide for manufacturing metrology and inspection.

We will demonstrate our methodology flow using defect inspection on FEM wafers and design based pattern centric defect analysis/classification software and the benefits on incoming design screens and metrology/inspection sampling.

8327-39, Poster Session

Fast optical proximity correction with timing optimization ready standard cells

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Resolution enhancement techniques (RET) such as optical proximity correction (OPC) has become an integral part of the fabrication of integrated circuits to maintain the edge placement integrity of the original circuit design. Conventional OPC schemes are usually shape driven and full chip based, resulting in unpredictability in electrical behavior and huge computational effort. To overcome these drawbacks, a new OPC methodology which is electrically driven and based on cell-wise optimization is proposed. Simulation results when compared to conventional OPC approaches in the literature demonstrate better timing accuracy, reduced mask cost. Depending of the circuit test-set, an average run-time improvement between 3 to 8 times is achieved for circuit size with 100 - 400 cells. Further improvements can be obtained by adopting a hybrid approach by only optimizing the timing performance of critical paths. For the hybrid approach, better timing accuracy can be achieved while incurring little penalty on mask cost.

8327-40, Poster Session

Electrical design for manufacturability and layout-dependent variability hotspot detection flows at 28 nm and 20 nm

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In advanced nodes such as 28nm, lithography and stress cause layout dependent variability (LDV) that can result in unexpected and unaccounted timing variations as shown in [2][3]. As presented in [1], LDV methodologies needed to account for lithography and stress variability due to context-dependent variations are needed at 28nm technology node. We present in this paper how the 28nm electrical e-DFM methodology developed by GLOBALFOUNDRIES using Cadence LEA has been extended to 20nm with the addition of hotspot detection flows. We furthermore present more results on 28 nm.

With the advent of stress techniques in manufacturing, analog custom design is becoming very challenging because the impact of layout proximity on transistor performance is considerable and multiple iterations are needed to converge to a layout that meets the electrical performance defined during schematic design. Layout designers currently depend on a cumbersome layout design, RC extraction, and layout modifications cycle to verify the impact of stress and it is easy to end up with post-layout simulation mismatches between the layout and the schematic, resulting in long iteration loops and delayed time-to-market. Today, an analog designer must complete the layout, before it can extract stress parameters and run a full simulation to find if the layout is consistent with the electrical intent of the schematic. In this paper we present an on-the-fly LDV electrical analysis that is implemented in Virtuoso and can be used during the creation of the layout and it does not require a complete layout or full RC extraction and simulation. As shown in Figure 1, this Rapid Analog Analysis (RAA) flow enables a correct-by-design layout by providing fast Virtuoso built-in ability to check impact on device performance and matching. RAA relies on a static check performed on the transistor layout to quantify the impact of LDV on transistor mobility or threshold using a 20nm foundry-qualified model, and then flags excessive variations to the layout designer in Virtuoso using a hotspot check mechanism. A designer can also specify LDV matching constraints that are checked during the layout phase. This tool allows designers to catch problematic LDV early in design cycle to improve their design quality and reduce iterations.

For digital designs, while more focus has been on post-placement gate-level timing analysis [7] and optimization [8], the LDV analysis presented in [1] covers both standard cell and critical path variations, and unlike [4-6] and [9],covers both lithography and stress effects. Because standard cells may yield unpredicted timing variations due to context differences not predicted by timing libraries, the LDV methodology includes a Cell Context Analysis (CCA) flow that provides cell designers a rigorous framework to optimize their layouts and tune cell electrical performance. We provide additional CAA results for 28nm process technologies across more than 27,000 contexts and report mean delay variations above 5% as shown in Figure 3.

Finally, traditional static timing analysis tools do not incorporate electrical impact due to nearby context proximity. The LDV methodology includes an Advanced Timing Analysis (ATA) flow that accounts for the electrical difference by providing more accurate timing results and identifying paths that may deviate from nominal timing using a hotspot check mechanism. We provide additional ATA results for 28HP and 28SLP process technologies as shown in Table 1 and Table 2, respectively.

As compared to [1], main contributions of this paper are:

1. Additional results for 28 nm node.

2. New results using 20 nm node and comparison of stress and lithographical variations with respect to 28 nm node.

3. Electrical hotspot detection methods.

4. Validation with respect to HSPICE results.

We validate the accuracy of the LDV flow based on LEA against SPICE accuracy. We extend CAA and ATA flows to 20nm standard cells and designs. 28SLP designs are about 3X more sensitive to lithography

effects than to stress effects. More than 400ps timing slack change is observed when running LEA on 28SLP designs. For 28HP designs, both lithography and stress effects should be taken into consideration.

8327-41, Poster Session

Yield impacting systematic defects search and management

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Despite great effort before design tapeout, there are still some pattern related systematic defects showing up in production, which impact product yield. Through various check points in the production flow endeavor is made to detect these defective patterns. It is seen that apart from the known defective patterns, slight variations of polygon sizes and shapes in the known defective patterns also cause yield loss. This complexity is further compounded when interactions among multiple process layers causes the defect. Normally the exact pattern matching techniques cannot detect these variations of the defective patterns. With the currently existing tools in the fab it is a challenge to define the 'sensitive patterns', which are arbitrary variations in the known 'defective patterns'. A design based approach has been successfully experimented on product wafers to detect yield impacting defects that greatly reduces the TAT for hotspot analysis and also provides optimized care area definition to enable high sensitive wafer inspection.

A novel "User-defined pattern search" technique developed by Anchor Semiconductor has been used to find sensitive patterns in the full chip design. This technique allows GUI based pattern search rule generation like, edge move or edge-to-edge distance range, so that any variations of a particular sensitive pattern can be captured and flagged. Especially the pattern rules involving multiple process layers, like M1-V1-M2, can be defined easily using this technique. Apart from using this novel pattern search technique, design signatures are also extracted around the defect locations in the wafer and used in defect classification. This enhanced defect classification greatly helps in determining most critical defects among the total defect population. The effectiveness of this technique has been established through design to defect correlation and SEM verification.

In this paper we will report details of the design based experiments that were successfully run on multiple process layers in the production.

8327-43, Poster Session

Model-based searching method to find the integrated critical failure on the wafer

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The sub-32nm device node requires thinner resist thickness to have the sufficient lithography process margin to define the sub-50nm lithography CD and on the other hand the hard mask to etch the low-k material becomes dense and rigid to have the etch selectivity to the low-k material. This integration scheme makes the resist's etch selectivity worse to the hard mask, which is easy to cause the integration systematic hard defect likes the Cu bridge in the Metal layers. The sub-32nm patterning performance with the single exposure is almost on the edge with the 193nm immersion litho tool due to the NA limitation in the scanner with the water immersion material. The smaller lithography CD makes the aerial image contrast worse to have higher DC level in the unexposed patterns in the sub-32nm device node. This higher DC (latent image) level in the aerial image can sacrifice the resist thickness after the litho development process. The reduced resist thickness with the low contrast is very harmful for the etch process to have the current hard mask which is etched with the photo resist and BARC layers. Especially the dual damascene process is very weak in the Cu bridge margin due

to the trench first process which is related to the low image contrast. The current ORC is to detect the critical failure in the lithography process and there is no predictable method for this kind of integration systematic killing defects. Therefore the new detection method using the image parameters is necessary to search for integrated systematic killing defects with the optical simulation to avoid these defects which is very critical for the sub-32nm integration. This model based search method can make the robust lithography and etch process to have the sufficient process margin related to the integration.

8327-44, Poster Session

A scoring methodology for quantitatively evaluating the quality of double-patterning technology compliant layouts

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This paper presents a DPT-aware scoring methodology that is used to systematically quantify the quality of DPT-compliant layout designs in order to evaluate layout designs and provide guidance for any opportunistic layout modifications such that manufacturability- and yield-related issues can be improved. The methodology evaluates a DPT-compliant layout based on DPT-specific metrics that characterize a layout's vulnerability to process variation. The score for each metric is determined by using a mathematical model, defined through simulations and correlation with silicon data, which maps layout-dependent parameters to process sensitivities. Since the final yield is dependent on the combination of all process-induced effects, the individual scores for each metric are combined and abstracted to a composite scale of 0 to 1, in which 1 is the optimum score. Examples of DPT-specific metrics include: spacing variability between two oppositely-colored adjacent features, density differences between the two decomposition masks, stitching enclosure's sensitivity to misalignment, and variability caused by the increase in the density of stitches.

This methodology is used to evaluate the quality of DPT-compliant layouts and automatic decomposition algorithms. Results show that two DPT-compliant layouts with similar topologies but different decomposition solutions have composite scores of 0.66 and 0.71. The differences between the scores are caused by two factors: (1) the density imbalance between the two decomposition masks, and (2) the sensitivity to changes in feature-to-feature spacing due to the nature of the decomposition.

8327-45, Poster Session

Optimization of standard cell-based placement for self-aligned double-patterning process

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Self-aligned double patterning technology is a type of process that requests a large amount design effort, which might not be very design friendly. In the meanwhile, with the requirement of sub-20nm technology node, SADP is still an important candidate. To make the process valid for the designer to manipulate, a new set of design tools are extremely needed.

Based on the existing SADP decomposition method, we first study the properties of the SADP friendly standard cell library. For any cell, the most important patterns are the ones on the boundaries, which will have interactions with patterns in other cells. By studying the decomposition result, we can classify the boundaries into several types. Each of the boundary combination can have different effect on the placement.

There are many ways to generate an optimal SADP decomposition result for a small cell. The remaining problem of the SADP-aware placement

is how to keep the quality of the decomposition result once the layout is grown up, in which optimality control is no longer an easy job. With the information of the boundary conditions, we can keep several decomposition versions of the same cell and then use them to adjust the standard cell location and sequence. The optimality is guaranteed by a dynamic programming process and standard cell can be switched locally to keep the overall wire length unchanged. The overall process can be used as an effective placement process as well as an optimal cell-based SADP decomposition processes.

8327-46, Poster Session

Design-based methodology for defect prioritization

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Upon shrinking design rules, defects of small dimension may impact the chip functionality and performance. As a result, engineers are using higher sensitivity tools to inspect the Fab production (wafer inspection tool). The amount of reported defects is very large; typically several thousand defects per wafer are reported and only essential defects DOI (defects of interest) have to be monitored.

In the last decade several tools for defects prioritization and monitoring have been introduced and partially adopted by the industry (Spatial Signature Analysis, repeater analysis, OTF Classification, region based binning).

Recently, sophisticated tools combining manufacturing data and design information have been introduced and found to be efficient and adapted to high data rate processing (DBB -for layout and process variation analysis).

In this paper we will present a new method for high throughput defect filtering based on design information extracted around the defect position (defect footprint). We will discuss how the SVRF (Standard Verification Rule Format) language generally used in the context of DRC analysis is used as a generic approach to rank the defects based on their possible layout impact. To illustrate our method we will present data collected at one of the most advanced foundry.

8327-39, Session 5

Sub-20nm logic lithography optimization with simple OPC and multiple pitch division

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The CMOS logic 22nm node is being done with single patterning and a highly regular layout style using Gridded Design Rules (GDR). Smaller nodes will require the same regular layout style but with multiple patterning for critical layers. A line/cut approach is being used to achieve good pattern fidelity and process margin.[1] As shown in Fig. 1a, even with line patterns, pitch division will eventually be necessary.

Design-Source-Mask Optimization (DSMO) has been demonstrated to be effective at the 20nm node.[2] The transition from single- to double- and in some cases triple- patterning was evaluated for different layout styles, with highly regular layouts delaying the need for multiple-patterning compared to complex layouts.

To address mask complexity and cost, OPC for the "cut" patterns was studied and relatively simple OPC was found to provide good quality metrics such as MEEF and DOF.[3,4] This is significant since mask data volumes of >500GB per layer are projected for pixelated masks created by complex OPC or inverse lithography; writing times for such masks are nearly prohibitive.

In this study, we extend the scaling using simplified OPC beyond 20nm in small steps, eventually reaching the 14nm node. The same "cut" pattern is used for each set of simulations, with "x" and "y" locations for the cuts scaled for each step. The test block is a reasonably complex logic function with ~100k gates of combinatorial logic and flip-flops.

Experimental demonstration of the cut approach using simplified OPC and conventional illuminators at the 14nm node dimensions will be presented with comparison to the complex OPC result. MEEF can be measured experimentally. Lines were patterned with 193nm immersion with no complex OPC. The final dimensions were achieved by applying pitch division twice.[5]

8327-40, Session 5

Fast source independent estimation of lithographic difficulty supporting large scale source optimization

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Source mask optimization (SMO) technology allows improved process window and variability for small numbers of critical clips and canonical layout configurations, and is emerging as a tool for technology development. Large scale SMO has been demonstrated recently, but processing thousands of patterns still presents performance challenges. We describe a fast, source independent method to identify patterns which are intrinsically difficult. Since lithographic performance is dominated by the weakest patterns, typically only a few patterns of the represented layout determine the source; adding additional patterns to the optimization does not change the result, so we would like to predict the subset of patterns likely to determine the source. We call this prediction problem lithographic difficulty estimation (LDE). LDE ranking may be used as a filter after clustering, or to choose representative cluster elements. A fast polygon based FFT gives a complex spectral representation (diffraction order weights) serving as as input to several functions corresponding to different aspects of imaging difficulty: Near Nyquist-limit spatial frequency, iso-dense patterns, frequency and phase diversity, and 2D vs. 1D. Each term contributes to an overall weighted formulation of estimated difficulty.

The method was validated by various approaches using synthetic and hand designed 22 nm patterns:

- Matching ranks provided by lithographic experts for a set of 2D metal patterns. Weights of the components of the LDE function were adjusted to improve the conformity of the sort order to expert judgment.

- With a ranked most difficult 10% subset of 1000 synthetic contact patterns (240 nm) , we used joint optimization to design a source, then performed process window simulation to estimate common process window (CPW) (Fig 1). We score within 5% of CPW metric obtained using all patterns as input to joint optimization. Using the 10% lowest ranked subset did not achieve the target depth of focus and degraded CPW 15%. Using a 10% random draws misses DOF target and degrades CPW 7% on average. Combining clustering with LDE representative element selection gave a CPW within 4% of the full set, combining coverage and possible interaction of weak and stronger patterns. It is shown to be robust as compression ratios are decreased; that is, the patterns from higher compression ratio are a proper subset of patterns selected with lower compression ratio.

- Using highest LDE rank to choose representative patterns after clustering, we show 79% reduction in ORC errors compared to a previous SMO source generated by joint optimization followed by spatial domain optimization from a few hand chosen patterns. The data in this case were 1000 M2 synthetic patterns of 400 nm extent.

The execution time of the method is lightweight compared to methods based on evaluating the mask transfer function (MTF) of a pattern based on a specific source (Torres, 2009); this high performance also supports use of the method in interactive DFM scenarios, where designers or algorithms may obtain feedback on more lithographically friendly solutions.

Limitations where the method fails due to limits of OPC only correction, pattern interactions, and possible improvements to address these issues are described.

8327-41, Session 5

Generator of predictive verification pattern using vision system based on higher-order local autocorrelation

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Although lithography conditions, such as NA, illumination condition, resolution enhancement technique (RET), and material stack on wafer have been determined to obtain hotspot-free wafer image, those are still often found on a wafer. This is because the lithography conditions are optimized with limited variety of patterns. For 40nm technology node and beyond, it becomes a critical issue and causes not only the delay of process development but also the opportunity loss of the business. One of the easiest ways to avoid unpredictable hotspots is to verify enormous variety of patterns in advance. This, however, is quite time consuming and cost inefficient.

This paper proposes a new method to create a group of patterns to cover pattern variations in a chip layout based on Higher-Order Local Autocorrelation (HLAC), which consists of two phases. First one is "learning phase" and second is "generating phase". In the learning phase, geometrical features are extracted from actual layouts using HLAC technique. Those extracted features are statistically analyzed and define "feature space". In the generating phase, a group of patterns which represent actual layout features, are generated by correlating feature space and process margin. By verifying the proposed generated patterns, the lithography conditions can be optimized efficiently and dramatically reduce the number of hotspots.

8327-42, Session 5

Demonstration of an effective flexible mask optimization (FMO) flow

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The 2x nm generation of advanced designs present a major lithography challenge to achieve adequate correction due to the very low k1 values. The burden thus falls on resolution enhancement techniques (RET) in order to be able to achieve enough image contrast, with much of this falling to computational lithography. Advanced mask correction techniques can be computationally expensive. This paper presents a methodology with proof data that demonstrates a mask optimization flow and technology that enables access to advanced technique levels of performance but with the costs of much simpler methods. Brion Technologies has developed a product called Flexible Mask Optimization (FMO) which identifies hotspots, applies an advanced technique to improve them, performs model based boundary healing to reinsert the repaired hotspot cleanly (without introducing new hotspots), and then performs a final verification. ST Microelectronics has partnered with Brion to evaluate and prove out the capability and performance of this approach.

The results shown demonstrate improved performance on 2x nm node complex 2D hole layers using a hybrid approach of rule based sub resolution assist features (SRAF) and model based SRAF (MB-SRAF). The effective outcome is to achieve MB-SRAF levels of quality but at only a slightly higher computational cost than a quick, cheap rules based approach.

8327-43, Session 5

Full-field lithographical verification using scanner and mask intrafield fingerprint

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Full chip verification has become a key component of the Optical Proximity Correction over the last decade. Full field verification to catch the cross-field effects based on scanner information becomes more important in lithography verification. Lithographic Manufacturing Check (LMC) performed on Brion Tachyon's engine, which is the industry reference tool, now provides the capability to predict wafer CD variations across the entire field through process windows. LMC is catching and reporting weak lithographic points having small process windows or excessive sensitivities to mask errors based on the simulation from models with ASML scanner specific parameters.

ASML scanner intra-field information such as Dose, Focus, Flare, Illuminator Map, Aberration files or Mask Bias Map are integrated into the LMC run to create an across-field verification and can improve the accuracy of the prediction at different field locations. This run could then be compared towards a reference LMC result which does not have any scanner specific data.

Scanner information has been loaded into the LMC model by using the Scanner Fingerprint File (SFF) functionality. Various across field LMC runs with realistic scanner information have been then performed and compared to identify critical design hotspots or scanner drifts. Hotspots are then measured on silicon with Scanning Electron Microscopy (SEM) on a matrix product to correlate with simulation and to a ranking of Intrafield parameter contribution

8327-44, Session 5

Pattern selection in high-dimensional parameter spaces

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The calibration of models for OPC and lithography process simulation is done using experimental data from printing large number of patterns and measuring the results. Reducing the number of patterns used in calibration without compromising simulator accuracy and stability is important to reduce metrology requirements and calibration turn-around time.

A well accepted approach is based on ensuring that the patterns provide a good coverage of an image parameter space (IPS): Here, the aerial images of the patterns are characterized by a number of image parameters, such as Imin, Imax, curvature, slope and image density. Each image is represented by one point in the n-dimensional space spawned by these parameters. Patterns are assumed to be similar and redundant for calibration if their points are close to each other in IPS. A pattern selection using the IPS can be done, for example, by selecting one representative pattern from each region using a grid based approach. Techniques such as Principal Components Analysis (PCA) can further reduce the dimensionality of the parameter space -because of the "curse of dimensionality" for larger n where no two images are close to each other. Unfortunately, the reduction of an image with thousands of different pixel intensities to a small number of parameters causes a loss of important information, sometimes resulting bad pattern selections.

In this paper, we show that an IPS based pattern selection works well for certain interpolation based simulation models. In essence, it works well if closeness in IPS is predictive for closeness in the resulting pattern, and - more importantly - if a large image difference will lead to large

distances in IPS. We show that this generally is the case for certain interpolating simulation models, but not necessarily for physical models. We propose a statistics based method that can handle IP-spaces with large dimensionality n, in principle allowing to use each pixel (n>>1000) as an individual parameter. The results from a prototype application of the method are discussed.

8327-19, Session 6

Design and manufacturability tradeoffs in unidirectional and bidirectional standard cell images in 14nm

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Regular design methodologies, local interconnects, multiple patterning processes and fin-based devices are enabling scaling to the 14 nm node. With the adoption of these new technologies it becomes necessary to rethink the conventions followed in standard cell library design that proved successful in the past. In this paper we have studied the interaction between standard cell library design and pattern transfer techniques in the 14nm node. Results of this work have identified a limited set of layout constructs which are needed for manufacture-able and efficient library design, with special emphasis on unidirectional BEOL standard cell libraries.

Bidirectional, unidirectional and fixed pitch BEOL standard cell images have been created and studied on the IBM 14nm FINFET based process. Even though design technology co-optimization (DTCO) revealed that the 14nm process is more amenable to unidirectional standard cell image design than its precursors, still a competitive unidirectional standard cell image required the following major changes compared to a bidirectional standard cell image: i)the transistor gates were contacted on the outside, ii) the power and ground were run inside the cell and iii) local interconnect was used to connect NMOS and PMOS networks.

As part of our holistic standard cell image design process we have considered physical design (or design integration) issues like pin access, power rail robustness and conflict-free coloring of multi-patterned BEOL levels. Standard cell image design results indicate that a unidirectional standard cell image has nearly the same active fin (or diffusion) efficiency as the bidirectional standard cell image, i.e. around 66% as seen in Figure 1. In order to compare the design-ability and manufacturability of the three classes of standard cell images we have also created a cell image evaluation framework. The framework starts with a medium sized library as input and performs the timing characterization of the cells. It proceeds with a real block design implementation using an automated commercial design flow (adapted to 14nm) to compare the design efficacy of the various standard cell images. Pattern construct counts and litho simulations demonstrate the superior manufacturability of unidirectional standard cell libraries. Preliminary construct count results as seen in Figure 2 reveal more than an order of magnitude fewer constructs on the M1 level for a unidirectional standard cell library as compared to an extremely regular bidirectional library. Thus the cell image evaluation framework would help identify patterning tradeoffs for an effective standard cell image design.

8327-20, Session 6

Design rule driven source mask co-optimization methodology for sub-20nm logic and SRAM

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Our study focuses on Back End of Line (BEOL) DRs optimization because BEOL includes a lot of critical DRs related to scalability for metal and via. The most critical DRs in metal layer are Tip to Tip (T2T) space and Tip to Side (T2S) space because T2T and T2S space are limiting scalability and routability for BEOL. However, as T2T and T2S become smaller as PW also becomes smaller. In our experiments, we show that through co-optimization of DRs, source and mask can improve 7% scaling of T2T and T2S DRs without reducing of process window. For via layer, the most critical DR is via to via (V2V) space and have to consider diagonal direction since via is located between bottom and upper metal overlap area orthogonally. It is important that reduce V2V space on diagonal direction because supposed that reducing metal pitch is available but cannot support V2V space on diagonal direction those does not have any improvement for routability. Our experiments show that 6% scaling improvement of V2V space on diagonal direction. We get to the conclusion which DRs optimization with SMO allow that improve scalability, PW and routability without any other process development at sub-20nm technology node.

8327-21, Session 6

A novel methodology for triple/multiple-patterning layout decomposition

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Double patterning (DP) in a litho-etch-litho-etch (LELE) process is an attractive technique to scale the K1 factor below 0.25. For dense bidirectional layers such as the first metal layer, however, density scaling with LELE suffers from poor tip-to-tip (TT) and tip-to-side (TS) spacing. As a result, triple-patterning (TP) in a LELELE process has emerged as a strong alternative. Because of the use of a third exposure/etch, LELELE can achieve good TT and TS scaling as well as improved pitch scaling over LELE if further scaling is needed.

TP requires the layout to be decomposed into three different masks. In common practice, layout decomposition is converted into a graph coloring problem, where nodes represent layout polygons and edges represent same-color spacing violations. Layout decomposition is challenging for DP and it is even more challenging for TP.

In this paper, we propose a novel method that performs TP layout decomposition that uses existing methodologies and algorithms developed for DP decomposition. Our TP decomposition method maximizes the use of stitching (among all three masks) to result in the least number of coloring conflicts. The proposed method is also scalable and can be used to perform layout decomposition for multiple patterning with k-colors (with k being greater than or equal to 3). We verify the method on 20 and 14nm layouts and obtain conflict-free coloring for almost all layouts and a modest number of conflicts in the case of extremely dense layouts.

8327-22, Session 6

Overlay, decomposition, and synthesis methodology of hybrid self-aligned triple and negative tone double-patterning

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A negative-tone SADP (nSADP) process can be accommodated in a SATP (self-aligned triple patterning) process by printing wider mandrels such that the left space for the second spacers is reduced and only one line structure is formed by merging neighboring spacers together. Two different layout design strategies need to be applied to SATP and nSADP regions separately. In addition to design flexibility and pitch reduction, a 3-mask SATP mandrel recession (SMR) technique is proposed to use a lateral undercut/recession process to separate the mandrel edge from the line ends of the second spacers. In this manner, the overlay requirement of the final pad layer can be relaxed. We shall discuss several 2-D pattern decomposition and synthesis techniques based on mandrel & spacer engineering: shape symmetry based patterning, lateral protrusion for line ending, dummy aided patterning, mandrel recession to relax overlay requirement, etc. These techniques may open the opportunities to remove some strict design limits posed by 1-D gridded layout.

8327-23, Session 6

Computational lithography work flows and design rule exploration automation

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Lithography development has become extremely computationally intensive. For a particular technology node being developed, it is critical to determine the optimum source and OPC/RET for each layer. In this paper we present a flexible new computation system for automation of source, OPC and RET optimization of advanced lithography layers. Of course, before determining the optimum source/RET/OPC of any layer, it is equally critical to determine the design rules which can be manufactured at a particular technology node. The design rule computational lithography problem is a superset of the source/OPC/RET optimization problem. With an automated methodology, time for process development can be reduced dramatically if a process development engineer can determine the design rules through accurate, automated simulation of the entire flow. This paper further provides examples of the determination of optimum design rules for a 14nm process, through the use of a computational lithography Design Rule Exploration (DRE) flow inside the flexible computation system. The optimum design rules have been determined by utilizing user defined filters of the computational results, such as CD variation metrics, process window metrics, etc.

8327-24, Session 7

Thickness-aware LFD for the hotspot detection induced by topology

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With the advancements in technologies as 32nm node & below, semiconductors manufacturing has been relying more on fine patterning. So, precise lithographic simulations for the prediction and detection of process defects induced by lithography are getting more required. With the inevitable increasing in number of pattern failures due to the tighter process margins, Litho simulation by litho friendly design (LFD) at the design stage become a necessity prior to wafer processing. As a result, low fidelity patterns due to process variations can be detected and eventually corrected by designers as early in the tape out flow as right after design rule checking (DRC); a step no longer capable to totally account for process constraints anymore. This flow has proven to provide a more adequate level of accuracy when correlating systematic defects as seen on wafer with those identified through LFD simulations. However, at the 32nm and below, still distorted patterns caused by process variation are unavoidable. And, given the current state of the defect inspection metrology tools, these pattern failures are becoming more challenging to detect. As one of the contributors to process variation, intra-chip topology has become a significant factor to define a process margin, and is one that can, through chemical mechanical polishing (CMP) simulations, be reflected into LFD analysis. A simple focus shifting from the nominal plane is usually sufficient factor to account for these distorted patterns by localized topology variations. In this paper, concurrent lithographic & CMP process variations, we study the chip level systematic topology as a determining factor in the overall process margin calculations.

In the framework of this paper, a methodology of advanced process window simulations with awareness of chip topology is presented. This method identifies the expected focal range different areas within a design would encounter due to different topology. As a result, respective defocus models are used to drive the LFD simulations and detect CD (Critical Dimension) variations in printing features. Identified hotspots are then compared to real wafer results, and a practical use of these results for systematic failure analysis and pattern correction are finally concluded.

8327-25, Session 7

The complexity of fill at 28nm and beyond

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The need for FILL in design layouts began as early as 0.25um and was primarily driven by the introduction of CMP processing. In today's designs at 28nm, there are many factors driving modern FILL technology such as timing, stress, implant, thermal anneal, etch, deposition, and resist developing just to name a few. The effects of FILL layout affect the entire semiconductor manufacturing system, from mask generation to final test. Additional complexity comes during the design phase, as the rules for compound multi-layer fill shapes are complex and difficult to meet. Run time for automated tools and output file size for FILL layers have become very large, causing inefficiencies in final tape release and post-tape out flow.

A study of test case layouts for the 28nm technology reveals some statistics which need to be analyzed for improving the FILL tools. As expected, the number of FILL shapes required continues to increase exponentially over each new technology node. A large percentage of shapes are now small enough to require OPC treatment during mask making. Spacing between fill shapes and signal routing is approaching 2x metal pitch. Electro-Chemical Plating (ECP) requirements do not allow for any small open areas, so all open surface area of the layout is affected by FILL.

To alleviate the complexity of creating FILL during layout, EDA has provided much needed enhancements to automatic fill based placement tools. These include cell based filling outside of the router for enhanced run time performance, and array based compression to reduce file size output. Studies of test cases show a significant improvement over older filling tools, and a more uniform layout with respect to distribution of FILL also being achieved. A comparison of results over several styles of test case will be presented. Several foundries have reported a significant increase in circuit performance and reliability when more enhanced fill methodologies are implemented. Today's tools are net aware, mitigating timing impacts to the layout.

In future technologies, research is showing that these problems will continue to get worse. During 20nm development cycles, new issues such as double patterning and pitch based layout bring new challenges. New EDA technology addresses these issues by creating fill which is correct by construction during the placement phase. Cell construction for

fill with pre-OPC based features are now available with little cost to FILL run time. This has been demonstrated at AMD in enhancing the design flow. These new features help the post-tape out flow at the foundry mask house by eliminating long processing steps required for RET. This is important in keeping TAT for initial designs as short as possible.

Additionally, the modern automated FILL tool is capable of adding passive and active circuitry cell layout to improve DFM characteristics of final layouts. Using a FILL based approach to solving these types of issues greatly enhances the solution, as distribution and density of these cells can be accounted for during the automatic generation of the placements.

FILL solutions continue to be an evolving technology provided by EDA to the design community. This type of EDA R&D in collaboration with foundries and design houses is critical for the continued success of the semiconductor fabrication industry.

8327-26, Session 7

Utilizing chemical-mechanical polishing models in IC design evaluation and mask sign-off flows

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Chemical Mechanical Polishing (CMP) is an essential process in semiconductor manufacturing. It is known to suffer from pattern dependencies and result in dishing and erosion, which can lead to potential yield problems. These problems include copper pooling and excessive copper loss [1 - 3] and become very significant as integrated circuit feature sizes continue to shrink. They can therefore no longer be neglected in advanced node designs for optimal yield and performance. In recent literature, [4] - [6] have presented model development methods and [4] has presented ways to reduce hotspots. However, there needs a better understanding of 1) how design rules interact with such hotspots, 2) how such models can be used to improve inductor designs in particular, and 3) how to determine hotspot criteria using silicon test structures.

In designing a chip, design rule checks are often followed rigorously to get the designs to high yield and meet performance specifications. However, following design rules does not guarantee that the resulting designs will be free of CMP induced hotspots and will meet performance specifications. In order to ensure that a design will yield and meet performance specifications, and to reduce design cycle time in general, it is essential that accurate CMP models be used in conjunction with design rules. Accurate CMP models are useful in screening designs very early on in the design cycle to detect potential hotspots and other CMP related failures. In addition, these models are useful in screening the full designs before a mask is made. Once hotspots are detected, designers would then be able to deploy a host of tools to fix the problem areas and optimize their designs to meet and possibly surpass specifications.

In this paper, we describe a method to screen designs for CMP induced hotspots in a mask sign-off flow. This paper advances state of the art in the following ways:

1) We provide a methodology to compare design rules with hotspots using CMP models.

2) We present results on using CMP models in the design of fills for inductors.

3) We present test structure silicon data for tuning hotspot criteria.

Item 1 targets deciding on how to waive some design rules using CMP models, or enforce additional restrictions using the models. Using item 2, we optimize inductor designs. Finally, using item 3, we tune our hotspot rules. Our silicon data is based on 40 and 28 nm technologies.

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8327-27, Session 7

In-design process hotspot repair by pattern matching

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As patterning for advanced process become more challenging, designs must be more process-aware. The traditional approach of running litho simulation on designs to detect process hotspot is prohibitive in terms of runtime for designers and also requires release of highly confidential process information. Therefore a more practical approach is required to make In-Design process-aware methodology affordable in terms of maintenance, confidentiality and runtime. We chose a pattern-based approach for process hotspot repair (PHR) because it captures very well the manufacturability challenges without having to release sensitive process information and is fast and well integrated in the design flow. By receiving the information of process weak patterns (caused by CMP, etch and other processes as well as litho) with regular interval and updating pattern library promptly, an immediate feedback can be performed on even the very next design. As compared to the pattern matching flow described in other papers [1][2][3][4], the patterns used here are derived from systematic analysis of actual silicon failure data rather than through model-based printability checks. Further, the flow described in this paper leverages the mature lithography fixing capabilities in the router to automatically clean up not just the small number of critical hotspot locations but also the large number of yield-sensitive layout locations, improving the overall manufacturability of the design. This paper will provide some data on overall performance and on manufacturability before and after hotspot repair.

We used pattern classification to define the library of patterns because it automatically collapses similar patterns in a pattern family defined by a pattern with some edge fuzziness. Pattern classification provides a superior coverage than exact pattern matching and reduces the number of patterns. The pattern database can then be used to identify such challenging patterns during design so layouts coming to manufacturing are more process-friendly. From the designer point of view, litho checking can be seen as additional burden and task that can delay tape-out; therefore, it is important to make these process checks as seamless as possible. Our approach leverages the integration of pattern matching in digital implementation flows. With the same pattern database, digital design teams can detect and fix process hotspots during the design phase and concurrently achieve their timing, area and manufacturability goals. Through the proposed flow, designers can get their tape-out with high confidence about the absence of known hotspot patterns. The gains from PHR have been validated in 32nm silicon products.

8327-28, Session 7

Clean pattern matching for full-chip verification

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(Japan)

Layout verification to guarantee no hotspots in a chip is essential in a current and future generation. The layout verification generally uses a lithography simulation (Lithography Compliance Check: LCC) and it requires a lot of calculation time as a circuit size becomes larger. In order to reduce the calculation time, several methods have been discussed so far and a "pattern matching" is one of the candidates. A current general flow of the pattern matching for the layout verification consists of the following three steps; (1) define hotspots on preceding LCC and/or experimental data (2) store the hotspots into a library (3) verify whether the same patterns exist in layouts or not on a pattern matching method with the hotspot library (Hotspot matching). However the above mentioned hotspot matching cannot find unrecognized hotspots so that we have to run LCC to find such unrecognized hotspots on the areas where the hotspot matching does not find any hotspots. The matched areas occupy small parts of a chip because designers run LCC every time they draw layout patterns. Therefore LCC time cannot be reduced because LCC need to be run in the most of the chip area even after the hotspot matching.

In this paper, we propose a clean pattern matching method that uses a "clean pattern library". Clean pattern matching is a method of defining non-hotspot patterns (clean patterns) in a chip. A layout verification flow with the clean pattern matching is the same as the hotspot matching except defining clean patterns. The verification flow is; (1) define clean patterns on preceding LCC and/or experimental data (2) store the clean patterns into a library (3) verify whether the same patterns exist in layouts or not and eliminate the matched patterns from the LCC area. The important point for the first step is to consider effects of neighboring patterns. Simulation results (wafer shape) are different if the neighboring patterns are different. This means if we do not consider neighboring patterns, a clean pattern may become a hotspot when the pattern is placed in a different location in a full chip layout because different neighboring patterns induce different simulation results.

We will discuss the detailed flow on the clean pattern matching method and experimental results of layout verification in our 40nm system LSI designs at the conference.

Conference 8328:
Advanced Etch Technology for Nanopatterning

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8328-01, Session 1

Extreme-UV lithography for semiconductor manufacturing at <20 nm generations

A. Yen, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan)

No abstract available

8328-02, Session 1

Advanced plasma etch technologies for nanopatterning

R. Wise, IBM System and Technology Group (United States)

Advances in patterning techniques have enabled the extension immersion lithography from 65/45nm through 14/10nm device technologies. A key to this increase in patterning capability has been innovation in the subsequent dry plasma etch processing steps. Multiple exposure techniques such as litho-etch-litho-etch, self-aligned double patterning, line/cut mask and self-aligned structures have been implemented to solution required device scaling. Advances in dry plasma etch process control, across wafer uniformity and etch selectivity to both masking materials and have enabled adoption of vertical devices and thin film scaling for increased device performance at a given pitch. Plasma etch processes such as trilayer etches, aggressive CD shrink techniques, and the extension of resist trim processes have increased the attainable device dimensions at a given imaging capability. Precise control of the plasma etch parameters affecting across design variation, profile stability within wafer, within lot, and across tools have been successfully implemented to provide manufacturable patterning technology solutions. IBM has addressed these patterning challenges through an integrated Total Patterning Solutions team to provide seamless and synergistic patterning processes to device and integration internal customers. This team works directly with industry leading suppliers and advanced laboratories through Joint Development Projects to pioneer advanced plasma based solutions for pattern transfer steps.

For two decades IBM and the semiconductor industry plasma based dry etching processes have operated in predominately one of two regimes. Multiple frequency capacitive reactors for high ion energy dielectric applications and more strongly decoupled (inductive/ECR) reactors for lower ion energy conductor applications. Symmetric chamber design, orthogonal uniformity tuning (radial tuning of power, flow, temperature) and hyper control of process variables (surface and wafer temperature, plasma volume, applied bias power) have all been employed to incrementally extend the capability of these source designs. The demands placed on pattern transfer are now exceeding the fundamental capability of mainstream plasma reactor technology. High energy electrons generated to provide adequate dissociation and ion flux cause charge separation of masking features and exceed process assumptions for line edge roughness and micro-trenching driven stop layer selectivity. This charge separation is particularly problematic for profile shaping in 3-dimensional device structures and high aspect ratio trench etching for embedded memory. Dispersion in the ion energy distribution limits thickness scaling of etch stop layers and depth control, particularly for 3-dimensional devices, limits shape control of spacers used in self-aligned double patterning and for gap fill assisting etching processes, and limits mask materials and thickness scaling. IBM has applied our technology development expertise to drive next generation plasma process equipment and overcome limitations in nonequilibrium plasma generation and ion energy dispersion.

This paper will discuss the innovative techniques pioneered at IBM and our development alliance partners to extend imaging technology through plasma etch processes and potential breakthroughs to continue IBM leadership in patterning capability.

8328-03, Session 1

Improving patterning capability through etch

R. A. Gottscho, K. J. Kanarik, J. W. Cossins, Lam Research Corp. (United States)

Photolithography and Etch historically have been viewed as separate fabrication steps, each independently integrated into the wafer manufacturing process. However, as we enter the nanoelectronics age, it is increasingly necessary to use an integrated patterning approach in order to exploit every opportunity to improve overall patterning fidelity. In this talk, I will review current practices and future opportunities for a combined Etch & Photolithography approach. For example, Etch technology is capable of shrinking critical dimension (CD), allowing the lithography system to print features larger than the target size, thereby relaxing lithography tool requirements. Pitch doubling schemes are now routinely used, and these introduce challenges in controlling line roughness and CD uniformity (CDU). Etch plays a critical role in pitch doubling by mitigating the resulting line roughness, thereby relaxing imaging requirements. With the introduction of pitch quadrupling schemes, the role of etch in reducing line roughness will become even more critical. However, there are fundamental limitations to improving roughness, and these will be discussed. Finally, I will discuss the increasing focus on understanding and compensating for non-uniformity in CD, feature profile and other important patterning errors introduced by both etchers and Lithography systems.

8328-04, Session 1

Plasma etch challenges and solutions for advanced patterning

T. B. Lill, Applied Materials, Inc. (United States); Y. Zhang, Taiwan Semiconductor Manufacturing Co. Ltd. (Taiwan); M. Shen, Applied Materials, Inc. (United States); O. P. Joubert, CNRS/LTM (France); B. Schwarz, Applied Materials, Inc. (United States); N. Posseme, CNRS/LTM (France); O. Luere, Applied Materials, Inc. (United States); Y. Xiao, Taiwan Semiconductor Manufacturing Co. Ltd. (United States); L. Vallier, CNRS/LTM (France)

Advanced patterning will require atomic level resolution. This level of performance can only be obtained with a deep understanding of the fundamental mechanisms driving CD control, line edge roughness, and microloading. Novel approaches for uniformity tuning with decoupled ICP source technology have fundamentally improved center to edge tuning capability. Much progress has been made in the understanding of line edge roughness. We will present the current state of knowledge about the interaction of CW and pulsed plasmas with resists with respect to line edge roughness. Microloading will be discussed from a plasma chemistry point of view.

8328-05, Session 1

Nanopatterning impacts on devices for advanced technology nodes

R. Jammy, SEMATECH Inc. (United States)

No abstract available

8328-07, Session 1

Ultimate top-down processes for future nanoscale devices

S. Samukawa, Tohoku Univ. (Japan)

For the past 30 years, plasma process technology has led in the efforts to shrink the pattern size of ultralarge-scale integrated (ULSI) devices. However, inherent problems in the plasma processes, such as charge build-up and UV photon radiation, limit the process performance for nanoscale devices. To overcome these problems and fabricate nanoscale devices in practice, we have proposed damage-free neutral-beam process. In this presentation, I introduce our developed damage-free etching, structure-designable deposition of super low-k SiOC film and low-temperature Si oxidation (thin SiO_2) processes using neutral beams and discuss the actual applications of neutral beam processing for future nanoscale devices (such as, Fin-MOSFET, and Quantum Dot Solar Cell). Neutral beams can perform atomically damage-free etching, deposition and surface modification. Then, the neutral beam process can precisely control the atomic layer chemical reaction and defect generation. This technique is a promising candidate for the nano-fabrication technology in future nanoscale devices.

8328-30, Session 1

Plasma etch transfer of self-assembled polymer patterns

C. T. Black, Brookhaven National Lab. (United States)

No abstract available

8328-06, Session 2

Patterning enhancement techniques by reactive ion

M. Honda, Tokyo Electron Miyagi Ltd. (Japan); K. Yatsuda, Tokyo Electron Ltd. (Japan)

As device features were scaled, resolution enhancement techniques (RET), such as phase shift mask and customized illumination, were introduced in lithography. Although it is only lithography which can define the pitch, etch has been compensating critical dimension (CD) by trimming at the gate level in order to obtain the required transistor performance. After 193-nm lithography was introduced into manufacturing, line edge roughness (LER) and line width roughness (LWR) became serious issues because 193-nm resist has low plasma tolerance. Additionally, the depth of focus (DOF) is so small that the 193-nm resist does not remain thick enough after etch. These issues will become more significant with EUV resist. In the meantime, contact mask is always marginal. Since positive tone resist is dominant at this moment, over dose may be preferred so that scum and/or exposure defects decrease. However, this technique often contributes to CD enlargement and contact-contact bridging. This paper introduces patterning enhancement techniques (PET) by reactive ion etch (RIE) to solve the above issues.

Plasma tolerance of resist is determined by the chemical structure of resin. Thus, it is necessary to deposit a protective layer or modify the chemical structure on the surface. We propose a modification technique by hybrid DC+RF RIE because the deposition technique is restrained by the required CD. The DC+RF hybrid RIE is a capacitive coupled plasma etcher with a superimposed DC voltage. A high negative DC bias is applied to the upper electrode. Secondary electrons emitted from the electrode surface under intense ion bombardment, are accelerated in the sheath and consequently injected into the bulk plasma, forming a ballistic electron beam. In this paper, the mechanism of resist modification is discussed with results of exposure to the ballistic electrons. The results include various surface analytical techniques (SEM, FTIR, Raman, and SIMS). In consequence, etch resistance and LWR of resist were improved by applying novel plasma gas chemistry cure with DC superimposed (DCS) plasma.

On the other hand, CD enlargement and contact-contact bridging require a deposition technique since CD needs to shrink and bridging potions need to be filled with polymer. It is also preferred that CD variation is minimized by the CD shrink technique. RIE cannot only etch but also deposit polymer onto the sidewall with sedimentary type gases, and it is well-known that RIE has a loading effect caused by a local depletion of reactive species. We can take advantage of the CD loading effect principles of the polymer deposition on the sidewall so that CD variation originating from lithography is minimized. In order to put this technique to practical use, it is very important to select an appropriate gas chemistry, which can shrink CD and etch BARC, and simultaneously control the shape of polymer deposition on the sidewall of the photoresist. By applying this new technique, we successfully fabricated a 35-nm hole pattern with a minimum CD variation.

8328-09, Session 2

Patterning of device structures for 40-80nm pitch and beyond

S. U. Engelmann, R. M. Martin, R. L. Bruce, H. Miyazoe, N. C. M. Fuller, W. S. Graham, E. M. Sikorski, M. Glodde, M. Brink, J. J. Bucchignano, D. P. Klaus, E. Kratschmer, M. A. Guillorn, Y. Zhu, IBM Thomas J. Watson Research Ctr. (United States)

Short Channel Effects (SCE) and variability in the threshold turn on transistor voltage (Vt) are the major issues limiting the use of planar device geometries for future technology nodes. Alternative device integration schemes are currently being evaluated to test the impact on SCE and Vt variability and thereby enable continued device scaling for future technology nodes. Some of the device candidates that are currently being examined include planar devices, FinFETs, Trigates and Nanowires (gate all around device). The gate formation on these advanced, multi-gated devices imposes completely new challenges on the plasma etch conditions, which translates to the demand of controlling the plasma etch rates and selectivities in a second (and a third) dimension. Electron beam lithography has been proven to be a very valuable tool to explore plasma processing at device sizes currently unattainable by state-of the art optical lithography.

One of the major limitations impeding aggressively scaled pitches (40nm and beyond) includes the mechanical failure of the patterning material after transfer into the subsequent material stack. While the impact of patterning material and process conditions has been illustrated previously, further process optimization by various pre- and post-treatments has shown to provide a robust process down to 40nm pitch. A systematic study of the important parameters will be shown. Extensions of the patterning work by sidewall image transfer and directed self assembly will be addressed and issues will be discussed.

The optimized patterning module has been applied to the fabrication processes of the devices technologies currently under examination. The execution of the Trigate device flow has proven extremely challenging. This challenge is primarily due to the fabrication of the gate while preserving the Si fin that has no hardmask to prevent plasma damage and erosion. Low electron temperature (Te) etch solutions have shown the most promise to meet the higher demands of non-planar device candidates. Further, we have demonstrated the fabrication of gates above a fin of varying dimensions for SRAM cells down to 0.025um2 and fin width down to 3nm .

As mentioned, another significant challenge is the spacer process, where SiN needs to be removed from the fin sidewall, while keeping it on the gate sidewall to prevent device shorts. Extremely high precision is needed to form a SiN Spacer without damaging exposed silicon and/or silicon oxide. This is even more challenging for Trigate devices, where the plasma process needs to be able form the spacer on the gate sidewall, but not the fin sidewall. At the same time the exposed oxide and silicon surfaces have to withstand the extended over-etch necessary to form the spacer. Multiple etch gas chemistries have been evaluated and their impact on etch rates and selectivities with target of spacer application has been evaluated. We observed that by using a novel gas chemistry, a true anisotropic nitride spacer profile can be obtained with high selectivity to the exposed oxide and silicon. This novel spacer solution provides a clear advantage over known processes, enabling scaling of spacer thickness without compromising device performance.

8328-10, Session 2

Plasma etch challenges for porous low-k materials for 32nm and beyond

C. B. Labelle, R. P. Srivastava, GLOBALFOUNDRIES Inc. (United States); Y. Yin, J. C. Arnold, IBM Corp. (United States); M. Ishikawa, Toshiba America Electronic Components, Inc. (United States); Y. Mignot, IBM Corp. (United States); A. Darlak, K. Zhou, Applied Materials, Inc. (United States); Y. Zhou, Applied Materials. Inc. (United States); J. T. Pender, Applied Materials, Inc. (United States)

The challenges facing back-end-of-line (BEOL) etch as technology nodes progress are becoming increasingly difficult as the challenges due to shrinking dimensions are compounded by the challenges from new materials integration. As critical dimensions decrease, key dimension-related etch challenges include CD control, aspect ratio of trench litho film stacks, RIE lag, and LER. The inclusion of low k dielectrics, including porous materials (k ≤ 2.55), requires the etch to consider the sensitivity of the films to compositional modification (i.e., dielectric damage), polymer interactions with the pores (i.e., rough etch front), and diffusion effects possible with porous materials. These materials issues have driven the bulk of the novel etch development in recent years. However, as the minimum pitch reaches sub-100nm and then goes even further, new interactions of the materials with this critical dimension need to be considered. The ability of low k materials to be patterned at the aspect ratios required without losing structural integrity will be one of the key challenges for future technologies' success. This challenge is independent of the patterning scheme used (via-first-trench-last vs. trench-first-via-last), although there are also challenges unique to each patterning scheme. In particular, while trench-first schemes can enable use of self-aligned via (SAV) patterning, there are a host of new patterning challenges associated with SAV that now need to be considered. In addition, double patterning of BEOL trenches is now a reality, with via double patterning closely following. The implementation of double patterning schemes in the BEOL further increases the complexity of the patterning process and raises some unique materials issues. Within the trench double patterning, there is increased focus on the same-color tip-to-tip and tip-to-side rules, requiring etch to focus on CD control capabilities not only for the line CD but also for the line end, and line ends have always been a key challenge for k ≤ 2.55 etching, where metallization is most sensitive to dielectric damage structural effects. This paper will review the key etch challenges as a function of dimensions vs. materials and highlight where their interactions which will drive future work.

This work has been supported by the independent Bulk CMOS and SOI technology development projects at the IBM Microelectronics, Div. Semiconductor Research & Development Center, Hopewell Junction, NY 12533.

This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

8328-11, Session 2

Toward new plasma technologies for 22nm gate etch processes and beyond

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Since more than 30 years, CW plasmas have been used in the microelectronics industry to pattern complex stacks of materials involved in Integrated Circuit technologies. Even if miniaturization challenges have been successfully addressed thanks to plasma patterning technologies, several fundamental limitations of the plasmas remain and are limiting our ability to shrink further the device dimensions. In this work, we analyze the capabilities of synchronized pulsed ICP technologies and their potential benefits for front end etch process performance.

In the first part of this talk, the impact of duty cycle and frequency on radical densities is analyzed. Our results show that decreasing duty cycle in ICP plasmas generates less fragmentation of feed gas stock molecules compared to CW plasmas (analyses of BCl_3, Cl_2, SF_6/CHF_3), leading in final to a decrease of the radical density in the plasma. The impact of the same parameters on the ion energy distribution function is also analyzed using a dedicated analyzer mounted on the 300 mm cathode. Experiments show that pulsing gives access to lower ion energy bombardment conditions than in CW plasmas.

On a process point of view, we have studied the etching of ultra-thin layers (SiO_2, HfO_2, SiN spacer) involved in front end processes and investigated what synchronized pulsed plasmas could bring to substrate damage and selectivity issues. We have shown, for example, that silicon recess, generated during the overetch step of an HBr/O_2 gate etch process can be very significantly reduced when going from continuous waves to synchronized pulsed plasma conditions (20% duty cycle). During HfO_2 etching in polymerizing BCl_3 plasmas pulsed plasma conditions can be found where no recess to silicon is generated and no damage to the underlying silicon is measured by XPS consistent with the decrease in ion energy generated in pulsed plasmas. Similar results on nitride spacer etching will be also presented.

Interaction between plasmas and photoresist is also another area of interest where synchronized pulsing can be beneficial. Indeed, for front end as well as back end applications, multilayer hard mask schemes are mandatory. Current 193 nm resists are therefore used to open a silicon containing layer (imposed by the 193 nm lithographic step) followed by patterning hard mask layers (typically SiO_2 and amorphous carbon layers). Current CW processes to open silicon containing layers use fluorocarbon based plasmas lead to roughness and striations being attributed to the stress induced by the fluorocarbon layer in interaction with the photoresist. Going to synchronized pulsing technology allows an increased selectivity to the mask thanks to molecular ion formation together with less fragmentation of the fluorocarbon feed gas stock, i.e less damage to the resist

Finally, the applications of Pulsed plasma technologies to the etching of the most advanced devices (FIN FET transistors and FD SOI devices) and their potential benefits will be discussed.

8328-12, Session 2

Key challenges in FEOL etch for 22 nm and below

P. L. Jones, C. B. Labelle, GLOBALFOUNDRIES Inc. (United States)

As the industry moves beyond the 32 nm technology node, the challenges facing patterning and integration teams are many and varied. The late arrival of a EUV patterning infrastructure necessitates the continued use of 193nm immersion lithography coupled with various

double patterning schemes. Each double patterning scheme has unique requirements and challenges. The selection of the double patterning scheme will depend on the unique lay-out requirements of each particular layer. The need for continuous Leff scaling inevitably results in serious SCE issues which can only be overcome by increasing process complexity. The need to enhance drive currents and sub threshold slopes with such restricted channel lengths has resulted in the need for 3-D transistor architectures such as FINFET and trigates where the gate is wrapped around a FIN. In an attempt to reduce the influence of Vt variability due to local channel doping fluctuations, fully depleted transistor devices (with undoped channels) over exceptionally thin SOI substrates (ETSOI) are also being actively investigated. Back-bias control is possible with this transistor architecture which is highly desirable for applications requiring variable Vt's and minimal off-state currents. These new transistor architectures obviously result in dramatic etch challenges. The severe topography seen in the FINFET device results in significant challenges in terms of selectivity to the FIN cap in the gate etch process. Spacer etch and MHK (metal-High K) removal etch from the FIN sidewalls are particularly challenging. FINFET's over SOI versus FINFET's on bulk Si require significant differences in their integration schemes which have implications to the etch processes. The gate etch processes used with ETSOI have very severe selectivity requirements due to the need to stop on an extremely thin SOI layer. The decision on whether a replacement gate (RG) or a gate-first approach is selected will drive the requirements of the etch processes. A gate-first approach often results in difficulties with MHK footing post gate etch due to the differing heights and compositions of the gate stacks in the PFET and NFET regions. This footing issue is particularly problematic near regions of STI or FIN topography and is frequently related to incompatibilities between the MHK material and the poly OE chemistry. The gate etch process with a replacement gate integration scheme has a requirement to etch poly Si stopping on an extremely narrow <10 A IL layer without punching through to the substrate. As reported in the literature for gate oxides <10-20A, a high selectivity HBr/O2 OE (over-etch) chemistry commonly used in the industry is often not successful in preventing punch-through into the substrate. Over-etch approaches which minimize oxygen diffusion through the IL layer are needed to prevent substrate punch-through. This is particularly important for gate etch with ETSOI where the recess requirements are more extreme. There have been numerous process and hardware solutions to this problem reported in the literature. One of the most promising solutions is a synchronous pulsing of the RF power. These issues will be reviewed in detail.

8328-13, Session 2

Etch challenges for 1xnm NAND flash

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In recent years, NAND flash technology node has shrunk below to 1x nm patterning with significant progresses of DPT (Double Patterning Technology) and SPT (Spacer Patterning Technology). Plasma etching processes involved in the fabrication of advanced NAND flash device become increasingly challenging. As critical dimensions decrease, controlling of micro-loading and pattern wiggling such as line edge roughness (LER) and line width roughness (LWR) has become key issues. In order to define the fine pattern, plasma etch process regime has been changed to lower pressure and to higher plasma density below sub 40 nm. However, below 20 nm, it seems that control of pressure and plasma density is not enough. In an effort to overcome these huddle, pulsing plasma etch technology has been evaluated for 1x nm node. By using pulsing plasma we have obtained improvement of etch selectivity and reduction of poly hard mask thickness. In this study, we have found that pulse applied etching as well as film stack optimization is remarkably effective to reduce micro-loading and pattern wiggling.

8328-14, Session 3

Plasma-polymer interactions for nanoscale patterning of materials

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We review chemical and morphological changes induced in selected model polymers and advanced photoresists during interaction with fluorocarbon/Ar plasmas, including ion-induced formation of a thin (~1 nm) dense graphitic layer at the polymer surface and deeper-lying modifications by vacuum UV irradiation. The picture of a possible fundamental mechanism of plasma-induced polymer surface roughness formation emerges from this work where polymer material-dependent near-surface modifications and changes in nanomechanical properties introduced at various depths by different plasma fluxes interact and produce surface roughness. We discuss how this understanding may be used to improve performance of polymer masks during plasma etching steps.

8328-15, Session 3

Plasma treatment to improve linewidth roughness during gate patterning

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With the decrease of feature size of large scale integrations, line edge/ width roughness (LER/LWR) is being recognized as a major concern in device manufacturing. Several experimental and modelling works indicated the harmful effects that LER or LWR may have on the voltage threshold shift, off-state leakage current in a typical MOSFET, or more advanced FinFET devices. For example the gate CD and 3 LWR requirements for the 32 nm technological node are 20 and 1.8 nm respectively while state of the art patterning techniques only allows 4-3 nm gate LWR at best. The origin of the LWR/LER of the final transistor gate is mainly attributed to the significant roughness of the photoresist pattern printed by the lithography step which is partially transferred into the gate stack during the subsequent plasma etching steps. One way to minimize the final gate LWR is to decrease the photoresist pattern LWR by applying post-litho treatments prior any plasma pattern transfer step. Another critical issue related to LER and LWR is to accurately estimate those parameters measured by metrology tools. As the LWR decreases and consequently the signal to noise ratio, extraction of the physical roughness value becomes even more difficult. The white noise of the metrology tool causes errors in LWR measurements, and one challenge is to determine the so called "unbiased LWR/LER" values

In the present study, we propose a simple and robust experimental protocol combining CD-SEM measurements at low integration frames and Power Spectral Density (PSD) fitting method for an accurate extraction of all roughness parameters (true LWR/LER, correlation length, fractal exponent) of any patterned materials, even photoresist degraded by the e-beam during SEM acquisition. Complementary roughness analyses are also performed using CDAFM to get information on the pattern profile and roughness evolution along the pattern height. CD-SEM and CD-AFM techniques have then been used to investigate

the impact of various resist post litho treatments (combining plasma exposure, vacuum ultra violet (VUV) light exposure, and annealing) on the photoresist LWR and profile. The benefits of the resist pre-treatments on both LWR and CD control after pattern transfer into the gate stack have also been investigated. Even if some specific treatments can improve the resist LWR before transfer, the subsequent plasma etching steps can degrade it and also induce a loss of CD control. This paper will show how to decrease the photoresist LWR down to 2.6nm using post litho treatment and how to transfer it into polysilicon gate without LWR and CD degradation.

8328-16, Session 3

The effects of plasma exposure on low-k dielectric materials

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Low-k dielectric films are subjected to varying fluxes of charged particles, photons and neutral particles/free radicals during plasma exposure. Each of these has the potential to produce various types of damage to the dielectric film such as trapped charge accumulation, changes in chemical and physical properties of the material and deterioration of time-dependent dielectric breakdown (TDDB) lifetime. To identify the types of damage produced by these species, two different systems were used: (1) a synchrotron radiation system as a pure vacuum ultraviolet (VUV) radiation source, and (2) an electron-cyclotron resonance (ECR) plasma system with a capillary-array window that can be used to separate photon from particle fluxes. Surface potential and C-V characteristics measurements are used to confirm the existence of trapped charges in the dielectric. With increasing VUV dose, an increase in the surface potential and, from the CV characteristics, a corresponding shift in flat-band voltage along with hysteresis appears. Hysteresis indicates the presence of mobile charges within the bandgap. Trapped charges can be depleted with UV-lamp exposure. VUV photons are responsible for trapped-charge accumulation within the dielectric, while ion bombardment results primarily in charge deposited on the surface of the dielectrics. The amount of charge accumulation depends on the UV curing process, the interfacial energy barrier and the dielectric porosity. For example, using different energy barriers between the dielectric and the substrate can result in less accumulated charge. For low-k dielectric films, during argon electron-cyclotron resonance (ECR) plasma exposure, both ion and photon bombardment increased the measured defect concentrations. Dielectric samples with a range of dielectric constants were examined showing that as the value of the dielectric constant was lowered, the defect concentrations were shown to increase significantly. Time-dependent dielectric breakdown (TDDB) was investigated as a function of photon/particle fluxes. Samples exposed to VUV photons or a combination of VUV photons and ion bombardment exhibited significant degradation in breakdown time. Under low-field stress VUV-exposed samples behave like unexposed samples whereas under high-field stress they behave like plasma-exposed samples. Samples exposed to VUV photons and ion bombardment showed more degradation in breakdown time in comparison to samples exposed to VUV photons alone. An equivalent-circuit model is developed which, once the circuit parameters are determined, can predict the photoemission response from dielectric materials under VUV irradiation. UV curing of low-k dielectric materials changes the response to plasma exposure substantially. In particular, depending on the material and process conditions, leakage currents in UV-cured dielectrics may be enhanced or decreased after plasma exposure compared with uncured dielectrics. X-ray photoelectron spectroscopy (XPS) shows a pronounced chemical shift after VUV exposure. Using a combination of XPS and Ultraviolet Photoelectron Spectroscopy the bandgap energy and the locations of defect states of a wide range of low-k dielectric materials may be determined.

Nanoindentation measurements after VUV/plasma exposure show that both plasma and VUV exposure act to increase the elastic modulus of the dielectric without affecting its hardness.

8328-17, Session 3

Photoresist strip challenges for advanced lithography at 20nm technology node and beyond

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Introduction

Traditionally, photoresist stacks were purely organic layers patterned over purely inorganic materials. Oxygen based plasmas removed the organic material with near infinite selectivity to the underlying layers. Any remaining residues could then be removed in standard aqueous cleaning chemistries such SPM + APM or RCA cleans. The migration to double patterning, immersion, and multi-layer resist stacks containing silicon or other inorganic elements combined with substrates that are sensitive to oxidation, place constraints on the photoresist removal and subsequent wafer cleaning. This paper will discuss the challenges and options for photoresist strip and re-work for future technology nodes.

Substrate and Junction Oxidation

Plasma oxidation of silicon, silicon-germanium, and other substrates has become an issue for photoresist strip. It is especially true for post ion implant strip, as the ion damage substantially increases the oxidation rate. Studies of the diffusion kinetics also show that oxidation is dramatically increased in the presence of electric fields, through a field enhanced diffusion process. In the absence of fields, oxidation on the order of 10-20Å is typical for an oxygen based strip owing to the fast diffusion of oxygen atoms through the growing oxide. Oxidation of shallow junction regions increases series resistance and is particularly damaging for 3D transistors. Figure 1 shows the change in a FinFET device performance when the strip and clean process oxidizes the extension doping.

Resist Strip Effects on Dopants

At junction depths of several hundred angstroms, surface effects begin to make measureable and sometimes dramatic changes to the dopant profiles, junction depth, activation and resultant resistivity. Significant changes to junction characteristics are observed when the surface is nitrogen versus oxygen terminated. Hydrogen also has shown the ability to dramatically alter dopant profiles and contribute to reduction in dopant activation through several mechanisms which will be described.

Implanted Resist

Ion implantation produces physical and chemical changes to all organic materials. Chain scission, crosslinking, PAG activation, densification and stress, etc, all occur as a result ion implantation, see Figure 2. The transition to zero degree implant angle causes strong dependence on the strip characteristics of the resist and BARC/Underlayer sidewall profile. The strip challenges are magnified in the presence of footing or worse, undercut. Resist and underlayer degradation by implantation effects the thermal stability and can promote resist "popping" during strip.

Multi-Layer Resist (MLR)

MLR rework presents unique challenges. Ideally it is preferred that each layer in the MLR structure can be removed with high selectivity to the layer immediately below it. For MLR structures that are all purely organic, this becomes a near impossibility. For MLR stacks including silicon containing hard masks or films containing amorphous carbon, reasonable selectivity can be achieved provided resist strip sensitive substrate materials are not exposed. Many times however, metals or SiCOH materials are exposed presenting daunting rework challenges.

Resist Strip over High-Aspect Ratio (HAR) Structures.

3D devices, DRAM storage cells, and STI are approaching or in many cases exceeding aspect ratios of 20:1. In advanced DRAM, the requirement to strip through a masking layer which is filling an HAR structure of up to 2μm deep while limiting the change to the cell electrode

resistivity by no more than 5% is extremely difficult. To achieve this requires a selectivity of greater than about 20,000:1.

8328-18, Session 3

Wet clean challenges for advanced lithogrpahy nodes

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No abstract available

8328-19, Session 3

Dry etching challenges for patterning smooth lines: LWR reduction of extreme ultraviolet photoresist

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We have investigated an H2 plasma smoothing process that improves the LER and LWR of the EUV PR at 30 nm half pitch. This process reduces the LWR from ~5 nm to ~3.5, a 30% LWR improvement. EUV PR height, after lithography exposure and plasma smoothing, is lower than 50 nm, provoking a low process window for subsequent etching steps. One strategy to open the process window is to encapsulate the PR with a more resistant material without destroying the lithography pattern. For this purpose a process was developed where 5-7 nm of SiO2-like layer was deposited on top of the PR at low temperature (50 degrees Celsius). TEM cross sections reveal this encapsulation layer: the core of the features is the EUV PR and the layer that surrounds this core is the SiO2-like layer deposited in the etching chamber. The main advantage of this deposited layer is that it is thicker in the top of the feature than in the space between the features. This nanoloading effect is key for opening the dry etching process window for future patterning steps. After the H2 plasma smoothing and the SiO2-like encapsulation, the main challenge is to maintain roughness improvement during the subsequent etching steps, requiring an optimization of the patterning stack and etching steps.

8328-20, Session 3

Self-assembly patterning using block copolymer for advanced CMOS technology: optimisation of plasma etching process

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Block copolymers (BCP), are two chemically dissimilar polymers self-assembled to form dense periodic arrays with dimensions and spacing of domains from ~3 to 50 nm (1) when they are joined together. Their self assembling properties as well as their ability to form well controlled nanostructures is attractive to provide low cost lithographic masks with a resolution beyond the one used today for the manufacturing of integrated circuitry. The aim of this work is to use the block copolymer as masks for silicon and silicon oxide etching by plasma.

We have first evaluated the masking capabilities of Polystyrene-block-poly(methyl methacrylate) (PS-b-PMMA) for pattern transfer into silicon. The polymers employed in this study are synthesised by Arkema. Perpendicular cylinders of PMMA into PS matrix were achieved using specific random copolymers (2). After selective PMMA wet removal, the transfer of PS patterns into silicon was studied using a SiO2 hard mask strategy. Indeed, direct Si patterning using PS as a mask is very challenging due to the PS thickness (<30nm) and fragility. In this work, the new parameters optimization of the BCP mask formation enables to

achieve nano-holes into 60 nm thick PS, i.e. twice thicker than a typical BCP mask (2).

The etching experiments were performed in an industrial ICP chamber (200 mm DPSTM from Applied Materials). The remaining random copolymers layer is opened using Ar/O2 plasma at low source bias power. The thin SiO2 mask (10 to 20 nm) is opened in CF4-based plasma and then the silicon is etched in HBr/Cl2/O2 plasma. The SiO2 mask opening step can be performed using conventional etching plasma while the silicon etching process needs to be revisited to get satisfactory etching profile. The key plasma parameters are the O2 concentration in the plasma chemistry and the source bias power. Indeed very low O2 concentration and high source bias power are required to achieve good profile control of 70 nm deep Si holes. Those results show that new etching mechanisms are observed at the nanoscale and those typical etching mechanisms and processes are not applicable at such small dimensions.

The etching of SiO2 was also investigated using a single masking strategy. The etching experiments were performed in an industrial ICP chamber (200 mm DPSTM from Applied Materials) and in a CCP chamber (200 mm eMaxTM from Applied Materials). The random copolymers is etched in Ar/O2 plasma in the ICP chamber while a typical CF4-based plasma for BARC opening is used in the CCP chamber. The etching of 60 nm deep SiO2 holes is done using CF4-based plasma in both chambers. The main difference in etching profiles is a straighter profile with the ICP chamber. To conclude, results of the transfer of the PS nanostructures in the bulk silicon substrate will be presented with graphoepitaxy approaches.

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8328-21, Session 3

EUV resist curing technique for LWR reduction and etch selectivity enhancement

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EUV lithography provides some etch challenges. Its depth of focus (DOF) is so small that the thickness of EUV resist is much thinner than that of 193-nm resist. Etch selectivity normally attributes to polymer which prevents material from being etched. In the case of EUV resist, line width roughness (LWR) is easily enhanced by polymer because its resist width is so small that the resist cannot tolerate the stress of polymer.

This paper introduces a new technique utilizing a direct current superimposed (DCS) capacitively-coupled plasma (CCP) to enhance the etch selectivity to EUV resist with decreasing LWR. This new technique includes chemical and e-beam curing effect. DCS CCP generates ballistic electrons, which reform chemical structure of photoresist. This surface modification hardens the photoresist (PR), and enhances the etch selectivity. The PR-hardening technique also improves the tolerance towards stress by polymer. Hence, a polymer becomes applicable to protect photoresist, and the etch selectivity increases even more. As a result, this cure can be processed without consuming the thickness of EUV resist. The mechanism of EUV resist cure is discussed based on the surface analysis. In addition to the basic physics of PR-hardening, this paper shows the benchmark results between DCS CCP and the conventional curing techniques by RIE, such as HBr-cure and H2-cure. Several new chemistries were applied to DCS CCP. In consequence, the PR-hardening by DCS CCP achieved 33% reduction in LWR at pre-etch treatment, and 30% reduction during under layer etch with maintaining enough thickness of EUV resist.

8328-22, Session 3

Mandrel and spacer engineering-based self-aligned triple patterning

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Self-aligned triple patterning (SATP) technology, when combined with 193nm immersion lithography, offers both improved resolution and design flexibility for scaling integrated circuits down to sub-15nm half pitch. Recently, the scaling capability of a SATP process was investigated, with final half-pitch CD at about 15nm demonstrated. However, the challenge of etching small and smooth mandrel lines was found to be non-trivial. During the experiment, after the first spacer was released by wet etch, we found some residues left around the mandrel lines. These residues could not be removed by wet etch and consequently degraded LWR of mandrel lines. In addition to the scaling difficulty due to small-mandrel etching, there is still some doubt about the SATP process complexity. Thus, further optimization of SATP process is attractive to compete with several other scaling candidates such as SAQP (self-aligned quadruple patterning) and EUV+SADP schemes. In this paper, we shall present the latest progress made to address above two critical issues: mandrel etching and cost of SATP process. First, we propose the first (sacrificial) spacers should be etched by highly selective dry plasma process which can help to smooth out the high-frequency LWR components related with the residues. Moreover, an etch based shrinking technique is developed to pattern 1x mandrels with good quality using 193nm dry lithography. This shrinking technique, combined with dry etch of the first sacrificial spacers, has proved to be a promising SATP approach to achieve satisfactory 1x (half-pitch) patterning.

Detailed cost analysis of several 1x NAND patterning candidates will also be presented, e.g., 3-mask SATP, 4-mask SAQP, and 3-mask EUV+SADP process (for each NAND critical layer including lines/spaces, pads and peripheral circuits). As SATP technique can relax the overlay spec and reduce the total mask number, our model and calculations show that SATP technique is the most cost-effective solution for 13-18nm half-pitch patterning. On the other hand, EUV+SADP is found to be the most expensive choice and unlikely to catch the insertion point for sub-19nm (e.g., ~16nm) NAND patterning in a timely manner.

8328-23, Session 3

Transfer optimized dry development process of sub-32nm HSQ/AR3 BLR resist pillar from low-K etcher to metal etcher

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New NVM, like RRAM, needs high aspect ratio bi-layer resist pillar pattern to act as etch mask for sub-50 nm cell metal pillar definition. Optimized dry development (DD) condition is obtained in low-k etcher for sake of wider tunable ranges of process parameters previously. The optimized DD condition of low-k etcher is transferred to DPSII metal etcher in this study for avoiding resist pillar collapse, etch residual magnification, process continuity and tool simplicity. The transfer of DD conditions to metal etcher is re-optimized based on the ranges of DPSII process parameters. Three key process parameters of oxygen flow rate, bottom power and e-chuck temperature are studied during the re-optimization for vertical pillar profiles through pattern density.

8328-24, Poster Session

How much further can lithography windows be improved?

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Utilization of thin photoresist layers for successful pattern transfer has gained acceptance as the lithography process of record, primarily due to the incorporation of silicon-containing hardmask layers for added etch resistance. We targeted our work on understanding the impact of incorporating inorganic additives consisting of HfO_2 nanocrystals into hardmask materials.

Our methodology included making nanocrystal dispersions by blending nanocrystals in PGMEA in various weight percent concentration ratios. The nanocrystals were added into polymers for investigating etch resistance and lithography process window capabilities. Conventional 193 nm photoresist and spin-on carbon (SOC) materials were selected as a reference for etching selectivity calculations.

The etching process was optimized to target process conditions that set the hardmask-to-photoresist selectivity in the range of 2:1, and greater than a 30:1 selectivity for hardmask to SOC underlayers.

The results of our work have enabled us to find the best-case nanocrystal-to-polymer ratio required to achieve successful lithography enhancements. Less pattern collapse was observed at the interface of the photoresist and hardmask. Line edge roughness (LER) values of less than 3 nm were measured, and the overall process window increased. See Figure 1.

8328-25, Poster Session

Removal of SU-8 resists using hydrogen radicals generated by tungsten hot-wire catalyzer

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It is well known that removal of the cross-linked SU-8 resists is difficult by conventional resist stripping techniques such as oxygen plasma and ozone ashing, and chemicals (ex. SPM, APM, organic amine solutions). If the cross-linked SU-8 resists can remove, SU-8 resists are available as a template of metal-plating for microelectromechanical systems (MEMS) manufacturing. In this study, we investigated the removal characteristics of the cross-linked SU-8 resists using hydrogen radicals. Hydrogen radicals were generated by the catalytic decomposition of hydrogen molecules in H2/N2 mixed gas (H2/N2=10/90vol.%, total gas pressure =21.3Pa) using a tungsten hot-wire catalyzer which was attached to the vacuum chamber. When catalyzer temperature is 2420 degree Celsius, distance between catalyzer and substrate is 100mm, and average substrate temperature during hydrogen radical irradiation is 177 degree Celsius, SU-8 resists with exposure dose from 0 to 280mJ/cm2 (Dg100×20) were removed at a removal rate of 0.17μm/min independent of exposure dose. When distance between catalyzer and substrate is constant, removal rate was enhanced with rising average substrate temperature. In addition, when average substrate temperature is constant, removal rate was enhanced with decreasing distance between catalyzer and substrate. As a result, we obtained the removal rate of approximately 4μm/min in the SU-8 resist with exposure dose of 14mJ/cm2 (Dg100) when the average substrate temperature is 318 degree Celsius, and distance between catalyzer and substrate is 20mm.

8328-26, Poster Session

Exploration of suitable dry etch technologies for directed self-assembly

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As geometries continue to shrink, the ability to produce a quality pattern for etch has been limited by challenges such as pattern collapse, line edge roughness (LWR) and pattern material thickness. Directed self-assembly (DSA) has shown the potential to replace photoresist for sub-14nm nodes. One of the key challenges for DSA integration is the capability to develop the pattern in the block co-polymer (BCP) to produce a sufficient pattern for the subsequent etch.

This paper will explore the etch technologies suitable for dry development of DSA patterns by a study of benchmark with an inductively-coupled plasma (ICP) and capacitively-coupled plasma (CCP) with varying source frequencies. In this study, PS-PMMA BCP line/space patterns are used. As a result, CCP with very high source frequency (VHF) showed superior pattern development after the BCP etch. The VHF CCP demonstrated minimal BCP height loss and LWR. The advantage of CCP over ICP is the low dissociation so that etch rate of BCP is maintained low enough. On the other hand, the advantage of VHF is the low electron energy with a tight ion energy distribution that enables removal of the PMMA with good selectivity to PS and minimal LWR.

8328-27, Poster Session

Pattern transfer from the e-beam resist, over the nanoimprint resist and to the final silicon substrate

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The nanoimprint lithography is an attractive emerging lithography technology for the patterning of nanostructures. A pre-patterned imprint template is first fabricated normally through E-Beam lithography and plasma etching. Then patterns are created in a resist film through pressing this pre-patterned template into it. These Patterns can then be transferred from the resist film into the substrate through plasma etching. During the whole pattern transfer process, the plasma etching has a very important role. The profile shape, the sidewall roughness and the CD uniformity of the etched patterns influence the total quality of the pattern transfer essentially.

In this work we developed a Fluor-based RIE process for the pattern transfer from the E-Beam resist to the final silicon substrate. First, patterns for the final structures were defined with the E-Beam lithography on a silicon substrate. These patterns were then etched into the silicon substrate with this RIE process. The fabricated silicon template was used as the moulding master for the polymer imprint template (PFPE - Perfluoropolyether). With the nanoimprint lithography, these patterns were transferred in a SU-8 resist film. After the removing of the residual layer with O2-Plasma, these patterns were then transferred into the final silicon substrate with the developed RIE process. We used in this RIE process the SF6 and C4F8 gas in an Etching Tool with an ICP plasma source. The etched silicon patterns have slightly tapered and smooth sidewalls. The roughness of the sidewall is less than 5 nm. The sidewall angle can be controlled between 85° and 90° by varying the ratio of the used gas. The tapered and smooth sidewall enabled the successful pattern transfer in the nanoimprint lithography. This RIE process has a quasi-zero lateral etching rate, so that the dimension of the etched structures in the final silicon substrate is identical with the patterns in the E-Beam resist. With this etching process we demonstrated line structures in silicon substrate down to 50 nm. The etching rate of silicon is about 100 nm/min and the maximal achieved aspect ratio is more than 10. With this RIE process, we realized a perfect pattern transfer from the E-Beam resist, over the nanoimprint resist and to the final silicon substrate.

8328-28, Poster Session

Fullerene-based spin on carbon hardmask

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As lithography resolution requirements have increased to enable '2x nm' devices extremely thin photoresist films have been required to mitigate problems such as resist collapse during development. We have previously demonstrated a high etch durability resist capable of aspect ratios of 5:1 at 25 nm halfpitch [1]. However, even with such a resist, usable resist thickness limits etch depth. The use of a multilayer

hardmask stack allows further increase of the achievable aspect ratio. Typically a thick amorphous carbon layer is deposited by chemical vapor deposition, and then coated with a thin silicon rich layer [2]. A thin photoresist film is then sufficient to pattern the silicon, avoiding pattern collapse issues, and the silicon is used as a hard mask to pattern the carbon giving a high aspect ratio carbon pattern suitable for subsequent etching of the substrate. In order to improve manufacturability it would be beneficial to use spin on hardmasks (both silicon and carbon) [3]. Here we introduce a fullerene based 'spin on carbon' (SoC) with high etch durability.

[6,6]-Phenyl-C61 butyric acid octyl ester was dissolved in chloroform or anisole. Crosslinker was added at 1:1 by weight. Films of SoC were prepared by spin coating on silicon (800-2000 rpm/ 60s). After coating the film was baked for five minutes at up to 330 C. Figure 1 shows the film became insoluble in organic solvents from temperatures above 280 C. Addition of thermal acid generator reduced processing temperature to 190 C. By varying coating conditions and solution concentration, films from 20 to 325 nm could be prepared in a single coating step. Greater thickness could be achieved via multiple coating steps - 1.3 micron films have been prepared by spinning 5 layers. After preparation of a ~300 nm carbon film, a silicon layer of thickness 50 - 65 nm was deposited using sputter coating or PECVD, and resist was deposited on top. Using e-beam lithography resist patterns were produced, and transferred to the silicon thin film using SF6/C4F8 ICP. The carbon layer was etched using O2 plasma. Figure 2 shows the results of transferring a 40 nm linewidth resist pattern to a 300 nm thick spin-on carbon layer via the silicon layer. Figure 3 shows 60 nm linewidth features etched into the silicon substrate from the spin-on carbon layer, with an aspect ratio of 11:1, using SF6/C4F8 ICP. Finally figure 4 shows an array of pillars, diameter 92 nm and height in excess of 1 micron, fabricated in the same manner.

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8328-29, Poster Session

3D modeling of line-edge roughness transfer from the underlying substrate: the effect of resist roughhness

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As the critical dimension of line features is continuously shrinking, Line Edge Roughness (LER) becomes an important fraction of the feature width and thus a candidate factor for degradation of device performance. The LER transfer from the resist to the underlying substrate via the plasma etching step plays an important role in the LER of the final feature and depends on the stack of materials, pre-etch resist LER and plasma chemistry and conditions.1,2 Systematic experimental measurements revealed the critical role of pre-etch resist LER and showed a reduction of substrate LER after plasma etching which becomes greater at large initial resist LER.3 Although several modeling works attempted to explain the main mechanisms controlling LER transfer, the role of the initial resist LER has not been considered in sufficient detail.

In this paper we extend to 3D the abstractive model for LER transfer proposed in our previous works and apply it to whole resist lines.4 In this model, the pattern transfer process is approximated with an anisotropic etching process where the sidewalls of the underlying substrate are determined only by the shadowing of the incident ions by the protrusions of the initial resist sidewall. The simulation starts with the generation of a 3d resist line with rough surfaces: A plane, fractal self-affine surface, whose roughness parameters (rms, correlation length, and fractal dimension) can be varied at will, is imposed on a smooth 3d line. The 3d geometry of the resist line is represented by the zero isosurface of an implicit function produced by the level set method.5 After the generation of the model resist line, the material thickness of the resist above the

underlying substrate is calculated at every position of the substrate. This material thickness, the etching rate of the substrate and the etch selectivity are used to calculate the etched depth at every position of the substrate. Then, the remaining resist is removed and the final outcome is the substrate line.

The first outcome of the simulation is that that shadowing of ions is enough to induce the striations at the sidewalls of the underlying substrate.4 Second, the rms value of the substrate sidewall is calculated as a function of the initial resist sidewall; it is found always lower than the rms of the initial resist sidewall. The absolute value of the difference increases as the rms of the initial resist sidewall increases. Additionally, the rms of the substrate sidewall increases linearly versus the rms of the initial resist sidewall. The latter results are in good agreement with the experimental results reported by Pawloski et al.3